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Carbon nanotube based ion sensitive field effect transistor

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CARBON NANOTUBE BASED ION SENSITIVE FIELD EFFECT TRANSISTOR

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ABSTRACT

Carbon nanotubes (CNTs) have been the subject of much research in the past two decades. Due to their extraordinary mechanical and electrical properties, CNTs are ideal candidates for various sensors and electronic device applications. The purpose of this research is to overcome the difficulties in separating and aligning CNTs so that they can be implemented in an ion sensitive field effect transistor (ISFET). A solution to the alignment process has been presented that involves cutting nano channels on a microelectrode chip with an Atomic Force Microscope (AFM) in order to nanomanipulate the CNTs into the nano channels. Upon successfully cutting the channels, the process of dielectrophoresis (DEP) will be used to align the CNTs into the nano channels. Preliminary work shows that the nano channels are a valid solution for bridging the gap between the electrodes, but they create an entirely new level of complexity. Cutting with an AFM can, at times, be an inconsistent process. Once the inconsistencies are overcome associated with AFM cutting, a carbon nanotube based ISFET device could be manufactured at lower cost and could operate without the need of an amplifier.

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INTRODUCTION

Through this research, it was the goal to apply the ideal properties of carbon nanotubes (CNTs) to an ion sensitive field effect transistor (ISFET). A CNT based ISFET would be beneficial because it would make a smaller device that would not require an amplifier. With the CNTs very high current-carrying capacity, the CNTs would be able to transmit a strong enough signal making an amplifier unnecessary. Eliminating the amplifier has the benefit of freeing up even more space on the chip. The proposed CNT based ISFET can be seen in Figure 1. Single walled carbon nanotubes (SWCNTs) will be used to connect nodes 2 to 3 and 1 to 3. In this situation, the semiconducting CNTs will act as transistors between the nodes. The metallic carbon nanotubes (MWCNTs) will then be used to connect nodes 1 and 2. Because of its metallic properties, the CNTs will essentially act as a nanowire between the two nodes. With the CNT application, the overall size of the device will be smaller and allow for more transistors to fit onto a single chip. Despite the benefits that the CNTs would provide, there is still one major difficulty in implementing this design. The separation and alignment of CNTs is still the topic of much study in the field of nanomaterials. Using the process of dielectrophorus (DEP), CNTs can be deposited and aligned on the surface of the chip. The specific purpose of this research was to assess whether cutting a nanochannel between the tips of the electrodes would result in better

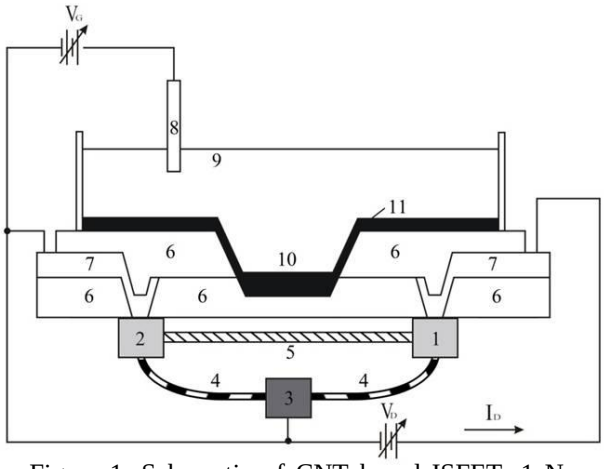

Figure 1: Schematic of CNT based ISFET: 1 N-doped drain; 2 N-doped source; 3 P-type silicone substrate; 4 SWCNT as transistor; 5 MWCNT as nano-wire; 6 insulator; 7 metal contacts; 8 reference electrode; 9 solution; 10 electroactive membrane; 11 encapsulate

performance from the chip. An Atomic Force Microscope (AFM) was used to cut the nano channels. The channels should help to better align the CNTs and ensure that an adequate electrical connection is being made between the two electrodes. After cutting the channels, wires will be attached to the gold (Au) pads located on each electrode. The DEP process will then be carried out to align the deposited CNTs. A multimeter and power supply will then be used to obtain the I-V curve for the electrodes. The I-V curve will then give insight as to whether the CNTs filling the nanochannel exhibit metallic or semi-conductive properties.

LITERATURE REVIEW

Carbon Nanotubes

Carbon Nanotubes (CNTs) are amazing structures that are finding their way into new applications every day. CNTs can be visualized by wrapping a layer of graphene into a hollow cylinder. The diameter of the CNTs depends not only on what type of CNT it is, but also on the way in which it was grown. CNTs come in two types: multi-walled carbon nanotubes (MWCNTs) and single-walled carbon nanotubes (SWCNTs). SWCNTs range in diameter from 1-10 nm. While, MWCNTs normally range in diameter from 10-50 nm [1]. Some of the most useful properties of CNTs pertain to their conductivity. 70-80% of SWCNTs exhibit semi-conductive properties. On the other hand, 70-80% of MWCNTs exhibit conductive properties [1]. CNTs also have an extremely high current-carrying capacity of approximately 1 TA/cm3. The very large current-carrying capacity makes CNTs great candidates for use in wire and cables [2]. Along with the extraordinary electrical properties, CNTs have great mechanical properties as well. The Young's modulus of CNTs is approximately 1 TPa. This is extraordinary compared to even that of steel which has a Young's modulus of approximately 0.2 TPa. CNTs also have a tensile strength of approximately 45 GPa [2]. Overall, the great electrical and mechanical properties that CNTs possess make them ideal candidates for implementation into many different applications.

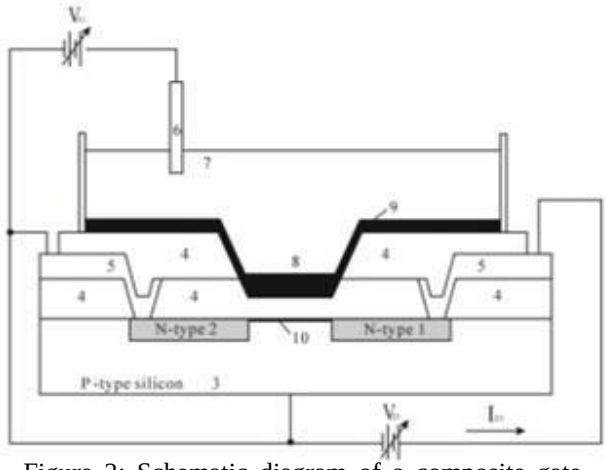

Figure 2: Schematic diagram of a composite gate, dual dielectric ISFET: 1 drain; 2 source; 3 substrate; 4 insulator; 5 metal contacts; 6 reference electrode; 7 solution; 8 electroactive membrane; 9 encapsulant; 10 inversion layer.

Ion Sensitive Field Effect Transistor

Ion Sensitive Field Effect Transistors (ISFETs) are transistors that measure ion levels in a liquid. When the ion concentration in a fluid changes, the current through the transistor will change. The change in current is amplified and translated into an output. The basic diagram of an ISFET is shown in Figure 2. Because of its design, ISFETs are often applied to pH measurement applications.

Dielectrophoresis

Dielectrophoresis is a process by which neutral particles can be aligned, moved, or separated in a supporting medium. The principle behind the DEP process is the creation and application of a non-uniform electric field. The Dielectrophoresis force created by the non-uniform field can be changed by varying the supporting medium, frequency of the electric field, or the conductivity and permittivity of the particles [5].

CHIP FABRICATION

Before microelectrode fabrication could begin, the design of a mask is required. The mask utilized was designed in AutoCAD by Zhuxin Dong. The mask consisted of 24 chips placed on a single 125 mm diameter silicon wafer. As can be seen in Figure 3, triangular tipped electrodes were utilized on the mask. The reason for this is that it will provide a more concentrated zone for the DEP force to act. Each chip contained nine pairs of electrodes that ranged in triangular angles of 30, 60, and 90 degrees. The gap sizes between the electrodes varied between one and fifteen microns. The mask also utilized a one micron resolution for precise gap distances. Following the construction of the mask, the next step is microelectrode fabrication. The microelectrode fabrication for this research was completed by Zhuxin Dong with the assistance Holly Tourtillott, at the High Density Electronics Center (HiDEC). The general process for the fabrication of a microelectrode chip can be seen in Figure 4. Beginning with a silicon wafer, silicon dioxide was added to the wafer by thermal oxidation. The process of thermal oxidation involves using very high temperatures of approximately 1100 C to promote the growth of a silicon oxide layer on the chip [4]. The silicon oxide layer itself

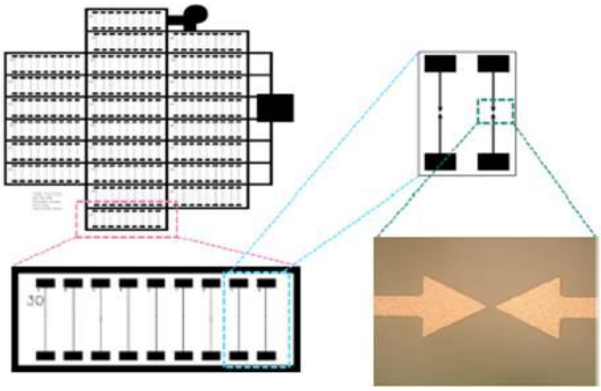

Figure 3: Mask design and Au microelectrodes on Si substrate.

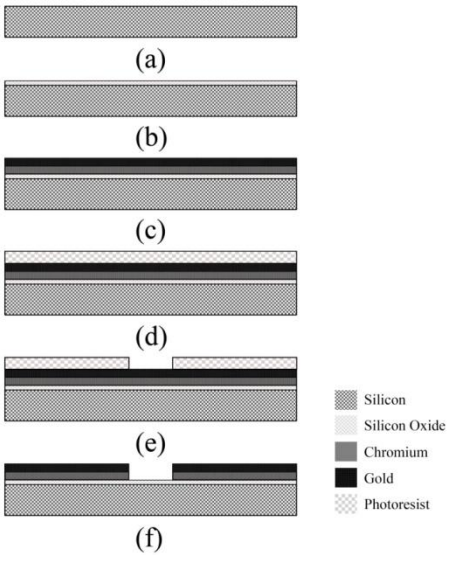

Figure 4: Fabrication process of the microelectrode. (a) is the silicon substrate, (b) the silicon-oxide is added, (c) the chromium and gold are deposited, (d) the photoresist is applied, (e) the pattern is constructed, (f) the photoresist is removed and the microelectrodes are fabricated.

acts as an insulator. The next step is the addition of a chromium layer adhered through the process of evaporation. The chromium layer acts as an adhesive for the gold. Gold is then deposited onto the wafer. The final step, in the microelectrode fabrication process, is the photolithography process. Using the previously mentioned electrode mask, the photolithography process can be completed in four steps: application, exposure, development, and inspection. Because of the etching process, the lines created were not completely true to the mask that was created. This variance means that the electrode gap size would have an error percentage between ten and fifteen percent. The slightly larger than expected gap size should not have an effect on the experiments that the chip will be used for. The following two chips were selected based off of their reported gap size and angle: 60 degree with a 1 μm gap size and 90 degree with a 1 μm gap size.

EXPERIMENTAL PROCEDURE AND EQUIPMENT

Atomic Force Microscope

Cutting a channel on the nanoscale level involves the use of an Atomic Force Microscope (AFM). The specific AFM used for this application is the Agilent 5500 Inverted Light Microscope. This microscope has numerous applications and modes. To cut the channels we will make use of the microscope's contact mode and large scanner. The large scanner has a resolution of 90 µm, but for the purpose of the experiment a resolution of 50 µm was utilized. The scanner can make use of various nose cones, but for the cutting application the alternating current nose cone was used.

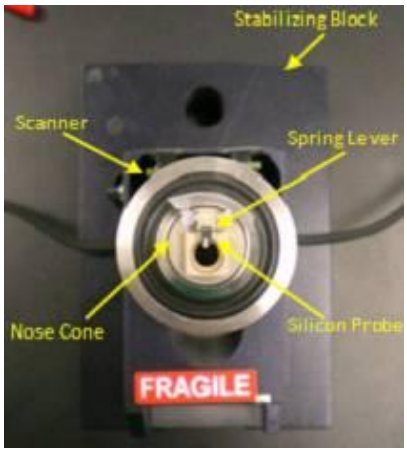

Figure 5: AFM large scanner assembly.

The nose cone is pushed into the underside of the scanner. An important consideration when using the AFM is which specific tip will be used. The tip used varies depending on the properties of the material being cut or examined. Because of the extremely hard surface on the chip, the use of the TAP190DLC tip was necessary. DLC refers to diamond like carbon which is the coating material for the tip. The tip has a resonance frequency of 190 Hz and a spring constant of 48 N/m. After placing the tip into the nose cone, the scanner assembly is complete and can be seen in Figure 5. After completing the hardware setup for the AFM, the focus was shifted to implementing the software. PicoView 1.4 is the name and version of the software used to communicate with the AFM. PicoView 1.4 was already setup and configured to work with not only the selected nose cone but also the TAP190DLC tip. Despite already being set up for the hardware in use, it was still necessary to ensure that the laser was on the tip and that the deflection and friction settings were within specifications.

The calibration, for the AFM, dictates that the deflection should be approximately -0.7 while the friction should be as close to zero as possible. Once the AFM was configured, it was necessary to place the selected chip on the AFMs sample holder. After the sample was loaded and the machine had approached, it was necessary to first scan the chip. The image was then loaded into the PicoLITH software. The PicoLITH software is an application available from the controls tab in PicoView 1.4. PicoLITH is the program that actually allows the cutting of a channel on the nanoscale level. PicoLITH allows the user to specify tip speed and also the number of cuts to be performed. The setpoint is another important parameter that needs to be set for cutting. The setpoint ranges between -10 V and 10 V. For this experiment, the setpoint was set a value of 7.5 V. Add this information as well.). After testing some areas on the chip that did not contain electrodes, it was determined that the experiment would utilize a 3 µm/s tip speed. Test cuts were performed at 100, 150, and 200 passes. It was determined that 150 cuts would give the desired depth and diameter.

Dielectrophoresis

To generate DEP forces, the use of an AC power supply is necessary. Connecting the power supply to the electrodes requires that wires be attached to the gold (Au) pads on the chip. Initially, soldering was attempted to attach the wire to the Au pad. Multiple attempts proved to be unsuccessful, because the solder did not seem to bond to the chip. It was then decided that conductive epoxy would be the best method to attach the wires. The two components of the epoxy were mixed together with a ratio of 1:1 and allowed to setup for one minute. A small amount of epoxy was then applied to each Au pad, and the wires were gently placed into the mixture. Particular attention was paid to ensure that the epoxy for one electrode did not

Figure 6: Heat plate for wire bonding.

touch the epoxy on the next. If two electrodes where to touch each other, the data obtained during the I-V testing could possibly be affected. Next, the chip, with all of the wires, was placed on a hot plate as shown in Figure 6. The epoxy was heated at 130°C for 1 hour to allow it to harden up and firmly hold the wires in place. Before power can be supplied to the chip, it is necessary to deposit the carbon nanotubes onto the chip. Two different solutions were used during the DEP process. For electrodes 1 – 4, a 1.5 µL 10X dilute of SWCNTs was used, and for electrodes 5 – 9, a 1.5 µL 10X dilute of MWCNTs was used. The 10X dilute represents a solution that contains a CNT concentration of approximately 0.02 g/L. Using a droplet with a range of 0.5 to 10 µL, a 1.5 µL drop of the CNT solution was placed in the gap between the electrodes. A sinusoidal function generator was used to supply AC power at a frequency of 1.5 MHz at a voltage of 20 V P-P. An oscilloscope was used to confirm that the desired specifications from the function generator had been met.

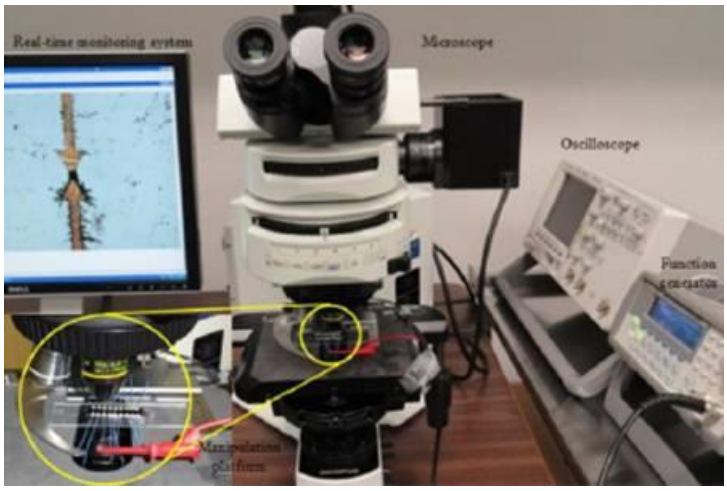

Figure 7: Experimental setup for DEP application.

Figure 7 shows an overview of the testing apparatus. The optical microscope was connected to a computer which allowed for real time monitoring of the DEP process. The

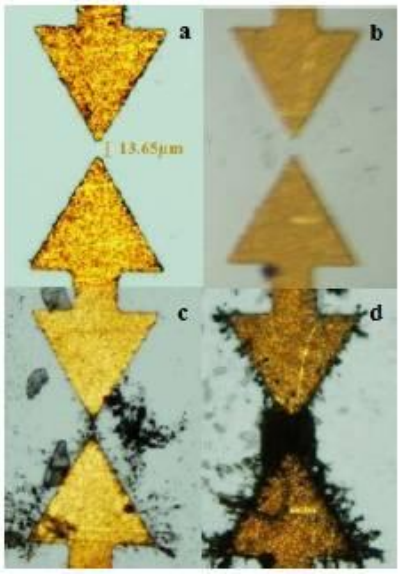

Figure 8: Pairs of Au electrodes observed by optical microscope: a. gap measure; b. covered by tiny CNT droplet; c & d. bridged by SWCNTs and MWCNTs respectively.

final step in the DEP process was to connect the power supply to the chip. Figure 8 shows an image of the CNTs bridging the gap between the two electrodes.

I-V Testing

I-V testing is used to determine whether the MWCNTs and CWCNTs used during the DEP process exhibit metallic or semi-conducting properties. A DC power supply is used to supply a voltage to the electrodes ranging from 0 V to 10 V in 1 V increments. A multimeter is used to measure the current through the electrode at each voltage setting. The testing procedure was repeated multiple times to ensure accurate readings.

RESULTS

Chip 1 Scratching: 60º Electrode, 1 µm Gap Size

For the first cut, the starting point was placed right on the tip of the electrode to the left and the end point was placed on the tip of the electrode on the right. All of the settings were double checked and the "Go" button was clicked to begin the cutting process. After the process had finished, the area was rescanned to view the cut that had just been made. The result that appeared on the screen was not what was expected. After examining the cut using the arbitrary line tool, the conclusion was made that because of the length of the cut, material from the channel was building up and creating high spots. An enlarged image of the issue with the cut can be seen in Figure 9. After a bit of deliberation, it was decided that cutting in the vertical direction may help eliminate the issue of build up while cutting. The process for placing the chip and approaching with the AFM was then repeated with the chip rotated to allow for cutting the electrodes in the vertical direction. After scanning the surface, the image was again loaded into PicoLITH. The same settings were used for the vertical cut as they are the horizontal cut. Upon the completion of the cut, the results were still not what was expected. Even though the cut was specified to go from one electrode to the other, it only cut half of the distance. Another cut was attempted, and the same thing happened again. To allow for the continuation of the experiment, it was decided that a distance twice of what is necessary would be specified. After doubling the cut length, the cut was finally successful. A continuous smooth channel was cut from electrode to electrode. Following the success, cuts were performed

Figure 9: Failed horizontal channel.

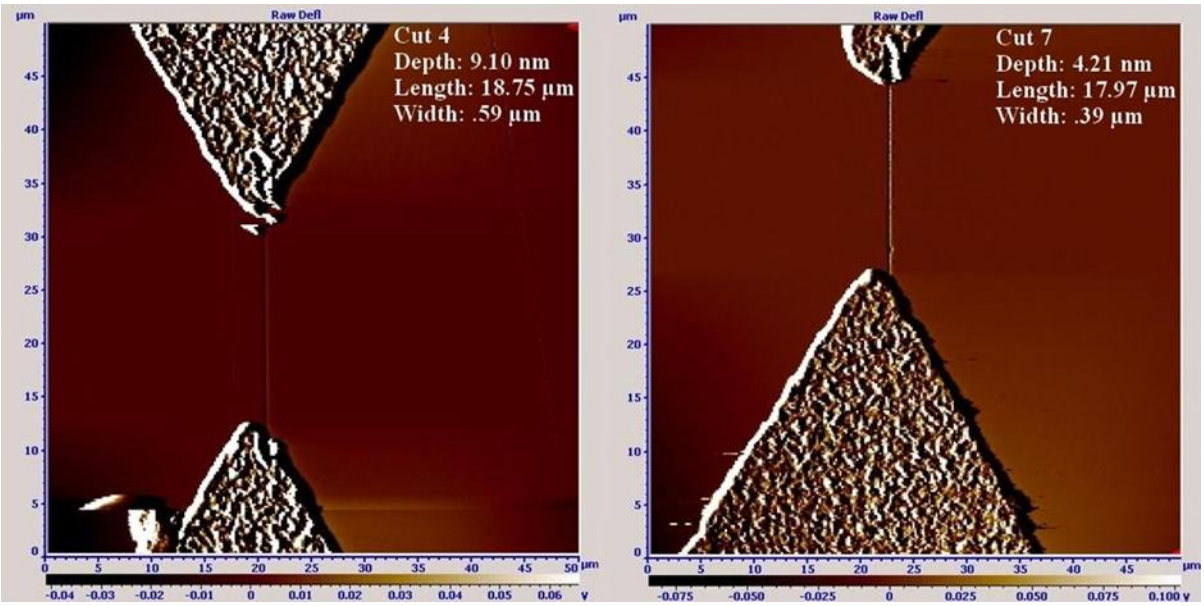

Figure 10: Electrodes 4 and 7 completed channels.

on the remaining seven electrode pairs. Electrode pair number five was skipped due to a defect that occurred during the manufacturing process. The two best cuts can be seen in Figure 10. Following each cut that was made, data was collected on the depth, length, and width of each channel. A three dimensional image of one of the cuts and electrodes is shown in Figure 11.The average depth was 6.0 nm with a standard deviation of 5.32 nm. The average length was 19.42 µm with a standard deviation of 1.48µm, and finally the average width was 0.50 µm with a standard deviation of 0.15 µm. Overall the lengths and widths were fairly consistent, but the depths ranged from 1.8 nm to 16.8 nm. A complete table with all of the nanochannel measurements can be seen in Appendix A.

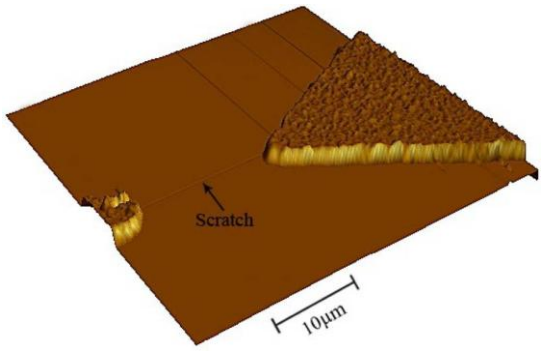

Figure 11: 3D view of electrode 7.

Chip 1 I-V Measurements: 60º Electrode, 1 µm Gap Size

All of the data obtained during the I-V testing can be seen in Appendix B. As previously mentioned, MWCNTs were used in the DEP process for electrodes 1-4. The result of the I-V testing can be seen in Fig. 12. The linear relationship between current and voltage shows that the CNTs exhibit metallic properties.

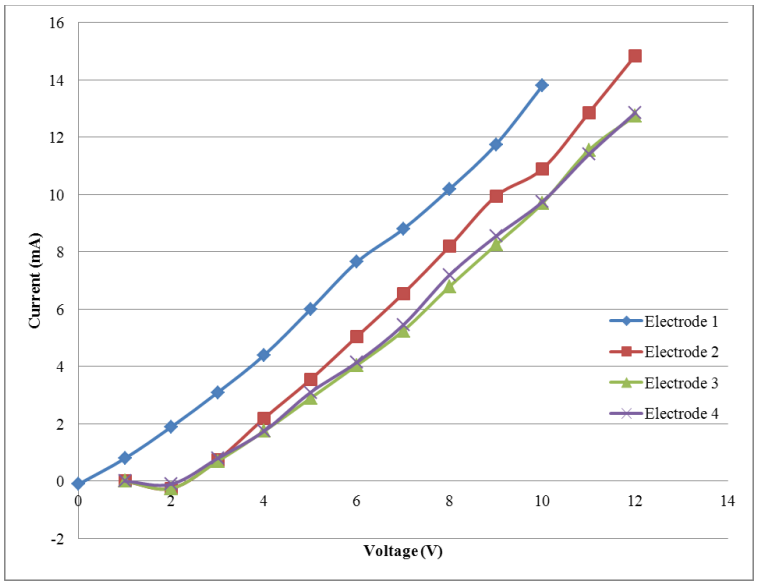

Figure 12: MWCNTs I-V measurements.

Electrodes 6-9 were tested with SWCNTs. Just as with the MWCNTs, a linear relationship between current and voltage was present. The maximum value was not as high with the SWCNTs as shown in Fig. 13, but the metallic property is still present.

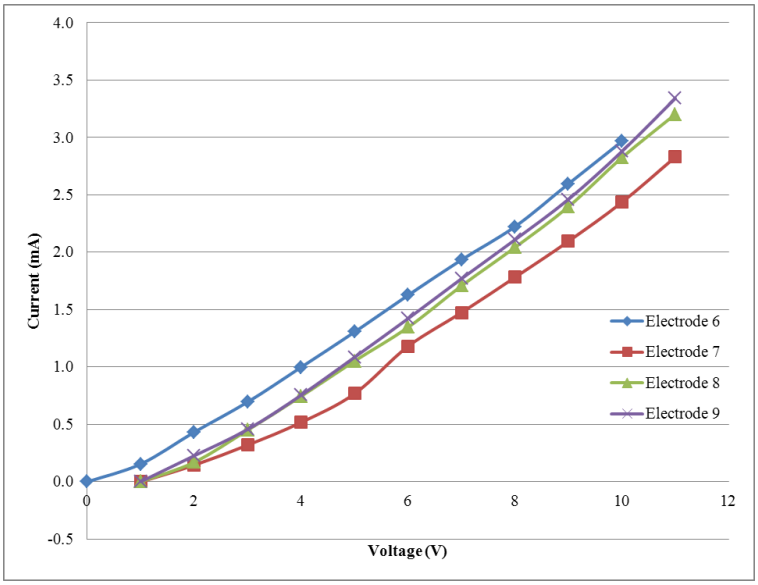

Figure 13: SWCNTs I-V measurements.

Chip 2 Scratching: 90º Electrode, 1 µm Gap Size

Because of the inconsistencies in the first chip on gap sizes, it was decided that for chip 2, a 1 µm gap would again be selected. The 90º chip was selected specifically to see whether the angle of the electrodes would improve the performance of the chip. A preliminary cut was performed on the chip to determine whether the same difficulties in chip scratching were going to be present. After multiple tests, it was concluded that the systematic error present during the scratching of the first chip had been replaced with a random error. Despite numerous trials, a calibration for the error could not be determined. Agilent was contacted concerning the error, and it was suggested that the lab upgrade the software, for the AFM, from PicoView 1.4 to PicoView 1.8. The new PicoLITH uses a different method to locate the tip on the sample, but it still did not help with the scratching problem. Numerous other chips were tested to ensure that this was not an isolated problem. All other tested specimens displayed the same result. Tests were then performed using a shorter cut length. It was determined that for cuts less than 5 µm, a reliable channel could be created.

FUTURE WORK RECOMENDATIONS

Based off of the discoveries from chip 2, the next step in the CNT based ISFET research should be the construction of a new chip. The mask has been examined, and it shows true to the required specifications. The microelectrode fabrication has an attributed error to it, but there still seems to be something else that has caused the gap sizes on the chips to be out of range. After the completion of a new chip, with reasonable gap sizes, testing can continue on the numerous types of chips. Analysis can be done to determine whether certain electrode angles work better than others. Another topic that needs to be addressed is the close-loop function in PicoLITH. The close-loop function was recommended by Agilent while dealing with PicoLITH application. It provides the user with a much more accurate control during nanomanipulation of the AFM probes. Therefore, it should help to improve the performance of cutting nanochannels.

ADDITIONAL WORK IN THE FIELD OF NANOMATERIALS

A research study of the environmental effects on vertically-aligned carbon nanofibers (VACNFs) was also conducted. The purpose of this study is to watch and record how different temperatures affect the height and diameter measurements of carbon nanofibers. For this experiment, two chips, one etched and one unetched, each containing nine arrays will be used. From those nine arrays, ten measurements will be taken at a specified temperature and a constant relative humidity of 10%. The study hopes to eventually cover the entire range from -90°C to 190° in increments of 5°C. At this point in time, only about half of the data has been collected for both chips and very little of it has been analyzed. What has been analyzed those conforms to the previously conceived theory. With higher temperatures, the height will go down, but the diameter will increase. Also, the preliminary numbers show that the average height on the etched chip is higher than that of a corresponding temperature of the unetched chip. Data collected from 30°C for both the etched and unetched chip can be seen in Appendix B. This once again conforms to theory, because of the acid wash that the etched chip is subjected to. The acid wash removes part of the silicon-oxide layer on the chip thereby allowing more of the fiber to be seen. The purpose of this study and how it relates to the CNT based ISFET design is that there is the possibility of using CNFs in an ISFET design. An even more interesting prospect is the thought of being able to grow the CNFs into a specific location on a chip or other device. Through this environmental effect study that may at one point be a possibility. The use of CNFs would create an even smaller device for use in even more applications.

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APPENDICES

A: Chip 1 Nanochannel Measurements: 60º Electrode, 1 µm Gap Size

Nanochannel Measurements			
Electrode Pair	**Length (µm)**	**Width (µm)**	**Depth (nm)**
1	17.32	0.58	2.80
2	21.88	0.39	2.10
3	18.16	0.59	4.90
4	18.75	0.59	9.10
6	21.09	0.78	3.40
7	17.97	0.39	4.21
8	18.95	0.39	16.80
9	19.14	0.39	1.80

B: I-V Measurements: 60º Electrode, 1 µm Gap Size

Measured Data										
Test	**Voltage (V)**	**Electrode 1 (mA)**	**Electrode 2 (mA)**	**Electrode 3 (mA)**	**Electrode 4 (mA)**	**Electrode 5 (mA)**	**Electrode 6 (mA)**	**Electrode 7 (mA)**	**Electrode 8 (mA)**	**Electrode 9 (mA)**
	0	0.000	-0.300	-0.200	0.000	-0.100	-0.002	-0.002	-0.001	0.001
	1	0.800	0.800	0.600	0.800	-0.100	0.088	0.085	0.112	0.220
	2	1.700	2.200	1.400	1.700	-0.100	0.406	0.221	0.434	0.454
	3	3.100	3.600	2.300	3.100	0.000	0.664	0.369	0.720	0.754
	4	4.200	5.000	3.400	4.100	-0.100	0.960	0.539	1.025	1.091
1	5	5.600	6.400	4.400	5.400	-0.100	1.274	1.122	1.322	1.424
	6	7.300	8.300	5.700	7.100	-0.100	1.604	1.403	1.683	1.771
	7	8.200	10.100	7.200	8.700	-0.100	1.909	1.717	2.023	2.112
	8	9.500	10.800	9.000	9.800	-0.100	2.194	2.072	2.398	2.443
	9	10.800	12.800	11.300	11.400	-0.100	2.556	2.423	2.827	2.905
	10	13.100	15.200	12.300	12.800	-0.100	2.951	2.851	3.189	3.369
	0	-0.200	-0.200	-0.300	-0.200		0.000	0.000	0.001	0.001
	1	0.800	0.700	0.800	0.800		0.221	0.204	0.228	0.233
	2	2.100	2.200	2.100	1.800		0.458	0.418	0.466	0.459
	3	3.100	3.500	3.500	3.100		0.726	0.665	0.769	0.754
	4	4.600	5.100	4.700	4.200		1.036	0.996	1.079	1.080
2	5	6.400	6.700	6.100	5.500		1.336	1.238	1.369	1.420
	6	8.000	8.100	7.900	7.300		1.647	1.545	1.732	1.768
	7	9.400	9.800	9.300	8.400		1.960	1.845	2.061	2.105
	8	10.900	11.000	10.400	9.700		2.252	2.118	2.395	2.479
	9	12.700	12.900	11.800	11.400		2.636	2.448	2.822	2.852
	10	14.500	14.500	13.200	12.900		2.981	2.809	3.217	3.314

C: Vertically Aligned Carbon Nanofibers: 30°C And 10% Relative Humidity

Vertically Aligned Carbon Nanofibers: 30°C And 10% Relative Humidity				
	Etched		**Unetched**	
	Average Diameter (nm)	**Average Height (nm)**	**Average Diameter (nm)**	**Average Height (nm)**
Array 1	143.67	8.63	125.82	8.63
Array 2	114.62	10.8	132.19	7.11
Array 3	136.57	11.69	134.76	7.8
Array 4	131.69	14.55	129.22	7.81
Array 5	132.69	8.74	128.21	6.27
Array 6	102.51	9.64	127.89	6.35
Array 7	133.76	14.44	124.66	6.6
Array 8	128.97	8.22	130.13	7.46
Array 9	123.13	11.18	124.71	6.87
Average Array Diameter (nm):	127.51		128.62	
Average Array Height (nm):	10.88		7.21	