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Encapsulated 2D Materials and the Potential for 1D Electrical Contacts

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Encapsulated 2D Materials and the Potential for 1D Electrical Contacts

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by

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1. Abstract

The utilization of two-dimensional materials and heterostructures, particularly graphene and hexagonal boron nitride, have garnered significant attention in the realm of nanoelectronics due to their unique properties and versatile functionalities. This study focuses on the synthesis and fabrication processes of monolayer graphene encapsulated between layers of hBN, aiming to explore the potential of these heterostructures for various electronic applications. The encapsulation of graphene within hBN layers not only enhances device performance but also shields graphene from environmental contaminants, ensuring long-term stability. Experimental techniques, including mechanical exfoliation and stamp-assisted transfer, are employed to construct three-layer stacks comprising hBN-graphene-hBN. The fabrication process involves the formation of one-dimensional edge contacts on graphene, addressing challenges related to contact resistance and interface contamination. The investigation highlights the advantages of edge contacts, such as reduced contact resistance and improved device performance, attributed to the covalent bonding between metal atoms and graphene edges. Computational modeling and experimental data support the effectiveness of edge contacts in graphene-based devices.

2. Introduction

Efforts to harness the full potential of 2D materials and heterostructures are characterized by the need to overcome various manufacturing challenges and achieve compatibility with established semiconductor processes. Historically, the semiconductor industry has focused on improving the performance of conventional bulk materials, but imposed limitations, such as size, weight and manufacturing constraints, have underscored the urgency for alternative solutions. This has led to a surge of interest in 2D materials and heterostructures, driven by their ability to address these challenges while offering unprecedented functionality and versatility. Recent research efforts have repeatedly demonstrated the feasibility of utilizing 2D materials, such as graphene and hexagonal boron nitride (hBN), in heterostructure construction. The development of encapsulated heterostructures is particularly significant. This involves multiple layers of 2D materials with complementary properties being stacked together to create a more complex electronic system. The primary focus of my research is the encapsulation of monolayer graphene between layers of hBN.

2.1 Review of 2D Materials

The physics behind 2D materials encompasses a range of phenomena arising from their unique structure and properties. Two-dimensional materials typically involve atoms arranged in a two-dimensional plane with weak van der Waals forces holding adjacent layers together. This allows for the isolation of individual layers through techniques like mechanical exfoliation.

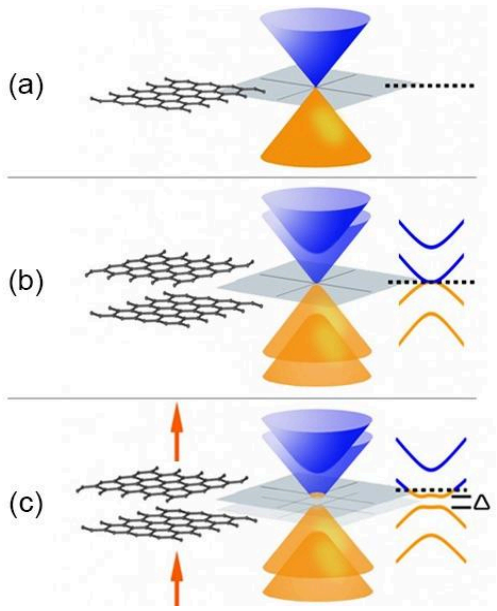

*Figure 1. Single-layer graphene **(a)** lacks a band gap due to the convergence of its conduction and valence bands. Similarly, symmetrical bilayer graphene **(b)** also lacks a bandgap. However, applying electrical fields to the bilayer structure **(c)** induces asymmetry, resulting in the formation of a tunable bandgap [1].*

Single-layer materials can exhibit attractive mechanical, electrical, and thermal properties. [2]. Heterostructures often combine various two dimensional materials to engineer new electronic and optical properties, offering increased control over material properties and certain device functionalities. Materials such as graphene and transition metal dichalcogenides (TMDCs) have tunable band gaps, adjusted by altering the number of atomic layers in the material [2]. This occurs due to the electronic structure of these materials, which is highly sensitive to the thickness or the number of layers comprising the structure. As the number of atomic layers changes, the electronic properties, including the band gap, are modified accordingly.

2.2 Graphene and hBN as 2D Materials

Graphene is a flat, two-dimensional sheet characterized by sp^2 hybridized carbon atoms bonded in a hexagonal pattern. It stands out among other nano-carbon materials due to its exceptional electron mobility, high thermal conductivity, mechanical strength, chemical stability, large surface area, and transparency to light [3]. Many characteristics of graphene arise from the combination of its unique dimensionality and its distinctive electronic band structure, where electrons behave akin to relativistic particles [4]. This property results in graphene's electrons acting as massless Dirac Fermions, implying that they appear to have shed their rest mass while retaining their fundamental particle properties [5]. Other studies have observed the cyclotron mass m_c of massless carriers in graphene described by the equation

$$E = m_c c^2 \text{ [4].}$$

Furthermore, graphene's valence and conduction bands merge at a singular point, resulting in a minimal number of electronic states close to the Fermi level as shown in Figure 2. Therefore, graphene is often called a semimetal or a semiconductor with zero band gap [5]. Due to these properties, graphene and a diverse range of graphene-based nano-hybrids have been created and employed in numerous practical applications across different sectors, including electronics, biomedical technology, sensor development, energy storage solutions, and environmental initiatives [3].

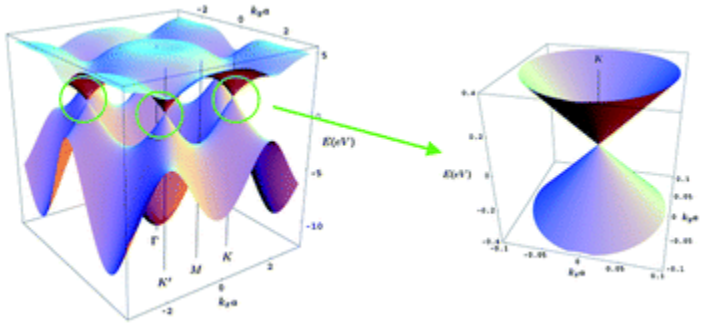

Figure 2. Three dimensional representation of graphene's electronic band structure. The region near the Fermi level in one K point has been enlarged on the right. Two cones touching at a single point can be clearly seen here [5].

Hexagonal boron nitride in its 2D form consists of hexagonal arrangements of Boron and Nitrogen atoms, forming covalent sp^2 bonds and sharing a lattice constant quite similar to graphite, just 1.8% longer. Due to its planar configuration, hBN splits into an extremely flat surface, and its covalent bonding structure typically results in a surface devoid of dangling bonds and charge traps [6]. Additionally, this material exhibits exceptional resistance to mechanical forces and chemical reactions alongside a substantial band gap in the UV spectrum. Due to these properties, hBN is preferred as a substrate or encapsulating material for 2D stacked devices [2]. This material acts as an insulator with a band gap of approximately 6eV [7]. This characteristic makes it highly desirable as a foundational element for creating electronic devices. Additionally,

hBN substrates minimally affect the band structure of graphene near the Dirac point while significantly enhancing the mobility of graphene devices [2].

3. Synthesis

This research utilizes the synthesis technique of mechanical exfoliation from a bulk material for both graphene and hBN. This method, pioneered by Novoselov et al., was originally designed for exfoliating graphene. It involves obtaining thin flakes through micromechanical cleavage, which can be further cleaved into progressively thinner samples, ultimately yielding few-layer and even single-layer graphene.

3.1 Exfoliation

The process begins by placing a small graphite or BN sample onto the surface of adhesive tape and layering another piece of tape on top. Separating the two pieces of tape selectively cleaves the flakes along the crystal plane, leaving atomically flat surfaces exposed. Repeatedly layering and peeling apart these two tape layers leads to further cleavage and thinner flakes. This iterative process continues until the desired thickness is achieved, with each repetition yielding thinner sheets of the material.

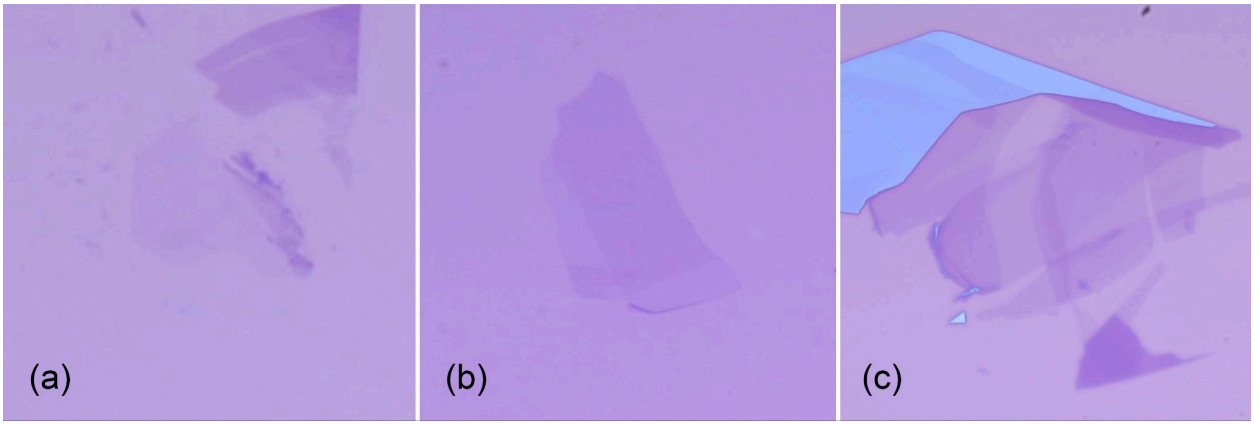

Figure 3. *Monolayer graphene flake.* ***(a)*** *Isolated few-layer graphene.* ***(b)*** *Graphene in a variety of thicknesses. Color becomes more opaque as flake thickness increases.* ***(c)***

Subsequently, the exfoliated flakes are pressed onto a substrate, typically SiO_2 coated silicon. Before transferring graphene or hBN onto silicon chips, the chips undergo a cleaning regimen to ensure minimal debris is present during the transfer. The chips are soaked in acetone for ten minutes, followed by a rinse with isopropyl alcohol (IPA) and subsequently soaked in IPA for an additional five minutes. An optional but beneficial step involves subjecting the chips to an O_2 plasma treatment that effectively etches away any residual contamination from the surface. The inclusion of this step exhibits preliminary indications, albeit inconclusive, of enhancing the yield of viable flakes with larger surface areas. Other studies, including that of Huang et al., indicate more definitively that oxygen plasma treatment consistently produces larger flakes of

graphene [8]. The plasma eliminates organic adsorbates from the substrate, enhancing the adhesion forces between the outermost surfaces in contact with a substrate.

The silicon chips are then heated, while still in contact with the tape, to 100°C for two to four minutes, depending on the stickiness of the tape and the material being exfoliated. The chips are removed from the heat and allowed to cool to room temperature. They are then removed from the tape and put through another cleaning process to remove adhesive residue and other impurities in preparation for device fabrication.

3.2 Alternative Methods for Graphene Synthesis

Alternative methods of preparing graphene include electrochemical exfoliation, chemical vapor deposition (CVD), and epitaxial growth [3]. During electrochemical exfoliation, ions from the electrolyte intercalate into the target material, causing it to expand and break apart. A recent method involves compressing graphite flakes in a permeable container, allowing continuous exfoliation. There are two types of electrochemical exfoliation: anodic and cathodic. Anodic exfoliation occurs by inserting anions into the material, weakening the interlayer bonds, and releasing gas to separate the layers. Cathodic exfoliation inserts cations into the material, which expands the layers and creates space for further insertion. Factors like solvent properties and voltage affect the exfoliation process and the quality of the resulting material [9]. Electrochemical exfoliation offers several benefits as compared to alternative synthesis methods. These advantages include a rapid synthesis time, a straightforward production process, cost-effective equipment, and capability to produce and adjust high-quality graphene [3].

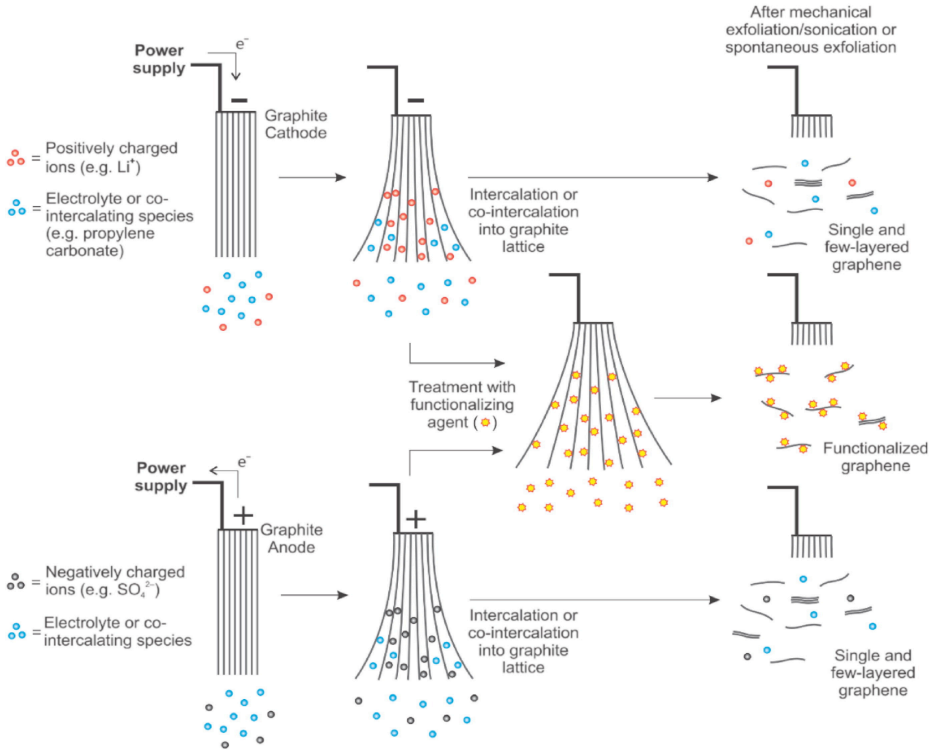

Figure 4. Schematic overview of cathodic and anodic exfoliation mechanisms [10].

CVD and epitaxial growth are both methods of producing graphene from non-graphitic sources [11]. CVD is a widely used, inexpensive method for producing high-quality graphene in substantial quantities. This technique is a bottom-up approach that involves synthesizing graphene by depositing carbon-containing vapors, like CH_4 and H_2, onto metal or dielectric surfaces. Graphene can also be obtained by separating carbon from metal/carbon solutions [3]. In the CVD process, gasses are introduced into a reactor and directed through a hot zone. Within this zone, hydrocarbon precursors break down into carbon radicals upon contact with the heated metal surface. These carbon radicals then assemble to form single-layer and few-layer graphene. The metal substrate acts as a catalyst to facilitate the reaction by reducing the energy barrier and influencing the mechanism of graphene deposition, thereby impacting the final quality of the graphene produced. [12]. The most common substrates used are copper and nickel [11].

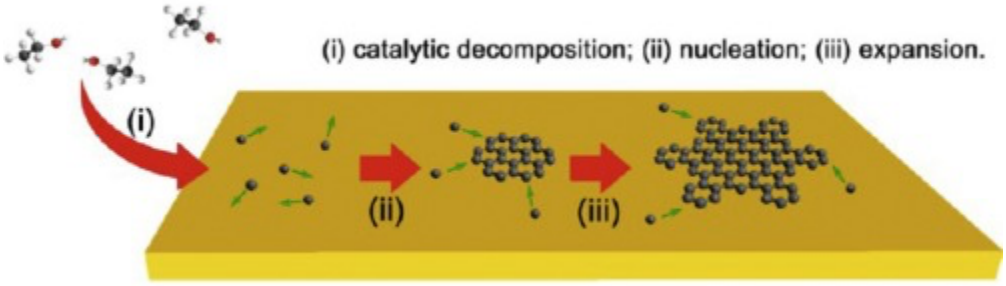

Figure 5. CVD graphene grown on metals with high carbon solubility [13].

Epitaxial growth of graphene relies on the thermal decomposition of silicon carbide (SiC) substrates. By heating the SiC surface to high temperatures in ultra-high vacuum conditions, silicon atoms sublime, leaving behind a carbon-rich surface. The rearrangement of carbon atoms into a hexagonal lattice forms the graphene layer, but challenges lie in controlling layer thickness, quality, and uniformity [14].

4. Identification

The most time-consuming aspect of graphene synthesis is identifying single or few-layer flakes. For this research project, identification is accomplished using optical microscopy and requires considerable patience. As graphene flakes get thinner, they become more transparent, making monolayer flakes of graphene difficult to identify against a substrate. Potentially useful flakes can be more efficiently identified if graphene sample chips are thoroughly cleaned after exfoliation. Pristinely clean surfaces are also necessary for a successful three-layer heterostructure assembly.

4.1 Cleaning Process

For optimal identification and stacking conditions, the exfoliated sample is immersed in acetone for two hours, followed by a soak in IPA for 30 minutes to an hour, contingent upon the

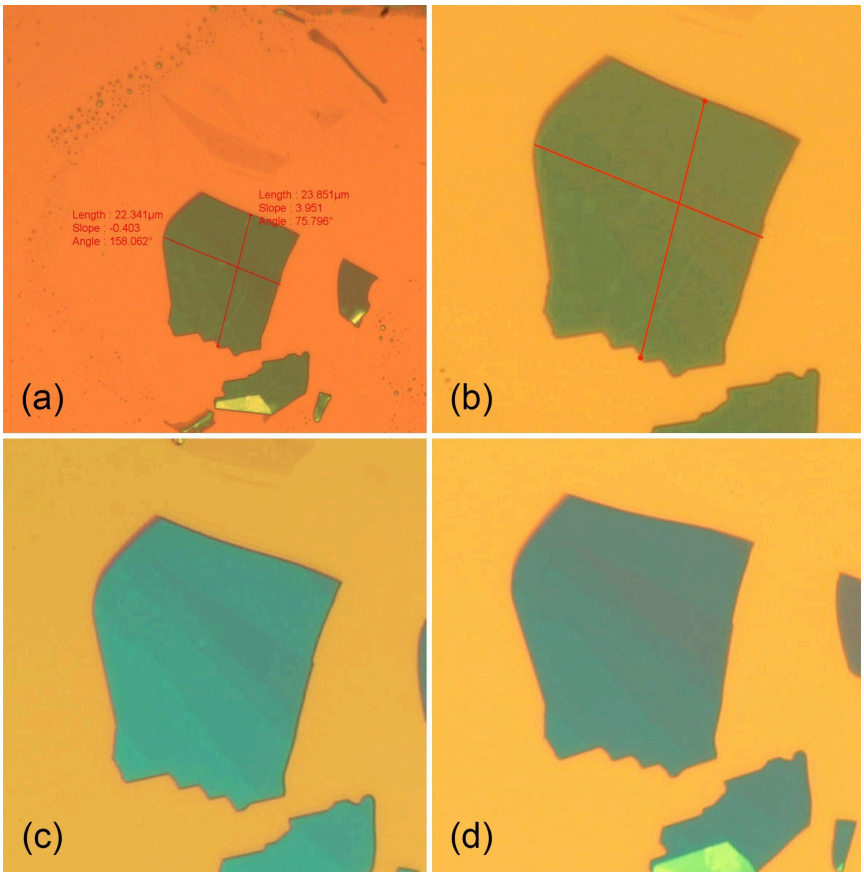

Figure 6. *hBN flake and its immediate surroundings, exhibiting significant tape residue prior to any cleaning procedures.* ***(a)*** *Magnified view of the hBN flake, revealing surface discoloration attributed to residue deposition.* ***(b)*** *Flake exhibits improved cleanliness yet retains some discoloration following one round of cleaning in acetone and IPA baths.* ***(c)*** *Flake after oxygen plasma etching. Flake is notably cleaner and has a smoother surface appearance.* ***(d)***

residue still present on the chip. Cleaning is complete after this step when working with graphene, as further manipulation may compromise the integrity of monolayer or few-layer flakes. However, the need for an extremely clean surface may occasionally necessitate additional chip cleaning. Further soaking in acetone and by IPA, for 30 minutes each, typically eradicates any remaining debris without damaging thin flakes. Monitoring the sample during this process is essential because excess cleaning can dislodge or damage viable thin flakes. Immediate and thorough drying of the chip with nitrogen after removal is necessary to prevent any IPA residue.

A similar cleaning process is used for hBN, but there is less concern for losing or damaging flakes due to the heterostructure requiring thicker, multilayer hBN flakes. The cleaning process may be used repeatedly on hBN samples to ensure a clean surface. Utilization of O_2 plasma etching may also be employed to address persistent surface contamination. Etching is viable for hBN because the thicker nature of these flakes can withstand the etching process. O_2 plasma etching has shown to be highly effective in eliminating debris and achieving a pristine surface on hBN flakes. Should residue persist despite initial etching, the etching process may be repeated.

4.2 Identifying Graphene

Monolayer graphene is reported to range in thickness from 0.4 to 1.7 nm [15], [16]. Graphene thickness is measured in various ways, including atomic force microscopy (AFM), but the use of this could result in folding or other damage to the flake. An alternative method for assessing thickness and gaining insights into a sample is Raman spectroscopy. This technique is

advantageous and is distinguished by its swift operation, nondestructive characteristics, high resolution, and ability to deliver comprehensive structural and electronic analyses [17]. Raman spectroscopy determines the thickness of graphene by analyzing the vibrational modes of the material. Each graphene layer exhibits characteristic Raman spectra due to its unique structural properties. When light shines onto the graphene sample, some photons scatter off the material, and the scattered light contains information about the material's vibrational modes [18]. In the case of graphene, two dominant peaks are detected in the Raman spectrum: the G peak and the 2D peak. The G peak corresponds to the in-plane vibration of carbon atoms, while the 2D peak arises from the second-order scattering process and is sensitive to the number of graphene layers. The intensity ratio of the 2D peak to the G peak provides valuable information about the number of layers in the graphene sample. In single-layer graphene, the intensity ratio of the 2D peak to the G peak is typically around 2.4. In few-layer graphene, this ratio decreases as the number of layers increases.

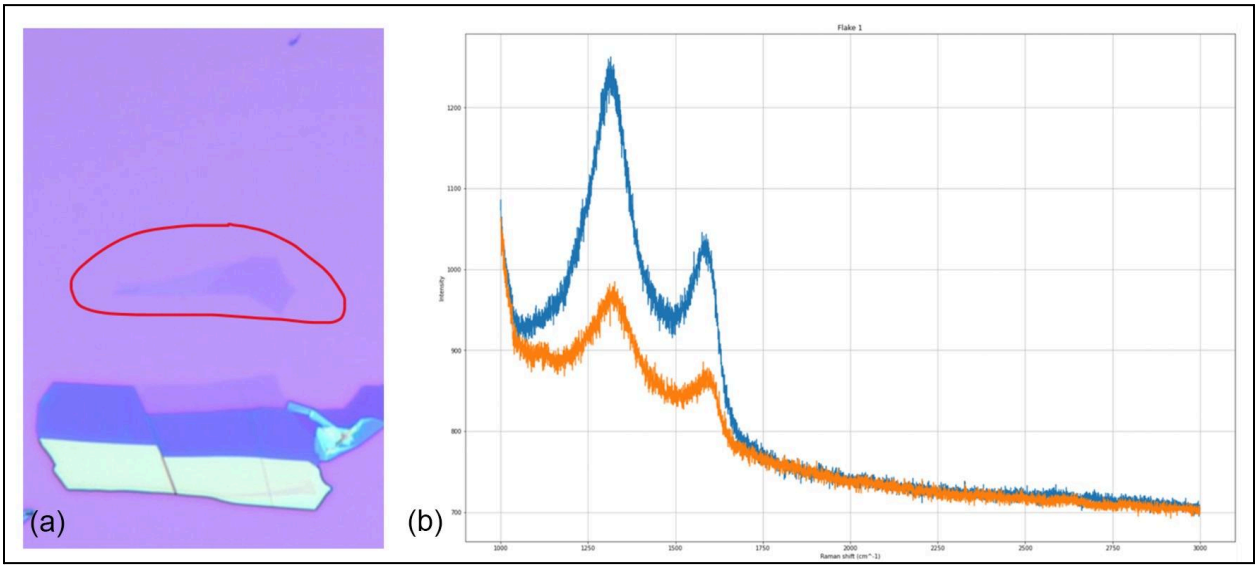

Figure 7. *Graphene flake of two different thickness. The left side of the flake is notably thinner than the right.* ***(a)*** *Graph of Raman spectrum for both areas on the flake. The blue data corresponds to the thinner area and the orange corresponds to the thicker area.* ***(b)***

5. Encapsulated Graphene

Vertically stacked heterostructures, particularly those integrating graphene and hexagonal boron nitride, have captured considerable interest due to their unique properties driven by interlayer van der Waals interactions [19].

5.1 Potential for Graphene-hBN Heterostructures

Hexagonal boron nitride functions as a compelling dielectric substrate, amplifying the capabilities of graphene-based devices. Many studies indicate a growing interest in atomic-scale heterostructures consisting of alternating graphene and hBN layers [20]. These types of

heterostructures enable novel possibilities in the design of electronic, optoelectronic, and micromechanical devices [21], [22].

Encapsulating graphene in layers of hBN results in high-quality graphene devices where ballistic transport over micrometer distances remains viable even at room temperature. The exceptionally smooth surfaces of both crystals and their minimal lattice mismatch promote bonding between graphene and hBN, effectively shielding the graphene from pollutants originating in nanofabrication processes [23]. Typically, graphene on oxidized Si wafers exhibits a charge carrier mobility (μ) of around 10,000 $cm^2 V^{-1} s^{-1}$, but by eliminating extrinsic scattering, graphene's mobility can reach approximately 200,000 $cm^2 V^{\wedge -1} s^{-1}$ at room temperature. However, suspended graphene devices, although capable of achieving high mobility, are fragile and susceptible to environmental factors. Using hBN as a substrate for graphene addresses these issues, resulting in devices with significantly improved electronic properties. Graphene-hBN heterostructures have exhibited room-temperature ballistic transport over distances exceeding 1μm, demonstrating high mobility even at low carrier concentrations. Encapsulating graphene between hBN crystals enhances device performance and protects graphene from environmental contaminants, ensuring long-term stability [24].

5.2 Stack Construction

Building a three-layer stack comprising hBN-graphene-hBN necessitates the construction of a stamp to facilitate the transfer of each flake layer. In this study, the stamp employed consists of a microscope slide affixed with a Polydimethylsiloxane (PDMS) at one end, onto which propylene carbonate (PC) film, 6% solution in chloroform, is stretched and secured.

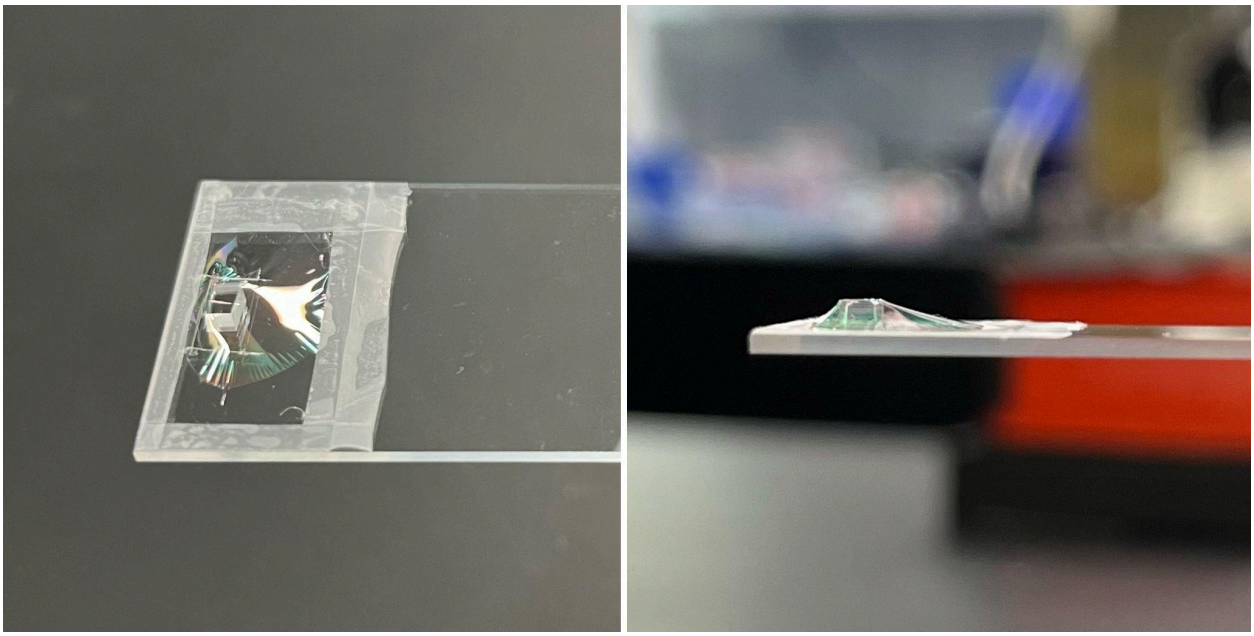

Figure 8. *PC film stretched over PDMS*

The 2D material assembly process begins by picking up the top hBN layer, then the graphene layer and finally the bottom hBN layer, all on one stamp. To begin, the top hBN flake is positioned under an optical microscope and located at 20x magnification. The PC stamp is placed in an apparatus designed to precisely adjust the position of the stamp in the x, y, and z directions. The stamp should also be tilted downward two degrees past parallel to the substrate.

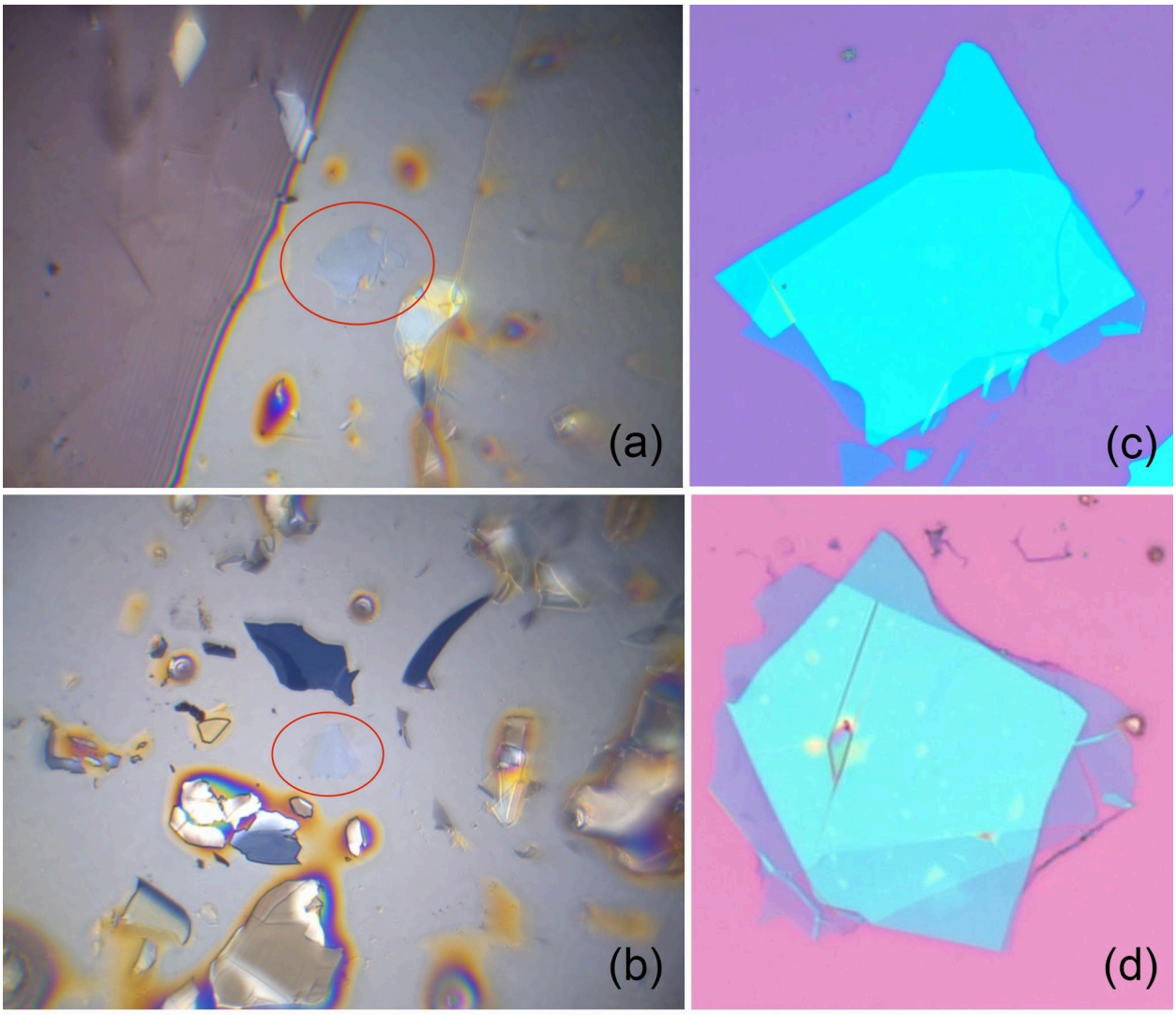

Figure 9. *Substrate engaged at an angle, picking up less of the surrounding debris.* ***(a)*** *Stamp engaged parallel to the substrate, picking up all surrounding residue and debris.* ***(b)*** *Completed 3-layer stack with minimal surrounding debris and no air bubbles due to angled pickup.* ***(c)*** *Complete stack, surrounding debris and air bubbles present.* ***(d)***

The top layer is picked up by aligning the stamp over the desired hBN flake and gradually lowering it until coming in contact with the substrate. Engaging the stamp at a two-degree angle ensures minimal interaction with surrounding flakes and reduces the likelihood of air bubble formation between the stamp and the flake. Applying excessive pressure when

engaging with a thick hBN flake risks cracking or breakage of the flake. Once engaged, the microscope stage is rapidly heated to 125°C and slowly cooled to room temperature. The stamp is then quickly disengaged, lifting the desired flake from the substrate.

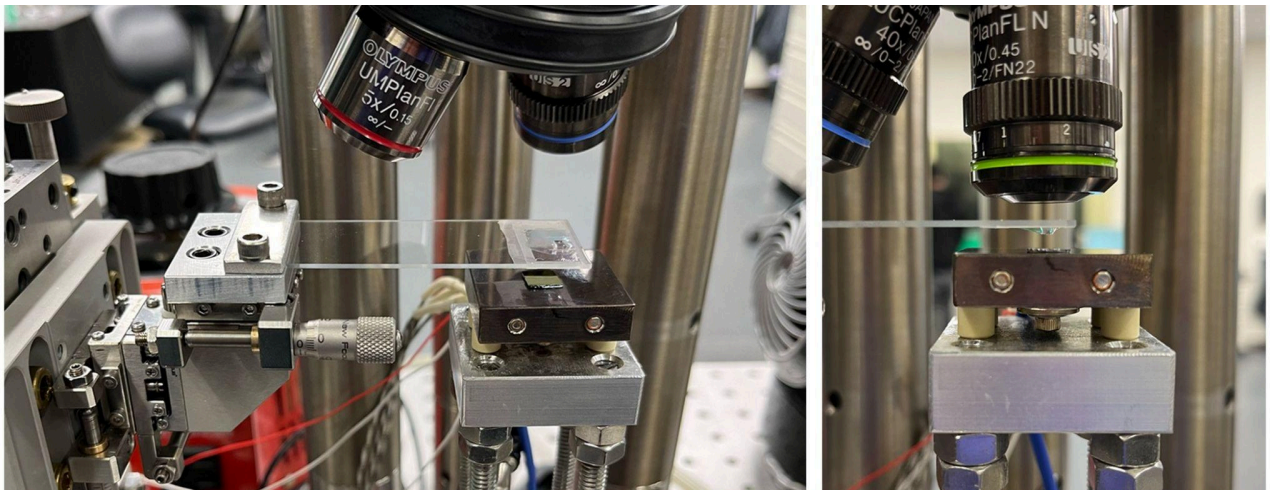

Figure 10. *Transfer setup with stamp and sample chip in place*

Once the top hBN is lifted successfully, the process is repeated using the same stamp to pick up a monolayer graphene flake. Ideally, the graphene flake has an area of at least 100μm². Once the top layer of hBN is in alignment with the graphene, the stamp is engaged with the substrate, heated to 105°C, cooled to room temperature, and quickly disengaged. The base layer of hBN is picked up using the same process, but the substrate is, once again, heated to 125°C. At this stage, it is especially important to not excessively engage the stamp with the substrate. Thick flakes are more likely to crack under pressure as the stack grows in thickness. This can be somewhat avoided by using thinner hBN flakes of 20 - 30 nm. A thinner flake is more flexible and less likely to break.

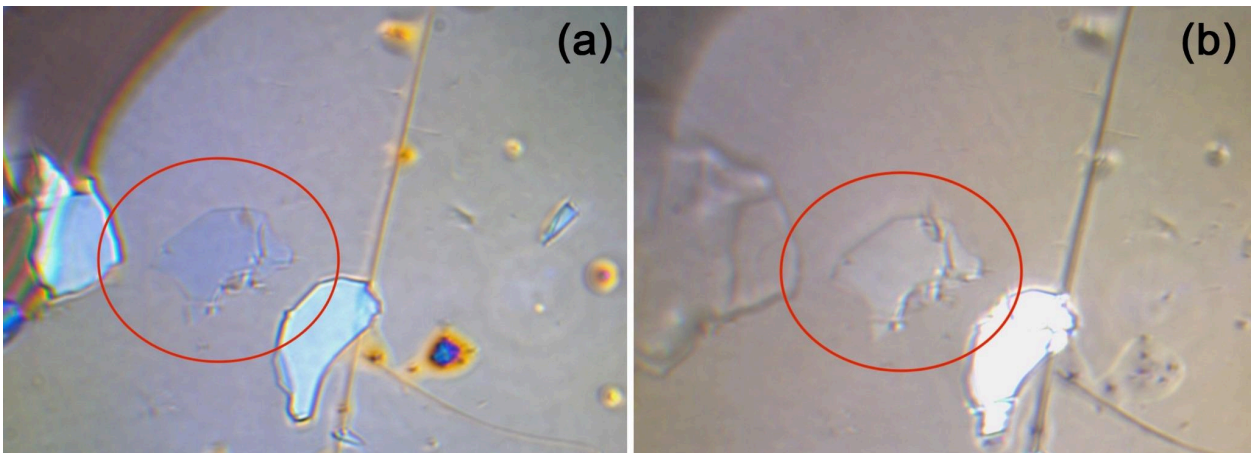

Figure 11. *hBN flake with stamp engaged.* ***(a)*** *PC film with hBN flake picked up.* ***(b)***

After the stack is complete, it is placed onto a clean silicon wafer and stored until needed for device fabrication. This is done by aligning the stack at the center of a clean wafer, firmly engaging, and heating up rapidly. Once the stage is around 160°C, the pressure of engagement is slowly decreased while the stage temperature continues to rise. Once the stage reaches 175 degrees, the PC film melts, and the stamp can be slowly disengaged, leaving behind both the stack and the PC film. The wafer containing the stack should be soaked in chloroform for 15 minutes to dissolve the film, leaving only the deposited flakes behind. It is then rinsed with IPA and dried.

5.3 Experimental Factors

Numerous considerations were involved in the three-layer stack fabrication, with the foremost importance being the cleanliness of the flakes, stamps, and substrates. A comprehensive cleaning regimen was implemented for flake-containing chips to prevent the contamination bubbles between the layers, a highly undesirable outcome. Additional research indicates that large-scale interfaces between graphene and hBN often display contamination bubbles formed by the aggregation of hydrocarbons and other residues caught between the two materials [20]. These bubbles result in notable inconsistencies in charge distribution and should thus be prevented within the active region of a device [25].

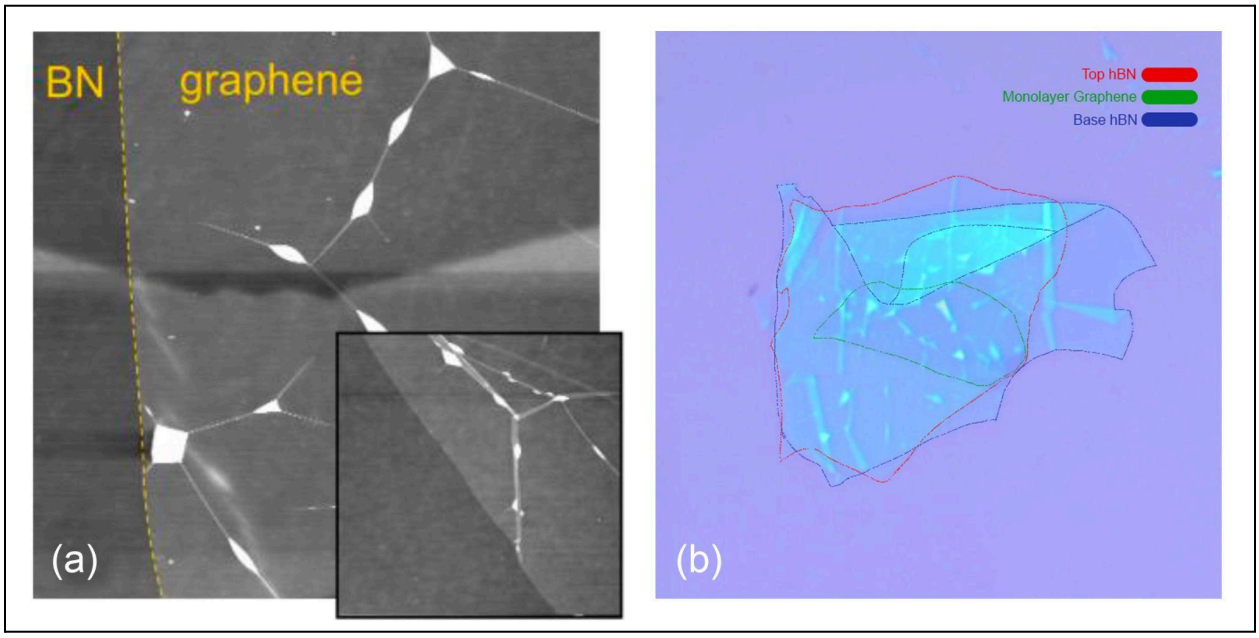

Figure 12. *AFM topology and TEM cross section image of graphene on hBN. The yellow dashed curves highlight edges of graphene flakes. Due to self cleansing for graphene on hBN, hydrocarbon contamination is aggregated into bubbles as bright spots connected by graphene wrinkles [25].* ***(a)*** *Optical micrograph of an hBN-g-hBN stack. Similar to AFM topology, contamination is aggregated into bubbles as bright spots connected by wrinkles.* ***(b)***

Extensive experimentation was conducted to identify the most effective and least damaging cleaning processes to achieve optimal surface cleanliness of viable flakes. In addition to the previously discussed wet cleaning method, alternative approaches were used to ensure optimal transfer. One method involved heating the substrate to temperatures up to 100°C in an effort to eliminate residual debris. The chip is then cooled slightly and the stamp engages the substrate at an elevated temperature ranging from 40°C to 75°C. This procedure aided in debris removal and mitigated the risk of non-debris-induced air bubble formation. However, the disadvantage of this tactic lies in the inability to reposition the stamp after first contact. In some cases, the flake on the stamp may not be adequately aligned with the target flake on the substrate. When working at room temperature, the stamp can be raised, adjusted, and lowered again without picking up or damaging the target flake. This practice at higher temperatures may damage or unintentionally pick up the flake, resulting in the need to discard the entire stack.

Another aspect of the cleaning process pertained to the treatment of the stamp itself. Surface etching of the film with O_2 plasma was performed to enhance its adhesive properties, thereby facilitating more consistent flake pickup during transfer operations. However, this method occasionally led to excessive stickiness, causing the PC film to adhere to the substrate upon heating to high temperatures. Consequently, attempts to disengage the stamp resulted in film stretching, rendering the flake invisible in most instances and the stamp unusable for future transfers. On average, etching the chips with O_2 plasma rather than the stamp itself had similar benefits and resulted in fewer inadvertent losses.

Furthermore, another variable is the application of pressure during flake engagement, with the requisite pressure varying as the stack progressed. Notably, a common issue encountered during stack assembly was engaging with a flake without effectively picking it up. This happened most often when attempting to pick up the final layer of the stack, the base hBN. Given that this layer typically comprises the largest, thickest flake, greater pressure is typically necessary to ensure successful pickup on the first attempt. As the stack increases in height during the final flake pickup, extra pressure is needed to fully encapsulate the sides of the final flake with the PC film, thereby facilitating pickup. Increased pressure allowed further stretching of the PC film and ensured proper contact with all flakes.

6. Fabrication

The device fabrication process begins with the cleaning of a high-resistivity silicon wafer. The silicon wafer is prepared by applying a spin coating of LOR3A resist at 4000 rpm and then baking at 180 degrees for five minutes. This is followed by an AZ1505 resist applied at 5000 rpm and baked at 110 degrees for 1 minute. A photolithography tool is used to create the design and uses a 365nm LED to pattern a photosensitive resist. An LED is mounted on a moving head which rasters over the sample to generate the desired pattern without the need for any mask. The resolution of this tool is 600 nm and has a fast writing speed of 10mm²/min. The sample undergoes exposure in the μMLA system using a 365 nm diode with a dose of 60mJ/cm². After exposure, the resist is developed in 300 MIF for 30 seconds, rinsed in deionized water for 30

seconds, and dried using nitrogen gas. Once the stack is prepared, small contacts are defined onto it through photolithography. Following lithography, the stack is etched using an inductively coupled plasma (ICP) etcher for 30 seconds, employing BCl_3 and Cl_2 gas. Immediately after etching, layers of chromium and gold, with thicknesses of 6nm and 50nm, respectively, are deposited. This process forms the one-dimensional edge contacts to the graphene within the heterostructure.

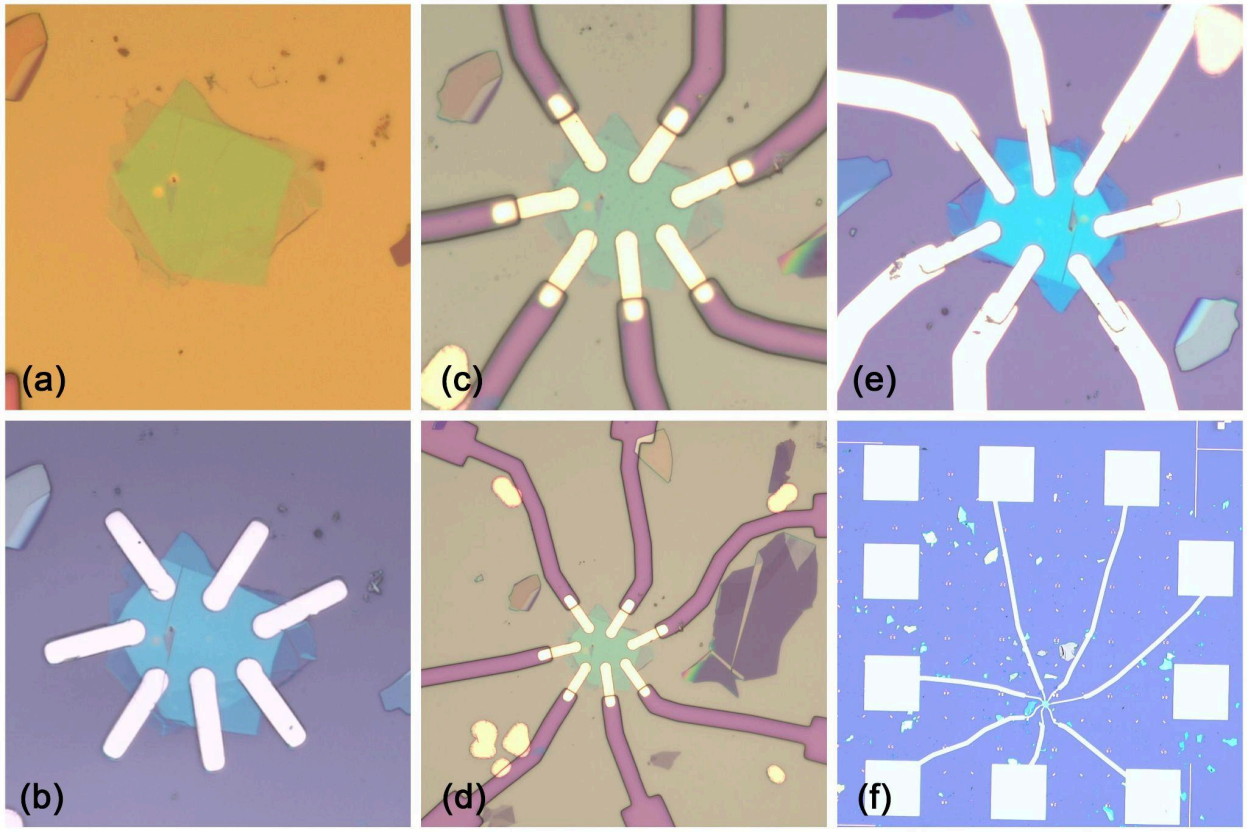

Figure 13. *Completed hBN-graphene-hBN stack.* ***(a)*** *Steps of the fabrication process.* ***(b-f)***

7. One Dimensional Electric Contacts

Interfacing 3D metal electrodes with 2D materials, particularly graphene, poses challenges due to graphene's lack of surface bonding sites. The usual method involves metalizing the graphene surface, resulting in significant contact resistance due to the absence of chemical bonding and strong orbital hybridization. In multilayer structures like hBN-G-hBN heterostructures, exposing the graphene surface for metallization during fabrication is essential and requires sequential assembly to maintain accessibility. However, removing BN layers poses difficulties. Residual polymers from assembly and lithography steps can impair electrical contact, channel mobility, and may cause interface contamination, limiting device size to around $1mm^2$ [26]. The one-dimensional edge-contact fabrication process is a possible solution to these problems. The process involves encapsulating the graphene layer within hBN and then etching

the multilevel stack to expose only the edge of the graphene layer. Subsequently, metal is deposited onto this exposed edge, forming the contact. This edge-contact process allows for the complete separation of the layer assembly and contact metallization processes [26].

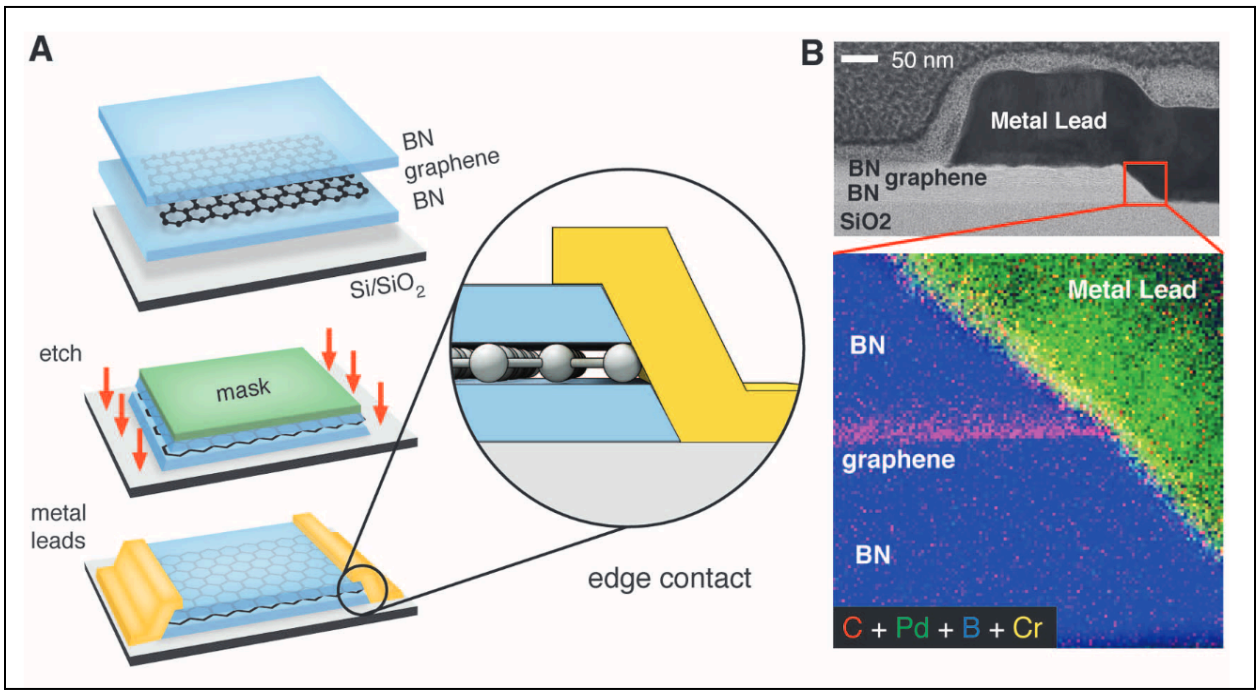

Figure 14. *Edge contact fabrication process.* ***(A)*** *High-resolution bright-field STEM image showing details of the edge contact geometry. The expanded region shows a magnified false-color EELS map of the interface between the graphene edge and metal lead.* ***(B)*** *[26]*

7.1 Advantages

The quality of edge contacts is surprising because graphene is buried inside hBN and exposed by less than one nanometer along the edge. In this innovative contact arrangement, efforts aim to minimize the spatial overlap between graphene and the metal, establishing a covalent bond between the metal atoms and the graphene [27]. The covalent bond between carbon and metal atoms has reportedly shown much lower resistivity than traditional surface contacts formed by metal deposition on the graphene layer [28]. Carbon atoms at the edge of a graphene sheet are not fully saturated with bonds like they are in the sheet interior. This creates dangling bonds or unsaturated carbon atoms at the edge. When a metal electrode is in contact with these edges, the binding distance between the metal atoms and the graphene edge is shorter compared to contacts made with the graphene surface. This shorter distance allows for stronger interactions between the metal and graphene, causing reduced resistance to electron flow [27]. Graphene's electronic structure is also characterized by its delocalized π orbitals that extend over the entire sheet. At the edges, however, these orbitals are less confined and can extend outward. When a metal electrode makes contact with these edge orbitals, there is a strong overlap between the metal's electronic orbitals and those of the graphene edge. This overlap promotes efficient

electron transfer between the metal and graphene, resulting in lower resistance to current flow [29].

Past measurements performed on encapsulated graphene devices with 1D ferromagnetic contacts indicate that a phenomenon primarily driven by the local Hall effect is observable. This occurs as the charge current spreads beyond the intended injection circuit, leading to a magnetoresistance switching characterized by single-step behavior. The local Hall magnetoresistance is attributed to the Lorentz force acting on moving charges in the presence of stray magnetic fields generated by the 1D edge contacts. Calculations indicate that optimizing the contact geometry can reduce the magnitude of the perpendicular stray magnetic field at the contact edge to below 100 mT, potentially mitigating the observed effects [30].

One study from Wang et al. utilized computational modeling techniques to gain insights into the mechanisms behind the low contact resistance of edge-contacts in graphene devices [26]. These simulations using a Cr metal electrode indicate that edge contacts lead to shorter bonding distances with larger orbital overlap than surface contacts, which is consistent with other studies [29]. Using density functional theory (DFT) in conjunction with nonequilibrium Green's function (NEGF), the simulations showed that incorporating additional interfacial species, such as oxygen from the etching process, could enhance bonding and improve transmission. Experimental data and the simulation model indicated that the contact resistance exhibited divergence near the charge neutrality point of graphene and predicted contact resistance as low as 118 ohm·μm at

$$E - E_{CNP} = 0.16eV\ (n = 2.2\ x\ 10^{12}\ cm^{-2})$$

for a Cr(110)-O-graphene interface, where

$$E - E_{CNP}$$

represents the fermi energy of graphene relative to the energy corresponding to the charge neutrality point [26].

8. Conclusion

This research has extensively covered the synthesis, encapsulation, and fabrication processes involved in creating heterostructures composed of monolayer graphene encapsulated by layers of hexagonal boron nitride. Through experimentation and analysis, we have explored the potential of these encapsulated heterostructures for various electronic applications. Investigations highlight the unique properties and advantages offered by encapsulated graphene heterostructures, including enhanced electronic mobility, protection from environmental contaminants, and novel device functionalities. The construction of these heterostructures, involving precise stacking and transfer techniques, has been detailed, emphasizing the importance of cleanliness and control in achieving high-quality devices.

Moreover, our exploration of one-dimensional electric contacts has revealed promising avenues for reducing contact resistance and improving device performance in graphene-based systems. By leveraging the edge-contact fabrication process, we see the potential to enhance the

efficiency and reliability of electronic devices, paving the way for advancements in nanoelectronics and quantum technologies. Further optimization of fabrication techniques and material choices could lead to even higher-performance in graphene-hBN heterostructures and devices. Additionally, exploring novel applications and device architectures could unlock new functionalities and capabilities in graphene-based electronics.

9. References

[1] P. Preuss, “Bilayer Graphene Gets a Bandgap,” Berkeley Lab News Center. Accessed: Feb. 12, 2024. [Online]. Available: https://newscenter.lbl.gov/2009/06/10/graphene-bandgap/

[2] K. S. Novoselov, A. Mishchenko, A. Carvalho, and A. H. Castro Neto, “2D materials and van der Waals heterostructures,” *Science*, vol. 353, no. 6298, p. aac9439, Jul. 2016, doi: 10.1126/science.aac9439.

[3] Q. Abbas *et al.*, “Graphene Synthesis Techniques and Environmental Applications,” *Materials*, vol. 15, no. 21, p. 7804, Nov. 2022, doi: 10.3390/ma15217804.

[4] K. S. Novoselov *et al.*, “Two-dimensional gas of massless Dirac fermions in graphene,” *Nature*, vol. 438, no. 7065, Art. no. 7065, Nov. 2005, doi: 10.1038/nature04233.

[5] R. Mas-Ballesté, C. Gómez-Navarro, J. Gómez-Herrero, and F. Zamora, “2D materials: to graphene and beyond,” *Nanoscale*, vol. 3, no. 1, pp. 20–30, 2011, doi: 10.1039/C0NR00323A.

[6] J. Xue *et al.*, “Scanning tunnelling microscopy and spectroscopy of ultra-flat graphene on hexagonal boron nitride,” *Nat. Mater.*, vol. 10, no. 4, Art. no. 4, Apr. 2011, doi: 10.1038/nmat2968.

[7] K. Kang Kim, H. Seok Lee, and Y. Hee Lee, “Synthesis of hexagonal boron nitride heterostructures for 2D van der Waals electronics,” *Chem. Soc. Rev.*, vol. 47, no. 16, pp. 6342–6369, 2018, doi: 10.1039/C8CS00450A.

[8] Y. Huang *et al.*, “Reliable Exfoliation of Large-Area High-Quality Flakes of Graphene and Other Two-Dimensional Materials,” *ACS Nano*, vol. 9, no. 11, pp. 10612–10620, Nov. 2015, doi: 10.1021/acsnano.5b04258.

[9] Y. Yang *et al.*, “Electrochemical exfoliation of graphene-like two-dimensional nanomaterials,” *Nanoscale*, vol. 11, no. 1, pp. 16–33, 2019, doi: 10.1039/C8NR08227H.

[10] P. Yu, S. E. Lowe, G. P. Simon, and Y. L. Zhong, “Electrochemical exfoliation of graphite and production of functional graphene,” *Curr. Opin. Colloid Interface Sci.*, vol. 20, no. 5, pp. 329–338, Oct. 2015, doi: 10.1016/j.cocis.2015.10.007.

[11] K. E. Whitener and P. E. Sheehan, “Graphene synthesis,” *Diam. Relat. Mater.*, vol. 46, pp. 25–34, Jun. 2014, doi: 10.1016/j.diamond.2014.04.006.

[12] Y. Zhang, L. Zhang, and C. Zhou, “Review of Chemical Vapor Deposition of Graphene and Related Applications,” *Acc. Chem. Res.*, vol. 46, no. 10, pp. 2329–2339, Oct. 2013, doi: 10.1021/ar300203n.

[13] X. Chen, L. Zhang, and S. Chen, “Large area CVD growth of graphene,” *Synth. Met.*, vol. 210, pp. 95–108, Dec. 2015, doi: 10.1016/j.synthmet.2015.07.005.

[14] H. Tetlow, J. Posthuma de Boer, I. J. Ford, D. D. Vvedensky, J. Coraux, and L. Kantorovich, “Growth of epitaxial graphene: Theory and experiment,” *Phys. Rep.*, vol. 542, no. 3, pp. 195–295, Sep. 2014, doi: 10.1016/j.physrep.2014.03.003.

[15] V. Kumar, A. Kumar, D.-J. Lee, and S.-S. Park, “Estimation of Number of Graphene Layers Using Different Methods: A Focused Review,” *Materials*, vol. 14, no. 16, p. 4590, Aug. 2021, doi: 10.3390/ma14164590.

[16] C. Shearer, A. Slattery, A. Stapleton, J. Shapter, and C. Gibson, “Accurate thickness measurement of graphene,” *Nanotechnology*, vol. 27, p. 125704, Feb. 2016, doi: 10.1088/0957-4484/27/12/125704.

[17] A. C. Ferrari and D. M. Basko, “Raman spectroscopy as a versatile tool for studying the properties of graphene,” *Nat. Nanotechnol.*, vol. 8, no. 4, pp. 235–246, Apr. 2013, doi:

10.1038/nnano.2013.46.
[18] M. Paillet, R. Parret, J.-L. Sauvajol, and P. Colomban, “Graphene and related 2D materials: An overview of the Raman studies,” *J. Raman Spectrosc.*, vol. 49, no. 1, pp. 8–12, 2018, doi: 10.1002/jrs.5295.
[19] Q. Li, M. Liu, Y. Zhang, and Z. Liu, “Hexagonal Boron Nitride–Graphene Heterostructures: Synthesis and Interfacial Properties,” *Small*, vol. 12, no. 1, pp. 32–50, 2016, doi: 10.1002/smll.201501766.
[20] S. J. Haigh *et al.*, “Cross-sectional imaging of individual layers and buried interfaces of graphene-based heterostructures and superlattices,” *Nat. Mater.*, vol. 11, no. 9, pp. 764–767, Sep. 2012, doi: 10.1038/nmat3386.
[21] H. Wang *et al.*, “BN/Graphene/BN Transistors for RF Applications,” *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1209–1211, Sep. 2011, doi: 10.1109/LED.2011.2160611.
[22] L. A. Ponomarenko *et al.*, “Tunable metal–insulator transition in double-layer graphene heterostructures,” *Nat. Phys.*, vol. 7, no. 12, pp. 958–961, Dec. 2011, doi: 10.1038/nphys2114.
[23] J. I.-J. Wang *et al.*, “Electronic Transport of Encapsulated Graphene and WSe2 Devices Fabricated by Pick-up of Prepatterned hBN,” *Nano Lett.*, vol. 15, no. 3, pp. 1898–1903, Mar. 2015, doi: 10.1021/nl504750f.
[24] A. S. Mayorov *et al.*, “Micrometer-Scale Ballistic Transport in Encapsulated Graphene at Room Temperature,” *Nano Lett.*, vol. 11, no. 6, pp. 2396–2399, Jun. 2011, doi: 10.1021/nl200758b.
[25] A. V. Kretinin *et al.*, “Electronic properties of graphene encapsulated with different 2D atomic crystals”.
[26] L. Wang *et al.*, “One-Dimensional Electrical Contact to a Two-Dimensional Material,” *Science*, vol. 342, no. 6158, pp. 614–617, Nov. 2013, doi: 10.1126/science.1244358.
[27] B. Kretz, C. S. Pedersen, D. Stradi, M. Brandbyge, and A. Garcia-Lekue, “Atomistic Insight into the Formation of Metal-Graphene One-Dimensional Contacts,” *Phys. Rev. Appl.*, vol. 10, no. 2, p. 024016, Aug. 2018, doi: 10.1103/PhysRevApplied.10.024016.
[28] S. Min Song, T. Yong Kim, O. Jae Sul, W. Cheol Shin, and B. Jin Cho, “Improvement of graphene–metal contact resistance by introducing edge contacts at graphene under metal,” *Appl. Phys. Lett.*, vol. 104, no. 18, p. 183506, May 2014, doi: 10.1063/1.4875709.
[29] D. W. Yue, C. H. Ra, X. C. Liu, D. Y. Lee, and W. J. Yoo, “Edge contacts of graphene formed by using a controlled plasma treatment,” *Nanoscale*, vol. 7, no. 2, pp. 825–831, 2015, doi: 10.1039/C4NR05725B.
[30] B. Karpiak, A. Dankert, A. W. Cummings, S. R. Power, S. Roche, and S. P. Dash, “1D ferromagnetic edge contacts to 2D graphene/h-BN heterostructures,” *2D Mater.*, vol. 5, no. 1, p. 014001, Oct. 2017, doi: 10.1088/2053-1583/aa8d2b.