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Smart Gate Driver Design for Silicon (Si) IGBTs and Silicon-Carbide (SiC) MOSFETs

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for

Silicon (Si) IGBTs and Silicon-carbide (SiC) MOSFETs

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in the

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Abstract

The design of an efficient and smart gate driver for a Si IGBT and SiC MOSFET is addressed in thesis. First, the main IGBT parameters are evaluated thoroughly in order to understand their effects in the design of the gate driver. All known consequences of previously designed gate drivers are studied in order to achieve an optimum gate driver. As a result of this assessment, the designer is able to determine whether adding or removing components from the gate driver circuit are beneficial or not. Then, exhaustive research is done to identify suitable integrated circuits to use for the power supplies, isolation circuit, protection circuit, and gate driver circuitry. Next, the final design is laid out in PCB Editor in order to eventually manufacture it and test it out. During this process, important techniques in making an efficient and compact PCB are taken into consideration.

CHAPTER 1

INTRODUCTION

1.1 Overview

Silicon (Si) insulated-gate bipolar transistors (IGBTs) are used widely in power electronic applications like motor drivers due to low conduction losses when compared to MOSFETs. IGBT are frequently preferred over MOSFETs and BJTs because they combine advantages of these transistors (i.e., low voltage drop and high current capabilities). IGBTs have the simple gate drive characteristics of MOSFETs, and the higher current capability of BJTs [1]. Therefore, a driver circuit should be implemented with certain specifications that fulfill the requirements of the driven device, the IGBT. Depending on the application, designing the most appropriate driver circuit is necessary in order to ensure high efficiency and better functionality of the whole application.

Consequently, the purpose of this thesis is to design an efficient gate driver for Si IGBTs and SiC MOSFETs for the projects being implemented in the Sustainable Smart Electric Energy Systems (SSEES) laboratory. The semiconductor devices that are used in the Solid State Transformer (SST) project are IKW40N120H3 and CMF20120D, which are a Si IGBT and a SiC MOSFET, respectively. The design of a gate driver in this thesis is based on these two devices because they have similar ratings.

Regarding the design process, this thesis considers important parameters for an IGBT gate driver. Therefore, in order to design a competent gate driver, these considerations have to be investigated separately to avoid malfunctions and to ensure proper functioning in the circuit.

After designing the gate driver, it will be built using different PCB design techniques in order to compare its efficiency. This is done because the layout of the circuit can have great impacts on the performance of the whole application.

1.2 Objectives of the Thesis

The primary intent of this thesis is to design an optimal gate driver for Si IGBTs and SiC MOSFETs. This gate driver should have better performance than previously designed gate drivers in the SSEES lab. Moreover, it should be able to overcome most of the challenges that gate drivers encounter such as protection against short-circuit currents and high voltage transients. This gate driver should be also as compact and economical as possible.

1.3 Organization of the Thesis

This thesis is organized as follows: the theoretical background of IGBTs and their driver circuits are addressed in Chapter 2. Then, the design considerations for an IGBT gate driver that examine every parameter's importance towards the whole design are highlighted in Chapter 3. The selection of suitable integrated circuits (ICs) and appropriate components completing the whole driver design is presented in Chapter 4. Finally, the experimental results obtained from the lab prototype are given and evaluated in Chapter 5. Lastly, the conclusions of this work are given in Chapter 6.

CHAPTER 2

THEORETICAL BACKGROUND

2.1 Introduction

The purpose of this chapter is to discuss the theory behind IGBT/MOSFET gate drivers. Theoretically speaking, IGBTs make use of inherent advantages in the MOSFETs and BJTs [2]. They have the low saturation voltage and high current capability of BJTs [3]. Every other characteristic in an IGBT resembles these characteristics of a MOSFET [3]. Thus, IGBTs are only discussed in this chapter since they are driven similarly to MOSFETs.

2.2 Theory of IGBT Operation

An IGBT and its parasitic capacitances are shown in Figure 1 below. In order to produce an efficient gate driver, designers should investigate the device operation under turn-on and turn-off conditions. This section discusses the IGBT operation in relation to the design of gate drivers. This section is divided into three subsections. The first one shows the analysis of the turn-on operation of the IGBT. The second subsection discusses the turn-off process of the IGBT. Finally, the last subsection explains the importance of the switching characteristics with respect to the design of a great gate driver.

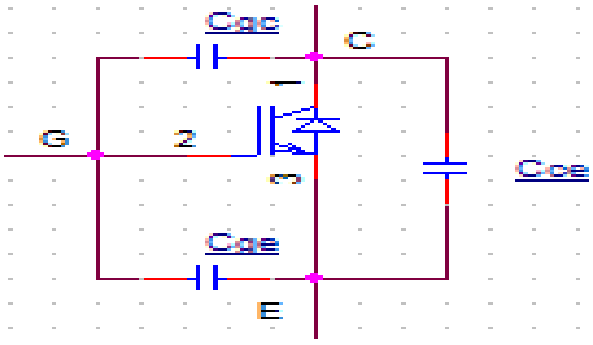

Figure 1. An IGBT with its parasitic capacitances.

2.2.1 Analysis of turn-on switching characteristics

[4] Initially, the turn-on process starts by applying a gate signal to the gate driver. Then, the gate current (i_G) starts charging the input capacitance (C_{ies}), which is equal to the sum of gate-emitter capacitance (C_{GE}) and gate-emitter capacitance (C_{GC}). As a result of charging the input capacitance, the gate voltage (v_{GE}) increases exponentially to the threshold of the gate voltage ($v_{GE(th)}$) of the IGBT. This process constitutes the delay time interval that is defined in the device's datasheet. During this time interval, the collector voltage (v_{CE}) and collector current (i_C) are not changed by this small increase of the gate voltage.

[4] After v_{GE} increases beyond the threshold voltage, the IGBT starts conducting current. Therefore, i_C starts increasing while the gate is being charged up. The collector current increases to the load current and exceeds the current due to the reverse recovery of the freewheeling diode; therefore, v_{CE} decreases slightly due to the parasitic inductance. Also, this decrease in v_{CE} is related to the rate of change of the collector current.

[4] Furthermore, the freewheeling diode starts having a great impact on the switching characteristics of the IGBT for the inductive loads. After i_C starts reaches the load current, a reverse recovery current from the freewheeling diode is added to the IGBT collector current. This phenomenon is shown in the switching waveform as a sudden increase in the collector current over the load current. Moreover, the rate of change of v_{CE} becomes very high during this time interval since C_{GC} is small and v_{CE} is quite large.

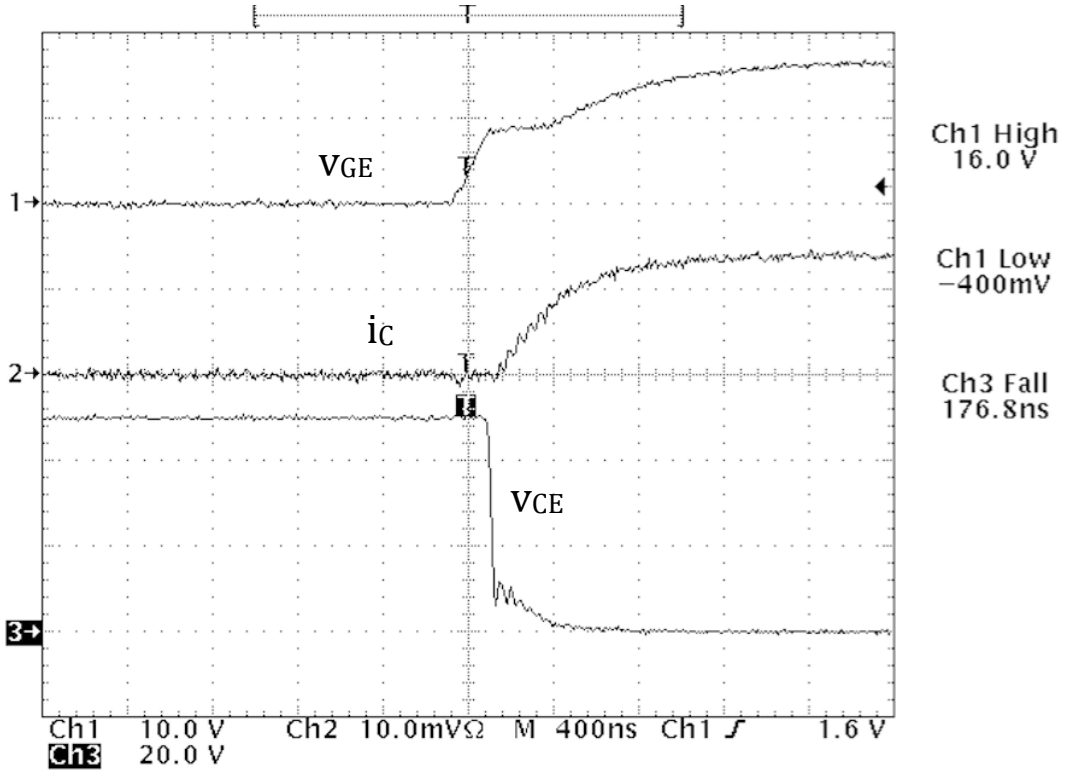

Figure 2. The turn-on characteristics of an IGBT.

[4], [5] At this point, the input capacitance is very large, which explains the rapid decrease in v_{CE}. The gate current still continues charging up C_{GC}, and this capacitance is getting larger due to the low value of the collector-emitter voltage. The gate voltage starts again increasing, after passing the Miller plateau region, to its positive rail voltage set by the designer. As this is happening, v_{CE} slowly goes to its lowest value, where it is fully saturated. An IGBT was tested in lab, and its switching waveforms during turn-on are shown in Figure 2. To clarify, channel 1 shows v_{GE}, channel 2 displays the collector current, i_C, and channel 3 shows v_{CE}.

2.2.2 Analysis of turn-off switching characteristics

[5] The turn-off process starts in an IGBT by removing the gate signal; initially, the parameter affected is the gate voltage that starts decreasing from its upper limit value, V_{GG+}. This time

interval corresponds to the turn-off delay time, where also neither the collector voltage nor the collector current is affected.

[4] After the gate voltage decreases to a certain value, v_{CE} starts increasing to the dc-bus voltage. Then, similarly to the turn-on effects, the parasitic inductance with the rate of change of the collector current boosts v_{CE} slightly over its dc-bus value. During this time interval, the gate voltage is maintained at the same level as when the Miller effects took place.

[4] After v_{CE} reaches it's the dc-bus voltage, the collector current starts decreasing with a high rate of change, and the gate voltage, v_{GE}, starts again decreasing after passing the Miller plateau region until it reaches its threshold value.

Finally, the gate voltage falls quickly to its lower limit, V_{GG-}. Also, the collector current decreases to zero, showing the tail current that will be discussed in the following subsection. At this point, the IGBT is completely turned off. The switching waveforms during turn-off are shown in Figure 3. To clarify, channel 1 shows v_{GE}, channel 2 displays the collector current, i_C, and channel 3 shows v_{CE}.

2.2.3 Importance of the IGBT switching analysis

Studying how the IGBT operates is really critical in order to design an optimal gate driver. The switching analysis shows what the recommended value of the gate voltage is, what the gate resistance should be, and what the driving current should be set to. Designing for these values minimizes switching losses in the system, and it increases the life of that device.

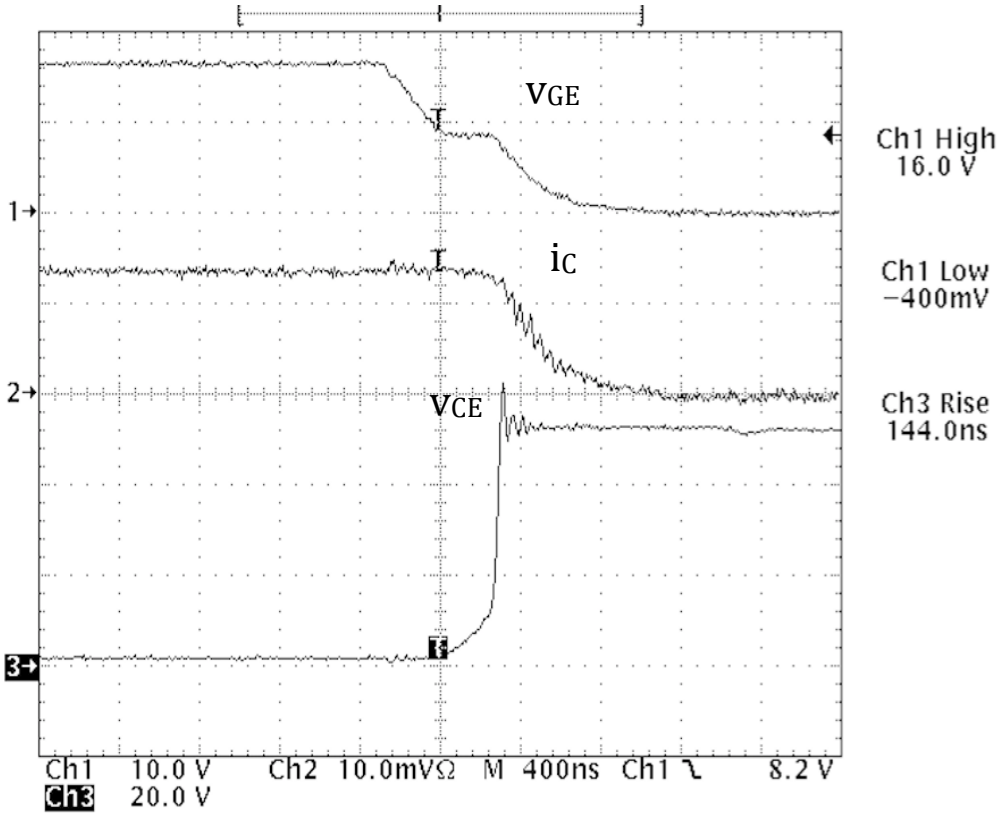

Figure 3. The turn-off characteristics of an IGBT.

CHAPTER 3

DESIGN CONSIDERATIONS FOR A GATE DRIVER

3.1 Introduction

The goal of this chapter is to consider and evaluate all common parameters for an IGBT gate driver. Every parameter is examined thoroughly in order to select its best value for the purpose of designing an optimal gate driver. It is known that some parameters are more important and influential than others in a gate driver; therefore, this trade-off is also analyzed to achieve a very efficient design. The IGBT datasheet is used to complement the parameter selection process.

3.2 Selection and Evaluation of a Gate Driver's Parameters

The main parameters of a gate driver circuit are V_{GG+}, V_{GG-}, and R_G. In addition, the designer considers integrating an isolation circuit and other protection circuits to enhance the performance of the gate driver. All these parameters are evaluated thoroughly in this section that is divided into two subsections. The first subsection discusses the associated parameters for the turn-on and turn-off processes. The other subsection evaluates additional parameters for protection purposes.

3.2.1 Selecting proper parameters for the turn-on and turn-off processes

As mentioned in Chapter 2, the turn-on and turn-off characteristics depend on multiple parameters in a gate driver circuit. For example, the gate voltage, v_{GE}, is extremely vital in both the turn-on and turn-off processes. The gate resistance, R_G, is also important in the same processes. For example, Figures 5 and 6 of the IGBT datasheet provide its voltage drop when turned on for certain values of v_{GE}. In addition, Figures 10 and 14 of the datasheet show the

switching times and switching losses as functions of the gate resistance. The designer chooses these parameters that relay on the gate charge of the IGBT and the gate driver current.

The gate-emitter voltage, V_{GG+}, during conduction

In order to turn the IGBT on, a positive signal that exceeds the threshold voltage is set to charge up the gate capacitance. This positive bias voltage, symbolized as V_{GG+}, is very critical in the turn-on process of the IGBT as several figures illustrate this in the datasheet. Many other parameters are dependent on the value of the on-state gate-emitter voltage.

The manufacturer of the IGBT sets the maximum and minimum values of v_{GE}; therefore, according to the IKW40N120H3's datasheet, the gate voltage must be within $\pm 20\ V$ [6]. Since the value of V_{GG+} has an impact on the short-circuit capability of the gate driver and the switching losses, the best value is chosen to ensure proper functioning [7]. A recommended value for $V_{GG+}$of +15V is suggested by Infineon to have a high short-circuit withstand time and lower short-circuit collector current [8].

The gate-emitter voltage, V_{GG-}, during turn-off

A zero volts or a negative bias voltage is normally applied to the gate of the IGBT to turn off the device. Applying zero volts to the gate may be enough to turn off the device, but it would be very slow and susceptible to noise sparks causing an unwanted turn-on of the device. Therefore, a negative bias voltage, V_{GG-}, is faster, and it protects the circuit from false turn-on due to the parasitic capacitances and inductances [2]. A recommended range for V_{GG-} is from -5 to -15V [7]. Since the turn-off process relies on the value of V_{GG-}, it should be large enough to ensure

short switching times and switching losses [7]. Consequently, the value chosen for this design is -8.7V.

The gate resistance, R_G, during both turn-on and turn-off

The gate resistance, R_G, is connected in series with the gate of the IGBT, and it is very crucial for both the turn-on and turn-off characteristics. There is a huge trade-off in choosing the optimal value of the gate resistance; if a large value for R_G is chosen, the switching loss is going to be greater, and the switching time is going to be longer [7]. However, the smaller the gate resistance, the greater the dv/dt shoot through current becomes [7]. This dv/dt shoot through current may cause the false turn-on of the IGBT, and then losses increase [4]. Consequently, the minimum value for R_G is set using the following equation.

$$R_G = \frac{(V_{GG+})-(V_{GG-})}{I_G} = \frac{(15V)-(-8.7V)}{(4A)} = 5.925\Omega \quad (1)$$

The value of the gate current, I_G, is taken from the gate driver IC discussed in the following chapter. From equation (1), the most appropriate value for the gate resistance is 6.8 Ω. A simple gate driver circuit including V_{GG+}, V_{GG-}, and R_G is shown in Figure 4 below.

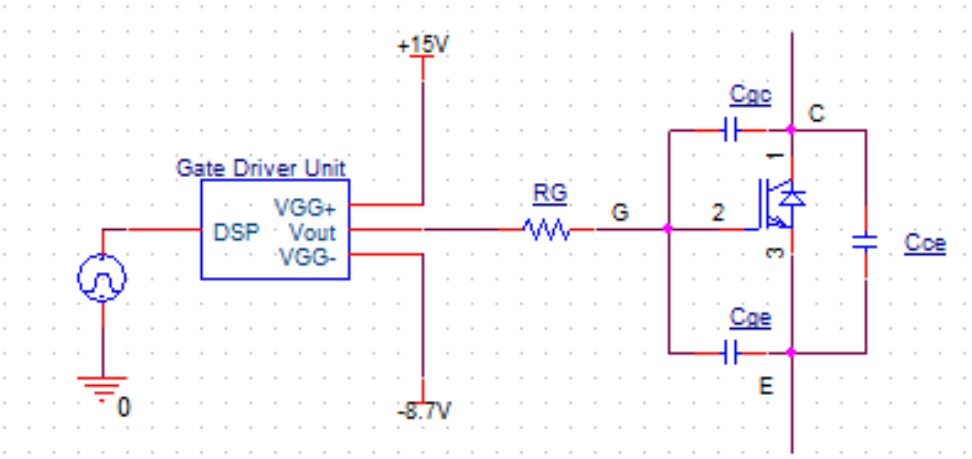

Figure 4. A simple gate driver circuit with the important drive parameters.

3.2.2 Selection of proper parameters for the protection circuits

A methodology to protect the gate driver circuit from overload or short-circuit is discussed in this subsection. Generally speaking, the device might be destroyed when the IGBT is operating outside its safe operating area (SOA) [2]. Therefore, a proper sensing and protecting circuit is designed in order to prevent such failures.

Pull-down resistor to avoid false turn-on

As mentioned before, the IGBT might be destructed when the gate driver circuit is not operating, and a voltage is applied to the circuit, [7]. To avoid this problem, a pull-down resistor is connected between the gate and emitter to discharge the gate-emitter capacitance, C_{GE}, and have a soft turn-off [2]. As shown in Figure 5, a recommended value for the pull-down resistor is 10 $k\Omega$.

De-saturation method for overload protection

A technique implemented to prevent short-circuit is called de-saturation sensing circuit. This method constantly checks the collector-emitter voltage [4]. When v_{CE} exceeds a certain value, while an adequate gate voltage is applied to the gate, it means that collector current, i_C, has risen to a very high value, and the IGBT must be softly turned off [2]. Therefore, this technique is implemented as follows. A diode is connected to the collector pin of the IGBT to monitor v_{CE}. A gate driver circuit with the de-saturation method being implemented is shown in Figure 5. Furthermore of this method is discussed in the following chapter because it is a part of the gate driver integrated circuit (IC).

A clamping circuit for overvoltage protection

Another important and common practice to protect to the gate voltage from exceeding the limit specified by the datasheet of the IGBT is to add a clamping circuit [9]. The gate voltage at turn-on, $V_{GG+,}$ is set to be +15V; therefore, if the gate voltage goes over this limit, short-circuit collector current increases, and short-circuit withstand time decreases [8]. As a result of this analysis, an active clamping circuit is used within the gate driver to protect the IGBT from such undesired complications. A gate driver circuit with the de-saturation and clamping methods being implemented is shown in Figure 5. The functionality of this circuit is explained in the following chapter since it is a part of the gate driver integrated circuit (IC).

Opto- and photo-couplers for proper isolation

Last but not least, an isolation circuitry is added to insulate the input control signals from the output signals. An opto-coupler offers a high isolation voltage from 2500 V to approximately 5000V [2]. Developing on the position of the IGBT within the power converter, the device emitter, ground of the gate driver, could be grounded to the positive terminal. Therefore, the opto-coupler avoids connecting the logical/control ground to the dc-bus positive terminal. More about opto-couplers is discussed in the following chapter.

3.3 Results from the Design Analysis

The primary parameters that make up most of the gate driver circuit designed in this chapter for high reliability and optimal functioning are shown in Table 1.

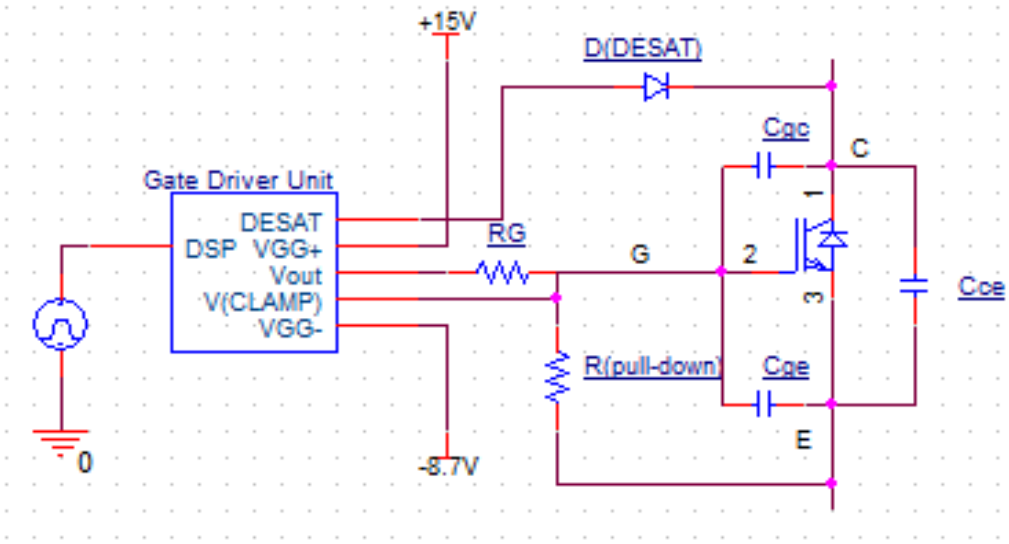

Figure 5. A gate driver circuit with the protection methods.

Table 1. Designed Values for the Gate Driver

Parameters	**Chosen Values**
V_{GG+}	+15 V
V_{GG-}	-8.7 V
R_G	6.8 Ω
$R_{Pull-down}$	10 kΩ
Photo-coupler isolation voltage	2500 V to 5000 V

CHAPTER 4

PROPER IC SELECTION FOR THE GATE DRIVER

4.1 Introduction

The advent of integrated circuits (ICs) to the electronics world has provided designers many advantages such as the ability to make printed circuit boards (PCBs) more compact and the time saved from designing each function integrated in an IC individually [2]. For the purpose of designing an efficient gate driver, the designer chooses to use ICs for the aforementioned reasons and for the attractive integrated features available in some ICs. The primary objective of this chapter is to discuss the criteria for selecting suitable ICs for the design of a gate driver. Each IC added to the whole design is investigated thoroughly to understand its functionality and to determine its importance to the design of the gate driver. The parameters associated with the selected ICs are also examined to ensure proper functioning of the ICs. The parameter consideration taken in chapter 2 and the datasheets of the selected ICs are heavily used to supplement the IC selection process.

4.2 Integrated Circuits for Power Supplies

There are several ways to power gate driver circuits. According to the discussion in chapter 3 about the designed gate voltages during both turn-on and turn-off, the designer identifies, a suitable integrated circuit (IC) that can provide that voltage requirements. [10] The first way is to use charge pumps. A second way is to utilize a PWM signal through a transformer. The third way is to use isolated DC-DC converters [10]. The advantages and disadvantages of these methods are discussed below to determine the best technique to power the driver circuitry.

[10] The charge pump method is usually used when two IGBTs are connected in series. The only important advantage of this approach is its low cost. One of the main problems of this technique is having isolation that may not meet safety requirements. Another disadvantage of this method is the complexity of driving the gate driver circuitry with positive and negative voltages [10]. Last but not least, the addition of more components in the design increases the size of the printed circuit board (PCB) and increases the time spent in bearing these components.

[10] A PWM signal through a transformer is a common way to power the gate driver circuitry. There are several advantages of utilizing transformers along with gate drivers. One of the benefits is having DC isolation and the capability of stepping the voltages up or down during turn-on and turn-off of the IGBT. This method is also able to provide negative bias voltage to ensure the benefits discussed in section 3.2.1 [10]. Another advantage of using transformers for a gate driver is that it does not have any propagation delay time when carrying signals from the primary side to the secondary side [2]. Some of the disadvantages of this technique are listed below [2], [10]:

- The possibility of delivering a massive amount of power that is not appropriate for high frequency devices.
- Only used for AC signals
- The larger the transformer, the higher the coupling capacitance that yields a high circulating current in the transformer.
- The complexity of constructing the transformer to meet safety regulations for isolation.
- The high cost for having to drive the primary side of the transformer by a high-speed buffer.

An alternative way for powering the gate driver circuitry is to use an isolated DC-DC converter. When using opto-couplers, this method is mandatory to power the gate driver connected to the opto-coupler. Isolated DC-DC converters offer more than 2000 V of isolation, which increases the efficiency of the overall design [2]. Some of the important advantages for using isolated DC-DC converter to feed a gate driver circuitry are listed below:

- The assurance of identical arrival time when using DC-DC converters along with gate driver circuits [2].
- The ability to provide positive and negative bias voltages to drive the gate of the IGBT [10].
- The compactness of readily available integrated circuits (ICs) for isolated DC-DC converters
- Low rated power [11].
- The reduction of time spent to design the power supply circuitry.
- Low coupling capacitances [10].

As a result of the aforementioned analysis, an isolated DC-DC converter is the optimal choice for the purpose of designing an efficient gate driver. The first requirement when selecting the suitable isolated DC-DC converter is that it bears the voltage specification of the gate driver circuitry, and according to Table 1 in chapter 3, V_{GG+} is 15 V, and V_{GG-} is -8.7 V. The efficiency of the selected DC-DC converter should be high enough to ensure proper functioning. The ripple and noise transients should be very small. Taking this analysis into consideration, the optimal DC-DC converters for this design are offered by Murata Power Solutions and CUI Inc. The components' designated names are MGJ2D151509SC and VQA-S15-D15-SIP. A comparison of

the specifications of these two isolated DC-DC converters derived from these datasheet is shown in Table 2 [11], [12]. For the purpose of designing an efficient gate driver, MGJ2D151509SC is chosen since it has a higher isolation voltage and a lower ripple and noise transients than VQA-S15-D15-SIP.

Table 2. A Comparison of MGJ2D151509SC and VQA-S15-D15-SIP.

DC-DC Converter specification	**MGJ2D151509SC Values**	**VQA-S15-D15-SIP Values**
Nominal Input Voltage (V)	15	15
Output Voltage 1 (V)	15	15
Output Voltage 2 (V)	-8.7	-8.7
Output Current 1 (mA)	80	80
Output Current 2 (mA)	40	40
Ripple and Noise Typ. (mVp-p)	30	NA
Ripple and Noise Max. (mVp-p)	50	200
Efficiency Typ. (%)	76	80
Efficiency Max. (%)	80	80
Isolation Voltage (V)	5200	3000

4.3 Integrated Circuits for Gate Drivers

In chapter 3, the designer examined the gate driver circuitry requirements to produce a competent and complete design for a smart gate driver. In this chapter, the designer selects ICs that meet those requirements. In order to select an efficient gate driver IC according to chapter 3 analyses, the following requirements are needed:

- A safe and high isolation voltage.
- A 4A output current.
- An internal opto-/photo-coupler to reduce PCB area.
- Power supply voltage allowing V_{GG+} to be +15 V and V_{GG-} to be -8.7 V.
- An internal desaturation-detection function.
- An internal voltage-clamping function.

This analysis simplifies the research the designer has to do on selecting the best gate driver IC in the market. That is due to the fact that there are not many gate driver ICs that contain all of the above-mentioned intrinsic capabilities. After a careful exploration, two smart gate driver ICs are identified to have very similar capabilities and include all the aforementioned functions. These gate driver ICs are from TOSHIBA and FAIRCHILD Semiconductor Inc., and their designated part names are TLP5214 and FOD8318, respectively. A brief comparison between these two gate driver ICs is shown in Table 3 to help decide which one is better for the overall design [13], [14]; TLP5214 is better for this design since it has a smaller propagation delay time, a lower output power dissipation, and most importantly, the rated output current capability is more suited to drive the gate of the IGBT on and off.

Table 3. A Comparison between TLP5214 and FOD8318.

Gate Driver Specification	TLP5214 Values	FOD8318 Values
Peak Output Current (A)	+/- 4	+/- 3
Power Supply Voltage ,V_{CC}-V_{EE}. (V)	From 15 to 30	From 15 to 30
Common Mode Transient Immunity (kV/us)	+/- 35	+/- 35
Isolation Voltage (V_{rms})	5000	4243
Peak Clamping Sinking Current (A)	1.7	1.7
Output Power Dissipation (mW)	410	600
Propagation Delay Time (ns) (Max.)	150	500
Output Rise time (ns) (Typ.)	32	34
Output Fall Time (ns) (Typ.)	18	34

As a result of this evaluation, the TLP5214 is chosen as the IC for the overall design of this thesis. This isolated smart gate driver is also capable of softly turning the IGBT off during short circuits and under voltage lockout (UVLO), and is also equipped with a fault detection function, which sends feedbacks to the controller [13]. In the following paragraphs, the operation of the internal functions of this gate driver IC is discussed thoroughly. This adds to the discussion on section 3.2.2.

Desaturation-detection function

The TLP5214 is equipped with an internal function that monitors the collector-emitter voltage, v_{CE}, for overload protection purposes, and this internal function operates as follows: The TLP5214 IC has a pin, called DESAT, dedicated for desaturation detection. [15] That makes sure that v_{CE} does not exceed normally 6.5V when the IGBT is on. When an overcurrent happens, v_{CE} rises. Then, the DESAT pin detects the increase in the collector voltage, v_{CE}, and instructs the output voltage pin to softly turn off in order to avoid destructing the IGBT. Ultimately, the fault pin notifies the controller of an extraordinary activity in the system. According to the application note provided by TOSHIBA for the TLP5214, the soft turn-off process is very fast, and it only takes a maximum of 700 ns [15].

One problem that might arise from this pin is false de-saturation detection. [16] Negative bias voltage spikes that are caused by reverse recovery IGBT freewheeling diode might cause a false triggering in the DESAT pin. Connecting Zener and Schottky diodes between the DESAT pin and the emitter of the IGBT should solve this problem. The Zener diode clamps voltage spikes, and the Schottky diode stops the flow of the forward current in the built-in diode [16].

Active Miller clamp function

One of the common malfunctions of IGBT/MOSFET gate drivers is an unexpected increase in the gate voltage, v_{GE}, which causes a false turn-on. This unexpected increase in v_{GE} is due to the Miller capacitance that is connected between the collector and gate of the IGBT. This problem is usually solved by adding two back-to-back Zener diodes between the gate and the emitter of the IGBT [9]. This method clamps the gate to emitter when v_{GE} increases over the specified limit.

[15] Fortunately, the TLP5214 is already equipped with an internal function that performs the same function without having to add more components to the whole circuit. The designated pin is called V_{CLAMP}, which clamps the gate voltage, v_{GE}, and prevents short circuits [15].

4.4 The Final Design of the Smart Gate Driver

Up to this point, the power supply circuitry and gate driver circuitry are completely designed. All the other parameter were specified and designed in chapter 3. Therefore, the circuit design of the smart gate driver is finalized and shown below in Figure 6.

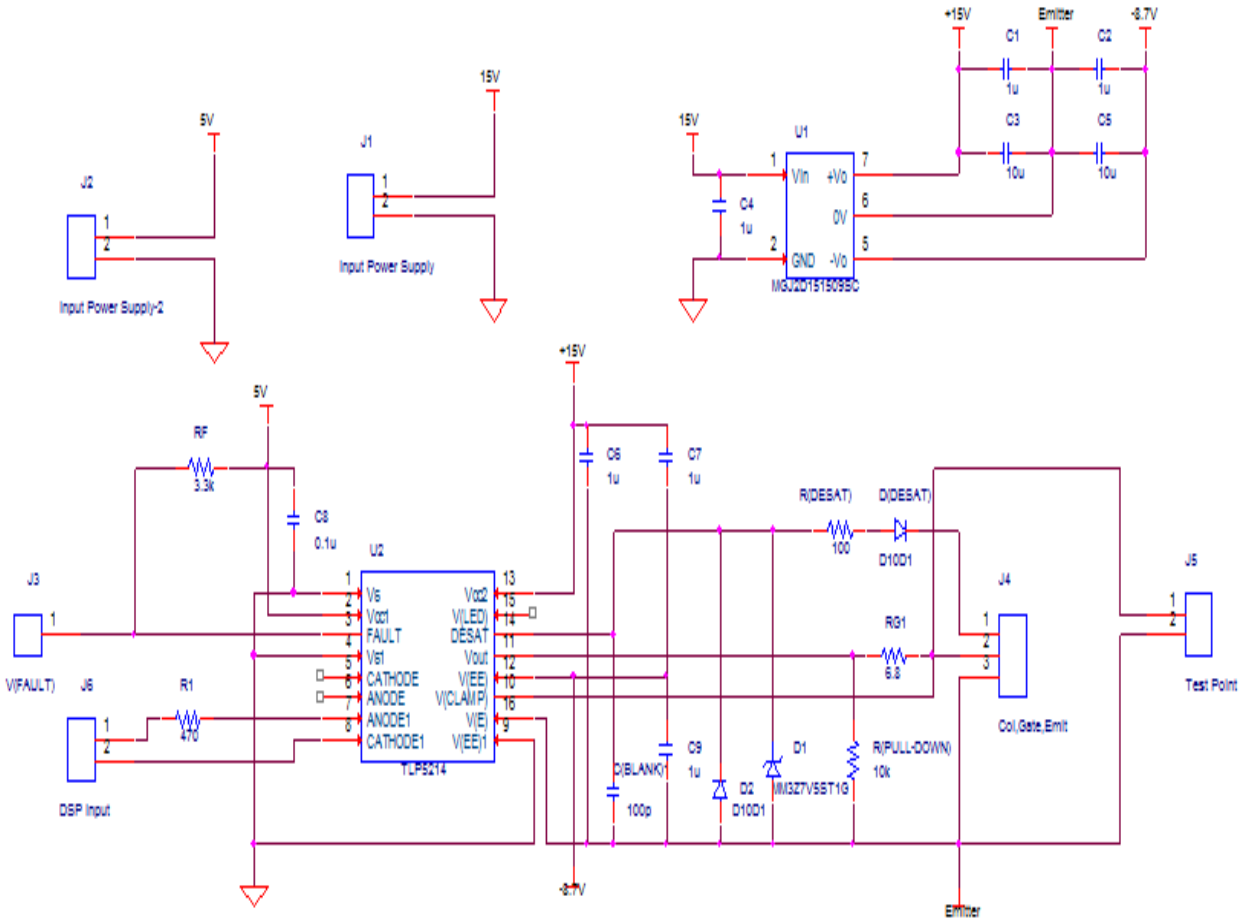

Figure 6. The final design of the smart gate driver.

CHAPTER 5

EXPERIMENTAL RESULTS

5.1 Introduction

A gate driver circuitry is always a part of a bigger circuit, because it is used to drive transistors that are used in this bigger circuit. Therefore, a gate driver circuitry is connected to an IGBT/MOSFET in a certain application in order to test its functionality. The chosen prototype circuit for testing for this project is a buck converter circuit. A simple buck converter was designed and milled out in order to test the gate driver designed in this thesis. The final designed circuitry of the buck converter is shown in Figure 7, and it was designed to have a 50V input, 50% duty cycle, 25V output, and a 2A output current. The PCB design of the buck converter was done in a way to enable the gate driver PCB to be mounted on it to reduce parasitic inductances between the gate driver IC and the IGBT/MOSFET.

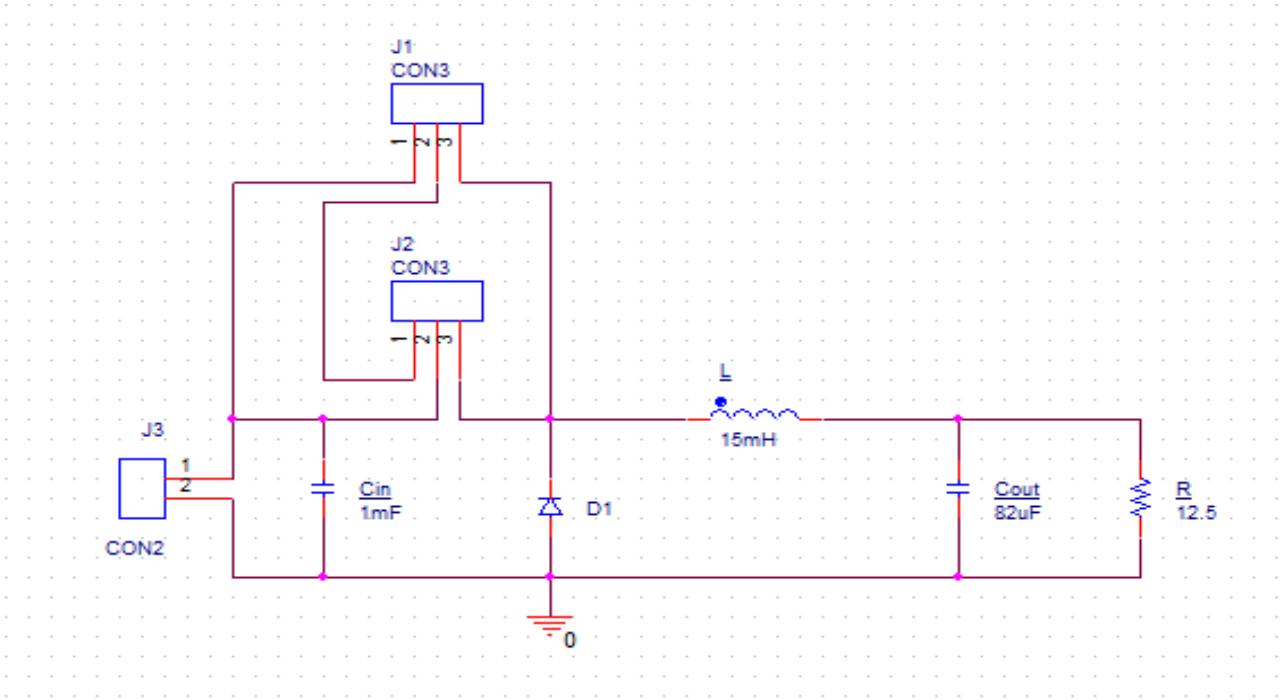

Figure 7. Final designed circuitry for a buck converter.

5.2 Experimental Result of the Designed IGBT Gate Driver

After mounting the gate driver PCB on the buck converter board and powering both circuits with the rated voltages specified in chapters 3 and 4, the designer started testing the gate driver circuit by measuring the gate-emitter voltage. The expected result from this testing was having a fine square wave showing 15V as an on-voltage and -8.7V as an off-voltage. Unfortunately, that was almost not the case. The result was a 15V square wave signal referenced to 0V. This meant that the negative supply voltage of -8.7V was not appearing at the gate of the IGBT/MOSFET. After a thorough investigation, it was found that pins 9 and 12 are shorted internally, which means that the turn-off voltage of the gate driver IC is 0V, not -8.7V anymore. The designer did not know this until the moment when testing the whole circuitry. This mistake was made because three examples using TLP5214 in its application note showed that it would be applicable if one of the two aforementioned pins was grounded and the other was providing the negative supply drive voltage. This is a complete contradiction since these two pins are shorted internally, and since they are shorted inside the IC, then they would always have the same value externally. Due to this problem, several capacitors in the gate driver circuitry was shorted as well, because they were connected between the emitter pin and the 0V reference of the DC-DC converter.

CHAPTER 6

CONCLUSIONS

6.1 Introduction

This thesis includes the design of a smart gate driver for a Si IGBT and SiC MOSFET. First, the main parameters of the IGBT were examined thoroughly to fathom out their impact on the whole design of the gate driver circuitry. Then, the designer did a detailed evaluation to identify proper integrated circuits for the power supplies, isolation circuits, protection circuits, and gate driver circuitry. Finally, a prototype circuit, which is a buck converter, was designed and built in order to test the gate driver PCB that was designed for this thesis.

6.2 Closing Comments About the Final Design

The primary values for the gate driver were designed after a comprehensive examination of their effect on the final design as shown in Table 1. Those values were chosen to meet all considerations that were mentioned in chapter 3, and they would greatly contribute to the final design of a very efficient gate driver. The DC-DC converter that was selected provides exactly what the designer actually set for the power supply rails. This means that this integrated circuit is able to carry out the supply voltage requirement of the gate driver circuitry, and it offers more featured applications than any other choice for power supply as explained in the analysis in chapter 4. After choosing the integrated circuits for power supply, the designer examined most gate driver ICs in the market in order to select the most suitable gate driver that meets all requirements and specifications discussed in chapter 3. TLP5214 was selected because it offers more capabilities than most of the other gate drivers, and it also meets the requirements that were set in chapter 3. A desaturation-detection circuit was also integrated into this gate driver design

in order to detect faults quickly and prevent destruction of the driven device. Another protection circuit, an active Miller clamping circuit, was added to the whole design to prevent false turn on of the IGBT. Ultimately, the integration of the aforementioned functions and circuits was finalized, and a smart gate driver circuit was designed and shown in Figure 6 in chapter 4.

6.3 Suggestions for Future Implementation of This Design

As explained in the previous chapter, this design experiment did not produce a negative voltage when turning off the device. The reason behind the failure in obtaining good results for the smart gate driver circuit was because of a wrongful representation of information from TOSHIBA. Pages 10 through 12, in the advanced version of TLP5214 application note show that pin 12 is grounded, whereas pin 9 is used to offer negative supply voltage for turn off (5). However, when these two pins were tested for connectivity using a digital multimeter in the lab, it was found that these two pins are shorted internally. Therefore, this is a contradiction because when two pins are shorted internally, they cannot have different connections externally. As a result, it is suggested, when using this gate driver in the future, to ensure connecting these two pins together in order to avoid losing the functionality of that pin.

Another suggestion that can enhance the implementation of this design in the future is eliminating the fault detection pin. By disregarding the fault detection network, more space can be available in the PCB. This means the whole design can be more compact, which has economic benefits as well as less parasitic inductances, which means better functionality. This fault detection network is not very beneficial in the whole design because it does not help in the

process of eliminating faults from the circuit; it only tells the user when a fault occurs to keep track of when faults usually take place.

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