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A Folded Cascode Operational Amplifier with Wide-Swing Current Mirrors and High ICMR, Designed with a 1.2-micron Silicon-Carbide Process

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A Folded Cascode Operational Amplifier with Wide-Swing
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Silicon-Carbide Process

A Folded Cascode Operational Amplifier with Wide-Swing Current
Mirrors and High ICMR, Designed with a 1.2-micron Silicon-Carbide
Process

An Undergraduate Honor's Thesis

in the

Department of Electrical Engineering

College of Engineering

University of Arkansas

Fayetteville, AR

By

James Austin Gattis

Abstract

This thesis describes in detail the process of designing, simulating, and creating the layout for a modified folded cascode op-amp, fabricated with silicon carbide MOSFETS. The modifications consist of using a wide-swing current mirror to help deal with output voltage issues stemming from high threshold voltages in the silicon carbide process, as well as using a modification that allows for an increased input common mode range. The folded cascode op-amp uses silicon carbide transistors, as it is intended to be used for high temperature applications, ideally in the 25 °C – 300 °C range. It is designed to have 25 dB of gain and approximately 70 degrees of phase margin. These qualifications were met, and the layout was successfully created and fabricated. Future testing of the fabricated folded cascode will be conducted to compare the measured and simulated result.

Acknowledgements

There are many people that I must show my thanks, as I have absolute certainty that I would not have been able to who I am and where I am today without the help of so many people in my life. I thank my parents, James Gattis and Jammie Moore, for offering me support in every aspect of my life for the past 23 years. I thank my friends for always being there for me and for being a 2nd family to me. I thank my coworkers from the IC design group and Dr. Mantooth especially, as he has allowed me to work for him as an undergraduate assistant for nearly two years and is the sponsor for my thesis. This would simply be impossible without him. Finally, I must offer the most sincere and well-deserved thanks to my Fiancé, Julia Sexton. She has been with me every step of the way with her unwavering support, just as she will continue to be there to support me as I begin perusing my master's degree. Once again, I offer my sincere thanks to everyone who has been part of my life, thank you.

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I. Introduction

The purpose of this thesis is to describe the process of designing, testing, and laying out a folded cascode op-amp. This op-amp is not designed in the typical folded fashion, but is instead the subject of a few modifications. The report will describe the primary modifications, such as using a wide swing current mirror topology and having a rail-to-rail input common mode operation.

First, the process of design will be described. This will include the reasoning behind the modifications and the purpose for designing the op-amp in the first place. Next, the testing procedure will be detailed, showing gain and phase responses and their relationship to changing temperature. Finally, the layout procedure will be detailed, as the design was laid out and fabricated using the Fraunhofer process.

II. Design

The design process began with the notion of analog to digital conversion, specifically by way of the sigma-delta modulator. The idea was that there was a clear usefulness to designing a sigma-delta modulator integrated with silicon carbide transistors to ensure high temperature reliability. The process of designing the entire system is extensive for current fabrication runs, so instead focus shifted towards designing the operational amplifiers that compose the converter. Figure 1 below shows a typical sigma-delta modulator design.

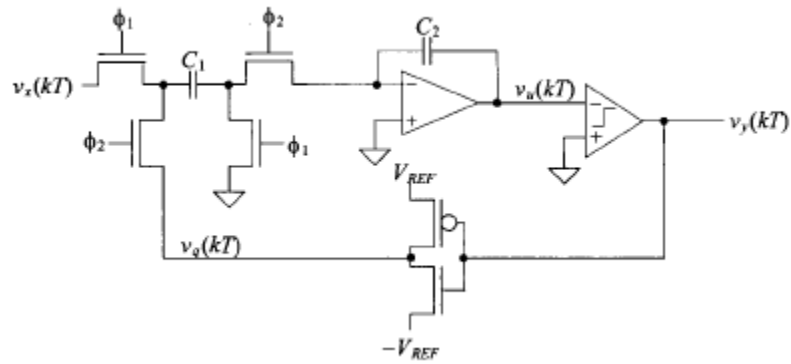


Fig 1. Sigma-Delta modulator schematic [1].

In the process of choosing which op-amp to design, attention was quickly diverted to the typical folded cascode setup, which appears in figure 2. In an effort to go beyond the typical folded cascode setup, several modifications were researched. The two that ultimately were implemented were modifications meant to increase the input common mode voltage and to increase the output voltage range by way of a wide-swing current mirror.

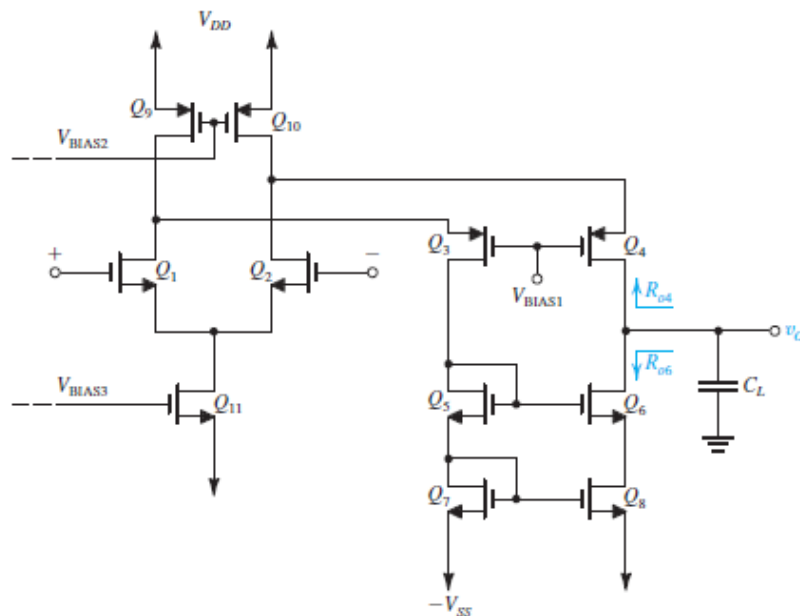


Fig 2. Typical folded cascode op-amp [2].

swing in the negative direction is always reduced by the threshold voltage, V_t [2]. This is especially problematic for silicon carbide designs, as it has been well-established that SiC circuits suffer from high threshold voltages. Seeing as how this could potentially limit the output swing of the folded cascode greatly, it was desirable to find some kind of work-around.

Fortunately, the work-around is well-established, specifically in the form of a wide-swing current mirror. An example of such a current mirror appears in figure 4. For this topology, the changes made and the use of a biasing network means the output voltage is now at a minimum value of $2|V_{ov}|$ instead of $2|V_{ov}| + V_t$, meaning it no longer relies on the threshold voltage to say how close it can get to its supply rails. This is incredibly useful for silicon carbide based circuits, as now the output swing is no longer restricted by the threshold voltage, which is known to be quite large for such cases.

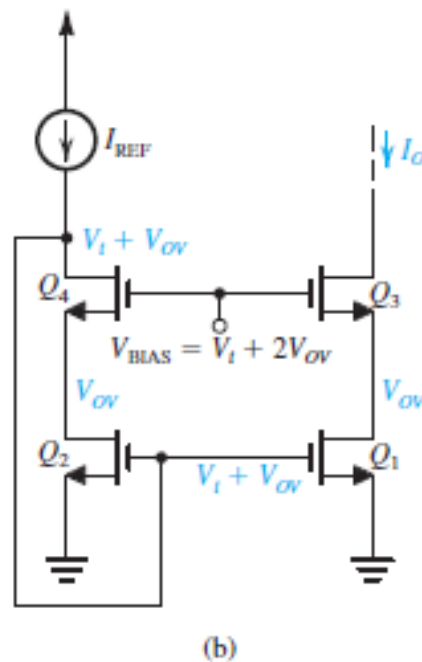


Fig 4. Wide-swing current mirror [2].

With the major modifications made, the modified folded cascode op-amp was created. The schematic used for this thesis appears in figure 5. It's accompanying biasing network appears in figure 6.

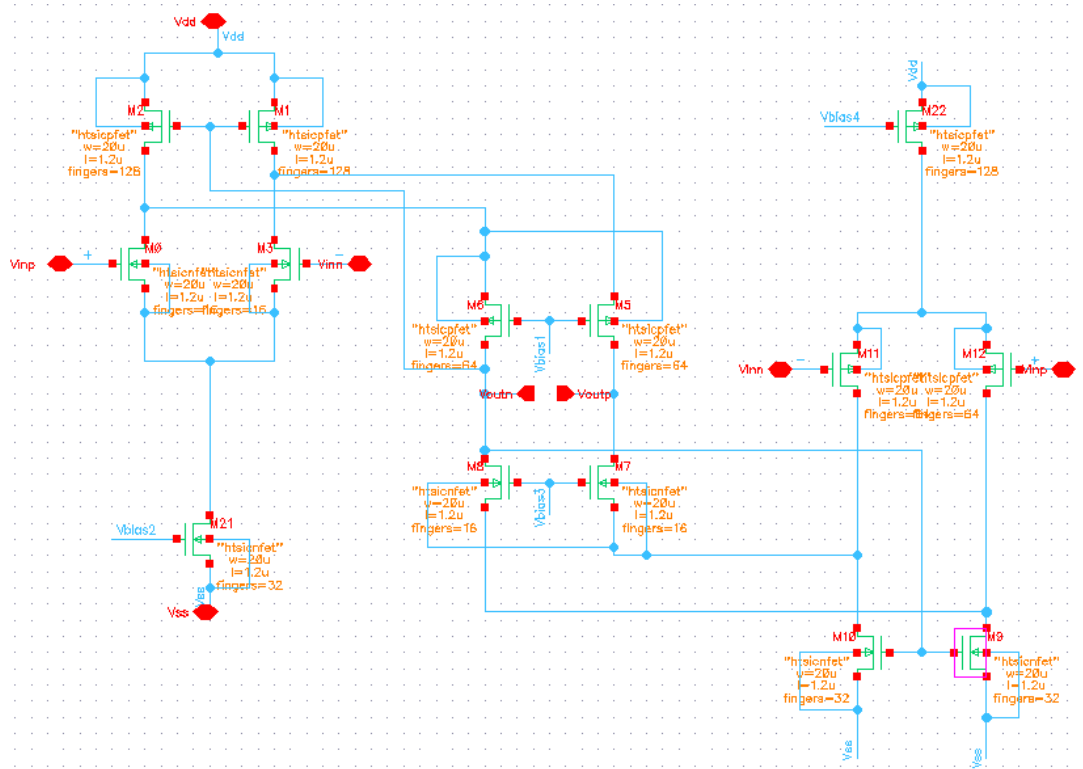


Fig 5. Finalized modified folded cascode schematic.

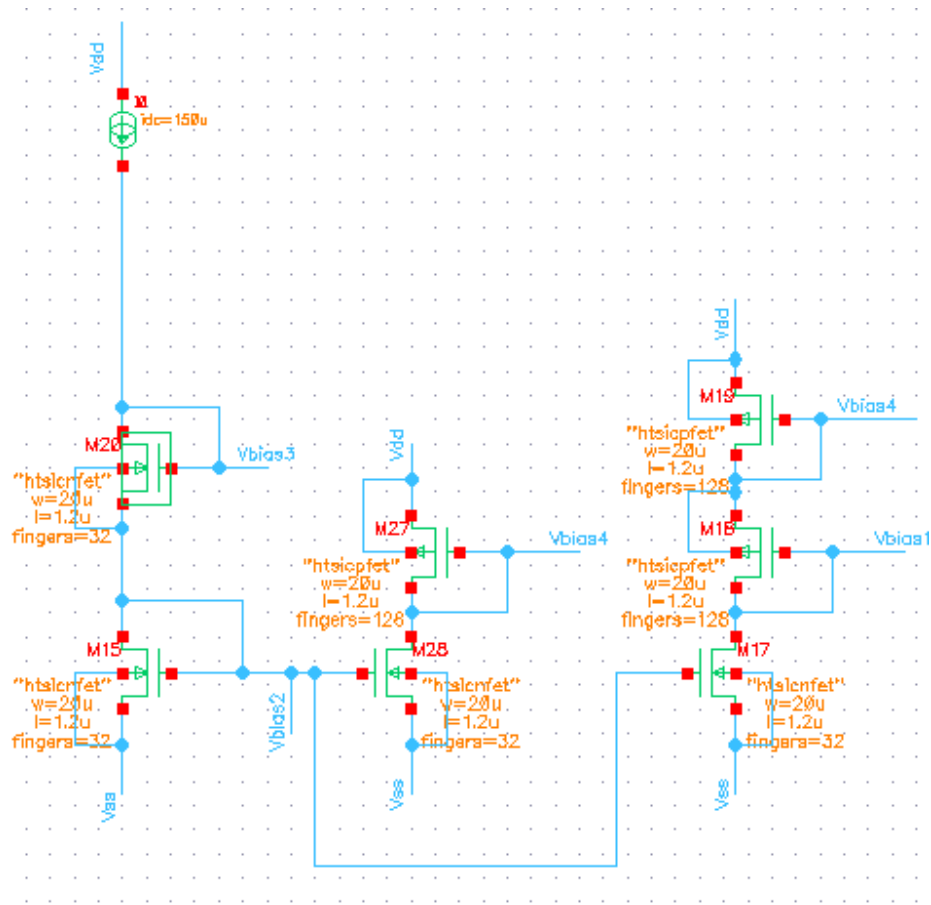


Fig 6. Finalized biasing network for folded cascode schematic.

It is useful to add detail to the sizing of the transistors of the schematic. For this process, each transistor used was a multiple of the 20u/1.2u ratio. The specific number of fingers for each transistor was determined based upon the current flow of the circuit. For instance, if one started with sizing M21, then the current would evenly split (ideally) between transistors M0 and M1, meaning that they need to be half the size of M21. This method of sizing was used throughout the circuit. For the folded cascode circuit, the appropriate aspect ratios appear in table 1.

Table 1: Transistor Sizes

Transistor	Aspect Ratio (W/L)
M0, M3, M7, M8	16
M1, M2, M22	128
M5, M6, M11, M12	64
M9, M10, M21, M22	32

Few modifications were made from the original circuit that combined the topologies of figures 3 and 4. That being said, some changes did occur. Specifically, the way the body connections are made in the two central transistor pairs, M5/M6 and M7/M8, changed slightly from what was initially expected. Originally, each PFET in this configuration had their body connections tied to their source, but modifications were made to alleviate issues in the layout stage, which will be elaborated on later. Other than this, alterations were minimal.

Table 2 shows the design specifications for the folded cascode op-amp. Many of these values were obtained from analyzing past designs using silicon carbide transistors or from operational amplifiers in general. The gain of 25 dB is not large but considering no buffer stage is used on this amplifier, it is still reasonable. The input common mode range for this circuit is also ideally high, as mentioned in the problem statement. The other values are rough estimations of what was expected from simulation.

Table 2. Design Parameters

Design Specification	Value
V_{dd}	15 V
V_{ref}	7.5 V
V_{sin}	10mV
Sampling Frequency	100 kHz
Capacitive Load	5 pF
Temperature Range	25 °C – 300 °C
DC Gain	25 dB
Phase Margin	70 °
ICMR	0 V – 10 V

III. Simulation

Once the parameters had all been set to something reasonable, work immediately began on simulating the circuit. The first simulation was an AC response to test the DC gain of the circuit, the phase margin, the Unity Gain Band Width (UGBW), and the corner frequency. The corner frequency is often referred to the 3 dB frequency and even as the bandwidth in some textbooks, though here it strictly refers to the point at which a 3 dB drop has occurred from the maximum gain. The UGBW refers to the frequency at which the gain is 0 dB, as the name suggests. The gain and phase response at 300 °C appear in figures 7 and 8. It should be noted that all simulations in this document were done using typical-fast models (TF).

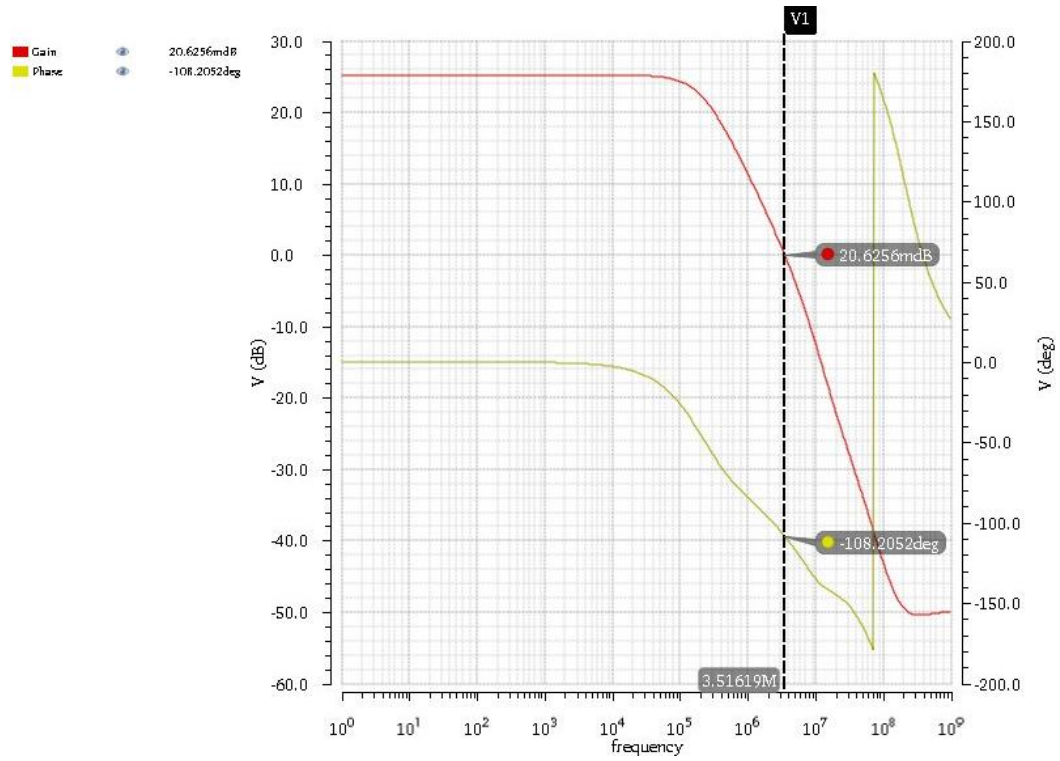


Fig 7. Gain and phase response at 300 °C.

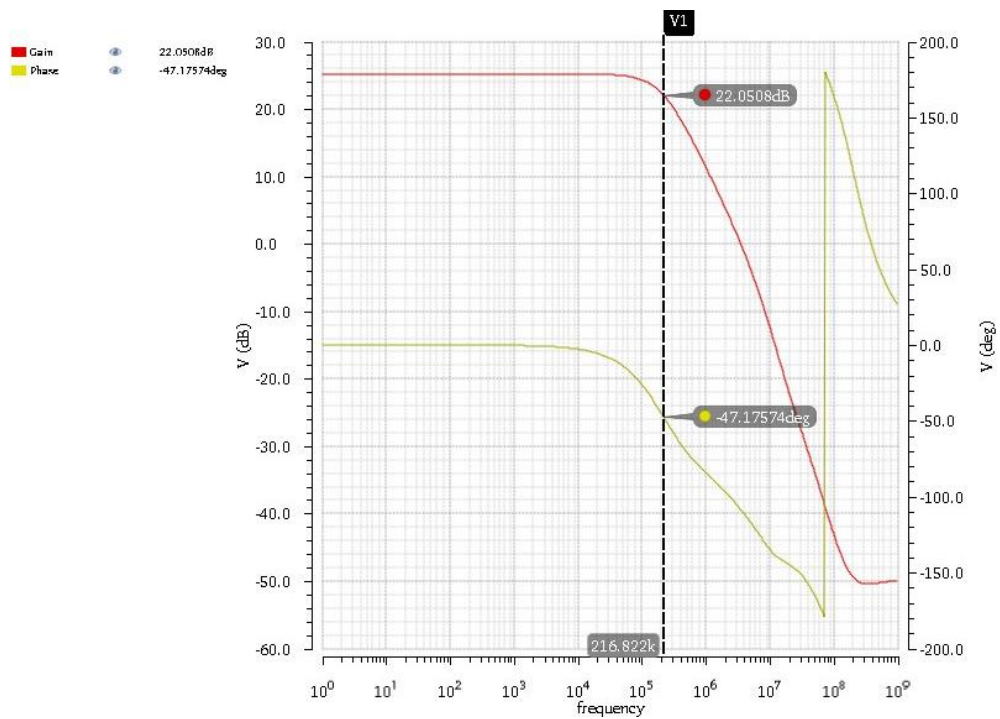


Fig 8. Corner Frequency at 300 °C.

These results clearly show that the DC gain is about 25 dB, the phase margin is about 72 degrees, and the UGBW is 3.5 MHz. Figure 8 shows the 3 dB frequency, which is approximately 217 kHz.

The next test done was to find the ICMR. Essentially, the reference voltage was swept from 0 to 15 V and the DC gain was plotted against it. The stable range of values included anything within 3 dB of the max gain, which was approximately 25 dB. This meant the range was from around 3.1 V to 11.2 V. This range would be larger, but the operating range was strictly defined as being in the range from maximum gain, only down to a 3 dB drop. If one were to expand this down to 15 dB, then it would nearly reach 0 V on the lower end. The results appear in figure 9.

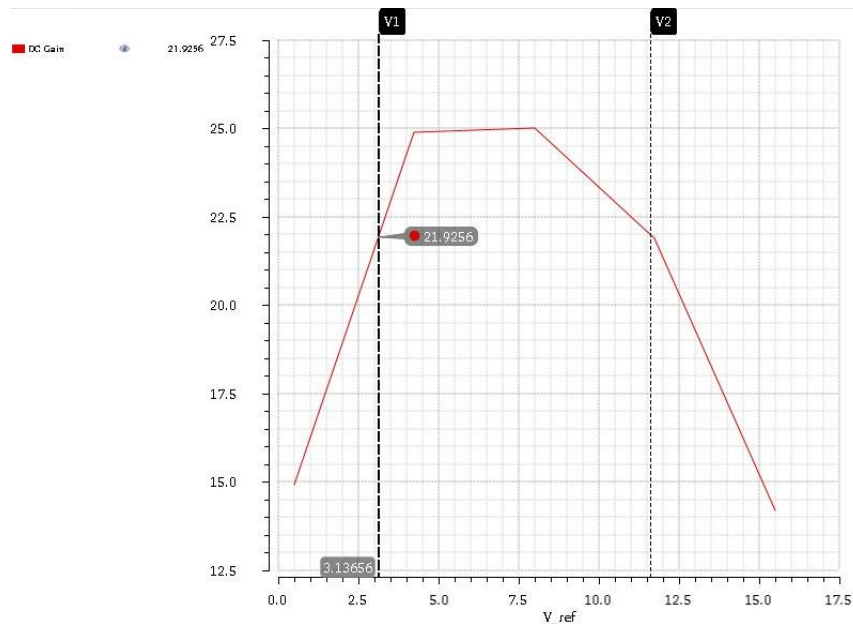


Fig 9. ICMR Test

The summation of all the data obtained appears in table 3, specifically for tests at 300 °C. As expected, the simulated values largely coincide with the expected ones. The ICMR range may initially appear as being small, but that is only due to restriction. Again, this is only reduced because of the stringent range of operation being defined as being from a 0 to a 3 dB

drop from maximum gain. Overall, the gain, phase, and general frequency response of the circuit is adequate, especially for its intended use for a test run of a new, silicon carbide based process.

Table 3. Simulated Results

Parameter	Value
DC Gain	25 dB
Phase Margin	72 °
UGBW	3.54 MHz
Corner Frequency	217 kHz
ICMR	3.1 V – 11.7 V

For comparison's sake, table 4 shows the data spread across temperature. It is expected that the circuit should perform better the closer it gets to 300 °C, though it was initially hypothesized the difference between tests at 300 °C and 100 °C would be further apart than they currently appear.

Table 4. Comparisons Across Temperature

	300 °C	200 °C	100 °C
DC Gain	25 dB	25 dB	24 dB
Phase Margin	72 °	72.5 °	73 °
UGBW	3.54 MHz	3.37 MHz	3.26 MHz
Corner Frequency	217 kHz	200 kHz	194 kHz
ICMR	3.1 V – 11.7 V	3.4 V – 11.9 V	3.5 V – 11.1 V

IV. Layout

With the device adequately simulated, work began on creating the layout. The first principle of design used was the common-centroid approach. This approach is ideal when one is concerned about process variations, especially when dealing with transistor pairs. Considering almost every transistor in the folded cascode topology has a pair and there is already concern over process variations since novel processes are being used, this approach is a necessity. Jacob Baker provides an example of how this process works with a layout of four matched resistors, as seen in figure 10. For the folded cascode topology, it only used half of this, so an A and a B, since it dealt with a single pair. For example, consider transistors M1 and M2. Each has 128 fingers. So, if one were to follow the common-centroid approach on the layout, each transistor would be split into 8 sub sections, meaning M1 and M2 each would have 8 sections of 16 fingers. These sections would alternate in the way seen in figure 10. This idea was repeated for each pair, meaning every transistor but M21 and M22 of the folded cascode.

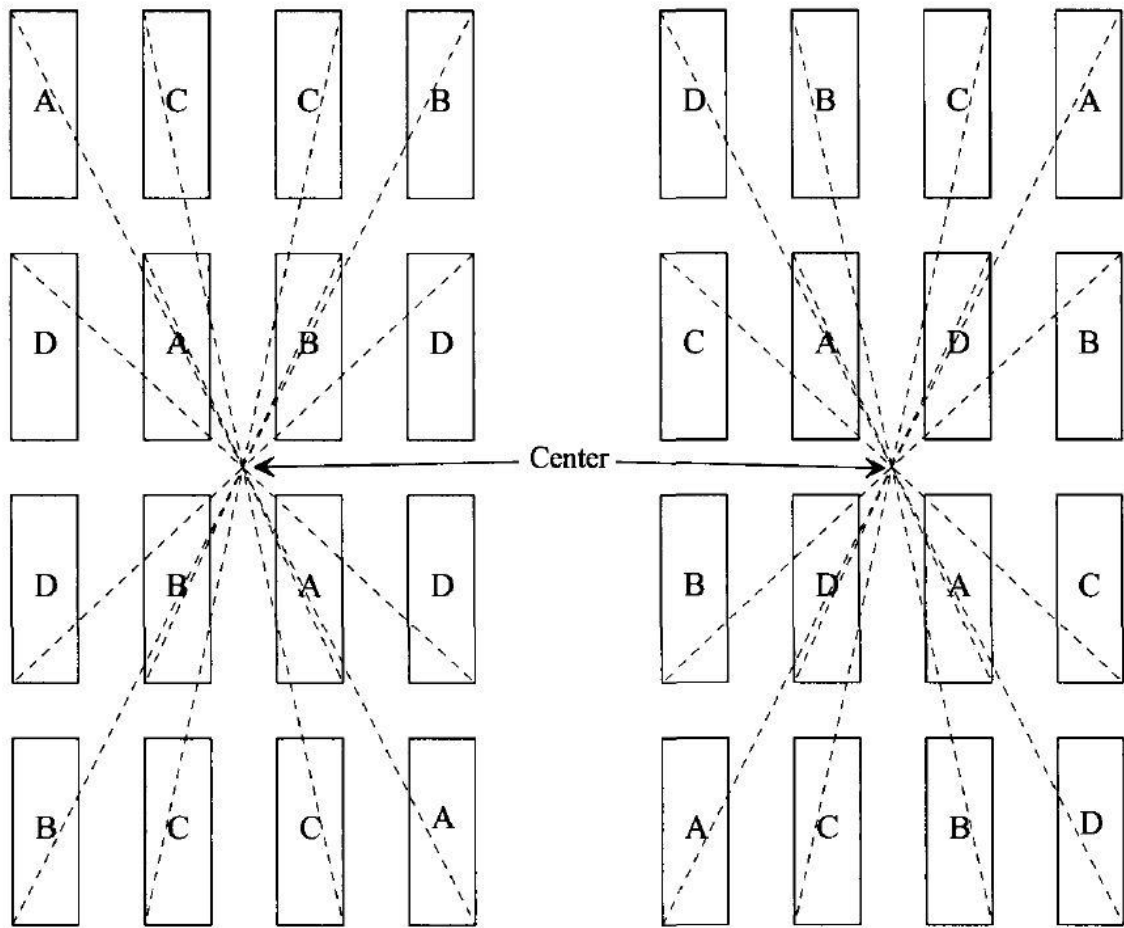


Fig 10. Common-centroid approach to layout [1].

This sort of layout was repeated for each transistor pair. The next challenge was integrating each pair in such a way that space was not wasted, and connections didn't have to be overly long. Thankfully, the new process used to fabricate this circuit allowed for two layers of metal in the design. This allowed for a less convoluted design, though the process still can not be considered simple. This is especially true for the two central transistor pairs, M5/6 and M7/8, as they did contain a common source connection between pairs, as did each other transistor pair. Figure 11 shows the completed layout, where you can see additional

complexity on and surrounding those two transistor pairs. Also of note in figure 11 is the top left corner, which is entirely dedicated to biasing the design.

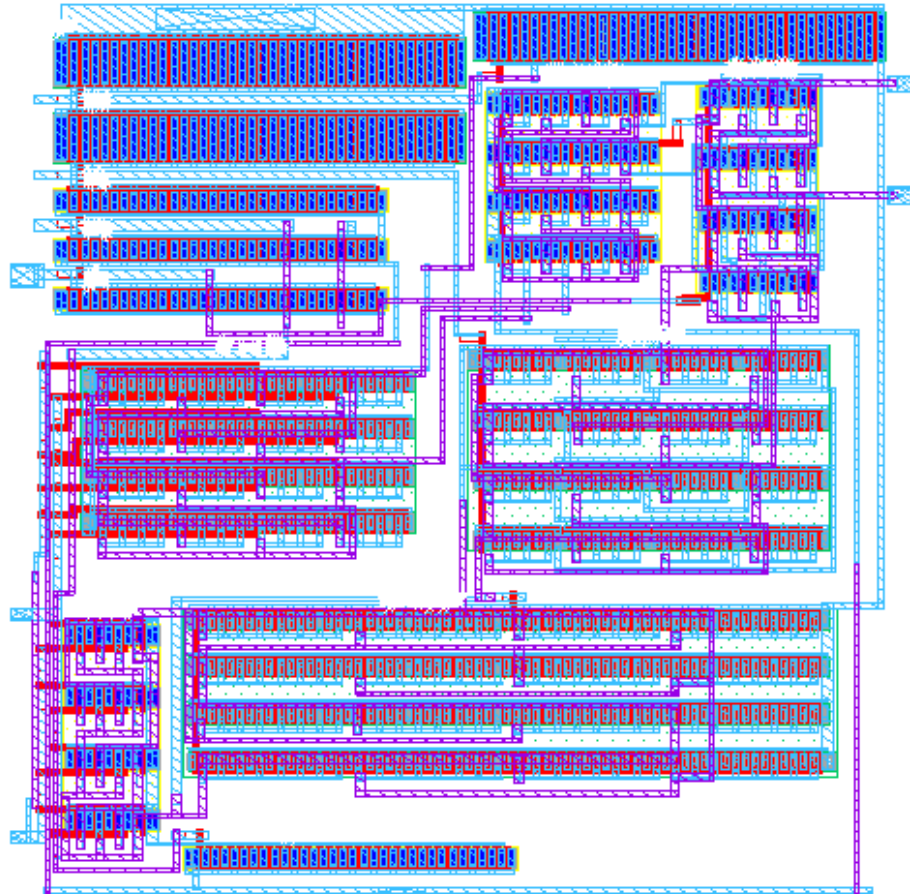
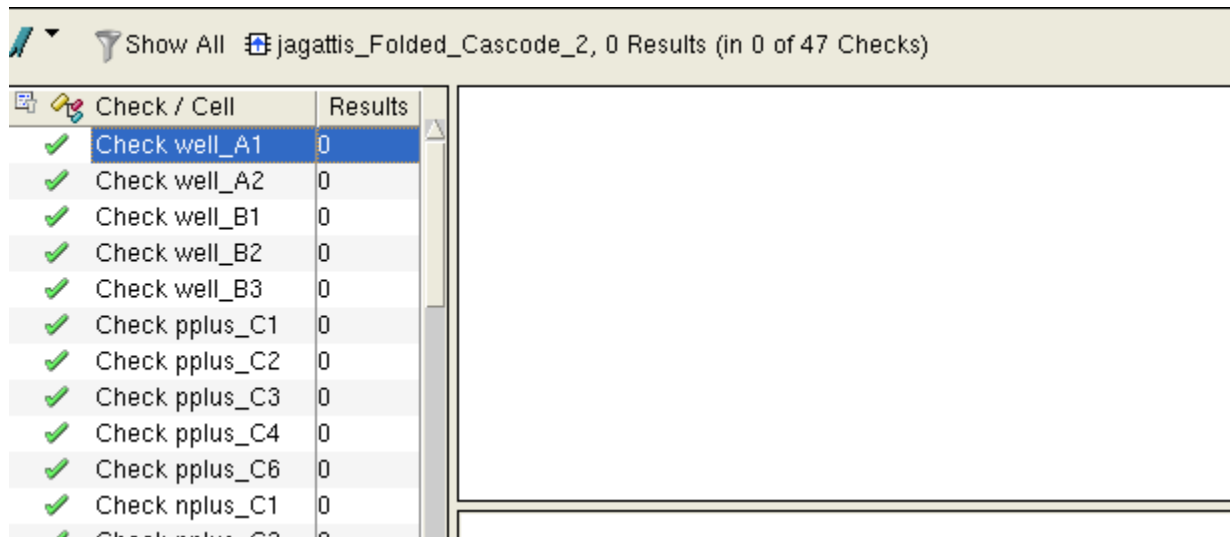


Fig 11. Completed layout.

For reference, the blue refers to metal 1 layer, the purple to metal 2 layer, and the red to the poly layer. The biggest challenge faced when creating this layout was figuring out a way to have so many transistor pairs close together and yet far enough away so that convolution can be kept at a minimum. For future designs, focus needs to be on compactness. The layout depicted in figure 11 has too much free space, so much so that it is believed the layout could potentially be cut in half in terms of total area. That being said, the process used to fabricate

this op-amp was not terribly size limited, meaning compactness was not incredibly important. Focus on this layout was instead on transistor placing and on having the transistor pairs themselves by efficient and more immune to process variation than anything else. By following the common-centroid approach whenever possible, this was hopefully done. The layout depicted in figure 11 was sent out for a project tapeout in March 2018 as part of a project from Dr. Mantooth's IC team, so this means it can be fully tested in the near future. As for layout checks, figures 11 and 12 show the completed DRC and layout checks. This indicates that no fabrication rule was broken, and the schematic perfectly matches the layout. Assuming the fabrication process works and that schematic was designed correctly, which seems to be the case from the simulation results, then the circuit should work as intended once fabricated.



The screenshot shows a software window titled "jagattis_Folded_Cascode_2, 0 Results (in 0 of 47 Checks)". Below the title bar is a table with two columns: "Check / Cell" and "Results". The table contains 13 rows of data, each with a green checkmark icon in the first column and the number "0" in the second column. The rows are: "Check well_A1", "Check well_A2", "Check well_B1", "Check well_B2", "Check well_B3", "Check pplus_C1", "Check pplus_C2", "Check pplus_C3", "Check pplus_C4", "Check pplus_C6", and "Check nplus_C1".

Check / Cell	Results
✓ Check well_A1	0
✓ Check well_A2	0
✓ Check well_B1	0
✓ Check well_B2	0
✓ Check well_B3	0
✓ Check pplus_C1	0
✓ Check pplus_C2	0
✓ Check pplus_C3	0
✓ Check pplus_C4	0
✓ Check pplus_C6	0
✓ Check nplus_C1	0

Fig 11. DRC Results

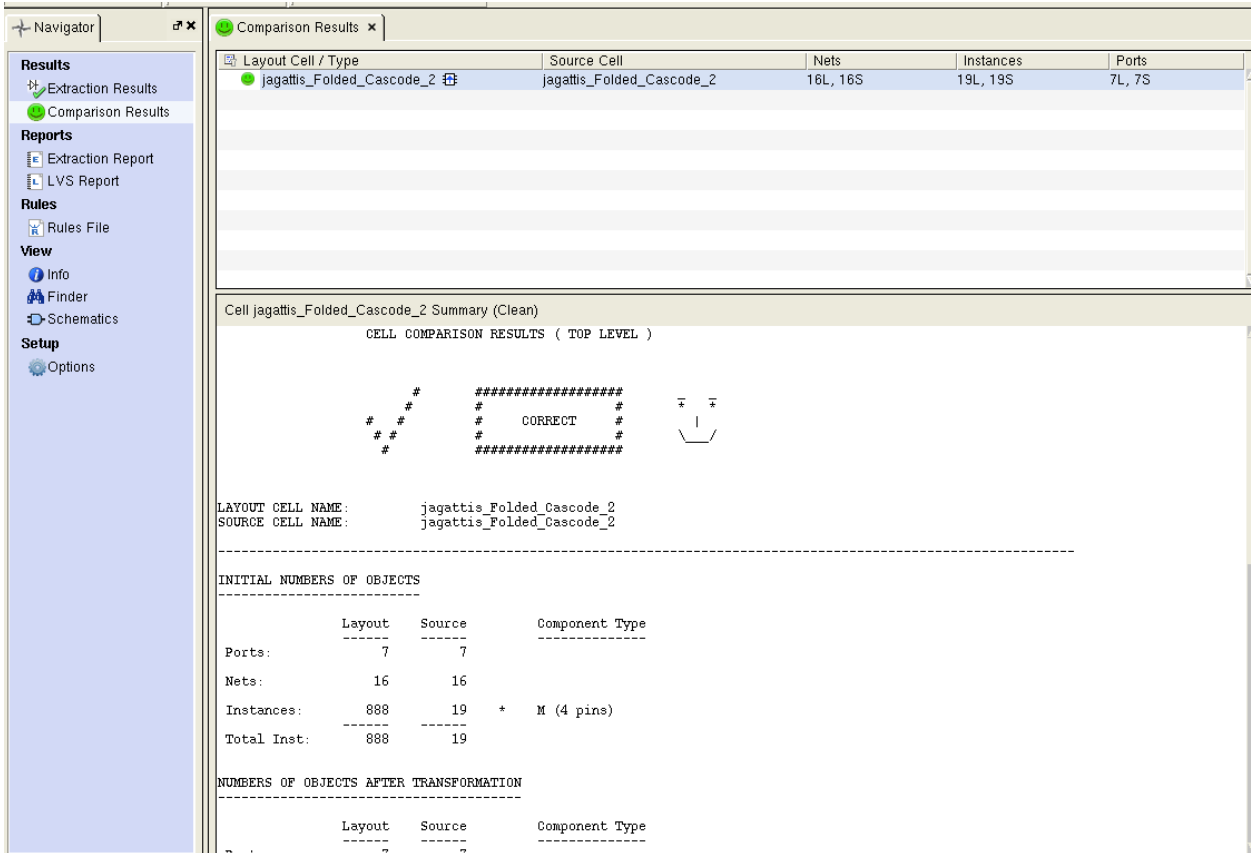


Fig 12. LVS Results

V. Conclusions and Future Work

The initial goal of creating a folded cascode op-amp with silicon carbide transistors, modified by having wide-swing current mirrors and an improved ICMR appears to have been met. The data obtained largely matches the expected result, with the exception of the ICMR. The ICMR is slightly reduced, as it was decided to define anything exceeding a 3 dB drop as being outside the acceptable range. If this strictness were to be reduced, then the range would be as large as initially predicted. Besides this, the design was seemingly a complete success.

Future work is also quite clear. Since this design was actually fabricated, the next test is to test the fabricated circuit to see how the actual results compare to the simulated and

suggested values. This will be the best indicator of functionality but won't be able to be done for several months at best. In the meantime, tests could continue to compare the ICMR between a typical folded cascode with this one to see how their ranges compare and to help troubleshoot some of the lingering issues.

Finally, as initially suggested, this op-amp was intended to be used as part of a sigma-delta modulator. Future tests would see this implementation realized. This would ideally be done with the next run of the same fabrication style used for this thesis.

VI. Appendix A: References

[1]. Baker Jacob, CMOS: Circuit Design, Layout, and Simulation, 3rd edition. Piscataway, NJ

United States of America: IEEE Press, 2010.

[2] Smith Sedra, Microelectronic Circuits, 6th ed. New York, United States of America: Oxford

University Press, 2006