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Chip-Package Interfacial Stress Analysis and Reliability Implications for Flip-Chip Power Devices

Jonathan GH Treco
University of Arkansas, Fayetteville

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By

Jonathan GH Treco

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University of Arkansas

Abstract

The solder in flip-chip assemblies experience high stress and strain because of thermal mismatch induced deformation. These deformations occur because of the differences of coefficient of thermal expansion between flip-chip assembly materials. The similarly in stress profiles between thermal induced and shear induced stress in solder joints enable the use of die shear testing as a representative technique for relating the max stress the flip-chip can withstand to cyclic thermal fatigue failures. In this work, two electronic device sample preparation types are evaluated: One set of samples are soldered together and other set of samples use epoxy as an adhesive. The soldered samples will have different temperature histories to observe how the max stress is affected by operating environments. For the epoxy samples there will be a sensitivity analysis between the adhesive height and temperature change to conclude what effects solder joint stress more. For solder samples, the temperature history (bake time in oven) decreases the max shear stress in the solder but due to sample limitations, knowing exactly how much is still undetermined. For epoxy samples, as temperature change doubles max interfacial and peeling stress doubles. When gap height doubles interfacial stress decreases by 29.29% and peeling stress decreased by 36.23% (traction free boundary) and 29.74% (periodic boundary).

Introduction

A power module provides the physical containment for several power electronic components, consisting of power semiconductor devices and passive elements, often on a single circuit board. The purpose of power electronic components is to control and convert electrical energy under the design conditions of the device. These power semiconductor devices, commonly called dice, are typically soldered or sintered onto a power electronic substrate that carries the power semiconductors; This allows electrical & thermal contact between the layers and electrical insulation where needed in the package. Silicon is the most popular material for semiconductor devices; it is usually chosen because of the low cost of raw material, simple processing and suitable temperature range. Power modules are so integrated today that they are found in applications like: appliances, battery chargers, inverters, medical electronics, switches, power supplies, HVAC Heater & Motor controls, power factor correction and many other industries. Some, but not limited to industries are: renewable energy, power plants and industrial machinery.

A die is a block of a semiconducting material where a circuit is fabricated on. To create dice photolithography is an essential process that uses light emission and some chemical processes to engrave desired geometric pattern onto the wafer. These engraved circuits are usually produced in large sets on a single wafer which is then diced into many identical copies, each copy being a die. Figure 1 shows the dicing process.

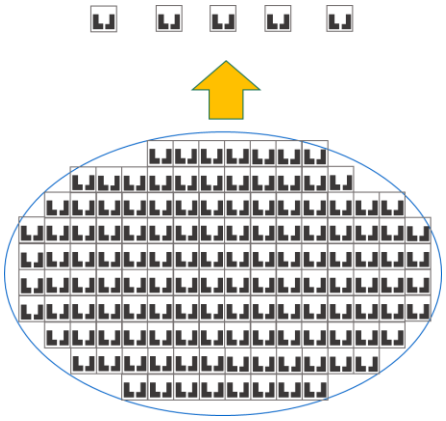

Figure 1: Process of wafer being diced

The power electronic substrate's purpose is to 'sandwich' the interconnects to create an electrical circuit and cool the power components. The substrate can carry high currents, high voltage insulation and capable to operate wide temperature ranges (usually up to 150°C-200°C). Understanding the limitations of what the components can handle is necessary in creating a reliable power module. FR-4 is a common substrate material used in Printed Circuit Boards (PCBs). FR-4 substrates are often used because the material is flame retardant, has negligible water absorption, a high strength to weight ratio and preserves its mechanical and dielectric properties in both humid and dry environments. The advantage of using PCBs is that the substrate can be multilayered to create complex circuits whereas Direct Bonded Copper (DCB) substrate is single-sided. Other advantages include that it is inexpensive to mass produce and all components are fixed on the board which increases the simplicity of use.

Research in power density improvement is of great value for these devices. Power packages provide a higher power density and are in many cases more reliable than discrete power semiconductors. The use of flip-chip configuration is now common in power packaging replacing wire bonding because it is more capable for high power density and longer module lifetime. Figure 2 shows the difference between the 2 configurations.

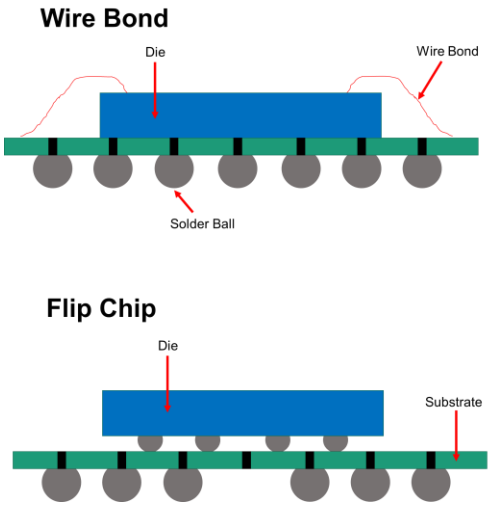

Figure 2: Wire Bonding and Flip Chip Configuration

The demands of decreasing the sizes of components at a given power while maintaining reliability with enhanced thermal management is a challenge. Thermal and mechanical stress concentrations are placed on reduced material sizes which introduce early thermo-mechanical failure in the device. These stresses must be evaluated to meet the demands of customers. Component improvements/alterations and manufacturing innovations are the goal of both companies and universities in this industry. New and improved materials being manufactured may also improve the overall reliability capabilities of the power package.

Power devices in high temperature applications are comprised of silicon carbide which has demonstrated greater power density and stability at high temperatures. Higher power density will create more heat in the device, which in turn means more thermal expansion of the materials. This will create more stress on the solder joints with creates a reliability concern.

Reliability Concern for Flip Chip

The development of miniaturizing while improving overall performance to increase power density has lead into an increase demand in flip chip assemblies. Thermal mismatch deformations occur due to coefficient of thermal expansion differences between the assembly materials. This creates high stress and strain in the solder joints. A common reliability test to determine the performance of the solder joints is the accelerated temperature cycling test. Creep deformation also occurs and is involved with fatigue failure in the solder joint. “The low cycle fatigue failure response of the solder joints in a creep-fatigue mechanism which involves crack initiation and crack growth until complete rupture of the solder connection”[1]. Once most/all solder connections rupture the circuit shorts to result in total part failure shown in Figure 3. Max stress was observed at the top edge of the solder joint where the crack initiates. This effect was illustrated by Li, et al. (2009) and is shown in Figure 3. Intermetallic diffusion also occurs between the solder and the

die layer as heat energy is added to the system. This energy begins to change the microstructure of the layer which usually increases the strength but also makes it more brittle. This factors in the crack initiation and propagation in the solder joint.

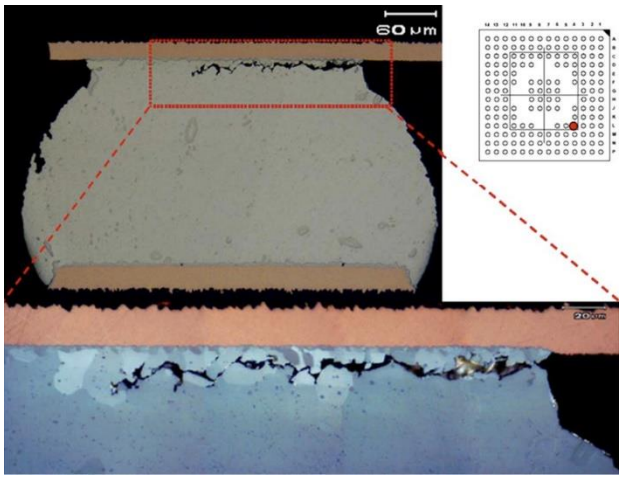

Figure 3: Crack Propagation in Solder Joint [2]

Quantitative Test Method

Accelerated temperature cycling (ATC) is when samples are systematically being switched between high and low temperatures. For flip-chip assemblies the range is usually between -55^{o}C to 125^{o}C, the peak temperature usually up to .87 of the melting temperature of the solder. Usually the cycles run between the boundary temperatures for 15 minutes and 15 minutes at each extreme temperature. Figure 4 is an example of 2 cycles of ATC.

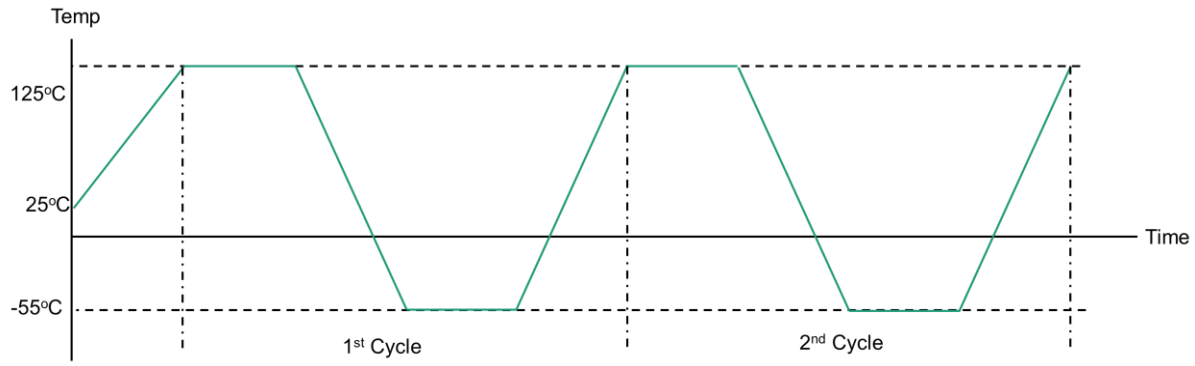

Figure 4: 2 Cycle example of ATC

While the temperature cycles are occurring, there are equipment attached to monitor the daisy chain to detect every failure, temperature cycle number, temperature of failure and time it occurred. Thermocouples are attached to the samples' substrate, die or close to the solder joints to monitor the temperature throughout the experiment. Before testing, failure is defined by the experimental team and failure analysis is done using electrical checks, x-ray review, ultrasonic viewing etc. Temperature cycling is done to emulate the temperature cycling the device will experience during operation as a means of estimating its total life expectancy.

Die shear testing is a mechanical test to evaluate the peak shear stress the flip-chip device can withstand. This is important because stress concentration profiles of thermal induced and shear stress are similar. It also is a useful quantitative value because at that stress the sample can only withstand 1 cycle. Figure 5 illustrates fatigue behavior of materials, where stress and number of cycles define the sample's potential lifetime as well as its potential endurance limit.

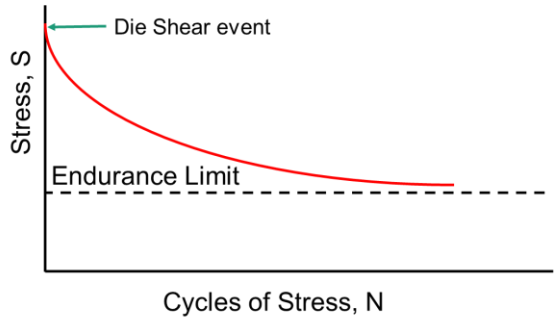

Figure 5: S-N diagram showing endurance limit for cyclic stress

The goal is to increase the reliability of the device and to accomplish that knowing how the peak shear stress correlates with the life expectancy of the device. Figure 6 shows the stress profiles inside of the solder innterconnects for both thermally induced and mechanically induced shear stress on solder joints, as measured in a 10x10mm SiC flip-chip device placed on a FR-4 substrate.

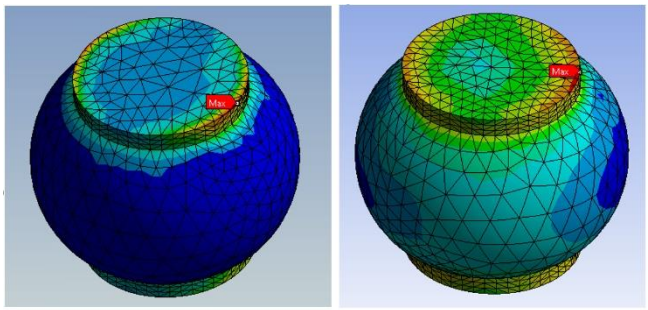

Figure 6: Stress profile of mechanical shear induced (left) vs thermal induced of solder joint using ANSYS

Although the stress profiles and stress distribution are not identical, the peak stress locations are very similar, so die shear testing is a good representation of how cracks may form during repeated thermal cycles during the life of a flip-chip device.

Problem Statement

Power modules have a design challenge with reliability due to high temperatures demands in the system. The thermal expansion and contraction places stress on the interconnects and interfaces due to the differences in the die's and substrate's coefficient of thermal expansion.

Objective

The goal is to understand and determine the thermo-mechanical stress that creates a reliability risk in the flip chip design to later optimize the life of the device. This will be done by locating the samples' max shear stress it can withstand and conducting a sensitivity analysis of epoxy samples. Understanding its max shear stress will impact the cyclic life of the device.

Theory

To calculate the max thermally induced interfacial stress and peeling stress the solder can withstand there are a few equations that can be utilized. These equations were derived by Wang, Kang Ping et al. (2001) for trilayer electronic assemblies. To determine which variables have the greatest effect on the stress a sensitivity analysis is conducted.

$$\lambda = 2\sqrt{\frac{G_a}{h_a}\left(\frac{1}{E_1' h_1} + \frac{1}{E_2' h_2}\right)} \tag{1}$$

$$E_i' = E_i/\left(1 - \nu_i^2\right) \tag{2}$$

$$\chi = \left[3\frac{E_a'}{h_a}\left(\frac{1}{E_1' h_1^3} + \frac{1}{E_2' h_2^3}\right)\right]^{\frac{1}{4}} \tag{3}$$

$$\beta = \frac{3\left(\frac{1}{E_1' h_1^2} - \frac{1}{E_2' h_2^2}\right)\frac{h_a}{G_a}\lambda}{4(1-\nu_a)\left(\frac{1}{E_1' h_1} + \frac{1}{E_2' h_2}\right)^2 + 6\left(\frac{1}{E_1' h_1^3} + \frac{1}{E_2' h_2^3}\right)\frac{h_a}{G_a}} \tag{4}$$

Traction-free Boundary Condition

$$\tau_{max} = A = \frac{G_a}{h_a \lambda}[(1+\nu_1)\alpha_1 - (1+\nu_2)\alpha_2]\Delta T \quad (5)$$

$$\sigma_{max} = \left(1 - \frac{\lambda^2}{2\chi^2} - \frac{2\chi}{\lambda}\right)\beta A \quad (6)$$

Periodic Boundary Condition

$$\tau_{max} = A = \frac{\left(\frac{l_2}{l_1} - \frac{E_1' h_1^3}{E_1' h_1^3 + E_2' h_2^3}\right)\frac{G_a}{h_a \lambda}[(1+\nu_1)\alpha_1 - (1+\nu_2)\alpha_2]\Delta T}{\frac{l_2}{l_1} - \frac{6G_a}{E_2' h_2^2 h_a \chi^4}\left[\beta\left(\frac{\lambda}{4} + \frac{\chi^4}{\lambda^3}\right) + \frac{1}{(1-\nu_a)h_2} + \frac{\chi^4 h_2}{2\lambda^2}\right]} \quad (7)$$

$$B = \frac{E_a'}{h_2 h_a \chi^2}[(1+\nu_1)\alpha_1 - (1+\nu_2)\alpha_2]\Delta T - \left[\lambda^2\beta + \frac{4\lambda}{(1-\nu_a)h_2}\right]\frac{A}{2\chi^2} \quad (8)$$

$$\sigma_{max} = \beta A + C \quad (9)$$

[3]

Method

There are two different types of samples that will be tested. Both samples have FR-4 as their substrate and silicon carbide as the die. The difference is the size and the interconnect material.

Table 1: Solder Attached Samples' Dimensions

Type 1	Length	Width	Depth
Die	4.40mm	2.91mm	.65mm
FR-4	13.5mm	11.87mm	1.68mm
Solder (Pb36Sn62Ag2)	.38mm	.38mm	.38mm

Table 2: Epoxy Attached Samples' Dimensions

Type 2	Length	Width	Depth
Die	15.24mm	15.24mm	.67mm
FR-4	20.37mm	20.37mm	.78mm
Epoxy (FP4549)	15.24mm	15.24mm	.076mm

Each sample was mounted on top of platform on the die shear machine (shown in Figure 7) parallel with the tooth. The vacuum must be turned on to keep sample in place. The tooth is then lowered closely with the die and programmed on destruct mode (run until part breaks).

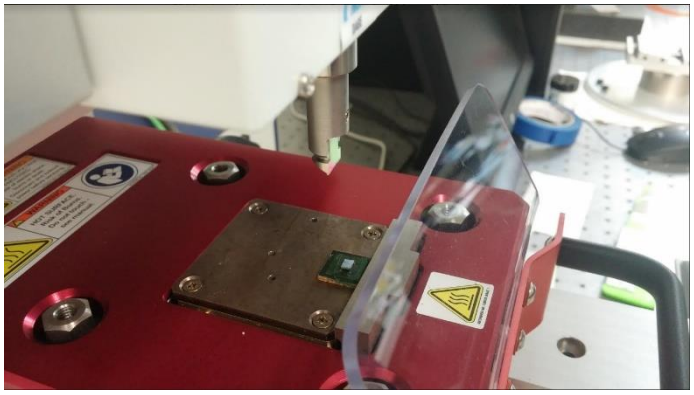

Figure 7: Flip-Chip mounted on Die Shear Machine

Using the die shear machine, shear force is placed in the die as shown in Figure 8.

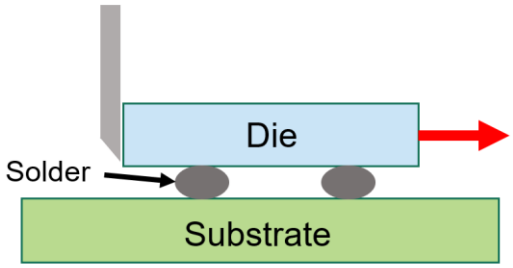

Figure 8: Die Shear force acting on Flip-Chip

Results

For type 1 there were 3 samples:

Table 3: Type 1 Samples Results

Sample	Oven Pretreated (150°C)	Time in oven	Max Force	Max Stress
1	No	0 hours	49.295 N	96.51 MPa
2	Yes	168 hours	6.254 N	12.24 MPa
3	Yes	336 hours	19.91 N	38.98 MPa

The samples' max shear stress decreased after heating in an oven over a period of time. Sample 2 showed weaker strength than sample 3 which wasn't expected. After 2 weeks of heating the sample decreased to 40% of its original shear strength.

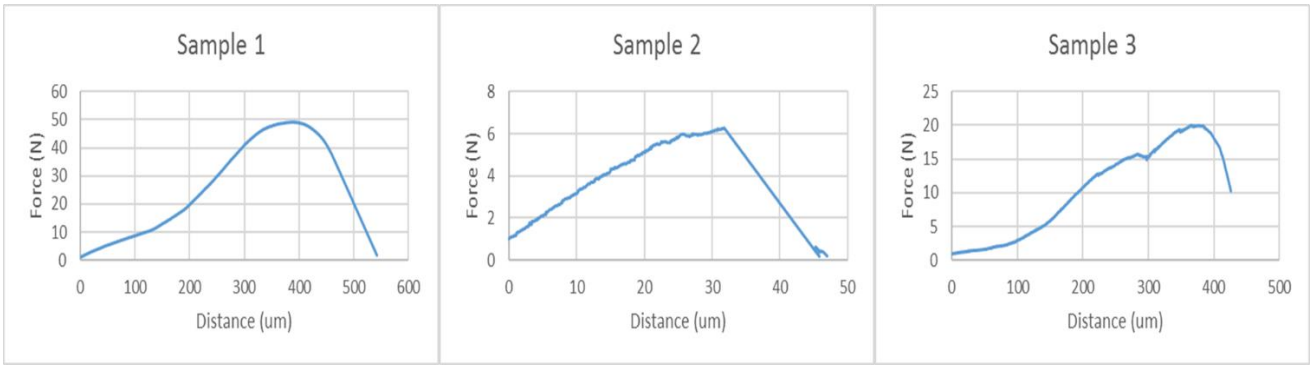

Figure 9: Type 1 sample graphs

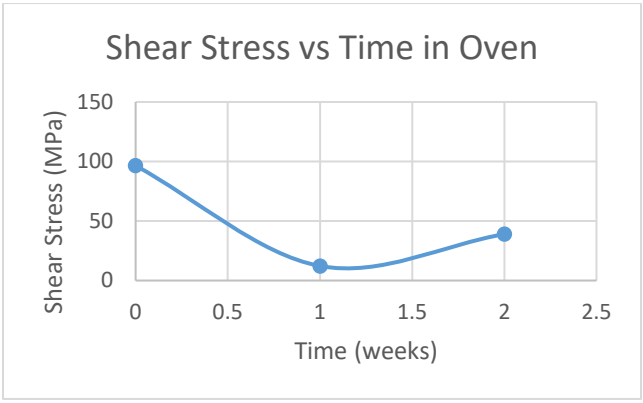

Figure 10: Type 1 Max Shear Stress vs Time in Oven

For type 2 there were 4 samples: None of these samples had any different temperature histories and all were conducted at room temperature.

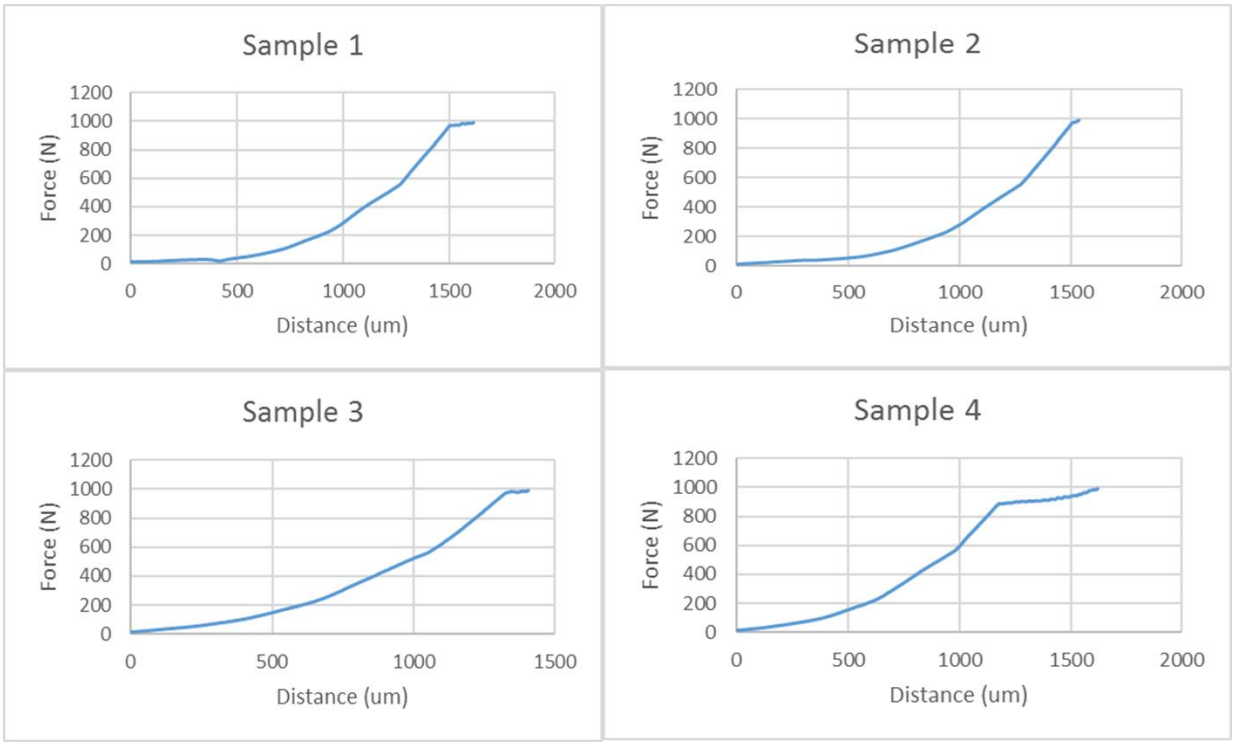

Figure 11: Type 2 sample graphs

The samples did not rupture and do not indicate the beginning of ductility so it is still within the elastic region. All samples maxed out at about 990N (limit of die shear tester).

Sensitivity Analysis

Sensitivity analysis is conducted on Type 2 samples to determine what has a greater effect on interfacial and peeling stress on solder joint. The 2 inputs varied are adhesive gap height and temperature change.

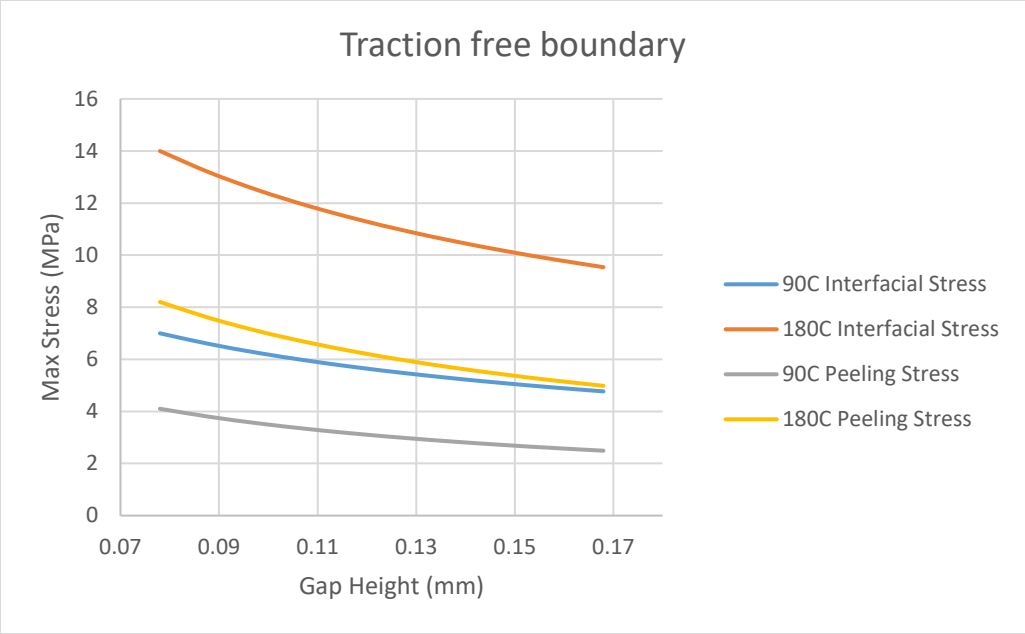

Figure 12: Sensitivity analysis Traction free boundary

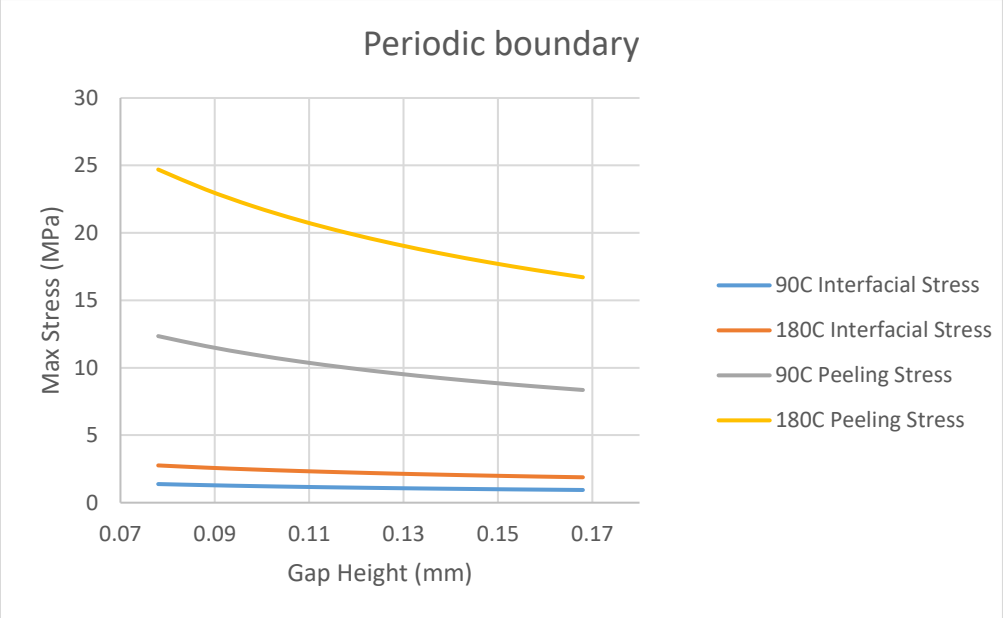

Figure 13: Sensitivity analysis Periodic boundary

For epoxy samples as temperature change doubles max interfacial and peeling stresses doubles in both boundary conditions. In traction free boundary condition, when gap height doubles interfacial stress decreases by 29.29% and peeling stress decreases by 36.23%. In periodic boundary condition, when gap height doubles interfacial stress decreases by 29.29% and peeling stress decreases by 29.74%.

Discussion

Looking at Figure 10 there is an obvious inconsistency with the curve. It would be expected that the as the time in the oven increases the max shear stress should decrease. The main problem with this experiment is the limited number of samples available; there was only 1 sample for each time variable. With a small count there is room for many inconclusive attributes for inconsistencies. During the photolithography process there were some samples that were over-exposed to the light emissions which greatly affect the solder bonding strength to the die. I believe type 1 sample 2 experienced this issue. In Figure 9, samples 1 and 3 moved 10 times further than sample 2 while being sheared indicating that an issue with bonding. The whole shape of the graph is different as well, there is no curve before it peaks. This shows that there was no ductility throughout the process. This distance traveled and graph shape difference alludes to the solder not rupturing but simply disconnecting.

Type 1 Samples 1 & 3 are a better representation of how temperature history affects the max shear stress in the assembly. Sample 3 there were 2 notable curves before the solder ruptured. After examining the sample (shown in Figure 14), 1 side was completely disconnected while the other was ruptured. The first curve probably shows where one side ruptured first and the second curve shows the other side rupturing. I believe the die was not completely parallel with the die shear tooth which unevenly distributed the stress amongst the 2 sides.

Figure 14: Picture of type 1 sample 2

Due to time and heat energy being added to the flip chip, intermetallic diffusion seems to have taken place in the solder. Intermetallic diffusion occurred between the eutectic solder and copper pad on silicon made the thin layer brittle. The constant heating may have created microvoids within the layer creating vacancies that contribute to the crack propagation throughout the layer as observed by Kumar et al.[4]. It is important to first understand how heat energy can degrade the mechanical resilience in the solder joint overtime.

For type 2 samples none of them even failed. The epoxy properties and high total area attributed to this result. What was observed was that there was no ductility observed throughout the test the max shear is unable to be determined by the tester. Epoxy is sometimes used along with solder balls to enhance the bonding strength of the flip chip layers. This addition may introduce other failure modes that need to be evaluated in reliability testing. In the sensitivity analysis temperature change was a much bigger factor compared to adhesive gap height change. However, changing the gap height in the assembly is easier to alter unlike the temperature around the assembly. This information can be beneficial for any manufacturing purposes.

Conclusion

The die shear test indicates a relationship of max shear stress to temperature history in samples. If more samples were available and tested, the relationship between the variables could have been clearer. Type 1 sample 2 data is functionally discarded due to improper bonding between solder and die. Solder cracking and propagation is seemed to be caused by intermetallic diffusion between the layers. This diffusion of copper and solder materials probably strengthened and the microstructure more brittle. Knowing this provides benchmark data for how much stress the solder joints can withstand under different heating environments. In sensitivity analysis the temperature change effected the max stress more than adhesive gap height. In traction free boundary condition, when gap height doubles interfacial stress decreases by 29.29% and peeling stress decreases by 36.23%. In periodic boundary condition, when gap height doubles interfacial stress decreases by 29.29% and peeling stress decreases by 29.74%. When temperature change doubled the max stresses doubled.

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