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Simultaneous Ohmic Contacts to n and p-type Silicon Carbide for Future Electric Vehicles

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Simultaneous Ohmic Contacts to n and p-type Silicon Carbide for Future Electric Vehicles

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By

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Abstract

The paper explores possible metallization schemes to form simultaneous ohmic contacts to n-type and p-type silicon carbide contacts. Silicon carbide has shown promise in revolutionizing the power electronics market due to its increased switching speed, compact design, and higher temperature tolerance when compared to Silicon, the market standard. With the continuing development of silicon carbide technology, higher efficiency in future electric vehicles can be achieved by employing this new technology. This paper discusses theoretical contact formation between metals and semiconductors along with a proposed experiment to create a Ni/Al metallization scheme on both n and p-type contacts simultaneously on a silicon carbide wafer. The original purposed experiment was not able to be carried due to the outbreak of COVID-19. However, the contact formation process and testing procedure are discussed in order to carry out the experiment.

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Introduction

As in most electronic area's silicon has been the predominant semiconductor in power electronics. However, wide bandgap materials in power electronic components are faster, smaller, and more efficient due to their unique properties [3]. Modeling of the replacement of these old Si devices with SiC in vehicles, especially traction inverters, has already shown a significant increase in performance [1]. Employing wide bandgap semiconductors in electric vehicle applications, better energy efficiency, more reliability, and compact design can be achieved by indirectly reducing the need for thermal management systems. SiC and GaN show great potential for revolutionizing the electric vehicle market.

The market for electric vehicles has been on the rise since conception but has reached many limitations in the design aspect. The main limitation is size and weight, which in turn affects the overall efficiency of the vehicle. Many of the components in electric vehicles, such as variable frequency drives, traction inverters, DC boost converters, and battery chargers, are employed with the semiconductor silicon. With the application, the new WBG materials such as silicon carbide in these components needed for the operation of an electric vehicle, the size of these components is dramatically reduced. This will allow for vehicle design to be more aerodynamic, reducing drag. Furthermore, the weight is also reduced by smaller packaging of these components as well as a less of a need for intensive thermal management systems to cool the temperature tolerant components. But wait there is more, Silicon Carbide and Gallium nitride have higher energy conversions resulting in less power dissipation in these components. WBG materials are the next generation semiconductor for electric vehicles by increasing the electrical efficiency in multiple ways. The current limitation of these WBG materials is the overwhelming dominance of Silicon as its fabrication process has become so widespread, and the current state of knowledge on WBG materials is just in its infancy. Through thorough research on WBG materials, the integration of the new generation semiconductor will become widespread and lead multiple industries to technological advancements that couldn't be achieved with silicon.

The efficiency of power generation, distribution, and delivery is an important factor in the electronic power sector. Power is money! Wide bandgap materials implementation can allow for power electronic components to utilize its energy source more efficiently. The two wide bandgap materials silicon carbide and gallium nitride both pose a great replacement for silicon in every sector, but the new technologies have advantages over another, showing greater prowess

for different applications. Both WBG materials have a high electric breakdown field, which allows these devices to operate at higher voltages and have lower on-resistance as well as higher electron mobility and electron saturation velocity that allow for a higher switching frequency compared to Silicon. Gallium nitride has higher electron mobility than Silicon carbide, which makes it better for high-frequency applications such as radio frequency amplifiers. But Silicon carbide has a higher thermal conductivity, which makes it better for power conversion applications. Gallium nitride devices also have poor heat conductivity, which in turn increases the intensive need for thermal management systems. This results in higher production of silicon carbide as this semiconductor is more attractive for the power electronics industry. This pushes the direction of the purposed research to focus on Silicon Carbide [3].

The current fabrication process for silicon carbide CMOS technology is still in development with challenges creating good ohmic contacts to both n-type and p-type materials. The type of contacts created for CMOS transistors is important for the transistor to function with high efficiency and reliability. The contacts can either act as a rectifying contact showing diode characteristics or ohmic contact acting as a resistor. The behavior of contact is largely dependent on the metal used for the semiconductor junction, as well as the doping concentration of the semiconductor. Multiple factors are taken into consideration for optimal contact formation, reliability, longevity, resistivity, time, and cost. Normally, the creation of ohmic contacts for n-type and p-type are created separately to optimize contact type but at the price of fabrication time and cost of the device [16]. To reduce fabrication time and cost, a process can be developed to simultaneously fabricate ohmic contacts to both n and p-type contacts.

The investigation of simultaneous ohmic contact formation to both n and p-type SiC devices lead to the main project goals (1) To understand how to create simultaneous ohmic contacts on SiC wafer and how to determine the type of contact by analyzing the current-voltage (I-V) relationship. (2) From the gathered data, the tested metallization schemes will increase the knowledge of different contact formation processes and how the resistivity and efficiency differ between each tested sample. The benefits of using SiC technology for power electronics over silicon and the knowledge gained from this research prove this project worthy of pursuit. Unfortunately, due to the outbreak of COVID-19, the experimental plan testing different contact formation processes will no longer be able to be performed. However, the process for creating simultaneous ohmic contacts and how to gather results from the proposed sample will be discussed.

Background

Silicon Carbide

A semiconductor is a material that has electrical conductivity between conductors such as metals and insulators like rubber. Silicon carbide is a semiconductor that can be altered, changing its conductive properties. These alterations are caused by adding impurities to the semiconductor called doping. The impurities are call dopants and are classified as electron donors or acceptors. A semiconductor with donor impurities is called n-type and with acceptors impurities p-type. In order to understand how to create ohmic contacts to silicon carbide, semiconductor bands and the metal-semiconductor junction is reviewed.

Semiconductor Bands

A semiconductor has two bands, conduction band and valance band [10]. The conduction band is the band where the electrons of the semiconductor can move freely. The valence band consists of electron holes that act inversely of the conduction band. The Fermi level, which is dependent on the doping of the semiconductor, is the amount of work needed to add an electron to the material [10]. This level resides in between the two bands of the semiconductor represented in the figures below. For n-type, the fermi level resides under to the conduction band because of the addition of electron donors, and for p-type fermi level is above the valence band for the addition of electron acceptors or holes. The vacuum level is the energy of a free electron. The work function is the amount of energy for an electron to reach the vacuum energy level. In figure 1 shows the semiconductor bands for both p and n-type.

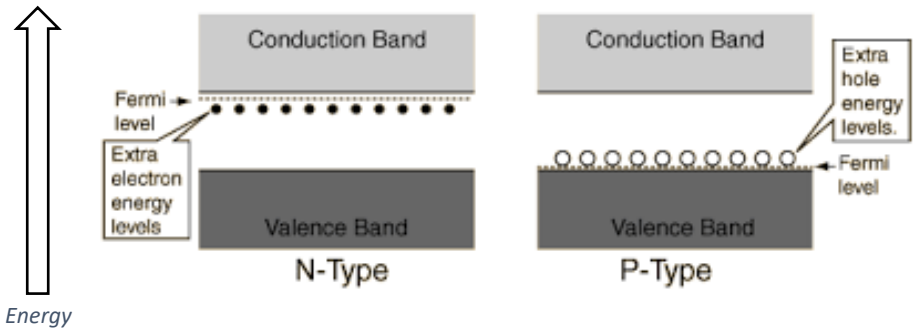

Figure 1. Semiconductor bands [12]

Schottky vs. Ohmic Contacts

When forming a junction between metal and semiconductor, two types of contacts can form ohmic or Schottky. These contacts are characterized by their I-V characteristics shown in figure 2. A Schottky contact requires a voltage bias to induce a current through the contact, which is undesirable as this leads to longer switching time and more power dissipation [10]. Whereas the ohmic contact acts like a resister where the current is directly proportional to voltage, giving the desired linear relationship for contact formation.

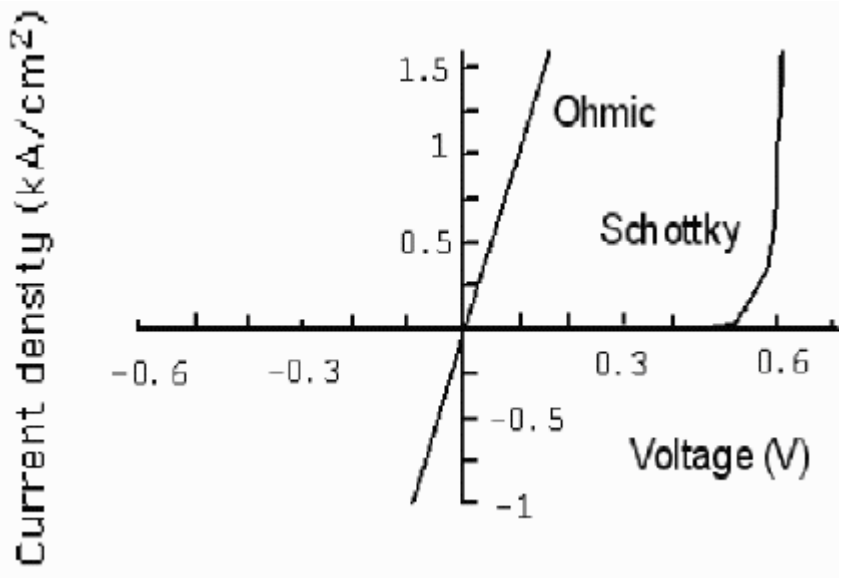

Figure 2. I-V relationship of Ohmic and Schottky contacts [9]

Metal-Semiconductor Junction

Metals bands overlap to allow for electrons to flow freely at any energy level within the material. Metals fermi levels are the same for each material and are important for determining what type of contact is formed. When bonding metal and semiconductor, the fermi levels of both materials are forced to match represented by the top of the metal and the dotted line in figure 3. This results in the semiconductors bands bending either forming an ohmic or Schottky contact. For an ohmic contact, the work function of the metal is less than the work function of the n-type contact and greater than for p-type. For Schottky contact, the work function of the metal is greater than the work function of the p-type semiconductor and less than for p-type. The disparity between the work functions for Schottky contacts is known as the Schottky barrier height.

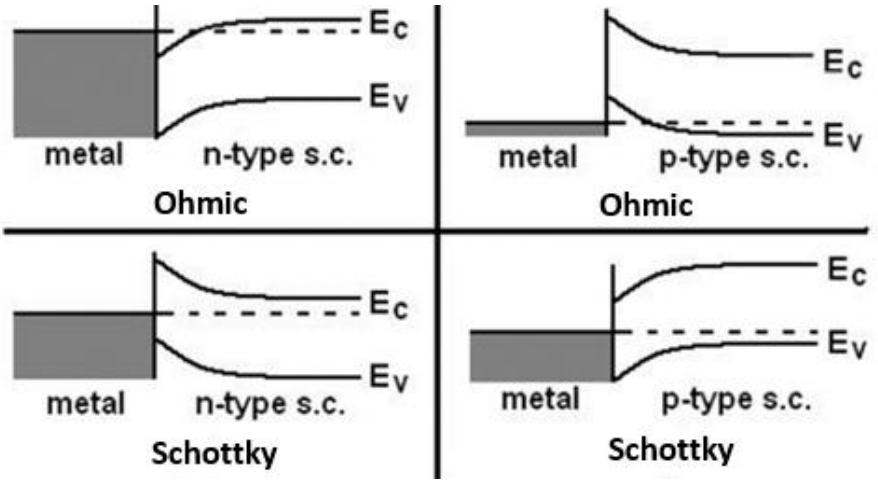

Figure 3. metal-semiconductor junction [11]

The doping of the material and high-temperature annealing can affect the contact type. With higher doping in either direction, p, or n-type, the width of the schlocky barrier decreases. This intern allows for electrons to diffuse through the reduced barrier size called tunneling and to reduce the effects of the schlocky contact and to create an ohmic like contact.

Since silicon carbide is a wide bandgap semiconductor meaning the disparity between the conduction band and valence band is larger in energy levels creating simultaneous ohmic contacts is a challenge as the work function of the p and n-type are to be close to that of the metal bonded. In order to circumvent this problem, the p or n-type contact can be degenerately doped through ion implantation by shooting dopants into the surface of the contact site. This process reduces the diffusion barrier width allowing for tunneling to be the primary means of charge transportations [16]. Ion implantation damages the surface of the substrate but can be partially repaired by high-temperature annealing.

Annealing

Annealing is a process of heating up the wafer at high temperatures post-metal deposition. Annealing can cause a multitude of effects depending on the metals placed on the silicon carbide. Annealing can be used to repair damage caused by ion implantation, which repairs the crystalline structure of silicon carbide. A high temperature anneal also allows for bonding between the substrate and metal stack, reducing voids inside the junctions. These voids can trap electrons or holes, in turn, increasing the Schottky barrier height [10]. Reactions between the metal stack and semiconductor can also form silicides, carbides, and alloys, depending on annealing conditions.

Transmission Line Method

In order to characterize the resistivity of the contact, the transfer length method (TLM) is used to derive it [14]. Resistivity is the desired result for continued studies as the resistivity is

independent of the geometry of the device. The diagram below illustrates how the total resistance is derived from the two adjacent metal contacts shown in figure 4. The resistance of the metal is R_m, the resistance of the semiconductor R_{semi} and the resistance of the Contacts R_C.

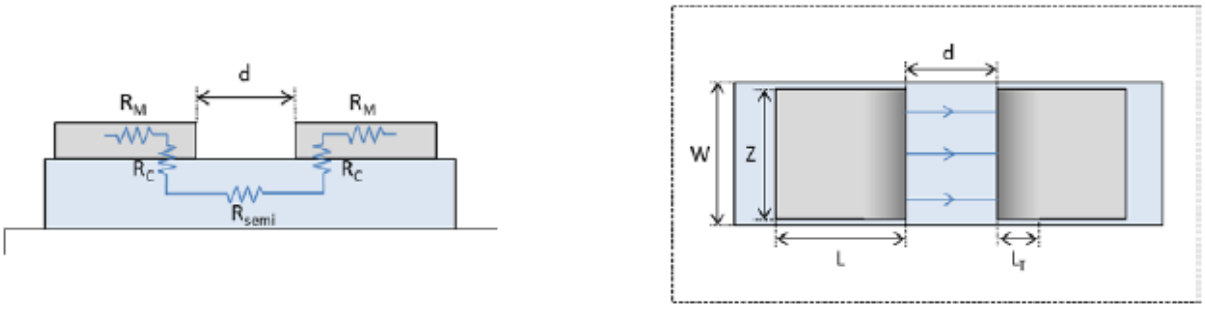

Figure 4. TLM structure [14]

The current will find the path of least resistance, meaning the entire length of the contact is not used and is considered when calculating the resistivity. This length called transfer length L_T and is calculated from the sheet resistance R_{sh} and the resistivity of the semiconductor ρ_c.

$$L_T = \sqrt{\frac{\rho_c}{R_{sh}}}$$

The TLM uses multiple contacts in a row separated by increasing distances d. shown in figure 4. The method finding the total resistances can be found from the following equation.

$$R_T = \frac{R_{sh}}{Z}(d + 2L_T)$$

The resistivity can now be extracted by plotting the R_T vs. d finding the sheet resistance and transfer length. The following equation is used to find the resistivity.

$$\rho_c = L_T R_{sh} Z$$

Experimental

Objectives

Fabrication and characterization of the contact formation were not able to be performed due to the sudden outbreak of COVID-19. Due to this event, the fabrication process will be discussed on how to form metal contacts on a silicon carbide wafer. The contact structure used to gather electrical characterizations called the Transmission line method. The TLM structure using multiple contacts grown on p and n-type regions allows for multiple I-V curves to be extracted to extract the desired resistivity value of the formed contact. Other results would include the characterization of grown contacts on both n and p-type regions determining the type of contact, breakdown voltage, and forward voltage drop.

With the theoretical background and review of outside research relating to contact formation on silicon carbide, an experimental setup worthy of pursuit can be created.

Experimental Setup

The experiment will use silicon carbide wafers with both n and p doped contact regions. The experimental goal is to create simultaneous ohmic contacts to both n and p-type so that the metal deposition process will occur once on all contacts for the tested wafer. The proposed metal stack to be deposited is a nickel aluminum stack Ni/Al. Nickel is chosen for the first deposition layer as previous research shows excellent results for created ohmic contacts and low resistivity to n-type semiconductor contacts [14]. Aluminum was chosen to lower the Schottky barrier by consuming the excess carbon released from the substrate as well as to alloy with the nickel silicide creating a low resistivity and a strong bond between the contact and substrate after annealing [13]. Aluminum also is known to act as a p-type dopant for SiC, creating an ion implantation doped effect on the contacts [15]. Annealing will occur in two steps, unlike traditional annealing, which normally occurs in one step. This was chosen to improve the efficiency of each chemical reaction during the annealing process [13]. The first anneal will occur in post-Ni deposition to form nickel silicide. Once formed, Al is deposited and annealed to efficiently create aluminum carbide and nickel aluminum alloy. The furnace will occur in an atmosphere of arsenic Ar to prohibit oxide formation. The Ni deposited was chosen at 20 nm to form a strong junction between a metal and semiconductor, minimizing reaction from the substrate. The Al deposited is chosen at 120 nm to ensure that the Al/Ni ratio exceeds 80% of the atomic concentration. This has found to further reduce resistivity and the formation of aluminum carbide to reduce the Schottky barrier height [13]. The experimental setup is shown in table 1.

Metallization Stack	***Metal Thickness (nm)***	***Anneal Temperature (C°)***	***Anneal Time (s)***	***Anneal Atmosphere***
Ni/Al	20/120	600+700	60+60	Ar

Table 1. Experimental setup

Sample processing

The sample wafer processes will use the same metallization pattern to both n and p-type contacts using the TLM structure. Before metal is deposited, a photolithography is performed [17]. The steps for creating the proposed metal stack are shown below.

1. First, a photoresist (PR) layer is applied to the surface of the substrate using a spin coater shown in figure 5.

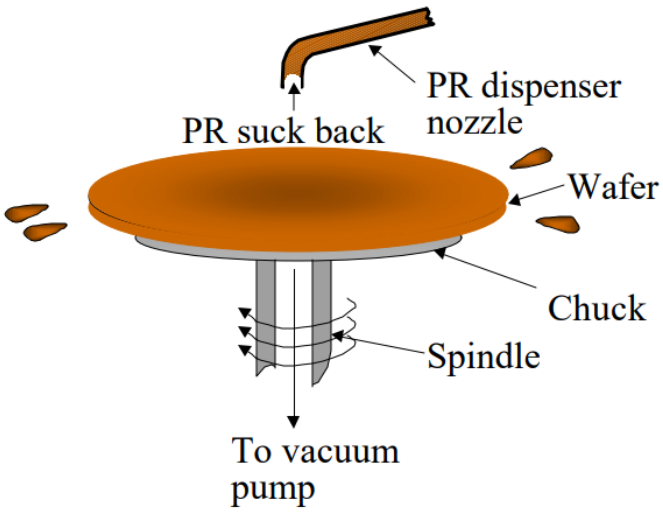

Figure 5. Photolithography step 1 [17]

2. Using a mask to protect the contact sites, a UV light is used to harden the exposed areas shown in figure 6.

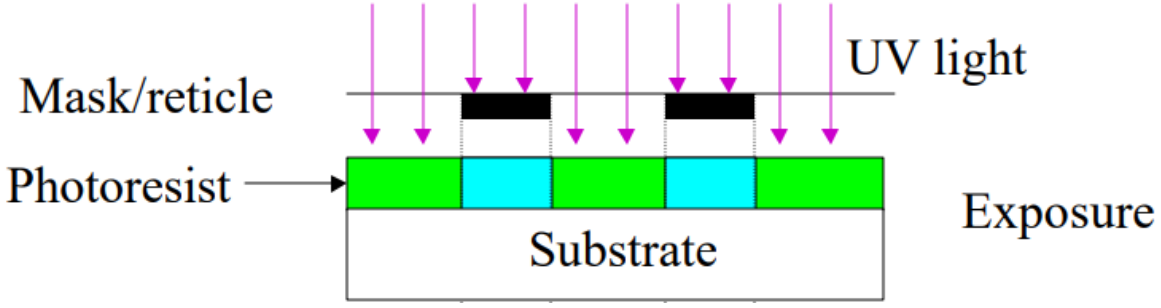

Figure 6. Photolithography step 2 [17]

3. After a soft bake helping the photoresist adhere to the substrate, a developer solution is a spin coated to the surface of the wafer, much like the PR spin coating in step 1. This developer solution removes the PR that was not exposed to UV light from step 2
4. Then the wafer is the hard-baked using a hot plate method shown in figure 7. This further improves the adhesion of the PR layer and preparing the wafer for metallization.

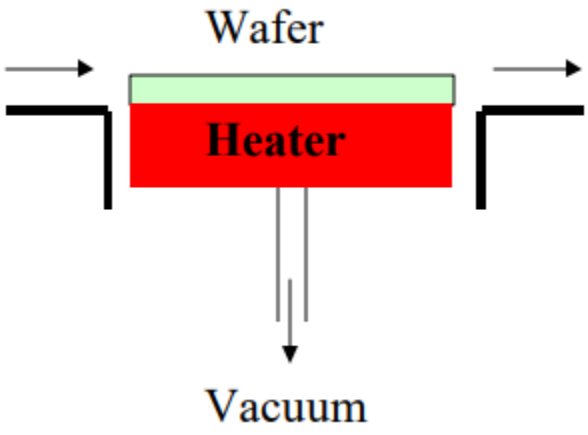

Figure 7. Hot Plate bake method [17]

5. The metal deposition process will be done with a sputtering technique; first Ni is deposited on to the entire surface of the substrate at the proposed thickness
6. The excess metal is then stripped from the substrate using a liftoff technique removing the PR using acetone. The contact areas PR was removed from the photolithography process leaving behind the metal deposited on the desired contact site.
7. A First step annealing process is performed. Annealing introduces high heat to the substrate for a short time. The first anneal at 600 C to form nickel silicide Ni_2Si and carbon C is released from the substrate.
8. This process is then repeated for Al deposition with the second annealing temperature of 700 C to form Al_4C_3 and a nickel aluminum alloy.

Testing Method

The electrical measurements were to be made at the probing station at a University of Arkansas facility, shown in figure 8.

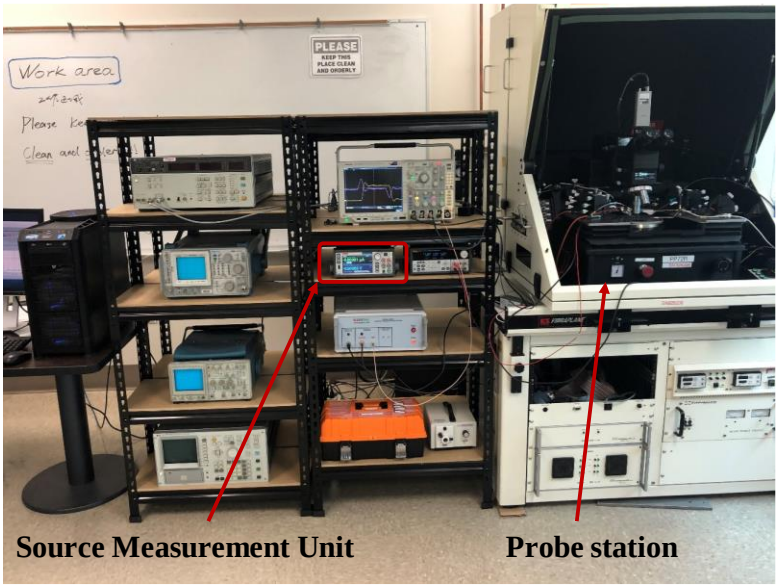

Figure 8. Probing station

Utilizing me source measurement unit, the current is measured while sweeping the voltage giving data for an I-V curve. The electrical schematic showing the source measurement unit and two probe connection is shown in figure 9. Repeating this technique for every contact in the TLM structure, the resistivity can be extracted. The type of contact can also be determined from the resulting I-V curves.

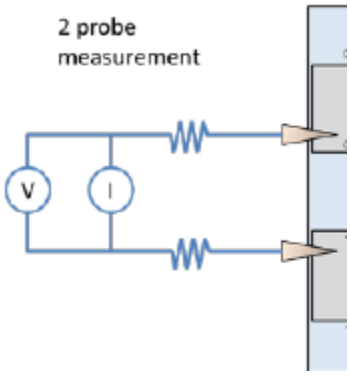

Figure 9. probe schematic [14]

Conclusions

Silicon carbide is on the horizon for revolutionizing the electronics market. As more and more knowledge of these semiconductors becomes readily available, the processes involving the creation of these products employing WBG materials will also grow due to the favorability of these semiconductors compared to silicon. The University of Arkansas provides the capability to perform the experimental plan and allow for future research characterizing many contact formations processes. This research will allow for the SiC technology to grow and become a better candidate to replace silicon in electric vehicle applications. As research continues on these WBG materials, widespread practical implementation will increase the overall efficiency of systems employing these devices not only in electric vehicles but in many other markets, making a greener and more efficient world.

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