Ohmic Contact Metallization for Silicon Carbide in Future Transportation and Aviation Systems

Tanner W. Rice
University of Arkansas, Fayetteville

Ohmic Contact Metallization for Silicon Carbide in Future Transportation and Aviation Systems

A thesis submitted in partial fulfillment
of the requirements for the degree of
Bachelor of Science in Electrical Engineering

by

Tanner Webb Rice

May 2020
University of Arkansas

This Thesis is approved for recommendation to the Honors College

[redacted]

Dr. Zhong Chen
Honors Thesis Advisor

Abstract

This paper analyzes metallization stacks in both n-type and p-type used in Silicon Carbide to create Ohmic Contacts. Silicon Carbide has shown its significance in usage as a semiconductor in high temperatures, and other extreme environments compared to its silicon counterpart. Additionally, silicon carbide exhibits many other favorable attributes such as strong radiation hardness, high power capability, and high-temperature tolerance. These attributes translate into great components for use in aviation and other future transportations by increasing reliability in a sector that already requires high reliability. Applications of this material could prove useful in fields such as aviation, among others. This paper highlights the objectives of metallization, preliminary research, the experimental plan on how to implement and characterize different metal stacks, future research, as well as the significance of proposed research in this up and coming technology. However, due to the unforeseen circumstances of COVID-19, the experimental plan concerning the metallization process and characterization of the metallization was not able to be carried out. Due to this, a layout of how the metallization process and how the results from said process can be extracted and read will be discussed.

Acknowledgments

This paper titled "Ohmic Contact Metallization for Silicon Carbide in Future Transportation and Aviation Systems" submitted by Tanner Webb Rice is carried out under the guidance of Dr. Zhong Chen and his research. The author is grateful for Dr. Zhong Chen for allowing me to do my honors thesis under him. Dr. Chen's professional guidance and encouragement from the start of this proposal was critical to the author's success. The author is also grateful for graduate research assistants, Syam Madhusoodhanan, Abbas Sabbar, and Kevin Chen who helped with training on equipment and pointing the author in the right direction during research.

Table of Contents

Chapter 1: Introduction..1
Chapter 2: Theoretical Background..4
A. Silicon Carbide..4
B. Ohmic and Schottky Contacts..4
C. Semiconductor Bands...6
D. Band Bending...8
E. Metallization..9
F. Annealing...10
Chapter 3: Objectives and Metallization Process...11
A. Objectives..11
B. Metallization Process...11
Chapter 4: Methodology and Experiment Setup..13
A. Methodology..13
B. Experiment Setup...14
Chapter 5: Future Research and Significance of Proposed Research..............................16
A. Future Research...16
B. Significance of Proposed Research..16
Chapter 6: Conclusion...18
References 19

List of Figures

Figure 1. Ohm and Schottky I-V Curve [10] 5
Figure 2. N-type semiconductor bands...7
Figure 3. P-type semiconductor bands...7
Figure 4. Positive and Negative biased p-n junctions [9] 8
Figure 5. Different types of band bending based on p and n types. [14] 9
Figure 6. View of C-TLM layout..13
Figure 7. Cleanroom and Metallization Equipment a) Suss Mircrotec MJB3 contact aligner. b) Specialty Vacuum Tech. PVD-1 E-Beam evaporator. Used with permission by Syam Madhusoodhanan...15

List of Tables

Table 1. Characteristics of Si and SiC [3] 1
Table 2. Ohmic and Schottky Contacts for work functions of metals and semiconductor.............9
Table 3. Experiment Metal Stacks..14

Chapter 1: Introduction

In this day and age, wide bandgap (WBG) semiconductor material (for example, silicon carbide (SiC)) has shown its prowess for many harsh environment applications, with exceptional properties including strong radiation hardness, high power capability, high-temperature tolerance, and a thermal conductivity. Some of these properties are shown in Table 1 below.

	Silicon	Silicon Carbide
Bandgap (eV)	1.12	3.2
Max Operating Temp. (˚C)	600	1580
Thermal Conductivity (W/cm*K)	1.7	3~4

Table 1. Characteristics of Si and SiC [3]

This semiconductor material has demonstrated great potential for use in aviation and future transportation that might require such specifications, causing an increase in reliability in aviation and transportation devices. For example, an application of this material could be seen in starter engines and power converters, which are devices that become incredibly hot when in use. With the integration of this material, devices like starter engines could be integrated in a more efficient manner that allows for a better aerodynamic profile, which in turn allows for the aircraft to be more fuel-efficient. Not only would this be more efficient aerodynamically but it would allow for the utilization of the aircraft's cooling system to redirect its resources to cool another component of the aircraft [8] Researching such materials thus opens new possibilities for advancement in aviation and other transportation technologies.

The types of contacts deposited on these transistors are very important for the transistors to function at these high temperatures. Known as metallization, the type of metal or metals used and annealed will affect whether the contact acts as a wire by displaying ohmic properties, or as a diode by displaying a Schottky contact. For SiC devices, many different metal combinations, also called metal stacks, have been tried for both p-type and n-type material. Examples of metal stacks include variations of Nickel, Aluminum, Titanium, Tungsten, as well as many others placed on the doped substrate. [15]

Since its conception in the 1950s, silicon devices have steadily been improving. Moore's law keeps pushing silicon-based devices to improve and become smaller and smaller; however, the physical size of these transistors can only get so small. Since it is a Wide Band Gap semiconductor, silicon carbide can also reach higher frequencies compared to silicon. Since silicon carbide semiconductors are able to switch at a higher frequency, they can enable lower switching losses which means a higher efficiency compared to its silicon counterparts [6]. Silicon carbide devices can not only achieve the same efficiency per size, as Silicon MOSFETs with only between 43%-54% of an area of a Silicon MOSFET, but also if one wanted to achieve the same power density of a Si MOSFET, it would only cost between 30-40% of the Si MOSFET chip area [4]. This in conjunction with its excellent thermal conductivity, its high radiation tolerance, and wide electrical bandgap makes it an excellent candidate for Aviation and Future Transportation power modules.

By using this semiconductor material for its high heat tolerance and thermal conductivity, one is able to use it for creating less of a need to cool electronics controlling the power conversion for the electrical loads on an aircraft .This means that since these electronics do not have as much as a need for cooling, the cooling systems can be smaller and lighter, and thus makes a more fuel efficient aircraft, as a lighter load in terms of weight leads to more fuel conservative aircraft [5]. It will also allow electronics to be integrated closer to high temperature devices, allowing devices like the electrical starter engine of a jet engine be integrated into the engine itself, leading to aerodynamic efficiencies, thus resulting in fuel efficiencies due to the less amount of drag of an aircraft. The other added benefit is its lower electrical losses for both aviation and electrical charging stations, allowing a lower carbon footprint.

One of the primary components that allows for such an Investigation and examination of the SiC devices will lead to two major project goals: [1] To understand how to properly form metal contacts using different types of metallization stacks by analyzing their characteristics on the electrical level. [2] With this data recorded, we can use it to increase our understanding in how different metallization stacks of SiC devices differ between each other in terms of resistivity and longevity in terms of heat, and how one might be able to optimize these stacks such that they are able to be used at a higher temperature without degradation in ohmic function and low resistivity. My research project will increase understanding of metal usage and how different metal stacks may be utilized in future applications. The significance to future usage of silicon carbide technologies, make this research project worthy of pursuit. However, due to the unforeseen circumstances because of COVID-19, the experimental plan concerning the metallization process and characterization of the metallization was not able to be carried out. Due to this, a layout of how the metallization process and how the results from said process can be extracted and read will be discussed.

Chapter 2: Theoretical Background

A. Silicon Carbide

Semiconductors are a material that can conduct electricity depending on the parameters of the device. For most transistors, an electrical semiconductor relies on whether a voltage or current is applied at the gate or base of the transistor, depending on whether the transistor is a Metal Oxide Field-Effect Transistor (MOSFET) or a Bipolar Junction Transistor (BJT). Current semiconductor devices utilize silicon as the wafer substrate for semiconductor device fabrication. This leads to some challenges when used in harsh environments such as environments with high temperatures and/or high radiation. For devices such as power modules and other electronics that use normal Si substrates, high temperatures and radiation affect both the characteristics and lifetime of the device the silicon is being used for. For applications in aviation, higher radiation tolerance can be useful, since aircraft are introduced to more cosmic radiation in the less dense atmosphere [7]. This in conjunction with high temperature and high radiation tolerance allows for more time of usefulness of the device before it fails. Some characteristics for SiC that make it a benefit over a simple Si substrate include a higher thermal conductivity compared to Si, meaning that SiC is able to transfer heat to another material easier [1]. The temperature range of a Si device also has a lower ceiling than that of a SiC device, meaning that a SiC device can survive a higher temperature compared to its Si cousin. In a study, the highest temperature before failure of a Si module was around 150 degrees Celsius, compared to a SiC device, whose temperature range can be designed for 200 Celsius or higher, depending on if the device is packaged in something that also has a high heat tolerance[3,9].

B. Ohmic and Schottky Contacts

When metallizing a contact for semiconductor, the band gap of the material plays into how the contact will behave electrically. The two types of behavior can be determined by their I-V curves. I-V curves that show more of a rectifying function shown in Figure 1 show properties of a Schottky contact. A Schottky contact acts as a diode, allowing a forward current, but not allowing for a reverse current unless a large reverse current causes it to breakdown. Essentially, a Schottky contact is like a one-way street, only allowing for a current flow in one direction but cannot flow in reverse unless a very high current overcomes the barrier in the reverse direction of the I-V curve. The ohmic contact however, acts as a wire, allowing for current to flow freely either one way or the other. In other words, an Ohmic contact is a two-way street, and can allow the current to go in both directions, unlike the Schottky contact that only allows for current in only one direction. This ohmic contact can be necessary, allowing for using the transistor both used in both directions of currents. This can be shown as such in Figure 1 below.

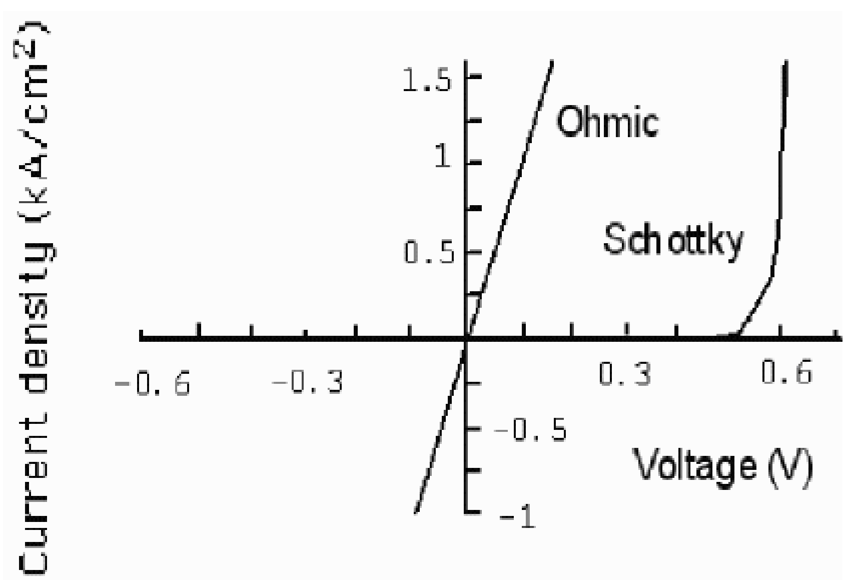

Figure 1. Ohmic and Schottky I-V Curve [10]

C. Semiconductor Bands

Since Silicon Carbide is a semiconductor, it possesses two separates bands, a conduction band and a valence band. The conduction band E_c is the band where electrons can move freely. The valence band, E_v acts in the opposite way of the conduction band, using empty states within the valence band, also known as holes, in order to be conducted [9]. E_f is the Fermi level. Based on whether it is the position of it, it determines whether the semiconductor has an abundance of free electron or free holes. N-type semiconductors' Fermi level will congregate towards the conduction band indicating a plentitude of free electrons, while the P-type semiconductor will do the opposite and move towards the valence band showing the abundance of holes [9]. Also, in Figure 2 and Figure 3, is the vacuum level, E_0 , and the work function, ϕ_s . The vacuum level, also known as E_0 , is the energy of a free electron outside the material. The work function is known as ϕ_s , and is the amount of energy for necessary for an electron to go to vacuum. Depending on the doping of the semiconductor, the Fermi band will move either up as shown in a n-type semiconductor, or down, as shown in a p-type semiconductor. Doing this also changes the work function of the semiconductor. Pairing non-identical work function of materials like a p type and n type semi-conductor causes each other's bands to bend, creating slope between the n type and p type bands as shown in Figure 4. Also shown in Figure 4, when the current is going forward biased, or flowing from the P-type semiconductor to the N-type semiconductor, it decreases the size of the barrier between them and allows for current to pass through. However, when the current is negatively biased, or when the current is flowing from the n type semiconductor to the p type semiconductor, it increases the size of the barrier between them and prevents current from passing through due to the increase in the barrier height between them.

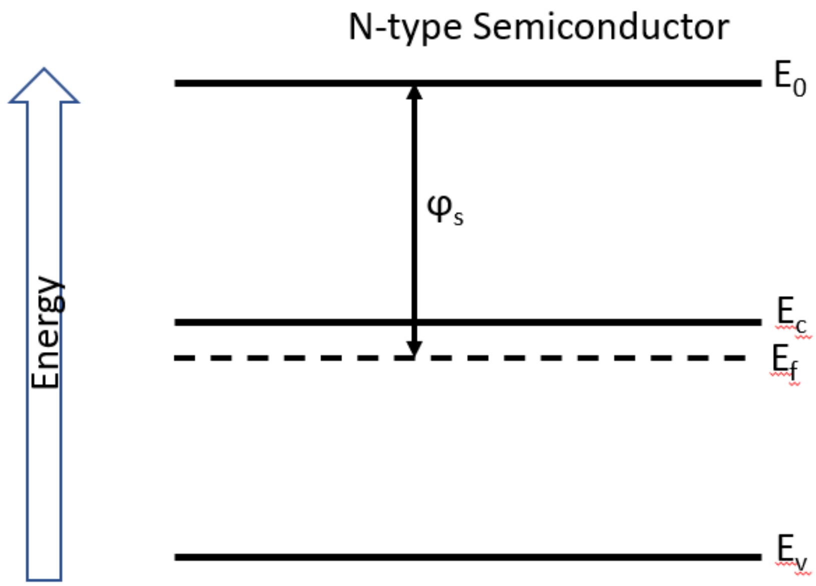

Figure 2. N-type semiconductor bands

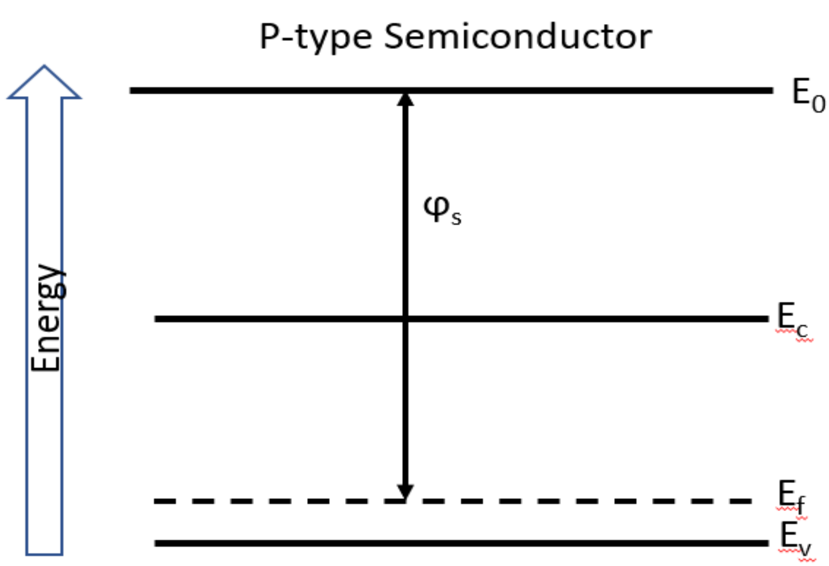

Figure 3. P-type semiconductor bands

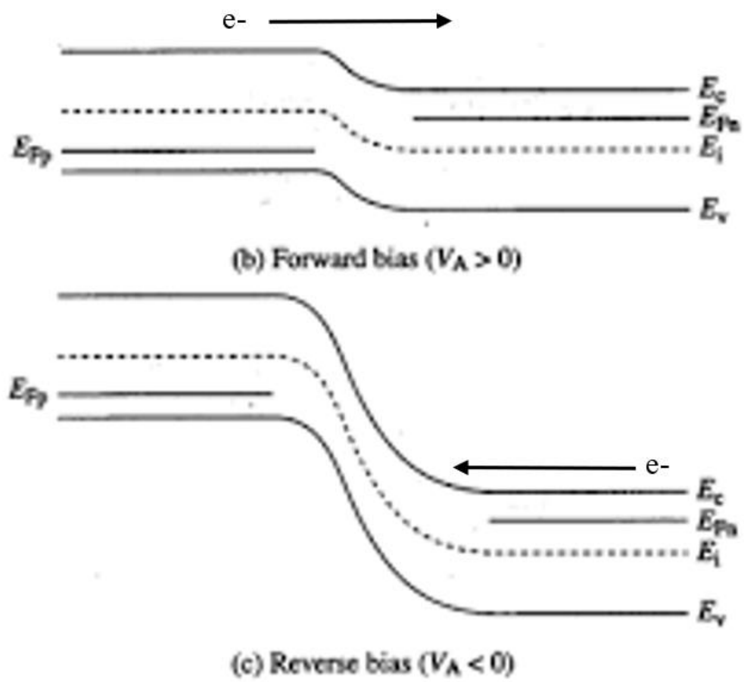

Figure 4. Positive and Negative biased p-n junctions [9]

D. Band Bending

Band bending is how Schottky and Ohmic contacts become formed. When metal and a semiconductor are bonded, the work function of the metal and fermi level of semiconductor will align with each other. This results in what is called "band bending" and determines whether a Schottky or Ohmic contact is formed based on the work functions of both the metal and the semiconductor. To form an ohmic contact, the work function of the metal will be less than the work function of the n-type semiconductor as shown in Figure 4a, but greater than the work function of the semiconductor in a p type as shown in Figure 4b. In order to achieve a Schottky contact, the work function of the metal will be greater than the work function of the n-type semiconductor as shown in Figure 4c, but less than the work function of the semiconductor in a p type as shown in Figure 4d. These pairings on each type of semiconductors contacts are formed can be summarized in Table 2.

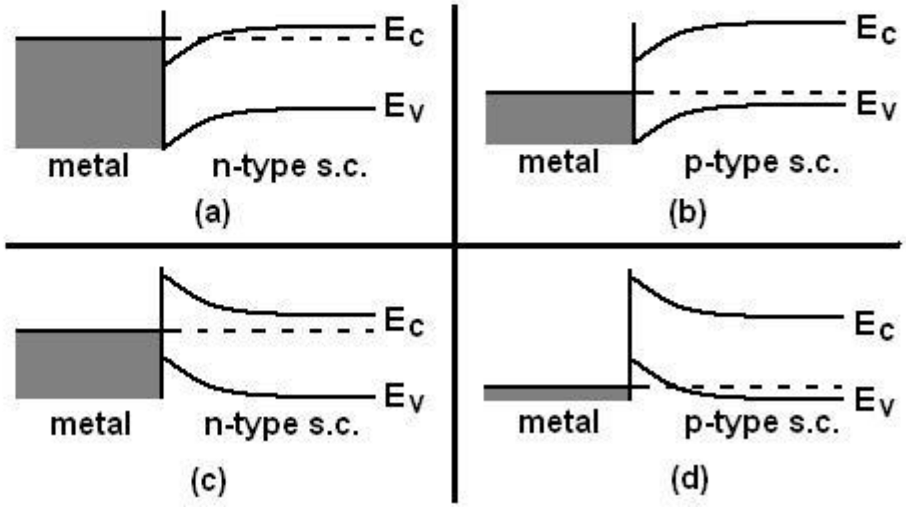

Figure 5. Different types of band bending based on p and n types. [14]

	Ohmic Contact	Schottky Contact
N-type semiconductor	ϕsemiconductor< ϕmetal	ϕsemiconductor> ϕmetal
P-type semiconductor	ϕsemiconductor> ϕmetal	ϕsemiconductor< ϕmetal

Table 2. Ohmic and Schottky Contacts for work functions of metals and semiconductors

E. Metallization

Metallization is the formation of a layer or layers of metal deposited onto the silicon carbide substrate, then heated up rapidly for a short period of time also known as annealing. This annealing process allows for the metals applied via sputtering, which is the act of depositing metals from a metal plate onto the silicon carbide substrate, to interact with the silicon carbide. The annealing of the metal allows for both the metals and the silicon carbide to form new bonds and alloys, allowing for a smoother interface between the semiconductor and metals deposited. As aforementioned in the previous subject of band bending, the Ohmic or Schottky characteristics depend on the work functions of the metal, as well as whether the silicon carbide is p-type or n-type. Depending on what metal stack is used in the interaction of the metallization, the band gap between the metal and the substrate is much lower and allows for more ohmic characteristics. Metals typically used in contacts consist of metals such as Nickel, Titanium, Aluminum, Tungsten as well as Tantalum. These metals are used due to their ability to alloy with either the Silicon or Carbon in the semiconductor and give it more favorable properties like reducing the barrier height between the silicon carbide and the metal [15].

F. Annealing

Annealing is the process of heating up the metallization stack in a low atmosphere environment. These high temperatures allow for the alloying between the semiconductor and the metal. Additionally, the high temperatures work to reduce the number of voids between the semiconductor and metal stack, as well as semiconductor “traps” or defects that electrons or holes can become trapped. Because of this, the unintentional barrier height is reduced [9][11]. This reduction of the barrier height is extremely beneficial in the creation of the ohmic contact. Creation of this ohmic contact is extremely important, as it not only allows for current to flow in either direction, but it also reduces the amount of power dissipated since in an ohmic contact there is no barrier or a reduced barrier height to overcome. With this reduction in power dissipated, less heat is created from use of the device, and the power efficiency of the device will go up.

Chapter 3: Objectives and Metallization Process

A. Objectives

Due to the abruptness of the University closing due to COVID-19, fabrication and characterization of the metal stack was unable to be performed. Because of this a fabrication process will be discussed to explain how to place and anneal different types of metallization stacks. Further, an analysis will be discussed on whether the contacts are ohmic or not, as well as the specific contact resistance. The overall purpose of this research is to learn the electrical characterizations such as I-V charts and through the circular transmission line method (C-TLM) on Silicon Carbide. Device data would have included data such as their leakage current, forward voltage drop, breakdown voltage, and the contact resistance.

With this experimentation, a better understanding of the properties of the different silicon carbide devices' metallizations can be achieved and how it can be better utilized in aviation and other forms of power modules compared to a silicon device.

B. Metallization Process

In order to metallize silicon carbide, a process had to be developed. Due to optimizing both n-type and p-type silicon carbide, two separate metallizations must be composed in order to achieve optimal characteristics. However, the process is the same and goes in such order:

1. Apply photoresist through use of a spin coater.
2. Apply a mask and use Ultraviolet light to harden the photoresist where we do not want the metal to stick to the Silicon Carbide substrate by using a stepper. For this experiment this will require use from the Suss Mircrotec MJB3 contact aligner.
3. After the photoresist has semi-hardened, the use of a developer solution is utilized to remove the photoresist that was not hardened by the Ultraviolet light and expose areas of

the Silicon Carbide substrate that are to be metallized.

4. After the developer process is done, a "hard bake" is done to harden the remaining photoresist to prepare it for metallization.
5. Metal deposition is done by sputtering. This is done by using energized particles to eject the metal from the desired metal target. This metal or metals will differ on the n-type and p-type substrate. For n-type, nickel has shown promise in ohmic characteristics and low resistivity, while a nickel-titanium-aluminum has developed low resistivity ohmic contacts for p-type substrates. Sputtering will use the Specialty Vacuum Tech. PVD-1 E-Beam evaporator system to deposit metal.
6. After the metal has been sputtered on, the unwanted metal is taken off through the liftoff process by using acetone or another liftoff chemical to remove the acetone from underneath the metal and lifting it from the substrate. This leaves the metal meant to be annealed on since there was no photoresist layer separating the metal from the Silicon Carbide substrate.
7. Finally annealing can take place. This is when the substrate is introduced to a high temperature for a very short time. This allows the metals from the metallization stack to diffuse and interact with the silicon carbide, allowing for lower resistivity.

Chapter 4: Methodology and Experiment Setup

A. Methodology

In order to determine the contact resistivity, the C-TLM method will be used. This process is where rings with different widths of semiconductor are exposed through the metallization process as shown below in Figure 6.

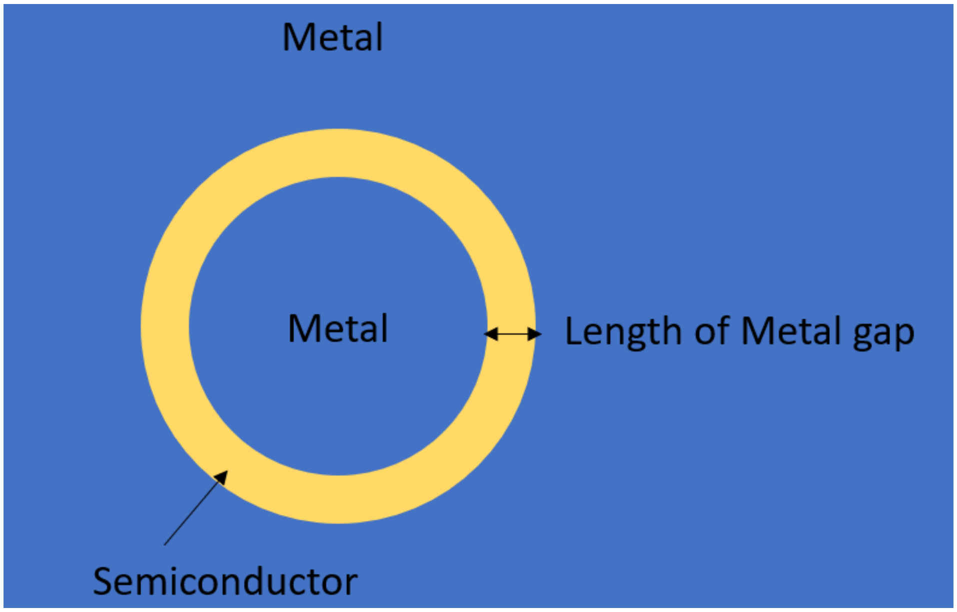

Figure 6. View of C-TLM layout

After metallization, a probe is placed on the inside of the metal and another probe is placed on the outside portion of the metal. After the probes are placed, the resistance between the probes can be measured. There are three types of resistances that are between the probe. The resistance of the metal R_M, the resistance of the semiconductor R_{SC}, and the resistances of the contacts R_C. The equation for the total resistance, R_T is shown below.

$$R_T = 2*R_M+2*R_C+R_{SC}$$

Since the resistance of the semiconductor is known through its doping profile and the resistance of the metal would also be known, then the equation above can be manipulated to find the contact resistivity as shown below.

$$(R_T - R_{SC} - 2*R_M)/2 = R_C$$

As differing size rings of semiconductor exposed are tested a graph can be plotted that allows the contact resistivity to be found.

B. Experiment Setup

For the experiment, use of a both a n-type 4-H SiC substrate with a .5µm n-type doped epilayer with a doping concentration of 1E20/cm^3 and a p type 4-H SiC substrate with a .5µm p-type doped epilayer with a doping concentration of 1E20/cm^3 would be used. For the n type and p type wafers, the following metallizations and conditions would be used in Table 1 below.

Type of SiC	***Metallization Stack***	***Metal Thickness (nm)***	***Anneal Temperature (˚C)***	***Anneal Time (s)***	***Anneal Atmosphere***
N-Type	Ni	100	1050	300	Ar
P-Type	Ni/Ti/Al	100/50/80	850	300	Ar

Table 3. Experiment Metal Stacks

The reason for only using nickel as the ohmic contact for the n-type contact is that it has been excellent in terms of resistivity based on previous research into ohmic contacts, generating contact resistivity as low as 0.49E-5 ohms per square centimeter [15]. Like the choice for the n-type contact, the Ni/Ti/Al stack for p-type SiC has also been well researched. Studies show that this stack when compared with different stack thickness in nanometers of 20/30/80, 60/30/80, and 80/30/80, the contact resistance decreases as the thickness of the nickel increases [12]. Another revision to the previous study is the thickness of titanium. The theory is that Ti_3SiC_2 forms a stable molecule, as well as a narrow gap semiconductor that has an electron affinity close to SiC, allowing for a lower barrier height [13]. This experiment setup will use cleanroom and metallization equipment such as the Suss Mircrotec MJB3 contact aligner and the Specialty Vacuum Tech. PVD-1 E-Beam evaporator shown in Figure 7.

Figure 7. Cleanroom and Metallization Equipment a) Suss Mircrotec MJB3 contact aligner. b) Specialty Vacuum Tech. PVD-1 E-Beam evaporator. Used with permission by Syam Madhusoodhanan.

Chapter 5: Future Research and Significance of Proposed Research

A. *Future Research*

A multitude of SiC device-based metallization stacks can be acquired and tested for the purpose of analysis at high temperatures, with the highest temperature being up to 400 degrees Celsius. The method of testing will be developed in order to test the different types of failures while at high temperatures and to analyze the lifetime and reliability of these metallization stacks. These types of failures include thermally aging the device and seeing how the ohmic contact behaves reliably over time at higher temperatures.

The steps taken for the thermal analysis will be the observation and recording of the locations where the device fails at high temperature, including an analysis of how quickly the ohmic resistance degrades over a high temperature aging process through characterizations of the C-TLM structures, as well as through I-V characteristics of the samples. These tests include heating up the SiC wafer at a multitude of different temperatures in an oven that still allows for probing of the contacts, and using those measurements to see how the contacts resistance change with temperature, as well as seeing how long the contacts reliably maintains its ohmic characteristics. The main goal is finding the design in which one is able to be the most electrically efficient through least specific contact resistance, reliable over long periods of times, create an efficient way for developing and processing samples, and to find space-saving avenues for aviation and transportation, as every bit of space saved can be more cost-efficient to the entire design.

B. *Significance of Proposed Research*

There is an extremely large market for power devices that have high thermal tolerance, as well as the ability to survive other types of harsh environments such as environments with above-average cosmic radiation. The size of the device is also a concern; there has been a rapid increase in demand in space, aviation, and new modes of transportation requiring smaller and smaller power components that can handle a multitude of environments. Silicon-based devices are no long as effective as wanted in these areas due to its max operation temperature of around 150 degrees Celsius and can only operate for high temperature applications if it is cooled by an external thermal system, thus not only increasing the size of the entire system, but also decreasing not the efficiency of the power module.

The development of these high temperature silicon carbide metallization stacks allows for the use of a wide bandgap energy, which increases the effective range of operation of the devices, meaning that it also increases the efficiency and temperature robustness of this technology. Combined with the fact that it has a significant longevity at high temperatures compared to regular Silicon, and what is shown is the amazing viability for aviation power module technology, as well as the power module technology of electric vehicles. Both sectors require reliability and toughness that a Silicon Carbide provides. With the use of the thermal benefits, these power module solutions can reach much higher performances than ordinary Silicon-based technologies used today in terms of thermal and electrical efficiency, size, and reliability.

Chapter 6: Conclusions

There is no doubt that Silicon Carbide has captured interest in both the aviation and power module industries. The next steps in researching these devices are to find the different characterizations that make these Wide Band Gap semiconductors so great compared to a silicon semiconductor. With the utilization of the University of Arkansas' research facilities, many conclusions can be made about different types of metallization stack, such as I-V characteristics, ohmic characteristics, and how resistivity of the metal stack changes due to thermal aging. With its current known characteristics of the reduction of size while still maintaining a comparable efficiency to silicon, hardness against radiation dealt at high altitudes, high-temperature tolerance, as well as requiring less cooling due to its great thermal dissipation, it is easy to see why many companies believe it might be useful in the next generation of electronics in these industries.

References

1. P. Vaculik, "The properties of SiC in comparison with Si semiconductor devices," *2013 International Conference on Applied Electronics*, Pilsen, 2013, pp. 1-4.

2. B. Hu *et al*., "Failure and Reliability Analysis of a SiC Power Module Based on Stress Comparison to a Si Device," in *IEEE Transactions on Device and Materials Reliability*, vol. 17, no. 4, pp. 727-737, Dec. 2017. doi: 10.1109/TDMR.2017.2766692

3. Guo, Xiaorui et al. "Silicon Carbide Converters and MEMS Devices for High-temperature Power Electronics: A Critical Review." *Micromachines* vol. 10,6 406. 19 Jun. 2019, doi:10.3390/mi10060406

4. J. Biela, M. Schweizer, S. Waffler and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2872-2882, July 2011. doi: 10.1109/TIE.2010.2072896

5. R. A. Mastromauro, M. C. Poliseno, S. Pugliese, F. Cupertino and S. Stasi, "SiC MOSFET Dual Active Bridge converter for harsh environment applications in a more-electric-aircraft," *2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles(ESARS)*,Aachen,2015,pp.1-6. doi:10.1109/ESARS.2015.7101427

6. S. Mao, J. Popovic and J. A. Ferreira, "300W 175°C Half Bridge Power Building Block with High Temperature SiC MOSFETs for Harsh Environment Applications," *2018 1st Workshop on Wide Bandgap Power Devices and Applications in Asia (WiPDA Asia)*, Xi'an, China, 2018, pp. 1-5. doi: 10.1109/WiPDAAsia.2018.8734567

7. R. A. Prado and C. N. L. Gajo, "Power semiconductor failures due to cosmic rays," *2017 Brazilian Power Electronics Conference (COBEP)*, Juiz de Fora, 2017, pp. 1-6. doi: 10.1109/COBEP.2017.8257437

8. R. A. Brewer, "High temperature electronics for demanding aircraft applications," *2018 International Applied Computational Electromagnetics Society Symposium (ACES)*, Denver, CO, 2018, pp. 1-2. doi: 10.23919/ROPACES.2018.8364108

9. Pierret, Robert F. *Semiconductor Device Fundamentals*. Addison-Wesley, 1996.

10. "The Metal-Semiconductor Junction.Schottky Diode. OHMIC CONTACTS." *Schottky Diode*, 2002, in.ncu.edu.tw/ncume_ee/SchottkyDiode.htm.

11. Zeghbroeck, Bart Van. "Chapter 3: Metal-Semicond. Junctions." *Metal-Semiconductor Contacts*, 2006, ecee.colorado.edu/~bart/book/book/chapter3/ch3_5.htm.

12. X. Zhang et al., "Study on simultaneous formation of ohmic contacts on p- and n- type 4H-SiC using Ni/Ti/Al ternary system," 2014 12th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Guilin, 2014, pp. 1-3.

13. Johnson, Brian & Capano, Michael. (2004). Mechanism of ohmic behavior of Al/Ti contacts to p-type 4H-SiC after annealing. Journal of Applied Physics. 95. 5616-5620. 10.1063/1.1707215

14. Puls, Conor. *Diagram of Band-Bending Interfaces between Two Different Metals and Two Different Semiconductors*. Dec. 2007, upload.wikimedia.org/wikipedia/en/b/bb/Diagram_of_band-bending_interfaces_between_two_different_metals_and_two_different_semiconductors.jpg.

15. Wang, Z., Liu, W. & Wang, C. Recent Progress in Ohmic Contacts to Silicon Carbide for High-Temperature Applications. *Journal of Elec Materi* **45,** 267–284 (2016). https://doi.org/10.1007/s11664-015-4107-8