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Design of a Bandgap Voltage Reference

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Abstract

This thesis details the design process of a bandgap voltage reference (BGR) integrated circuit in a 180 nm CMOS process. A BGR provides a constant DC voltage across a range of operating temperatures and supply voltages. By its nature, the circuit is intended as a reference, not to provide current, so the output would be connected to a very high impedance, such as the gate of a transistor. At 27°C, this design provides a 955 mV reference voltage given a nominal VDD of 3 V. From 20°C to 175°C, the output voltage has a variance of 7.2 mV (approximately 0.8%) at the nominal supply voltage. Also, when the supply voltage changes from 2 V to 3.6 V, the output voltage changes by 10.9 mV (approximately 1.1%). CTAT (complimentary to absolute temperature) and PTAT (proportional to absolute temperature) devices placed in series provide stability over temperature variation, and a differential amplifier provides feedback, stabilizing the output over changes in VDD.

Acknowledgements

First, I would like to thank Dr. Alan Mantooth for giving me the opportunity to work in his IC Design group this past year. I would also like to thank him for his advice as my mentor during my undergraduate research. Working in the lab has been an extremely rewarding and valuable experience which has benefited me greatly and will continue to do so in my future academic and professional career. Next, I would like to thank the graduate students working in the IC Design group for their help with my design process. Their knowledge and support was instrumental in my work. Finally, I would like to thank my family, who have supported me in many ways my entire life. I would not be where I am without their love and encouragement, and I am extremely grateful.

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Introduction

Bandgap voltage references are used for many applications where a known, constant voltage is needed for proper operation. This is particularly important in systems that are exposed to a wide range of environmental conditions, or where the supply voltage is unstable. For example, a battery monitor might use a comparator, which compares the battery voltage to that of a fixed reference voltage (V_{ref}). If this V_{ref} changes, the monitor would yield an inaccurate measurement of the battery level. For this application, the BGR was intended to provide a reference for a low-dropout regulator (LDO). It was less important to design towards a specific value for V_{ref} because voltage dividers can be used to scale the feedback voltage down to be compared against the reference voltage. Therefore, priority was given to reducing the variation of V_{ref} across changes in temperature.

This thesis is divided into two sections. The first section outlines some of the theory behind designing a bandgap reference, as well as some useful equations for choosing the initial values of the components. The second section discusses the design process of the circuit, including the bias circuit and the amplifier. It also details the layout process and final simulations performed after parasitic components are extracted.

Theory and Calculations

To generate a stable reference voltage, this design utilizes PTAT and CTAT devices. PTAT stands for "proportional to absolute temperature," and CTAT stands for "complimentary to absolute temperature." As temperature rises, there will be an increase in voltage drop across PTAT devices and a decrease in voltage drop across CTAT devices [1]. By placing these two types of components in series and adjusting their parameters (width and length for transistors, resistance for resistors), the changes in voltage drop across CTAT and PTAT devices can cancel each other out, resulting in a near constant voltage with respect to temperature.

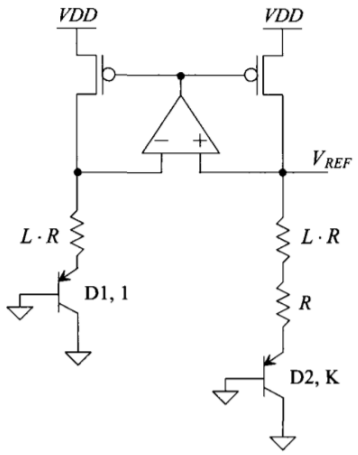

Figure 1: Basic Topology of BGR [1]

In Fig. 1, the two branches in the circuit are connected to the source through two matched PMOS devices, which are gate connected to force equal current through both branches. Each branch contains resistors and parasitic diodes, which are, respectively, PTAT and CTAT. Fig. 1 shows D1 and D2 as parasitic pnp bipolar junction transistors, but in this design, diode connected NMOS transistors are used in their place. The output branch has a higher resistance than the other branch, so by placing a differential amplifier with its inputs tied to each branch and its output tied to the gates of the PMOS devices at the top, a negative feedback loop is created, stabilizing the output voltage with respect to changes in the supply voltage. From Fig. 1, it can be seen that:

$$I = \frac{V_{ref} - V_{GS,2}}{R(1+L)} = \frac{V_{ref} - V_{GS,1}}{R} \quad (1)$$

$$\frac{1}{2}k'_n \frac{W_1}{L}\left(V_{GS,1} - V_t\right)^2 = \frac{1}{2}k'_n \frac{W_2}{L}\left(V_{GS,2} - V_t\right)^2 \quad (2)$$

These equations provide a relationship between the widths of the two transistors at the bottom of the circuit, while the lengths are kept equal. For stability, the temperature coefficients of the resistors and transistor must be matched. From the data sheet for the process used, the transistors have a threshold voltage temperature coefficient $\left(\frac{\partial V_t}{\partial T}\right)$ of approximately -1 mV/K for a width and length of 10 µm [2]. Through simulation, the resistor was found to have a temperature coefficient $\left(\frac{\partial V_{res}}{\partial T}\right)$ of about 1.1 mV/K with a resistance of 250 kΩ. Now, while $\frac{\partial V_t}{\partial T}$ stays mostly constant despite changes in the width of the transistor, $\frac{\partial V_{res}}{\partial T}$ changes non-linearly with respect to the resistance of the component. This makes it very difficult to equate the temperature coefficients and solve for the values of the components. So, a linear approximation for the change of $\frac{\partial V_{res}}{\partial T}$ was made, which equals about -1 µV/K*kΩ. That is, $\frac{\partial V_{res}}{\partial T}$ decreases by about 1 µV/K for every increase in resistance of 1 kΩ. This means, theoretically, to match $\frac{\partial V_t}{\partial T}$ and $\frac{\partial V_{res}}{\partial T}$, the resistors on the output branch should have a total value of 350 kΩ, or R in Fig. 1 should equal 175 kΩ (setting L equal to 1). Though there is no given V_{ref}, there must be some target value to start designing, so 1 V was chosen, as this circuit is designed for a VDD of 3 V. 1 µA was chosen as a very low branch current, and solving Equations (1) and (2) with a V_t = 0.7 V gives:

$$V_{GS,2} = 0.65\ V, V_{GS,1} = 0.825\ V \quad (3), (4)$$

$$W_2 = 6.25W_1 \quad (5)$$

Design of Supporting Circuits

After the initial specifications for the BGR are identified, an amplifier is constructed for the feedback loop.

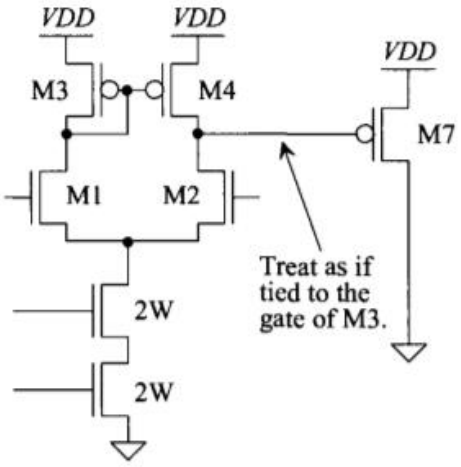

Figure 2: Differential Amplifier Schematic [1]

Fig. 2 was the basis for the amplifier used in this design. However, this design uses only one bias transistor at the bottom of the differential pair, and one at the bottom of the PMOS common source amplifier as seen in Fig. 3 below, the final schematic used in the BGR. A compensation capacitor was also added between the gate and drain of M2 to improve the phase margin.

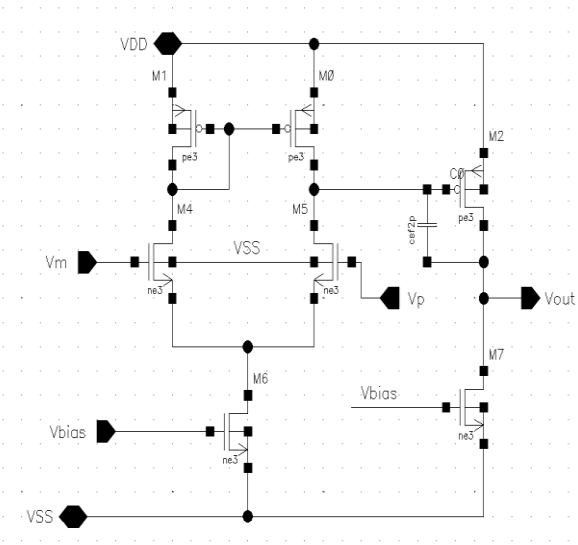

Figure 3: Differential Pair tied to CS Amplifier

In the amplifier, the widths of M4, M5, and M7 are all matched to allow equal current to flow through each branch. M6 is twice as wide as M4 and M5 for the same reason. The gain increase from increasing the size of the NMOS past what is required to sink the desired current is negligible. The gain is also maximized when the widths of M1, M0, and M2 are about five times that of the NMOS, but the gain is negligibly increased when all widths are increased equally beyond this. The amplifier has an open loop gain of 47 dB and a phase margin of 90° as seen in Fig. 9 in the Results section. The bias circuit was constructed to provide NMOS gate voltages for the bias transistors in the amplifier which force equal current through each branch. The bias circuit is a simple beta multiplier current mirror biased by a 100 kΩ resistor. The device also has a start-up circuit as seen in Fig. 4.

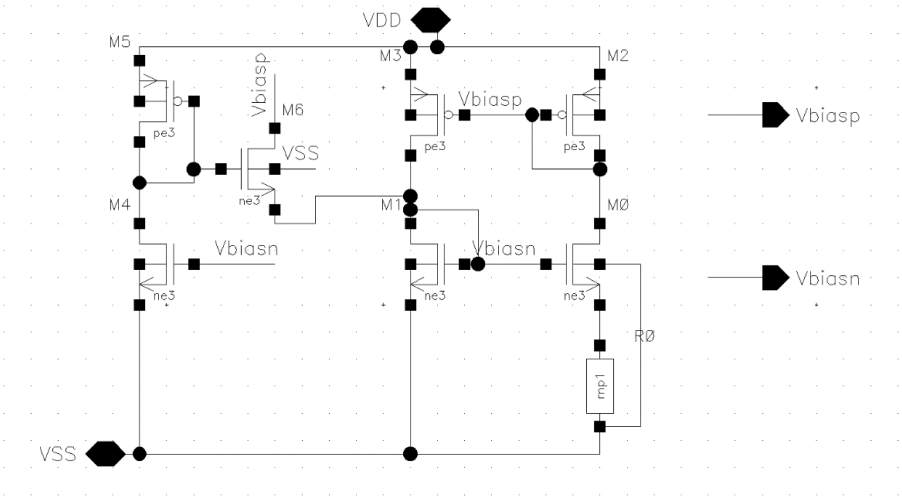

Figure 4: Beta Multiplier Current Reference for Amplifier Biasing

Design and Layout of BGR

With the amplifier and bias circuit made, the BGR was constructed in Cadence. The schematic can be seen in Fig. 5 below.

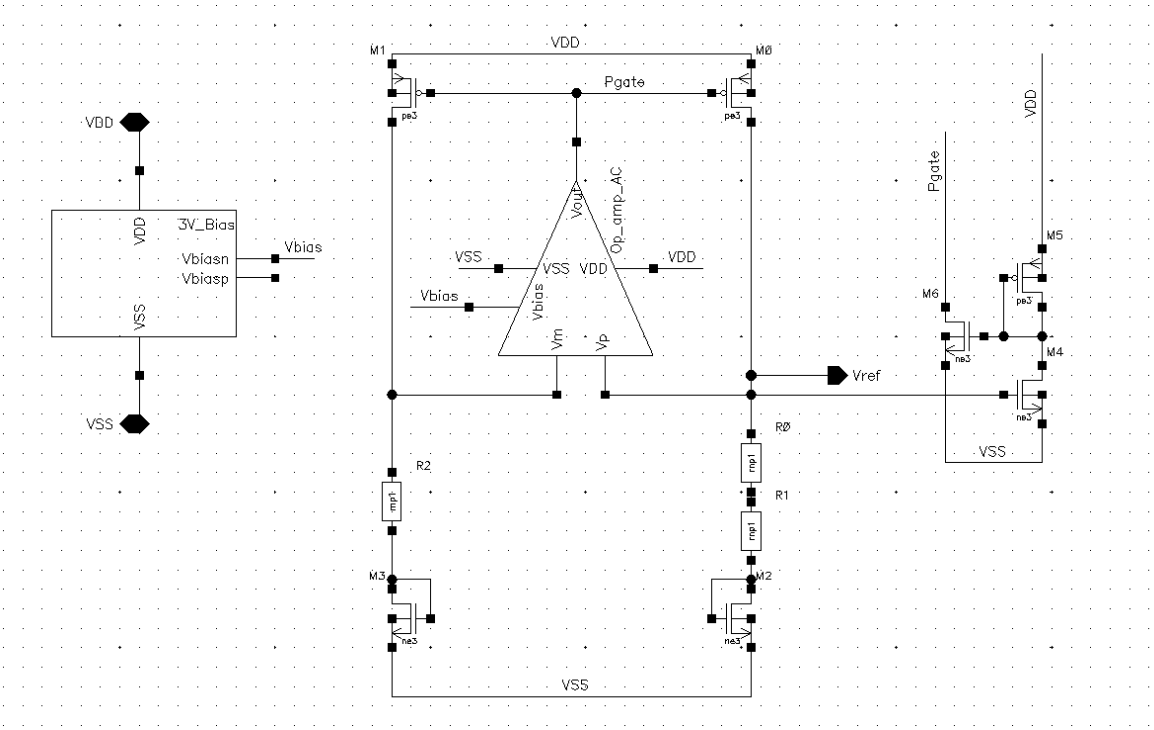

Figure 5: BGR Schematic

The initial resistor values from the Theory section were used, along with the ratio of W_2 to W_1 from Eq. 5. The PMOS at the top are matched at 1 µm/4µm, and the length of the NMOS are both 1 µm. There is also a simple startup circuit to initiate current flow if needed. From the hand calculations and some small tweaks, the best performance obtained of the BGR in simulation was a variation of approximately 50 mV from 20°C to 175°C. To improve the performance, an optimization routine was implemented in Cadence Virtuoso using the ADE XL design environment. The values of the resistors and the widths of both NMOS were used as parameters, as well as the size of the PMOS, but these did not have a significant impact on the performance. The routine was setup to minimize the difference between V_{ref} at the minimum and

maximum temperatures, as well as the minimum and maximum VDD. Some constraints were added to keep the branch current above 1 µA, as well as V_{ref} above 900 mV, for practicality and reliability. After the routine was completed, several sets of parameters yielded desirable results. The parameters used in the final design were chosen to minimize the area of the completed circuit when laid out. The final values in Fig. 5 are W_1 = 3.76 µm, W_2 = 200 µm, and R = 132.5 kΩ. When the resistor value was reduced, the ideal ratio of W_2 to W_1 increased beyond what was initially calculated, but this was deemed acceptable because it reduces the layout area. The resistors have a much greater impact on the chip area than the transistor size, so keeping them as small as possible is ideal.

First, the amplifier and bias circuit blocks were laid out. The bias circuit is an extremely simple device, but the 100 kΩ resistor takes up a considerable amount of space. M3 and M2 from Fig. 4 are laid out in a basic common centroid configuration. The amplifier is also laid out in a common centroid configuration, with the transistors split into more blocks to make the overall shape of the circuit squarer. Since these circuits are very small, the common centroid technique has only a slight effect on reducing device mismatch and is mainly utilized for shaping the layout and reducing the die area of the final circuit [3]. The layout blocks for the amplifier and bias circuit can be seen in Fig. 6 and 7 respectively. With the two supporting circuits complete, the entire BGR circuit was laid out. As with the bias circuit, the resistors accounted for much of the chip area. The two circuit blocks were fitted together, then the remaining components in the schematic were placed to minimize the area. As a simple DC circuit, much more consideration was given to reducing area rather than minimizing parasitics, and there was no discernable difference found between the performance of the circuit with or without parasitics extracted. The final layout has dimensions of 122 µm by 75 µm and can be seen in Fig. 8.

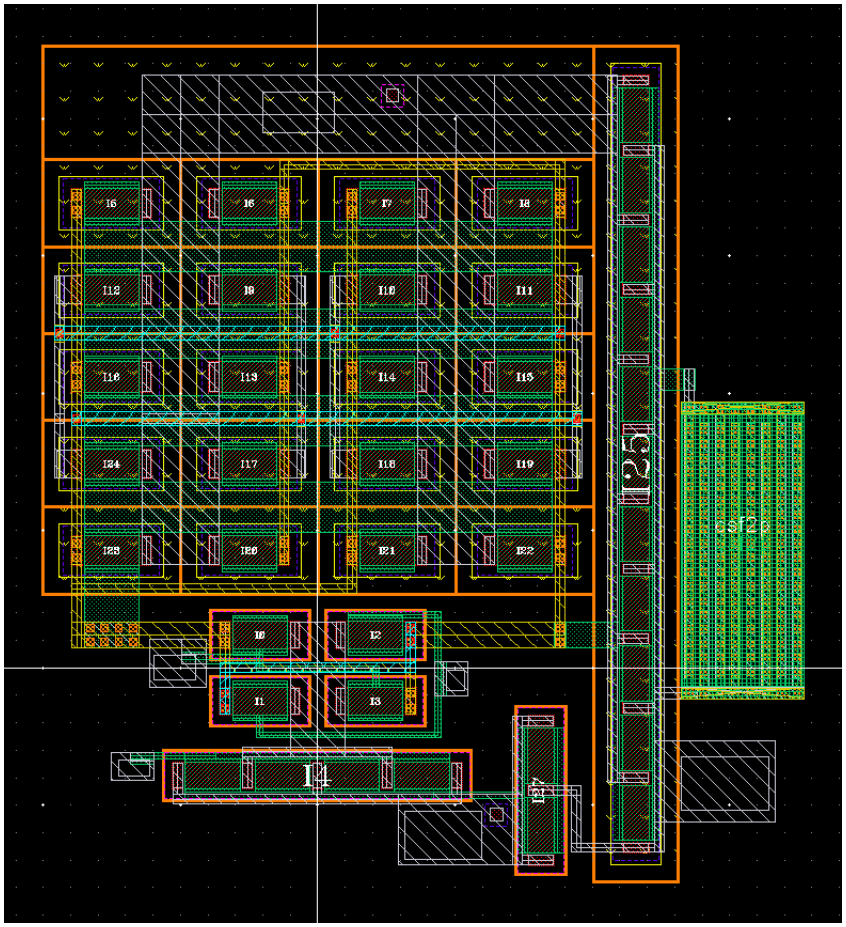

Figure 6: Amplifier Block Layout

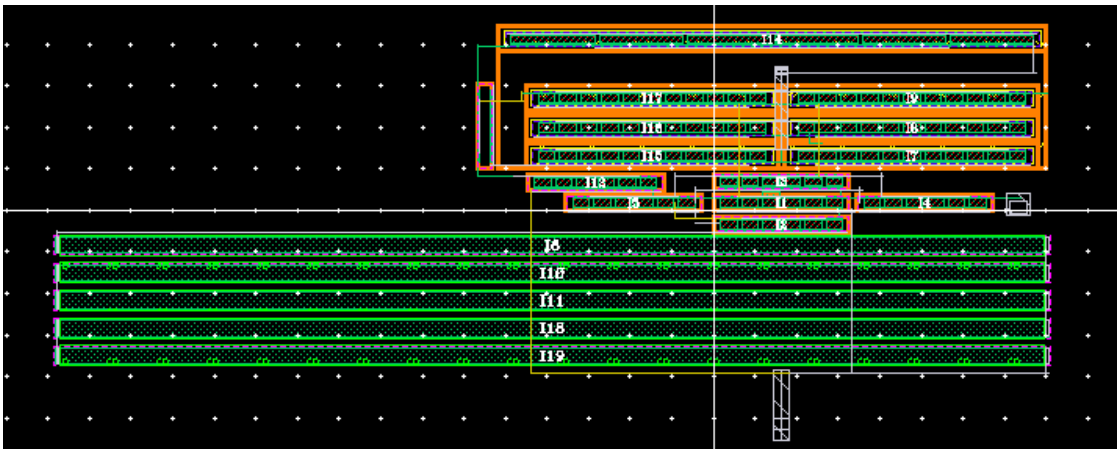

Figure 7: Bias Circuit Block Layout

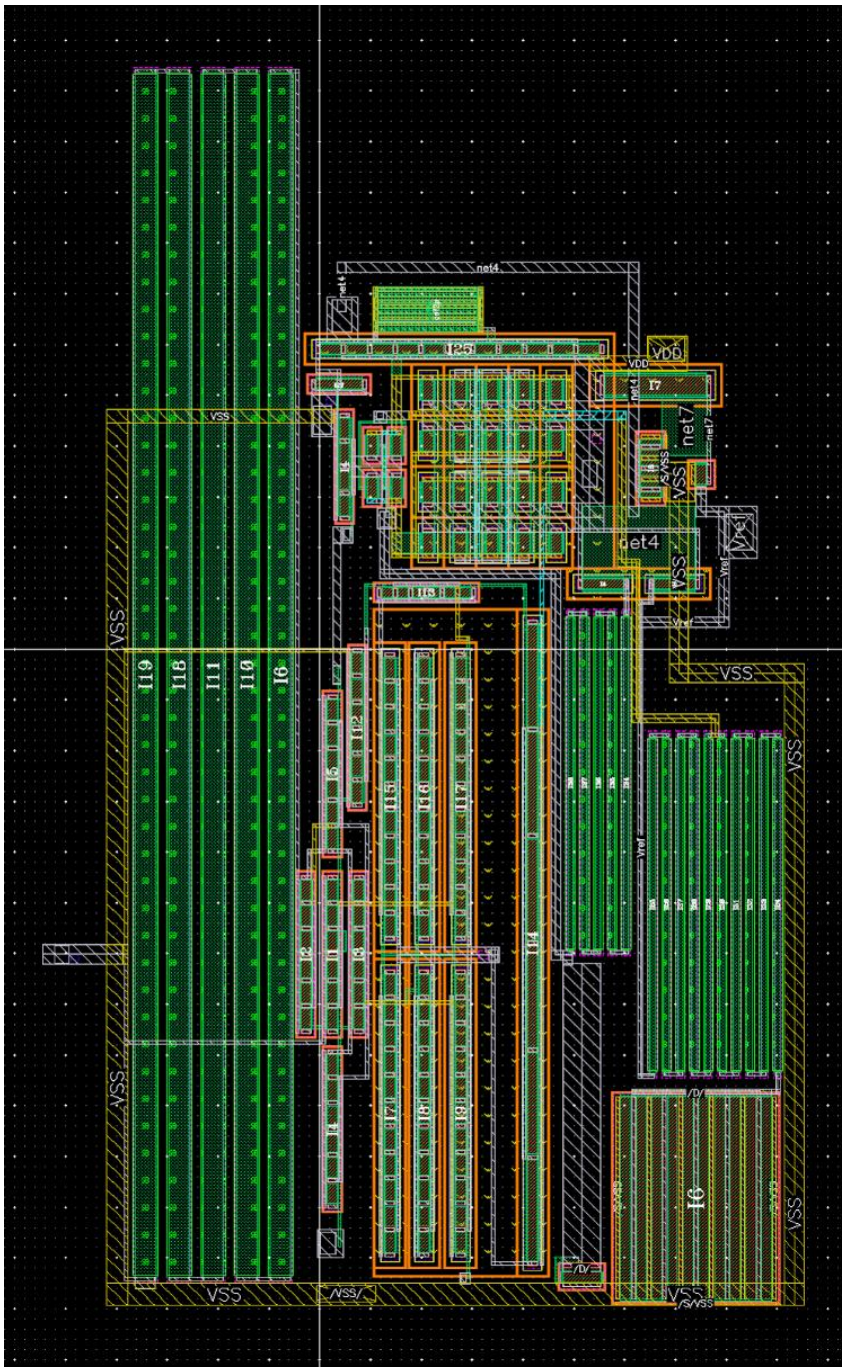

Figure 8: Final BGR Layout

Results

Fig. 9 shows the frequency response of the amplifier designed previously. Fig. 10 shows three traces of V_{ref} over the temperature range with VDD equal to 2 V, 3 V, and 3.6 V. As can be seen, V_{ref} increases slightly when VDD is above the nominal value but is very stable when VDD drops. Table 1 shows the change in V_{ref} while the temperature is swept from 20°C to 175°C at different values of VDD, and Table 2 shows the change in V_{ref} while the supply voltage is swept from 2 V to 3.6 V at different operating temperatures.

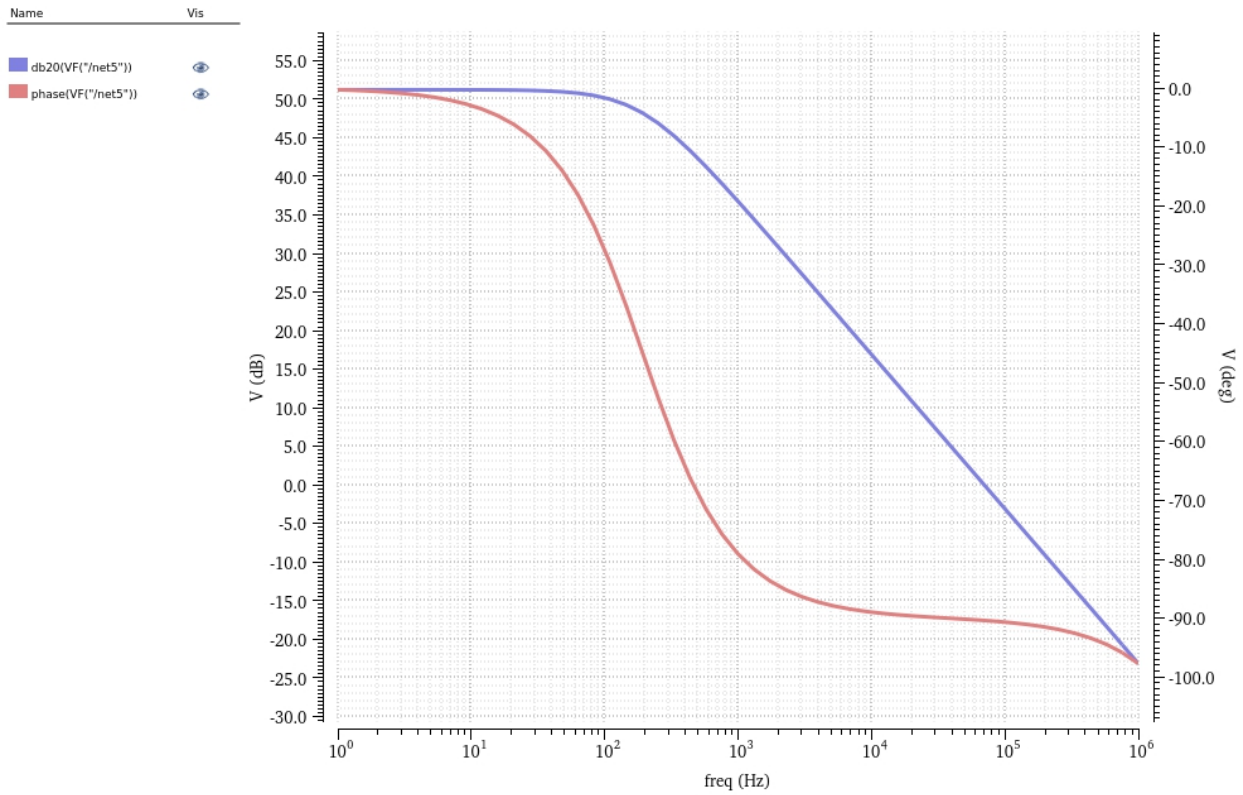

Figure 9: Amplifier Frequency Response

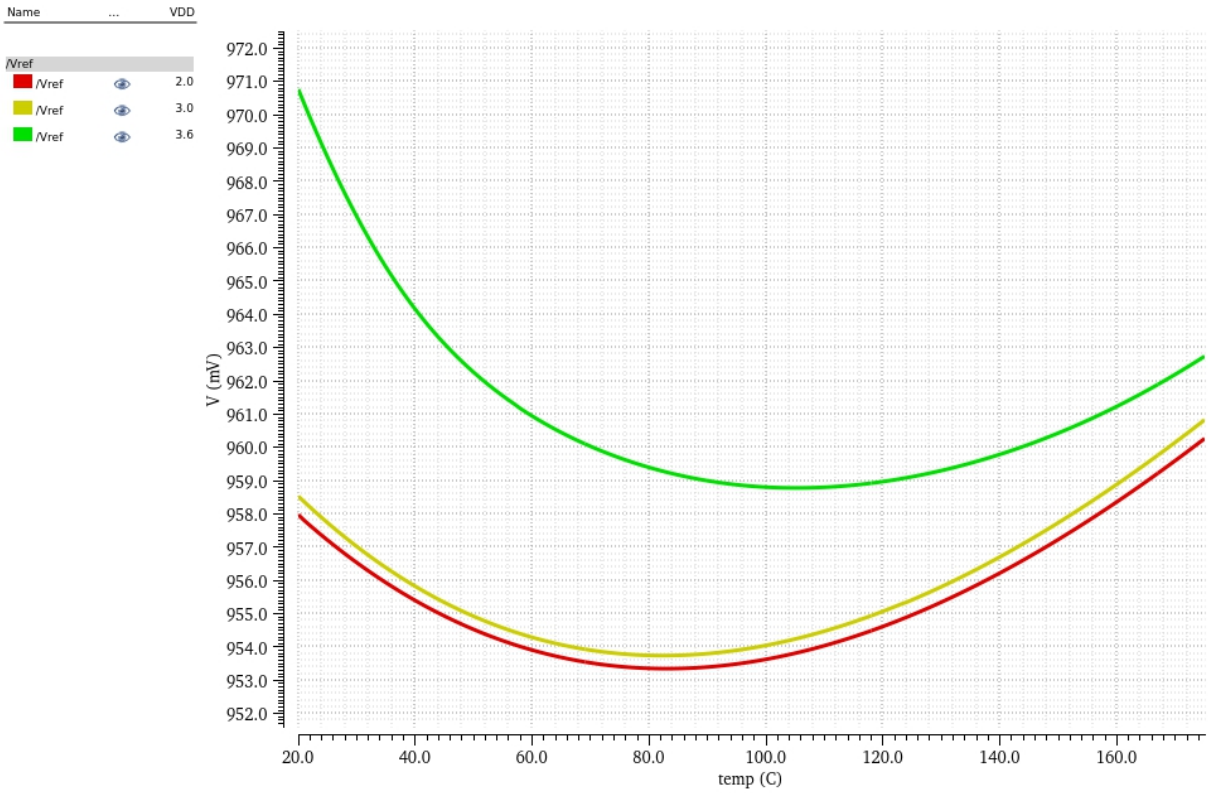

Figure 10: V_{ref} Over Temperature Sweep

Table 1: V_{ref} Over Temperature Variation

$\boldsymbol{VDD}$ (V)	$\boldsymbol{\Delta Vref}$ $\boldsymbol{(mV)}$	$\boldsymbol{Max\ Diff}$ $\boldsymbol{(mV)}$
2	2.6	7.1
2.8	2.8	7.2
Nominal	2.5	7.2
3.6	-7.4	11.5

Table 2: V_{ref} Over Supply Variation

$\boldsymbol{Temp}$ (℃)	$\boldsymbol{\Delta Vref}$ $\boldsymbol{(mV)}$	$\boldsymbol{Max\ Diff}$ $\boldsymbol{(mV)}$
20	12.6	12.6
Nominal	10.9	10.9
97.5	5.4	5.4
175	2.6	2.6

These results were gathered from simulations performed after the parasitic components were extracted from the final layout. As stated before, the parasitics present in the final layout did not affect the performance of the circuit in any meaningful way. The data shows that the reference voltage changes by a maximum of 1.2% of the nominal value over the entire temperature range, and a maximum of 1.3% over the supply voltage range. The data also shows that the circuit is much more tolerable to changes in the supply voltage towards the maximum operating temperature.

Conclusion and Future Work

This paper outlined the design process of a bandgap voltage reference in 180 nm CMOS. The presented circuit performs well, providing a nominal output voltage of 955 mV which changes by less than 1.5% over the entire operating range. It provides an adequately stable reference for an LDO, the intended purpose, but this design would be suitable for many devices which need a stable voltage to operate. The design process was straightforward and successful, but the performance could still be improved. Using an amplifier which is self-biased without resistors would drastically reduce the size of the circuit. Using an amplifier with more stages to increase the gain would also increase the amount of negative feedback, improving the stability over changes in the supply voltage.

References

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