Thin Film Integrated Capacitors with Sputtered-Anodized Niobium Pentoxide Dielectric for Decoupling Applications

Susan Jacob
University of Arkansas

Follow this and additional works at: https://scholarworks.uark.edu/etd

Citation

This Dissertation is brought to you for free and open access by ScholarWorks@UARK. It has been accepted for inclusion in Graduate Theses and Dissertations by an authorized administrator of ScholarWorks@UARK. For more information, please contact scholar@uark.edu.
THIN FILM INTEGRATED CAPACITORS WITH SPUTTERED-ANODIZED NIOBIUM PENTOXIDE DIELECTRIC FOR DECOUPLING APPLICATIONS
THIN FILM INTEGRATED CAPACITORS WITH SPUTTERED-ANODIZED NIOBIUM PENTOXIDE DIELECTRIC FOR DECOUPLING APPLICATIONS

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microelectronics-Photonics

By

Susan Jacob
Visvesvaraya National Institute of Technology
Bachelor of Engineering in Metallurgical Engineering, 2003
University of Missouri-Rolla
Master of Science in Materials Science & Engineering, 2006

December 2009
University of Arkansas
Abstract

Electronics system miniaturization is a major driver for high-k materials. High-k materials in capacitors allow for high capacitance, enabling system miniaturization. Ta$_2$O$_5$ ($k$~24) has been the dominant high-$k$ material in the electronic industry for decoupling capacitors, filter capacitors, etc. In order to facilitate further system miniaturization, this project has investigated thin film integrated capacitors with Nb$_2$O$_5$ dielectric. Nb$_2$O$_5$ has $k$~41 and is a potential candidate for replacing Ta$_2$O$_5$. But, the presence of suboxides (NbO$_2$ and NbO) in the dielectric deteriorates the electrical properties (leakage current, thermal instability of capacitance, etc.). Also, the high oxygen solubility of niobium results in oxygen diffusion from the dielectric to niobium metal, if any is present. The major purpose of this project was to check the ability of NbN as a diffusion barrier and fabricate thermally stable niobium capacitors.

As a first step to produce niobium capacitors, the material characterizations of reactively sputtered Nb$_2$O$_5$ and NbN were done. Thickness and film composition, and crystal structures of the sputtered films were obtained and the deposition parameters for the desired stoichiometry were found. Also, anodized Nb$_2$O$_5$ was characterized for its stoichiometry and thickness.

To study the effect of nitrides on capacitance and thermal stability, Ta$_2$O$_5$ capacitors were initially fabricated with and without TaN. The results showed that the nitride does not affect the capacitance, and that capacitors with TaN are stable up to 150$^\circ$C. In the next step, niobium capacitors were first fabricated with anodized dielectric and the oxygen diffusion issues associated with capacitor processing were studied. Reactively sputtered Nb$_2$O$_5$ was anodized to form complete Nb$_2$O$_5$ (with few oxygen vacancies) and
NbN was used to sandwich the dielectric. The capacitor fabrication was not successful due to the difficulties in anodizing the sputtered dielectric. Another method, anodizing reactively sputtered Nb$_2$O$_5$ and a thin layer of sputtered niobium metal yielded high yield (99%) capacitors. Capacitors were fabricated with and without NbN and the results showed 93% decrease in leakage for a capacitor with ~2000 Å dielectric when NbN was present in the structure. These capacitors could withstand 20 V and showed 2.7 µA leakage current at 5 V. These results were obtained after thermal storage at 100°C and 150°C in air for 168 hours at each temperature.

Two set of experiments were performed using Ta$_2$O$_5$ dielectric: one to determine the effect of anodization end point on the thickness (capacitance) and the second to determine the effect of boiling the dielectric on functional yield. The anodization end point experiment showed that the final current of anodization along with the anodizing voltage determines the anodic oxide thickness. The lower the current, the thicker the films produced by anodization. Therefore, it was important to specify the final current along with the anodization voltage for oxide growth rate. The capacitors formed with boiled wafers showed better functional yield 3 out of 5 times compared with the unboiled wafer.

Niobium anodization was studied for the Nb→Nb$_2$O$_5$ conversion ratio and the effect of anodization bath temperature on the oxide film; a color chart was prepared for thicknesses ranging from 1900 Å — 5000 Å. The niobium metal to oxide conversion ratio was found to change with temperature.
Another area explored in this research was trench capacitors. Fabricating capacitors in trenches yields high capacitance due to increased plate area without increasing device area. The fabrication steps were studied and the issues are discussed.
This dissertation is approved for recommendation to the Graduate Council

Dissertation Director:

_____________________________________  
Dr. Leonard W. Schaper

Dissertation Committee:

_____________________________________  
Dr. Susan L. Burkett

_____________________________________  
Dr. Ingrid Fritsch

_____________________________________  
Dr. Richard Ulrich

_____________________________________  
Prof. Ken Vickers
Dissertation Duplication Release

I hereby authorize the University of Arkansas Libraries to duplicate this dissertation when needed for research and/or scholarship.

Agreed _______________________________

Susan Jacob

Refused _______________________________

Susan Jacob
Acknowledgements

I thank God for all blessings and for leading me through the right path. I thank Dr. Schaper for believing in me and giving me this opportunity to learn and grow. I thank him for his understanding, patience, guidance, support, and for walking me through all the problems/ issues I had in my research. I will always remember him as a great teacher and researcher. I am grateful to Dr. Burkett, Dr. Fritsch, and Dr. Ulrich for being on my committee.

I would like to thank Deepa Mannath for introducing me to Prof. Ken Vickers and the microEP program. Without her support, I wouldn’t be sitting here writing this. I thank all the UARK employees who worked hard to get me admitted into the university in the shortest time possible. I want to thank Prof. Ken Vickers for his support and encouragement throughout this program. I also thank him for taking the initiative to bring me in. I thank Renee Hearon for being there as a source of encouragement and helping me throughout this program.

Research was possible through the use of the High Density Electronic Center at the University of Arkansas, Fayetteville campus. This research was really a group effort and I want to thank Michael Glover, Errol Porter, Jeff Mincy, Mike Steger, Alan Toland, and Tom Cannon for help and support all these years and making me feel at home. Thanks to Dr. Benamara for all the time and selfless service he provided to this research, for sharing the knowledge, and helping me with TEM analysis. I am also thankful to Dr. Hameed Naseem and his student, Hafeez for their help with evaporation process. Thanks to Jeff Wight at Missouri University of Science and Technology for his help with XPS and Auger analysis.
I had a wonderful research group and I thank Yang, Alphonse, Gayathri, and Isi for all the great times we had in the office and outside. Special thanks to Yang for all the ideas and crazy times we had in the clean room. I thank all my friends for the good times I had with you. Thank you, Joe for your support and always being there for me.

Finally and most importantly, I thank my parents and my sister for their prayers and encouragement. I thank God for giving me parents like you and I am really lucky to have you as my parents. I have no words to describe how much I love you all and without you I wouldn’t have reached where I am now. Thank you for all the things you have done for me and for always putting my wishes first. Thanks to my sister, Annie for all the fun and laughter you brought to my life.

This program is financially supported by Irvine Sensors under contract FA8650-04-C7120 from the Defense Advanced Projects Research Agency (DARPA). Any opinions, findings, conclusions, or recommendations expressed in this material are those of the author and do not necessarily reflect the views of Irvine Sensors.
Dedication

This dissertation is dedicated to,

My loving parents, T.J. Jacob and Marcelline Philomena

My sister, Annie Saji Varghese,

My brother-in-law, Saji Varghese,

My niece and nephew, Sheena and Alfie
# Table of Contents

Abstract .................................................................................................................................................... ii

Acknowledgements .................................................................................................................................. vii

Table of Contents .................................................................................................................................. x

List of Figures ........................................................................................................................................ xiv

List of Tables .......................................................................................................................................... xxxiv

Chapter 1: Introduction .......................................................................................................................... 1

Chapter 2: Background .......................................................................................................................... 3

2.1 Decoupling Applications ................................................................................................................. 4

2.2 Niobium ........................................................................................................................................... 7

2.2.1 Niobium Applications .................................................................................................................. 8

2.2.2 Oxides of Niobium ..................................................................................................................... 9

2.2.3 Niobium Pentoxide (Nb$_2$O$_5$) ............................................................................................ 10

2.2.4 Nb$_2$O$_5$ Applications .............................................................................................................. 10

2.2.5 Nb$_2$O$_5$ Deposition Technologies ......................................................................................... 11

2.2.6 Nb$_2$O$_5$ for Capacitors ........................................................................................................... 11

2.3 Niobium Capacitors – State of the Art ......................................................................................... 16

2.4 Issues with Nb$_2$O$_5$—Defining the Problem ............................................................................... 18

2.5 The Solution/Approach Used in This Project .............................................................................. 23

Chapter 3: Dielectric Formation — Technologies Used ......................................................................... 25

3.1 Reactive Sputtering ......................................................................................................................... 25

3.2 Anodization .................................................................................................................................... 28

3.2.1 Anodization Process .................................................................................................................. 28

3.2.2 Anodization profile .................................................................................................................... 30

3.2.3 Anodic Oxide Films and Electrolytes ....................................................................................... 33

Chapter 4: Material Characterization: Technologies Used ................................................................. 35

4.1 Dektak Profilometer ....................................................................................................................... 35

4.1.1 Reason for Usage ....................................................................................................................... 36

4.2 Transmission Electron Microscopy (TEM) ................................................................................... 36

4.2.1 Reason for Usage ....................................................................................................................... 37
Chapter 9: Niobium Anodization

9.1 Nb Anodization Profile

9.2 Nb $\rightarrow$ Nb$_2$O$_5$ Conversion Ratio

9.3 Anodization to the End

9.4 Effect of Anodization Bath Temperature

9.4.1 Fabrication

9.4.2 Cold Anodization

9.4.3 Hot Anodization

9.4.4 Comparison of room temperature, low temperature, and high temperature anodization

9.5 Color Chart of Anodic Nb$_2$O$_5$ Films

Chapter 10: Niobium Capacitors

10.1 Capacitors with anodized dielectric

10.1.1 Fabrication

10.1.2 Results & Discussion

10.2 Solutions to Oxygen Diffusion for the Anodized Dielectric

10.3 Capacitors with reactively sputtered and anodized dielectric

10.3.1 Reactively Sputtered and Anodized Dielectric with NbN

10.3.2 Reactively Sputtered and Anodized Dielectric without NbN

10.4 (Reactively Sputtered Nb$_2$O$_5$ and Niobium) Anodized Capacitors

10.4.1 Dielectric with 1596 Å Nb$_2$O$_5$ at 200 W and 528 Å Nb WITH NbN

10.4.2 Dielectric with 1071 Å Nb$_2$O$_5$ at 200 W and 528 Å Nb WITH NbN

10.4.3 Dielectric with anodized (1071 Å Nb$_2$O$_5$ at 200 W and 528 Å Nb) and gold top plates with no chromium

10.4.4 200 W versus 500 W

10.4.5 (Reactively Sputtered Nb$_2$O$_5$ and niobium) Anodized Capacitors at 500 W

10.4.6 Effect of NbN on electrical properties of Nb$_2$O$_5$ capacitors

Chapter 11: Trench Capacitors

11.1 Motivation

11.2 Trench Design

11.3 Trench Fabrication

11.4 Capacitor Formation in the Trenches

Chapter 12: Conclusions
List of Figures

Figure 2.1: Schematic of a decoupling capacitor on a printed circuit board [14]............. 5

Figure 2.2: Effect of decoupling/bypass capacitor on supply voltage noise in an electrical
circuit [15]........................................................................................................................................... 5

Figure 2.3: A closer look at ripple voltage and ripple current in a circuit with and without
a decoupling capacitor [15]................................................................................................................. 6

Figure 2.4: Niobium-Oxygen phase diagram showing different phases for oxygen
concentration from 0 to 80% [19]......................................................................................................... 9

Figure 2.5: Chemical structure of niobium pentoxide (Nb_2O_5). ........................................ 10

Figure 2.6: Oxicap® capacitors from AVX Corporation [49]............................................... 17

Figure 2.7: Diffusion profiles of oxygen diffusion from Nb_2O_5 to Nb at 125°C at 1 hour,
10 hours, and 168 hours................................................................................................................... 22

Figure 2.8: Nb—Nb_2O_5 interface at (a) t = 0 and (b) t = 168 hours at 125°C................. 22

Figure 3.1: Schematic of a reactive sputtering system/process. ............................................. 26

Figure 3.2: Anodization setup at HiDEC; (a) setup and (b) anodization bath containing
anode, cathode, and the electrolyte. ................................................................................................. 29

Figure 3.3: Anodization voltage, current, and oxide thickness variation with time [after
60]........................................................................................................................................................ 31

Figure 3.4: Anodization profiles of (a) tantalum metal and (b) reactively sputtered
tantalum pentoxide............................................................................................................................. 32

Figure 4.1: Schematic of profilometer stylus scanning across a thin film surface. .......... 36

Figure 4.2: Electron and ion gun positions (a) before and (b) after tilting the sample to
52° ......................................................................................................................................................... 39
Figure 4.3: (a) shows the platinum strip and the trenches (b) a closer look at the specimen, the platinum strip, and the trenches with the excess material removed... 40

Figure 4.4: A close-up view of the sample and the platinum strip showing the thickness of SiO$_2$ in this sample.................................................................................................................. 40

Figure 4.5: (a) Omniprobe and platinum GIS needle inserted, (b) closer view at the specimen location, (c) Omniprobe connected to the specimen with a platinum patch showing the edges and bottom cuts, and (d) Omniprobe and the specimen before lift out. ........................................................................................................................................ 42

Figure 4.6: (a) Omniprobe lifting the sample out and (b) sample attached to the Omniprobe with a 500 nm thick platinum patch. ................................................................. 43

Figure 4.7: (a) Omniprobe with the specimen at the TEM grid, (b) specimen close to the grid, (c) specimen touching the grid, and (d) After Omniprobe removal and polishing...................................................................................................................................... 43

Figure 4.8: Finished sample ready to be loaded into TEM.................................................. 44

Figure 4.9: Schematic illustration of the XPS system. ............................................................ 46

Figure 4.10: Energy level diagram for an Auger process. Steps 2, 3, and 4 are key steps in the process........................................................................................................................................ 48

Figure 5.1: Schematic of a parallel plate capacitor................................................................. 50

Figure 5.2: Capacitor and its parasitic components modeled as a series R, L, C circuit. 53

Figure 5.3: Impedance versus Frequency of an ideal capacitor [74] ................................. 55

Figure 5.4: Impedance versus Frequency plot of a practical capacitor [74]................. 56

Figure 5.5: Vector diagram for the series RLC circuit: model shown in Figure 5.2. ....... 57

Figure 6.1: Mask for top plate etching in tantalum capacitor fabrication....................... 60
Figure 7.1: Thermally oxidized silicon substrate................................................................. 62

Figure 7.2: Copper bottom plate and titanium adhesion layer sputter deposited on oxidized silicon. .......................................................................................................................... 63

Figure 7.3: Ta$_2$O$_5$ reactively sputtered on copper bottom plate.................................... 63

Figure 7.4: Anodized dielectric and exposed bottom plate for contact. ......................... 64

Figure 7.5: Copper top plate sputter deposited on Ta$_2$O$_5$ dielectric. ......................... 64

Figure 7.6: Photoresist patterning with plating mask for Ni/Au plating......................... 65

Figure 7.7: Ni/Au plating for capacitor top plate contacts............................................... 66

Figure 7.8: Photoresist stripped after Ni/Au plating and new photoresist patterned for copper etching. .................................................................................................................. 66

Figure 7.9: Capacitor structure with Ta$_2$O$_5$ dielectric and copper top and bottom plates with Ni/Au contacts. ........................................................................................................ 67

Figure 7.10: TaN sputter deposited on copper bottom plate........................................... 67

Figure 7.11: Reactively sputtered and anodized Ta$_2$O$_5$ on TaN diffusion barrier........ 68

Figure 7.12: The anodization profile of a 2000 Å Ta$_2$O$_5$ on an entire 125 mm wafer anodized at 61 mA and 125 V .............................................................. 68

Figure 7.13: TaN reactively sputtered on reactively sputtered-anodized Ta$_2$O$_5$ dielectric, forming a sandwich structure................................................................. 69

Figure 7.14: Copper top plate sputtered and patterned for Ni/Au plating. ................. 70

Figure 7.15: Capacitor structure after Ni/Au plating (a) before photoresist removal and (b) after removal.............................................................. 70

Figure 7.16: Capacitor structure with TaN diffusion barrier sandwiching the Ta$_2$O$_5$ dielectric........................................................................ 71
Figure 7.17: Sputtered-anodized Ta$_2$O$_5$ capacitors without TaN diffusion barrier in the as-deposited state. ................................................................................................................................. 72

Figure 7.18: Sputtered-anodized Ta$_2$O$_5$ capacitors with TaN diffusion barrier in the as-deposited state. ................................................................................................................................. 74

Figure 7.19: Sputtered-anodized Ta$_2$O$_5$ capacitors with TaN diffusion barrier after 168 hours in N$_2$ at 100°C. ................................................................................................................................. 76

Figure 7.20: Sputtered-anodized Ta$_2$O$_5$ capacitors with TaN diffusion barrier after 168 hours in N$_2$ at 150°C. ................................................................................................................................. 77

Figure 7.21: Schematic of capacitor structure of Ta$_2$O$_5$ dielectric with copper top and bottom plates. ................................................................................................................................. 80

Figure 7.22: Capacitance data of Ta$_2$O$_5$ capacitors anodized to a final current of 10% of initial current; end point at 6.1 mA. ................................................................................................................................. 81

Figure 7.23: Capacitance data of Ta$_2$O$_5$ capacitors anodized to a final current of 0.51 mA. ................................................................................................................................. 83

Figure 7.24: Processed wafers showing different dielectric colors: (a) 0.51 mA wafer and (b) 6.1 mA wafer. ................................................................................................................................. 84

Figure 7.25: Schematic of the capacitor structure of the boiled and unboiled wafers. ..... 88

Figure 7.26: Capacitance data of the unboiled Ta$_2$O$_5$ capacitors, anodized at 125 V to a final current of 1 mA. ................................................................................................................................. 89

Figure 7.27: Capacitance data of the boiled Ta$_2$O$_5$ capacitors, anodized at 125 V to a final current of 1 mA: anodized dielectric boiled in water for 30 minutes. ....................... 89

Figure 7.28: Capacitance data of (a) Boiled #2, (b) Boiled #3, (c) Boiled #4, and (d) Boiled #5. ................................................................................................................................. 90
Figure 8.1: Deposition rate of niobium at different sputtering powers................................. 95
Figure 8.2: Deposition rate of niobium at 2200 W at different sputtering times............. 96
Figure 8.3: The Auger depth profile of the Nb$_2$O$_5$ film on silicon substrate sputter
deposited at 100 W, showing Nb, O, and Si only. ......................................................... 98
Figure 8.4: Graph showing niobium oxide deposition rate as a function of sputtering
power, based on Table 8.4. ......................................................................................... 99
Figure 8.5: Cross-sectional view of the reactively sputtered Nb$_2$O$_5$ sputtered at 200 W for
6000 seconds in Ar/O$_2$ (90:10) at 10 mTorr showing a thickness of 3400 Å. ....... 100
Figure 8.6: Niobium oxide deposition rate as a function of sputtering power from Table
8.4 and Table 8.5 showing TEM data point at 200 W. ........................................... 101
Figure 8.7: Cross-sectional view of the reactively sputtered Nb$_2$O$_5$ at 500 W; (a) Nb$_2$O$_5$
and adjacent layers and (b) Nb$_2$O$_5$ showing columnar structure. ......................... 102
Figure 8.8: Nb 3d spectrum of niobium oxide, reactively sputtered at 100 W in the as-
deposited state (a) before and (b) after peak fitting. ............................................... 103
Figure 8.9: Nb 3d spectrum of niobium oxide, reactively sputtered at 100 W after Ar$^+$
etching (a) before and (b) after peak fitting ................................................................. 104
Figure 8.10: Auger depth profile of the Nb$_2$O$_5$ film on silicon substrate sputtered at 100
W.................................................................................................................................... 105
Figure 8.11: O/Nb ratio calculated from the depth profile of sputtered film at 100 W, as a
function of sputter time ............................................................................................. 107
Figure 8.12: Nb 3d spectrum of niobium oxide, reactively sputtered at 200 W in the as-
deposited state (a) before and (b) after curve fitting ............................................... 108
Figure 8.13: Nb 3d spectrum of niobium oxide, reactively sputtered at 200 W after Ar$^+$ etching (a) before and (b) after peak fitting. ................................................................. 108

Figure 8.14: Auger depth profile of the Nb$_2$O$_5$ film on silicon substrate sputtered at 200 W ...................................................................................................................... 110

Figure 8.15: O/Nb ratio calculated from the depth profile of sputtered film at 200 W, as a function of sputter time. .............................................................................................................. 111

Figure 8.16: Nb 3d spectrum of niobium oxide, reactively sputtered at 300 W in the as-deposited state. .................................................................................................................. 112

Figure 8.17: Nb 3d spectrum of niobium oxide, reactively sputtered at 300 W after Ar$^+$ etching (a) before and (b) after peak fitting. ................................................................. 113

Figure 8.18: Nb 3d surface spectrum of niobium oxide, reactively sputtered at 400 W (a) before and (b) after peak fitting. .................................................................................... 114

Figure 8.19: Nb 3d spectrum of niobium oxide, reactively sputtered at 400 W after Ar$^+$ etching (a) before and (b) after peak fitting. ................................................................. 114

Figure 8.20: Nb 3d surface spectrum of niobium oxide, reactively sputtered at 500 W (a) before and (b) after peak fitting. .................................................................................... 115

Figure 8.21: XPS Nb3d surface spectrum of Nb—O film, reactively sputtered at 500 W. ............................................................................................................................... 116

Figure 8.22: Nb 3d spectrum of niobium oxide, reactively sputtered at 500 W after Ar$^+$ etching (a) before and (b) after peak fitting. ................................................................. 117

Figure 8.23: Percentage of each compound present on the surface of the reactively sputtered film at different sputtering powers before and after Ar$^+$ etching. .......... 119
Figure 8.24: Electron diffraction patterns taken from the niobium oxide film sputtered at
(a) 200 W and (b) 500 W indicating the amorphous nature of the film................. 120

Figure 8.25: Cross-sectional view of Nb$_2$O$_5$ anodized at 83 V and 0.5 mA/cm$^2$ to a final
current of 1 mA: (a) Image showing thickness and double layer of Nb$_2$O$_5$ with gold
and niobium on either side (b) Comparison of porous top layer and dense bottom
layer (c) Bottom layer of Nb$_2$O$_5$ and Nb interface, and (d) Cross-section contrasting
two layers of Nb$_2$O$_5$, ........................................................................................................ 122

Figure 8.26: Cross-sectional view of Nb$_2$O$_5$ anodized in the galvanostatic regime only, at
83 V and 0.5 mA/cm$^2$: (a) Image showing multiple layers in the wafer (b)
thicknesses and double layer of Nb$_2$O$_5$ with gold and niobium on either side. ...... 123

Figure 8.27: Nb$_2$O$_5$ film anodized in the galvanostatic regime, at 83 V and 0.5 mA/cm$^2$
current density, (a) both the layers of the oxide film and (b) bottom layer, the layer
close to Nb. .................................................................................................................................. 124

Figure 8.28: Double layer oxide structure correlating to AES depth profile............. 126

Figure 8.29: XPS Nb 3d surface spectrum of the anodized niobium oxide CENTER. .. 127

Figure 8.30: XPS spectrum (Nb 3d) of anodized niobium oxide CENTER after Ar$^+$
etching.............................................................................................................................................. 128

Figure 8.31: Depth profile of CENTER niobium oxide anodized at 83 V and 0.5 mA/cm$^2$
current density.......................................................................................................................... 129

Figure 8.32: O/Nb ratio calculated from the depth profile of the oxide film (CENTER),
anodized at 83 V, as a function of sputter depth........................................................................ 130

Figure 8.33: XPS spectrum (Nb 3d) of as-deposited anodized niobium oxide LEFT.... 131
Figure 8.34: XPS spectrum (Nb 3d) of anodized niobium oxide LEFT after Ar⁺ etching.
........................................................................................................................................ 131

Figure 8.35: Depth profile of LEFT niobium oxide anodized at 83 V and 0.5 mA/cm²

current density.......................................................................................................................... 132

Figure 8.36: O/Nb ratio calculated from the depth profile of the oxide film (LEFT),
anodized at 83 V, as a function of sputter depth................................................................. 133

Figure 8.37: Comparison of O/Nb ratios from the LEFT and CENTER samples......... 134

Figure 8.38: Electron diffraction pattern of anodized Nb₂O₅ (a) galvanostatic and
potentiostatic modes were used and (b) only galvanostatic mode was used. ........ 135

Figure 8.39: Cross-sectional view of the reactively sputtered (Nb₂O₅ + sputtered Nb)
anodized oxide; (a) showing the multilayered structure and (b) showing the crack
propagation at the reactively sputtered and anodized oxide interface. ..................... 136

Figure 8.40: Schematic of stages of crack formation during anodization; (a) before
anodization, (b) volume change of Nb during anodization, and (c) crack formation.
........................................................................................................................................ 137

Figure 8.41: Cross-sectional TEM image of reactively sputtered (Nb₂O₅ + sputtered Nb)
anodized oxide from the RIGHT area of the wafer; (a) showing the multilayered
structure and (b) showing total Nb₂O₅ thickness and individual oxide layers........ 137

Figure 8.42: Electron diffraction pattern of (reactively sputtered Nb₂O₅ + sputtered Nb)
anodized Nb₂O₅ (a) right and (b) center................................................................. 138

Figure 8.43: Graph showing niobium nitride deposition rate as a function of sputtering
power, based on Table 8.12. ......................................................................................... 140
Figure 8.44: Cross-sectional view of a silicon wafer with multiple thin films including NbN sputtered at 2200 W for 25 seconds in Ar/N\textsubscript{2} at 5 mTorr; (a) multilayered structure and (b) NbN thickness. ................................................................. 141

Figure 8.45: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 800 W in the as-deposited state; (a) original data and (b) after curve fitting. .......... 142

Figure 8.46: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 800 W after Ar\textsuperscript{+} etching. ......................................................... 143

Figure 8.47: XPS Nb 3d surface spectrum of the niobium nitride thin film reactively sputtered at 1500 W. ................................................................. 145

Figure 8.48: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 1500 W after Ar\textsuperscript{+} etching. ......................................................... 146

Figure 8.49: XPS Nb 3d surface spectrum of the niobium nitride thin film reactively sputtered at 2000 W. ................................................................. 147

Figure 8.50: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 2000 W after Ar\textsuperscript{+} etching. ......................................................... 148

Figure 8.51: XPS Nb 3d surface spectrum of the niobium nitride thin film reactively sputtered at 2200 W. ................................................................. 149

Figure 8.52: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 2200 W after Ar\textsuperscript{+} etching. ......................................................... 150

Figure 9.1: Anodization profile of niobium metal anodized to 83 V at 0.5 mA/cm\textsuperscript{2} current density at room temperature......................................................... 152

Figure 9.2: Cross-sectional view of (a) sputtered Nb (b) anodized Nb wafer showing Nb\textsubscript{2}O\textsubscript{5} and the residual Nb. ......................................................... 154
Figure 9.3: Anodization profile of Nb, anodized at 83 V and 0.5 mA/cm² in room temperature for ~2.5 days; 3 (a) full time scale for voltage and current (log scale) and 3 (b) first hour of anodization showing galvanostatic regime and the initial current decrease. Current is in log scale. ................................................................. 158

Figure 9.4: Anodization setup to maintain cold bath temperature. ......................... 160

Figure 9.5: Anodization profile of a niobium wafer anodized at 83 V and 0.5 mA/cm² at 1°C—4°C. ............................................................................................................ 160

Figure 9.6: Cross-sectional view of the wafer anodized at 1°C—4°C; (a) shows all the layers including top Pt, Au, Cr, Nb₂O₅, and Nb and (b) shows the anodized film and the thicknesses. ........................................................................................................... 161

Figure 9.7: The electron diffraction pattern of Nb₂O₅ formed at 1°C—4°C electrolyte temperature. ............................................................................................................. 162

Figure 9.8: Anodization profile of a niobium wafer anodized at 83 V and 0.5 mA/cm² at 61°C—64°C. .............................................................................................................. 163

Figure 9.9: Cross-sectional view of the wafer anodized at 61°C—64°C; (a) shows all the layers including top Pt, Au, Cr, Nb₂O₅, and Nb and (b) shows the anodized film and the layer thicknesses, (c) shows the residual Nb and its thickness, and (d) diffraction pattern of the oxide. ................................................................................................................. 164

Figure 9.10: Nb₂O₅ films anodized at (a) 1°C-4°C, (b) 20°C, and (c) 61°C-64°C. ....... 166

Figure 9.11: Anodization profiles of Nb in cold, hot, and room temperatures. .......... 166

Figure 9.12: Arrhenius plot of ionic conductivity for 4°C, 20°C, and 64°C. ............. 169

Figure 9.13: (a) Nb₂O₅ thickness and (b) ionic conductivity as a function of temperature. .......................................................................................................................... 170
Figure 9.14: Anodization profiles of seven wafers anodized from 83 V to 218.3 V...... 172

Figure 9.15: Time to reach anodization set voltage versus anodization voltage and oxide thickness................................................................. 174

Figure 9.16: Anodic oxide thickness versus anodization voltage for a final current of 1 mA.................................................................................. 174

Figure 9.17: Color bar of Nb2O5 films according to their thicknesses. ....................... 175

Figure 9.18: Nb2O5 films anodized at (a) 83 V, (b) 109.2 V, (c) 131.0 V, (d) 152.8 V, (e) 174.7 V, (f) 196.5 V, and (g) 218.3 V to a final current of 1 mA......................... 176

Figure 10.1: Schematic of the cross-section of anodized Nb2O5 capacitors.............. 178

Figure 10.2: Capacitance data of anodized Nb2O5 capacitors with copper top and bottom plates. ........................................................................................................... 179

Figure 10.3: Niobium/Nb2O5 interface (a) before sputtering and (b) after sputtering.... 180

Figure 10.4: Process flow for capacitors with anodized dielectric and NbN diffusion barrier .................................................................................................. 181

Figure 10.5: AFM images showing surface morphology of Nb2O5 films at (a) pH = 2.2 and (b) pH = 5.6. ................................................................. 183

Figure 10.6: Capacitance data of anodized Nb2O5 capacitors with evaporated aluminum top plates. .................................................................................................. 187

Figure 10.7: Capacitance data for anodized Nb2O5 capacitors with evaporated aluminum top plates in N2 after 100°C for 8 hours........................................... 188

Figure 10.8: The anodization profile of a 2088 Å Nb2O5 film, reactively sputtered at 500 W in Ar:O2 (90:10) gas mixture for 1200 seconds. ......................... 190

Figure 10.9: The 2088 Å Nb2O5 after anodization at 83 V and 0.5 mA/cm².............. 191
Figure 10.10: The capacitance data of the reactively sputtered and anodized dielectric with NbN.

Figure 10.11: Anodization profile of a 3400 Å Nb$_2$O$_5$ reactively sputtered at 200 W...

Figure 10.12: Dielectric breakdown during anodization of Nb$_2$O$_5$ reactively sputtered at 200 W.

Figure 10.13: Capacitance data with Nb$_2$O$_5$ reactively sputtered at 200 W and anodized to 70 V.

Figure 10.14: Reactively sputtered dielectric without NbN (a) before anodization and (b) after anodization.

Figure 10.15: Reactively sputtered dielectric without NbN after anodization showing defect concentration (a) just outside the center circle (rim area) (b) just outside the rim (c) further away.

Figure 10.16: Nb$_2$O$_5$ dielectric breakdown during anodization, identifying each layer on the wafer.

Figure 10.17: Schematic of the cross-section of a (reactively sputtered Nb$_2$O$_5$ + Nb) anodized dielectric with NbN and aluminum top plates.

Figure 10.18: Capacitance plot of a (reactively sputtered 1596 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with aluminum top plates.

Figure 10.19: Capacitance distribution in the center row of the wafer with (reactively sputtered 1596 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with aluminum top plates.

Figure 10.20: Comparison of center capacitances as a function of time spent in the furnace.
Figure 10.21: Capacitance of the center capacitor (BF row and #35 column) as a function of heat treatment time. ................................................................. 207

Figure 10.22: Different mechanisms in the Nb/Nb$_2$O$_5$/Al stack during heat treatment at 100°C in N$_2$. ........................................................................................................... 208

Figure 10.23: Capacitance of the edge capacitor (BF row and #1 column) as a function of heat treatment time................................................................. 209

Figure 10.24: Capacitance data during different stages of heat treatment; (a) as-deposited, (b) after 4 hours, (c) after 8 hours, and (d) after 12 hours. ......................... 212

Figure 10.25: Capacitance data during different stages of heat treatment, continuing from Figure 10.24: (e) after 18 hours, (f) after 26 hours, (g) after 38 hours, (h) after 62 hours, and (i) after 120 hours and 40 minutes. All the times mentioned are cumulative hours................................................................. 213

Figure 10.26: Anodization profile of a reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal ......................................................................................... 214

Figure 10.27: Reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb after anodization at 83 V and 0.5 mA/cm$^2$. ........................................................................................................... 215

Figure 10.28: Capacitance plot of a (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with aluminum top plates. .............................. 216

Figure 10.29: Capacitance distribution at the center of the wafer with (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with aluminum top plates. ......................................................................................... 217

Figure 10.30: Schematic cross-section of the wafer with the new top plate structure, Cr/Au/Ni/Cr/Au. ......................................................................................... 218
Figure 10.31: Capacitance plot of a (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates. ........................................... 219

Figure 10.32: Capacitance distribution at the center of the wafer with (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates. ................................................................................. 220

Figure 10.33: Capacitance plot of a (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates after 168 hours in air at 85°C (a) capacitance scale 6 nF and (b) at a scale 3 nF. ......................................................... 221

Figure 10.34: Comparison of capacitance data from the center of the wafer with aluminum top plates, Cr/Au/Ni/Cr/Au top plates and boiled dielectric, and with Cr/Au/Ni/Cr/Au top plates after 168 hours in air at 85°C. ................................................. 222

Figure 10.35: Schematic of Nb$_2$O$_5$ and its adjacent layers after heat treatment. ........ 223

Figure 10.36: Anodization profile of a reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal................................................................................................................................. 224

Figure 10.37: Dielectric and adjacent layers (a) before heat treatment, (b) after 169 hours at 85°C, (c) after 168 hours at 100°C, and (d) after 168 hours at 124°C. ................. 225

Figure 10.38: Anodization profile of a reactively sputtered 1044 Å Nb$_2$O$_5$ (at 500 W) + 528 Å Nb metal without NbN under the dielectric. ................................................................. 230

Figure 10.39: Anodization profile of a reactively sputtered 1044 Å Nb$_2$O$_5$ (at 500 W) + 528 Å Nb metal with NbN under the dielectric. ................................................................. 230

Figure 10.40: Capacitance plot of a set #1 (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates...... 235
Figure 10.41: Capacitance plot of a set #1 (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air. ................................................................. 236

Figure 10.42: Comparison of center capacitance data for the set #1 wafer with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN before and after heat treatment. ................................................................. 237

Figure 10.43: Magnitude of the impedance of two capacitors with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates, taken in the floating plate configuration. ....................... 238

Figure 10.44: Phase of the impedance of the capacitor with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates. ................................................................. 239

Figure 10.45: Current (log scale) versus voltage of a capacitor with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates. ................................................................. 240

Figure 10.46: Leakage current at 5 V as a function of time for the capacitor without NbN. ................................................................................................................................. 241

Figure 10.47: Capacitance plot of a set #1 (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates. ..................... 242

Figure 10.48: The center row capacitance distribution on the wafer from left end to the right with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates. ........................................ 243
Figure 10.49: Capacitance plot of a Set #1 (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air. ................................................................. 244

Figure 10.50: Comparison of center capacitance data for the set #1 wafer with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN before and after heat treatment................................................................. 245

Figure 10.51: Capacitance distribution in the top, center, and bottom of the set #1 wafer with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN after heat treatment................................................................. 246

Figure 10.52: Current versus voltage of a capacitor set #1 with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates. ................................................................. 247

Figure 10.53: Current at 5 V versus time for a capacitor located at the center of the wafer, (1044 Å Nb₂O₅ + 528 Å Nb) anodized dielectric with NbN. ................................................. 248

Figure 10.54: Comparison of capacitance data from the center row of the set #1 wafers with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with and without NbN................................................................. 250

Figure 10.55: Comparison of center capacitances obtained for the set #1 wafers with and without NbN................................................................. 251

Figure 10.56: Capacitance plot of a set #2 (reactively sputtered 904 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates................. 252
Figure 10.57: Capacitance plot of a set #2 (reactively sputtered 904 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air. ................................................................. 253

Figure 10.58: Comparison of center capacitance data for the set #2 wafer with (reactively sputtered 904 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN before and after heat treatment ........................................................................................................ 254

Figure 10.59: Current (log scale) versus voltage of a capacitor with (reactively sputtered 904 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates. ................................................................. 255

Figure 10.60: Capacitance plot of a set #3 (reactively sputtered 696 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates. ................................................. 256

Figure 10.61: Capacitance plot of a set #3 (reactively sputtered 696 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air. ................................................................. 257

Figure 10.62: Comparison of center capacitance data for the set #3 wafer with (reactively sputtered 696 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN before and after heat treatment .................................................................................. 258

Figure 10.63: Compilation of the impedance magnitude of two capacitors in the floating plate configuration, located at top, bottom, center, left, and right areas of the wafer with (reactively sputtered 696 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric without NbN. ................................................................. 260

Figure 10.64: Impedance magnitude of a niobium leaky capacitor. Note the deviation from the model. ......................................................................................................................... 261

xxx
Figure 10.65: Impedance phase of a niobium leaky capacitor. Note the deviation from the model. .............................................................................................................................. 261

Figure 10.66: Current versus voltage of a capacitor with (reactively sputtered 696 Å
Nb2O5 + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top
plates. .......................................................................................................................... 262

Figure 10.67: Current (log scale) at 5 V versus time for capacitors located at the bottom,
center, and the top of the wafer, without NbN......................................................... 263

Figure 10.68: Capacitance plot of a set #3 wafer with (reactively sputtered 696 Å Nb2O5
+ 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates. .... 264

Figure 10.69: Capacitance plot of a set #3 wafer with (reactively sputtered 696 Å Nb2O5
+ 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air. ................................. 265

Figure 10.70: Comparison of center capacitance data for the set #3 wafer with (reactively
sputtered 696 Å Nb2O5 + 528 Å Nb metal) anodized dielectric with NbN before and
after heat treatment.................................................................................................. 266

Figure 10.71: Current (log scale) versus voltage of a capacitor with (reactively sputtered
696 Å Nb2O5 + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au
top plates. ................................................................................................................ 267

Figure 10.72: Leakage current at 5 V versus time for capacitors located at the bottom,
center, and the top of the wafer, with NbN; current in logarithmic scale. ............ 268

Figure 10.73: Comparison of measured capacitances and calculated capacitances for
different dielectric thicknesses.................................................................................. 271
Figure 10.74: Leakage current (log scale) at 5 V of capacitors located at the center of the sets #1 and #3 wafers, as a function of time. .......................................................... 273

Figure 10.75: Leakage current as a function of applied voltage ........................................... 274

Figure 10.76: Comparison of currents at 5 V after 5 minutes of application of voltage for #1 and #3 wafer sets. ............................................................................................. 275

Figure 10.77: Poole-Frenkel plot for wafer set #3 wafers. ................................................ 276

Figure 11.1: Comparison of the area availability of a (a) planer capacitor and a (b) trench capacitor. .............................................................................................................. 278

Figure 11.2: (a) Mask used for trench formation and (b) schematic of a cell showing trench widths and the pitch. ................................................................. 279

Figure 11.3: Three sets of trenches with bottom openings (a) 20 microns, (b) 25 microns, and (c) 30 microns after DRIE. ................................................................. 282

Figure 11.4: Process flow for trench capacitors. ............................................................... 283

Figure 11.5: After copper bottom plate electroplating ...................................................... 284

Figure 11.6: Cross-sectional view of the top of the silicon wall after anodization (a) 25 µm wide and (b) 20 µm wide in the bottom ........................................... 285

Figure 11.7: Cross-sectional view of the bottom of the trench with (a) 25 µm opening and (b) 30 µm opening ................................................................. 285

Figure 11.8: Cross-sectional view of the silicon walls with metal layers showing continuity from the top to the bottom. ................................................... 286

Figure 11.9: Bottom of a trench showing delamination of Nb$_2$O$_5$ from the bottom plate copper ................................................................. 287
Figure 11.10: (a) cracking and delamination of oxide and (b) delamination of the oxide from the copper at the trench corner. ................................................................. 288

Figure 11.11: (a) shows delamination on a single wall and (b) shows the same process in multiple walls. ................................................................................................. 288
List of Tables

Table 2.1: Properties of tantalum and niobium [3].................................................................. 15

Table 4.1: The material characteristics and the technologies used for characterization.. 35

Table 7.1: Recipe for TaN reactive ion etching in Plasma-Therm SLR 720 .................... 71

Table 7.2: Summary of the average capacitances of sputtered-anodized Ta$_2$O$_5$ capacitors
with TaN after fabrication and after each thermal excursion........................................... 77

Table 7.3: Comparison of capacitances and $k$ values of capacitors with and without TaN.
........................................................................................................................................ 78

Table 7.4: Anodization details of 6.1 mA Wafer and 0.51 mA Wafer. ......................... 80

Table 7.5: Ta$_2$O$_5$ capacitors anodized to a final current of 6.1 mA and 0.51 mA. .... 86

Table 7.6: Average capacitance and functional yield of boiled and unboiled wafers. .... 91

Table 8.1: Sputtering gas parameters for niobium, niobium oxide, and niobium nitride. 93

Table 8.2: Niobium deposition parameters and corresponding thicknesses measured with
Dektak Profilometer. ........................................................................................................ 94

Table 8.3: Sputtering times, average thicknesses, and the deposition rates of niobium,
sputtered at 2200 W and 5 mTorr pressure. ................................................................. 96

Table 8.4: Niobium oxide deposition parameters and corresponding thicknesses. .... 98

Table 8.5: Niobium oxide deposition parameters and corresponding thicknesses (revised
with TEM data). ............................................................................................................. 101

Table 8.6: Binding energies of Nb-O compounds. ......................................................... 103

Table 8.7: Nb-O compounds present in the reactively sputtered niobium oxide at 100 W.
................................................................................................................................. 104
Table 8.8: Nb-O compounds present in the reactively sputtered niobium oxide at 200 W.
.................................................................................................................................................. 109

Table 8.9: Nb-O compounds present in the reactively sputtered niobium oxide at 300 W.
.................................................................................................................................................. 113

Table 8.10: Nb-O compounds present in the reactively sputtered niobium oxide at 400 W.
.................................................................................................................................................. 115

Table 8.11: Nb-O compounds present in the reactively sputtered niobium oxide at 500 W.
.................................................................................................................................................. 117

Table 8.12: Nb-O compounds present on the surface and deep inside the film at different sputtering powers. ........................................................................................................................................ 118

Table 8.13: Niobium nitride deposition parameters and corresponding deposition rates.
.................................................................................................................................................. 139

Table 8.14: Binding energies of Nb-N compounds and Nb$_2$O$_5$ used in this section. ..... 141

Table 8.15: Nb 3d peak binding energies from NbN thin film reactively sputtered at 800 W and corresponding Nb compounds. ................................................................. 143

Table 8.16: Nb 3d peak binding energies from NbN thin film reactively sputtered at 800 W, and corresponding Nb compounds, after Ar$^+$ etching. ................................. 144

Table 8.17: Nb 3d peak binding energies from NbN thin film reactively sputtered at 1500 W, and corresponding Nb compounds. ................................................................. 145

Table 8.18: Nb 3d peak binding energies from NbN thin film reactively sputtered at 1500 W and corresponding Nb compounds, after Ar$^+$ etching. ................................. 146

Table 8.19: Nb 3d peak binding energies from NbN thin film reactively sputtered at 2000 W and corresponding Nb compounds. ................................................................. 147
Table 8.20: Nb 3d peak binding energies from NbN thin film reactively sputtered at 2000 W, and corresponding Nb compounds, after Ar⁺ etching. ........................................... 148

Table 8.21: Nb 3d peak binding energies from NbN thin film reactively sputtered at 2200 W and corresponding Nb compounds. ................................................................. 149

Table 8.22: Nb 3d peak binding energies from NbN thin film reactively sputtered at 2200 W and corresponding Nb compounds, after Ar⁺ etching. ........................................... 150

Table 8.23: Comparison of compounds present in the nitride films reactively sputtered under different powers. ......................................................................................................... 151

Table 8.24: Sputtering power versus Nb/N ratio. ............................................................................. 151

Table 9.1: Comparison of film properties and anodization profiles of low, room, and high temperature anodizations. ........................................................................................ 165

Table 9.2: Anodization parameters for the color chart of Niobium oxide films..................... 171

Table 9.3: The anodization times, thicknesses, and the colors of the wafers. ................. 173

Table 10.1: Sputtering parameters for the adhesion layer, bottom plate, diffusion barrier, and the dielectric layer. ..................................................................................... 189

Table 10.2: Table relating the wafer position, dielectric thickness, capacitance, and defect density. ........................................................................................................... 199

Table 10.3: Sputtering parameters and thicknesses of the reactively sputtered Nb₂O₅ and Nb anodized wafer. ............................................................................................. 201

Table 10.4: Thermal excursion steps and the hours the wafer spent in the furnace. ...... 205

Table 10.5: Capacitance in the as-deposited state and after 85°C in air for 169 hours. . 224

Table 10.6: The capacitance change from the as-deposited state to after thermal excursions at 85°C, 100°C, and 124°C.*After being in the oven for 75 hours and 25
minutes at 100°C, the wafer had to be transferred to a different oven at the same conditions. The time taken to transfer was monitored and was compensated in the new oven. ................................................................. 226

Table 10.7: Calculated Nb$_2$O$_5$ and NbON thicknesses for the measured capacitances. 226
Table 10.8: Three sets of wafers with their Nb$_2$O$_5$ and Nb thicknesses before anodization, and the dielectric thickness after anodization. ................................................................. 228
Table 10.9: Sputtering parameters and thicknesses of the (reactively sputtered Nb$_2$O$_5$ and Nb) anodized wafers. ................................................................. 229
Table 10.10: Capacitance adjustment factors used for measurements from the Impedance Analyzer. ................................................................. 234
Table 10.11: Data from the wafer with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates. .......... 235
Table 10.12: The average capacitance and functional yield from (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN after heat treatment. ................................................................. 236
Table 10.13: Data from the wafer with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates. .......... 237
Table 10.14: ESR and ESL of the measured capacitors and calculated values for a single capacitor. ................................................................. 239
Table 10.15: Comparison of data from the set #1 wafers with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates with and without NbN. ................................................................. 244
Table 10.16: ESR and ESL values of the measured capacitors and calculated values for a single capacitor on the wafer set #1 with NbN ................................................................. 246
Table 10.17: Comparison of data from set #1 wafers with and without NbN. ............. 249
Table 10.18: Data from the wafer with (reactively sputtered 904 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates........................... 252
Table 10.19: ESR and ESL of the measured capacitors and calculated values for a single capacitor .................................................................................................................. 254
Table 10.20: Comparison of data from set #2 wafer with NbN before and after heat treatment. ................................................................................................................ 256
Table 10.21: Average capacitance and functional yield from (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN.............................................. 257
Table 10.22: Comparison of capacitance data of set #3 wafers without NbN before and after heat treatment........................................................................................................ 259
Table 10.23: ESR and ESL of the measured capacitors and calculated values for a single capacitor .................................................................................................................. 259
Table 10.24: Data from the set #3 capacitor with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN before and after heat treatment.... 264
Table 10.25: Average capacitance and functional yield from set #3 wafer with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN ............. 265
Table 10.26: Average capacitance and functional yield comparison of set #3 wafer with NbN before and after heat treatment................................................................. 267
Table 10.27: Comparison of data from Wafer set #3 before and after heat treatment. .. 269
Table 10.28: Comparison of average capacitances of the three wafer sets before and after heat treatment ........................................................................................................ 270

Table 10.29: ESR and ESL of the three sets of wafers ........................................................................................................ 272

Table 10.30: Current at 5 V for capacitors with NbN and no NbN after heat treatment 272

Table 10.31: Comparison of functional yield of NbN and no NbN wafers before and after heat treatment ........................................................................................................ 277

Table 11.1: DRIE recipe for 80 degree tapered walled trenches on p-Si (100) ............. 281
Chapter 1: Introduction

Capacitors are major passive components present in electronic systems. Since passive components occupy a majority of the available space, it is important to reduce their size to allow room for more active circuitry, in order to make electronics smaller and faster. Integrated capacitors are attractive as they consume less space and have better electrical properties (lower parasitics) compared to their surface mount counterparts. These capacitors are mainly used for decoupling purposes in printed circuit boards or chip package substrates. When electronic systems are made smaller, better performance is also expected out of the smaller available area. Thus, the capacitance (capacitance/unit area) must be increased to meet this requirement. This can be achieved by using a thinner dielectric, which is possible only up to a certain degree due to tunneling currents at very low thickness levels. Another way is to use a material with high dielectric constant, ‘$k$’.

Tantalum pentoxide ($\text{Ta}_2\text{O}_5$) has been widely used in the electronics industry owing to its high $k$ ($k \sim 24$) and the ability to form thinner (<1 µm) films [1]. With $\text{Ta}_2\text{O}_5$, researchers have achieved high capacitance by building multilayered (dual and triple layers) structures, essentially, stacking one capacitor one on top of the other. The area efficiency achieved with this structure comes with a cost. These stacked capacitors involve ~2× film deposition steps compared to a single layer dielectric capacitor, and defects in one dielectric layer can affect the effective capacitance of the entire stack. Overall, this process is not very cost effective compared to fabricating a simple planar capacitor. Thus, there is a need for a dielectric material with higher $k$, which can deliver high capacitance with a simple planar geometry. The potential of niobium pentoxide
(Nb$_2$O$_5$) as a high-k material has been known since the 1960s [2]. Nb$_2$O$_5$ has a dielectric constant of 41 [3]. With 1.7 times the dielectric constant and about 30 to 100 times the abundance in nature relative to tantalum, niobium oxide is a very interesting candidate for future capacitors [4]. The availability of niobium in politically stable regions of the world offers stability in supply and price compared to tantalum, which is located in politically sensitive areas. For a given thickness, Nb$_2$O$_5$ can give $1.7 \times$ capacitance/area compared to a Ta$_2$O$_5$ dielectric in a parallel plate structure and is a proven dielectric for electrolytic type surface mount capacitors [5, 6]. This project investigates Nb$_2$O$_5$ as a high-$k$ material for thin film integrated capacitors and the challenges to achieve a stable capacitor.
Chapter 2: Background

An integrated passive device in simple terms is embedded in the substrate. An integrated capacitor may be defined as a capacitor that is built within the layers of the primary interconnect substrate or formed on the surface of another substrate which is eventually packaged and surface mounted onto the primary interconnect substrate. As of [1], integrated passives are of interest because they allow reduced system volume and footprint, improved electrical performance, increased design flexibility, improved reliability, and reduced unit cost. Discrete capacitors must overcome high equivalent series resistance (ESR) and equivalent series inductance (ESL) that limit high frequency performance. Therefore, they must be used in parallel to lower these parasitics. With integrated capacitors, low parasitic inductance and resistance can be achieved. Since they are embedded in the substrate, there is more room for other components on the board surface.

There has been much research done on integrated passives at the University of Arkansas. Integrated spiral inductors, resistors, and capacitors have been successfully fabricated at the university [7]. Volumetric efficiency, low leakage current, reliability, and very efficient noise filtering characteristics make tantalum capacitors perfect for high-k applications as of [8]. Approximately six theses and one dissertation have been done especially on tantalum oxide integrated capacitors; recent work on tantalum decoupling capacitors can be found in [9-12]. Dual layer and triple layer capacitors fabricated at University of Arkansas exhibit high capacitance densities, but multiple steps in fabrication make them complicated and expensive [13].
2.1 Decoupling Applications

An important use of integrated capacitors is power supply decoupling. The voltage ripple generated in a power distribution system (PDS) from the switching integrated circuits in a digital environment, across a capacitor (ideal), at a given current can be written as,

\[ I = C \frac{dV}{dt} \]  
Equation (1)

\[ \frac{dV}{dt} = \frac{I}{C} \]  
Equation (2)

\[ \Rightarrow V = \frac{I}{\omega C} \]  
Equation (3)

Where,

\( I \) — current
\( C \) — capacitance
\( dV \) — voltage ripple
\( dt \) — time
\( V \) — voltage
\( \omega \) — angular frequency \((\omega = 2\pi f); \ f \) — frequency

Therefore, for a given current and frequency, the ripple voltage decreases with an increase in capacitance. By adding a decoupling capacitor, the voltage ripple can be reduced by 75% as will be seen in the next pages. These decoupling capacitors, otherwise known as bypass capacitors, decouple an IC from the power source. Decoupling capacitors serve two purposes: they act as charge reservoirs to satisfy the transient power requirements of an IC and they bypass any high-frequency noise to the
ground, improving signal quality. Figure 2.1 shows a power bus decoupling capacitor for a printed circuit board without power planes [14]. Note that it is connected to the ground for bypassing noise.

Figure 2.1: Schematic of a decoupling capacitor on a printed circuit board [14].

Figure 2.2 shows the effect of decoupling capacitance on supply voltage noise [15].

Figure 2.2: Effect of decoupling/bypass capacitor on supply voltage noise in an electrical circuit [15].
For a voltage range of 4.95 V to 5.05 V, the blue line shows noisy voltage without a decoupling capacitor in the circuit and the pink line shows the voltage with a decoupling capacitor. It can be seen that ripples/voltage fluctuations in the voltage caused by electrical noise are reduced with a decoupling capacitor. The voltage range may seem small, but for low power applications involving digital logic gates ripples in the voltage cause undesired effects as the ripple current acts as a backflow in the circuit. For example, an AND gate will be shut down if the ripple current flows through it when it is in the stable state. Hence, “a good rule of thumb is to add one bypass capacitor for every integrated circuit on your board” [15].

Figure 2.3 shows ripple voltage and ripple current in a very narrow range [15], which shows the ripple voltage enlarged from Figure 2.2. Pink and blue lines have the same meaning as discussed above. It can be seen as a sinusoidal variation in voltage and current with no decoupling capacitor. Thus, these ripples created an AC component in the circuit, and by using a decoupling capacitor voltage fluctuations were reduced by 75%.

Figure 2.3: A closer look at ripple voltage and ripple current in a circuit with and without a decoupling capacitor [15].
By keeping the decoupling capacitor close to the IC, trace inductance can be reduced as the trace length gets shorter. Lowering trace inductance is important since the trace inductance introduces noise and ringing in voltage waveforms. Integrated decoupling capacitors have very low parasitic inductance compared to their discrete counterparts. Due to lower inductance, a single integrated capacitor can potentially replace multiple discrete capacitors that are connected in parallel to reduce inductance. Thus, the number of components is reduced, saving time and money. Though integrated passives have many advantages over discrete devices, they are more sensitive to yield issues. Hence, it is imperative that the new integrated capacitors are optimized for yield and reliability.

2.2 Niobium

Niobium is a transition metal that belongs to Group VB in the periodic table. It has an atomic weight of 92.9 a.m.u and carries the atomic number 41. This element exhibits three common oxidation states, +5, +4, and +2 in oxides. Initially mistaken for iron ore and locked up in the British Museum for 150 years, Niobium was discovered by Charles Hatchett in the year 1801. The mineral was called Columbium by Hatchett to honor its country of origin, Columbia (according to the reference, America was then called Columbia). A year later, tantalum was discovered, after which followed a confusion that both the elements were the same. Tantalum was given its name because of the difficulty in dissolving tantalum oxide, which symbolizes the torments of Tantalus. In 1844, Heinrich Rose clearly distinguished that Columbium and Tantalum were different and he renamed columbium as niobium. U.S and Britain retained the name Columbium until 1950, when the International Union of Pure and Applied Chemistry (IUPAC) accepted “niobium” as the official name of the element. However, even today, a search with the
key word, ‘columbium’ can bring up details of niobium. Writings about niobium are never complete without mentioning tantalum. Niobium was named after “Niobe,” who was the daughter of Tantalus in Greek mythology, due to the similarities of both elements and their geochemical coherence. Niobium deposits are found in Brazil, Canada, Africa, Norway, Australia, and the United States with major minerals being pyrochlore and columbite-tantalite. Niobium is also found in the tin mineral, cassiterite, and can be extracted by smelting [16].

2.2.1 Niobium Applications

Niobium has a broad spectrum of applications, ranging from thin films to the automotive industry. This refractory metal finds its main application in the steel industry, where it is added as a micro alloying element for grain refinements and such. Another important area is super alloys, which are Ni-, Fe-Ni, Co- based high performance alloys that can withstand temperatures greater than ~ 540°C (1000°F) [17]. An obvious application of super alloys is aircraft engine manufacturing. In nickel-based super alloys, niobium is mainly used as a precipitation strengthener and as a solid solution strengthener. Other inherent excellent material properties make niobium the best choice. For example, niobium and niobium alloys have high corrosion resistance and good high temperature properties, making them attractive for the aircraft industry. High temperature strength, creep resistance, toughness, cost, availability, and ease of processing put niobium in the first place for high temperature applications. Alloys of Nb-Zr and Nb-Hf-Ti are some of the high temperature materials. These high temperature alloys are used in missile and spacecraft propulsion systems. High critical temperature and ease of processing made NbTi and Nb3Sn compounds suitable for use as
superconductors. Niobium has also been investigated as a biomaterial for medical implants. Biocompatibility and elastic modulus, lower than the bone, which minimizes bone resorption, are the main driving forces for developing niobium-containing alloys for implant applications. This is because materials with elastic modulus higher than bone will potentially cause failure of arthroplasty. The shape memory effect of niobium alloys has also been studied as part of implant applications. It is also used as an adhesion promoter between stainless steel substrates and diamond-like-carbon (DLC) coatings; a common application of DLC is razor blades [18].

2.2.2 Oxides of Niobium

Figure 2.4 shows the niobium-oxygen phase diagram indicating different phases that form at different temperatures and oxygen concentrations [19].

![Niobium-Oxygen phase diagram](image)

**Figure 2.4:** Niobium-Oxygen phase diagram showing different phases for oxygen concentration from 0 to 80% [19].
The phase diagram indicates that three Nb-O phases exist, which are, niobium (II) oxide (NbO), niobium (IV) oxide (NbO\textsubscript{2}), and niobium (V) oxide (Nb\textsubscript{2}O\textsubscript{5}) and they contain 50, 66.7, and 71.4 atomic percent of oxygen respectively. Among these three compounds, Nb\textsubscript{2}O\textsubscript{5} is insulating, NbO\textsubscript{2} is semi-conductive, and NbO is conductive. Other than these phases, Nb\textsubscript{2}O\textsubscript{3}, Nb\textsubscript{12}O\textsubscript{29}, and Nb\textsubscript{11}O\textsubscript{27} are also reported [19].

2.2.3 *Niobium Pentoxide (Nb\textsubscript{2}O\textsubscript{5})*

Niobium pentoxide, with a chemical formula Nb\textsubscript{2}O\textsubscript{5}, has the chemical structure as shown in Figure 2.5. The structure forms a resultant dipole as indicated by the positive and negative signs on the side of the figure. The arrow indicates the direction of electric field.

![Figure 2.5: Chemical structure of niobium pentoxide (Nb\textsubscript{2}O\textsubscript{5}).](#)

2.2.4 *Nb\textsubscript{2}O\textsubscript{5} Applications*

Nb\textsubscript{2}O\textsubscript{5} is very attractive to jewelry makers, as different colors can be achieved by varying the oxide thickness. It is used as a barrier layer in Josephson junctions, which are formed by linking two superconductors with a thin insulating barrier. The high refractive index of Nb\textsubscript{2}O\textsubscript{5} allows this material to be used in antireflective coatings, which are usually a stack of thin films built in the order of low-refractive index/high-refractive index, and the sequence is repeated until the reflectance of the system is reduced to the desired amount. These coatings can be used to improve visual acuity by using them on
lenses and on computer screens for antireflection purposes. Antireflective coatings also find applications in museum displays, shop windows, etc. Another major use is as a dopant in ceramic capacitors with barium titanate dielectric. Niobium pentoxide is used to modify barium titanate by shifting the Curie temperature to lower temperatures. During modification, some of the titanium ions, which occupy the center of the crystal structure, are replaced with niobium ions. Nb$_2$O$_5$ is also used in lead relaxor dielectrics and piezoelectric sensors [4]. Due to the high dielectric constant, niobium pentoxide has been investigated as a dielectric material for capacitors. Use of Nb$_2$O$_5$ can yield high capacitance.

2.2.5 Nb$_2$O$_5$ Deposition Technologies

Niobium pentoxide can be formed in a number of ways. Some of them are explained below.

a. Plasma enhanced chemical vapor deposition (PECVD): Nb$_2$O$_5$ can be formed by PECVD using penta-ethoxy niobium, Nb(OC$_2$H$_5$)$_5$ as the precursor. Films can be deposited using the microwave or RF modes or a combination of microwave and RF known as dual-mode [20].

b. Spray pyrolysis: As the name implies, this deposition technique involves spraying the desired solution onto a preheated substrate; the pyrolysis of the solution will form thin solid films on the substrate. Patil et al. formed the solution, [NbO$_4$(CHOHCOO$^-$)$_2$]$^{5-}$ by fusing Nb$_2$O$_5$ powder with potassium pyrosulphate and dissolving the resulting product in tartaric acid. When this solution is sprayed on heated substrates, the following pyrolytic decomposition occurs to form Nb$_2$O$_5$ [21].

$$2\left[NbO_4\left(CHOHCOO^-ight)_2\right]^{5-} \rightarrow Nb_2O_5 + 4H_2O \uparrow + 8CO_2 \uparrow$$
c. Molecular Beam Epitaxy: MBE is a growth technique in which the material to be deposited is heated and forms a stream of atoms. This collimated beam impinges on the substrate in a line of sight fashion and grows layers with a structure based on the crystal structure of the substrate. This technique gives excellent process control over film thickness, stoichiometry, and uniformity, ensuring high quality films. In order to deposit Nb$_2$O$_5$, niobium is evaporated using an electron-beam gun and oxygen is introduced into the chamber as a collimated beam. Flux rates are varied to achieve different stoichiometries. Substrates can be chosen according to the desired crystal orientation of the film. Lithium niobate (LiNbO$_3$) may be used as a substrate for niobium pentoxide deposition [22].

d. Sol-gel process: In the sol-gel process, chemical precursors are dissolved in a liquid and sol is formed. The sol is then converted (by dehydration or chemical reaction) to form a gelatinous, polymerized network called ‘gel.’ Gel can be dried to form shapes such as fibers, lenses, etc. or spin coated, dipped, or sprayed onto a substrate. Using niobium ethoxide (Nb(OC$_2$H$_5$)$_5$) as the precursor, the coating solution can be prepared by polymerization. Initially, niobium ethoxide undergoes hydrolysis and the product, Nb(OH)$_5$ is condensed to form a Nb$_2$O$_5$ layer [23].

e. Plasma Immersion Ion Implantation (PIII): This process is also known as plasma source ion implantation. In this technique, the substrate is placed in a plasma and the oxygen ions in the plasma are accelerated onto the sample surface. By this technique, the structure and composition of the film and its interface to the substrate can be modified and good adhesion and structural density of films on non-planar substrates can be achieved. Using niobium’s high chemical affinity to oxygen, an oxygen plasma can be
used to convert evaporated niobium into niobium oxide. The process begins with an evaporated niobium substrate and is then treated in RF oxygen plasma for a certain period of time (minutes to hours). The sample was charged with voltage (~30 kV) in pulses on the order of a few microseconds [24].

f. Sputtering: Reactive magnetron sputtering has been used to prepare Nb$_2$O$_5$ films. This is achieved by sputtering a metallic target in an argon/oxygen atmosphere. Both RF and D.C magnetron sputtering have described in the literature [25—29].

g. Electron beam evaporation: Nb$_2$O$_5$ thin films can be deposited by electron beam evaporation by evaporating granular Nb$_2$O$_5$ in an oxygen atmosphere. Glancing angle deposition (GLAD) is used to deposit different microstructured thin films. In this technique, the angle of incident flux is modified to achieve various structures. One of the ways to change the angle is tilting the substrate. In this way, different microstructures can be achieved which are difficult to form with normal incidence deposition. The formed films are often called sculptured films [30].

h. Plasma oxidation: Deposited metal is subjected to oxidation in an Ar/O$_2$ atmosphere in the plasma. For Nb, evaporated niobium is oxidized in an RF plasma containing Ar/O$_2$. For plasma oxidation, both RF plasma and laser-pulsed plasma have been used [31, 32]. In the laser-pulsed oxidation technique, a pulsed CO$_2$ laser is employed in an oxygen atmosphere to activate oxidation at a metal surface to form Nb$_2$O$_5$ [31].

i. Metalorganic Chemical Vapor Deposition (MOCVD): This technique makes use of pyrolysis of organometallics to form thin film deposits on the substrates. Nb$_2$O$_5$ films can be formed by the pyrolysis of pentaethoxy niobium [PEN: Nb (OC$_2$H$_5$)$_5$] vapor along with reactive gas, O$_2$. After the substrate is heated to the deposition temperature
(200—500°C), PEN and O₂ reactive gas are introduced into the deposition chamber and Nb₂O₅ is formed [33].

**j. Pulsed laser deposition (PLD):** PLD is a promising technique for the deposition of compound materials. Thin films are deposited using laser ablation, where high energy laser pulses erode the material to be deposited, under ultra high vacuum. Eroded material condenses on the substrate. The major advantage is its ability to transfer the original stoichiometry from the target to the deposited film with little changes. For Nb₂O₅ thin film deposition, the ambient gas, O₃/O₂ is introduced into the deposition chamber and a 355 nm Nd: YAG laser is focused onto a rotating Nb₂O₅ target. Nb₂O₅ is deposited onto a heated substrate by laser ablation [34].

**k. Atomic Layer Epitaxy (ALE):** ALE is also known as atomic layer deposition (ALD). This thin film deposition technique uses pulses of gas forming one atomic layer at a time. In this process, the vaporized precursors are alternately introduced into the ALD chamber containing the substrate. Purging periods are included in between precursor introduction periods to remove reaction products. For a metal oxide deposition, precursor 1 will be the metal precursor; the substrate is exposed to the metal precursor for a period of time, followed by the first purging period. Then precursor 2, the oxygen precursor is introduced into the chamber, and the adsorbed metal on the substrate surface reacts with the oxygen to form metal oxide. This is followed by the second purging period. This cycle is repeated until the desired film thickness is reached; each cycle time lasts between 1 to 10 seconds. Due to the self-limited adsorption of the precursors onto the substrate surface, precise thickness control can be achieved. Total film thickness is determined by
the total number of deposition cycles. Nb$_2$O$_5$ can be grown using Nb(OC$_2$H$_5$)$_5$ and H$_2$O precursors and deposition temperatures 150—350°C [35].

1. Anodization: A simple technology to form Nb$_2$O$_5$ is by electrochemical oxidation, known as anodization. In an electrochemical cell, niobium metal is maintained as the anode and an inert electrode is used as the cathode, immersed in a suitable electrolyte. When voltage is applied across the anode and the cathode, the oxide grows on Nb, proportional to the applied voltage. Acid-based (phosphoric, sulfuric, oxalic, hydrofluoric etc.) or organic electrolytes can be used [36—41]. With a hydrofluoric acid-based anodization solution, Nb$_2$O$_5$ microcones can be produced [39].

Among the deposition technologies described, reactive sputtering and anodization are most suitable for capacitor manufacturing as they are economical compared with other techniques. Most of the above technologies are applied only at the research level.

2.2.6 Nb$_2$O$_5$ for Capacitors

In the early 2000s when tantalum availability decreased and the price went up to a 20 year high, niobium was proposed as an alternative material for capacitor applications. Ta and Nb belong to the same group, VB, with Nb placed above Ta in the periodic table. Their properties are compared in Table 2.1 [3].

Table 2.1: Properties of tantalum and niobium [3].

<table>
<thead>
<tr>
<th>Properties</th>
<th>Tantalum</th>
<th>Niobium</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atomic Number</td>
<td>73</td>
<td>41</td>
</tr>
<tr>
<td>Atomic Weight (a.m.u)</td>
<td>180.9</td>
<td>92.9</td>
</tr>
<tr>
<td>Specific Gravity(g/cm$^3$)</td>
<td>16.6</td>
<td>8.57</td>
</tr>
<tr>
<td>Melting Point(°C)</td>
<td>2996</td>
<td>2468</td>
</tr>
<tr>
<td>Dielectric Constant</td>
<td>24</td>
<td>41</td>
</tr>
<tr>
<td>Dielectric oxide</td>
<td>Ta$_2$O$_5$</td>
<td>Nb$_2$O$_5$</td>
</tr>
</tbody>
</table>
Since both tantalum and niobium belong to the same group, their properties are similar and Nb can be processed using the same technologies as Ta. Above all, high dielectric constant is the major motivation to adapt Nb$_2$O$_5$ technology.

Nb$_2$O$_5$ has been investigated as a dielectric in its purest form as well as in combination with other compounds. Electrical properties of reactively sputtered Nb$_2$O$_5$ capacitors were investigated by Goldstein and Leonhard, dating back to 1967. They summarized that the capacitance with Nb$_2$O$_5$ dielectric is largely affected by heat treatment and it is destructive to heat-treat the oxide to 200°C [26]. Nanolaminates with Nb$_2$O$_5$—Ta$_2$O$_5$, and Nb$_2$O$_5$—Al$_2$O$_3$ were developed using ALD to achieve high permittivity and low leakage dielectric systems [42]. Similarly, Nb$_2$O$_5$ with HfO$_2$/Al$_2$O$_3$ barrier layers were formed for RF bypass capacitor applications [43]. Nb$_2$O$_5$ and Ta$_2$O$_5$ mixtures were investigated for DRAM cell applications [44]. Also, thick film pure Nb$_2$O$_5$, calcined Nb$_2$O$_5$, and Nb$_2$O$_5$ mixed with glass binders were studied under different conditions of firing temperature, sintering time, etc. on electrical properties such as capacitance, dissipation factor, temperature coefficient of capacitance, etc. [45]. Anodized niobium, Nb$_2$O$_5$ has been produced in the form of electrolytic capacitors with a Nb anode or NbO anode [5, 46].

### 2.3 Niobium Capacitors – State of the Art

Currently available niobium capacitors are of the electrolytic type. Niobium electrolytic capacitor fabrication starts with niobium powder, which is first pressed or compacted into pellets around a Nb anode lead wire. Then, these pellets undergo ‘sintering,’ which essentially is a solid-state fusion bonding. During sintering, contact areas of powders melt to form a strong bond. It is done in vacuum and at high
temperatures, but below the melting point of the material. This bonding will give good mechanical strength and electrical conductivity. After sintering, these pellets are anodized to form the dielectric layer and a conductive polymer or MnO$_2$ is coated on the dielectric to form the cathode.

AVX Corporation introduced niobium capacitors under the name, OxiCap® in 2007 [47]. These capacitors find applications in the automotive sector and commercial sector (notebooks, LCD/PDP panels, etc.). They are rated for voltages up to 10 V [48]. OxiCap® capacitors are shown in Figure 2.6 [49].

![OxiCap® capacitors from AVX Corporation](image)

**Figure 2.6: OxiCap® capacitors from AVX Corporation [49].**

These discrete capacitors range from 4.7 µF to 1000 µF with a tolerance of ±20%. The leakage is specified at 2%CV and the maximum temperature rating is 125°C [48]. AVX Corporation is the biggest player in niobium capacitors, though VISHAY® introduced their niobium capacitor technology in 2001. EPCOS is another capacitor manufacturer who announced their niobium capacitors in 2001 [50].
2.4 Issues with Nb$_2$O$_5$—Defining the Problem

The high dielectric constant of niobium pentoxide (Nb$_2$O$_5$) makes it an attractive choice for miniaturization. In order to be useful for capacitor applications, the dielectric needs to be stable in the 85°C — 125°C temperature range. Niobium has higher oxygen solubility than tantalum and this results in three stable oxides of Nb, as opposed to just one in tantalum (insulating Ta$_2$O$_5$). Of the three niobium oxides (Nb$_2$O$_5$, NbO$_2$, and NbO), Nb$_2$O$_5$ is the desired dielectric because NbO$_2$ is semi-conductive and NbO is conductive [51]. The presence of these suboxides in Nb$_2$O$_5$ provides a conduction path in the dielectric, resulting in an inoperable device.

In a Nb-Nb$_2$O$_5$ structure (eg. anodically oxidized film), high oxygen solubility leads to oxygen diffusing from the oxide into the substrate [52]. This leaves the oxygen deficient portion of the oxide conductive, creating a large leakage current through the dielectric, and eventually causing failure of the capacitor. Oxygen diffusion happens at high temperatures ($\geq$ 100°C), so a capacitor may show good electrical properties at room temperature, but can fail at elevated temperatures. Therefore, in this work, the issue addressed is the poor thermal stability of Nb$_2$O$_5$ and the creation of a process to achieve stable electrical parameters with Nb$_2$O$_5$ dielectric.

Since Nb$_2$O$_5$ has been investigated thoroughly for electrolytic capacitor applications, this oxygen migration problem at high temperatures has been addressed. The solutions were:

a. Addition of oxygen: A Nb/Nb$_2$O$_5$ interface is thermodynamically instable due to the following reactions [36, 52];

$$2NbO_2 + Nb \rightarrow 5NbO_2 \quad \Delta G = -147kJ/mol$$
\[ \text{Nb}_2\text{O}_5 + 3\text{Nb} \rightarrow 5\text{NbO} \quad \Delta G = -231.09 \text{ kJ/mol} \]

The negative free energy change of the reaction indicates that these reactions are spontaneous and these reactions occur when Nb/Nb$_2$O$_5$ interface is present. As mentioned earlier, NbO$_2$ is semiconductive and NbO is conductive, which are detrimental to the electrical properties of capacitors. This interface (Nb/Nb$_2$O) can be modified by the addition of oxygen to niobium, forming NbO, where NbO makes the anode of the capacitor. Thus, the interface is thermodynamically stable NbO/Nb$_2$O$_5$. Niobium monoxide (NbO) was chosen as the substrate material for capacitors, owing to its conductive nature and the ability to form a continuous Nb$_2$O$_5$ dielectric film similar to anodic oxide on Nb. The thermodynamic driving force, \( \Delta G \) (free energy change) of oxygen migrating from Nb$_2$O$_5$ to Nb is found to be larger compared to Nb$_2$O$_5$ to NbO [52]. Also, kinetically, NbO as the anode reduces the oxygen concentration gradient across the electrode/dielectric interface, reducing the oxygen diffusion driving force from the oxide to the substrate. Also, due to the conductive nature of NbO, the dielectric constant of the assembly is not affected. NbO is less pyrophoric compared to Nb metal, making it more attractive to industry. Information on NbO capacitors by AVX Corp. can be found in [53]. Other investigations on NbO capacitors include [46, 51, 52].

**b. Addition of nitrogen:** Nitrogen was incorporated with a Nb substrate (doping, addition in the form of gas, etc.) to reduce the diffusion of oxygen into the substrate. This was shown to reduce DC leakage in capacitors, suggesting dielectric to anode interfacial stability [54]. However, the addition of nitrogen was found to decrease the dielectric constant of the oxide film. As a result, lower capacitance was obtained [46]. But, the effective diffusion barrier nature of nitrogen is more attractive.
The goal of this work was to fabricate thin film Nb2O5 capacitors with stable electrical parameters. In order to build thin film capacitors, two techniques were to be used to form the dielectric; anodization and reactive sputtering. In the case of an anodized dielectric, there was always the Nb-Nb2O5 interface, due to the presence of residual niobium. As mentioned earlier, the presence of niobium next to Nb2O5 results in oxygen diffusion from the dielectric to the metal. This diffusion process can be modeled using the equation below [55].

\[
\frac{C(x,t) - C_o}{C_s - C_o} = \left[1 - \text{erf} \left( \frac{x}{2\sqrt{Dt}} \right) \right]
\]

Equation (4)

\[
\frac{C(x,t) - C_o}{C_s - C_o} = \left[1 - \text{erf} (z) \right]
\]

Equation (5)

Where, \(C(x,t)\) — oxygen concentration at a distance ‘x’ from the interface at time \(t\)

\(C_o\) — initial oxygen concentration in niobium

\(C_s\) — oxygen concentration at the interface

\(x\) — distance from the interface

\(D\) — diffusion coefficient of oxygen \((D=D_o \cdot f(T))\)

\(t\) — time

\(\text{erf} (z)\) — error function, which can be calculated using the following polynomial approximation:

\[
erf (z)=1-(1+0.278393z+0.230389z^2+0.000972z^3+0.078108z^4)^{-1}
\]

Equation (6)

Since, \(C_o = 0\) at \(t = 0\), we can rewrite the Equations (4) and (5) as,

\[
\frac{C(x,t)}{C_s} = \left[1 - \text{erf} \left( \frac{x}{2\sqrt{Dt}} \right) \right]
\]

Equation (7)
\[
\frac{C(x,t)}{C_s} = [1 - erf(z)]
\]

Equation (8)

Assumptions used in this work:

A sharp interface between Nb and Nb\textsubscript{2}O\textsubscript{5} (no suboxides present at the interface)

At the interface, i.e., \( x = 0 \), \( C(x,t)/C_s = 1 \)

Since capacitors are normally rated at 125°C, the concentration variations from the interface into the bulk of the metal at these temperatures for different times were calculated using Equation (7).

The oxygen diffusion coefficient in the temperature range, 100°C — 150°C,

\[
D = 1.38 \times 10^{-2} \exp \left( \frac{-111530}{RT} \right) \text{cm}^2/\text{s}
\]

Equation (9)

Where,

R — Universal gas constant, 8.314 J/mol.K

T — Temperature, K

The error function was calculated using the polynomial approximation.

Diffusion profiles at 125°C for 1 hour, 10 hours, and 168 hours were plotted as relative oxygen concentration as a function of depth into the bulk of the metal in Figure 2.7.
Figure 2.7: Diffusion profiles of oxygen diffusion from Nb$_2$O$_5$ to Nb at 125°C at 1 hour, 10 hours, and 168 hours.

At 125°C, after 1 hour, oxygen diffuses and reaches ~20 nm into the film. In 10 hours and 168 hours (1 week), diffusion extends to 40 nm and 150 nm respectively. Therefore, even with the presence of 20 nm residual Nb, oxygen can diffuse completely into it if maintained at 125°C for 1 hour. Thus, it is imperative that no permeable interface be present in a capacitor. A schematic of the Nb-Nb$_2$O$_5$ interface is shown in Figure 2.8.

Figure 2.8: Nb—Nb$_2$O$_5$ interface at (a) $t = 0$ and (b) $t = 168$ hours at 125°C.
The figure shows the thickness reduction of Nb$_2$O$_5$ with time and diluted oxide between Nb$_2$O$_5$ and Nb. Similar models have been used to predict oxygen diffusion during baking at high temperatures [56].

### 2.5 The Solution/Approach Used in This Project

From examining the problem, it seems two issues can affect the reliability of Nb capacitors.

**a. Nb-Nb$_2$O$_5$ interface:** It is detrimental as oxygen diffusion takes place from the oxide to the metal.

**b. Presence of NbO, NbO$_2$ along with Nb$_2$O$_5$:** The presence of these lower valence oxides makes the film function less like a dielectric because of their conductive nature.

For the first issue, the obvious answer is to avoid the Nb-Nb$_2$O$_5$ interface. For a purely anodized dielectric, this is not possible, as it is difficult to deposit the exact amount of metal needed to be converted into oxide. As a result, for an anodized dielectric there is always the metal-oxide interface present. Therefore, another dielectric formation technology must be considered. Reactive sputtering is an alternative to anodization for thin film dielectric deposition. With this, Nb$_2$O$_5$ can be directly deposited onto the bottom plate of the capacitor to avoid an Nb-Nb$_2$O$_5$ interface.

For the second issue, there must be a way to form absolute Nb$_2$O$_5$, with no suboxides. But, it has been shown that reactive sputtering produces dielectrics with many defect sites in them [57]. Especially in the case of Nb that has high oxygen solubility, sputtering can result in a mixture of niobium oxides. This in turn is not good for the electrical properties due to the presence of conductive oxides. Thus, with reactive sputtering the interface can be avoided, but absolute Nb$_2$O$_5$ is difficult to produce. Rohit Raghuveer from the
University of Arkansas has been shown that a combination of reactive sputtering and anodization can give high functional yield, meaning very low defect density [57]. In this combination process, the dielectric is reactively sputtered and then the sputtered oxide is anodized to the sputtered thickness. In that way, any oxygen vacancies present in the dielectric after sputtering are filled during anodization.

Thus, in this project the dielectric will be formed by a dual process: reactive sputtering and anodization to eliminate the interface from anodization and create a complete Nb$_2$O$_5$ dielectric.

Transition metal nitrides are proven diffusion barriers (TiN, TaN etc.) [58]. Therefore, as a diffusion barrier, NbN will be reactively sputtered above and below the dielectric to prevent any oxygen diffusion from the dielectric to the adjacent metal layers. The ability of nitrogen to lower oxygen diffusion has already been shown [46, 54].
Chapter 3: Dielectric Formation — Technologies Used

In this project, two technologies were used for Nb₂O₅ formation; reactive sputtering and anodization. An overview of these technologies is given below.

3.1 Reactive Sputtering

Reactive sputtering is a combination of physical and chemical sputtering. Sputtering is done in the presence of reactive gases such as oxygen, nitrogen, or methane, to form compound thin films on the wafer. For this, a mixture of an inert and a reactive gas is used. During reactive sputtering, the atoms are sputtered off the target or the material to be deposited and react with the reactive gas to form the desired film on the substrate. The compounds formed include oxides, nitrides, carbides, etc. Oxides are produced using oxygen gas, nitrides are produced with nitrogen or NH₃, carbides are formed with methane, acetylene, or propane, and sulfides with hydrogen sulfide. Other than oxides and nitrides, oxynitrides and oxycarbides can also be deposited. Reactive sputtering is an attractive deposition technique because it is easy to form alloys, and a wide range of materials can be formed with a wide range of properties while having step coverage as compared to evaporation. This process is mainly used to deposit insulators such as SiO₂, Si₃N₄, Ta₂O₅, etc. A notable application is the deposition of wear resistant coatings like TiN, TiC, TiAlN, etc. on bearing gears and saw blades [59].

Figure 3.1 shows the schematic of a reactive sputtering system.
The system contains a metallic target, which is maintained at a high negative potential; the substrate is facing the target. When a gas mixture of reactive gases with inert gas is introduced, ionization takes place, creating a plasma or glow discharge. The argon ions accelerate to the metallic target and eject the target material. The desired compound is formed by the reaction between the ejected target material and the reactive gas. The compound material is then condensed on the substrate, placed on the anode. A magnet placed behind the target creates a magnetic field to concentrate electrons closer to the target surface, improving the sputter rate. If the reactive gas concentration is too low then the films will have only partially reacted compounds; if the reactive gas level is too high then the compound films will be formed on the target surface, both of which are undesirable. Thus, an optimum pressure must be maintained to obtain the desired stoichiometry compound on the substrate.
It is believed that at low gas pressures these reactions between the target material and the reactive gas take place at the substrate while the material is deposited. At high gas pressures the reactions take place at the cathode [59]. An RF Magnetron system is normally used for reactive sputtering. A major issue with reactive sputtering is ‘target poisoning,’ a process by which the compounds are formed on the target surface which lowers the deposition rate.

**Reactive sputtering in this project**

A DC magnetron sputtering system, the Varian XM-8, was used in this work for reactive sputtering. Two types of compound materials were sputtered for this project: oxide and nitride. For oxide sputtering, an Ar:O\textsubscript{2} mixture of the ratio 90:10 was used, and for nitride sputtering, an Ar:N\textsubscript{2} mixture of the ratio 75:25 was used. Note that both of these gases were premixed. Gas pressures of 10 mTorr and 5 mTorr were used respectively for oxide and nitride deposition. Some of the important considerations for reactive sputtering using the XM-8 were the following. First, the sputtering chamber was flushed with the gas mixture for a minimum of 1 minute prior to reactive sputtering. Second, since a DC magnetron was used, target poisoning was a major issue, therefore, it was important to do dummy sputtering about every 20 passes or so. Since there was no wafer cooling in the XM-8, sputtering was done for short periods of time, about 20 seconds, with a 2 minute wait before the next 20 seconds of sputtering. Each of these short sputtering periods was called a ‘pass.’

Dummy sputtering indicated that sputtering was performed on a SiO\textsubscript{2} wafer in argon plasma for at least 1 minute continuously removing any oxide/nitride film on the target.
Dummy sputtering was also done after completing reactive sputtering if the equipment was dedicated for sputtering pure metal.

### 3.2 Anodization

In simple words, anodization is the electrochemical oxidation of metals. Like iron forming rust, most metals tend to form a thin layer of oxide on the surface when exposed to air. These native oxides are porous and do not offer much protection to the metal. Anodization is a technique to form dense oxide on metal surfaces. Aluminum is the most commonly found anodized metal in the world and you may find anodized aluminum vessels in your kitchen. For dielectric formation, anodization is a simple and easy way to form oxides. The metals that can be anodized are known as valve metals. Some of the valve metals are aluminum, tantalum, zirconium, niobium, and titanium.

#### 3.2.1 Anodization Process

In the anodization process, a metal is placed in a suitable electrolyte as the anode and an oxide layer is formed with the passage of electricity. The thickness of the oxide layer can be controlled by controlling the applied voltage.

Anodization is carried out in an electrochemical cell consisting of an anode which is connected to the positive terminal of a power supply; a cathode, which is usually a stable metal, connected to the negative terminal of the power supply; and an electrolyte. The anode is the specimen that needs to be anodized. When the voltage is applied between the electrodes, the following half-cell reactions occur:

At the cathode,

\[ 10H_2O + 10e^- \rightarrow 10OH^- + 5H_2 \]
At the anode,

\[ Nb \rightarrow Nb^{5+} + 5e^- \]
\[ 2Nb^{5+} + 10OH^- \rightarrow Nb_2O_5 + 5H_2O \]

Once the initial film is formed, anodization continues through the transport of niobium cations and oxygen anions through the existing film under the electric field. \( Nb^{5+} \) ions migrate outward and \( OH^- \) ions migrate inward. Due to these motions, the oxide is grown at the metal/oxide interface as well as the oxide/electrolyte interface [40]. The film growth is approximately proportional to the formation voltage applied between the anode and cathode.

For this project, anodization was carried out in an organic–based electrolyte, which was a mixture of tartaric acid \([\text{L-}(+)-(\text{CHOH})_2(\text{CO}_2\text{H})_2]\), ethylene glycol, and deionized (DI) water. Ethylene glycol served the purpose of reduction of oxide blistering during anodization. The cathode was a platinized titanium mesh. The anodization setup is shown in Figure 3.2.

![Figure 3.2: Anodization setup at HiDEC; (a) setup and (b) anodization bath containing anode, cathode, and the electrolyte.](image-url)
The power supply used was Sorensen DCR600–1.5B; current was monitored using a NIDA Multimeter; and the voltage was monitored with a FLUKE multimeter. Anodization voltage is set according to the desired oxide thickness. For tantalum, the oxide growth rate is 16 Å/Volt and for Nb, the growth rate is 24 Å/Volt [3]. For example, in order to produce a 2000 Å thick Ta$_2$O$_5$ film, a voltage of 125 V must be used. In this project, a current density of 0.5 mA/cm$^2$ was used for all the anodizations.

Anodization can be carried out in a constant current mode (galvanostatic) or a constant voltage mode (potentiostatic) or a combination of both. In this project, all the anodizations were carried out in a combination of modes. For the combination of modes, the galvanostatic regime came first, and then the potentiostatic regime. Initially, constant current was maintained until the desired voltage is reached, and then the power supply switched to a constant voltage mode where the current reduced to 10% or 2% of the initial value. For our project, the anodization was terminated when the current reached 1 mA to allow for a complete oxide formation.

### 3.2.2 Anodization profile

The anodization profile shows the variation of anodization voltage or current or both with time. The profile along with the change in film thickness with time is shown in Figure 3.3 [60].
Anodization begins with zero voltage and the voltage increases linearly with time while the current stays constant. Once the set voltage is reached, the voltage stays constant for the rest of the process, and the process is potentiostatic. Most of the oxide growth takes place during the galvanostatic regime; the growth continues at a slower rate during the potentiostatic regime. Anodization profiles can give information on how well the oxide formation is proceeding. Any change in voltage during potentiostatic mode could be an indication of defect formation in the dielectric. Therefore, it is important to monitor the voltage and current variation with time during anodization closely. Figure 3.4 shows the anodization profiles of a metal and an oxide.
Figure 3.4: Anodization profiles of (a) tantalum metal and (b) reactively sputtered tantalum pentoxide.

Figure 3.4 (a) shows the Ta metal profile and (b) shows the reactively sputtered Ta$_2$O$_5$ profile. Both materials were anodized to 125 V at a current density of 0.5 mA/cm$^2$. The solid line corresponds to voltage change with respect to time and the dashed line represents the variation of current over time. Note that the time axis does not start from zero, but from 0.25 min (15 seconds). This is due to the fact that data acquisition was started at 15 seconds into the anodization. Note the time taken for each to reach the set voltage. The Ta metal reached the set voltage in ~8 minutes whereas the oxide took less than 30 seconds. This time indicated how close the initial sputtered oxide was to stoichiometric Ta$_2$O$_5$. Thus, anodization can be used as a test to get an approximate idea of how oxidized the initial ‘oxide’ is by monitoring the time to reach set voltage. The rate of increase of voltage, otherwise known as the voltage growth rate, is given by the slope of the slanted line during galvanostatic regime. For tantalum, it was calculated to be 0.21 V/second and for Nb it was 0.14 V/second.
3.2.3 Anodic Oxide Films and Electrolytes

Anodic films can be dense or porous depending on the electrolytes used. Anodization in acid solutions can result in porous oxides [61, 62]. In this case, metal dissolution takes place faster than the oxide formation. Also, phosphate, borate, and glycol based electrolytes show incorporation of anions from the electrolyte [63, 64, 65, 66]. The oxide film formed in an alkaline electrolyte (pH adjusted by the addition of NH₄OH) has been found to be composed of two layers, a nitrogen containing outer layer and a pure Nb₂O₅ inner layer [67]. Electrolytes used for Nb anodization include borate-based, phosphate-based, sulfate-based, oxalate-based, etc [36, 37, 38, 64]. Electrolytic concentration becomes important for anodization when the electrolytes enhance recrystallization in the anodic film. Recrystallization is the formation of crystalline oxide when held under anodizing voltages for extended periods. This is also known as field crystallization. The pH of the electrolyte is another important factor. The pH must be optimized to obtain desired films. For example, aluminum anodization in neutral films forms a barrier type insulating alumina, but when anodized in acid solutions, it forms porous alumina [68].

Agitation of the electrolyte is important when temperature control is needed and for current densities > 1 mA/cm². During anodization, a temperature rise occurs due to the passage of ionic current through the film. The rate of heat dissipation per unit volume of oxide can be given as, \( \frac{iV}{D} \) or \( Ei \).

\[
\frac{dH}{dT} \text{ per volume of oxide} = \frac{iV}{D} \quad \text{Equation (10)}
\]

\[
= Ei \quad \text{Equation (11)}
\]
Where,

\[ i \] — current density

\[ V \] — Anodization voltage

\[ D \] — Film thickness

\[ E \] — Electric field due to the applied voltage

This shows that for high electric field and current density the rate of heat dissipation is high. Therefore, it is important to provide agitation when high current densities are used [69].
Chapter 4: Material Characterization: Technologies Used

The initial step of any thin film process is to ensure that the desired material is obtained at the desired thickness. Thus, it is important to check the film deposition rate as well as the composition of the material. In this project, three materials, Nb, Nb$_2$O$_5$, and NbN were characterized for film thickness and composition. This chapter describes the technologies used for characterization. The three technologies used are shown in Table 4.1.

Table 4.1: The material characteristics and the technologies used for characterization.

<table>
<thead>
<tr>
<th>Film Characteristic</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thickness</td>
<td>Dektak Profilometer, TEM, AES</td>
</tr>
<tr>
<td>Composition</td>
<td>XPS, AES</td>
</tr>
<tr>
<td>Crystal Structure</td>
<td>TEM</td>
</tr>
</tbody>
</table>

Each technology is discussed below giving information on what it is, why it was used, and how it was used.

4.1 Dektak Profilometer

Profilometry is a technique commonly used to obtain topographical information of a sample. This technique uses a diamond tipped stylus to scan across the sample and gives surface variations as a function of position. Figure 4.1 is a schematic of stylus movement on an uneven surface.
Figure 4.1: Schematic of profilometer stylus scanning across a thin film surface.

The profilometer at HiDEC is capable of accurately analyzing films of thicknesses greater than 1000 Å. The instrument has a measurement error of ±5%. Profilometers with much smaller vertical resolution, as low as 5 Å, are also available in the market.

4.1.1 Reason for Usage

This instrument is a simple and fast technique to obtain film thickness information. Thus, in this project, it was used for film thicknesses greater than 2000 Å.

4.2 Transmission Electron Microscopy (TEM)

Transmission Electron Microscopy (TEM) is a powerful analytical technique that uses the interaction of electrons with the specimen to form images or spectra. The microscope consists of an electron source followed by a succession of electromagnetic lenses that are used either to control the beam parameters or to form an image or a diffraction pattern. The electrons are transmitted through the sample after having been scattered by atoms and/or having lost some of their energy. These transmitted electrons are collected by an acquisition system (CCD cameras, plates, spectrometers, etc.) giving direct information about the structure, elemental or chemical properties of the analyzed materials. In addition, the relaxation processes following the core-shell level excitation
by the electron beam are often accompanied by the emission of photons, the energy of which is characteristic of the elements present in the specimen. The analysis of the energy distribution of these photons can be conducted inside the TEM and is often referred to as Energy Dispersive Spectroscopy (EDS).

TEM analysis requires a thin specimen with a thickness not exceeding 300 nm for conventional analysis and well below 50 nm for high-resolution imaging (HREM). Sample preparation for TEM is a difficult and long process. There are two usual methods of preparing samples for TEM: mechanical milling followed by ion milling, and focused ion beam (FIB) cutting.

**Mechanical milling:** The samples are cut into thin slices (less than 0.5 mm) using a diamond saw and are mechanically polished to about 50 µm. They are dimpled at the center area to 10 µm. Finally, electron transparent areas are obtained using an ion miller with low-energy beam.

**Focused Ion Beam cutting:** A focused beam of Ga or Ar ions is used at normal incidence to etch material away defining a thin lamella. A single FIB or dual-beam SEM equipped with focused ion beam (FIB) can be used.

### 4.2.1 Reason for Usage

Owing to its high resolution, this technique is very useful for analyzing thin films. Thicknesses can be directly measured in the TEM images with much higher accuracy (due to Å level resolution) compared to other standard techniques (profilometry, AFM, XRD). The diffraction pattern from specific areas (i.e. layers, precipitates) can be obtained using a Selected Area Diffraction (SAD) aperture, providing structural information on the nanoscale.
4.2.2 Equipment used

A FEI Dual Beam SEM-FIB Nova Nano Lab 200 was used for sample preparation. It was equipped with an electron gun operating at an acceleration voltage of 200 V to 30 kV and a Ga$^+$ ion gun, which is operable from 5 to 30 kV. Ion currents ranged from 1 pA to 20 nA. Ion and electron beams were mounted at 52° to each other. For sample manipulation within the chamber, an Omniprobe micromanipulator, which carries a tungsten needle of tip diameter 50 to 300 nm was used. Another important part was the Gas Injection System (GIS), which consisted of a chemical crucible and a needle for injection. In the above mentioned system, platinum GIS was used to deposit platinum on the sample to protect it from ion damage during ion milling.

4.2.3 Sample Preparation

The samples were initially cut into 1 cm × 1 cm size for ease of placement on the sample stub.

1. The first step was to deposit a 150 nm film of gold on top of the sample surface in order to protect the film from ion beam damage. This ion damage refers to the damage from ion currents before and during above mentioned platinum deposition. 10 nm of chromium was used as the adhesion layer.

2. The sample was then loaded into the dual-beam chamber (pumped down to $10^{-5}$ Torr or less). The experiment began with electron beam imaging to bring the sample to eucentric height (operating parameters were optimum). Eucentric height is the ‘Z’ axis height at which the image movement is minimal for different specimen tilting angles.
3. A region of interest (ROI) was selected and the sample was tilted to $52^\circ$ to allow normal incidence of the ion beam. The relative positions of electron and ion guns before and after tilting are shown in Figure 4.2.

![Figure 4.2: Electron and ion gun positions (a) before and (b) after tilting the sample to $52^\circ$.](image)

4. The specimen preparation began with 1 μm thick platinum layer deposition in a rectangular area of 10 μm × 1.5 μm size. The purpose of platinum was to provide extra protection to the specimen from high ion beam damage during cutting.

5. Rectangular areas on either side of the platinum strip were then etched. The dimensions of both areas were 10 μm × 5 μm and the trenches were cut 5 μm deep into the specimen. A high ion beam current of 5 nA or above is usually used for cutting into the sample. The lamella in between the two trenches defined the TEM sample location.

6. Excess material was removed by using a lower beam current of 0.3 nA. Then, the faces of the sample were polished at 50 pA to obtain a clean cross-section. Figure 4.3 shows the status of the preparation up to this stage.
Figure 4.3: (a) shows the platinum strip and the trenches (b) a closer look at the specimen, the platinum strip, and the trenches with the excess material removed.

A sharp cross-section obtained after polishing gave an estimate of the thicknesses of different layers in the sample as shown in Figure 4.4.

Figure 4.4: A close-up view of the sample and the platinum strip showing the thickness of SiO₂ in this sample.
7. Once the sample was satisfactorily polished, it was then tilted to 7° to cut the TEM size specimen off the sample. The sides and the bottom were cut using the lower beam. The edges were cut in such a way that the sample was hanging from the top and free at the bottom [Refer to Figure 4.5 (c)].

8. The sample was then tilted back to 0° and the micromanipulator Omniprobe was inserted to pick up the specimen. The Omniprobe was directed to contact the specimen at the Pt strip, and a 500 nm thick platinum patch deposition was used to attach the specimen to the Omniprobe.

Figure 4.5 shows the steps from inserting the Omniprobe and the platinum GIS needle till the platinum patch deposition.

9. After the specimen was attached to the Omniprobe, the edges of the specimen were completely cut to release the specimen. Refer to Figure 4.6.

10. Once the specimen was released, the Omniprobe was brought to the TEM grid and the specimen was attached to the grid using another thin Pt patch. The patch connecting the probe to the specimen was then cut using the ion beam and the probe homed.

11. The final stage was the surface polishing of the specimen at 50 pA or below until transparency.

Referring to Figure 4.7 and Figure 4.8, after polishing, the sample was reduced from the initial 1.5 μm to 1000 Å or less in thickness. The TEM grid with the specimen was then placed in the TEM system and analyzed.
4.2.4 TEM Specifications

A FEI Titan™ 80-300 S/TEM fitted with an image Cs-aberration (spherical aberration) corrector (CEOS) was used for specimen analysis. It was equipped with a 300 keV field emission gun (FEG), a Fischione HAADF STEM detector, a Gatan 2k CCD camera and an EDAX energy dispersive spectrometer (EDS) for elemental analysis [70]. An information limit of 68 pm was routinely achieved.
Figure 4.6: (a) Omniprobe lifting the sample out and (b) sample attached to the Omniprobe with a 500 nm thick platinum patch.

Figure 4.7: (a) Omniprobe with the specimen at the TEM grid, (b) specimen close to the grid, (c) specimen touching the grid, and (d) After Omniprobe removal and polishing.
4.3 X-ray Photoelectron Spectroscopy (XPS)

XPS or Electron Spectroscopy for Chemical Analysis (ESCA) is a very useful tool for the analysis of thin films. This characterization technique is commonly used for elemental identification and to obtain chemical states of elements present in a sample. In this technique, the sample to be analyzed is placed in an ultra high vacuum chamber and a beam of X-rays is made incident on the sample surface. The electrons in the sample absorb energy from the incident X-rays and are ejected out of the sample; these electrons are called photoelectrons. For the electrons to escape from the sample, the incident X-ray should provide the electrons sufficient energy to overcome the energy barrier (work function), binding energy, and kinetic energy. Therefore, the X-ray energy, $hv$ can be given as,

Incident X-ray energy

$$= \text{Work function} + \text{Binding energy} + \text{Kinetic energy} \quad \text{Equation (12)}$$
\[ h\nu = q\phi + E_b + \frac{1}{2}mv^2 \]  

Equation (13)

Where,

- \( h \) – Planck’s constant, \( 6.62 \times 10^{-34} \) J.sec
- \( \nu \) – Frequency of the radiation, 1/sec
- \( q\phi \) – Work function
- \( E_b \) – Binding energy
- \( m \) – Mass of an electron
- \( v \) – Velocity of the photoelectron

Since the work function is a small number compared with the binding energy, the equation can be simplified as,

\[ \text{Incident X-ray energy} = \text{Binding energy} + \text{Kinetic energy} \]  

Equation (14)

Here the incident energy of X-rays is a known quantity, and by measuring the kinetic energy of the photoelectrons, binding energy can be calculated [71]. Binding energy will tell us what elements are present in the sample and the oxidation state of each element. Therefore each photoelectron is characteristic of an element. The major components of an XPS system are the following: an X-ray source, the sample, electron energy analyzer, electron detector, and a data processor and display unit. The X-ray source can be Mg or Al. The electron energy analyzer measures the kinetic energy of ejected electrons, whereas the electron detector counts the photoelectrons. The schematic of the setup is shown in Figure 4.9.
The output of XPS is a spectrum with binding energy in electronvolts (eV) on the X-axis and number of photoelectrons or intensity in counts per second (cps) on the Y-axis. XPS can be used for both quantitative and qualitative analysis. This technique can qualitatively identify the elements present in the sample from the peak binding energies in the spectra. Also, the concentration of each element can be calculated using the area under the peaks and elemental sensitivity factors.

For this project, a Kratos Axis 165 Photoelectron Spectrometer (Missouri University of Science and Technology) equipped with a Mg Kα X-ray source was used. A charge neutralizer, which is a stream of electrons, was used to compensate for photoelectrons and to keep the sample from becoming positively charged. The sample analysis area was 800 × 600 microns. For every sample, a survey spectrum was acquired initially with analyzer pass energy of 80 eV, and 20 eV was used for the window scan.

The spectra were obtained from the samples in the as-deposited state and after sputter cleaning. The samples were bombarded with Ar⁺ ions for 60 seconds and approximately
100 Å of the surface was etched. The sputter rate was determined with a Ta$_2$O$_5$ sample under identical sputtering conditions. Ion etching is one way to ensure a contaminant-free surface for composition analysis which is very important as the sample surface in the as-deposited state is usually contaminated with adventitious carbon (surface carbon). Also, XPS is a very surface sensitive technique and any kind of contamination can affect the spectra.

**Data Analysis Method**

XPS spectra were handled using XKRATOS software, provided by the Missouri S&T Surface Analysis Laboratory staff. Once the spectrum was obtained, the binding energy scale was calibrated by setting the C 1s peak at 284.6 eV. This took into account any charging effect or chemical shifts. Following this the peaks were deconvoluted and peak fitting was done. The Nb 3d spectrum gave a doublet depending on the spin orbital states $3/2$ and $5/2$ of the 3d electrons. Thus, each 3d peak was split into $3d_{3/2}$ and $3d_{5/2}$ peaks ($3/2$ and $5/2$ represent angular momentum quantum numbers). Peak fitting was made based on the fixed separation between the two peaks of Nb 3d orbital. Each peak binding energy was matched to the peak energies available at the National Institute of Standards and Technology (NIST) database and literature data. This gave the valence of each element present in the sample.

**4.4 Auger Electron Spectroscopy (AES)**

AES is another material characterization technique that uses electrons from the sample to obtain information about the sample, similar to XPS. Instead of photoelectrons in XPS, AES makes use of Auger electrons. These electrons are ejected as a result of the Auger effect. The Auger effect is a three-electron process in which an electron beam is
incident on a sample and a series of transitions takes place. If the incident beam has sufficient energy, then a core electron (#1) can be ejected and the atom is ionized. The core vacancy is filled by another electron (#2) from one of the outer shells. During this transition, this second electron loses some energy, corresponding to the energy difference between the transition shells. A third electron (#3), an outer shell electron, absorbs this energy and is emitted out of the sample. This third electron is called an Auger electron.

A schematic of the Auger process for KL\textsubscript{1}L\textsubscript{2} transition is shown in Figure 4.10.

![Energy level diagram for an Auger process. Steps 2, 3, and 4 are key steps in the process.](image)

Auger electrons are detected with an electron spectrometer and a plot is made between the number of Auger electrons and the electron kinetic energies. The peaks correspond to the intensity of Auger electrons from elements. “Auger electrons are characteristics of the target material and independent of the incident beam energy” [72].
The kinetic energy of an Auger electron can be calculated using the following equation [71].

\[
K.E_{\text{Auger}} = B.E_1 - B.E_2 - B.E_3 - U
\]  
Equation (15)

Where,

- \( K.E_{\text{Auger}} \) — Kinetic energy of Auger electron
- \( B.E_1 \) — Binding energy of the 1\textsuperscript{st} electron (ejected)
- \( B.E_2 \) — Binding energy of the 2\textsuperscript{nd} electron (transition)
- \( B.E_3 \) — Binding energy of the 3\textsuperscript{rd} electron (Auger)
- \( U \) — Hole-hole repulsion energy

A common Auger transition is KLL, in which the first electron is ejected from the K shell, whose vacancy is filled by a second electron from the L shell, and finally, the Auger electron is emitted from one of the L shells.

General uses of AES include elemental identification, quantitative elemental analysis, depth profiling by inert gas sputtering, and identification of chemical states of elements.

For this project, depth profiling of thin films with AES was obtained. A depth profile consists of elemental composition plotted as function of sample depth. Inert gas was used to erode the material away by sputtering and the Auger electrons were collected and analyzed.
Chapter 5: Electrical Characterization: Theory and Technologies Used

Three important properties were measured to characterize the capacitors; capacitance, impedance, and leakage current. Basics of each of these and the equipment used to measure them are given below.

5.1 Capacitance

In simple terms, a capacitor is a device capable of storing charge when a voltage is applied to it. The application of voltage leads to polarization of charges within the dielectric. The quantity of charge stored is directly proportional to the voltage applied across the capacitor plates, and the constant of proportionality is the capacitance. The relationship between charge, $Q$ (in Coulombs), capacitance, $C$ (in Farads), and voltage (in Volts) is shown below.

$$Q = CV$$  \hspace{1cm} \text{Equation (16)}

The capacitors are generally represented as a parallel plate structure with a dielectric sandwiched between two conductive plates. A schematic of a parallel plate capacitor is shown in Figure 5.1.

![Figure 5.1: Schematic of a parallel plate capacitor.](image)
The capacitance equation for the above shown parallel plate capacitor is given as,

\[ C = \frac{\varepsilon_r \varepsilon_o A}{d} \]  \hspace{1cm} \text{Equation (17)}

Where,

- \( C \) — capacitance in farads (F)
- \( \varepsilon_o \) — absolute permittivity of space, \( 8.85 \times 10^{-12} \text{ F/m} \)
- \( \varepsilon_r \) — relative permittivity or dielectric constant of material, also known as ‘k’, between the two plates
- \( A \) — area of the capacitor in \( \text{m}^2 \)
- \( d \) — the distance between top and bottom plates or thickness of dielectric in meter (m)

The equation shows that by changing \( \varepsilon_r, A, \) or \( d, \) or all of them, the capacitance value can be varied. ‘\( A \)’ and ‘\( d \)’ have reached the limit in today’s world due to miniaturization of electronics. Therefore, \( \varepsilon_r \) is the key factor to achieve high or low capacitance.

Two important properties of dielectric materials are dielectric strength and dielectric loss. Dielectric materials should have high dielectric strength, meaning they should be able to withstand high voltages without breakdown. Dielectric materials should have low dielectric loss or the loss of electrical energy in an alternating electric field.

The dielectric constant of a material gives the degree of polarization or charge displacement in a dielectric when a voltage is applied. The polarizability of the dielectric has four components as given below [73].

**a. Electronic polarizability:** Arises from the displacement of the negatively charged electron cloud relative to the positively charged nucleus.

**b. Ionic polarizability:** This kind of polarization is found in ionic crystals and is due to the relative displacements or the separation of anions and cations.
c. **Dipolar polarizability:** This is dominant in materials that contain permanent dipoles and the change in orientation of the dipole results in this kind of polarization.

d. **Space charge polarizability:** Found in materials that can have long range charge migration. This creates space charges and thus the polarization.

The above mentioned polarizations change over a range of frequency; meaning, some of them will occur or will not occur at high frequencies. For example, in the microwave range dipolar polarization does not occur as there is no time to orient the dipoles [73].

**Equipment used**

The capacitance was measured using the HiDEC Two Probe Robotic Micro Tester. This system was capable of making capacitance as well as resistance measurements. The capacitances were obtained using RC time constant. The capacitor was charged through a fixed resistor and the capacitance was calculated from the charging time. This tester made use of two probes, Probe 1 and Probe 2, in which the former was connected to the ground whereas the latter was connected to the device to be measured. For our capacitor design, one probe was connected to the bottom plate, through the contact pad, and the other probe moved from one top plate to the other taking measurements. The position of the stationary probe divided the wafer into two sections. When the probe, initially connected to the top plates, reached the axis of the bottom plate connected probe (stationary) the probes switched their positions. The stationary probe then became the moving top plate-connecting probe and vice versa. Since anodization forms polarized capacitors, the state at which the top plate is connected to ground (Probe 1) and the bottom plate is connected to positive bias (Probe 2) is referred as correct polarity in the rest of the discussions. The capacitance measured with the correct polarity was taken as
the true capacitance and the average of these true capacitances was referred to as true average capacitance.

5.2 Impedance

A capacitor can be modeled as a series combination of inductance (L), capacitance (C), and resistance (R) as shown in Figure 5.2.

![Figure 5.2: Capacitor and its parasitic components modeled as a series R, L, C circuit.](image)

The inductance and resistance in the model are called equivalent series inductance (ESL) and equivalent series resistance (ESR). ESR mainly comes from the top and bottom plate materials of the capacitor. The capacitor plate and lead resistances, termination losses, or dissipation in the dielectric are treated together as a single resistor with resistance ESR [74]. The ESL results from the plate geometry. The total ESL in a circuit is defined by the connection geometry (in effect, the current path). A good capacitor will have very small inductance and resistance compared to its capacitance. The resistance offered by these components to the current flow in an AC circuit is called impedance and the unit is Ohm. The opposition offered by the inductor is called inductive reactance, $X_L$. The equation to calculate $X_L$ is given in Equation (18).

$$X_L = 2\pi f L$$

Equation (18)

Where,
$f$ — frequency of the applied voltage in hertz (Hz)

$L$ — inductance in henry (H)

The opposition offered by the capacitor is called capacitive reactance, $X_C$. The equation for $X_C$ is given in Equation (19).

$$X_C = \frac{1}{2\pi fC} \quad \text{Equation (19)}$$

The final component opposing the current flow is resistance, $R$. The collective opposition to the current flow, impedance, $Z$ relating, $X_L$, $X_C$, and $R$ is shown in Equation (20).

$$|Z| = \sqrt{R^2 + (X_L - X_C)^2} \quad \text{Equation (20)}$$

**Why is impedance important for capacitors?**

Impedance data is very important for capacitors as the components constituting impedance vary with the applied signal frequency. Therefore, impedance plots must be studied for the frequency range over which the capacitor is intended to be used. The change of each component with frequency is given below.

$X_C$: From Eqn. 19, $X_C \propto \frac{1}{f}$ Therefore, at low frequencies, $X_C$ dominates.

$X_L$: From Eqn. 18, $X_L \propto f$ As frequency increases, $X_L$ increases.

Therefore, if a capacitor is built with minimum inductance, above a certain frequency the capacitor will act as an inductor because $X_L$ takes over $X_C$.

There is a frequency region where $X_L$ and $X_C$ cancel and the capacitor will act as a resistor. The frequency at which $X_L$ becomes equal to $X_C$ is called the resonant frequency and at this state the device is said to be in self-resonance.
Thus, the capacitor must be designed in such a way that it acts as a capacitor at all frequencies of interest. An impedance versus frequency plot demonstrates if the capacitor is suitable for the desired frequency range.

**Impedance versus frequency plot**

Figure 5.3 shows the impedance and frequency of a typical capacitor plotted on a logarithmic scale.

![Impedance versus Frequency Plot](image)

**Figure 5.3: Impedance versus Frequency of an ideal capacitor [74].**

The horizontal axis is log frequency and the vertical axis is log impedance. In the frequency region to the left of the center dip, the capacitor acts as a capacitor. For the frequencies to the right of resonance, $X_L$ dominates and the capacitor will act as an inductor as shown in the figure. The ‘dip’ is the self-resonant point where the impedance becomes zero if there is no resistance in the device, which is an ideal situation.

Figure 5.4 shows the impedance plot of a practical capacitor [74]. Instead of the dip, there is a flat region because of the device resistance.
The impedance data consists of impedance magnitude and impedance phase. The magnitude of impedance is calculated using Equation (20). The phase angle ($\theta$) can be calculated using:

$$\tan \theta = \frac{X_L - X_C}{R} \quad \text{Equation (21)}$$

$$\theta = \tan^{-1} \left( \frac{X_L - X_C}{R} \right) \quad \text{Equation (22)}$$

The relationships between $X_L$, $X_C$, and $R$ are shown in Figure 5.5.
The phase implies that the major contribution for impedance comes from capacitive, inductive or resistive components. When the phase angle is $-90^\circ$, the circuit is purely capacitive; for the phase angle $90^\circ$, the circuit is purely inductive. If the phase angle is zero, the circuit is purely resistive. In the first case for the pure capacitive circuit, if an inductor is added then the phase angle will start to become more and more positive with increasing inductance. Similarly, for the pure inductive circuit if capacitance is added the phase angle will decrease with an increase in capacitance.

**Equipment used**

Impedance measurements were done using an HP 4291A RF Impedance/Material Analyzer over a frequency range of 1 MHz to 1.8 GHz. This equipment measured impedance by applying a stimulus signal to the capacitor and measuring the complex voltage and complex current. Impedance was derived from this and an equivalent circuit was modeled, from which, $R$, $L$, and $C$ parameters were calculated.
5.3 Leakage Current

For an ideal capacitor, once the capacitor is charged to a DC voltage, no current should flow through it. In real capacitors, a small current will flow when subjected to a DC voltage. This current flowing through the capacitor under DC bias is called direct current leakage (DCL). Leakage current in a capacitor is taken as a measure of its quality. Leakage currents typically increase with an increase in applied voltage and temperature. These currents are mainly attributed to the imperfections of the dielectric, such as impurity centers and any mechanical damage of the film. Different mechanisms contribute to the leakage current and they are discussed in Chapter 10.

Equipment Used

An HP 4140B pA Meter/DC Voltage Source was used for the capacitor leakage current measurements. Leakage currents were measured by applying DC voltages from 0.1 V to 12 V. The voltage was incremented by 0.5 V from 0.5 – 12 V range. All the measurements were made at room temperature. The maximum current range for the equipment was $10^{-2}$ A.
Chapter 6: Test Vehicle — Structure and Layout

Thin film tantalum and niobium capacitors were designed and fabricated in a single layer parallel plate structure. This structure used a common bottom plate and dielectric, with individual top plates defining multiple capacitors. This design was adopted because it allowed use of the Two-Probe Test system for the capacitance measurements. The test vehicle used was a metal/insulator/metal (MIM) structure and was designed at the High Density Electronics Center (HiDEC) at the University of Arkansas, Fayetteville. 125 mm diameter silicon wafers were used as the substrate for all the experiments in this dissertation. The test structure and the mask layouts are discussed below.

6.1 Test Structure

The test structure consisted of 1mm × 1mm capacitors laid out on a 125 mm diameter wafer outline. A total of 4410 capacitors were designed in a matrix of 63 rows and 70 columns.

6.2 Masks

Two masks were needed to fabricate the above described capacitors; one for etching and one for plating. The Etching mask defined the initial capacitor area and was a clear field mask. The Plating mask was a dark field mask for the final Ni/Au contacts. The masks were designed by Dr. Len Schaper and were laid out by Michael Glover at HiDEC. Since there were no small (<100 µm) features, it was not necessary to order glass masks for this project. These masks were made as photoplots on high-resolution transparencies by Advance Reproductions Corporation. Figure 6.1 shows the mask for etching (Etching mask) and the dark field image of the same design was used for plating.
(Plating mask). In the Plating mask, only the squares and the top area (above the line) were clear field and everywhere else was dark field so that plating took place only in the clear areas when a positive photoresist was used. The top area on the mask was designed as a bottom plate contact pad for capacitor testing.

Figure 6.1: Mask for top plate etching in tantalum capacitor fabrication.
Chapter 7: Tantalum Capacitors

This chapter discusses the studies done on capacitors with Ta$_2$O$_5$ dielectric. These included;

1. The effect of tantalum nitride (TaN) on capacitance and the functional yield of Ta$_2$O$_5$ integrated capacitors,
2. The effect of change in anodization end point on thickness (capacitance), and
3. The effect of boiling the dielectric on capacitor functional yield.

Each of these is explained below.

7.1 Effect of TaN on capacitance and the functional yield of Ta$_2$O$_5$ integrated capacitors

TaN was primarily tested for its effect on capacitance and its ability to prevent oxygen diffusion in the temperature range 100 – 150°C in capacitors with tantalum pentoxide (Ta$_2$O$_5$) dielectric. Two sets of capacitors were processed, with and without TaN, and the devices were tested for functional yield. Also, the capacitors with TaN were subjected to thermal excursions and testing was done to compare the before and after capacitances. Since Ta$_2$O$_5$ is more stable than Nb$_2$O$_5$, this is a good test to determine the effect of the presence of nitride along with the dielectric [46].

7.1.1 Capacitor Structure

A 2000 Å sputtered-anodized Ta$_2$O$_5$ dielectric was used in this project. A 2 µm sputtered copper layer was used as the top plate as well as the bottom plate. In order to avoid oxidation of copper when exposed to atmosphere, 2 µm of plated nickel/gold (Ni/Au) was used as the top contact of the capacitors. For capacitors with a TaN
diffusion barrier, a 500 Å reactively sputtered TaN layer was used above and below the dielectric.

### 7.1.2 Fabrication Equipment

All the experiments were carried out in HiDEC at the University of Arkansas, Fayetteville. Major equipment for the capacitor fabrication included: Varian XM-8 for sputtering, Anodization setup, SUSS MicroTec MA-150 for photolithography and Plasma-Therm SLR 720 for reactive ion etching.

### 7.1.3 Fabrication Procedure

**Capacitors without TaN**

Step 1: A 2 µm thick thermal oxide was grown on the silicon wafer to act as an isolation layer between silicon and the capacitors. The oxidation was carried out in a Bruce BDF-4 tube furnace at 1100°C for 12 hours in the presence of steam (wet oxidation). Refer to Figure 7.1. Please note that none of the figures in this section are to scale and they only serve the purpose of schematics.

![Figure 7.1: Thermally oxidized silicon substrate.](image)

Step 2: Prior to film deposition the oxidized wafer was subjected to back sputtering, also known as RF etching, to remove any contaminants on the wafer surface and to roughen the surface to improve adhesion of films onto the oxide. Following RF etching, a 500 Å titanium (Ti) thin film and a 2 µm copper (Cu) film were deposited in this order. The
copper film formed the bottom plate of the capacitor and the Ti layer acted as an adhesion layer between the oxide and copper. Refer to Figure 7.2.

![Diagram of Copper, Titanium, SiO₂, and Silicon layers]

**Figure 7.2:** Copper bottom plate and titanium adhesion layer sputter deposited on oxidized silicon.

Step 3: A 2000 Å Ta₂O₅ layer was reactively sputtered on the copper bottom plate. The oxide was reactively sputtered in an Ar/O₂ atmosphere with the ratio of Ar:O₂ = 90:10. Refer to Figure 7.3.

![Diagram of Ta₂O₅, Copper, Titanium, SiO₂, and Silicon layers]

**Figure 7.3:** Ta₂O₅ reactively sputtered on copper bottom plate.

Step 4: The reactively sputtered Ta₂O₅ was anodized in the bath consisting of ethylene glycol, tartaric acid, and DI water using a platinized titanium electrolyte. The anodization setup and the parameters are explained in Chapter 3. The anodization was carried out at 125 V and 61 mA. The voltage was calculated based on the growth rate of
16 Å/V and the current density used was 0.5 mA/cm². For a 125 mm diameter wafer, the total surface area is 122 cm², giving a current of 61 mA. After anodization, the dielectric was scratched on the top of the wafer, opposite to the primary flat, and close to the edge of the wafer to make contact to the bottom plate when the top plate is sputtered. Refer to Figure 7.4.

![Diagram of anodized dielectric and exposed bottom plate for contact.](image)

**Figure 7.4: Anodized dielectric and exposed bottom plate for contact.**

Step 5: A 2 µm copper layer was sputtered as the capacitor top plate. Refer to Figure 7.5.

![Diagram of copper top plate sputter deposited on Ta₂O₅ dielectric.](image)

**Figure 7.5: Copper top plate sputter deposited on Ta₂O₅ dielectric.**

Step 6: The deposited copper was patterned photolithographically to define the top plates of the capacitors. AZ4330, a positive photoresist, was dispensed and was spun on to form
a 3.75 µm thick resist on the wafer. The thickness was chosen to be thicker than the combined thickness of 3 µm nickel and gold plating performed in Step 7. The photoresist was then hard baked at 110°C to remove the remaining solvents in the resist and to alleviate the residual stresses in the film. The hard baked photoresist was then exposed in the SUSS MicroTec MA-150 through the plating mask and developed in AZ400 K developer. Refer to Figure 7.6.

![Layer Diagram](image)

**Figure 7.6: Photoresist patterning with plating mask for Ni/Au plating.**

Step 7: After the photoresist was patterned, the wafer was moved to the plating station to form Ni/Au plating contacts. 2 µm of nickel was plated first, followed by nickel strike, and 1 µm gold. Refer to Figure 7.7.
Figure 7.7: Ni/Au plating for capacitor top plate contacts.

Step 8: Following Ni/Au plating, the photoresist was removed by using acetone and then by an AZ300T hot resist strip bath. Once the photoresist was removed, photolithography was done using a 2.5 µm thick AZ4110 photoresist and etching mask. The photoresist was patterned as described above. Refer to Figure 7.8.

Figure 7.8: Photoresist stripped after Ni/Au plating and new photoresist patterned for copper etching.

Step 9: After patterning, the top plate copper was etched away by wet etching. The copper etchant contained 5 parts acetic acid, 5 parts nitric acid, 2 parts sulfuric acid, and
10 parts of DI water. After inspection under the microscope, the photoresist was stripped off with acetone and AZ300T. The final structure is shown in Figure 7.9.

![Figure 7.9: Capacitor structure with Ta$_2$O$_5$ dielectric and copper top and bottom plates with Ni/Au contacts.](image)

**Capacitors with TaN**

For the fabrication of capacitors with a TaN diffusion barrier, Steps 1 and 2 from the “no TaN process” were repeated.

Step 3: Following bottom plate sputtering, 500 Å thick TaN was reactively sputtered using Ar/N$_2$ in the ratio of Ar:N$_2$ = 75:25. Refer to Figure 7.10. As before, these figures are schematics and none of them are drawn to scale.

![Figure 7.10: TaN sputter deposited on copper bottom plate.](image)
Step 4: A 2000 Å thick Ta₂O₅ was reactively sputtered and anodized as in the previous case. A purple colored dielectric was obtained after anodization. The capacitor structure up to this step is shown in Figure 7.11.

![Diagram showing the capacitor structure](image)

**Figure 7.11: Reactively sputtered and anodized Ta₂O₅ on TaN diffusion barrier.**

The anodization profile of Ta₂O₅ at 61 mA and 125 V is shown in Figure 7.12.

![Graph showing anodization profile](image)

**Figure 7.12: The anodization profile of a 2000 Å Ta₂O₅ on an entire 125 mm wafer anodized at 61 mA and 125 V.**
The profile shows the variation of current and voltage with time during anodization. As explained in Chapter 3, the voltage increases initially to the set point and stays constant at that value. While the voltage is constant, current falls rapidly, reaching values close to zero. Data were taken every 15 seconds. Here, voltage increased from 0 V to 125 V in 30 seconds at a rate of 4.2 V/second. This short time to reach the set voltage suggested that the reactive sputtering created an almost perfect dielectric with few oxygen vacancies. After the voltage reached 125 V, the current fell to 0.98 mA in 4 minutes and 15 seconds. Thus, the total anodization time was 4 minutes and 45 seconds for a final current of 0.98 mA. Once again, this was a short time compared with the anodization time for pure tantalum for the same anodization parameters. Tantalum and Ta$_2$O$_5$ anodization profiles are compared in Chapter 3.

Once the anodization was completed, the top area of the wafer was scratched to expose part of the bottom plate to form a contact pad using subsequent metal deposition.

Step 5: Another layer of 500 Å TaN was reactively sputtered on top of the dielectric as shown in Figure 7.13. A shadow mask was used during sputtering to cover the exposed copper for the bottom plate contact.

![Figure 7.13: TaN reactively sputtered on reactively sputtered-anodized Ta$_2$O$_5$ dielectric, forming a sandwich structure.](image-url)
Step 6: Top plate, 2 µm copper was deposited and was patterned using the plating mask for Ni/Au plating contacts as shown in Figure 7.14.

![Figure 7.14: Copper top plate sputtered and patterned for Ni/Au plating.](image)

Step 7: 2 µm nickel and 1 µm gold layers were plated with nickel strike in between for improved adhesion. Photoresist was stripped with acetone and AZ300T hot resist strip bath. Refer to Figure 7.15.

![Figure 7.15: Capacitor structure after Ni/Au plating (a) before photoresist removal and (b) after removal.](image)
Step 8: Another step of patterning was done with the etching mask. The top plate copper was wet etched as described above.

TaN was removed by reactive ion etching (RIE). In this process, the reactive species in plasma react with the material to be removed and form volatile complexes that are removed from the chamber by the vacuum system. Since these species are accelerated towards the wafer surface, etching is anisotropic. The recipe used for TaN etching is shown in Table 7.1. SF$_6$ dissociates in the presence of RF field and forms reactive fluoride ions. In oxygen-halogen plasma, the reaction products are metal oxyhalides, in our case, tantalum oxyfluorides [75].

**Table 7.1: Recipe for TaN reactive ion etching in Plasma-Therm SLR 720.**

<table>
<thead>
<tr>
<th>Pressure</th>
<th>200 mTorr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gases</td>
<td>SF$_6$</td>
</tr>
<tr>
<td></td>
<td>O$_2$</td>
</tr>
<tr>
<td>Power</td>
<td>100 W</td>
</tr>
</tbody>
</table>

The photoresist was stripped following RIE to obtain the final structure shown in Figure 7.16.

![Capacitor structure with TaN diffusion barrier sandwiching the Ta$_2$O$_5$ dielectric.](image)

Figure 7.16: Capacitor structure with TaN diffusion barrier sandwiching the Ta$_2$O$_5$ dielectric.
7.1.4 Results and Discussion

The capacitors were tested with a Two Probe Robotic Micro Tester and the results are given below.

**Capacitors without TaN**

Figure 7.17 shows the capacitance data of the sputtered-anodized capacitors with no TaN.

Figure 7.17: Sputtered-anodized Ta$_2$O$_5$ capacitors without TaN diffusion barrier in the as-deposited state.

There are three axes for this surface plot. The vertical axis represents the capacitance in nF, while the horizontal and the depth axes give the position of each capacitor on the wafer. Numbers (columns) and letters (rows) are used for capacitor positions and the plot is slightly tilted for a better view. Please refer to the mask image in Chapter 6 for a clear image of the capacitor layout. The spikes pointing down indicate shorted/defective
capacitors. There were a total of 25 defective capacitors, which gave a functional yield of 99.4%. The equation used for functional yield is given in Equation (23).

\[
Yield = \frac{\text{No. of good Capacitors}}{\text{Total no. of Capacitors}} \times 100 \quad \text{Equation (23)}
\]

The step seen in the plot is a result of the probes switching over while doing measurements. Since each probe is connected to either a ground or positive voltage source, when the probes switch over, the voltage polarity applied to the two plates also changes. This results in the change in measured capacitance. The change occurred after the 18\textsuperscript{th} row of capacitors. The average capacitance up to 18 rows was 1.13 nF and the rest was 1.07 nF. The difference between these averages was 0.06 nF. This difference in measured capacitance was due to the fact that these capacitors are polarized. This is because, during anodization, the dipoles orient themselves in the direction of the applied electric field. The changing voltage polarity applied to the top and bottom plates either aid or oppose the built-in polarity of the capacitor. When opposite polarity is applied to the plates of a polarized capacitor, the dipoles (refer to Section 2.2.3 in Chapter 2) reorient themselves in the direction of applied field and lead to a change in dielectric thickness (like a junction capacitor) and/or change in the distance between the dipoles leading to change in dielectric constant of the material. These two contribute the change in capacitance with changed polarity.

Once again, the average of the capacitances measured to the left side of the step will be referred to as true average capacitance, since the measurements were done with the correct polarity applied to the plates.

The dielectric constant was calculated from the capacitance and a dielectric thickness of 2000 Å using Equation (17).
Since the etching mask was 50 µm bigger than the plating mask, the final capacitor had an area of 1.05 mm × 1.05 mm. Also, the capacitance of 1.13 nF was used for the calculation as it represents the proper voltage application to the capacitor plates. Using, \( \varepsilon_0 = 8.85 \times 10^{-12} \) F/m, \( A = 1.05 \text{ mm} \times 1.05 \text{ mm} \), and \( d = 2000 \) Å, \( k \) was calculated to be \( \sim 23 \). This value agrees well with the literature value of \( k_{\text{Ta}_2\text{O}_5} = 24 \) [1].

The raised edge on the top right side of the plot showed a continuous increase in capacitance from \( \sim 1.1 \) to 1.5 nF. These capacitors were located close to the edge, situated next to the numbers. The overplating of the numbers led to connection with the capacitor top plates. This increased the top plate area and thereby, the measured capacitance was 9 to 36% larger than the other capacitors.

**Capacitors with TaN**

Figure 7.18 shows the capacitance data of the capacitors with TaN.

![Figure 7.18: Sputtered-anodized Ta$_2$O$_5$ capacitors with TaN diffusion barrier in the as-deposited state.](image.png)
There were a total of 4 shorts and the functional yield over the entire wafer was calculated to be 99.91%. There was a raised spot on the top right hand corner of the plot, which showed a capacitance of 1.21 nF. This observation was similar to the previous wafer and was explained by the edge effect, which resulted in a 12% higher capacitance compared to other capacitors.

The average capacitance up to 18 rows was 1.14 nF. The average of the remaining capacitors was 1.08 nF. These average capacitances are very close; a difference of 0.06 nF. So, the capacitors measured with one polarity gave a 5.6% higher capacitance than with the reverse polarity. This was due to the polarized nature of the capacitors as explained earlier. The dielectric constant was calculated from the 1.14 nF capacitance and an assumed 2000 Å dielectric thickness. Like earlier, a capacitance value of 1.14 nF (correct polarity) and an area of 1.05 mm × 1.05 mm were used. The $k$ was calculated to be 23.4, close to the literature value of 24. Thus, the presence of TaN did not affect the dielectric constant, in other words, the capacitance.

7.1.5 Reliability Testing: High Temperature Storage

In order to check the thermal stability of the capacitors with TaN, temperature annealing was performed in two steps. First, the capacitors were stored at 100°C for 168 hours and were tested. Second, the capacitors were stored at 150°C for 168 hours, followed by capacitance measurements. The test vehicle was stored in a preheated FISHER Isotemp Model 281 oven in nitrogen environment. After the desired storage time, the wafer was taken out and was allowed to cool for 10-15 minutes in the atmosphere. The capacitance measurements were done at room temperature.
Figure 7.19 shows the capacitance data of sputtered-anodized Ta$_2$O$_5$ capacitors with TaN after 168 hours in the oven at 100°C.

![Capacitance Data](image)

**Figure 7.19: Sputtered-anodized Ta$_2$O$_5$ capacitors with TaN diffusion barrier after 168 hours in N$_2$ at 100°C.**

The functional yield did not change, as the total number of defects did not change. The average capacitance to the left side of the step and the right side of the step did not change.

Figure 7.20 shows the capacitance data of sputtered-anodized Ta$_2$O$_5$ capacitors with TaN after an additional 168 hours in the oven at 150°C.
Figure 7.20: Sputtered-anodized Ta$_2$O$_5$ capacitors with TaN diffusion barrier after 168 hours in N$_2$ at 150°C.

Once again, the functional yield did not change. No new defects were introduced. The average capacitances stayed the same as in the as-deposited state and after 100°C.

As a final check, the leakage measurements were performed with a HP4145A Semiconductor Parameter Analyzer. The leakage was as low as 0.1 μA, for a voltage of 20 V. Thus, the presence of TaN did not affect the capacitance and did not introduce any effects to capacitance with heat treatment.

Table 7.2 summarizes the capacitance data before and after thermal excursions.

Table 7.2: Summary of the average capacitances of sputtered-anodized Ta$_2$O$_5$ capacitors with TaN after fabrication and after each thermal excursion.

<table>
<thead>
<tr>
<th>State of the Wafer</th>
<th>Average Capacitance (nF)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Left to the Step</td>
<td>Right to the Step</td>
</tr>
<tr>
<td>As-deposited</td>
<td>1.14</td>
<td>1.08</td>
</tr>
<tr>
<td>After 100°C</td>
<td>1.14</td>
<td>1.08</td>
</tr>
<tr>
<td>After 150°C</td>
<td>1.14</td>
<td>1.08</td>
</tr>
</tbody>
</table>
The table shows that the capacitors are stable up to 150°C and TaN did not introduce any change to capacitance with heat treatment.

The capacitors without TaN were also subjected to thermal storage by a PhD candidate, Alphonse Kamto and the capacitors were found to be thermally stable up in the temperature range with TaN capacitors were tested.

7.1.6 Comparison of Capacitors with and without TaN

Table 7.3 shows the capacitance data along with calculated dielectric constants for capacitors with and without TaN. Capacitance data shown are from only one side of the step in the plot.

Table 7.3: Comparison of capacitances and $k$ values of capacitors with and without TaN.

<table>
<thead>
<tr>
<th>Type</th>
<th>Capacitance (nF)</th>
<th>Dielectric Constant, $k$</th>
<th>Literature Value, $k$</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without TaN</td>
<td>1.13 ± 0.01</td>
<td>23.2</td>
<td>24</td>
<td>[1]</td>
</tr>
<tr>
<td>With TaN</td>
<td>1.14 ± 0.01</td>
<td>23.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

When the capacitance data with TaN and without TaN capacitors were compared, there was only a difference of 0.01 nF, which was only 0.9% of the capacitance without TaN and was negligible. Thus, the effect of TaN on the measured capacitance was negligible. Also, the calculated $k$ values were within ~3% of the literature dielectric constant.

In conclusion, high-functional yield, low-leakage, almost defect free capacitors were fabricated with a TaN barrier layer. This indicates that TaN diffusion barrier can be used in thin film capacitors with little effect on capacitance up to 150°C. In the next chapters, the same concept is applied to Nb$_2$O$_5$ capacitors for improved functional yield.
7.2 The Effect of Change in Anodization End Point on Thickness (Capacitance)

The goal of this experiment was to learn the difference in anodized films that are anodized to the same voltage but stopped at different currents. In the literature, anodization voltage is given as the primary and in most cases the sole parameter, which determines the thickness of the oxide. The anodization profiles have shown that the anodization has two segments, galvanostatic and potentiostatic. It is true that the voltage does determine almost all of the oxide thickness during the galvanostatic regime, but during the potentiostatic segment the current drops exponentially close to zero. During this time dielectric growth occurs very slowly and the thickness will be different from the thickness obtained at the end of galvanostatic segment.

Two wafers were prepared with two end points, 0.51 mA and 6.1 mA, with the voltage at 125 V. The fabrication procedure of the two wafers is explained below.

7.2.1 Fabrication Procedure

The fabrication began with a thermally oxidized 125 mm silicon substrate. 500 Å titanium, 2 µm copper, and 3000 Å tantalum were deposited in order. The wafer was immediately transferred to the anodization bath in order to avoid atmospheric oxidation. The anodization parameters were:

Anodization voltage = 125 V (@16Å/V for 2000 Å oxide),

Anodization Current = 61 mA (0.5 mA/cm² for 125 mm diameter wafer)

The first wafer reached the set voltage in 7 minutes and 30 seconds and the anodization was stopped at a final current of 6.1 mA, 10% of the initial current. The total anodization time was 17 minutes.
The second wafer reached the set voltage in 7 minutes and 25 seconds and the final current was 0.51 mA. The total anodization time was 77 minutes and 23 seconds. The end points and the anodization times are compiled in Table 7.4. From now on, Wafer #1 will be noted as the 6.1 mA Wafer and Wafer #2 will be called the 0.51 mA Wafer.

Table 7.4: Anodization details of 6.1 mA Wafer and 0.51 mA Wafer.

<table>
<thead>
<tr>
<th>No.</th>
<th>Anodization Voltage (V)</th>
<th>Initial Current (mA)</th>
<th>Final Current (mA)</th>
<th>Time to reach Set Voltage (min:sec)</th>
<th>Total Anodization Time (hr:min:sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer #1</td>
<td>125</td>
<td>61</td>
<td>6.1</td>
<td>7:30</td>
<td>0:17:00</td>
</tr>
<tr>
<td>Wafer #2</td>
<td>125</td>
<td>61</td>
<td>0.51</td>
<td>7:25</td>
<td>1:17:23</td>
</tr>
</tbody>
</table>

The colors of the anodized films are discussed in the coming paragraphs. After anodization, a 2 µm copper top plate was sputtered and then patterned and etched to define individual plates of 1 mm × 1 mm capacitors on both the wafers. The final structure is shown in Figure 7.21.

![Figure 7.21: Schematic of capacitor structure of Ta$_2$O$_5$ dielectric with copper top and bottom plates.](image-url)

80
7.2.2 Results and Discussion

The capacitors were tested using the Two Probe Tester as in the previous cases.

6.1 mA Wafer

The capacitance data of the wafer anodized to a final current of 6.1 mA are shown in Figure 7.22. The average capacitance was 1.23 nF to the left side of the step and 1.17 nF to the right side of the step. There was one data point showing a larger capacitance of 1.43 nF compared to others. Out of 4410 capacitors, a total of 10 shorts were found, giving a functional yield of 99.77%. As before, the higher average capacitance was taken as the true average capacitance over the entire wafer for comparison purposes. Please note that the capacitors were measured with the same probe polarities as the previous wafers. Also, the color of the dielectric was violet.

Figure 7.22: Capacitance data of Ta2O5 capacitors anodized to a final current of 10% of initial current; end point at 6.1 mA.
Thickness of the film was calculated based on the color of the film using the following equations:

For a film with refractive index, $n_f$ greater than the refractive index of the substrate, $n_s$, $n_f > n_s$,

$$2n_f d \cos \theta = (p + \frac{1}{2})\lambda$$

Equation (24)

For $n_f < n_s$,

$$2n_f d \cos \theta = (p)\lambda$$

Equation (25)

Where,

- $d$ – Thickness of the film
- $\theta$ – Angle of incidence on the film
- $p$ – Order of interference
- $\lambda$ – Wavelength for the maximum reflection

Here, $n_s = n_{Ta} = 2.84$ and $n_f = n_{Ta2O5} = 2.1$, Equation (25) were used. For $\theta = 0^\circ$, $\lambda = 420$ nm, and $p = 2$, the dielectric thickness for a violet color Ta$_2$O$_5$ film was calculated to be 2000 Å.

**0.51 mA Wafer**

Figure 7.23 shows the capacitance plot of the capacitors anodized to a final current of 0.51 mA.
Figure 7.23: Capacitance data of Ta$_2$O$_5$ capacitors anodized to a final current of 0.51 mA.

The capacitances range from 1.14 nF to 1.05 nF moving from left to right. The average capacitance to the left of the step was 1.13 nF and to the right was 1.06 nF. From a total of 4410 measured capacitors, 8 were shorted. Functional yield was calculated to be 99.82%. The true average capacitance is taken as the 1.13 nF as it was measured with correct polarity voltages applied to the capacitor plates. The color of the dielectric was teal/close to green indicating a thickness of 2280 Å based on the color using Equation (25).
### 7.2.3 Comparison of 6.1 mA Wafer and 0.51 mA Wafer

Figure 7.24 shows the processed wafers; (a) is the 0.51 mA Wafer and (b) is the 6.1 mA Wafer.

![Processed wafers](image)

(a) (b)

**Figure 7.24**: Processed wafers showing different dielectric colors: (a) 0.51 mA wafer and (b) 6.1 mA wafer.

The difference in color indicated the difference in dielectric thickness. Also, the capacitance changed from 1.23 nF to 1.13 nF; a difference of 0.1 nF. From the capacitance equation of a parallel plate capacitor, the capacitance is inversely proportional to the dielectric thickness. Therefore, higher capacitance indicates thinner dielectric and vice versa.

\[
C_{6.1} - C_{0.51} = 1.23 - 1.13
\]

Equation (26)

Let \(d_1\) = dielectric thickness of 6.1 mA wafer

\(d_2\) = dielectric thickness of 0.51 mA wafer,

\[
\frac{\varepsilon_0 \varepsilon_r A}{d_1} - \frac{\varepsilon_0 \varepsilon_r A}{d_2} = 1.23 - 1.13
\]

Equation (27)

Since, the numerator on the left hand side is constant,
\[ \varepsilon_o \varepsilon_r A \left[ \frac{1}{d_1} - \frac{1}{d_2} \right] = 0.1 nF \]  

Equation (28)

Using \( k_{\text{Ta}_2\text{O}_5} = 24 \) and \( A = 1.05 \times 1.05 \text{ mm}^2 \), \( d_1 \) and \( d_2 \) were calculated as follows.

\[ C_1 = \frac{\varepsilon_o \varepsilon_r A}{d_1} \]  

Equation (29)

\[ d_1 = \frac{\varepsilon_o \varepsilon_r A}{C} \]  

Equation (30)

\[ = \frac{8.85 \times 10^{-12} F / m \times 24 \times 1.05 \times 10^{-3} \text{ m} \times 1.05 \times 10^{-3} \text{ m}}{1.23 \times 10^{-9} F} \]

\[ = 1904 \times 10^{-10} \text{ m} \]

\[ = 1904 \text{ Å} \]

\[ C_2 = \frac{\varepsilon_o \varepsilon_r A}{d_2} \]  

Equation (31)

\[ d_2 = \frac{\varepsilon_o \varepsilon_r A}{C} \]  

Equation (32)

\[ = \frac{8.85 \times 10^{-12} F / m \times 24 \times 1.05 \times 10^{-3} \text{ m} \times 1.05 \times 10^{-3} \text{ m}}{1.13 \times 10^{-9} F} \]

\[ = 2072 \times 10^{-10} \text{ m} \]

\[ = 2072 \text{ Å} \]

Therefore, \( d_1 = 1904 \text{ Å} \) and \( d_2 = 2072 \text{ Å} \), for \( k_{\text{Ta}_2\text{O}_5} = 24 \). So, \( d_1 - d_2 = 168 \text{ Å} \). The calculated thickness is smaller compared to \( \sim 250 \text{ Å} \) predicted by the color change. This difference is mainly due to the observer’s ability to exactly match the film color to the wavelength in the visible spectrum. This thickness difference arose from anodizing the wafer for a longer time, as the current \( \times \) time corresponds to the number of Coulombs of charge transferred during anodization. This charge corresponds to the thickness of the oxide formed. Therefore, the longer the process runs, the thicker the film becomes. But,
when the film is thicker, the current (ionic flow) through the film decreases. Only a few ions (ions with high energy) will reach the metal/oxide interface and grow fresh oxide, thickening the film. Since anodization baths vary, it is possible that the lowest current is achieved at different times for different baths. Thus, the final current of anodization can be specified as the end point. Therefore, it is important to specify the final current along with the anodization voltage when anodized oxide thicknesses are mentioned. The data from the 6.1 mA Wafer and the 0.51 mA Wafer are compiled in Table 7.5.

<table>
<thead>
<tr>
<th>Wafer Type</th>
<th>Dielectric Color</th>
<th>Calculated Dielectric Thickness (Å)</th>
<th>Average Capacitance (nF)</th>
<th>Functional yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.1 mA Wafer</td>
<td>violet</td>
<td>1727</td>
<td>1.23</td>
<td>99.77</td>
</tr>
<tr>
<td>0.51 mA Wafer</td>
<td>teal</td>
<td>1780</td>
<td>1.13</td>
<td>99.82</td>
</tr>
</tbody>
</table>

Table 7.5: Ta$_2$O$_5$ capacitors anodized to a final current of 6.1 mA and 0.51 mA.

In order to verify the results, the 6.1 mA wafer was repeated and the results were verified. The average capacitance from the repeated wafer was 1.21 nF, comparable to 1.23 nF from the first trial.

Thus, it can be concluded that unless the dielectric is prepared only in the galvanostatic regime the use of growth rates to predict the material thickness is not the correct method. If galvanostatic and potentiostatic segments are used during anodization, which usually is the case, it is important to mention the final current along with the anodization voltage to determine the correct thickness. Also, since the defects were fewer or the functional yield was higher when anodized longer to a smaller final current, anodizing to a lower current leads to a less defective dielectric. This is because the longer the anodization is done, more and more oxygen vacancies are filled in the dielectric, rendering a more ‘complete’ oxide.
7.3 Effect of Boiling the Dielectric on the Functional yield of a Capacitor

The goal of this study was to compare the functional yield from a wafer that was boiled in DI water after anodization to that of an unboiled wafer. Researchers at the University of Arkansas have used ‘wafer boiling’ technique earlier to improve functional yield. Test capacitors were fabricated with copper top and bottom plates and anodized Ta$_2$O$_5$ dielectric.

7.3.1 Fabrication Procedure

Wafers were prepared and sputtered with Ti, Cu, and Ta as previously described. Then they were anodized at a voltage of 125 V and a current density of 0.5 mA/cm$^2$ was used. For a 125 mm diameter wafer, 61 mA current was calculated. The set voltage was reached in ~10 minutes and the anodization was terminated at a final current of 1 mA. Total time of anodization was ~42 minutes. Notice that the time to reach the set voltage was increased compared to the anodization time given in the 6.1 mA Wafer versus 0.51 mA Wafer section. This increased time indicated the depletion of ions in the bath. After anodization, one of the wafers was boiled in DI water for 30 minutes. The water was initially heated to the boiling temperature in a glass beaker with a stirrer in it. Then, the wafer was immersed into the water for 30 minutes.

The color of the anodized films was bright green after anodization, indicating ~2100 Å calculated thickness from interference color, and boiling did not show any apparent color variation. 2 µm copper was sputtered and pattern etched to form the capacitor top plates. The final structure is shown in Figure 7.25.
Figure 7.25: Schematic of the capacitor structure of the boiled and unboiled wafers.

7.3.2 Results & Discussion

Figure 7.26 shows the capacitance data of the unboiled wafer. The average capacitance was 1.15 nF to the left of the step and 1.09 nF to the right of the step. As before, correct polarity was applied to the left of the step, therefore those measurements were taken for comparison. The same is applicable to the rest of the wafers. 4 shorts were found among 4410 tested capacitors, and a functional yield of 99.91% was calculated. Two spikes pointing up represent bridged capacitors. In both the places, two capacitors in each area were bridged together. These were lithography defects resulting from having inclusions in the mask.
Figure 7.26: Capacitance data of the unboiled Ta$_2$O$_5$ capacitors, anodized at 125 V to a final current of 1 mA.

Figure 7.27 shows the capacitance data of the wafer boiled in water for 30 minutes.

Figure 7.27: Capacitance data of the boiled Ta$_2$O$_5$ capacitors, anodized at 125 V to a final current of 1 mA: anodized dielectric boiled in water for 30 minutes.
The average capacitance to the left of the step was 1.16 nF and to the right of the step was 1.1 nF. The true average capacitance was taken as 1.16 nF. From 4410 tested capacitors, 2 were found to be defective, which gave a functional yield of 99.96%. This result suggested that boiling did not degrade the functional yield; rather an improvement in functional yield was observed. This wafer is noted as Boiled #1 in the next paragraphs.

Four more wafers were fabricated and tested to check for the repeatability of boiling effect. The results are shown in Figure 7.28.

Figure 7.28: Capacitance data of (a) Boiled #2, (b) Boiled #3, (c) Boiled #4, and (d) Boiled #5.
Wafers were named Boiled #2, Boiled #3, Boiled #4, and Boiled #5 corresponding to Figure 7.28 (a), (b), (c), and (d) respectively. Boiled #2 and #5 wafers were boiled for 30 minutes and #3 and #4 were boiled for 1 hour.

Figure 7.28 (a) shows 10 shorted capacitors. Optical inspection revealed that 8 out of 10 defects resulted from particle inclusions. Inclusions can occur during sputtering and/or anodization, and the bath must be covered at all times to avoid contamination. A big chunk (~20 µm diameter) of metal was found in one shorted capacitor, which happened during sputtering. Functional yield was calculated to be 99.77% without eliminating inclusion shorted capacitors.

Figure 7.28 (b) for Boiled #3 wafer shows 9 shorts, giving a functional yield of 99.80%. All the defective capacitors except one had particle inclusions/scratches. Figure 7.28 (c) and (d) show only one shorted capacitor, giving 99.98% functional yield from Boiled #4 and #5 wafers.

Table 7.6 compile the functional yield and true average capacitances of unboiled and boiled wafers.

<table>
<thead>
<tr>
<th>Wafer Name</th>
<th>Boiling Time (min.)</th>
<th>Average Capacitance (nF)</th>
<th>Functional Yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unboiled</td>
<td>0</td>
<td>1.15</td>
<td>99.91</td>
</tr>
<tr>
<td>Boiled #1</td>
<td>30</td>
<td>1.16</td>
<td>99.96</td>
</tr>
<tr>
<td>Boiled #2</td>
<td>30</td>
<td>1.19</td>
<td>99.77</td>
</tr>
<tr>
<td>Boiled #3</td>
<td>60</td>
<td>1.18</td>
<td>99.80</td>
</tr>
<tr>
<td>Boiled #4</td>
<td>60</td>
<td>1.18</td>
<td>99.98</td>
</tr>
<tr>
<td>Boiled #5</td>
<td>30</td>
<td>1.20</td>
<td>99.98</td>
</tr>
</tbody>
</table>

The table shows that Boiled #1, Boiled #4, and Boiled #5 gave high functional yield compared with the unboiled wafer. Notice that changing boiling time from 30 minutes to 1 hour did not affect the functional yield. But the other two wafers suggest that boiling
the dielectric is not the only solution to obtaining good functional yield. Functional yield is affected by every process step and if one can do each step with no inclusions, an almost perfect dielectric is possible with boiling. At this point, the major contribution to the defects in the dielectric is from oxygen vacancies rather than inclusions. Here, if the oxygen vacancies can be completely filled, a perfect dielectric can be achieved. The reason for functional yield improvement of oxide by boiling could be explained by the ability of valve metals to displace hydrogen from water to form oxide [69]. It may be speculated that boiling helps the diffusion of oxygen ions and any incomplete oxide is converted into a perfect dielectric.

Functional yield from boiled and unboiled capacitors were calculated eliminating physically damaged (scratches or inclusions) capacitors. The number of actual defects for boiled wafers were 1, 2, 1, 1, and 1 for #1, #2, #3, #4, and #5 boiled wafers respectively. The total number of defects from the unboiled wafer eliminating damaged capacitors was 3. Thus the overall functional yield from boiled wafers was 99.97% and for the unboiled wafer was 99.93%. Therefore, boiling the dielectric indicated an improvement in functional yield, but more wafers need to be processed to reach a solid conclusion.
Chapter 8: Material Characterization

This chapter discusses the material characterization of Nb, Nb$_2$O$_5$, and NbN using the techniques described in Chapter 4. It begins with the material deposition and parameters and is followed by characterization. The material characterization includes thickness, composition, and crystal structure of the films.

8.1 Material (Nb, Nb-O, and Nb-N) Deposition

Niobium, niobium oxide, and niobium nitride were prepared on p-type Si (111) substrates by DC magnetron sputtering in the Varian XM-8 Sputterer. For niobium deposition inert gas (Ar) plasma was used and for niobium oxide and niobium nitride reactive sputtering was employed. Niobium oxide and niobium nitride films were reactively sputtered using a pre-diluted gas mixture of O$_2$: Ar (10:90) and N$_2$: Ar (25:75) respectively. Gas pressure for sputtering was normally set at 5 mTorr, except for oxide sputtering where 10 mTorr was used. Reactive sputtering was described in detail in Chapter 3. A shadow mask was placed on the wafer during sputtering to obtain a step height which was measured using the Dektak Profilometer. Three areas on the wafer (top, bottom, and the center) were measured and the average thickness was calculated. Please note that Dektak profilometer measurements have an error of ±5%. The gases, their composition, and the gas pressures are shown in Table 8.1.

Table 8.1: Sputtering gas parameters for niobium, niobium oxide, and niobium nitride.

<table>
<thead>
<tr>
<th>Material</th>
<th>Gas(es)</th>
<th>Gas Composition</th>
<th>Gas Pressure (mTorr)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Niobium</td>
<td>Ar</td>
<td>99.99%</td>
<td>5</td>
</tr>
<tr>
<td>Niobium nitride</td>
<td>Ar/N$_2$</td>
<td>75:25</td>
<td>5</td>
</tr>
<tr>
<td>Niobium oxide</td>
<td>Ar/O$_2$</td>
<td>90:10</td>
<td>10</td>
</tr>
</tbody>
</table>
Niobium oxide formed by two other techniques, anodization and a combination of reactive sputtering and anodization, were also investigated. The deposition procedures will be explained in their respective sections.

8.2 Niobium

**Thickness Characterization**

Deposition parameters and the corresponding thicknesses of niobium films are shown in Table 8.2.

**Table 8.2: Niobium deposition parameters and corresponding thicknesses measured with Dektak Profilometer.**

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Power (W)</th>
<th>Pressure (mTorr)</th>
<th>Time/pass (sec)</th>
<th>No. of Passes</th>
<th>Thickness (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2200</td>
<td>5</td>
<td>25</td>
<td>20</td>
<td>2.14</td>
</tr>
<tr>
<td>2</td>
<td>2000</td>
<td>5</td>
<td>25</td>
<td>20</td>
<td>2.03</td>
</tr>
<tr>
<td>3</td>
<td>1500</td>
<td>5</td>
<td>25</td>
<td>20</td>
<td>1.63</td>
</tr>
</tbody>
</table>

Sputtering powers ranged from 1500 W to 2200 W, while the other parameters were kept constant. Since no wafer cooling was available in the sputtering system, the process had to be carried out at regular intervals as wafer overheating can affect the film quality as thermal stresses develop during deposition. If sputtering is carried out for longer periods with no wafer cooling, the films may crack when they are cooled to room temperature due to stress relief. Therefore, sputtering was done for ‘x’ seconds and stopped for some time (~ 2 minutes) to let the wafer cool. Then the process was repeated, until the desired thickness is achieved. Each sputtering period is called a ‘pass.’

In this project, the metal was sputtered every two minutes for twenty-five seconds, for a total of 500 seconds sputtering time per wafer. Thus, there were twenty passes with
twenty five seconds per pass for niobium deposition. Thickness measurements of sputtered films were carried out using the Dektak Profilometer.

As mentioned earlier, five areas of the wafer were measured and the average thickness was calculated. Deposition rate was calculated according to Equation (33).

\[
\text{Deposition Rate} = \frac{\text{Average Thickness}}{\text{No. of passes} \times \text{Time/ pass}}
\]

Equation (33)

The table in Figure 8.1 compares the deposition rates derived from the average thickness and sputtering power. Film deposition rates ranged from 33 Å/second at 1500 W to 43 Å/second at 2200 W. The data are depicted graphically in Figure 8.1. The deposition rate increase with higher sputtering powers as expected. The three measurements taken from top, center, and bottom gave very close deposition rates.

<table>
<thead>
<tr>
<th>Sputtering Power (W)</th>
<th>Average Deposition Rate (Å/second)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1500</td>
<td>33</td>
</tr>
<tr>
<td>2000</td>
<td>41</td>
</tr>
<tr>
<td>2200</td>
<td>43</td>
</tr>
</tbody>
</table>

Figure 8.1: Deposition rate of niobium at different sputtering powers.

For good control over the anodized oxide thickness, it is important to obtain very accurate thickness data for a single power and pressure. Niobium films were deposited at 2200 W and 5 mTorr for different sputtering times. Table 8.3 shows the deposition parameters, thicknesses, and corresponding deposition rates obtained. Figure 8.2 displays
individual measurements taken at top, bottom, and center areas of the wafer. Only center and bottom measurements were available for 500 seconds sputtered niobium. The graph shows that the material is thicker in the center compared to the top and bottom areas. The increased deposition rate for longer sputtering time arose from the time spent for power up and power down in every pass. The average deposition rate of Nb at 220 W was found to be 45 Å/second.

Table 8.3: Sputtering times, average thicknesses, and the deposition rates of niobium, sputtered at 2200 W and 5 mTorr pressure.

<table>
<thead>
<tr>
<th>Niobium: Power = 2200 W &amp; Pressure = 5 mTorr</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time/Pass (sec)</td>
</tr>
<tr>
<td>----------------</td>
</tr>
<tr>
<td>22</td>
</tr>
<tr>
<td>25</td>
</tr>
<tr>
<td>25</td>
</tr>
</tbody>
</table>

Figure 8.2: Deposition rate of niobium at 2200 W at different sputtering times.
8.3 Niobium Oxide

Three types of niobium oxides were characterized: reactively sputtered, anodized, and reactively sputtered and anodized.

8.3.1 Reactively Sputtered

Thickness Characterization

Niobium oxide films were sputtered at 100, 200, 300, 400, and 500 W at a gas pressure of 10 mTorr. The total sputtering time at each power was maintained at 1200 seconds. Reduced time per pass at 100 W and 500 W was used in order to lower the heat buildup in the wafer and to prevent overheating of the cryogenic pump during the sputtering process. Since low power sputtering, 100 W and 200 W, resulted in thinner films, they fell below the measurement range of our profilometer. Thicknesses of these films were investigated by using Auger Electron Spectroscopy (AES). From the depth profiles of sputtered films, the thickness was calculated by multiplying the sputter etch rate in AES by the sputtering depth. The sputtering depth was chosen as the point where Nb and oxygen started to decrease and the underlying silicon concentration started to increase. This happened for the 100 W film at about 12 minutes (~150 Å) into depth profiling as shown in Figure 8.3. Using a 13 Å/minute sputtering rate, based on the sputter etching rate of Ta$_2$O$_5$ standard, for 12 minutes sputtering time, the oxide thickness was calculated to be 156 Å. The same procedure was repeated for the film sputtered at 200 W. The depth profile of the 200 W wafer will be discussed later in the chapter.
Figure 8.3: The Auger depth profile of the Nb$_2$O$_5$ film on silicon substrate sputter deposited at 100 W, showing Nb, O, and Si only.

Deposition parameters and corresponding thicknesses are shown in Table 8.4. Thickness measurements were done only on the center of the wafer.

Table 8.4: Niobium oxide deposition parameters and corresponding thicknesses.

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>Pressure (mTorr)</th>
<th>Time/pass (sec)</th>
<th>No. of Passes</th>
<th>Thickness (Å)</th>
<th>Deposition Rate (Å/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>10</td>
<td>20</td>
<td>60</td>
<td>156</td>
<td>0.13</td>
</tr>
<tr>
<td>200</td>
<td>10</td>
<td>25</td>
<td>48</td>
<td>494</td>
<td>0.41</td>
</tr>
<tr>
<td>300</td>
<td>10</td>
<td>25</td>
<td>48</td>
<td>1050</td>
<td>0.88</td>
</tr>
<tr>
<td>400</td>
<td>10</td>
<td>25</td>
<td>48</td>
<td>1440</td>
<td>1.20</td>
</tr>
<tr>
<td>500</td>
<td>10</td>
<td>20</td>
<td>60</td>
<td>2050</td>
<td>1.71</td>
</tr>
</tbody>
</table>

Oxide film thickness is plotted against sputtering power in Figure 8.4.
The deposition rate ranged from 0.13 Å/second at 100 W to 1.71 Å/second at 500 W. The deposition rate of the 500 W film was verified by thickness analysis of another wafer using the profilometer (1.74 Å/second). The deposition rate increases linearly with the increase in sputtering power.

Since sputter depth values were based on AES profiles of 1000 Å Ta₂O₅ on Ta foil as a standard, it cannot be conclusively said that the obtained thickness was accurate. Therefore, the 200 W film was repeated for a longer sputtering time and the profilometer was used to obtain the thickness information. For a sputtering time of 6000 seconds (150 passes) using profilometry, the average thickness was found to be 3362 Å. Thus, the deposition rate was 0.56 Å/second, higher than the value obtained from AES depth profiling. This difference was attributed to the use of a material of different composition.

Figure 8.4: Graph showing niobium oxide deposition rate as a function of sputtering power, based on Table 8.4.
(Ta₂O₅) for sputter rate calibration from the sample (Nb-O compound). In order to obtain accurate thickness data from Auger profiling, the calibration sample must be of the same composition as the sample for analysis. For a visual confirmation of the deposition rate, a cross-sectional analysis of the same sample, 6000 seconds sputtering time, was done under SEM. Figure 8.5 shows the cross-sectional view of the wafer.

![Cross-sectional view of the wafer](image)

**Figure 8.5: Cross-sectional view of the reactively sputtered Nb₂O₅ sputtered at 200 W for 6000 seconds in Ar/O₂ (90:10) at 10 mTorr showing a thickness of 3400 Å.**

The oxide film thickness was measured to be 3400 Å. This gave a deposition rate of 0.57 Å/second, very close to the value (0.56 Å/second) obtained from the profilometer measurements. Thus, Table 8.4 was revised with the corrected deposition rate for 200 W sputtered niobium oxide of 0.57 Å/second and the revised table is shown in Table 8.5. Figure 8.6 plots the data in Table 8.4 and Table 8.5.
Table 8.5: Niobium oxide deposition parameters and corresponding thicknesses (revised with TEM data).

<table>
<thead>
<tr>
<th>Power (W)</th>
<th>Pressure (mTorr)</th>
<th>Time/pass (sec)</th>
<th>No. of Passes</th>
<th>Thickness (Å)</th>
<th>Deposition Rate (Å/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>10</td>
<td>20</td>
<td>60</td>
<td>156</td>
<td>0.13</td>
</tr>
<tr>
<td>200</td>
<td>10</td>
<td>25</td>
<td>48</td>
<td>494</td>
<td>0.57</td>
</tr>
<tr>
<td>300</td>
<td>10</td>
<td>25</td>
<td>48</td>
<td>1050</td>
<td>0.88</td>
</tr>
<tr>
<td>400</td>
<td>10</td>
<td>25</td>
<td>48</td>
<td>1440</td>
<td>1.20</td>
</tr>
<tr>
<td>500</td>
<td>10</td>
<td>20</td>
<td>60</td>
<td>2050</td>
<td>1.71</td>
</tr>
</tbody>
</table>

Figure 8.6: Niobium oxide deposition rate as a function of sputtering power from Table 8.4 and Table 8.5 showing TEM data point at 200 W.

Thickness measurement was also done on the reactively sputtered oxide at 500 W (10 mTorr in Ar/O₂). The TEM cross-sectional images are shown in Figure 8.7. The oxide sputtering time was 1200 seconds and the thickness was measured to be 2080 Å. This gave a deposition rate of 1.73 Å/second, close to that obtained by profilometry (1.71 Å/second). Figure 8.7 (a) shows the oxide film along with the top gold and platinum.
Figure 8.7 (b) gives a closer look at the dielectric, which shows a columnar structure indicating porous nature.

![Figure 8.7](image)

**Figure 8.7: Cross-sectional view of the reactively sputtered Nb₂O₅ at 500 W; (a) Nb₂O₅ and adjacent layers and (b) Nb₂O₅ showing columnar structure.**

**Film Chemical Composition**

The sputtered films were analyzed using XPS. XPS is the best choice for analyzing reactively sputtered compounds as reactive sputtering can result in a mixture of compounds with different valence states. The Nb 3d spectrum was used to obtain information on the Nb compounds present in the film. Doublets were fitted using the fixed separation, 2.7 eV, between 3d₃/₂ and 3d₅/₂ peaks with Nb3d₅/₂ energy peaks primarily used for the identification of chemical state. The spectrum obtained at each power is discussed below. Spectra were obtained from the surface of the film, as well as ~100 Å deep into the film, which was done by 60 seconds of Ar⁺ etching. The binding energy values for different Nb-O compounds are given in Table 8.6.
Table 8.6: Binding energies of Nb-O compounds.

<table>
<thead>
<tr>
<th>Nb-O Compound</th>
<th>Nb 3d_{5/2} peak energy (eV)</th>
<th>Nb 3d_{3/2} peak energy (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NbO</td>
<td>202.5 — 204.8</td>
<td>205.2 — 207.5</td>
</tr>
<tr>
<td>NbO_{2}</td>
<td>205.2 — 206.1</td>
<td>207.9 — 208.8</td>
</tr>
<tr>
<td>Nb_{2}O_{5}</td>
<td>207.1 — 207.6</td>
<td>209.8 — 210.3</td>
</tr>
</tbody>
</table>

These energy values were taken from the XPS Handbook and National Institute of Science and Technology (NIST) XPS database [76, 77].

**XPS Analysis of the Reactively Sputtered Film at 100 W**

**Initial Surface:**

Figure 8.8 shows the Nb 3d spectrum of reactively sputtered niobium oxide at 100 W in the as-deposited state. Figure 8.8 (a) and (b) show the spectrum before and after peak fitting, respectively.

![Figure 8.8: Nb 3d spectrum of niobium oxide, reactively sputtered at 100 W in the as-deposited state (a) before and (b) after peak fitting.](image)

Peaks were identified and two doublets, (210.1 eV and 207.4 eV) and (208.4 eV and 205.7 eV) were fitted. The first set corresponds to the +5 valence state of niobium (Nb_{2}O_{5}) and the second set indicates the presence of the +4 valence state of niobium.
(NbO₂). Thus, the film sputtered at 100 W mainly contains a mixture of Nb₂O₅ and NbO₂.

**After Ar⁺ etching:**

Figure 8.9 (a) and (b) show the spectra obtained after etching with Ar ions for 60 seconds. Figure 8.9 (a) is before peak fitting and Figure 8.9 (b) after peak fitting.

![Figure 8.9: Nb 3d spectrum of niobium oxide, reactively sputtered at 100 W after Ar⁺ etching (a) before and (b) after peak fitting.](image)

Compared to the surface spectrum, the Nb 3d spectrum after etching showed two prominent peaks and a small peak, seen as a bump on the left hand side of the two peaks. Peak fitting showed that the middle peak was composed of two peaks. Two sets of peaks were fitted into the spectrum. The peaks located at 207.4 eV and 204.8 eV matched 3d₅/₂ binding energies of Nb₂O₅ and NbO respectively. Thus, the inner oxide layer consisted of a lower valence oxide along with Nb₂O₅, compared to the surface. Data from the surface and inside of the film are compiled in Table 8.7.

**Table 8.7: Nb-O compounds present in the reactively sputtered niobium oxide at 100 W.**

<table>
<thead>
<tr>
<th>Analysis Area</th>
<th>NbO</th>
<th>NbO₂</th>
<th>Nb₂O₅</th>
</tr>
</thead>
<tbody>
<tr>
<td>On the Surface</td>
<td>▲</td>
<td>▲</td>
<td>▲</td>
</tr>
<tr>
<td>Inside the Film</td>
<td>▲</td>
<td></td>
<td>▲</td>
</tr>
</tbody>
</table>
Chemical composition of this film was also analyzed with AES. The depth profile with atomic percent of on the vertical axis and sputtering depth on the horizontal axis is shown in Figure 8.10.

Figure 8.10: Auger depth profile of the Nb$_2$O$_5$ film on silicon substrate sputtered at 100 W.

The depth profile showed the presence of five elements, Nb, O, Si, C, and N during the sputtering time of 50 minutes (650 Å sputtering depth). Carbon and oxygen were prominent on the surface with some amount of niobium and ~1% nitrogen. Adventitious carbon was present on the surface and carbon concentration decreased to negligible levels deeper into the film. In the case of nitrogen, as the sputter depth increased, the nitrogen concentration increased and reached 17 at. % and then decreased. The peak was observed where the niobium oxide film ended and silicon started. So it is possible that
nitrogen was incorporated into the film during sputtering. Nitrogen incorporation was due to the presence of gases in the sputtering chamber. When oxide sputtering was done immediately after nitride sputtering, chamber flushing with Ar/O\textsubscript{2} might not have completely removed the nitrogen. As oxide sputtering continued, nitrogen was consumed and eventually reduced to a very low concentration in the chamber. This was evident from the decrease of nitrogen concentration from the interface (Nb-O/Si) to the surface of the film. Nitrogen also extended into silicon, indicating possible diffusion from the oxide film. The thickness of the oxide film can be obtained from this depth profile data as described earlier in the *Thickness Characterization* section.

Depth profile data can also be used to obtain the variation of O/Nb as a function of film depth. Figure 8.11 shows the oxygen/niobium ratio calculated from the atomic concentrations from the depth profile in Figure 8.10. The O/Nb ratio is plotted as a function of sputter time, in other words, sputter depth.

In the graph, the horizontal line represents the ideal O/Nb ratio, 2.5 and the other curve represents the ratio calculated from the depth profile. The area of interest is from 0 minutes sputtering time to 12 minutes where the oxide film ends. Figure 8.11 shows that the O/Nb ratio is the maximum on the surface at 7.3, which was a result of oxygen adsorption on the surface. The ratio decreased to 1.4 at the interface of oxide and silicon. Thus, AES confirmed that 100 W sputtering power did not create stoichiometric Nb\textsubscript{2}O\textsubscript{5}.
Figure 8.11: O/Nb ratio calculated from the depth profile of sputtered film at 100 W, as a function of sputter time.

**XPS Analysis of the Reactively Sputtered Film at 200 W**

**Initial Surface:**

Figure 8.12 shows the Nb3d spectrum obtained from the surface of the sample reactively sputtered at 200 W. The surface spectrum gave two well-defined peaks, located at 209.8 eV and 207.1 eV. These peaks corresponded to the Nb 3d$_{3/2}$ and 3d$_{5/2}$ of +5 valence state of niobium, Nb$_2$O$_5$. 
Figure 8.12: Nb 3d spectrum of niobium oxide, reactively sputtered at 200 W in the as-deposited state (a) before and (b) after curve fitting.

After Ar$^+$ etching:

Figure 8.13 (a) and (b) give the spectrum after Ar$^+$ etching, before curve fitting (a), and after curve fitting (b) respectively.

Figure 8.13: Nb 3d spectrum of niobium oxide, reactively sputtered at 200 W after Ar$^+$ etching (a) before and (b) after peak fitting.

After Ar$^+$ etching, the major peak at 207.8 eV matched Nb$_2$O$_5$ and the second, 205.4 eV corresponded to the +4 valence of niobium (NbO$_2$). The peaks were fitted for both the doublets. The 3d$_{3/2}$ peak of NbO$_2$ was masked by the 3d$_{5/2}$ peak from Nb$_2$O$_5$. A reduction in the valence state could be attributed to either sputter-induced reduction or
stoichiometric change with depth. Literature shows that the sputter-induced reduction can be minimized by adding O\textsubscript{2} to the chamber during sputtering, but that was not done in this project. Thus, a 200 W reactively sputtered oxide contained Nb\textsubscript{2}O\textsubscript{5} on the surface and deeper in the film the oxide was partially reduced to NbO\textsubscript{2}, giving a mixture of Nb\textsubscript{2}O\textsubscript{5} and NbO\textsubscript{2}. The results from the 200 W oxide are summarized in Table 8.8.

**Table 8.8: Nb-O compounds present in the reactively sputtered niobium oxide at 200 W.**

<table>
<thead>
<tr>
<th>Analysis Area</th>
<th>NbO</th>
<th>NbO\textsubscript{2}</th>
<th>Nb\textsubscript{2}O\textsubscript{5}</th>
</tr>
</thead>
<tbody>
<tr>
<td>On the Surface</td>
<td></td>
<td>▲</td>
<td></td>
</tr>
<tr>
<td>Inside the Film</td>
<td></td>
<td>▲</td>
<td>▲</td>
</tr>
</tbody>
</table>

AES Analysis of the Film at 200 W

Similar to the 100 W sputtered film, the oxide sputtered at 200 W was also analyzed using AES as seen in the Nb section. The depth profile of the film sputtered at 200 W is shown in Figure 8.14.

The total sputtering time was 60 minutes and the niobium oxide-silicon interface was reached \( \sim 500 \) Å into the film. Similar to the 100 W film, the nitrogen content was prominent and its concentration, 14\% also matched the concentration in the 100 W film. Surface carbon was high and decreased into the film, similar to the 100 W wafer. All the characteristics were similar to the 100 W film, except for the oxide film thickness.
Figure 8.14: Auger depth profile of the Nb$_2$O$_5$ film on silicon substrate sputtered at 200 W.

Figure 8.15 shows the oxygen/niobium ratio calculated from the depth profile information. O/Nb is shown only for the extent of the oxide film. The figure shows that the oxygen concentration was highest on the surface; it decreased into the film and reached the stoichiometric ratio, 2.5, 6 minutes (78 Å) into the film. The ratio was maintained between 2.3 to 2.1 between 10 minutes (130 Å) and 36 minutes (470 Å). Overall, the O/Nb ratio remained at 2.2 ± 0.1 throughout the film, which was close to the desired 2.5. The increased oxygen content close to the surface came from oxygen adsorption. The decrease in O/Nb ratio into the film indicated the removal of excess oxygen.
Figure 8.15: O/Nb ratio calculated from the depth profile of sputtered film at 200 W, as a function of sputter time.

Depth profiling cannot independently determine the stoichiometry of any compound, because Ar$^+$ etching may preferentially sputter lighter elements and alter the stoichiometry of the compound. Also, the O/Nb ratio was calculated from the atomic concentrations of total oxygen and niobium present in the film, with no distinction as to the valence state of each element, e.g., NbO or Nb$_2$O$_5$.

Auger depth profiling showed that the reactively sputtered film at 200 W gave a close to Nb$_2$O$_5$ stoichiometry, which was verified by XPS analysis.

*XPS Analysis of the Reactively Sputtered Film at 300 W*

**Initial Surface:**

Figure 8.16 shows the Nb 3d spectrum of reactively sputtered niobium oxide at 300 W, taken from the surface of the film.
Figure 8.16: Nb 3d spectrum of niobium oxide, reactively sputtered at 300 W in the as-deposited state.

Peaks were fitted and two sets of peaks, located at (210.0 eV and 207.3 eV and (208.4 eV and 205.6 eV) were obtained. Each set corresponded to Nb$_2$O$_5$ and NbO$_2$ compounds respectively. Thus, the surface of the film sputtered at 300 W consisted of Nb$_2$O$_5$ and NbO$_2$.

**After Ar$^+$ Etching:**

Figure 8.17 (a) and (b) give the spectrum after Ar$^+$ etching before curve fitting and after curve fitting respectively.

Figure 8.17 (a) shows three peaks (one major, one minor, and one seen as a bump on the left side) in the spectrum. These were formed from two sets of doublets with 3d$_{5/2}$ peaks at 207.2 eV and 204.6 eV and they corresponded to Nb$_2$O$_5$ and NbO respectively.
Thus reactively sputtered niobium oxide at 300 W consisted of NbO\textsubscript{2} and Nb\textsubscript{2}O\textsubscript{5} on the surface and NbO and Nb\textsubscript{2}O\textsubscript{5} deeper in the film. These results are given in Table 8.9.

**Table 8.9: Nb-O compounds present in the reactively sputtered niobium oxide at 300 W.**

<table>
<thead>
<tr>
<th>Analysis Area</th>
<th>NbO</th>
<th>NbO\textsubscript{2}</th>
<th>Nb\textsubscript{2}O\textsubscript{5}</th>
</tr>
</thead>
<tbody>
<tr>
<td>On the Surface</td>
<td></td>
<td>▲</td>
<td>▲</td>
</tr>
<tr>
<td>Inside the Film</td>
<td>▲</td>
<td></td>
<td>▲</td>
</tr>
</tbody>
</table>

**XPS Analysis of the Reactively Sputtered Film at 400 W**

**Initial Surface:**

Figure 8.18 shows the Nb 3d spectrum of reactively sputtered niobium oxide at 400 W at the surface. The peaks were fitted into two sets of doublets. The first doublet was located at 210.2 eV and 207.4 eV. These represented the 3d\textsubscript{3/2} and 3d\textsubscript{5/2} binding energies of +5 valence niobium (Nb\textsubscript{2}O\textsubscript{5}). The other doublet with peaks at 208.9 eV and 206.2 eV indicated the presence of NbO\textsubscript{2}. 

---

113
Figure 8.18: Nb 3d surface spectrum of niobium oxide, reactively sputtered at 400 W (a) before and (b) after peak fitting.

**After Ar$^+$ etching:**

Figure 8.19 shows the Nb 3d spectrum of the sample after Ar$^+$ etching. Peaks were identified and fitted at (210.1 eV and 207.4 eV) and (207.5 eV and 204.7 eV) as shown in Figure 8.19 (b). The former and the latter doublets corresponded to Nb$_2$O$_5$ and NbO compounds respectively.

Figure 8.19: Nb 3d spectrum of niobium oxide, reactively sputtered at 400 W after Ar$^+$ etching (a) before and (b) after peak fitting.
Thus, niobium oxide reactively sputtered at 400 W gave Nb₂O₅, NbO₂, and Nb on the surface and Nb₂O₅ and NbO deeper in the film. The results from the oxide sputtered at 400 W are summarized in Table 8.10.

Table 8.10: Nb-O compounds present in the reactively sputtered niobium oxide at 400 W.

<table>
<thead>
<tr>
<th>Analysis Area</th>
<th>NbO</th>
<th>NbO₂</th>
<th>Nb₂O₅</th>
</tr>
</thead>
<tbody>
<tr>
<td>On the Surface</td>
<td>▲</td>
<td>▲</td>
<td>▲</td>
</tr>
<tr>
<td>Inside the Film</td>
<td>▲</td>
<td>▲</td>
<td>▲</td>
</tr>
</tbody>
</table>

XPS Analysis of the Reactively Sputtered Film at 500 W

Initial Surface:

Figure 8.20 shows the Nb 3d surface spectrum of reactively sputtered niobium oxide at 500 W.

![Figure 8.20: Nb 3d surface spectrum of niobium oxide, reactively sputtered at 500 W (a) before and (b) after peak fitting.](image-url)

Peaks were fitted as a single doublet (210.0 eV and 207.2 eV), corresponding to the 3d₃/₂ and 3d₅/₂ binding energy peaks of the +5 valence state of niobium. The fitted peaks are shown in Figure 8.20 (b). Thus it was concluded that the oxide sputtered at 500 W
gave the desired stoichiometry. Most of the experiments in this research project were carried out based on 500 W sputtering giving the desired Nb$_2$O$_5$.

But, a closer inspection revealed the presence of a small peak, seen in Figure 8.21, with binding energy corresponding to NbO$_2$. This result was later verified by analyzing another sample, sputtered at 500 W.

![Figure 8.21: XPS Nb3d surface spectrum of Nb—O film, reactively sputtered at 500 W.](image)

**After Ar$^+$ etching:**

Figure 8.22 shows the Nb 3d spectrum of the sample after Ar$^+$ etching.
Figure 8.22: Nb 3d spectrum of niobium oxide, reactively sputtered at 500 W after Ar$^+$ etching (a) before and (b) after peak fitting.

Peaks were fitted for two sets of peaks whose 3d$_{5/2}$ located at 207.4 eV and 204.6 eV. These peaks matched Nb$_2$O$_5$ and NbO compounds.

Thus, niobium oxide reactively sputtered at 500 W gives Nb$_2$O$_5$ and NbO$_2$ on the surface, whereas the inner film is a mixture of NbO and Nb$_2$O$_5$. The results from 500 W oxide are summarized in Table 8.11.

Table 8.11: Nb-O compounds present in the reactively sputtered niobium oxide at 500 W.

<table>
<thead>
<tr>
<th>Analysis Area</th>
<th>NbO</th>
<th>NbO$_2$</th>
<th>Nb$_2$O$_5$</th>
</tr>
</thead>
<tbody>
<tr>
<td>On the Surface</td>
<td>▲</td>
<td>▲</td>
<td>▲</td>
</tr>
<tr>
<td>Inside the Film</td>
<td>▲</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Table 8.12 compiles the data from reactive sputtering at different sputtering powers.

**Table 8.12: Nb-O compounds present on the surface and deep inside the film at different sputtering powers.**

<table>
<thead>
<tr>
<th>Sputtering Power (W)</th>
<th>Analysis Location</th>
<th>Nb-O Compounds</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>NbO</td>
</tr>
<tr>
<td>100</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
<tr>
<td>200</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
<tr>
<td>300</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
<tr>
<td>400</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
<tr>
<td>500</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
</tbody>
</table>

The table shows that all the sputtering powers give Nb₂O₅, both on the surface and deeper in the film. This was mainly due to the surface oxidation when exposed to air. Also, a reduction in oxide was observable in all the films when sputtered down. Oxide sputtered at 200 W gave stoichiometric Nb₂O₅ on the surface and the other sputtering powers (100 W, 300—500 W) give a combination of Nb₂O₅, and NbO₂. For sputtering powers except 200 W, after etching into the film, NbO₂ changed to NbO. Sputtered films at 200 W, which showed complete stoichiometric oxide on the surface, showed NbO₂ inside the film. This indicated preferential oxygen removal, so that during sputtering Nb₂O₅ reduces to NbO₂ and NbO₂ reduces to NbO. Sputter induced reduction is reported in the literature [78]. Therefore, we cannot conclusively say that the composition changes with film thickness.

Figure 8.23 shows the amount of each compound present on the surface of the reactively sputtered films as a function of sputtering power.
Figure 8.23: Percentage of each compound present on the surface of the reactively sputtered film at different sputtering powers before and after Ar$^+$ etching.

Figure 8.23 shows that the film surface consists mainly of Nb$_2$O$_5$. Nb$_2$O$_5$ concentration reached a peak at 200 W and then decreased. After Ar$^+$ etching, the ratio of compounds became about 1:1, except for 400 W.

Crystal Structure:

The crystal structure of the niobium oxide films reactively sputtered at 200 W and 500 W are shown in Figure 8.24 (a) and (b) respectively. The SAD patterns show that the oxides are amorphous.
8.3.2 Anodized

Material Deposition

A thermally oxidized 125 mm silicon wafer was backsputtered and 5500 Å of niobium was deposited at 2200 W and 5 mTorr Argon pressure. The wafer was allowed to cool in the chamber before taking it out of the sputtering system. The niobium film was then anodized in a mixture of tartaric acid, ethylene glycol, and DI water at room temperature. The details of the anodization bath can be found in Chapter 3. Anodization was carried out in two segments, the first galvanostatic and the second potentiostatic. Niobium pentoxide (Nb$_2$O$_5$) was formed at 83 V and at a current density of 0.5 mA/cm$^2$. Based on that, the initial current was set at 61 mA for the 125 mm diameter wafer. The voltage calculation was based on the 24 Å /V literature value for the growth rate of Nb$_2$O$_5$ [3, 79]. The total time taken for anodization was 40 minutes, out of which the
galvanostatic regime lasted for the first 8 minutes. The final current was 1 mA and the
color of the anodized film was pale green, indicating 2200 Å thickness from calculations
based on interference color. This is an approximation and not an accurate thickness as it
depends on the observer’s ability to match the film color to the spectrum color for the
correct wavelength. The wafer was then rinsed and dried.

**Thickness Characterization**

The thickness measurements of anodized films were made using TEM. Figure 8.25
(a) shows the cross-section of the anodized film. The image clearly shows a double layer
structure. EDS confirmed that both the layers were of the same composition. The
thickness of each layer was measured and the total thickness was calculated. The layer
close to niobium, referred to as the bottom layer, measured ~1050 Å and the top layer,
the layer close to gold, measured ~850 Å, giving a total oxide thickness of 1900 Å. The
ratio of the bottom to top layer thickness was calculated to be 1.2. Figure 8.25 (b) and (c)
give a closer look at the individual layers. The bottom layer was dense and the top layer
was porous. Even though the boundary between the layers was uneven, the average
thickness of each layer was consistent throughout the sample. Figure 8.25 (d) shows the
contrast between the two layers with gold and niobium films on either side. One reason
for this structure could be that the double layer structure corresponds to the two regimes
of anodization; galvanostatic and potentiostatic. During the galvanostatic regime, the
total oxide thickness was formed as a function of applied voltage. In the second regime,
the current decreased to 1 mA during which the oxide densification took place. Thus, the
two layers corresponded to each anodization regime; the porous layer to galvanostatic
and the dense layer to potentiostatic.
Figure 8.25: Cross-sectional view of Nb$_2$O$_5$ anodized at 83 V and 0.5 mA/cm$^2$ to a final current of 1 mA: (a) Image showing thickness and double layer of Nb$_2$O$_5$ with gold and niobium on either side (b) Comparison of porous top layer and dense bottom layer (c) Bottom layer of Nb$_2$O$_5$ and Nb interface, and (d) Cross-section contrasting two layers of Nb$_2$O$_5$.

In order to validate this theory, a second wafer was processed. The niobium film was anodized at 83 V and 0.5 mA/cm$^2$ as before. But, anodization was terminated as soon as the voltage reached the set point, 83 V, i.e., film was anodized only in the galvanostatic regime. The TEM images of the anodized film are shown in Figure 8.26.
Figure 8.26: Cross-sectional view of Nb$_2$O$_5$ anodized in the galvanostatic regime only, at 83 V and 0.5 mA/cm$^2$: (a) Image showing multiple layers in the wafer (b) thicknesses and double layer of Nb$_2$O$_5$ with gold and niobium on either side.

Figure 8.26 (a) shows the cross-sectional view of different layers in the specimen. Figure 8.26 (b) gives a closer view of the dielectric showing two-layered oxide. Total thickness of the film was 1446 Å. The thickness of the top layer was ~750 Å and that of the bottom layer was 696 Å. Visually, the two layers were about the same thickness and the measurements showed only a difference of ~50 Å. The ratio of the top and the bottom thickness was close to 1, whereas in the previous case, the ratio was 1.25. Thus, there was a difference in film thickness when anodization was done using both galvanostatic and potentiostatic regimes and when it was done in only the galvanostatic regime. Comparing the total oxide thicknesses in both cases, the sample analyzed with only the galvanostatic regime gave a thickness 454 Å lower than the thickness obtained with both the regimes. Thus, it can be concluded that the oxide growth continued in the potentiostatic regime as well.

Figure 8.27 shows the double layer structure of the oxide.
Figure 8.27: Nb$_2$O$_5$ film anodized in the galvanostatic regime, at 83 V and 0.5 mA/cm$^2$ current density, (a) both the layers of the oxide film and (b) bottom layer, the layer close to Nb.

Clearly, both the layers were porous, which supported the theory that the galvanostatic regime produces porous films and densification takes place during the potentiostatic regime.

Since two layers were seen after anodization in only the galvanostatic regime, the explanation that two regimes give two layers was not valid. Therefore, another aspect of anodization was considered. When oxide is grown during anodization, it consumes metal and grows on the surface of the metal as well as into the metal. There is a high possibility that these layers represent the oxide grown into the metal and above the surface of the metal. The author could find only one reference that gave numerical data on how much oxide is grown out and into the metal during anodization [79]. It stated,

“For each unit of oxide, two thirds grows out and one third grows in.”
This means the surface layer is thicker compared with the bottom layer. In our case, the first scenario gave a thicker bottom layer compared with the top or surface, and the second scenario gave about equal thickness on both layers.

AES analysis of the anodized film (both galvanostatic and potentiostatic regimes were used) showed carbon species incorporation into the film. More on carbon incorporation will be discussed in the Film Chemical Composition section. Note that there is some discrepancy between the thicknesses given by AES and by TEM imaging. Therefore, the ratio method was used to compare the thicknesses. AES shows that the oxide film contains ~13% carbon around 870 Å into the film; afterwards the content drops to ~1%. This value is very close to the top layer thickness obtained in the first wafer (850 Å). This gives rise to the possibility that the image contrast came from carbon incorporation. A similar effect has been reported for anodic films with phosphorous species incorporation [80]. The incorporation of these species gives a lighter appearance to the outer layer compared to the inner layer.

The carbon species are incorporated during the oxide growth out of the metal. Since film growth takes place at the metal-electrolyte interface, anions (tartarate ions/carbon species in this case) can be easily incorporated into the oxide film as seen in Figure 8.28.
Film Chemical Composition

Two techniques were used for chemical analysis of anodized films; XPS and AES. Results from each of these techniques are discussed below. Two samples were taken;
one from the center and the other from the left area of the wafer. This was done to evaluate the uniformity of anodization across the wafer.

**XPS Analysis of the Anodized Film CENTER**

**Initial Surface:**

Figure 8.29 shows the spectrum of the anodized niobium oxide dielectric taken from the CENTER area of the wafer.

![XPS Nb 3d surface spectrum of the anodized niobium oxide CENTER.](image)

The figure shows the typical Niobium 3d doublet with the higher energy peak, 3d\(_{3/2}\), 209.7 eV of the +5 valence state of Niobium (Nb\(_2\)O\(_5\)). Similarly, the lower energy peak at 207.0 eV matches the 3d\(_{5/2}\) binding energy of the +5 valence Niobium. In essence, anodization results in stoichiometric Nb\(_2\)O\(_5\) as expected.
After Ar\(^+\) etching:

Figure 8.30 (a) shows the Nb 3d spectrum before curve fitting and (b) shows the spectrum after curve fitting.

![Figure 8.30: XPS spectrum (Nb 3d) of anodized niobium oxide CENTER after Ar\(^+\) etching.](image)

The first doublet, 209.9 eV and 207.2 eV, corresponds to the binding energy of +5 oxidation state of niobium (Nb\(_2\)O\(_5\)). The second set, 207.0 and 204.3 eV, indicates the presence of NbO. Thus, the anodic film gives a mixture of Nb\(_2\)O\(_5\) and NbO deeper in the film after Ar\(^+\) sputtering.

The depth profile of the anodic oxide from the center area of the wafer is shown in Figure 8.31. Carbon incorporation has been reported in the literature where a tartaric acid-glycol-water mixture is used as the anodization electrolyte [65]. This is similar to phosphorous pick up from a phosphorous-based electrolyte and boron pickup from a borate based electrolyte [63, 64, 66]. In all these cases, the incorporated element does not extend all the way to the metal/oxide interface. The same trend can be observed in Figure 8.31.
The lower oxygen concentration in the initial layer could be due to faster removal of oxygen due to the porous nature of the film. There is also the presence of nitrogen, which increases into the silicon, while maintaining a uniform concentration through the film. It is possible that nitrogen migrated into the oxide film during anodization. Nitrogen in the bulk was incorporated in the film during sputtering due to the presence of residual gases in the chamber.

Figure 8.32 shows the oxygen/niobium ratio in the CENTER sample derived from the depth profile. Both ideal (O/Nb = 2.5) and actual ratios are compared. The plot shows that the oxygen concentration is highest on the surface and decreases to a value close to stoichiometric and eventually decreases to zero. The high concentration on the surface results from adsorption of oxygen on the surface. The O/Nb ratio is maintained between...
2.3 and 2.4 all throughout the film. The deviation from the stoichiometric ratio, 2.5 can be a result of sputter reduction.

![Graph showing O/Nb ratio as a function of Auger sputter depth.]

**Figure 8.32:** O/Nb ratio calculated from the depth profile of the oxide film (CENTER), anodized at 83 V, as a function of sputter depth.

*XPS Analysis of the Anodized Film LEFT*

**Initial Surface:**

Figure 8.33 shows the Nb 3d spectrum from the surface of the anodized film from the LEFT area of the wafer.
Figure 8.33: XPS spectrum (Nb 3d) of as-deposited anodized niobium oxide LEFT.

The major and minor peaks at 207.0 eV and 209.7 eV correspond to the binding energies of Nb 3d\(_{5/2}\) and Nb 3d\(_{3/2}\) respectively of Nb\(_2\)O\(_5\). Therefore, 100% Nb\(_2\)O\(_5\) was obtained on the LEFT area of the wafer as well.

**After Ar\(^+\) etching:**

Figure 8.34 shows the Nb 3d spectrum after Ar\(^+\) sputtering for sixty seconds. Figure 8.34 (a) and (b) show the spectrum before and after curve fitting respectively.

Figure 8.34: XPS spectrum (Nb 3d) of anodized niobium oxide LEFT after Ar\(^+\) etching.

Two sets of doublets were observed in the fitted data. The first set, 209.8 eV and 207.0 eV, corresponded to the +5 valence state of niobium (Nb\(_2\)O\(_5\)), and the second set,
207.2 eV and 204.4 eV, matches the binding energy of NbO. Therefore, similar to the CENTER sample after etching, the film is a mixture of Nb$_2$O$_5$ and NbO.

**AES Analysis of the Anodized Oxide - LEFT**

Figure 8.35 shows the depth profile from the oxide film on the LEFT area of the wafer.

![Sputter Depth based on TEM Data(Å)](image)

**Figure 8.35: Depth profile of LEFT niobium oxide anodized at 83 V and 0.5 mA/cm$^2$ current density.**

The plot shows the presence of Nb, O, C, and N. Similar to the CENTER sample, tartarate ion (carbon) incorporation into the film was observed. Compared to the CENTER sample, the ions were incorporated into about the same thickness (100 Å difference) of the film. Nitrogen was present in the film uniformly and extended into the bulk from sputtering as explained for the CENTER wafer. Figure 8.36 shows the O/Nb ratio derived from the depth profile.
Figure 8.36: O/Nb ratio calculated from the depth profile of the oxide film (LEFT), anodized at 83 V, as a function of sputter depth.

Similar to the CENTER sample, the oxygen concentration was highest on the surface and it decreased close to stoichiometric. The O/Nb ratio was between 2.23 and 2.4 throughout the film. CENTER and LEFT samples are compared in Figure 8.37.

The figure shows that the data from both the samples were similar. The only difference observed was the thickness for which the stoichiometric ratio held. The thickness of the film in the center was greater compared with the left. If the wafer was not uniformly spaced from the cathode, the electric field varied across the wafer and some of the areas became thinner compared with the others.
The XPS analysis of the CENTER and the LEFT samples showed that the surface of the film contained the desired Nb$_2$O$_5$, and deeper into the film the oxide was partially reduced to form NbO, which could be a result of preferential oxygen removal during sputtering.

**Crystal Structure**

The electron diffraction pattern of the oxide films anodized using the galvanostatic and potentiostatic modes and only the galvanostatic mode are shown in Figure 8.38. The diffused pattern indicated the amorphous nature of the film.
Figure 8.38: Electron diffraction pattern of anodized Nb$_2$O$_5$ (a) galvanostatic and potentiostatic modes were used and (b) only galvanostatic mode was used.

8.3.3  *(Reactively Sputtered Nb$_2$O$_5$ + Sputtered Nb) Anodized*

A third type of oxide formed was composed of a reactively sputtered oxide and sputtered niobium. The two-layer stack was then anodized to form complete Nb$_2$O$_5$. Films were formed on a 125 mm wafer and two samples were analyzed for thickness uniformity. These samples were taken from the center and the right areas of the wafer.

**Material Deposition**

The fabrication began with a thermally oxidized silicon wafer. After backspattering for 60 seconds, Ti (500 Å)/ Cu (2 μm)/ Ti (500 Å)/ NbN (500 Å)/ Nb$_2$O$_5$/Nb (528 Å) were deposited. Nb$_2$O$_5$ was sputtered at 500 W for 400 seconds in Ar/O$_2$ at 10 mTorr pressure. Then the wafer was anodized at 83 V and 0.5 mA/cm$^2$ current density. The voltage was increased step by step, starting at 60 V to 80 V in 5 V increments; after that the voltage was increased to 83 V. The final current was 2.1 mA.
**Thickness Characterization**

Figure 8.39 shows the cross-sectional view of the sample taken from the center of the wafer. Figure 8.39 (a) shows the multilayered structure. Darker areas in the sample indicate that the sample is thicker and electrons could not be transmitted.

![Cross-sectional view of the sample](image)

**Figure 8.39: Cross-sectional view of the reactively sputtered (Nb$_2$O$_5$ + sputtered Nb) anodized oxide; (a) showing the multilayered structure and (b) showing the crack propagation at the reactively sputtered and anodized oxide interface.**

The total oxide thickness was measured in four places and the thickness averaged to be 2377 ± 19 Å. Figure 8.39 (b) shows a crack at the interface between anodized and reactively sputtered oxide. These interfacial cracks resulted from the volume expansion occurring during the anodization of Nb. The crack propagation shown in the figure extends to about 1870 Å in length. A schematic of crack formation during anodization is shown in Figure 8.40.
Figure 8.40: Schematic of stages of crack formation during anodization; (a) before anodization, (b) volume change of Nb during anodization, and (c) crack formation.

Figure 8.41 shows the cross-sectional view of the sample taken from the right area of the wafer.

Figure 8.41: Cross-sectional TEM image of reactively sputtered (Nb₂O₅ + sputtered Nb) anodized oxide from the RIGHT area of the wafer; (a) showing the multilayered structure and (b) showing total Nb₂O₅ thickness and individual oxide layers.

Figure 8.41 (a) identifies each layer and Figure 8.41 (b) shows both the reactively sputtered layer and the anodized film. Figure 8.41 (b) shows the similar interfacial cracks (circles) between the reactively sputtered and anodized films. The bigger crack measured ~210 Å thick. As seen earlier, the anodized oxide was composed of two layers. These layers measured 880 Å (inner layer, close to the reactively sputtered film) and 650 Å (outer layer). The thickness of the reactively sputtered film was measured to be ~ 630 Å.
above the bottom circle and ~740 Å at the top of the image. Notice that the total dielectric thickness varied from 2120 Å to 2250 Å moving up in the image. Compared to the center dielectric thickness these thicknesses were smaller. Therefore, the dielectric was thicker in the center and the thickness decreased from the center to the right of the wafer. The reactively sputtered thickness difference with location on the wafer also supported the conclusion that the thickness varies across the wafer, which was a result of sputter non-uniformity.

**Crystal Structure**

The combined structure of reactively sputtered and anodized niobium oxide film from the right and the center areas of the wafer are shown in Figure 8.42. The patterns showed the amorphous nature of the film.

![Figure 8.42: Electron diffraction pattern of (reactively sputtered Nb₂O₅ + sputtered Nb) anodized Nb₂O₅ (a) right and (b) center.](image)

Figure 8.42: Electron diffraction pattern of (reactively sputtered Nb₂O₅ + sputtered Nb) anodized Nb₂O₅ (a) right and (b) center.
8.4 Niobium Nitride

Thickness Characterization

Niobium nitride films were sputtered at 800 W, 1500 W, 2000 W, and 2200 W at a gas pressure of 5 mTorr. These powers were chosen based on the sputtering parameters of TaN. The highest power was limited to 2200 W because of arcing issues from the target. A gas pressure of 5 mTorr was used as opposed to the 10 mTorr used in oxide sputtering because of the higher nitrogen content in the gas mixture compared to the Ar/O\textsubscript{2} mixture. The deposition rate ranged from 7 to 24 Å/second from 800 W to 2200 W. Deposition parameters and thicknesses of niobium nitride films are shown in Table 8.13 and the deposition rates and corresponding sputtering powers are plotted in Figure 8.43.

Table 8.13: Niobium nitride deposition parameters and corresponding deposition rates.

<table>
<thead>
<tr>
<th>Wafer #</th>
<th>Power (W)</th>
<th>Pressure (mTorr)</th>
<th>Time/pass (sec)</th>
<th>No. of Passes</th>
<th>Thickness (µm)</th>
<th>Deposition Rate (Å/sec)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>800</td>
<td>5</td>
<td>25</td>
<td>35</td>
<td>0.62</td>
<td>7</td>
</tr>
<tr>
<td>2</td>
<td>1500</td>
<td>5</td>
<td>25</td>
<td>20</td>
<td>0.70</td>
<td>14</td>
</tr>
<tr>
<td>3</td>
<td>2000</td>
<td>5</td>
<td>25</td>
<td>15</td>
<td>0.87</td>
<td>23</td>
</tr>
<tr>
<td>4</td>
<td>2200</td>
<td>5</td>
<td>25</td>
<td>15</td>
<td>0.91</td>
<td>24</td>
</tr>
</tbody>
</table>
Figure 8.43: Graph showing niobium nitride deposition rate as a function of sputtering power, based on Table 8.12.

Five different areas (top, bottom, center, left, and right) in the wafer were measured for all the powers except 800 W; only top, center, and bottom were measured. Measurements were close together and are contained in the markers. The deposition rate at 2200 W was verified using TEM imaging.

Figure 8.44 shows the cross-sectional view of a silicon wafer with Pt/Au/Cr/Nb$_2$O$_5$/NbN/Ti/Cu/Ti/SiO$_2$ layers. The NbN sputtering power was 2200 W for 25 seconds at 5 mTorr. The thickness of NbN was measured to be 685 ± 20.4 Å, giving a deposition rate of 27.4 Å/second, which is within 12% agreement with the deposition rate from profilometry (24.2 Å/second).
Figure 8.44: Cross-sectional view of a silicon wafer with multiple thin films including NbN sputtered at 2200 W for 25 seconds in Ar/N₂ at 5 mTorr; (a) multilayered structure and (b) NbN thickness.

**Film Chemical Composition**

XPS spectra obtained for each sputtering power are analyzed below. The binding energy values for different compounds used in this section are shown in Table 8.14.

**Table 8.14: Binding energies of Nb-N compounds and Nb₂O₅ used in this section.**

<table>
<thead>
<tr>
<th>Compound</th>
<th>Nb 3d₅/₂ peak energy (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NbN</td>
<td>203.6 — 203.9</td>
</tr>
<tr>
<td>NbNₓ</td>
<td>203.0 — 203.3</td>
</tr>
<tr>
<td>NbON</td>
<td>204.6 — 205.8</td>
</tr>
<tr>
<td>Nb₂O₅</td>
<td>206.6 — 207.1</td>
</tr>
</tbody>
</table>

*XPS Analysis of the Reactively Sputtered Film at 800 W*

**Initial Surface:**

Figure 8.45 shows the Nb 3d spectrum of the film sputtered at 800 W.
Figure 8.45: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 800 W in the as-deposited state; (a) original data and (b) after curve fitting.

From deconvolution and curve fitting, four major peaks were obtained. These peaks were located at 209.8 eV, 207.1 eV, 204.9 eV, and 203.9 eV. The first and the second peaks (209.8 eV and 207.1 eV) correspond to the $3d_{3/2}$ and $3d_{5/2}$ peaks of the +5 valence state of niobium Nb, (Nb$_2$O$_5$). But, the middle peak is composed of more than one peak as will be seen. The third peak, the small peak at 204.9 eV corresponds to the $3d_{5/2}$ peak of NbON [81]. The final peak, 203.9 eV, corresponds to the $3d_{3/2}$ peak of the +3 valence of niobium (NbN). Since ‘d’ orbital peaks must appear as doublets, the middle peak is comprised of $3d_{3/2}$ of NbN and NbON along with $3d_{5/2}$ of Nb$_2$O$_5$. The results are summarized in Table 8.15.
Table 8.15: Nb 3d peak binding energies from NbN thin film reactively sputtered at 800 W and corresponding Nb compounds.

<table>
<thead>
<tr>
<th>3d_{5/2} Peak Energy (eV)</th>
<th>Compound</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>207.1</td>
<td>Nb_{2}O_{5}</td>
<td>[77]</td>
</tr>
<tr>
<td>204.9</td>
<td>NbON</td>
<td>[81]</td>
</tr>
<tr>
<td>203.9</td>
<td>NbN</td>
<td>[81]</td>
</tr>
</tbody>
</table>

Thus, the film sputtered at 800 W was comprised of three types of niobium compounds: Nb_{2}O_{5}, NbON, and NbN. The presence of Nb_{2}O_{5} may be explained by the surface oxidation of niobium compounds when exposed to air [81].

**After Ar^+ etching:**

Figure 8.46 shows the Nb 3d spectrum after Ar^+ etching for 60 seconds.

Figure 8.46: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 800 W after Ar^+ etching.

Three peaks were located at 208.5 eV, 206.0 eV, and 203.3 eV. The major peaks, 206.0 eV and 203.3 eV corresponded to the 3d_{3/2} and 3d_{5/2} peaks of NbN_x (x<1)
compound [77]. The binding energy peak at 208.5 eV corresponded to NbON, whose 3d_{5/2} peak (205.8 eV) resides within the 3d_{3/2} peak of NbN_x. The oxynitrides and surface oxides had largely disappeared after sputtering. This confirmed that Nb_2O_5 was a result of surface oxidation. Also, preferential sputtering of oxygen and some nitrogen took place during Ar^+ bombardment [78, 82]. The results are tabulated in Table 8.16.

Table 8.16: Nb 3d peak binding energies from NbN thin film reactively sputtered at 800 W, and corresponding Nb compounds, after Ar^+ etching.

<table>
<thead>
<tr>
<th>3d_{5/2} Peak Energy (eV)</th>
<th>Compound</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>205.8</td>
<td>NbON</td>
<td>[81]</td>
</tr>
<tr>
<td>203.3</td>
<td>NbN_x</td>
<td>[77]</td>
</tr>
</tbody>
</table>

Therefore, the nitride film sputtered at 800 W consisted of a mixture of nitrides and oxides on the surface. Inside the film, the composition was non-stoichiometric NbN and niobium oxynitride.

*XPS Analysis of the Reactively Sputtered Film at 1500 W*

**Initial Surface Analysis:**

Figure 8.47 shows the Nb 3d spectrum of the film sputtered at 1500 W. Four peaks obtained were located at, 209.6 eV, 206.7 eV, 204.6 eV, and 203.7 eV. The first two peaks belong to binding energies of Nb_2O_5 and the second and third peaks correspond to NbON and NbN respectively. Table 8.17 compiles the data from the surface analysis.
Figure 8.47: XPS Nb 3d surface spectrum of the niobium nitride thin film reactively sputtered at 1500 W.

Table 8.17: Nb 3d peak binding energies from NbN thin film reactively sputtered at 1500 W, and corresponding Nb compounds.

<table>
<thead>
<tr>
<th>3d_{5/2} Peak Energy (eV)</th>
<th>Compound</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>206.7</td>
<td>Nb_2O_5</td>
<td>[77]</td>
</tr>
<tr>
<td>204.6</td>
<td>NbON</td>
<td>[81]</td>
</tr>
<tr>
<td>203.7</td>
<td>NbN</td>
<td>[77]</td>
</tr>
</tbody>
</table>

Therefore, the film sputtered at 1500 W contained Nb_2O_5, NbON, as well as NbN similar to other sputtered films discussed above.

**After Ar^+ etching:**

Figure 8.48 shows the Nb 3d spectrum after Ar^+ etching for 60 seconds. There were two major peaks and a minor peak seen as a bump to the left of the spectrum. The two major peaks (205.7 eV and 203.0 eV), corresponded to the doublet of NbN_x. The minor peak at 207.6 eV corresponded to 3d_{3/2} of NbON, whose 3d_{5/2} was located at 204.8 eV within the first major peak. Thus, the film sputtered at 1500 W after Ar^+ etching was composed of a large percentage of NbN_x and small amounts of NbON.
Figure 8.48: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 1500 W after Ar$^+$ etching.

Data are summarized in Table 8.18.

Table 8.18: Nb 3d peak binding energies from NbN thin film reactively sputtered at 1500 W and corresponding Nb compounds, after Ar$^+$ etching.

<table>
<thead>
<tr>
<th>3d$_{5/2}$ Peak Energy (eV)</th>
<th>Compound</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>204.8</td>
<td>NbON</td>
<td>[81]</td>
</tr>
<tr>
<td>203.0</td>
<td>NbN$_x$</td>
<td>[77]</td>
</tr>
</tbody>
</table>

XPS Analysis of the Reactively Sputtered Film at 2000 W

Initial Surface Analysis:

Figure 8.49 shows Nb 3d spectrum of the film sputtered at 2000 W. Four peaks were found and were located at 209.4 eV, 206.6 eV, 204.6 eV, and 203.6 eV. The first two peaks represent Nb$_2$O$_5$, the second and third peaks represent Nb3d$_{5/2}$ of NbON and NbN respectively. Data are summarized in Table 8.19.
Figure 8.49: XPS Nb 3d surface spectrum of the niobium nitride thin film reactively sputtered at 2000 W.

Table 8.19: Nb 3d peak binding energies from NbN thin film reactively sputtered at 2000 W and corresponding Nb compounds.

<table>
<thead>
<tr>
<th>3d_{5/2} Peak Energy (eV)</th>
<th>Compound</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>206.6</td>
<td>Nb_{2}O_{5}</td>
<td>[77]</td>
</tr>
<tr>
<td>204.6</td>
<td>NbON</td>
<td>[81]</td>
</tr>
<tr>
<td>203.6</td>
<td>NbN</td>
<td>[77]</td>
</tr>
</tbody>
</table>

After Ar\(^+\) etching:

Figure 8.50 shows the Nb 3d spectrum after Ar\(^+\) etching 60 seconds. There were two major peaks and one minor peak in the spectrum. The major peaks, 205.7 eV and 203.0 eV corresponded to 3d\(_{3/2}\) and 3d\(_{5/2}\) peaks of NbN\(_x\) [77]. The minor peak, 207.8 eV, corresponded to the 3d\(_{3/2}\) peak of NbON within an error of 0.2 eV, whose 3d\(_{5/2}\) was
located at 205 eV within the first major peak. Therefore, a film sputtered at 2000 W after Ar\textsuperscript{+} etching showed a combination of non-stoichiometric niobium nitride and NbON.

Figure 8.50: XPS Nb 3d spectrum of the niobium nitride thin film reactively sputtered at 2000 W after Ar\textsuperscript{+} etching.

The data are summarized in Table 8.20.

Table 8.20: Nb 3d peak binding energies from NbN thin film reactively sputtered at 2000 W, and corresponding Nb compounds, after Ar\textsuperscript{+} etching.

<table>
<thead>
<tr>
<th>3d\textsubscript{5/2} Peak Energy (eV)</th>
<th>Compound</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>205.0</td>
<td>NbON</td>
<td>[81]</td>
</tr>
<tr>
<td>203.0</td>
<td>NbN\textsubscript{x}</td>
<td>[77]</td>
</tr>
</tbody>
</table>

*XPS Analysis of the Reactively Sputtered Film at 2200 W*

*Initial Surface Analysis:*

Figure 8.51 shows the Nb 3d spectrum of the film sputtered at 2000 W. Four peaks found were located at 209.5 eV, 206.6 eV, 204.6 eV, and 203.6 eV. The first two peaks represented 3d\textsubscript{3/2} and 3d\textsubscript{5/2} peaks of Nb_2O_5; the third peak corresponded to 3d\textsubscript{5/2} of
NbON. The fourth peak at 203.6 eV matched 3d_{5/2} of NbN. Thus, the 3d_{3/2} peaks of NbON and NbN were assigned at 207.4 eV and 206.4 eV respectively.

![XPS Nb 3d surface spectrum of the niobium nitride thin film reactively sputtered at 2200 W.](image)

Figure 8.51: XPS Nb 3d surface spectrum of the niobium nitride thin film reactively sputtered at 2200 W.

The data are summarized in Table 8.21.

<table>
<thead>
<tr>
<th>3d_{5/2} Peak Energy (eV)</th>
<th>Compound</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>206.6</td>
<td>Nb_{2}O_{5}</td>
<td>[77]</td>
</tr>
<tr>
<td>204.6</td>
<td>NbON</td>
<td>[81]</td>
</tr>
<tr>
<td>203.6</td>
<td>NbN</td>
<td>[77]</td>
</tr>
</tbody>
</table>

Table 8.21: Nb 3d peak binding energies from NbN thin film reactively sputtered at 2200 W and corresponding Nb compounds.

In comparison to the spectra from the 2000 W sample, the peaks at 2200 W were very much alike and the peak binding energies were the same. Thus, we can say that a 200 W increase in power was not sufficient to bring forth major compositional differences. **After Ar^+ etching:**

Figure 8.52 shows the Nb 3d spectrum after Ar^+ etching for 60 seconds.
The three peaks corresponded to 203.1 eV, 205.8 eV, and 208.2 eV. These are two sets of doublets, (205.8 eV and 203.1 eV) and (208.2 eV and 205.5 eV), corresponding to NbN\textsubscript{x} and NbON respectively. Therefore, ~100 Å into the film, the composition was a mixture of NbN\textsubscript{x} and NbON. Data from the 2200 W wafer after Ar\textsuperscript{+} etching are given in Table 8.22.

Table 8.22: Nb 3d peak binding energies from NbN thin film reactively sputtered at 2200 W and corresponding Nb compounds, after Ar\textsuperscript{+} etching.

<table>
<thead>
<tr>
<th>3d\textsubscript{5/2} Peak Energy (eV)</th>
<th>Compound</th>
<th>Ref.</th>
</tr>
</thead>
<tbody>
<tr>
<td>205.5</td>
<td>NbON</td>
<td>[81]</td>
</tr>
<tr>
<td>203.1</td>
<td>NbN\textsubscript{x}</td>
<td>[77]</td>
</tr>
</tbody>
</table>

Table 8.23 compiles the composition data from niobium nitride films, reactively sputtered at different powers.
Table 8.23: Comparison of compounds present in the nitride films reactively sputtered under different powers.

<table>
<thead>
<tr>
<th>Sputtering Power (W)</th>
<th>Analysis Location</th>
<th>Nb-N Compounds</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>NbN</td>
</tr>
<tr>
<td>800</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
<tr>
<td>1500</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
<tr>
<td>2000</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
<tr>
<td>2200</td>
<td>Surface</td>
<td>▲</td>
</tr>
<tr>
<td></td>
<td>Inside the Film</td>
<td>▲</td>
</tr>
</tbody>
</table>

The table shows that Nb2O5 was present on the surface of all the films. Oxynitrides were present both on the surface and within the films. Surface oxides were removed by Ar⁺ etching. Deeper into the film, the composition was non-stoichiometric nitride (NbNx) and oxynitrides. None of the sputtered films showed absolute NbN. The Nb/N ratio for the sputtering powers in Table 8.24 shows that as sputtering power increased the ratio became closer to 1. Since the current target power supply in XM-8 was limited to 2200 W, NbN was sputtered at 2200 W for all the wafers.

Table 8.24: Sputtering power versus Nb/N ratio.

<table>
<thead>
<tr>
<th>Power</th>
<th>Nb/N</th>
</tr>
</thead>
<tbody>
<tr>
<td>800</td>
<td>1.5</td>
</tr>
<tr>
<td>1500</td>
<td>1.4</td>
</tr>
<tr>
<td>2000</td>
<td>1.3</td>
</tr>
<tr>
<td>2200</td>
<td>1.3</td>
</tr>
</tbody>
</table>
Chapter 9: Niobium Anodization

This chapter discusses the features of Nb anodization. It begins with the anodization profile of niobium metal, then the conversion ratio of niobium metal into niobium oxide, the effect of anodization bath temperature on the formed film as well as on the anodization profile, and finally a color chart for oxide with anodization voltage.

9.1 Nb Anodization Profile

A typical anodization profile for niobium is shown in Figure 9.1. The anodization parameters were; anodization voltage — 83 V and current density — 0.5 mA/cm². The final current was 1 mA.

![Anodization profile of niobium](image)

**Figure 9.1: Anodization profile of niobium metal anodized to 83 V at 0.5 mA/cm² current density at room temperature.**

In the figure, the dotted line represents the variation of current with time and the solid line indicates the variation of voltage with time. Data were acquired every 15 seconds.
from the beginning until the end of anodization. The set voltage was reached in 8 minutes and 15 seconds. The voltage increase was linear with a slope of 0.14 V/second. This is also called the voltage growth rate. The oxide thickness formed when anodized at 83 V and 0.5 mA/cm² with an end current of 1 mA was 1900 Å. From this, the growth rate was calculated to be 22.9 Å/V. This growth rate was comparable to the value found in literature [3]. The color of the anodized film was pistachio green.

9.2 Nb → Nb₂O₅ Conversion Ratio

In order to calculate the metal to oxidation conversion ratio during anodization, two wafers were processed. In the first wafer, a definite thickness of Nb was sputtered. The second wafer was also sputtered with the same amount of Nb, using the same sputtering parameters. Then the second wafer was anodized at 83 V and 0.5 mA/cm² current density. The anodization was terminated when the current reached 1 mA. The conversion ratio can be determined if the Nb thickness prior to anodization and the Nb thickness after anodization are known. Therefore both the above mentioned wafers were imaged with TEM to obtain the Nb thickness information.

Figure 9.2 (a) and (b) show the cross-sectional view of the sputtered Nb metal and the anodized wafer with residual niobium and anodized oxide on top. In Figure 9.2 (a), the layers between Nb and platinum are gold and chromium. About 150 nm gold was evaporated to protect the Nb film from ion damage during sample preparation and Cr acted as an adhesion layer for gold. The thickness of the Nb metal was measured to be 5500 Å and that of the residual Nb was 4847 Å. Thus, 653 Å was converted into oxide. The oxide thickness was measured to be 1900 Å. Therefore, Nb → Nb₂O₅ conversion ratio was calculated to be 2.9.
Figure 9.2: Cross-sectional view of (a) sputtered Nb (b) anodized Nb wafer showing Nb$_2$O$_5$ and the residual Nb.

The conversion ratio is theoretically calculated below.

Number of moles of Nb consumed = Number of moles of Nb present in the oxide film

Equation (34)

\[
\text{Number of moles of Nb} = \frac{\text{Mass of Nb}}{\text{Molecular Weight of Nb}}
\]

Equation (35)

Number of moles of Nb present in the oxide film = \( \frac{\text{Mass of Nb present in the oxide film}}{\text{Molecular Weight of Nb}} \)

Equation (36)

Since every molecule of Nb$_2$O$_5$ contains 2 atoms of Nb,

\[
\text{Mass of Nb in Nb}_2\text{O}_5 = \text{Mass of Nb}_{2}\text{O}_5 \left( \frac{2 \times \text{Molecular Weight of Nb}}{\text{Molecular Weight of Nb}_{2}\text{O}_5} \right)
\]

Equation (37)
From Equation (36),

Number of moles of Nb in the oxide film

\[
\text{Mass of Nb}_2O_3 \left( \frac{2 \text{Molecular Weight of Nb}}{\text{Molecular Weight of Nb}_2O_3} \right)
\]

\[
= \text{Mass of Nb}_2O_3 \left( \frac{2}{\text{Molecular Weight of Nb}_2O_3} \right)
\]

Equation (38)

Mass = density \times volume

= density \times area \times thickness

Equation (39)

Or,

\[ M = \rho \times A \times d \]

Equation (40)

For Nb\(_2\)O\(_5\),

\[ M_{\text{Nb}_2O_5} = \rho_{\text{Nb}_2O_5} \times A_{\text{Nb}_2O_5} \times d_{\text{Nb}_2O_5} \]

Equation (42)

Similarly, for Nb,

\[ M_{\text{Nb}} = \rho_{\text{Nb}} \times A_{\text{Nb}} \times d_{\text{Nb}} \]

Equation (43)

From Equation (35) and Equation (38),

\[
\frac{\text{Mass of Nb}}{\text{Molecular Weight of Nb}} = \frac{\text{Mass of Nb}_2O_3 \left( \frac{2}{\text{Molecular Weight of Nb}_2O_3} \right)}{\text{Molecular Weight of Nb}}
\]

Equation (44)

\[
\left( \frac{M_{\text{Nb}}}{MW_{\text{Nb}}} \right) = M_{\text{Nb}_2O_3} \left( \frac{2}{MW_{\text{Nb}_2O_3}} \right)
\]

Equation (45)

From Equations (42) and (43),

\[
\left( \frac{\rho_{\text{Nb}} \times A_{\text{Nb}} \times d_{\text{Nb}}}{MW_{\text{Nb}}} \right) = \rho_{\text{Nb}_2O_5} \times A_{\text{Nb}_2O_5} \times d_{\text{Nb}_2O_5} \left( \frac{2}{MW_{\text{Nb}_2O_5}} \right)
\]

Equation (46)
\[ d_{\text{Nb}} = \frac{\rho_{\text{Nb}_2\text{O}_5} \times A_{\text{Nb}_2\text{O}_5}}{\rho_{\text{Nb}} \times A_{\text{Nb}}} \left( \frac{2MW_{\text{Nb}}}{MW_{\text{Nb}_2\text{O}_5}} \right) \times d_{\text{Nb}_2\text{O}_5} \]  
Equation (47)

Rearranging for \(d_{\text{Nb}_2\text{O}_5}\),

\[ d_{\text{Nb}_2\text{O}_5} = \frac{\rho_{\text{Nb}} \times A_{\text{Nb}}}{\rho_{\text{Nb}_2\text{O}_5} \times A_{\text{Nb}_2\text{O}_5}} \left( \frac{MW_{\text{Nb}_2\text{O}_5}}{2MW_{\text{Nb}}} \right) \times d_{\text{Nb}} \]  
Equation (48)

Assume, \(A_{\text{Nb}}\) and \(A_{\text{Nb}_2\text{O}_5} = 1\)

\(\rho_{\text{Nb}} = 8.57\ \text{g/cm}^3, \rho_{\text{Nb}_2\text{O}_5} = 4.47\ \text{g/cm}^3, MW_{\text{Nb}} = 92.9\ \text{g/mol}, MW_{\text{Nb}_2\text{O}_5} = 265.81\ \text{g/mol}\)

From Equation (48),

\[ d_{\text{Nb}_2\text{O}_5} = \frac{8.57 \times 1 \left( \frac{265.81}{2 \times 92.9} \right)}{4.47 \times 1} \times d_{\text{Nb}} \]

\[ = 2.74 \times d_{\text{Nb}} \]

Therefore, for 1 Å Nb forms 2.74 Å Nb\(_2\)O\(_5\).

According to these theoretical calculations, the conversion ratio is 2.74 Å. The ratio obtained from the thickness measurements was very close, 2.9 to this value. The difference may have been from the measurement error.

The terms are defined as follows.

Molecular weight of Nb\(_2\)O\(_5\) — \(MW_{\text{Nb}_2\text{O}_5}\)

Molecular weight of Nb — \(MW_{\text{Nb}}\)

Density of Nb — \(\rho_{\text{Nb}}\)

Density of Nb\(_2\)O\(_5\) — \(\rho_{\text{Nb}_2\text{O}_5}\)

Thickness of Nb — \(d_{\text{Nb}}\)

Thickness of Nb\(_2\)O\(_5\) — \(d_{\text{Nb}_2\text{O}_5}\)
9.3 Anodization to the End

From the anodization profile shown in Figure 9.1, the anodization current starts to decrease when the set voltage is reached. The current decreases rapidly initially and then decreases slowly once the current level reaches lower values. It continues to decrease very slowly with time, for currents <1 mA. An experiment was performed to see how low the current will go if the wafer was anodized for about 2 days. For that, a wafer was sputtered with 5500 Å Nb and was anodized at 83 V and 0.5 mA/cm² current density. The voltage and the current was monitored closely and the anodization profile is shown in Figure 9.3. Figure 9.3 (a) shows the profile in full time scale and (b) shows the profile in the first hour for a better view of the galvanostatic regime.

The set voltage was reached in 8 minutes and 15 seconds. Anodization then continued for 61 hours and 49 minutes (~2.5 days), which includes the time to reach 83 V. Like a typical plot, the current decreased and below 0.1 mA the rate of decrease was extremely slow. This low current indicated that the oxide film was almost perfect and there were very few oxygen vacancies. At the end of ~2.5 days, the current display was fluctuating among 0.01, 0.02, and 0.03 mA. The current stayed constant at these values for 40 hours and at the end of 40 hours, the wafer was taken out and rinsed. The color of the dielectric was yellow, very close to the color of gold indicating ~2500 Å thickness calculated based on the film color.

In the initial stages of potentiostatic regime, the current is mainly ionic (unless there is leakage). During the course of time, the oxygen vacancies in the film are filled and few vacancies are left. Therefore, the ionic current decreases with time and finally, it will reach a value close to zero. At this point, the total anodization current is the sum of ionic
current and leakage current through the oxide [69]. Thus, due to the presence of leakage current the anodization current will not reach zero, even though the ionic current is too small.

![Graphs showing anodization profile](image)

**Figure 9.3**: Anodization profile of Nb, anodized at 83 V and 0.5 mA/cm² in room temperature for ~2.5 days; 3 (a) full time scale for voltage and current (log scale) and 3 (b) first hour of anodization showing galvanostatic regime and the initial current decrease. Current is in log scale.
9.4 Effect of Anodization Bath Temperature

This section is a study of the effect of electrolyte temperature on the film properties and anodization profiles. Two anodization processes were performed for different anodization temperatures.

1. Cold Anodization: bath temperature ~ 1°C — 4°C
2. Hot Anodization: bath temperature ~ 61°C — 64°C

9.4.1 Fabrication

For the two anodizations, two wafers were fabricated. Thermally oxidized silicon wafers were used as the substrates. These wafers were backspattered and 5500 Å Nb was sputter deposited. Following sputtering, anodization was carried out under respective bath conditions. Both the wafers were anodized at 83 V and 0.5 mA/cm² current density and the process was terminated when the current reached 1 mA. In both hot and cold anodization, a range of temperature was used because of the difficulty in achieving precise temperature control.

9.4.2 Cold Anodization

Anodization was carried out at bath temperatures ~ 1°C — 4°C. The bath was maintained at this temperature using a technique similar to a double boiler. The anodization bath was placed inside another tank containing a mixture of ice and water. The temperature of the anodization bath was monitored continuously during the course of anodization. A schematic of the anodization setup is shown in Figure 9.4.
Figure 9.4: Anodization setup to maintain cold bath temperature.

The anodization profile for cold anodization is shown in Figure 9.5.

Figure 9.5: Anodization profile of a niobium wafer anodized at 83 V and 0.5 mA/cm² at 1°C — 4°C.

The anodization set voltage was reached in 6 minutes and 15 seconds and the total anodization time was 36 minutes and 44 seconds. The color of the anodized oxide was
bright blue indicating ~1100 Å thickness based on the film color. As mentioned earlier, this is only an approximation. A cross-sectional view of the anodized wafer is shown in Figure 9.6.

![Cross-sectional view of the wafer anodized at 1°C—4°C; (a) shows all the layers including top Pt, Au, Cr, Nb$_2$O$_5$, and Nb and (b) shows the anodized film and the thicknesses.](image)

**Figure 9.6:** Cross-sectional view of the wafer anodized at 1°C—4°C; (a) shows all the layers including top Pt, Au, Cr, Nb$_2$O$_5$, and Nb and (b) shows the anodized film and the thicknesses.

The oxide film thickness was 1320 Å. From the residual Nb thickness, the Nb→Nb$_2$O$_5$ conversion ratio can be calculated for low temperature anodization. From Figure 9.6 (a), the residual Nb was measured to be 4850 Å and the initial Nb sputtered thickness was 5500 Å. Therefore, 650 Å was converted into 1320 Å. Thus, the conversion ratio was 2.03. The double layers in the oxide were measured at 730 Å for the inner layer (layer close to Nb) and 590 Å for the outer layer. The electron diffraction pattern of the film is shown in Figure 9.7 and it shows that the film was amorphous.
9.4.3 Hot Anodization

The temperature of the bath was maintained between 61°C—64°C using a double boiler. The setup was similar to that shown in Figure 9.7 for cold anodization. Instead of ice and water, for hot anodization, the water was heated to ~ 60°C to bring the bath temperature to high levels. The anodization profile of Nb at high temperature is shown in Figure 9.8. The anodization set voltage was reached in 11 minutes and the total anodization time was 48 minutes. This is more than the time taken by the wafer anodized in the cold bath. The color of the anodized film was light yellow from normal incidence indicating a thickness of ~2500 Å.
Figure 9.8: Anodization profile of a niobium wafer anodized at 83 V and 0.5 mA/cm² at 61°C — 64°C.

The cross-sectional view of the anodized wafer, along with the SAD pattern of the oxide is shown in Figure 9.9. The oxide film thickness was 2170 Å. The double layers in the oxide were measured as 1480 Å for the inner layer (layer close to Nb) and 690 Å for the outer layer. From the residual Nb thickness, Nb—>Nb₂O₅ conversion ratio can be calculated for high temperature anodization. From Figure 9.9 (c), the residual Nb was measured to be 4860 Å. Therefore, the conversion ratio was 3.39. The electron diffraction pattern of the film in Figure 9.9 (d) shows the amorphous nature. Diffraction patterns were taken from both the layers of Nb₂O₅ and they were found to be the similar to the pattern shown in (d).
Figure 9.9: Cross-sectional view of the wafer anodized at 61°C—64°C; (a) shows all the layers including top Pt, Au, Cr, Nb$_2$O$_5$, and Nb and (b) shows the anodized film and the layer thicknesses, (c) shows the residual Nb and its thickness, and (d) diffraction pattern of the oxide.
9.4.4 Comparison of room temperature, low temperature, and high temperature anodization

Table 9.1 compares different parameters of low, room, and high temperature anodizations.

Table 9.1: Comparison of film properties and anodization profiles of low, room, and high temperature anodizations.

<table>
<thead>
<tr>
<th></th>
<th>Low Temperature, 1°C—4°C</th>
<th>Room Temperature, 20°C</th>
<th>High Temperature, 61°C—64°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide Thickness (Å)</td>
<td>1320</td>
<td>1900</td>
<td>2170</td>
</tr>
<tr>
<td>Oxide growth constant (Å/V)</td>
<td>16</td>
<td>23</td>
<td>26</td>
</tr>
<tr>
<td>Oxide Color</td>
<td>Bright blue</td>
<td>Pista green</td>
<td>Champagne</td>
</tr>
<tr>
<td>Crystal Structure</td>
<td>Amorphous</td>
<td>Amorphous</td>
<td>Amorphous</td>
</tr>
<tr>
<td>Nb→Nb₂O₅ Conversion Ratio</td>
<td>2.03</td>
<td>2.92</td>
<td>3.39</td>
</tr>
<tr>
<td>Total Anodization Time (min:sec)</td>
<td>36:44</td>
<td>39:30</td>
<td>48</td>
</tr>
<tr>
<td>Time to reach the set voltage, 83 V (min:sec)</td>
<td>6:15</td>
<td>8:15</td>
<td>11</td>
</tr>
</tbody>
</table>

Figure 9.10 shows the oxide colors for low, room, and high temperature anodizations.
Figure 9.10: Nb$_2$O$_5$ films anodized at (a) 1°C-4°C, (b) 20°C, and (c) 61°C-64°C.

The anodization profiles under three conditions are compiled in Figure 9.11.

Figure 9.11: Anodization profiles of Nb in cold, hot, and room temperatures.

The oxide thickness increases with anodization temperature, which indicates that the mobility of ions increases with temperature and can reach deeper into the Nb film to form the oxide. The difference between the inner layer thicknesses between hot and cold anodizations (100 Å) supports this. The color difference shown in Figure 9.10 is also an indicator of changing thickness with temperature.
The Nb—\(\rightarrow\)Nb\(_2\)O\(_5\) conversion ratio, based on the thickness difference, also increased with anodization temperature. From Section 9.2, conversion ratio calculations were made based on density and molecular weight of Nb and Nb\(_2\)O\(_5\). The results at different temperatures indicated a change in composition of the formed oxide. AES analysis of the oxide formed at room temperature had indicated the presence of carbon the formed oxide. As temperature increases, mobility of the ions also increases, thus incorporating more carbon at high temperatures than at low temperatures. The presence of carbon in the oxide film altered the film properties (density and molecular weight) used in Equation (48). This resulted in different conversion ratios at different temperatures.

Anodization takes place faster in low temperature electrolyte and it takes \(~36\%\) more time to complete anodization in a high temperature electrolyte. When hot, cold, and room temperature anodization profiles are plotted together, it can be seen that the cold anodization profile shows the highest voltage at a given time. This means that more voltage is required to maintain the constant current density. The lower mobility of ions at low temperatures therefore need higher field strength to maintain the given current density. Similarly, for hot anodization, the ionic mobility was high and the lower voltage was sufficient to maintain the desired current density. The rates of increase of voltage, during the galvanostatic regime for hot and cold were 0.12 and 0.15 respectively. The smaller slope or the voltage growth rate was again due to the increased mobility of ions at high temperatures.

The ionic movement during anodization can be modeled using the equation below.

\[
\text{Current density} = \text{ionic conductivity} \times \text{electric field} \quad \text{Equation (49)}
\]

Or,
Electric field, \( E \) was calculated from \( \frac{dV}{dh} \) (\( h \) – dielectric thickness), where ‘\( h \)’ was derived using Faraday’s law.

\[
h = \frac{Q \times M}{z \times F \times \rho \times A}
\]

Equation (51)

Where,

\( Q \) – Total charge went into the formation of the film (\( Q = \text{current} \times \text{time} \))

\( M \) – Molecular weight of the formed oxide

\( z \) – Electrons transferred; for \( \text{Nb}_2\text{O}_5 \), \( z = 10 \)

\( F \) – Faraday’s constant, 96500 C/mol

\( \rho \) – Density of formed oxide (\( \rho_{\text{Nb}_2\text{O}_5} = 4.47 \text{ g/cm}^3 \))

\( A \) – Area of anodization

‘\( h \)’ at different times were calculated and differential values were taken to calculate \( \frac{dV}{dh} \). Using a current density of 0.5 mA/cm\(^2\), the ionic conductivities at 1-4°C, 20°C, and 61-64°C were calculated and plotted in along with the measured thicknesses at each temperature.

Ionic conductivity, \( m \) can be written in the form of Arrhenius equation as,

\[
m = m_o e^{-E_a / kT}
\]

Equation (52)

Where,

\( m_o \) – conductivity coefficient

\( E_a \) – activation energy in Joules

\( k \) – Boltzmann’s constant, \( 1.38 \times 10^{-23} \text{ J/mol.K} \)

\( T \) – Temperature in Kelvin
Equation (52) can be rewritten as,

\[ \ln m = \ln m_o - \frac{E_a}{kT} \quad \text{Equation (53)} \]

By plotting \( \ln m \) as a function of \( 1/T \), \( m_o \) and \( E_a \) can be calculated. The plot is shown in Figure 9.12 and the fitted equation gives \( m_o \) as 16.70 S/m. \( E_a \) was calculated as follows.

\[
\frac{E_a}{k} = -496.85
\]

\[
E_a = -496.85 \times 1.38 \times 10^{-23} = 6.86 \times 10^{-21} \text{ J} = 43 \text{ meV}
\]

Thus, the experimentally determined activation energy for ionic conductivity in anodization was 43 meV. Figure 9.13 compares the conductivities and thicknesses at different temperatures and they follow similar trends.

**Figure 9.12: Arrhenius plot of ionic conductivity for 4°C, 20°C, and 64°C.**
Figure 9.13: (a) Nb$_2$O$_5$ thickness and (b) ionic conductivity as a function of temperature.

Current efficiency was calculated for room temperature anodization by comparing the measured thickness and the thickness calculated using Faraday’s law and was found to be 97.83%.

9.5 Color Chart of Anodic Nb$_2$O$_5$ Films

Anodized niobium oxides show beautiful colors according to the voltage used for anodization. These colors can be used to determine the approximate thickness of anodized films, if the anodization voltage is known. Here, seven voltages were used to form oxides of thickness ranging from 1900 Å to 5000 Å.

Thermally oxidized 125 mm diameter silicon wafers were used as the substrates. They were rinsed thoroughly with DI water and rinsed and dried in an SRD. The substrates were subjected to dehydration bake at 110°C for two minutes on a hot plate. This was an important step prior to sputtering, as any amount of moisture could adversely affect film adhesion. After dehydration bake, the substrates were loaded into the sputtering chamber and were cleaned using RF plasma for two minutes. This process also improved film adhesion by roughening the substrate surface. Next, a niobium film
of 5500 Å was deposited at 2200 W sputtering power, and 5 mTorr gas pressure. A sputtering time of 125 seconds was used, with 5 passes at 25 seconds/pass and two minutes waiting time in between the passes to let the wafer cool down from prolonged exposure to plasma. For the seventh wafer 6600 Å of niobium was sputtered instead of 5500 Å, since the niobium film was to be anodized to form a 5000 Å oxide. Once the sputtering was finished, the substrates were left to cool in the sputtering chamber for 10 minutes to relieve thermal stresses induced during deposition. The anodization parameters are shown in Table 9.2. Here, for each voltage, a single wafer was processed.

### Table 9.2: Anodization parameters for the color chart of Niobium oxide films.

<table>
<thead>
<tr>
<th>Wafer No.</th>
<th>Current Density (mA/cm²)</th>
<th>Final Current (mA)</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5</td>
<td>1</td>
<td>83.0</td>
</tr>
<tr>
<td>2</td>
<td>0.5</td>
<td>1</td>
<td>109.2</td>
</tr>
<tr>
<td>3</td>
<td>0.5</td>
<td>1</td>
<td>131.0</td>
</tr>
<tr>
<td>4</td>
<td>0.5</td>
<td>1</td>
<td>152.8</td>
</tr>
<tr>
<td>5</td>
<td>0.5</td>
<td>1</td>
<td>174.7</td>
</tr>
<tr>
<td>6</td>
<td>0.5</td>
<td>1</td>
<td>196.5</td>
</tr>
<tr>
<td>7</td>
<td>0.5</td>
<td>1</td>
<td>218.3</td>
</tr>
</tbody>
</table>

From the table, it can be seen a constant current density of 0.5 mA/cm² was used, e.g., for a 125 mm diameter wafer, the current was 61 mA. As mentioned previously, anodization was done in a mixture of tartaric acid-ethylene glycol-water at room temperature and no stirring was employed. The same electrode, platinized titanium, was used as the cathode. The anodization was terminated when the final current reached 1 mA.

The thickness of the first wafer, anodized at 83 V, was analyzed by TEM imaging and was found to be 1900 Å. Thus, a growth rate of 22.9 Å/V was obtained. This growth rate agreed well with the growth rate mentioned in the literature, 24 Å/V [3, 79]. Also,
23 Å/V have been reported in [82]. More details on the anodized film can be found in Chapter 8. The voltages for the rest of the wafers were selected to obtain thicknesses from 2500 Å to 5000 Å at 500 Å intervals. All the thicknesses were calculated based on a growth rate of 22.9 Å/V. For sample calculation, 109.2 V will give an oxide film of thickness of 2500 Å at a rate of 22.9 Å/V growth.

The anodization profiles of the seven films are shown in Figure 9.14. The anodization profiles are plotted for voltages from 83 V to 218.3 V.

![Figure 9.14: Anodization profiles of seven wafers anodized from 83 V to 218.3 V.](image)

In these typical anodization profiles, initially, the voltage increased from 0 V to the set point while the current stayed constant at 61 mA. During the second segment, the current dropped exponentially from 61 mA once the voltage reached the set point. These profiles showed an average slope of 9.6 V/min in the galvanostatic regime. Total
anodization time was taken as the time from 0 V to reach the final current of 1 mA. The total anodization time, the time to reach the set voltage, calculated thicknesses based on the growth rate from TEM thickness analysis, and the color of each wafer are shown in Table 9.3. These values are plotted in Figure 9.15 and Figure 9.16. Figure 9.15 shows the time to reach the anodization set voltage as a function of anodization voltage. The anodic oxide thickness as a function of voltage is shown in Figure 9.16.

Table 9.3: The anodization times, thicknesses, and the colors of the wafers.

<table>
<thead>
<tr>
<th>Wafer No.</th>
<th>Total Anodization Time (min.)</th>
<th>Time to reach Anodization Set Voltage (min.)</th>
<th>Calculated Thickness (Å)</th>
<th>Voltage (V)</th>
<th>Color of the Dielectric</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Voltage (TEM)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>38.80</td>
<td>8.50</td>
<td>1900</td>
<td>83.0</td>
<td>Pista green</td>
</tr>
<tr>
<td>2</td>
<td>52.78</td>
<td>10.80</td>
<td>2500</td>
<td>109.2</td>
<td>Light purple</td>
</tr>
<tr>
<td>3</td>
<td>61.10</td>
<td>13.50</td>
<td>3000</td>
<td>131.0</td>
<td>Dark green</td>
</tr>
<tr>
<td>4</td>
<td>70.00</td>
<td>16.00</td>
<td>3500</td>
<td>152.8</td>
<td>Rose</td>
</tr>
<tr>
<td>5</td>
<td>79.25</td>
<td>18.25</td>
<td>4000</td>
<td>174.7</td>
<td>Dark rose</td>
</tr>
<tr>
<td>6</td>
<td>102.25</td>
<td>20.50</td>
<td>4500</td>
<td>196.5</td>
<td>Light green</td>
</tr>
<tr>
<td>7</td>
<td>94.70</td>
<td>23.75</td>
<td>5000</td>
<td>218.3</td>
<td>Light purple</td>
</tr>
</tbody>
</table>
The figure shows the expected linear increase of anodization time with increases in anodization voltage. It also shows that an average time of 2.6 minutes was taken for a 500 Å increase in thickness.

Figure 9.16: Anodic oxide thickness versus anodization voltage for a final current of 1 mA.
Figure 9.16 shows the increase in oxide thickness with anodization voltage. The figure shows a linear increase of anodic oxide thickness with anodization voltage, indicating that the mobility of ions increased with increasing field. The color bar (colors viewed normal to the surface) with film thicknesses is shown in Figure 9.17.

![Color bar of Nb$_2$O$_5$ films according to their thicknesses.](image)

**Figure 9.17: Color bar of Nb$_2$O$_5$ films according to their thicknesses.**

The pictures of the wafers are shown in Figure 9.18. The colors have been slightly altered by camera reflection. Since different angles give different reflections, care has been exercised while obtaining these images in a consistent manner.
Figure 9.18: Nb$_2$O$_5$ films anodized at (a) 83 V, (b) 109.2 V, (c) 131.0 V, (d) 152.8 V, (e) 174.7 V, (f) 196.5 V, and (g) 218.3 V to a final current of 1 mA.
Chapter 10: Niobium Capacitors

This chapter discusses the capacitors fabricated with Nb$_2$O$_5$ dielectric. Initially, capacitors were fabricated using anodized Nb$_2$O$_5$. The rest of the capacitors were fabricated using a combination of reactive sputtering and anodization, and reactive sputtering of Nb$_2$O$_5$, followed by anodization of Nb metal sputtered on the oxide. Capacitors were fabricated with and without NbN and the results are compared.

10.1 Capacitors with anodized dielectric

Niobium capacitors were initially fabricated with anodized niobium. The results obtained are discussed below.

10.1.1 Fabrication

The test vehicle contained an array of 4410 capacitors of 1 mm $\times$ 1 mm size. The substrate used was a 125 mm wafer of p-type Si (111). These capacitors were fabricated with a niobium oxide dielectric, which was formed by anodizing the sputtered metal. The fabrication steps of these capacitors follow:

The silicon substrate was thermally oxidized to form 2 $\mu$m silicon dioxide. Thickness of the oxide was measured by using a Nanospec reflectometer. Back sputtering was done prior to subsequent processing to ensure a clean wafer surface and to roughen the surface for better film adhesion. A 500 Å titanium, a 2 $\mu$m copper bottom plate, and 5500 Å niobium metal were sputtered in order. The initial titanium film was sputtered to improve adhesion between silicon dioxide and copper. Then, the wafer was anodized in a tartaric acid-ethylene glycol-deionized water electrolytic mixture to 83 V at a current density of 0.5 mA/cm$^2$. Anodization was stopped when the current reached 1 mA,
resulting in a pale green niobium oxide dielectric. Total time for anodization was about 41 minutes, out of which the galvanostatic regime lasted for the initial 8 minutes.

Following anodization, a top copper plate of 2 μm thickness was sputtered on the dielectric. The top plate copper was patterned with a 2.5 μm AZ4110 resist and copper etching was performed. Photoresist was then stripped off the wafer using acetone and resist strip, AZ300T at 90°C. The bottom plate contact was formed by removing a small dielectric area, close to the top edge of the wafer, as in Chapter 7, and about 1 μm thick copper was sputtered in that area with the shadow mask covering the rest of the wafer. The test vehicle fabrication was completed and the final capacitor structure is shown in Figure 10.1. Residual niobium can be seen under the green Nb2O5 dielectric.

![Figure 10.1: Schematic of the cross-section of anodized Nb2O5 capacitors.](image)

### 10.1.2 Results & Discussion

A Two Probe Robotic Micro Tester was used for capacitance measurements. The capacitance plot over the entire wafer is shown in Figure 10.2.
Figure 10.2: Capacitance data of anodized Nb$_2$O$_5$ capacitors with copper top and bottom plates.

As mentioned before, the tester made use of two probes, Probe 1 and Probe 2, in which the former is connected to the ground whereas the latter is connected to the device to be measured. The probes switch their positions when the two crossed each other. The figure shows a high capacitance area and a zero capacitance area. The switching of the probes (in effect, polarity change) caused large variations in the measured capacitance, which can be thought as reverse biasing a junction capacitor (like PN junction) and the capacitance values were beyond the measurement range of the probes, thus showing no measurements. The data showed that the capacitance values increased towards the
center, reaching 8 nF, except that the exact center region, where all capacitors were shorted. What happened to this wafer may be explained as follows.

Prior to top plate sputtering, niobium and the oxide looked like Figure 10.3 (a). But, during top plate sputtering, the heat from the plasma caused the oxygen from Nb₂O₅ to diffuse into niobium metal, thinning the effective dielectric [refer to Figure 10.3 (b)]. This thickness reduction caused an increase in the measured capacitance. The wafer center became so thin that shorts developed. The reason for the prominent effect at the wafer center is that the center of the wafer is located directly under the target, thus susceptible to more material deposition or high temperature compared to other areas of the wafer.

Figure 10.3: Niobium/Nb₂O₅ interface (a) before sputtering and (b) after sputtering.

The measured capacitances outside of the unusual center region showed an average capacitance of 2.6 nF. This gave a calculated dielectric constant of ~55, which was 34% more than the literature value of $k \sim 41 \ [3]$ which is not possible. This higher capacitance than normal indicated oxygen diffusion from the dielectric to the underlying niobium metal and that the effective thickness of the dielectric was less than 2000 Å.
10.2 Solutions to Oxygen Diffusion for the Anodized Dielectric

One way to avoid oxygen diffusion from the dielectric to the niobium metal would be to completely anodize the sputtered niobium. Literature shows that one-third of the oxide grows into the metal and two-thirds of the oxide grows out [79]. Therefore, a thinner niobium layer was deposited for anodization. In addition, a diffusion barrier was sputtered above and below the anodized dielectric to prevent oxygen diffusion. 500 Å NbN barrier layer was sputtered above and below the anodized dielectric, with 1500 Å of niobium instead of 5500 Å sputtered for anodization. Exact thickness control was difficult with sputtering. The process flow is shown in Figure 10.4.

![Flowchart](image)

Figure 10.4: Process flow for capacitors with anodized dielectric and NbN diffusion barrier.
Testing showed that all the capacitors were found to be shorts. There were two possible causes, oxygen diffusion from the plasma heating during sputtering and reactive ion etching, or the quality of the anodized dielectric. Also, incomplete removal of NbN could lead to false measurements; but complete NbN removal was confirmed by measuring the thickness removed after RIE using profilometry.

The oxygen diffusion during sputtering was tested by carrying out a simple experiment. A sample wafer was prepared depositing Ti (500 Å) / Cu (2 µm) / Nb (1500 Å) and anodizing niobium at 83 V to a final current of 1 mA. As the top plate, 2 µm copper was sputtered and was pattern-etched in a mixture of copper sulfate, sulfuric acid, and hydrogen peroxide at 25°C. Once the capacitors were completed, top copper was completely etched away and the resistance of the dielectric was measured with a multimeter. Most areas measured resistance as low as 2 Ω. The wafer was re-anodized and the total anodization time (time to reach 1 mA) was 2 minutes and 54 seconds. This says that the oxide film became deficient in oxygen after processing. Once again, the top plate (Ti/Cu) was sputtered and pattern-etched. Then, the top metal was etched away and resistance measurements were taken. The measured resistances were 0.7 – 0.9 Ω. Re-anodization took longer than before, with a total anodization time of 9 minutes and 16 seconds. Afterwards, the dielectric was tested for resistance and good insulation was obtained. This proved that sputtering drove oxygen away from the oxide film.

This was confirmed by doing another test, in which the anodized dielectric was stored in the furnace in N₂ for 6 hours and 30 minutes at 250°C. Surface resistance was measured before and after storage and it was found that the dielectric became resistive after being in the furnace. For verification, the wafer was re-anodized, which took 1
minute and 30 seconds, which was a short time compared to the re-anodization time of 9 minutes for the Ti/Cu sputtered wafer. This meant that the sputter heating reached more than 250°C. Therefore, the process of sputter depositing the diffusion barrier and the patterning by RIE posed problems due to plasma heating.

As far as the anodized dielectric was concerned, XPS data has shown that the anodization produces 100% Nb$_2$O$_5$. Since the desired composition was produced, the next thing to look at was the anodization bath. It was possible that the pH was not correct and was producing porous oxide films causing premature dielectric breakdown. The pH of the bath was analyzed and was found to be 2.2, which is in the acidic range. The bath pH was modified by adding ammonium hydroxide (NH$_4$OH), which brought the pH up to 5.6, closer to the neutral level. The AFM (AFM, Digital Instruments: NanoScope III) images of the Nb$_2$O$_5$ films anodized at 83 V in tartaric acid-ethylene glycol-DI water bath, at pH=2.2 and pH=5.6 (with NH$_4$OH) are shown in Figure 10.5.

![Figure 10.5: AFM images showing surface morphology of Nb$_2$O$_5$ films at (a) pH = 2.2 and (b) pH = 5.6.](image-url)
The surface was scanned in a \(1 \mu m \times 1 \mu m\) area at a scan rate of 0.4 Hz using silicon cantilevers in tapping mode. It is evident that the grain size increased as the pH of the solution increased. The average grain size changed from 85 nm at pH=2.2 to 200 nm at pH=5.6. However, the capacitance data taken from the films formed under the 5.6 pH conditions did not show any improvement when compared to the 2.2 pH condition capacitors.

To find out if the problem was the anodization bath, a new anodization bath was prepared with ammonium pentaborate and ethylene glycol. This recipe was based on mixing 9 g of ammonium pentaborate in 100 ml of ethylene glycol [83]. A new wafer was prepared by sputtering Ti (500 Å) / Cu (2 μm) / Nb (1000 Å) and anodized at 83 V. Top plates were sputtered at 500 W, instead of 3000 W. However, the tests showed all shorts, indicating oxygen diffusion.

The following paragraphs explain different techniques that were tried to avoid sputtering or sputter heating.

1. **Lower sputtering power:** Top plates were sputtered at a power as low as 200 W. But, this resulted in shorted capacitors.

2. **Electroplating copper instead of sputtering:** Electroplating needs to have an initial seed layer. For copper, it had to be sputter deposited. One wafer was fabricated with seed sputtered at 200 W and electroplated to form 2 μm copper top plates. Again, this option resulted in shorted capacitors.

3. **Sputtering system with backside wafer cooling:** The sputtering system previously used, Varian XM-8, did not have wafer cooling, so the metal was deposited for short times (20-25 seconds) with 2 minutes breaks in between. The next wafer was prepared in
a sputtering system, the Varian 3180, with backside wafer cooling. The first wafer was copper sputtered at 550 W for 180 seconds to form a seed layer and was then electroplated to form a 2 μm thick top plate. The wafer overheated due to the prolonged exposure to plasma and resulted in shorted capacitors. The second wafer was sputtered for a total of 180 seconds, but was done in 6 passes with 30 seconds each pass. Plating followed, but again resulted in shorted capacitors.

4. ‘Pulse’ sputtering: The metal was sputtered in pulses, for 5 seconds, with 2 minutes wait to cool the wafer. The steps were repeated until the desired thickness (2 μm) was reached. This was done at 500 W, in the Varian 3180 sputterer, which had backside cooling. This also resulted in shorted capacitors.

5. Nb₂O₅ with diffusion barrier: This technique was explained before. The downside to this method was that the process of depositing the NbN diffusion barrier, itself was reactive sputtering. NbN was largely produced at powers >2000 W. Also, NbN patterning was done in plasma (RIE). Both of these steps overheat the wafer and cause oxygen diffusion. Therefore, depositing a diffusion barrier on top of the dielectric could not be done with sputtering.

Since none of the above solutions worked, alternatives for sputtering were examined. The final technique was to evaporate top plates instead of sputtering. Evaporation is done in an ultra high vacuum chamber. This technique keeps the wafer relatively cool compared to sputtering. Our choice of material was aluminum, as it was the only material in the evaporator to which we had access at that time. The fabrication of capacitors with evaporated top plates is explained below.
A 125 mm thermally oxidized silicon wafer was RF etched for 60 seconds and Ti (500 Å) / Nb (1000 Å) were sputtered. As before, titanium was the adhesion promoter between the oxide and niobium. Here, niobium acted as the bottom plate metal. The niobium thickness was calculated according to the one-thirds in, two-thirds out oxide growth. Based on that, when a 2000 Å oxide was grown, ~700 Å niobium was consumed. Since it was difficult to control the exact thickness deposited during sputtering and due to sputter non-uniformity, ~400 Å extra material was sputtered to ensure that the desired metal thickness (~700 Å) was reached over the entire wafer. After niobium sputtering, the wafer was immediately moved to the anodization bath to minimize surface oxidation, which forms a porous oxide. The anodization was performed at 83 V and 0.5 mA/cm². The process was terminated when the current reached 0.92 mA. The top plates were evaporated in an EDWARDS AUTO 306 evaporator. The deposition rate was maintained at 1.5 nm/second by controlling the current. A total of 4500 Å was evaporated. Patterning followed with 2.5 µm AZ4110 photoresist. The top metal was etched in a solution of phosphoric acid (65%), acetic acid (5%), sodium-M-nitrobenzene sulfonate (10%), and DI water (20%) at 50°C. A Dektak profilometer was used before and after etching to obtain the exact thickness of evaporated aluminum and was found to be ~6000 Å. The photoresist was removed first with acetone, then with AZ300T hot strip bath at 90°C for 8 minutes. The wafer was tested with the Two Probe Tester and the data is shown in Figure 10.6.
Figure 10.6: Capacitance data of anodized Nb$_2$O$_5$ capacitors with evaporated aluminum top plates.

The true average capacitance was calculated from the left hand side data to the step and was calculated to be 2.07 nF. As explained earlier in the dissertation, true average capacitance is the measured capacitance obtained when correct polarity (top plate to ground and bottom plate to positive bias) was applied to the capacitor. There were a total of 4 shorts and the functional yield was calculated to be 99.91%. The raised edge in the plot, in the top right hand side, showing higher capacitance indicates possible oxygen diffusion from the dielectric. This was due to the positioning of that edge directly over the evaporation source. Compared to the capacitances in the other areas, only a difference of 0.1 — 0.2 nF was observed for the raised edge. A few capacitors were sampled and tested for breakdown strength and the capacitors could withstand up to 10
V. Finally, the solution with evaporated top plates for preventing oxygen diffusion worked successfully.

To test for oxygen diffusion, the wafer was stored in the furnace in N₂ at 100°C for 8 hours. The test results are shown in Figure 10.7.

![Figure 10.7: Capacitance data for anodized Nb₂O₅ capacitors with evaporated aluminum top plates in N₂ after 100°C for 8 hours.](image)

The capacitance values were increased by 4—18% after thermal storage. This meant that oxygen diffusion took place into the residual niobium that was acting as the bottom plate. The higher capacitance edge has been destroyed completely, which confirms the initial oxygen diffusion from heating due to proximity.

The initial data confirmed that evaporation works for depositing top plates without causing oxygen diffusion. But, having residual niobium in the structure will allow oxygen diffusion that is detrimental to the device performance. Since it is difficult to obtain just enough niobium to produce 2000 Å dielectric precisely with sputtering, Nb₂O₅
must be directly sputtered as the dielectric, which will eliminate the possibility of having residual niobium after anodization due to sputter nonuniformity. Therefore, as proposed, the dielectric was reactively sputtered and then anodized to fill the oxygen deficient areas of the dielectric.

10.3 Capacitors with reactively sputtered and anodized dielectric

A TEM analysis proved that an anodization voltage of 83 V and a final current of 1 mA at a current density of 0.5 mA/cm$^2$ produced 1900 Å thick dielectric. The thickness characterization of Nb$_2$O$_5$ at 500 W and 10 mTorr Ar/O$_2$ pressure gave a deposition rate of 1.74 Å/second. Therefore, capacitors were fabricated with and without NbN using ~2000 Å dielectric.

10.3.1 Reactively Sputtered and Anodized Dielectric with NbN

Dielectric films were reactively sputtered at 500 W as well as 200 W, as initial XPS analysis showed that both powers give desired Nb$_2$O$_5$.

**Dielectric Reactively Sputtered at 500 W**

**Fabrication:**

A thermally oxidized 125 silicon wafer was backsputtered and Ti (500 Å) / Cu (2µ) / NbN (500 Å) / Nb$_2$O$_5$ (2088 Å) were sputtered in order. The sputtering conditions are shown in Table 10.1.

**Table 10.1: Sputtering parameters for the adhesion layer, bottom plate, diffusion barrier, and the dielectric layer.**

<table>
<thead>
<tr>
<th>Material</th>
<th>Power (W)</th>
<th>Gas(es)</th>
<th>Pressure (mTorr)</th>
<th>Time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>2500</td>
<td>Ar</td>
<td>5</td>
<td>20</td>
</tr>
<tr>
<td>Cu</td>
<td>3000</td>
<td>Ar</td>
<td>5</td>
<td>160</td>
</tr>
<tr>
<td>NbN</td>
<td>2200</td>
<td>Ar/N$_2$</td>
<td>5</td>
<td>25</td>
</tr>
<tr>
<td>Nb$_2$O$_5$</td>
<td>500</td>
<td>Ar/O$_2$</td>
<td>10</td>
<td>1200</td>
</tr>
</tbody>
</table>
The oxide was then anodized at 83 V and 0.5 mA/cm² current density. The anodization profile is shown in Figure 10.8.

Figure 10.8: The anodization profile of a 2088 Å Nb₂O₅ film, reactively sputtered at 500 W in Ar:O₂ (90:10) gas mixture for 1200 seconds.

The time to reach 83 V was 3 minutes and 30 seconds; the anodization was stopped at 6.7 mA, six minutes into the process, when a strong gas evolution was observed from the surface of the wafer. Gas evolution is associated with dielectric breakdown, with oxygen, or steam, or both being evolved during breakdown. Steam evolves from localized heating of the oxide surface leading to vaporization of water present in the electrolyte.

When sputtered niobium was anodized, the time to reach 83 V was about 8 minutes. Here, the set voltage was reached in 3 minutes and 30 seconds. If complete Nb₂O₅ had formed by reactive sputtering, the set voltage would have reached in less than 1 minute. Based on that, only about 43% of the oxide was perfect. When compared to the anodization profile of sputtered niobium, this oxide anodization profile showed a non-
linear voltage increase initially. This meant that the dielectric layer close to the surface was anodized slowly compared to the inner layers. XPS analysis showed that the surface consists of Nb₂O₅ and NbO₂. One speculation is that the NbO₂ $\rightarrow$ Nb₂O₅ conversion was difficult or slower compared to the inner layer consisting of NbO. As mentioned earlier, it has been shown that NbO can form a continuous Nb₂O₅ layer. Figure 10.9 shows the picture of the wafer after anodization.

![Image](image_url)

**Figure 10.9: The 2088 Å Nb₂O₅ after anodization at 83 V and 0.5 mA/cm².**

Since aluminum scavenges the oxygen from Nb₂O₅ during heat treatment, it was decided to replace the aluminum top plates with gold. In order to test the wafers with the Two Probe Tester, it was necessary to have a thicker top plate, ~ 2 µm. Since it is not economical to use 2 µm gold, the top plate was designed to have Cr (100 Å) / Au (500 Å) / Ni (2 µm) / Cr (100 Å) / Au (500 Å) in that order. Thus, after anodization, Cr and Au were evaporated and nickel was plated after patterning using the plating mask, followed by Cr and Au evaporation.
Results & Discussion:

The wafer was tested using the Two Probe Tester and the results are shown in Figure 10.10.

Figure 10.10: The capacitance data of the reactively sputtered and anodized dielectric with NbN.

The capacitances ranged from 1.06 nF to 2.45 nF from the edge towards the center. Then, at the center, the capacitance decreased to 1.7 nF. This change of capacitance was a result of dielectric thickness variation across the wafer, as evidenced by the color of the dielectric after anodization (refer to Figure 10.9). The sputtered material was thicker in the center and the edges compared to the other areas of the wafer. When the wafer was anodized, anodization occurred only up to 1900 Å of the dielectric. So, there was residual sputtered oxide in the center and the edges, giving lower capacitances. Out of 4410 capacitors, 32 were found to be shorts and the values ranged from 3 to 231 Ω. The functional yield was calculated to be 99.27%.
Dielectric Reactively Sputtered at 200 W

Fabrication:

A thermally oxidized silicon wafer was backspattered and Ti (500 Å)/Cu (2 μm)/Ti (500 Å)/NbN (500 Å)/Nb_2O_5 (3400 Å) layers were sputtered. The sputtering parameters were the same as given in Table 10.1, except for the sputtering power and total sputtering time. The oxide film was sputtered at 200 W and the sputtering time was 6000 seconds. A thicker Nb_2O_5 was sputtered to compensate for sputter non-uniformity across the wafer.

As mentioned in Chapter 3, before reactive sputtering, the chamber was flushed with the respective gas combination to saturate the chamber with the needed gas, and after sputtering the chamber was flushed with pure Ar to remove any trace of reactive gases. Once sputtering was finished, the wafer was left in the chamber for 10 minutes to relieve all the thermal stresses and to bring the wafer to room temperature. The color of the sputtered dielectric was a combination of purple center, green circular area around the center, and an outer purple area on the edge of the wafer. Based on these colors, the thickness difference between purple and green Nb_2O_5 film was derived and was found to be ~200 Å. This pattern was in a concentric circle fashion. The sputtered dielectric was anodized at 83 V and a current density of 0.5 mA/cm^2 was used. The set voltage was reached in 2 minutes and 30 seconds and the process was terminated at 2.54 mA, when the current started to increase. This indicated a decrease in the resistance of the oxide film, which meant that the film was breaking down. This meant that the anodization voltage was close to the breakdown voltage of the sputtered oxide and the breakdown occurred from spending 29 minutes at a voltage close to the breakdown voltage. The
total time of anodization was 29 minutes. The anodization profile is shown in Figure 10.11.

![Anodization Profile](image)

**Figure 10.11**: Anodization profile of a 3400 Å Nb$_2$O$_5$ reactively sputtered at 200 W.

The color of the dielectric after anodization was bright orange color indicating a thickness of ~3000 Å based on the interference color. The film had large defects distributed over the wafer. The SEM image of one of the defects is shown in Figure 10.12.
Figure 10.12: Dielectric breakdown during anodization of Nb$_2$O$_5$ reactively sputtered at 200 W.

The defect was about 57 μm long and wide. Different areas were identified in the defect based on EDS analysis. Dielectric breakdown in niobium oxide films can be either electrical or mechanical. Electrical breakdown occurs by an electron avalanche. The electrons are accelerated through the oxide after gaining sufficient energy from the applied electric field. In their path, they collide with other atoms, ionizing them to cause an electron avalanche. The breakdown site is normally seen as a rupture like the one in Figure 10.12. Mechanical breakdown occurs in the bulk of the film due to an increase in tension of the film. The difference in composition and structure of the oxide film gives rise to stresses within the film. A pure mechanical breakdown site is seen as a fissure or crack in the dielectric. Dielectric breakdown can be due to electrical or mechanical failure or both in the same anodization process [38]. As was previously shown, cracks
can develop between layers even in the oxide layer (see Figure 8.35). The defect shown in Figure 10.12 was a result of electrical breakdown.

Another wafer was repeated with the same process parameters, and anodization was done at 70 V, instead of 83 V. A current of 56.5 mA instead of 61 mA was used. The idea was to anodize gradually; anodize a thin layer, increase the voltage and anodize a little more thickness and so on. In this case, again the anodization was not successful. The voltage reached 70 V in 2 minutes and 45 seconds. The defects started to form when the current reached 19.34 mA. Total time for anodization was 4 minutes. 4500 Å of aluminum was then evaporated to form the top plates. The capacitance data from the Two Probe Tester is shown in Figure 10.13.

![Figure 10.13: Capacitance data with Nb₂O₅ reactively sputtered at 200 W and anodized to 70 V.](image)

The data shows many shorts, which was expected, as the anodization was incomplete. There were 38 shorts and they ranged from 0.5 Ω to 177 kΩ. The bowl shape was
noticeable. Lower capacitance occurs at the edge, then higher capacitance, and the capacitance falls off at the center. The capacitance values ranged from 2.1 to 3.6 nF. This capacitance variation across the wafer could be attributed to sputter nonuniformity.

10.3.2 Reactively Sputtered and Anodized Dielectric without NbN

Fabrication

Like the wafer with NbN, a thermally oxidized silicon wafer was back sputtered and Ti (500 Å) / Cu (2 µm) / Nb$_2$O$_5$ (2088 Å) layers were sputtered. Sputtering conditions were maintained the same as the wafer in Section 10.3.1. The color of the sputtered dielectric was light purple with a green center indicating a thickness difference of ~200 Å from calculations based on the film colors. Following Nb$_2$O$_5$ sputtering, the wafer was anodized at 83 V and 0.5 mA/cm$^2$ current density. During anodization, dielectric breakdown occurred when the voltage reached 51 V. Anodization was terminated when the current reached 24 mA. Before and after pictures of the wafer are compared in Figure 10.14.

![Reactively sputtered dielectric without NbN](image)

(a) (b)

Figure 10.14: Reactively sputtered dielectric without NbN (a) before anodization and (b) after anodization.
The images of different areas of the post anodized wafer are shown in Figure 10.15.

![Figure 10.15: Reactively sputtered dielectric without NbN after anodization showing defect concentration (a) just outside the center circle (rim area) (b) just outside the rim (c) further away.](image)

The center of the wafer showed no defects, suggesting that area was anodizing well. The rim, just outside the center as seen in Figure 10.15 (a), had the maximum concentration of defects. The defect concentration decreased when moved away from the center. Also, notice the color change of the dielectric from the left image to the rightmost. This indicated a difference in thickness in all three regions. Correlating this to the capacitance data of the wafer with NbN, the capacitance changed from a lower value to higher value and then to a lower value when moving from the periphery to the center of the wafer. Thus, starting from the periphery, moving inward, the dielectric was first thicker, then thinner, and thicker when the center was reached. This non-uniformity gave rise to non-uniform capacitances even after anodization. Table 10.2 relates the capacitance, dielectric thickness, and defect density of this wafer.
Table 10.2: Table relating the wafer position, dielectric thickness, capacitance, and defect density.

<table>
<thead>
<tr>
<th>Position</th>
<th>Dielectric Thickness</th>
<th>Capacitance</th>
<th>Defect Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer edge</td>
<td>Thick</td>
<td>Low</td>
<td>Low</td>
</tr>
<tr>
<td>Between wafer edge and the center</td>
<td>Thin</td>
<td>High</td>
<td>High</td>
</tr>
<tr>
<td>Center</td>
<td>Thick</td>
<td>Low</td>
<td>Low-None</td>
</tr>
</tbody>
</table>

Microscopic inspection of a defect spot in the dielectric is shown in Figure 10.16.

![Microscopic inspection of a defect spot in the dielectric](image)

Figure 10.16: Nb$_2$O$_5$ dielectric breakdown during anodization, identifying each layer on the wafer.

It showed that the dielectric was severely damaged during anodization. Based on EDS analysis, the composition of each area was identified and is marked in the figure. This defect was similar to the previous one shown in Figure 10.12. When the oxide broke down, copper came in contact with the electrolyte. As ethylene glycol/water mixture is known to be corrosive for copper, the copper plate was dissolved [84]. Finally, it exposed the silicon dioxide.
Sputtering thicker films to overcome sputtering non-uniformity did not improve the anodization results. TEM imaging of the cross-section of a 500 W reactively sputtered film showed a columnar structure with small pores. Porosity of the film can be another reason for dielectric breakdown at high fields.

10.4 (Reactively Sputtered Nb$_2$O$_5$ and Niobium) Anodized Capacitors

Due to the difficulties in anodizing the reactively sputtered dielectric and producing defect free films, a different approach was adopted. Instead of depositing a 2000 Å reactively sputtered dielectric, the new structure had a thin layer of reactively sputtered dielectric and on the top of that a thin layer of niobium metal. Then, the niobium metal and the oxide were anodized at 83 V. By adjusting the reactively sputtered oxide and the niobium metal thicknesses, a 2000 Å dielectric was achieved. The idea was to anodize both the metallic niobium and the reactively sputtered Nb$_2$O$_5$ to give a complete and defect-free oxide. This section describes the wafers fabricated with dielectrics formed using this approach. Like before, capacitors were fabricated with both 200 W and 500 W sputtered dielectrics.

10.4.1 Dielectric with 1596 Å Nb$_2$O$_5$ at 200 W and 528 Å Nb WITH NbN

Fabrication

A thermally oxidized wafer was backsputtered, followed by sputtering of Ti/Cu/Ti/NbN/Nb$_2$O$_5$ in order. The sputter parameters and the thicknesses are shown in Table 10.3.
Table 10.3: Sputtering parameters and thicknesses of the reactively sputtered Nb$_2$O$_5$ and Nb anodized wafer.

<table>
<thead>
<tr>
<th>Material</th>
<th>Power (W)</th>
<th>Gas(es)</th>
<th>Pressure (mTorr)</th>
<th>Time (s)</th>
<th>Thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>2500</td>
<td>Ar</td>
<td>5</td>
<td>20</td>
<td>500</td>
</tr>
<tr>
<td>Cu</td>
<td>3000</td>
<td>Ar</td>
<td>5</td>
<td>160</td>
<td>200000</td>
</tr>
<tr>
<td>Ti</td>
<td>2500</td>
<td>Ar</td>
<td>5</td>
<td>20</td>
<td>500</td>
</tr>
<tr>
<td>NbN</td>
<td>2200</td>
<td>Ar/N$_2$</td>
<td>5</td>
<td>25</td>
<td>500</td>
</tr>
<tr>
<td>Nb$_2$O$_5$</td>
<td>200</td>
<td>Ar/O$_2$</td>
<td>10</td>
<td>2800</td>
<td>1596</td>
</tr>
<tr>
<td>Nb</td>
<td>2200</td>
<td>Ar</td>
<td>5</td>
<td>12</td>
<td>528</td>
</tr>
</tbody>
</table>

TEM analysis of the sputtered dielectric gave a deposition rate of 0.57 Å/second. After dielectric sputtering, a 528 Å thick niobium metal layer was sputtered. The sputtering parameters of Nb$_2$O$_5$ and Nb were chosen to achieve a 3000 Å dielectric. Literature shows that during anodization, 7.5 Å Nb is converted to 20 Å Nb$_2$O$_5$ [85]. Thus, 528 Å Nb will be converted to 1408 Å Nb$_2$O$_5$, which combined with 1596 Å Nb$_2$O$_5$ will give a total dielectric thickness of 3004 Å. The wafer was then anodized at 83 V and 0.5 mA/cm$^2$ current density. Anodization was successful with no breakdown. The set voltage was reached in 7 minutes and the final current was 0.6 mA. The total anodization time was 20 minutes. The color of the anodized film was green with purple edges, caused by the edge effect from sputtering. Green color indicates a dielectric thickness of $\sim$ 2500 Å based on interference calculations. 4500 Å aluminum was evaporated on the dielectric and was pattern etched to form the complete structure as shown in Figure 10.17.
Results & Discussion

The capacitors were tested using the Two Probe Tester and the results are shown in Figure 10.18. The capacitance plot shows one spike pointing upward, which was a result of lithography defect that shorted two capacitors together. It gave a combined capacitance of 2.47 nF; therefore each capacitor measured 1.24 nF. There were a total of 4 shorts, ranging from 60 – 65 Ω. The lower capacitance seen on the left hand side in the corner was due to top plate contact issues. This gave a 99.91% functional yield for the wafer. Therefore, this layered structure helped niobium anodize without severe defect formation.
Figure 10.18: Capacitance plot of a (reactively sputtered 1596 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with aluminum top plates.

Figure 10.18 shows that the capacitance over the entire wafer is mostly uniform except for a rim around the center, where the capacitance was lower than other areas, which is possibly due to sputter nonuniformity. The rim around the center showed an average capacitance of 1.16 nF. As described earlier, the switching of the probes changed the polarity applied to the plates which changes the measured capacitance. So, the important region was the capacitance data to the left side of the step only. The average capacitance over the entire wafer taking the capacitances on the left side of the step was 1.26 ± 0.05 nF. From the average capacitance, and using $k \sim 41$, the dielectric thickness was calculated to be 2926 Å. This was 254 Å lower than the calculated thickness which was due to the thickness variation with sputtering. The capacitance distribution in the row taken from the center of the wafer is shown in Figure 10.19.
Figure 10.19: Capacitance distribution in the center row of the wafer with (reactively sputtered 1596 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with aluminum top plates.

The horizontal axis shows the capacitor number (not the number of capacitors) from one end of the wafer to the other. The vertical axis represents the capacitance from each center line capacitor, in nF. The distribution shows a high capacitance on the left end, decreasing close to the center, and increasing by a small value, reaching a small peak at the center and decreasing again. After capacitor #50, the probes changed over and from 51-70, the capacitors were measured with the opposite polarity. From the data of 51-70, we can see an increase in capacitance towards the edge of the wafer. This indicates that if the probes had not changed over the right hand side of the graph would have looked exactly the same as the left hand side i.e., high capacitance at the edge of the wafer,
decreasing close to the center, increasing to a peak in the center, decreasing to a certain capacitance and increasing to the other wafer edge. This gave the plot a ‘W’ shape.

In order to test the thermal stability of these capacitors, they were subjected to temperature storage at 100°C in N₂. A nitrogen environment was employed to prevent aluminum oxidation. Thermal storage was done in several steps and the capacitance data were obtained after each step. There were eight steps. Each step and the results are explained below.

Table 10.4 shows the Number of hours the wafer spent in the furnace at each step and the cumulative number of hours. Initially, the wafer was tested in the as-deposited state and was placed in the furnace at 100°C for 4 hours. Then, the wafer was taken out and was tested. Again the wafer was placed in the furnace for another 4 hours and was tested at the end of that period. This was repeated up to a total of 120 hours and 40 minutes.

Table 10.4: Thermal excursion steps and the hours the wafer spent in the furnace.

<table>
<thead>
<tr>
<th>Step #</th>
<th>No. of Hours in the Furnace (hours)</th>
<th>Cumulative No. of Hours (hours)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
<td>8</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>12</td>
</tr>
<tr>
<td>4</td>
<td>6</td>
<td>18</td>
</tr>
<tr>
<td>5</td>
<td>8</td>
<td>26</td>
</tr>
<tr>
<td>6</td>
<td>12</td>
<td>38</td>
</tr>
<tr>
<td>7</td>
<td>24</td>
<td>62</td>
</tr>
<tr>
<td>8</td>
<td>58.67</td>
<td>120.67</td>
</tr>
</tbody>
</table>

Average capacitances from all the steps are plotted in Figure 10.20. Most of the capacitors after 120 hours 40 minutes were beyond the measurement range of the tester; the average was calculated based on the available data.
From the figure, the center capacitances will be analyzed first. The capacitances taken from the center (#35) of the wafer are plotted in Figure 10.21 with time spent in the furnace. Figure 10.21 shows that the capacitance initially increased from the as-deposited state and then decreased up to 12 hours of heat treatment. A plateau was observed between 12 hours and 26 hours, where the capacitance variation was only ±0.01 nF. From there, the capacitance increased and at the end of 120 hours, capacitance increase was too high that they were out of measurement range. This variation of capacitance with heat treatment time is explained below.
Figure 10.21: Capacitance of the center capacitor (BF row and #35 column) as a function of heat treatment time.

The capacitance data of the wafer in the as-deposited state showed that the dielectric thickness varied across the wafer and the thickness was more in the center (low capacitance) and the thickness was less at the edges (high capacitance). This thickness variation was a result of sputter non-uniformity. In order to explain the variation of capacitance, two mechanisms are proposed.

1. oxygen diffusion within the dielectric
2. oxygen scavenging by aluminum top plate and the formation of NbO$_x$N$_y$.

After the first four hours of heat treatment, the oxygen diffusion was dominant due to thermal activation and caused an increase in capacitance. During this time, aluminum started to combine with oxygen from Nb$_2$O$_5$ and formed aluminum oxide. At the same time, the NbN/Nb$_2$O$_5$ interface produced NbO$_x$N$_y$. These two products reduced the effective dielectric constant of the material. Since oxygen diffusion was dominant, the capacitance increased as the effective Nb$_2$O$_5$ thickness decreased. In the next four hours,
aluminum oxide and NbO$_3$N$_y$ formation continued and the films got thicker and thicker, which lowered the average capacitance. The growth continued up to 12 hours into heat treatment, where the growth of these layers stopped, indicating their self-limiting nature. Between 12 hours to 26 hours, oxygen diffusion and the layer formation were balanced, giving constant capacitance during these periods. Eventually, oxygen diffusion became more prominent and the capacitance increased until the end. Figure 10.22 shows a schematic of the mechanisms during heat treatment.

**Figure 10.22:** Different mechanisms in the NbN/Nb$_2$O$_5$/Al stack during heat treatment at 100°C in N$_2$.

Figure 10.23 shows the variation of the capacitance at the left end of the wafer (#1 column) as a function of heat treatment time.
This figure shows that the capacitance decreased from the as-deposited state, 1.33 nF to 1.2 nF at the end of 12 hours. From there, the capacitance stayed constant until the end of the heat treatment. Here, the trend was different from that observed for the center capacitors. This again was an effect of the thickness difference between the center and the edge. It has already been shown that the sputtered dielectric was thinner at the edges. Thus, the dielectric at the edges was more completely anodized, most of the way into the sputtered film, compared to the center, where the sputtered thickness was more and the anodization field was not enough to reach all the way through the film. Therefore, there was more residual sputtered oxide present in the center, compared to the edges. Thus, there was less room for oxygen diffusion at the edges, and the aluminum oxide and NbO$_x$,$N_y$ formation and their effect dominates.

By oxygen diffusion above, the author means the formation of suboxides by the combination of Nb$_2$O$_5$ and incomplete oxides present in the reactively sputtered film.
This caused the thinning of the desired dielectric, Nb$_2$O$_5$, leading to high capacitance measurements.

Both the capacitances at the edge and the center showed the same capacitance before the heat treatment, yet followed different capacitance paths with the same heat treatments and finally ended with two different capacitances after heat treatment. It is possible that the dielectric thickness as well as the composition (dielectric constant) was different in the center compared to the wafer edge. Therefore, it is recommended to do a composition analysis on different areas of the wafer to verify this theory. Also, more wafers need to be processed to confirm the capacitance variation with heat treatment to ensure that no processing errors had occurred.

The capacitances in the initial state and after a total of 62 hours of heat treatment were compared. It was assumed that Al$_2$O$_3$ ($k$~9) was formed in the first step of heat treatment and reached a limiting thickness of ~50 Å. All the calculated capacitances include Al$_2$O$_3$ dielectric. For the center capacitor, the capacitance difference between the initial (1.32 nF) and after 62 hours (1.57 nF) showed a difference of ~0.3 nF. If only Nb$_2$O$_5$ thinning had happened, the dielectric thickness contributing to the measured thickness would have been 2250 Å. With NbON formation, in order to achieve the same capacitance, thickness of Nb$_2$O$_5$ and NbON had been 2100 Å and 100 Å respectively. The effective thinning of dielectric in this case was ~800 Å. This is close to the movement of Nb/Nb$_2$O$_5$ interface in niobium (~500 Å).

For the edge sample, initial (1.3 nF) and after 62 hours (1.2 nF), the capacitance change was only 0.1 nF, which corresponded to a thickness change of ~250 Å. This difference in the edge capacitance variation compared to the center again indicated the
possibility of having a combination of different thickness and composition across the wafer. Calculations after 72 hours showed that the presence of Al$_2$O$_3$ compensated for the Nb$_2$O$_5$ thinning and the calculated capacitance after 62 hours was the same as the initial capacitance. This decrease in capacitance indicated the formation of another dielectric within the system. Similar to the center capacitor, to achieve the measured capacitance, the thickness of NbON formed and the effective NbON was calculated and found to be 100 Å. The oxide thickness for this combination was 2900 Å. Thus, the data suggested that the film was varying across the wafer in terms of composition as well as thickness. More work is needed to confirm this effect. See Appendix for full calculations and results.

Figure 10.24 and Figure 10.25 compile all the data from different steps of heat treatment.
Figure 10.24: Capacitance data during different stages of heat treatment; (a) as-deposited, (b) after 4 hours, (c) after 8 hours, and (d) after 12 hours.
Figure 10.25: Capacitance data during different stages of heat treatment, continuing from Figure 10.24: (e) after 18 hours, (f) after 26 hours, (g) after 38 hours, (h) after 62 hours, and (i) after 120 hours and 40 minutes. All the times mentioned are cumulative hours.
Now, the total dielectric thickness needed to be reduced to 2000 Å to compare with the results of tantalum capacitors. The following experiments were done to iterate the sputtering time of Nb$_2$O$_5$ while maintaining the Nb sputtering time to obtain a total of 2000 Å dielectric.

**10.4.2 Dielectric with 1071 Å Nb$_2$O$_5$ at 200 W and 528 Å Nb WITH Nb**

**Fabrication**

A thermally oxidized silicon wafer was backspattered and Ti/Cu/Ti/NbN/Nb$_2$O$_5$/Nb were sputtered in order. Please refer to Table 10.3 for deposition parameters. All the parameters were the same except for Nb$_2$O$_5$ sputtering time, which was 1880 seconds to achieve a 1071 Å dielectric. After sputtering, the wafer was anodized at 83 V and 0.5 mA/cm$^2$ current density. The anodization profile is shown in Figure 10.26.

![Anodization profile of a reactivity sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal.](image)

Figure 10.26: Anodization profile of a reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal.
The galvanostatic regime lasted for 8 minutes and 15 seconds and the process was terminated when the current reached 1.31 mA. Total anodization time was 14 minutes. Figure 10.27 shows the image of the wafer after anodization.

![Image of wafer after anodization](image)

**Figure 10.27: Reactively sputtered 1071 Å Nb₂O₅ + 528 Å Nb after anodization at 83 V and 0.5 mA/cm².**

The color of the film was purple (~2200 Å) with some green (2300 Å) edge effect. These thicknesses were calculated based on the film color. After anodization, 4500 Å aluminum was evaporated and was pattern etched to form the top plates of the capacitors.

**Results & Discussion**

The wafer was tested for capacitance using Two Probe Tester. The capacitance data is plotted in Figure 10.28. Out of 4410 capacitors 8 random capacitors were shorted and their resistances ranged from 0.4 Ω to 74.7 kΩ. The probes could not make contact with the top plates of 173 capacitors from having possible contamination on the plate surface and these capacitors were left unmeasured. Functional yield was calculated based on measured capacitors and their shorts, eliminating unmeasured capacitors. Functional yield was found to be 99.81%. The data points that look like needles pointing down were
not all shorts; they were the capacitors that were not measured. The average capacitance was calculated to be 1.49 nF.

Figure 10.28: Capacitance plot of a (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with aluminum top plates.

The capacitance variation at the center of the wafer from the left end of the wafer to the right is shown in Figure 10.29. The variation gave a ‘V’ shape to the center and the capacitance changed from 1.51 to 1.39 nF from the left to the center of the wafer. So, there was about 9% difference between the measured capacitance in the center and the edge of the wafer; once again sputter nonuniformity is the problem.
Figure 10.29: Capacitance distribution at the center of the wafer with (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with aluminum top plates.

**Wafer with new top plate structure**

Since aluminum plates were subjected to oxidation, the aluminum top plates on this wafer were etched away and a new top plate structure was used. The new top plate structure consisted of a gold seed layer, followed by 2 µm nickel, and then another gold layer on top to prevent nickel from oxidizing during thermal excursions. The structure is Cr (100 Å)/Au (500 Å)/Ni (2 µm)/Cr (100 Å)/Au (500 Å). Cr and Au were evaporated and nickel was electroplated. Chromium was used as the adhesion promoter for gold. A schematic of the processed wafer cross-section is shown in Figure 10.30.
Since it was observed that immersing the dielectric in boiling water gave better yield compared with the unboiled wafer for Ta$_2$O$_5$ dielectric, this wafer was immersed in boiling water for 1 hour before the top plates were deposited. After the top plates were created, the capacitors were tested again and the results are shown in Figure 10.31. The data showed 25 shorts ranging from 0.7 Ω to 222 kΩ. The spike on the right hand corner was a result of lithography error where two capacitors became connected. The total capacitance of these connected capacitors was measured to be 4.61 nF, giving 2.31 nF per capacitor. The average capacitance over the entire wafer was calculated to be 2.47 nF. In contrast to the previous results with aluminum top plates, the capacitance in the center was higher than the rest of the wafer.
Figure 10.31: Capacitance plot of a (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates.

The capacitance distribution from a capacitor row located at the center of the wafer is shown in Figure 10.32. The capacitance ranged from 2.14 nF on the left end to 3.4 nF close to the center and fell off to 3.03 nF in the center. A similar trend was repeated on the other end. This increase in capacitance was a possible indication of a difference in dielectric thickness at the center with respect to the edges of the wafer. This was only possible if there was oxygen diffusion during processing, possibly during the immersion of wafer in boiling water for 1 hour. This prolonged exposure to high temperature can cause oxygen diffusion, leading to reduction of effective dielectric thickness. As observed earlier, the dielectric was thicker in the center and relatively thinner in the edges. Since the sputtered oxide was thicker in the center, there were more oxygen vacancies that could be filled by oxygen diffusing down from the top anodized layer.
Therefore, immersion in water at 100°C could have lead to oxygen diffusion within the dielectric, leading to a thinner effective dielectric in the center, thereby giving larger capacitances.

![Capacitance distribution](image)

**Figure 10.32: Capacitance distribution at the center of the wafer with (reactively sputtered 1071 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates.**

*Heat Treatment at 85°C in air for 168 hours*

The thermal stability of these capacitors was tested by placing the wafer in the furnace at 85°C in air for 168 hours. This temperature was chosen to meet the baseline requirements for capacitor applications. The capacitance data after the thermal testing is shown in Figure 10.33. From the measured capacitors, 21 were shorts, which ranged from 1.1 Ω to 651 Ω. Functional yield was calculated to be 99.52%. Figure 10.33 (a) shows the capacitance data in the same scale as Figure 10.31. A noticeable change was that the high capacitance in the center was gone after heat treatment. Figure 10.33 (b)
shows the data in a scale of 3 nF and a slightly increased capacitance all over the wafer except for the four corners and the edges can be observed. Figure 10.33 (b) was tilted for a better view from the top.

![Figure 10.33](image)

**Figure 10.33:** Capacitance plot of a (reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates after 168 hours in air at 85°C (a) capacitance scale 6 nF and (b) at a scale 3 nF.

Figure 10.34 compares the data for the aluminum top plates, boiled dielectric with Cr/Au/Ni/Cr/Au top plates, and after thermal storage. The figure shows that the capacitance increased from aluminum top plate capacitors to heat-treated capacitors to boiled and Cr/Au/Ni/Cr/Au top plated capacitors. In the center, the capacitance with aluminum top plates was almost constant at 1.43 nF, which changed to ~3 nF after boiling and depositing the Cr/Au/Ni/Cr/Au top plates. After heat treatment, the capacitance dropped to 1.62 nF, 0.19 nF higher than the aluminum plated capacitors. If oxygen diffusion had occurred, the capacitors should have measured very high capacitances as the effective dielectric thickness would be very low. Since that did not happen, one other possibility is the formation of a low ‘k’ oxide. Looking at the capacitor structure, the layers close to Nb$_2$O$_5$ were NbN and Cr. There are two possibilities; either
the oxygen was being diffused into NbN to form NbO$_x$N$_y$ or chromium scavenged the oxygen from Nb$_2$O$_5$ and formed oxides of chromium or both.

Figure 10.34: Comparison of capacitance data from the center of the wafer with aluminum top plates, Cr/Au/Ni/Cr/Au top plates and boiled dielectric, and with Cr/Au/Ni/Cr/Au top plates after 168 hours in air at 85°C.

Figure 10.35 shows a simple model of post-heat treated dielectric and its adjacent layers. In this case, since the three materials (Nb$_2$O$_5$, NbO$_x$N$_y$, and Cr$_x$O$_y$) are in series, the effective dielectric constant can be given as,

$$\frac{1}{k} = \frac{1}{k_1} + \frac{1}{k_2} + \frac{1}{k_3}$$

Equation (54)

When two or more capacitors are connected in series, the total capacitance will be less than the capacitance of the smallest capacitor in the combination. Therefore, the effective dielectric constant of this series combination will be less than the smallest of the dielectric constants in this combination. This reduced dielectric constant gives a smaller capacitance to the capacitor. Figure 10.35 shows a schematic of the process.
In order to test this theory, a wafer was fabricated with gold as the top plate and no chromium was used for adhesion. The wafer was subjected to thermal testing and the capacitances before and after were compared. Fabrication and the results are described below.

10.4.3 Dielectric with anodized (1071 Å Nb$_2$O$_5$ at 200 W and 528 Å Nb) and gold top plates with no chromium

Fabrication

A thermally oxidized silicon substrate was backspattered and Ti/Cu/Ti/NbN/Nb$_2$O$_5$/Nb were sputtered in order. The sputtering conditions and the film thicknesses were maintained as described in Section 10.4.2. The wafer was then anodized at 83 V using a current density of 0.5 mA/cm$^2$. The anodization profile is shown in Figure 10.36. The color of the film was purple with green edge effects. The set voltage was reached in 8 minutes and 30 seconds and the total anodization time was 17 minutes and 45 seconds. The final current was 1 mA. The profile is very similar to the previous wafer and the only difference was that the anodization was terminated at 1 mA, instead of 1.3 mA. After anodization, 500 Å gold was evaporated on the dielectric with no chromium for adhesion. Initially it was decided to follow Ni/Cr/Au structure, but due to the difficulties in keeping gold film adhered to the wafer in the nickel bath it was
decided to evaporate another 4500 Å gold on top of the gold seed layer. Therefore, the final top plate was a 5000 Å thick layer of evaporated gold.

Figure 10.36: Anodization profile of a reactively sputtered 1071 Å Nb$_2$O$_5$ + 528 Å Nb metal.

**Results & Discussion**

The wafer was tested with the Two Probe Tester after processing. Then, the wafer was placed in the oven at 85°C for 169 hours in air and the capacitance measurements were done after thermal storage. Forty data points were taken and the change was monitored. Table 10.5 shows the capacitance values before and after thermal storage from one data point. All the measured capacitors showed similar trend seen in Table 10.5

<table>
<thead>
<tr>
<th>Wafer state</th>
<th>Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Initial</td>
<td>1.34</td>
</tr>
<tr>
<td>After 169 hours at 85°C in air</td>
<td>1.31</td>
</tr>
</tbody>
</table>
From the table, it can be seen that the capacitance decreased to 1.31 nF after thermal storage. The capacitance equation tells that a change in capacitance occurs when $k$ or dielectric thickness is changed, provided that the area is the same. Since, the dielectric thickness should not increase with heating, the other possibility is the formation of another dielectric along with Nb$_2$O$_5$. This is only possible if NbN combines with oxygen from Nb$_2$O$_5$. This result showed that NbON formed during heat treatment, lowering the capacitance by 2.2%. The dielectric and its adjacent layers before and after this heat treatment are shown in Figure 10.37 (a) and (b).

![Figure 10.37: Dielectric and adjacent layers (a) before heat treatment, (b) after 169 hours at 85°C, (c) after 168 hours at 100°C, and (d) after 168 hours at 124°C.](image)

After 85°C, the wafer was subjected to 100°C and 124°C in air for 168 hours at each temperature. Table 10.6 compares the capacitance change before and after thermal excursions.
Table 10.6: The capacitance change from the as-deposited state to after thermal excursions at 85°C, 100°C, and 124°C.* After being in the oven for 75 hours and 25 minutes at 100°C, the wafer had to be transferred to a different oven at the same conditions. The time taken to transfer was monitored and was compensated in the new oven.

<table>
<thead>
<tr>
<th>Thermal Storage</th>
<th>Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td>169/85°C</td>
<td>—</td>
</tr>
<tr>
<td>169/85°C</td>
<td>—</td>
</tr>
<tr>
<td>169/85°C</td>
<td>168/100°C</td>
</tr>
</tbody>
</table>

The capacitance increase seen after 100°C and 124°C thermal excursions showed that the effect of the oxygen diffusion within the reactively sputtered imperfect oxide overpowered the effect of NbON formation. As a result of this, a higher effective capacitance was obtained. Figure 10.37 (c) and (d) show schematics of the process going on in the wafer at 100°C and 124°C. The NbON and Nb₂O₅ thicknesses that had to be formed to achieve the measured capacitances were calculated (See Appendix G). The thinning of effective Nb₂O₅ due to oxygen redistribution within the oxide film was approximated using oxygen diffusion rate based on the rate of interface movement. These calculated Nb₂O₅ and NbON thicknesses at 85°C, 100°C, and 124°C are shown in Table 10.7. The oxygen deficient layer was taken as conductive (refer to Section 2.4 in Chapter 2).

Table 10.7: Calculated Nb₂O₅ and NbON thicknesses for the measured capacitances.

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Nb₂O₅ Thickness (Å)</th>
<th>NbON Thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>85</td>
<td>2296</td>
<td>232</td>
</tr>
<tr>
<td>100</td>
<td>2846</td>
<td>602</td>
</tr>
<tr>
<td>124</td>
<td>946</td>
<td>1142</td>
</tr>
</tbody>
</table>
Calculations were made using $k_{\text{Nb}_2\text{O}_5}$ of 37.8, calculated from the initial measured capacitance and the total dielectric thickness. This value is ~3 less than the theoretically reported $k \sim 41$. The incorporation of suboxides (NbO/NbO$_2$) can lead to a change in $k$ value as the material is not pure Nb$_2$O$_5$. Calculated NbON thicknesses for 85°C and 100°C are reasonable, indicating the possibility of NbON formation at the interface. But they are based on an assumed dielectric thinning. Therefore, compositional analysis is necessary to verify this theory.

10.4.4 200 W versus 500 W

According to initial XPS analysis, both 200 W and 500 W sputtering powers gave stoichiometric Nb$_2$O$_5$. In order to verify that, capacitors were fabricated with dielectrics sputtered at 200 W and 500 W and were tested. The capacitors fabricated with 500 W sputtered dielectric gave reasonable capacitance (2.3 nF), whereas those fabricated with 200 W sputtered oxide gave incredibly high capacitance (3.8 nF) for 2000 Å dielectric thickness. This indicated that the dielectrics sputtered at 500 W gave a reasonable amount of Nb$_2$O$_5$ in the film and was probably of better quality compared to 200 W sputtered dielectrics. Therefore, the following capacitors were fabricated with dielectrics sputtered at 500 W and dielectric sputtering times were adjusted to obtain 2000 Å total dielectric thickness.

10.4.5 (Reactively Sputtered Nb$_2$O$_5$ and niobium) Anodized Capacitors at 500 W

Three sets of capacitors were fabricated to study the effect of NbN on the electrical properties of Nb capacitors. Sets #1 and #3 had wafers with and without NbN, but set #2 had only a wafer with NbN. The dielectric thickness was decreased step by step to achieve a capacitance of 1.9 nF (calculated based on $k = 41$ and $d = 1900$ Å). In all the
wafers, the sputtered Nb thickness was kept constant and the reactively sputtered Nb$_2$O$_5$ thickness was varied to obtain the desired capacitance. Table 10.8 shows the three sets with the thicknesses of Nb$_2$O$_5$ and Nb before anodization and the estimated total dielectric thickness after anodization. Total thickness calculations were based on the Nb $\rightarrow$ Nb$_2$O$_5$ conversion ratio of 1:3 obtained from TEM imaging. A sample calculation is shown below.

For #1 set, 1044 Å Nb$_2$O$_5$ and 528 Å Nb

Total dielectric thickness after anodization $= 1044$ Å $+ (528 \times 3)$ Å

$= 2628$ Å

Table 10.8: Three sets of wafers with their Nb$_2$O$_5$ and Nb thicknesses before anodization, and the dielectric thickness after anodization.

<table>
<thead>
<tr>
<th>Wafer Set</th>
<th>Thickness (Å)</th>
<th>Thickness (Å)</th>
<th>Before Anodization</th>
<th>After Anodization</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Nb$_2$O$_5$</td>
<td>Nb</td>
</tr>
<tr>
<td>#1</td>
<td>1044</td>
<td>528</td>
<td>2628</td>
<td>2708</td>
</tr>
<tr>
<td>#2</td>
<td>904</td>
<td>528</td>
<td>2488</td>
<td>2568</td>
</tr>
<tr>
<td>#3</td>
<td>696</td>
<td>528</td>
<td>2280</td>
<td>2360</td>
</tr>
</tbody>
</table>

Note that set #3 has the thinnest dielectric in the group. TEM measurement was done only on the #3 wafer and #1 and #2 were calculated based on that. TEM measured thicknesses are slightly more (80 Å) than the calculated thickness. The fabrication procedure for each set is described below.

**Fabrication**

A thermally oxidized silicon wafer was used as the substrate for all the sets. The wafers were backsputtered for 60 seconds prior to metal deposition. The capacitors fabricated with NbN followed the structure; Ti/Cu/Ti/NbN/Nb$_2$O$_5$/Cr/Au/Ni/Cr/Au and without NbN followed; Ti/Cu/Ti/Nb$_2$O$_5$/Cr/Au/Ni/Cr/Au. The sputtering parameters for
each film are shown in Table 10.9. Since the Nb$_2$O$_5$ thickness was varied for different sets, the sputtering parameters are mentioned separately for each set in the table. Note that the only parameter that changed was the sputtering time.

### Table 10.9: Sputtering parameters and thicknesses of the (reactively sputtered Nb$_2$O$_5$ and Nb) anodized wafers.

<table>
<thead>
<tr>
<th>Material</th>
<th>Power (W)</th>
<th>Gas(es)</th>
<th>Pressure (mTorr)</th>
<th>Time (s)</th>
<th>Thickness (Å)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ti</td>
<td>2500</td>
<td>Ar</td>
<td>5</td>
<td>20</td>
<td>500</td>
</tr>
<tr>
<td>Cu</td>
<td>3000</td>
<td>Ar</td>
<td>5</td>
<td>160</td>
<td>20000</td>
</tr>
<tr>
<td>Ti</td>
<td>2500</td>
<td>Ar</td>
<td>5</td>
<td>20</td>
<td>500</td>
</tr>
<tr>
<td>NbN</td>
<td>2200</td>
<td>Ar$\text{/N}_2$</td>
<td>5</td>
<td>25</td>
<td>500</td>
</tr>
<tr>
<td>Nb$_2$O$_5$</td>
<td>#1</td>
<td>500</td>
<td>Ar$\text{/O}_2$</td>
<td>10</td>
<td>1044</td>
</tr>
<tr>
<td>Nb$_2$O$_5$</td>
<td>#2</td>
<td>500</td>
<td>Ar$\text{/O}_2$</td>
<td>10</td>
<td>904</td>
</tr>
<tr>
<td>Nb$_2$O$_5$</td>
<td>#3</td>
<td>500</td>
<td>Ar$\text{/O}_2$</td>
<td>10</td>
<td>696</td>
</tr>
<tr>
<td>Nb</td>
<td>2200</td>
<td>Ar</td>
<td>5</td>
<td>12</td>
<td>528</td>
</tr>
</tbody>
</table>

The NbN thickness was maintained at 500 Å for all the wafers. After Nb sputtering, the wafers were anodized at 83 V using a current density of 0.5 mA/cm$^2$. Anodization details for each set are given below.

**Wafer Set #1: Dielectric with 1044 Å and 528 Å Nb**

**Without NbN:**

The anodization profile of the wafer without NbN is shown in Figure 10.38. The set voltage was reached in 10 minutes and 15 seconds. This was longer than the time taken for the previous wafers, partly because of the depletion of ions in the electrolyte with every anodization. The final current was 1 mA. The total anodization time was 19 minutes and 5 seconds. The color of the anodized dielectric was purple (2600 Å) with green (2400 Å) edge effects. The thickness is based on the film color.
Figure 10.38: Anodization profile of a reactively sputtered 1044 Å Nb$_2$O$_5$ (at 500 W) + 528 Å Nb metal without NbN under the dielectric.

With NbN:

The anodization profile of the wafer with NbN is shown in Figure 10.39.

Figure 10.39: Anodization profile of a reactively sputtered 1044 Å Nb$_2$O$_5$ (at 500 W) + 528 Å Nb metal with NbN under the dielectric.
The set voltage was reached in 9 minutes. The anodization process was terminated when the current reached 1 mA and the total anodization time was 14 minutes and 56 seconds. Compared to the 1071 Å Nb₂O₅ + 528 Å Nb wafer analyzed in Section 10.4.3, in which Nb₂O₅ was sputtered at 200 W, the total anodization time was less for this wafer whose dielectric was sputtered at 500 W. This was an indication of having a dielectric close to the desired stoichiometry with 500 W sputtering power compared to 200 W sputtered films. The color of the film was purple with some green (~2500 Å) edge effects similar to the wafer without NbN. The thickness for purple can vary from ~2300 Å to 2600 Å depending on the chosen wavelength (range of color).

**Wafer Set #2: Dielectric with 904 Å and 528 Å Nb**

**With NbN:**

Unlike the wafers discussed in set #1, the anodization process was different for this wafer and the set #3 wafers. The wafer was anodized by increasing the voltage to the set point, 83 V, in multiple steps. Since the sputtering time was less compared to previous wafers, the anodization voltage had to be set carefully as a high voltage could punch through the dielectric. So anodization was completed in different steps.

For this wafer, initially, anodization was started at 75 V and 0.5 mA/cm² current density. Once the voltage was increased to the set voltage, the voltage was increased to 77.5 V. After the voltage was increased, 30 seconds were spent at that voltage to let the current decrease. This was done to ensure the dielectric stability at that voltage. Following that, the voltage was increased to 79.5 V and the current decreased. When the current reached 2.69 mA, the voltage started to decrease which indicates onset of dielectric failure. Anodization was immediately stopped and the wafer was taken out and
rinsed. Total anodization time was 12 minutes and 45 seconds, out of which, 9 minutes and 15 seconds were taken to reach 75 V. The color of the anodized film was purple (~2400 Å) with some green (~2500 Å) edge effects as seen before. Since the thickness differences were close together, the colors were similar.

**Wafer Set #3: Dielectric with 696 Å and 528 Å Nb**

**Without NbN:**

In this case, anodization began at 60 V and 0.5 mA/cm² current density. Once the voltage increased to 60 V and the current started to decrease, the voltage was increased to 64 V. The voltage was subsequently increased to 69 V, 75 V, 80 V, and 83 V. The anodized film was light purple (~2300 Å) with a green circular center.

**With NbN:**

For anodizing this wafer, the initial voltage was set to 70 V at 0.5 mA/cm² current density. 70 V was chosen because, from the wafer without NbN, it became clear that the film could hold a minimum of 70 V without failing. Once the voltage was reached, the voltage was increased to 73 V, 78 V, 80 V, and 83 V in order. The anodized film was purple with a green circular area in the center of the wafer. Similar to other wafers, there were edge effects.

The top plates of the capacitors consisted of Cr (100 Å)/Au (500 Å)/Ni (2 µm)/Cr (100 Å)/Au (500 Å) layers. Following anodization, Cr (100 Å)/Au (500 Å) layers were evaporated as the seed layer and 2 µm nickel was electroplated. The fabrication process ended with evaporating Cr (100 Å)/Au (500 Å) and patterning the top plates to define each capacitor.
**Thermal Excursion:**

The capacitors were subjected to 100°C and 124°C for 168 hours each. After being in the oven for 75 hours and 25 minutes at 100°C, the wafers had to be transferred to a different oven under the same conditions. The time taken to transfer was monitored and was compensated for in the new oven.

**Testing:**

The capacitors were tested before and after thermal storage at 124°C. The wafer state before thermal storage is referred to as ‘As-deposited.’ Capacitance, impedance, leakge current, and breakdown voltage measurements were done. All the measurements were performed at room temperature. In the as-deposited state, only capacitance measurements were made using the Two Probe Tester. But, after thermal storage, the capacitance values increased beyond the measurement range of the tester. Therefore, after thermal storage capacitance measurements were performed with the HP4291A Impedance Analyzer. Since different pieces of equipment were used for the capacitance measurements before and after heat treatment, data comparison might give false conclusions. So the capacitance values obtained with the impedance analyzer were compared to the probe data and were adjusted to match the Two Probe Tester measurements. The capacitance adjustment factors for each wafer are shown in Table 10.10. This capacitance difference came from the way in which capacitances were measured in each equipment. The Two Probe Tester measures capacitance using RC time constant whereas the Impedance Analyzer measures capacitance by applying a stimulus voltage and measuring the current across the capacitor. From the current, impedance is calculated and R, L, and C parameters for the device were extracted. Since
these niobium capacitors had high leakage currents, the equipment calculated longer time
to charge indicating larger capacitance. For the Impedance Analyzer, high current across
the capacitor meant smaller impedance, thus calculated capacitance was smaller
compared to the Two Probe Tester.

Table 10.10: Capacitance adjustment factors used for measurements from the
Impedance Analyzer.

<table>
<thead>
<tr>
<th>Wafer Set</th>
<th>ΔC Adjustment Factor (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td></td>
</tr>
<tr>
<td>No NbN</td>
<td>0.09</td>
</tr>
<tr>
<td>NbN</td>
<td>0.11</td>
</tr>
<tr>
<td>#2</td>
<td></td>
</tr>
<tr>
<td>NbN</td>
<td>0.78</td>
</tr>
<tr>
<td>#3</td>
<td></td>
</tr>
<tr>
<td>No NbN</td>
<td>0.69</td>
</tr>
<tr>
<td>NbN</td>
<td>0.64</td>
</tr>
</tbody>
</table>

Results & Discussion:

Wafer Set #1: Dielectric with 1044 Å and 528 Å Nb

Without NbN:

As-deposited state

The capacitance data in the as-deposited state for the wafer without NbN are shown in
Figure 10.40. There were 5 shorts and they ranged from 0.7 – 15.3 kΩ. The average
capacitance over the entire wafer was 1.59 ± 0.03 nF. Functional yield was calculated to
be 99.89%. Figure 10.41 shows uniform capacitance across the wafer except for the
center and the corners. High corner capacitance can be attributed to the edge effects from
sputtering. The data from this wafer is compiled in Table 10.11.
Figure 10.40: Capacitance plot of a set #1 (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates.

Table 10.11: Data from the wafer with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates.

<table>
<thead>
<tr>
<th>No. of Capacitors Tested</th>
<th>No. of Shorted Capacitors</th>
<th>Functional yield (%)</th>
<th>Average Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4410</td>
<td>5</td>
<td>99.89</td>
<td>1.59 ± 0.03</td>
</tr>
</tbody>
</table>

After Thermal Storage

1. Capacitance Measurements

The capacitance plot in Figure 10.41 was obtained after 124°C thermal storage. The number of shorts was 6, compared with 5 prior to heat treatment. A corner capacitor became leaky after heat treatment, possibly from damage while handling. The average
capacitance was $2.21 \pm 0.04 \, \text{nF}$. Functional yield was calculated to be 99.86%. Table 10.12 shows the data after heat treatment.

![Capacitance plot](image)

**Figure 10.41**: Capacitance plot of a set #1 (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air.

**Table 10.12**: The average capacitance and functional yield from (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN after heat treatment.

<table>
<thead>
<tr>
<th>No. of Capacitors Tested</th>
<th>No. of Shorted Capacitors</th>
<th>Functional yield (%)</th>
<th>Average Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4410</td>
<td>6</td>
<td>99.86</td>
<td>2.21 ± 0.04</td>
</tr>
</tbody>
</table>

The capacitance distributions taken from the center row of the wafers before and after heat treatment are shown in Figure 10.42. The figure shows that the capacitance increased after heat treatment as predicted by prior experiments. Increase in capacitance from the end to the center was not very prominent after heat treatment. The ends of the
wafer showed maximum capacitance difference (0.7 nF) compared to other areas (0.6 nF). The average capacitance difference before and after heat treatment was 0.62 nF. This increase in capacitance indicated effective thinning of the dielectric due to oxygen diffusion. Table 10.13 compiles data after heat treatment.

![Graph showing comparison of capacitance before and after heat treatment](image)

**Figure 10.42:** Comparison of center capacitance data for the set #1 wafer with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN before and after heat treatment.

Table 10.13: Data from the wafer with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates.

<table>
<thead>
<tr>
<th>No. of Capacitors Tested</th>
<th>No. of Shorted Capacitors</th>
<th>Functional Yield (%)</th>
<th>Average Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4410</td>
<td>6</td>
<td>99.86</td>
<td>2.21 ± 0.04</td>
</tr>
</tbody>
</table>

### 2. Impedance Measurements

The impedance measurements of the capacitors were done over a frequency range of 1 MHz to 1.8 GHz. The measurements were taken across two capacitors in the floating
plate configuration. The impedance magnitude and the impedance phase plots for the capacitors without NbN are shown in Figure 10.43 and Figure 10.44 respectively.

![Impedance Magnitude Plot]

**Figure 10.43:** Magnitude of the impedance of two capacitors with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates, taken in the floating plate configuration.

From the figure, we can see that impedance plot is as expected for a capacitor. The negative slope continues up to 400 MHz and the impedance levels off up to ~700 MHz during which range, the resistive component dominates. The impedance increases from 700 MHz to 1.8 GHz, where inductive reactance takes over and the capacitor starts to act like an inductor. The ESR is slightly less than 1 Ω, which comes from the Cr/Au/Ni/Cr/Au structure.

Figure 10.44 shows that at low frequencies, phase angle was about −90° just like a pure capacitor. As frequency increased, the angle also became more positive; indicating
that the capacitive reactance was decreasing and the resistive component was becoming more dominant. The phase angle increased to $-63^\circ$ until high frequency introduced noise in the signal.

![Figure 10.44: Phase of the impedance of the capacitor with (reactively sputtered 1044 Å Nb₃O₅ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates.](image)

The ESR and ESL values for the capacitors and the values recalculated for a single capacitor are given in Table 10.14.

**Table 10.14: ESR and ESL of the measured capacitors and calculated values for a single capacitor.**

<table>
<thead>
<tr>
<th></th>
<th>R (Ω)</th>
<th>L (pH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two capacitors in floating plate configuration</td>
<td>0.78</td>
<td>30</td>
</tr>
<tr>
<td>Single capacitor</td>
<td>0.39</td>
<td>15</td>
</tr>
</tbody>
</table>
3. Leakage Measurements

Capacitor currents were measured as a function of voltage. Figure 10.45 shows the leakage current-voltage characteristics with horizontal axis representing applied voltage and vertical axis representing current in log scale.

Figure 10.45: Current (log scale) versus voltage of a capacitor with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates.

Currents were measured for voltages from 0.1 V to 20 V. Currents ranged from 5 nA to 7.5 mA and at 5 V, the current was 33 μA. Based on this data, an acceptable operating voltage would be 3 V, where the current was only 3 μA.

Figure 10.46 shows the current at 5 V as a function of time.
The current decreased with time. Initially, when the DC voltage is applied across the capacitor, the capacitor was charged and the charge current flows through it. Finally, the current reached a stable value, which is the actual leakage of the capacitor. Thus, the leakage current of this capacitor at 5 V was 9.5 µA (current at the end of 12 minutes).

4. **Breakdown Voltage Measurements**

Breakdown voltage measurements were performed with the Impedance Analyzer, but the capacitors did not show breakdown up to the voltage limit of the equipment. The capacitors in the floating plate configuration were tested at 5 V, 10 V, 15 V, 20 V, 25 V, 30 V, 35 V, and 40 V and were found to be stable at all these voltages. Thus, a single capacitor could withstand 20 V without breaking down.
With NbN:

As-deposited state

The capacitors were tested with the Two Probe Tester and the results are shown in Figure 10.47.

![Capacitor Positions](image)

**Figure 10.47:** Capacitance plot of a set #1 (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates.

There were 56 shorts from a total of 4410 capacitors and the shorts ranged from 4 – 221 Ω. That gave a functional yield of 98.73%. Like most of the other plots, the upward spike was a result of mask defect and two capacitors were connected, which showed a combined capacitance of 4.01 nF, or 2.01 nF per capacitor. The average capacitance over the entire wafer was calculated to be 1.78 ± 0.08 nF.
The capacitance distribution in the center row of the wafer is shown in Figure 10.48. The figure shows an increase in capacitance from the edge to the center. But, the overall distribution is uniform.

![Figure 10.48: The center row capacitance distribution on the wafer from left end to the right with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates.](image)

The goal was to achieve a capacitance of 1.9 nF (from $k \approx 41$ and $t = 1900$ Å) to compare with the anodized capacitors with 1900 Å thickness. Table 10.15 compares the data for wafers with and without NbN.
Table 10.15: Comparison of data from the set #1 wafers with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates with and without NbN.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>No. of Capacitors Tested</th>
<th>No. of Shorted Capacitors</th>
<th>Functional Yield (%)</th>
<th>Average Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Without NbN</td>
<td>4410</td>
<td>6</td>
<td>99.86</td>
<td>2.21 ± 0.04</td>
</tr>
<tr>
<td>With NbN</td>
<td>4410</td>
<td>56</td>
<td>98.73</td>
<td>1.78 ± 0.08</td>
</tr>
</tbody>
</table>

After Thermal Storage

1. Capacitance Measurements

The capacitance data after thermal storage is plotted in Figure 10.49.

Figure 10.49: Capacitance plot of a Set #1 (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air.

The average capacitance over the entire wafer was 1.95 ± 0.13 nF. There were 7 new failed capacitors, out of which, 5 of them were located in the corner and dielectric defects were visible under the microscope. Thus, the total number of shorts was 63. Functional
yield was calculated to be 98.57%. Figure 10.50 shows that the capacitance is higher towards the edges and it decreases in the center.

**Comparison of capacitance data before and after heat treatment**

The center row capacitance distribution before and after heat treatment is shown in Figure 10.50.

![Figure 10.50: Comparison of center capacitance data for the set #1 wafer with (reactively sputtered 1044 Å Nb_2O_5 + 528 Å Nb metal) anodized dielectric with NbN before and after heat treatment.](image)

The plot shows an increase in capacitance after heat treatment in the edges. The center capacitance decreases after heat treatment. This behavior was not observed for any other capacitors. Therefore it was an anomalous capacitance variation. The capacitance had increased by ~20% in the edges. Figure 10.50 shows the capacitance data taken from the top, center, and bottom rows of the wafer after heat treatment. The figure shows that the top and bottom capacitors behaved differently from the capacitors located in the center of the wafer. Thus, the average capacitance in Figure 10.50 reflects
the capacitance in the center of the wafer. The data before heat treatment shows (not shown here) a higher center capacitance compared to the top and bottom areas of the wafer, which meant the dielectric was thinner in the center and thicker in the top and the bottom. Due to the thinness, the oxygen diffusion occurred only in the edges increasing the capacitance.

![Capacitance distribution graph]

Figure 10.51: Capacitance distribution in the top, center, and bottom of the set #1 wafer with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN after heat treatment.

2. Impedance Measurements

The impedance data was similar to the previous wafer. ESR and ESL for the capacitors and the values recalculated for a single capacitor are given in Table 10.16.

Table 10.16: ESR and ESL values of the measured capacitors and calculated values for a single capacitor on the wafer set #1 with NbN.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>ESR (Ω)</th>
<th>ESL (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two capacitors in floating plate config</td>
<td>0.196</td>
<td>76</td>
</tr>
<tr>
<td>Single capacitor</td>
<td>0.098</td>
<td>38</td>
</tr>
</tbody>
</table>
3. Leakage Measurements

Figure 10.52 shows the variation of current through the capacitor with applied voltage. The current is plotted in log scale. Measurements were taken after 20 seconds after the application of voltage.

![Current vs Voltage Graph]

**Figure 10.52: Current versus voltage of a capacitor set #1 with (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates.**

The currents were measured for voltages from 0.1 V to 12 V. The current ranged from 0.5 nA to 0.3 mA for this voltage range. The current increases to 0.32 μA at 5 V for this capacitor. High current can be due to current through the flaws in the dielectric, or through a conduction path connecting the plates directly [86]. The current at 5V, measured as a function of time is shown in Figure 10.53.
The figure shows that the leakage current increased with time and it reaches 1.5 µA at the end of 12 minutes. Compared with the capacitor without NbN, the current was much lower, even though, in one case, it increased and in the other case it decreased. But, the highest current in the capacitor with NbN was significantly lower (84%) than the current in the capacitor with no NbN.

“Leakage currents are normally expressed as a single value, measured at room temperature, at a rated voltage, and after 3 or 5 minutes” [86]. Leakage current based on the capacitor can be calculated using a ‘selection limit’ of 10 nA/µFV, which is typically applied to solid tantalum electrolytic capacitors [86]. The selection limit is used in the industry to compare the leakage current to see whether it is high or low. The average capacitance obtained after heat treatment was ~1.95 nF. Assume that the operating
voltage of the capacitor is 5 V. Thus, the selection limit of a 1.95 nF, 5 V capacitor is 97 µA. Figure 10.53 shows that, at the end of 5 minutes, the current was ~1 µA. Thus, the capacitor performance was quite good.

**Comparison of the results of the set #1 (reactively sputtered 1044 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates with and without NbN**

Table 10.17 compares data from capacitors with and without NbN.

**Table 10.17: Comparison of data from set #1 wafers with and without NbN.**

<table>
<thead>
<tr>
<th>Wafer</th>
<th>As-deposited state</th>
<th>After Heat Treatment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Average Capacitance (nF)</td>
<td>Functional Yield (%)</td>
</tr>
<tr>
<td>NbN</td>
<td>1.78 ± 0.08</td>
<td>98.73</td>
</tr>
<tr>
<td>No NbN</td>
<td>1.59 ± 0.03</td>
<td>99.89</td>
</tr>
</tbody>
</table>

The table shows that the capacitance increased when NbN layer was present and the functional yield for this wafer decreased with NbN. Both the wafers showed an increase in capacitance with heat treatment and could withstand 20 V. The incorporation of NbN decreased the leakage current significantly (~98%). More samples are needed to conclude the NbN effect on capacitance functional yield.

Figure 10.54 compares the center row distribution of capacitance with and without NbN wafers in the as-deposited state. The figure shows that the capacitance value increased with NbN. The increase in capacitance towards the center is a common trend
for both the capacitors. The capacitors with NbN showed higher capacitance compared to those without NbN.

Figure 10.54: Comparison of capacitance data from the center row of the set #1 wafers with (reactively sputtered 1044 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with and without NbN.

Figure 10.55 shows center capacitances of wafers with and without NbN before and after heat treatment. The figure shows that the wafer with NbN showed more capacitance variation across the wafer compared with the wafer without NbN. This thickness variation resulted from the added sputter non-uniformity with NbN sputtering, which enhances the ‘d’ in the capacitance equation (since NbN in non-stoichiometric as seen from XPS data, it may not act as an absolute conductor). The higher capacitance with NbN was not an effect related to the presence of NbN; this rather comes from the sputtering system. Heat treatment increased the capacitance for both with and without NbN wafers. For the wafers without NbN, the capacitance across the wafer increased
uniformly, whereas, for the wafers with NbN, the capacitance increased at the ends, but the center capacitance did not change.

Figure 10.55: Comparison of center capacitances obtained for the set #1 wafers with and without NbN.

Wafer Set #2: Dielectric with 904 Å and 528 Å Nb

With NbN:

As-Deposited State

The capacitor results are shown in Figure 10.56. The cluster in Figure 10.57 represents missing capacitors resulting from poor adhesion due to contamination. There were only two shorts out of 4313 capacitors, giving a functional yield of 99.95%. The average capacitance was measured to be $1.68 \pm 0.06$ nF. The plot shows a uniform capacitance distribution across the wafer. The capacitance data from this wafer is compiled in Table 10.18.
Figure 10.56: Capacitance plot of a set #2 (reactively sputtered 904 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates.

Table 10.18: Data from the wafer with (reactively sputtered 904 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates.

<table>
<thead>
<tr>
<th>No. of Capacitors Tested</th>
<th>No. of Shorted Capacitors</th>
<th>Functional yield (%)</th>
<th>Average Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4313</td>
<td>2</td>
<td>99.95</td>
<td>1.68 ± 0.06</td>
</tr>
</tbody>
</table>

After Thermal Storage

1. Capacitance Measurements

The capacitance data after thermal storage is plotted in Figure 10.57. The average capacitance was $2.2 \pm 0.06 \text{ nF}$. No new defects were introduced. Functional yield was same as before heat treatment. The maximum difference between data points was 0.22 nF and the capacitance distribution was more or less uniform.
Figure 10.57: Capacitance plot of a set #2 (reactively sputtered 904 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air.

Comparison of capacitance data before and after heat treatment

The capacitance distributions from the center row before and after heat treatment are shown in Figure 10.58. The plot clearly shows ~30% increase in capacitance after heat treatment, owing to oxygen diffusion.
Figure 10.58: Comparison of center capacitance data for the set #2 wafer with (reactively sputtered 904 Å Nb2O5 + 528 Å Nb metal) anodized dielectric with NbN before and after heat treatment.

2. Impedance Measurements

Impedance versus frequency data was similar to the previous wafers. The combined ESR and ESL values for the capacitors and the values recalculated for a single capacitor are given in Table 10.19.

Table 10.19: ESR and ESL of the measured capacitors and calculated values for a single capacitor.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>R (Ω)</th>
<th>L (pH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two capacitors in floating plate configuration</td>
<td>0.14</td>
<td>84</td>
</tr>
<tr>
<td>Single capacitor</td>
<td>0.07</td>
<td>42</td>
</tr>
</tbody>
</table>

3. Leakage Measurements

Figure 10.59 shows the variation of current in the capacitor with applied voltage. As before, the measurements were taken after ~20 seconds of application of voltage.
Currents were measured for voltages from 0.1 V to 13 V and currents ranged from 1.8 nA to 10 mA for this voltage range. The current increased to 50 µA at 5 V. The leakage current is larger compared to the previous wafer with thicker dielectric (1044 Å Nb$_2$O$_5$ + 528 Å Nb). This is because the thinner dielectric under same voltage stress develops a greater number of defects compared to a thicker dielectric.

4. **Breakdown Voltage Measurements**

Breakdown testing of the capacitors was performed. Similar to the previous wafers, the capacitors did not show any breakdown up to 40 V. The data from this wafer is compiled in Table 10.20.
Table 10.20: Comparison of data from set #2 wafer with NbN before and after heat treatment.

<table>
<thead>
<tr>
<th></th>
<th>Average Capacitance (nF)</th>
<th>Functional Yield (%)</th>
<th>ESR (Ω)</th>
<th>ESL (pH)</th>
<th>Leakage Current at 5 V (µA)</th>
<th>Withstand Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before Heat Treatment</td>
<td>1.68 ± 0.06</td>
<td>99.95</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>After Heat Treatment</td>
<td>2.2 ± 0.06</td>
<td>99.95</td>
<td>0.07</td>
<td>42</td>
<td>42</td>
<td>20</td>
</tr>
</tbody>
</table>

Wafer Set #3: Dielectric with 696 Å Nb$_2$O$_5$ and 528 Å Nb

Without NbN:

As-Deposited State

The capacitors data of the wafer without NbN in the as-deposited state are shown in Figure 10.60.

Figure 10.60: Capacitance plot of a set #3 (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates.
The average capacitance was calculated to be 1.92 ± 0.07 nF. The total number of shorts was 22 and the functional yield was calculated to be 99.50%. The figure plot shows a slight increase (0.02 nF max.) in capacitance values when moved from the ends to the center. The capacitance data from this wafer is compiled in Table 10.21.

### Table 10.21: Average capacitance and functional yield from (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN.

<table>
<thead>
<tr>
<th>No. of Capacitors Tested</th>
<th>No. of Shorted Capacitors</th>
<th>Functional Yield (%)</th>
<th>Average Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4410</td>
<td>22</td>
<td>99.50</td>
<td>1.92 ± 0.07</td>
</tr>
</tbody>
</table>

**After Thermal Storage**

1. **Capacitance Measurements**

The capacitance plot in Figure 10.61 was obtained after 124°C thermal storage.

![Capacitance Plot](image)

**Figure 10.61:** Capacitance plot of a set #3 (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air.
After heat treatment, the number of defective capacitors increased from 22 to 31. Out of the 31 defects, 22 were the same defects found before heat treatment. So, 9 defects were newly formed. Newly formed defects were in random areas of the wafer. Functional yield decreased to 99.3% and the average capacitance was $2.31 \pm 0.03$ nF. The capacitance remained constant with minimum variation across the wafer, except for a slight variation from the ends to the center of the capacitor. The capacitance increases by ~0.07 nF at the center which can be attributed to sputter nonuniformity leading to oxygen diffusion during heat treatment.

**Comparison of capacitance data before and after heat treatment**

Figure 10.62 shows capacitance distribution in the center row of the wafer before and after heat treatment.

![Capacitance Distribution](image)

**Figure 10.62:** Comparison of center capacitance data for the set #3 wafer with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN before and after heat treatment.
The plot clearly shows an increase in capacitance after heat treatment like previous wafers owing to oxygen diffusion. The capacitance increased by ~ 20% after heat treatment.

The data before and after heat treatment are compiled in Table 10.22.

<table>
<thead>
<tr>
<th>Wafer state</th>
<th>Average Capacitance (nF)</th>
<th>Functional yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before Heat Treatment</td>
<td>1.92 ± 0.07</td>
<td>99.39</td>
</tr>
<tr>
<td>After Heat Treatment</td>
<td>2.31 ± 0.03</td>
<td>99.30</td>
</tr>
</tbody>
</table>

### 2. Impedance Measurements

Impedance versus frequency data for the capacitors located in the center of the wafer when measured in floating plate configuration were similar to previous wafers. The combined ESR and ESL values for the capacitors and the values recalculated for a single capacitor are given in Table 10.23.

#### Table 10.23: ESR and ESL of the measured capacitors and calculated values for a single capacitor.

<table>
<thead>
<tr>
<th></th>
<th>ESR (Ω)</th>
<th>ESL (pH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Two capacitors in floating plate configuration</td>
<td>0.24</td>
<td>99</td>
</tr>
<tr>
<td>Single capacitor</td>
<td>0.15</td>
<td>49</td>
</tr>
</tbody>
</table>

Figure 10.63 compiles the impedance data taken from the top, bottom, left, right, and the center areas of the wafer, and shows that the plots are laying one on top of the other and the five plots are identical. Thus, the impedance is independent of the capacitor position on the wafer.
Figure 10.63: Compilation of the impedance magnitude of two capacitors in the floating plate configuration, located at top, bottom, center, left, and right areas of the wafer with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN.

The impedance data of a leaky niobium capacitor is shown in Figure 10.64. Deviation from the model data points and the measured data indicates leakage. The impedance phase of the same capacitor is shown in Figure 10.65. The deviation from the modeled value indicates leakage. A leaky capacitor can be modeled as a resistor in parallel with the capacitor. Due to the presence of this extra resistor, the phase angle deviated from the $-90^\circ$ for a pure capacitor.
Figure 10.64: Impedance magnitude of a niobium leaky capacitor. Note the deviation from the model.

Figure 10.65: Impedance phase of a niobium leaky capacitor. Note the deviation from the model.
3. Leakage Current Measurements

Figure 10.66 shows the variation of current (log scale) in the capacitor with applied voltage. Currents were measured for voltages from 0.1 V to 12 V and they ranged from 96 nA to 2.2 mA.

![Graph showing leakage current measurements](image)

**Figure 10.66: Current versus voltage of a capacitor with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN and Cr/Au/Ni/Cr/Au top plates.**

Current measurements were done at 5 V as a function of time for capacitors selected at the bottom, top, and the center of the wafer and are shown in Figure 10.67. Again, the current is plotted in log scale. Data were taken every 15 seconds for 12 minutes and the graph was plotted. For the top and bottom capacitors, the current increases and reaches a plateau. The leakage at 5 V at the end of 12 minutes was 93 µA for the bottom capacitor and 0.12 mA for the top capacitor. Unlike the other capacitors, the center capacitor...
showed a different trend in leakage current with time. Instead of increasing, the leakage current decreased. Four capacitors were tested and the trend was verified. This difference can be attributed to the sputtered dielectric thickness difference across the wafer. The thicker dielectric in the center gives lower leakage compared to the thinner top and bottom areas.

![Current vs Time Graph](image)

**Figure 10.67:** Current (log scale) at 5 V versus time for capacitors located at the bottom, center, and the top of the wafer, without NbN.

### 4. Breakdown Voltage Measurements

Capacitors were tested for breakdown voltage and they showed no breakdown up to 20 V. Table 10.24 below compiles the data from set #3 without NbN wafer.
Table 10.24: Data from the set #3 capacitor with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric without NbN before and after heat treatment.

<table>
<thead>
<tr>
<th></th>
<th>Before Heat Treatment</th>
<th>After Heat Treatment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average Capacitance (nF)</td>
<td>1.92 ± 0.07</td>
<td>2.31 ± 0.03</td>
</tr>
<tr>
<td>Functional Yield (%)</td>
<td>99.39</td>
<td>99.30</td>
</tr>
<tr>
<td>Average Capacitance (nF)</td>
<td></td>
<td>0.15</td>
</tr>
<tr>
<td>Functional Yield (%)</td>
<td></td>
<td>49</td>
</tr>
<tr>
<td>ESR (Ω)</td>
<td>2.5k</td>
<td>1.5k</td>
</tr>
<tr>
<td>ESL (µF)</td>
<td>2.5k</td>
<td>1.5k</td>
</tr>
<tr>
<td>DCL at 5 V (µA)</td>
<td>2.5k</td>
<td>1.5k</td>
</tr>
<tr>
<td>Withstand Voltage (V)</td>
<td>2.5k</td>
<td>1.5k</td>
</tr>
</tbody>
</table>

With NbN:

As-Deposited State

The capacitors data of the wafer with NbN in the as-deposited state are shown in Figure 10.68.

Figure 10.68: Capacitance plot of a set #3 wafer with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates.
As can be seen from Figure 10.69, there were 4 shorts which gave a functional yield of 99.91%. The average capacitance was calculated to be $1.87 \pm 0.02 \text{ nF}$. The figure showed a uniform capacitance distribution across the wafer. The capacitance data of this wafer is compiled in Table 10.25.

Table 10.25: Average capacitance and functional yield from set #3 wafer with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN

<table>
<thead>
<tr>
<th>No. of Capacitors Tested</th>
<th>No. of Shorted Capacitors</th>
<th>Functional Yield (%)</th>
<th>Average Capacitance (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4410</td>
<td>4</td>
<td>99.91</td>
<td>$1.87 \pm 0.02$</td>
</tr>
</tbody>
</table>

After Thermal Storage

1. Capacitance Measurements

The capacitance plot in Figure 10.69 was obtained after 124°C thermal storage.

Figure 10.69: Capacitance plot of a set #3 wafer with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN and Cr/Au/Ni/Cr/Au top plates after 168 hours at 100°C and 168 hours at 124°C in air.
In this wafer, 13 capacitors were accidentally damaged while handling. There were 51 shorts out of which 38 were clustered together. They were located towards the bottom center of the wafer. There was no physical damage such as cracks that were observed, but since they were found in a cluster it is possible that some physical damage could have happened. While setting up the test equipment, the wafer was mechanically stressed by the test head, which might have led to dielectric damage inside. The average capacitance was $2.31 \pm 0.05$ nF. Functional yield was calculated eliminating damaged capacitors and was found to be 98.84%.

**Comparison before and after heat treatment**

The average capacitances before and after heat treatment are compared in Figure 10.70.

![Figure 10.70: Comparison of center capacitance data for the set #3 wafer with (reactively sputtered 696 Å Nb$_2$O$_5$ + 528 Å Nb metal) anodized dielectric with NbN before and after heat treatment.](image)

The capacitance increased after heat treatment as expected. Table 10.26 compares the capacitance data before and after heat treatment.
Table 10.26: Average capacitance and functional yield comparison of set #3 wafer with NbN before and after heat treatment.

<table>
<thead>
<tr>
<th></th>
<th>Average Capacitance (nF)</th>
<th>Functional Yield (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before Heat Treatment</td>
<td>1.87 ± 0.02</td>
<td>99.91</td>
</tr>
<tr>
<td>After Heat Treatment</td>
<td>2.31 ± 0.05</td>
<td>98.84</td>
</tr>
</tbody>
</table>

2. Leakage Measurements

Figure 10.71 shows the variation of current in the capacitor with applied voltage. The current is plotted in log scale. The measurements were taken ~ 20 seconds after the application of voltage.

Applied voltage ranged from 0.1 V to 12 V and the measured leakage ranged from 10 nA to 9 mA. The currents were measured at 5 V as a function of time for capacitors
located in different areas of the wafer. Two capacitors were tested in each area in order to verify the test results. Figure 10.72 shows the current (log scale) versus time data for a capacitor located at the center of the wafer.

![Graph showing current versus time](image)

**Figure 10.72**: Leakage current at 5 V versus time for capacitors located at the bottom, center, and the top of the wafer, with NbN; current in logarithmic scale.

Data were taken every 15 seconds for 10 minutes and the graph was plotted. The current in the wafer center was significantly lower (~97%) compared to the top and bottom areas of the wafer. The lower leakage from the center can be related to the thicker sputtered films in the center. The presence of excess NbN along with the reactivity sputtered oxide decreased the leakage at the center of the wafer. The center capacitor without NbN showed a different trend in Figure 10.68 compared to that shown in Figure 10.73. This might be an indication of compositional variation in the center with the edges.
3. Breakdown Voltage Measurements

Like other wafers, no breakdown was observed up to 20 V.

Comparison of the results of the set #3 wafers with (reactively sputtered 696 Å Nb₂O₅ + 528 Å Nb metal) anodized dielectric with Cr/Au/Ni/Cr/Au top plates with and without NbN

Table 10.27: Comparison of data from Wafer set #3 before and after heat treatment.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Before Heat Treatment</th>
<th>After Heat Treatment</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Average Capacitance (nF)</td>
<td>Functional Yield (%)</td>
</tr>
<tr>
<td>NbN</td>
<td>1.87 ± 0.02</td>
<td>99.91</td>
</tr>
<tr>
<td>No NbN</td>
<td>1.92 ± 0.07</td>
<td>99.39</td>
</tr>
</tbody>
</table>

The table shows that an improved functional yield obtained with NbN. Decreased functional yield after heat treatment was mainly due to physical damage of the wafer. Current through the capacitor was significantly reduced (~93%) with the incorporation of NbN. Current at 5 V was the average current measured from the center of the wafer. Both the capacitors could withstand 20 V.

10.4.6 Effect of NbN on electrical properties of Nb₂O₅ capacitors

1. Capacitance:

Table 10.28 compares the average capacitance of all the three sets before and after heat treatment.
Table 10.28: Comparison of average capacitances of the three wafer sets before and after heat treatment.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>NbN/No NbN</th>
<th>Nb$_2$O$_5$ Thickness (Å)</th>
<th>Average Capacitance (nF)</th>
<th>Capacitance Difference (nF)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>As Deposited</td>
<td>After Heat Treatment</td>
</tr>
<tr>
<td>#1</td>
<td>No NbN</td>
<td>2628</td>
<td>1.59 ± 0.03</td>
<td>2.21 ± 0.04</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td></td>
<td>1.78 ± 0.08</td>
<td>1.95 ± 0.13</td>
</tr>
<tr>
<td>#2</td>
<td>No NbN</td>
<td>2488</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td></td>
<td>1.68 ± 0.06</td>
<td>2.2 ± 0.06</td>
</tr>
<tr>
<td>#3</td>
<td>No NbN</td>
<td>2280</td>
<td>1.92 ± 0.07</td>
<td>2.31 ± 0.03</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td></td>
<td>1.87 ± 0.02</td>
<td>2.31 ± 0.05</td>
</tr>
</tbody>
</table>

Based on the two complete sets, the information on the effect of NbN in the as-deposited state is contradictory. For the thicker dielectric wafer (set #1), the capacitance increased by 12% when NbN was included, whereas for the thinner dielectric (set #3), the presence of NbN decreased the capacitance by 2.6%. Since there were inconsistencies with the sputtering operation, the effect on capacitance could be related to that. Set #3 did not show any significant difference between capacitance data before and after heat treatment. As the dielectric became thinner, the capacitance change with heat treatment decreased for no NbN wafer as suggested by the capacitance difference in the as-deposited state and after heat treatment. This may be explained as follows. Wafer sets #1 and #3 were anodized to the same voltage; the voltage to anodize 1900 Å material. Therefore, a thicker dielectric had a significant amount of unanodized reactively sputtered dielectric. This meant there were more oxygen vacancies in a thicker dielectric compared to the thinner dielectric. Thus, oxygen could diffuse deeper into the film in the given time for thicker dielectrics, compared to thinner dielectrics, giving a higher capacitance change with heat treatment.
Figure 10.73 plots capacitance data from Table 10.28 along with the calculated capacitance for an assumed $k \sim 41$ and dielectric thicknesses in Table 10.28.

![Capacitance vs. Nb2O5 Thickness](image)

Figure 10.73: Comparison of measured capacitances and calculated capacitances for different dielectric thicknesses.

The calculated capacitances were less than the measured capacitances. The imperfect dielectric along with inclusions decreased the dielectric thickness, which resulted in a high measured capacitance.

2. Impedance:

Impedance data of all the wafers were similar. Therefore, the plot was shown only for the first wafer set. Table 10.29 shows the equivalent circuit parameters of capacitors after heat treatment. The high ESL values resulted from measuring the capacitors in the edges in floating plate configuration. Therefore, the fields did not cancel, resulting in a high ESL value. ESR resulted from having a multilayered top plate structure with nickel and chromium. By correcting these issues, lower parasitics can be achieved.
Table 10.29: ESR and ESL of the three sets of wafers.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>ESL (pH)</th>
<th>ESR (Ω)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>No NbN</td>
<td>43</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td>38</td>
</tr>
<tr>
<td>#2</td>
<td>NbN</td>
<td>46</td>
</tr>
<tr>
<td>#3</td>
<td>No NbN</td>
<td>49</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td>47</td>
</tr>
</tbody>
</table>

3. Leakage Current:

Table 10.30 shows the current through the capacitor data after heat treatment obtained at 5 V, measured after 20 seconds of application of voltage.

Table 10.30: Current at 5 V for capacitors with NbN and no NbN after heat treatment.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>NbN/No NbN</th>
<th>Current at 5 V (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>No NbN</td>
<td>42.00</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td>0.27</td>
</tr>
<tr>
<td>#2</td>
<td>No NbN</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td>0.70</td>
</tr>
<tr>
<td>#3</td>
<td>No NbN</td>
<td>39.00</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td>2.70</td>
</tr>
</tbody>
</table>

Sets #1 and #3 showed a significant reduction of current when NbN was present in the film. For set #1, which had the thicker dielectric, the current was reduced by 99%, and for set #3, with thinner dielectric, leakage current decreased by 93% with NbN in the capacitor structure.

Figure 10.74 shows the leakage current at 5 V for set #1, #2, and #3 capacitors, located at the center of the wafer as a function of time.
Figure 10.74: Leakage current (log scale) at 5 V of capacitors located at the center of the sets #1 and #3 wafers, as a function of time.

Figure 10.74 shows that the leakage in capacitor with NbN increased with time, but the one with no NbN decreased with time. The two curves for each set converge at the end of 12 minutes. The maximum leakage is shown by the capacitor with the thickest dielectric and no NbN due to the presence of unanodized sputtered oxide. The capacitors with no NbN followed the typical leakage versus time curve. But, leakage measurements in the top, bottom, and center areas of the set #3 no NbN wafer showed both the trends; initial upward trend for the top and bottom like and downward trend for the center capacitors. This suggests that the different trends result from Nb$_2$O$_5$ rather than a sole effect of NbN. More investigation needs to be done to explain these trends.

Figure 10.75 shows the leakage current variation as a function of voltage up to 10 V for the capacitors with NbN and without NbN.
Figure 10.75: Leakage current as a function of applied voltage.

Figure 10.75 clearly shows that for a given thickness, the leakage in the capacitors with no NbN at a given voltage is higher than the leakage exhibited by capacitors with NbN. Leakage current increases in the following order.

#1 NbN < #2 NbN < #3 NbN < #3 No NbN < #1 No NbN

The capacitors without NbN and having the thickest reactively sputtered oxide showed maximum leakage. Minimum leakage was shown by the capacitors with NbN and the thickest dielectric. This clearly shows the effect of NbN on leakage current. The capacitors with 2200 Å dielectric, set #3, with NbN showed 41 µA less leakage at 5 V, compared to the one without NbN. Thus, the data indicated that the incorporation of NbN improved leakage characteristics of niobium capacitors. Figure 10.76 shows the effect of NbN on current through the capacitor at 5 V after 5 minutes of application of
voltage for #1 and #3 wafer sets. The plot shows that incorporation of NbN decreased the current by ~91%.

![Figure 10.76: Comparison of currents at 5 V after 5 minutes of application of voltage for #1 and #3 wafer sets.](image)

Different conduction mechanisms have been proposed for leakage in NbO capacitors. These include Poole-Frenkel conduction, Ohmic conduction, and the current due to non-stoichiometry. At high voltages tunneling dominates. Poole-Frenkel conduction can be expressed as [87],

\[
I_{PF} = G_p \cdot U \cdot \exp(\beta \cdot U^{1/2})
\]

Equation (55)

Where,

- \( I_{PF} \) — Leakage current due to Poole-Frenkel conduction
- \( G_p \) — Conductivity
- \( U \) — Applied voltage
- \( \beta \) — Constant for Poole-Frenkel emission

\[
\ln I_{PF} = \ln G_p \cdot U + \beta \cdot U^{1/2}
\]

Equation (56)
Therefore, when \( \ln I_{PF} \) is plotted against \( U^{1/2} \), it should be a straight line, which means if the \( \ln \) (leakage current) versus (voltage\(^{1/2}\)) forms a straight line, the Poole-Frenkel mechanism is dominant for that voltage range.

Figure 10.77 shows the (leakage current) versus (voltage\(^{1/2}\)) plot for the wafer set #3.

![Poole-Frenkel plot for wafer set #3 wafers.](image)

The figure shows that up to \( \sim 3.5 \) V, the graph is a straight line for NbN. The deviation from the straight-line at high voltages indicates that Poole-Frenkel conduction is less and possibly, tunneling is dominant. Similar trend was observed for the capacitor without NbN.

4. **Breakdown Voltage:**

As discussed in the earlier chapters, breakdown voltage measurements could be done only up to 20 V. Therefore, 20 V was called ‘withstand voltage’ if the capacitors survived 20 V test. All the wafers could safely survive 20 V. More rigorous treatment needs to be done to evaluate the effect of NbN on breakdown of these capacitors.
5. Functional Yield:

Table 10.31 shows functional yield from each capacitor in the as-deposited state and after heat treatment.

Table 10.31: Comparison of functional yield of NbN and no NbN wafers before and after heat treatment.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>NbN/ No NbN</th>
<th>Functional Yield (%)</th>
<th>Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>As Deposited</td>
<td>After Heat Treatment</td>
</tr>
<tr>
<td>#1</td>
<td>No NbN</td>
<td>99.89</td>
<td>99.86</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td>98.73</td>
<td>98.57</td>
</tr>
<tr>
<td>#2</td>
<td>No NbN</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td>99.95</td>
<td>99.95</td>
</tr>
<tr>
<td>#3</td>
<td>No NbN</td>
<td>99.50</td>
<td>99.30</td>
</tr>
<tr>
<td></td>
<td>NbN</td>
<td>99.91</td>
<td>98.84</td>
</tr>
</tbody>
</table>

No functional yield change was seen for the #2 wafer set with NbN. But both the #1 and #3 sets show that the functional yield decreased with heat treatment. The wafer set #3 with NbN had been mechanically stressed prior to testing after heat treatment. Thus, there is a possibility of having induced defects by other means than thermal stresses alone. Therefore, based only on this data, it is difficult to conclude the effect of NbN on functional yield.
Chapter 11: Trench Capacitors

This chapter discusses the fabrication of capacitors on trench structures. The fabrication steps at each stage are studied.

11.1 Motivation

Ever decreasing electronics size and increasing circuit density calls for increased capacitance. As seen earlier, one of the ways to increase capacitance is to use a high-\(k\) material. Another way is to increase capacitance is to increase the plate area of the capacitor. But, this must be done without sacrificing area for active circuitry. With trench structures, the surface area can be increased dramatically. A comparison of planar and trench capacitors is shown in Figure 11.1.

Figure 11.1: Comparison of the area availability of a (a) planer capacitor and a (b) trench capacitor.

Figure 11.1 (a) shows a planar capacitor of length, \(l\) and width, \(w\). This gives an area \(A\). In Figure 11.1 (b), the area of the trench capacitor is the sum of area of two sidewalls
(A1 & A3) and the bottom area (A2). Thus, the area can be significantly increased with the trench structure. Depending on the depth of the trenches, the capacitance can be as high as 4× the capacitance obtained with a planar structure. Building trenches into the surface also decreases the board area consumed by the capacitors.

11.2 Trench Design

The mask used for trench fabrication is shown in Figure 11.2.

![Figure 11.2](image)

**Figure 11.2:** (a) Mask used for trench formation and (b) schematic of a cell showing trench widths and the pitch.

In the mask, each cell (square in the mask) contained a set of trenches (96 trenches/cell). Three sets of trench sizes were used. Pitch was maintained at 50 μm and the trench wall widths varied from 15 μm to 20 μm to 25 μm. Figure 11.2 (b) shows the sizes as well as the pitch.
11.3 Trench Fabrication

The trench fabrication began with a p (100) silicon wafer cleaned with DI water, followed by rinsing/drying in Semitool™ ST-270D Spin Rinse Dryer (SRD) for 240/180 seconds rinsing/drying respectively. The p (100) orientation was selected to obtain the desired trench shape. The first step in the trench formation was patterning the substrate to expose the areas to be etched; the trenches were formed by deep reactive ion etching (DRIE). These steps are explained below.

a. Photolithography

The silicon wafer was first coated with hexamethyldisiloxane (HMDS) as an adhesion promoter between the silicon surface and the photoresist. A YES vapor prime oven was used to form a monolayer of HMDS on the surface of the silicon, where one end of the molecule was attached to the silicon and the other to the photoresist. The next step was to apply photoresist for patterning. A positive photoresist, AZ4330, was dispensed onto the wafer, which was held by a vacuum chuck and was spun at 1000 r.p.m. to form an 8 µm thick film on the wafer surface. After spin coating, the wafer was baked at 110°C for 3 minutes on a hot plate to remove the solvents and the stress in the photoresist and to improve the adhesion of the resist to the wafer [59]. Following that, the resist-coated wafer was exposed to i-line (365 nm) for an exposure time (~36 seconds) calculated for an energy of 320 mJ. The wafer was then developed in an aqueous solution of 25% w/w tetramethyl ammonium hydroxide (TMAH) for 6 minutes. After the wafers were inspected, they were baked at 110°C for 2 minutes. The wafers were then ready for etching.
b. Deep Reactive Ion Etching (DRIE)

Trenches were formed using the deep reactive ion etching (DRIE) process. DRIE, as the name suggests, is used to make deep structures using reactive species for etching. The DRIE system at HiDEC, STS Multiplex Advanced Silicon Etcher (ASE®) does etching by the Bosch process, consisting of etching and passivation cycles. Deep etching is achieved by switching between etching and passivation steps. Etching is performed with sulfur hexafluoride, SF₆ for a certain time, followed by passivation of the side walls with octafluorocyclobutane, C₄F₈. This passivation step slows down the lateral etch rate and results in high anisotropy. The desired depth can be achieved by repetitive alternation of etching and passivation. Trench profiles can be varied by varying gas flow rate, pressure, etch/passivation cycles, and platen and coil powers.

The recipe used to achieve the tapered side walled trenches is shown in Table 11.1.

Table 11.1: DRIE recipe for 80 degree tapered walled trenches on p-Si (100).

<table>
<thead>
<tr>
<th>Module</th>
<th>E/P (sec/sec)</th>
<th>APC angle</th>
<th>SF₆</th>
<th>C₄F₈</th>
<th>Ar</th>
<th>COIL</th>
<th>Platen</th>
<th>Cycles</th>
<th>EP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>30/05</td>
<td>60</td>
<td>112</td>
<td>10</td>
<td>18</td>
<td>200/100</td>
<td>12/0</td>
<td>20</td>
<td>EP</td>
</tr>
<tr>
<td>2</td>
<td>27/08</td>
<td>60</td>
<td>112</td>
<td>10</td>
<td>18</td>
<td>200/100</td>
<td>12/0</td>
<td>20</td>
<td>EP</td>
</tr>
<tr>
<td>3</td>
<td>24/11</td>
<td>60</td>
<td>112</td>
<td>10</td>
<td>18</td>
<td>200/100</td>
<td>12/0</td>
<td>20</td>
<td>EP</td>
</tr>
<tr>
<td>4</td>
<td>21/14</td>
<td>60</td>
<td>112</td>
<td>10</td>
<td>18</td>
<td>200/100</td>
<td>12/0</td>
<td>20</td>
<td>EP</td>
</tr>
<tr>
<td>5</td>
<td>18/17</td>
<td>60</td>
<td>112</td>
<td>10</td>
<td>18</td>
<td>200/100</td>
<td>12/0</td>
<td>20</td>
<td>EP</td>
</tr>
<tr>
<td>6</td>
<td>15/20</td>
<td>60</td>
<td>112</td>
<td>10</td>
<td>18</td>
<td>200/100</td>
<td>12/0</td>
<td>20</td>
<td>EP</td>
</tr>
<tr>
<td>7</td>
<td>12/23</td>
<td>60</td>
<td>112</td>
<td>10</td>
<td>18</td>
<td>200/100</td>
<td>12/0</td>
<td>20</td>
<td>EE</td>
</tr>
</tbody>
</table>

This process was developed by Yang Liu, a fellow PhD student at HiDEC. The trench profiles after DRIE are shown in Figure 11.3.
The average height of the silicon wall was 55 µm and the sidewall angle was calculated to be about 80 degrees. This slope was needed to achieve uniform sputter coverage on the trenches. This formed a walled structure in blocks across the wafer.

### 11.4 Capacitor Formation in the Trenches

The process flow for capacitor fabrication is shown in Figure 11.4 and each of the steps are discussed below.
Figure 11.4: Process flow for trench capacitors.

Trench Passivation and seed layer sputtering: The wafer with trenches etched into the silicon was passivated. 2 μm of SiO₂ was deposited using PECVD for that purpose. This was followed by Ti/Cu sputtering as a seed for plating.

Trenches with copper bottom plate: After Ti/Cu seed sputtering, electroplating was done to form the bottom plate of the capacitors. Plating was chosen in order to ensure uniform metal coverage over the trench walls. Both DC and a combination of DC and reverse pulse plating were tried. Figure 11.5 shows the trenches with a plated bottom plate. A combination of DC and reverse pulse plating was used for uniform coverage of trenches. The figure shows continuous step coverage.
Figure 11.5: After copper bottom plate electroplating.

After anodization: After copper plating, titanium and niobium were sputtered and Nb was anodized. Figure 11.6 compares the layer thicknesses on two different size silicon walls. In the figure, the bottom copper was electroplated using DC plating. In both the silicon walls, the material thicknesses were similar as expected.

Figure 11.7 compares the thicknesses on the bottom of the trenches with two different trench openings. Figure 11.7 shows that thicker layers were obtained for the trench with wider opening as expected. The layers were in the following order from the bottom; SiO₂/Ti/sputtered Cu/Plated Cu/Ti/Nb₂O₅. Compared to the top, titanium sputtered thickness had decreased by 71%. For niobium, the thinnest bottom layer was 0.724 μm. Since the anodization voltage was set at 83 V to anodize 0.2 μm, more than enough thickness was available in the bottom to form Nb₂O₅. The Nb₂O₅ layer was uniform with
no color contrast indicating that the sputtered metal had been uniformly anodized. This was verified by EDS compositional analysis. Figure 11.8 shows the continuity of layers from the top to the bottom.

Figure 11.6: Cross-sectional view of the top of the silicon wall after anodization (a) 25 μm wide and (b) 20 μm wide in the bottom.

Figure 11.7: Cross-sectional view of the bottom of the trench with (a) 25 μm opening and (b) 30 μm opening.
Figure 11.8: Cross-sectional view of the silicon walls with metal layers showing continuity from the top to the bottom.

Figure 11.8 shows that the copper was conformally coated on the walls and the niobium oxide layer was continuous from the top to the bottom. As said earlier, the thickness of niobium oxide decreased from the top to the bottom and the thickness on the side walls measured ~1 µm. EDS showed that all the deposited niobium had been converted to Nb$_2$O$_5$. However, there were voids seen close to the bottom of the walls. Figure 11.9 shows the delamination of the dielectric layer from underlying copper.

Figure 11.9 shows that the dielectric layer on the sidewalls had delaminated under stress as shown by the folds on the film at the bottom. This may be explained as follows. During anodization, the oxide grows from the metal and a 3:1 volume expansion takes place. For the bottom metal, when the volume expansion takes place, there is ideally no
X or Y-axes movement in the trench bottom. It can grow only in the Z-direction. Thus, the anodized oxide in the bottom pushed the sidewall oxide layers up. The fold mentioned earlier indicated the stress translating from the bottom to top. This stress affected the oxide close to the bottom only and caused delamination in the bottom areas. This conclusion was supported by the fact that no delamination was seen on the top of the walls.

![Delamination](image)

**Figure 11.9:** Bottom of a trench showing delamination of Nb$_2$O$_5$ from the bottom plate copper.

Figure 11.10 shows the delamination and the resulting cracking of the oxide layer close to the trench bottom. Figure 11.10 supports that the stress induced by the bottom anodization had caused delamination of the sidewall anodized film. Figure 11.11 shows delamination in a row of walls.
It is important to mention that this wafer was anodized to 83 V, but the current did not decrease to low values. When the voltage reached 83 V, the current started to decrease, but after a certain period of time the current started to increase. This may be related to the delamination and formation of cracks in the oxide. The crack formation indicated a dielectric breakdown that provided a low resistance current path, increasing the measured current.
This problem must be further studied and overcome in order to successfully fabricate high capacity trench capacitors.
Chapter 12: Conclusions

The purpose of this project was to fabricate thermally stable niobium capacitors. The presence of suboxides and oxygen diffusion made the capacitors fabricated with Nb$_2$O$_5$ unstable when heated. It is well-known that nitrides are good barriers for oxygen diffusion. This project tested the ability of NbN to prevent oxygen diffusion from the dielectric to the adjacent layers.

Niobium oxides and niobium nitrides were initially characterized for composition and thickness. Both reactively sputtered and anodized oxides were characterized, and the films were amorphous. A 200 W sputtering power in Ar:O$_2$ (90:10) at 10 mTorr gave stoichiometric Nb$_2$O$_5$. Anodized Nb$_2$O$_5$ gave 100% Nb$_2$O$_5$, though sputter induced reduction was observed when sputtered deeper into the film. 100% NbN could not be achieved with the available sputtering power. It was found that the NbN reaches Nb/N = 1:1 with increasing sputtering power. The combined anodization of Nb$_2$O$_5$ and Nb metal introduced cracks at the reactively sputtered oxide/metal interface.

Initial tests with TaN showed that the capacitance values were not affected by the presence of nitrides and the capacitances were thermally stable up to 150°C. Initial niobium capacitors were fabricated with anodized Nb$_2$O$_5$ and the effect of processing steps on oxygen diffusion was evaluated. From the results from the anodized dielectric, it was concluded that sputter heating was sufficient to cause oxygen diffusion, leading to thinning of the desired Nb$_2$O$_5$. Therefore, wafers had to be fabricated with evaporated/electroplated top plates.

In order to avoid the presence of suboxides, the dielectric was proposed to be formed using a combination of reactive sputtering and anodization. After reactively sputtering
the dielectric, anodization was carried out to fill any oxygen vacancies present in the sputtered oxide. But the reactively sputtered oxide broke down during anodization. So, a new film structure was used for dielectric formation; a thin layer of Nb$_2$O$_5$ was reactively sputtered, followed by a thin layer of niobium. This bi-layer stack was anodized to form Nb$_2$O$_5$.

Capacitors were fabricated using this technique with and without NbN. From the results, it was concluded that the presence of NbN decreased the leakage current in niobium capacitors. A 93% decrease in leakage was observed for a 2000 Å dielectric after thermal storage at 100°C and 150°C in air for 168 hours at each temperature. For both capacitors with and without NbN, an increase in capacitance was observed after high temperature storage. The parasitic resistance (ESR) and inductance (ESL) of all capacitors were measured. Values were reasonable given the contribution of these small test devices and the way in which they were probed. All the six fabricated capacitor wafers could withstand 20 V. Functional yield of all capacitor wafers was above 99% for a 2000 Å thick dielectric with and without NbN. More data is needed to conclude the effect of NbN on functional yield.

Anodization of niobium was investigated in three different areas; Nb→Nb$_2$O$_5$ conversion ratio, the effect of anodization electrolyte on the anodic oxide, and the color variation of anodic oxide with the set voltage. The Nb to Nb$_2$O$_5$ conversion ratio changed with electrolyte temperature and ranged from 2.03 at a bath temperature between 1°C and 4°C to 3.39 at a temperature of 61°C to 64°C. The room temperature (20°C) conversion ratio was determined to be 2.9. Thus, the growth rate increased with
electrolyte temperature. The films formed at all these temperatures were amorphous. The colors of anodic films for voltages from 83 V to 218.3 V were also recorded.

Tantalum capacitors were studied for the effect of final current on dielectric thickness. From the results, it was concluded that film growth continued well into the potentiostatic regime. Therefore, it is important that the final current must be mentioned for oxide growth rates when anodized in galvanostatic and potentiostatic modes. The wafers were also fabricated with boiled and unboiled dielectric and the boiled dielectric indicates a higher yielding population than unboiled.

The final part of this research was the investigation of the fabrication of capacitors on trenches. The goal was to increase the capacitance by increasing the surface area. Anodization was found to introduce cracks in the dielectric and delamination from the adjacent layers. Therefore, the trench capacitors were not successful.

**Future Work**

Anodization of thin films in the trenches needs to be carefully studied and is the key to form trench capacitors successfully.

More wafers need to be fabricated with and without NbN to verify the repeatability of the results presented in this dissertation.

Leakage current mechanisms of capacitors with and without NbN must be well studied to explain the effects found in this dissertation.

Composition analysis of wafers with NbN after heat treatment would help confirm the theory of formation of interfacial compounds.

Study of kinetics and other aspects of niobium anodization would be a good contribution to the knowledge base of niobium.
It would be interesting to see if anodization is possible without breaking down when a lower current density (0.25 mA/cm$^2$) is used instead of 0.5 mA/cm$^2$ for reactively sputtered Nb$_2$O$_5$ anodization.
References


   Accessed: 10/05/2009.

   Accessed: 10/05/2009.


Appendix A: Description of Research for Popular Publication

“Honey, I Shrunk the Caps!!”
Susan Jacob and Leonard Schaper
University of Arkansas, Fayetteville
Fayetteville, AR 72701

“The number of transistors per square inch on integrated circuits would double every year,” goes Moore’s law. So, transistors double every 18 months. But, do you want a cell phone that does not fit in your pocket? No! We want to go ‘nano’ in everything. So, how can we put twice the number of transistors in a smaller case? No problem. Smart people at Intel are working hard on that issue. Now that transistors are taken care of, we need to think about other components in your cell phone. Passive components called capacitors, resistors, and inductors occupy up to 50% available area in electronic systems. Therefore, it is imperative that these components must be shrunk as well.

The new niobium (Nb) thin film capacitors developed at the University of Arkansas by Dr. Len Schaper and his ace PhD microEP student, Susan Jacob can be almost half (1/1.7, to be exact) the size of the currently used tantalum (another metal) capacitors, at the same time, delivering the same capacitance. Also, they can be embedded into the circuit board that holds all components, and this embedding technique can save a significant amount of space for other components that make the system work. So, instead of mounting a capacitor on top of a board, we can hide it within. Thus, the area taken by the capacitor on the board = zero! “Best thing since pockets on a shirt,” exclaims Prof. Vickers on this. These capacitors also offer better performance.

Niobium was named after “Niobe,” daughter of Tantalus in Greek mythology due to their similarities in properties. The oxide of niobium, called niobium pentoxide, is of interest because of its material property called relative permittivity. This relative permittivity can be thought of as the ability of a material to store electric charge. The higher the permittivity, the larger the capacitance. But, like anything and everything in life, something good comes at a cost. Niobium pentoxide is always associated with other oxides of niobium. These other oxides provide a path for current when voltage is applied between the plates of a capacitor, making the electric charge leak away. So, a leaky capacitor doesn’t perform the way it should. For niobium pentoxide, the other oxides act as leakage path. Also, the oxygen present in niobium pentoxide tends to move around, leaving the oxide deficient in oxygen. This moving around, also called diffusion is another important issue. These had prevented niobium pentoxide from becoming the material of choice for capacitors.

This approach makes possible low leakage thin film capacitors. They have produced a capacitor structure that sandwiches the oxide layer between two other thin layers that keep the oxygen where it belongs, even at the high operating temperatures of some electronics. Shazam! A smaller and cheaper ‘nano’ gizmo for you!
Appendix B: Executive Summary of Newly Created Intellectual Property

A list of newly created intellectual property is given below.

1. A new approach to niobium capacitors has been shown in the research. A thin film layered structure with NbN/anodized (reactively sputtered Nb$_2$O$_5$ + sputtered Nb metal)/gold top plates for low leakage capacitors, has been implemented.

2. The formation constant of anodized Nb$_2$O$_5$, listed in the literature as 24 Å/second, has been shown to be both a function of final anodization current as well as bath temperature.
Appendix C: Potential Patent and Commercialization Aspects of listed Intellectual Property Items

C.1 Patentability of Intellectual Property (Could Each Item be Patented)

From the list above, the items are discussed below whether each item could be patented.

1. The thin film layered structure with NbN as a separate layer for lowering leakage cannot be patented as it was suggested in the literature. The structure was shown as effective for tantalum capacitors and was adapted to this research for niobium.

2. The formation constant depends on current and temperature.

C.2 Commercialization Prospects (Should Each Item Be Patented)

1. The approach should not be patented at this point as more tests need to be done to verify the results.

2. No, the concept is interesting scientifically, but not something that could be patented.

C.3 Possible Prior Disclosure of IP

1. U.S Patent #6051044 has been issued for nitrided powders for producing low leakage niobium electrolytic capacitors. The capacitors are formed using nitrided niobium as the anode, thus forming the dielectric from the nitrided layer. In our research, the nitride layer and dielectric are separate entities and are formed separately.

2. No patents or publications were found on boiling dielectric by this author.
Appendix D: Broader Impact of Research

D.1 Applicability of Research Methods to Other Problems

This work involved the standard research methods of trials of material and process conditions and analysis of created structures for functional yield performance and reliability.

D.2 Impact of Research Results on U.S. and Global Society

The research can impact the consumer electronics market, cell phones, PDAs, pagers, etc by making them smaller by implementing these capacitors in circuit boards. Thus, our research has the potential to impact the U.S and global population by providing them with smaller electronics.

D.3 Impact of Research Results on the Environment

The research results do not have any adverse impact on the environment. In fact, niobium is plentiful in the earth’s crust and capacitor manufacturing will not exhaust the mineral, whereas tantalum is more rare, requiring mining in potentially sensitive areas.
Appendix E: Microsoft Project for MS MicroEP Degree Plan
<table>
<thead>
<tr>
<th>ID</th>
<th>Task Name</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
</tr>
</thead>
<tbody>
<tr>
<td>49</td>
<td>tantalum and niobium technology overview</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>technology of niobium oxide capacitor</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>copper plating to fill blank area for three-dale</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>niobium as new material for electrolyte cap</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>thin film dielectric capacitors formed by resin</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>electrical properties of anodically oxidized tantalum</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>dielectric materials in thin film capacitors</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>replacing mco2 with polymers</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>the stabilization of niobium-based solid electrolyte</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>comparison of multiper ceramic and metal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>lead-free soldering effect on tantalum cap</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>wafer level processing of 3d system in past</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>pave's thesis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>select dissertation committee</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>63</td>
<td>dissertation talk</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>64</td>
<td>research</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>65</td>
<td>fabrication of ta capacitance with diffusion barrier</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>66</td>
<td>new capacitor process with ta/n diff two</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>67</td>
<td>spattering Ta, Cu, TaN, 2000 A Ta</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>68</td>
<td>activation of TaO5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>69</td>
<td>spattering TaN, Cu</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>70</td>
<td>ni-ao passivation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>71</td>
<td>cu thick and tantalum electrode</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>72</td>
<td>defect testing</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>73</td>
<td>new cap with ta/n tantalum</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>74</td>
<td>tantalum sputtering</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>75</td>
<td>cu sputtering</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>76</td>
<td>ta2o5 sputtering</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>77</td>
<td>activation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>78</td>
<td>cu sputtering</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>79</td>
<td>lithography</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80</td>
<td>cu etching</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ID</td>
<td>Task Name</td>
<td>2006</td>
<td>2007</td>
<td>2008</td>
<td>2009</td>
</tr>
<tr>
<td>----</td>
<td>-----------------------------------------------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Qtr 1</td>
<td>Qtr 2</td>
<td>Qtr 3</td>
<td>Qtr 4</td>
</tr>
<tr>
<td>113</td>
<td>Nb205 Color Chart</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>114</td>
<td>NbN-Nb205 film optimization</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>115</td>
<td>NbN deposition at different powers and</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>116</td>
<td>Nb205 deposition at different powers</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>117</td>
<td>NbN Etch rate determination</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>118</td>
<td>NbN-Nb205 thickness and composition</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>119</td>
<td>Fix anodization Parameters</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>120</td>
<td>Sputter Nb metal and anodize</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>121</td>
<td>Fabrication of planar Nb205 capacitors</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>122</td>
<td>Fabrication with 2000 A dielectric-Anodize</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>123</td>
<td>Yield testing</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>124</td>
<td>Fabrication with 2000 A dielectric-NbN</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>125</td>
<td>Yield testing</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>126</td>
<td>REPT Fabrication with 2000 A dielectric</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>127</td>
<td>Yield testing</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>128</td>
<td>Ti Diffusion Barrier+ plated top plates</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>129</td>
<td>Yield testing</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>130</td>
<td>Reactively Sputtered+ Anodized</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>131</td>
<td>Reactively Sputtered</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>132</td>
<td>Heat Treatment of Anodized film for an</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>133</td>
<td>Bath Modification</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>134</td>
<td>3180_TopPlate</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>135</td>
<td>New bath-sodium pentaborate-tetry</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>136</td>
<td>Al top plates</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>137</td>
<td>Plated top plates with low power reed</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>138</td>
<td>500 W in Varian 3180</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>139</td>
<td>Pulse sputtering</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>140</td>
<td>Cr6A top wafer</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>141</td>
<td>NbN_500W BS+Ano</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>142</td>
<td>NbN_200 W BS+Ano</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>143</td>
<td>Nb205_200W_thickness Characteristic</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>144</td>
<td>SEM Thickness Analysis</td>
<td>✔</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ID</td>
<td>Task Name</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-----</td>
<td>-----------------------------------------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>177</td>
<td>Trench Formation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>178</td>
<td>Trench passivation and seed layer q</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>179</td>
<td>Copper electroplating</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>180</td>
<td>ESTEM imaging</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>181</td>
<td>NbTa deposition and anodization</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>182</td>
<td>Anodization with different thickness</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>183</td>
<td>ESTEM imaging</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>184</td>
<td>Research Data Analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>185</td>
<td>Defect test data of NewCap 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>186</td>
<td>Capacitor testing - no contacts detected</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>187</td>
<td>Capacitor data of NewCap WH 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>188</td>
<td>Leakage current data of NewCap WH 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>189</td>
<td>Capacitance data of NewCap WH 1 after an</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>190</td>
<td>Capacitance data of NewCap WH noTaN</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>191</td>
<td>Capacitance data of NewCap WH noTaN-100</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>192</td>
<td>Nb characterization</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>193</td>
<td>Nb, NbO, NbN analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>194</td>
<td>Film thickness + composition optimization</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>195</td>
<td>XPS data analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>196</td>
<td>wafer processing study</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>197</td>
<td>Trench anodization analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>198</td>
<td>All cap data analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>199</td>
<td>Heat Treatment data analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200</td>
<td>Electrical characterization data analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>201</td>
<td>TEM data analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>202</td>
<td>Trench ESTEM mage analysis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>203</td>
<td>Conferences &amp; Publications</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>204</td>
<td>Poster Presentation @ EUREC</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>205</td>
<td>IMAPS Int Passives Workshop</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>206</td>
<td>IMAPS Conference 2018</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>207</td>
<td>MRS Meeting 2019</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>208</td>
<td>Proposal Presentation</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Year</th>
<th>Qtr 1</th>
<th>Qtr 2</th>
<th>Qtr 3</th>
<th>Qtr 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>2006</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2007</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2008</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2009</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(Chart showing project timeline and milestones)
<table>
<thead>
<tr>
<th>ID</th>
<th>Task Name</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Qtr 1</td>
<td>Qtr 2</td>
<td>Qtr 3</td>
<td>Qtr 4</td>
</tr>
<tr>
<td>209</td>
<td>CANDIDATE EXAM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>210</td>
<td>WRITING DISSERTATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>211</td>
<td>WRITING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>212</td>
<td>FIRST DRAFT SUBMISSION</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>213</td>
<td>EDITING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>214</td>
<td>FINAL DRAFT SUBMISSION</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>215</td>
<td>FINAL EDITING</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>216</td>
<td>GIVE DISSERTATION TO COMMITTEE MEMBERS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>217</td>
<td>WORK ON THE PUBLIC PRESENTATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>218</td>
<td>REVIEW BY ADVISOR AND CHANGES</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>219</td>
<td>PUBLIC PRESENTATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>220</td>
<td>DEFENSE DAY</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>221</td>
<td>DISSERTATION TO GRAD SCHOOL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Appendix F: Identification of All Software Used in Research and Dissertation Generation

Computer #1:
   Model Number: Dell Inspiron 1150
   Serial Number: 7F03561
   Location: Home
   Owner: Susan Jacob

Software #1:
   Name: Microsoft Office 2007
   Purchased by: University of Arkansas

Software #2:
   Name: Image J

Software #3:
   Name: XKRATOS
   From Jeff Wight (www.mst.edu), the developer of the program

Computer #2: DELL
   Serial Number: 210MT71
   Location: ENRC 363E
   Owner: Dr. Susan Burkett

Software #1:
   Name: Microsoft Office 2007
   Purchased by: University of Arkansas

______________________________________________________________________________
Susan Jacob                                                        Dr. Leonard W. Schaper
Appendix G: Calculations for Oxygen Diffusion and NbON formation in Chapter 10 (Section 10.4.3)

The capacitances at different temperatures are calculated below based on the theory explained.

Assumptions:
1. NbON can be completely converted into NbO$_x$N$_y$
2. Oxygen diffusion through Nb$_2$O$_5$ is 50% of that through metallic niobium
3. Dielectric constant of NbO$_x$N$_y$ = Dielectric constant of Nb$_2$O$_5$ – 10% of $k_{Nb_2O_5}$
4. Thickness limit for NbO$_x$N$_y$, when all the NbN becomes converted into NbO$_x$N$_y$

NbN to NbON conversion ratio

Rewriting Equation (48) for NbON,

$$d_{NbON} = \frac{\rho_{NbN} \times A_{NbN}}{\rho_{NbON} \times A_{NbON}} \left( \frac{MW_{NbON}}{MW_{NbN}} \right) \times d_{NbN}$$

(Equation AG.1)

Assuming $A_{NbN}$ and $A_{NbON} = 1$ cm$^2$ and density for NbON was approximated from the density of TaON

$$d_{NbON} = \frac{6 \times 1 \left( \frac{122.91}{107} \right)}{5 \times 1} \times d_{NbN}$$

$$= 1.38 \times d_{Nb}$$

For every Angstrom of NbN consumed, ~ 1 Angstrom of NbON is formed.

Initial state

Measured capacitance = 1.34 nF, dielectric thickness = 2496 Å, area = 1 mm$^2$, and a theoretical ‘$k$’ of 41.
The theoretical capacitance is ~8% larger than the experimental capacitance indicating the possibility of having a thinner dielectric and/or having a dielectric of lower dielectric constant.

The dielectric constant of the oxide film can be calculated using the above values and the following equation:

\[ C = \frac{\varepsilon_0 \varepsilon_r A}{d} \]  

(Equation AG.3)

The terms have their usual meanings.

\[ 1.34 \times 10^{-9} F = \frac{8.85 \times 10^{-12} F/m \times \varepsilon_r \times 1 \times 10^{-6} m^2}{2496 \times 10^{-10} m} \]

\[ \varepsilon_r = \frac{1.34 \times 10^{-9} F \times 2496 \times 10^{-10} m}{8.85 \times 10^{-12} F/m \times 10^{-6} m^2} \]

\[ = 37.8 \]

This dielectric constant is used as the \( k_{\text{Nb}_2\text{O}_5} \) in the following discussions.

At 85°C after 169 hours

Total distance oxygen diffused into NbN to form NbO\textsubscript{x}N\textsubscript{y} and the diffusion within the oxide at 85°C was calculated using Equation (8) in Chapter 2 and was found to be 200 Å. Thus,

Thickness of Nb\textsubscript{2}O\textsubscript{5}, \( d_{\text{Nb}_2\text{O}_5} = \) Initial thickness – oxygen deficient thickness

\[ = 2496 \text{ Å} – 200 \text{ Å} \]

\[ = 2296 \text{ Å} \]
\[ k_{\text{Nb}_2\text{O}_5} = 37.8 - 10\% \text{ of (37.8)} \]

\[ = 34.02 \]

\[ \sim 34 \]

Now, the capacitor structure consists of a \( \text{Nb}_2\text{O}_5 \) dielectric in series with a \( \text{NbO}_x\text{N}_y \).

Total capacitance at 85°C after 169 hours, \( C_{85} \) can be calculated using the following equation.

\[
\frac{1}{C_{85}} = \frac{1}{C_{\text{Nb}_2\text{O}_5}} + \frac{1}{C_{\text{NbO}_x\text{N}_y}}
\]

\[
= \frac{d_{\text{Nb}_2\text{O}_5}}{\varepsilon_o k_{\text{Nb}_2\text{O}_5} A} + \frac{d_{\text{NbO}_x\text{N}_y}}{\varepsilon_o k_{\text{NbO}_x\text{N}_y} A}
\]

\[
= \frac{1}{\varepsilon_o A} \left( \frac{d_{\text{Nb}_2\text{O}_5}}{k_{\text{Nb}_2\text{O}_5}} + \frac{d_{\text{NbO}_x\text{N}_y}}{k_{\text{NbO}_x\text{N}_y}} \right)
\]

Equation (AG.4)

Rearranging for \( d_{\text{NbO}_x\text{N}_y} \),

\[
\frac{1}{1.34 \times 10^{-3}} = \frac{1}{8.85 \times 10^{-12} \text{ F/m} \times 10^{-6} \text{ m}^2} \left( \frac{2296 \times 10^{-10} \text{ m}}{37.8} + \frac{d \times 10^{-10} \text{ m}}{34} \right)
\]

\[ d = 231.8 \text{ Å} \]

At 100°C after 168 hours

The capacitance at 100°C after 168 hours is calculated similar to that of 85°C.

\( \text{Nb}_2\text{O}_5 \) thinning at 100°C in 168 hours = 450 Å

\( d_{\text{Nb}_2\text{O}_5} = d_{\text{Nb}_2\text{O}_5} \text{ at 85°C} - 450 \text{ Å} \)

\[ = 2296 \text{ Å} - 450 \text{ Å} \]

\[ = 1846 \text{ Å} \]

From Equation (AG.4),
\[
\frac{1}{1.33} = \frac{1}{8.85 \times 10^{-12} \text{ } F / m \times 10^{-6} \text{ } m^2} \left( \frac{1846 \times 10^{-10} m}{37.8} + \frac{d \times 10^{-10} m}{34} \right)
\]

\[
d = 601.9 \text{ Å}
\]

At 125°C after 168 hours

\[
\text{Nb}_2\text{O}_5 \text{ thinning at 125°C in 168 hours} = 900 \text{ Å}
\]

\[
d_{\text{Nb}_2\text{O}_5} = d_{\text{Nb}_2\text{O}_5} \text{ at } 85°C - 900 \text{ Å}
\]

\[
= 1846 \text{ Å} - 900 \text{ Å}
\]

\[
= 946 \text{ Å}
\]

From Equation (AG.4),

\[
\frac{1}{1.51} = \frac{1}{8.85 \times 10^{-12} \text{ } F / m \times 10^{-6} \text{ } m^2} \left( \frac{1246 \times 10^{-10} m}{37.8} + \frac{d \times 10^{-10} m}{34} \right)
\]

\[
d = 1141.8 \text{ Å}
\]
Appendix H: Calculations for Oxygen Diffusion and NbON formation at 100°C in Chapter 10 (Section 10.4.1)

The capacitances at different temperatures are calculated below based on the theory explained.

Assumptions:

1. Maximum NbO₅Nₓ formation is limited to NbN thickness
2. Oxygen diffusion through Nb₂O₅ is 50% of that through metallic niobium
3. Dielectric constant of NbOₓNₐ = Dielectric constant of Nb₂O₅–10% of kₙb₂O₅
4. Al₂O₃ formation takes place in the first step itself and the thickness is limited to 50 Å

Initial state:

Measured capacitance = 1.3 nF, dielectric thickness = 3021 Å, area = 1 mm², and a theoretical ‘k’ of 41.

\[
C = \frac{8.85 \times 10^{-12} \ F / m \times 41 \times 1 \times 10^{-6} \ m^2}{3021 \times 10^{-10} \ m} \\
= 1.2 \ nF
\]

The measured capacitance is ~8% more than the experimental capacitance indicating the possibility of having a thinner dielectric due to the presence of suboxides.

The dielectric constant of the oxide film can be calculated using the above values and Equation (AG.3).

\[
1.3 \times 10^{-9} \ F = \frac{8.85 \times 10^{-12} \ F / m \times \varepsilon_r \times 1 \times 10^{-6} \ m^2}{3021 \times 10^{-10} \ m} \\
\varepsilon_r = \frac{1.3 \times 10^{-9} \ F \times 3021 \times 10^{-10} \ m}{8.85 \times 10^{-12} \ F / m \times 10^{-6} \ m^2} \\
= 44.4
\]
This dielectric constant is used as $k_{\text{Nb}_2\text{O}_5}$ in the following discussions.

**CENTER CAPACITOR:**

After 62 hours (cumulative) at 100°C:

From Equation (AE.1),

\[
\frac{1}{1.57 \times 10^{-9}} = \frac{1}{8.85 \times 10^{-12} \text{ F/m} \times 10^{-6} \text{ m}^2} \left( \frac{2150 \times 10^{-10} \text{ m}}{37.8} + \frac{50 \times 10^{-10} \text{ m}}{9} + \frac{d \times 10^{-10} \text{ m}}{34} \right)
\]

\[
d = 100 \text{ Å}
\]

A combination of 2150 Å Nb$_2$O$_5$ and 100 Å NbON are needed to achieve the measured capacitance, 1.57 nF.

**EDGE CAPACITOR:**

After 62 hours (cumulative) at 100°C:

From Equation (AE.1),

\[
\frac{1}{1.2 \times 10^{-9}} = \frac{1}{8.85 \times 10^{-12} \text{ F/m} \times 10^{-6} \text{ m}^2} \left( \frac{2900 \times 10^{-10} \text{ m}}{37.8} + \frac{50 \times 10^{-10} \text{ m}}{9} + \frac{d \times 10^{-10} \text{ m}}{34} \right)
\]

\[
d = 100 \text{ Å}
\]

Therefore, a combination of 2900 Å Nb$_2$O$_5$ and 100 Å NbON are needed to achieve the measured capacitance, 1.2 nF.