Experimental Study of Novel Materials and Module for Cryogenic (4K) Superconducting Multi-Chip Modules

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Experimental Study of Novel Materials and Module for Cryogenic (4K) Superconducting Multi-Chip Modules
Experimental Study of Novel Materials and Module for Cryogenic (4K) Superconducting Multi-Chip Modules

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Microelectronics-Photonics

By

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ABSTRACT

Niobium based superconducting electronics (SCE) are the fastest known digital logic which operate at 100GHz and greater. Nevertheless, the performance of the SCE device depends on the temperature of the SCE integrated circuits being maintained between 4.2 – 4.25 K. Additionally, as semiconductors are slowly approaching their performance limitations the SCE devices are viewed as a viable alternative for high end computing and commercial wireless applications. However, the successful commercialization of SCE’s requires the demonstration of these devices in multichip module (MCM) architecture. Thus the stringent thermal constraint and the complex MCM architecture require an innovative method for thermal management.

This research addressed the above challenges by using a nano-engineered polymer adhesive, namely, single walled carbon nanotube (SWCNT) integrated epoxy as underfill for the packaging of SCE in MCM architecture. The current research distinguished itself by (1) examining the thermal management issues across a single chip SCE-MCM and developing a thermal model based on literature and experimental analysis, (2) developing a new material, namely SWCNT-integrated epoxy whose thermal and electrical performance were analyzed as a function of SWCNT loading and (3) demonstrating the thermal and electrical performance of single chip SCE-MCM test structure and 2D SCE-MCM test structure with SWCNT-epoxy as underfill.

The thermal analysis of the single chip SCE-MCM was studied by modeling, which illustrated that cryogenic underfill with thermal conductivity of 0.04 W/mK plays a vital role in thermal management of SCE-MCMs. A SWCNT-epoxy underfill material which was thermally conductive but electrically insulating was developed and the experimental verification of the thermal model was completed by studying the thermal performance of single chip SCE MCMs
with and without SWCNT-epoxy as underfill. It was determined that the heat transport between the SCE chip and SCE carrier chip in MCM architecture was enhanced by the use of SWCNT underfill. Current-Voltage characteristics of Josephson Junctions of SCE chip and carrier bonded using SWCNT underfill were measured at 4.2 K, demonstrating the electrical performance of SCE devices bonded using SWCNT underfill. Finally, 2D SC-MCM was fabricated, and the transition to superconducting state was demonstrated at 4 K with and without SWCNT underfill.
This thesis is approved for recommendation to the Graduate Council.

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DEDICATION

This work is dedicated to my awesome wife Maria, my loving kids Samuel and Elyannah and my wonderful parents John and Malathi for their love, support, patience and belief in me.
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ABBREVIATIONS

Al – Aluminum
APS – Ammonium Persulphate Solution
A.U. – Arbitrary Units
AWG – American Wire Gauge
BCB – Benzocyclo Butane
BGA – Ball Grid Array
CMOS – Complementary Metal Oxide Semiconductor
CO – Carbon Monoxide
COP – Coefficient of Performance
CTE – Coefficient of Thermal Expansion
Cu – Copper
DRIE – Deep Reactive Ion Etching
DWCNT – Double Walled Carbon Nanotube
EP – Electroplating
Fe – Iron
HiDEC – High Density Electronic Center
HIPCO – High Pressure Catalytic Decomposition of Carbon Monoxide
Hg – Mercury
IC – Integrated Circuits
I_c – Critical Current
I_s – Supercurrent
I_b – Bias Current
JJ – Josephson Junctions
KGD – Known-Good-Die
MCM – Multi-Chip Modules
MWCNT – Multi Walled Carbon Nanotube
MRI – Magnetic Resonance Imaging
Nb – Niobium
NSA – National Security Agency
OFHC – Oxygen Free High Conductivity Copper
Pb – Lead
PCB – Printed Circuit Board
PR – Photoresist
PVD – Physical Vapor Deposition
R_int – Thermal Interfacial Resistance
RIE – Reactive Ion Etching
RSFQ – Rapid Single Flux Quantum
R_W – Wire Resistance
SC – Superconducting
SCE – Superconducting Electronics
SCMCM – Superconducting Multichip Module
SRD – Spin Rinse Dry
SWCNT – Single Walled Carbon Nanotube
SIS – Superconductor-Insulator-Superconductor
SCE-IC – Superconducting Electronic Digital Integrated Circuit
Ta – Tantalum

$T_c$ – Critical Temperature

$T_{\text{Cold}}$ – Cold temperature

$\text{TCR}$ – Temperature Coefficient of Resistance

$T_g$ – Glass Transition Temperature

Ti – Titanium

TIM – Thermal Interface Material

TMAH – Tetramethyl Ammonium Hydroxide

$T_R$ – Room Temperature

UV - Ultraviolet

YBCO – Yttrium Barium Copper Oxide
CHAPTER 1 – INTRODUCTION

Decades of complete dominance by Complementary Metal Oxide Semiconductor (CMOSs) devices is approaching its performance limits for high end computing application. This is evidenced by the industrial trend, where dual core and quad core processors are currently being used for parallel processing of information. Furthermore, currently research is being done in the semiconductor packaging industry to enhance 3D silicon integration and 3D Integrated Circuit (IC) integration to further maximize the packing density of CMOS processors with shorter interconnects for performance enhancement [1]. These trends have opened the avenues for other technologies such as nanotechnology based devices and revived the interest in superconducting electronic (SCE) devices as a potential alternative to CMOS technology in the realm of high end computing applications required by military and commercial wireless applications. The National Security Agency (NSA) has recently reported that the superconducting technology based on Rapid Single Flux Quantum (RSFQ) logic is the most promising technology for high end computing applications which require fast processing speeds at low power [2].

The state of zero resistance to flow of current or the state of infinite electrical conductivity of a material is called superconductivity. The discovery of superconductivity was enabled by the liquefaction of helium gas by the Dutch physicist Kammerlingh Onnes. He went on to discover the phenomenon of superconductivity in mercury in 1911 [3]. He observed that the electrical resistance of mercury disappeared when cooled below a certain temperature; this temperature at which the electrical resistance of a material disappears is called critical or transition temperature (T_c). Based on the transition temperature superconductors are classified into two major classes, namely; low temperature superconductors which require liquid helium
temperature (4.2 K) and high temperature superconductors which exhibit superconductivity at liquid nitrogen temperature (77 K). The focus of the current research is on low temperature superconducting electronics, particularly, RSFQ superconducting devices based on niobium chemistry. Table 1.1 shows transition temperature of some of these materials

Table 1.1: Transition Temperature of few low temperature superconducting materials [4, 5]

<table>
<thead>
<tr>
<th>Material</th>
<th>Transition Temperature (T_c) K</th>
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<tr>
<td>Al</td>
<td>1.2</td>
</tr>
<tr>
<td>Hg</td>
<td>3.9 – 4.2</td>
</tr>
<tr>
<td>Pb</td>
<td>7.2</td>
</tr>
<tr>
<td>Ta</td>
<td>4.5</td>
</tr>
<tr>
<td>Nb</td>
<td>9.2</td>
</tr>
<tr>
<td>Ti</td>
<td>0.4</td>
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According to the BCS Theory, when certain metals are cooled below their critical temperature the electron-phonon interaction causes electrons of opposite spin to pair. These paired electrons are called Cooper pairs. When two wires made of superconducting material are weekly coupled by a thin insulator there exists a phase difference between the two wires. Applying a voltage leads to a change in flux, which results in an oscillating current across the superconductor-insulator-superconductor (SIS) junction due to the Cooper pairs. This alternating current is called the Josephson Effect. The Josephson current of the SCE digital circuits is given as

\[ I_s = I_c \sin (\Phi) \]  

(1.1)
where $I_s$ is the lossless DC supercurrent, $I_c$ is the critical current or the maximum supercurrent of the SIS junction, and $\Phi$ the phase difference between the two superconducting wires [6]. The weakly coupled SIS junction is called the Josephson Junction (JJ). The Josephson Effect and the JJ form the basis for many superconducting applications such as sensitive magnetometers, precision voltage standards and digital electronics. In a superconducting digital circuit the JJs of the SCE device performs the same role as a transistor. In semiconductor technology the transistor acts as the switch and, though there is no definite practical superconducting transistor, the JJ provides the switching mechanism for digital SCE devices.

Based upon the Josephson Effect there were two definite approaches towards creating superconducting digital circuits, (1) Voltage State Logic and (2) Rapid Single Flux Quantum Logic (RSFQ). In the 1970’s – 1980’s the IBM Corporation aimed at the creation of a JJ computer using superconducting Lead and what was called as the “Voltage State Logic”. Even though this approach led to the development of new device and packaging principles which are currently used, it met with failure for a couple of reasons. First, the explosive growth of the semiconductor industry along with the requirement of liquid helium made the research and development of the JJ computer superfluous. Second, the use of the Voltage State Logic in which the JJ was initially in the superconducting state “$V=0$” which represented the “ON” state and switched to resistive state “$V=1$” or “OFF” state by increasing the applied current beyond $I_c$ was used to switch the superconducting digital circuits. The JJ was switched to “OFF” state the logic gates had to be reset (1 to 0) by turning the bias current to zero [8]. Third technology failed due to the fact that thermal aging of Lead resulted in degradation of the superconducting properties. This reduced the flexibility in design and ultimately resulted in the JJ computer project being terminated. A more comprehensive review of the IBM JJ project is explained elsewhere [7].
The second approach called RSFQ logic, which is currently implemented and the fastest known digital logic, was developed by three scientists Likharev, Mukhanov and Semenov from Moscow State University [8]. In this approach, Lead was replaced by Niobium as the superconducting material of choice. Niobium, being a more rigid material than Lead resulted in robust devices whose performance was not affected by thermal aging. Additionally, the JJs of a RSFQ SCE device consist of a Nb-AlxOx-Nb trilayer which forms the SIS structure of the JJs. The more critical aspect of the present approach is that the “1” and “0” states of the digital logic are based on the transmission of a picosecond voltage pulse (V(t)) of quantized area which is denoted by Equation 1.2 [8]

\[ \int V(t) \, dt = \Phi_0 \]  \hspace{1cm} (1.2)

Based on the above Equation 2 it was determined that a single flux quantum pulse would toggle the JJ between 1 and 0 resulting in switching the logic gates from “ON” to “OFF” state. Furthermore, the use of RSFQ logic resulted in the JJ automatically resetting without the need for an external influence. Over the last decade several companies in the US and Japan have advanced the field of superconducting digital industry by the demonstration of these ultrafast digital circuits. For instance, Hypres Inc. has shown the demonstration of RSFQ based superconducting receiver operating at 20 GHz [9] and a complete Analog-to-Digital Converter (ADC) [10]. Furthermore the researchers in Japan have demonstrated the performance of SFQ based digital integrated circuits with 40 GHz clock frequencies [11]. Though SCE devices have shown performance attributes which are highly desirable, the testing has primarily been in a liquid helium environment [12]. This is clearly undesirable for the successful commercialization of SCE.
As the complexity of the superconducting integrated circuits increases it is critical to demonstrate the performance of the RSFQ based SCE devices in a multi-chip module (MCM) architecture. The MCM architecture offers the opportunity for SCE design engineers to increase the functionality of the SCE package by placing multiple superconducting IC’s on a common carrier. The rest of the chapter gives an overview of what has been accomplished in the field of SCE cryopackaging and details the challenges in the transition from a single chip package to a MCM package.

1.1. Literature Review

Cryopackaging is the field of electronic packaging for low temperatures SCE devices. There are several key elements that determine the success of a cryopackage:

- Availability of a stable cryogenic environment.
- Thermal management both on and off the SCE integrated circuits
- Implementation in MCM architecture

1.1.1. Cryogenic Environment

1.1.1.1. Background

Cryogenics is a term generally used for temperatures below 100 K. Conventionally the cryogenic environment for SCEs is provided by the use of liquid helium Dewar’s. Though this is a fast and convenient method for the testing of digital integrated circuits (ICs) of SCEs, from a practical standpoint it reduces the viability for the commercial use of SCE devices. Thus the liquid helium Dewar’s have been replaced by the liquid cryogen free commercial cryocooler technology. Cryocoolers are currently used as cryo-pumps for plasma vapor deposition systems in thin film fabrication, for cooling of superconducting magnets in Magnetic Resonance Imaging (MRI) systems, space applications, particle accelerators and also explored for cooling SCE-ICs.
A more detailed list of potential applications of cryocoolers has been described by Radebaugh [13, 14].

1.1.1.2. Classification of Cryocoolers:

Based on the type of flow cryocoolers are classified into two groups: (1) recuperative cycle and (2) regenerative cycle. The recuperative flow is based on the continuous flow of the refrigerant in one direction whereas in the regenerative cycle the gas is compressed and expanded to exchange heat in a regenerative material placed between the hot and cold side inside of the cryocooler. Cryocoolers are further classified as follows: (1) Joule Thompson cryocooler, (2) Brayton cryocooler, (3) Stirling cryocooler, (4) Pulse-Tube cryocooler and (5) Gifford-McMahon cryocooler. Figure 1 shows the common recuperative and regenerative cryocoolers[14].

![Figure 1: Classification of cryocoolers [14]](image)

The most important parameters of a cryocooler are (1) cooling capacity, which is the power rating of the cooling provided at a certain temperature, (2) power input, which is the work done in cooling from room temperature \(T_R\) to 4.2 K and (3) efficiency –which is the ratio of
the actual coefficient of performance to the ideal coefficient of performance (COP). The ideal COP is the given in Equation 3 [15]

\[
\text{COP} = \frac{T_{\text{Cold}}}{T_R - T_{\text{Cold}}}
\]  

(1.3)

In SCE the cryocooler is not used to take heat away, but rather to maintain the temperature of the SCE-ICs between 4.2 K – 4.25 K where the device exhibits superconductivity. The cryocooler is the enabling technology for the success of commercial wireless and military applications based on SCEs. Detailed description of the various cryocoolers has been extensively discussed elsewhere [14-20]. In this research the Gifford McMahon (GM) cryocooler was used to provide the cryogenic environment and thus a detailed description of the GM cryocooler is given below.

The GM cryocooler falls under the category of a regenerative flow closed loop system in which helium gas provides the cooling power. The GM cryocooler consists of a cold head which houses the displacer, a regenerator matrix, and inlet and outlet valves operated by an external compressor. The compressor and the cold head are connected by flexible connectors which are filled with helium gas. The compressor has a supply and return valve which alternatively switch between high and low pressure to compress and expand helium gas and provide the cooling power to the cold head. The GM cryocooler has two stages where cooling is provided, the 1st stage, also called the hot stage, is generally where the helium gas is expanded and precooled to about 27 K. This is followed by the 2nd stage, called the cold stage, which can be cooled to 2.5 K – 2.7 K depending on the mass of the material attached to it. The operation of the GM cryocooler is governed by the simple compression of the helium gas by the piston or displacer during which the heat generated is exchanged with the regenerator matrix. This is followed by the expansion
cycle where heat from the cold head is transferred to the helium gas and the returning gas picks up the heat from the regenerator matrix. This is then exchanged with the cooling medium in the compressor, which could be either air cooled or water cooled. Figure 2 shows the schematic of a typical 2-stage GM cryocooler [13].

![Schematic of a 2-stage GM cryocooler](image)

**Figure 2: Schematic of a 2-stage GM cryocooler [13]**
1.1.1.3. *The GM Test Bed:*

The GM cryocooler was used to provide the cryogenic environment for all tests completed in the current research. The GM cryocooler was chosen because it was lower in cost compared to the more recent pulse tube cryocoolers, its performance was well established, reliable, and offered the highest cooling capacity of 1.5 W @ 4.2 K. In the rest of the dissertation the GM cryocooler used in the current research will be addressed as the test bed. The test bed was purchased from Sumitomo (Model # RDK 415D) and fitted with electrical feed-through’s and vacuum and radiation shields by Janis Inc. The test bed consisted of two stages, the 1\textsuperscript{st} stage achieved a temperature of 27 K and the 2\textsuperscript{nd} stage cooled to a base temperature of 2.6 K. Calibrated silicon diode temperature sensors (670 SD) where mounted on the 1\textsuperscript{st} stage and 2\textsuperscript{nd} stage of the cryocooler and the cooling capacity was verified. An 8” diameter copper plate with 4-40 tapped holes was mounted on the 2\textsuperscript{nd} stage of the cold head and used as the sample mount stage for all experiments. Additionally, the 1\textsuperscript{st} stage also had 4-40 tapped holes for sample mounting which were only used to monitor the 1\textsuperscript{st} stage temperature during experiments. A water cooled compressor (Model # F50) was chosen to provide the oscillating pressure to the test bed. Figure 3 is the picture of the test bed and compressor used in the current research and Figure 4 is the schematic of the test bed.
Figure 3: Test bed and compressor

Figure 4: Schematic of the test bed
1.1.2. The Single Chip Cryopackage Architecture

The term “cryopackage” is used to describe the SCE chip, substrate, input/output lines and the cryocooler. In section 1.1.1., the cryocooler which is a key enabler for the SCE technology was discussed. The current section describes the background architecture of the cryopackage for a single chip SCE cryopackage.

The single chip SCE cryopackage consisted of a SCE chip fabricated using well established niobium chemistry [21-23]. The SCE chip was flip chip bonded to a carrier substrate which initially was a printed circuit board (PCB) [24]. The connection between the SCE chip and the PCB was made with the help of beryllium copper spring finger contacts and a cryocooled copper block. Figure 5 shows the schematic of the typical arrangement of a SCE single chip cryopackage [24].

![Figure 5: Single chip SCE cryopackage [24]](image)
Recent developments in materials, electronic packaging technology, and need for high density packaging led to the PCB being replaced by a silicon carrier as the substrate [25]. The SCE single chip was flip chip bonded to a silicon substrate by reflow of the solder bumps, which were made of indium-tin (In-Sn) [25]. The flip chip bonded single chip package was then connected to a printed circuit board (PCB) using a similar press contact mating arrangement to the spring finger contacts made of beryllium copper [26]. A cryocooled oxygen free high conductivity (OFHC) copper block was mounted onto the back side of the substrate to secure the substrate to PCB connection. A thin layer of indium was used as thermal interface material (TIM) between the OFHC copper block and the substrate to reduce the thermal resistance due to surface roughness. It has been shown that the TIM was critical to help the chip achieve the required temperature for proper operation [26]. The connection between the PCB board, which was at 4 K, and that of the room temperature electronics was accomplished by using a combination of coaxial copper, coaxial phosphor bronze, and flexible ribbon cables [27, 28]. Since the RSFQ circuitry operates based on the transmission of flux quantum pulses of the SCE-IC, it was protected from external magnetic fields with mu-metal shields made of rare-earth metals. The current chip-substrate-PCB arrangements along with the I/O connectors and mu-metal shields were housed inside the cryogenic test bed. Figure 6 shows the typical arrangement of a single chip SCE cryopackage [29].
1.1.3. **Thermal Management**

The challenge in ensuring the functionality of SCE devices is managing the thermal budget for SCE cryopackage. Thermal management for SCE is two-fold, namely; (A) reduce the heat load into the cryocooler from the input and output lines used for signal transmission between room temperature electronics and the cryogenic environment and (B) maintain the temperature of the SCE chip between 4.2 K – 4.25 K.

*Figure 6: Shows the complete single chip cryopackage architecture [29]*
The heat load from room temperature to the cold stage of the cryocooler is from three primary sources. Radiation from room temperature to the cold stage of the test bed is the first source of heat. This is reduced by the use of thermal radiation shields at various stages along the test bed. The second source of heat is transmission through the coaxial cables which serve as the input/output (I/O) lines that connect the PCB to room temperature electronics. The I/O lines need to have low attenuation which will result in high electrical conductance. According to Weidman-Franz law [30] the electrical resistance and thermal resistance of a metal is directly proportional and related by Equation 1.4 shown below

\[ L = \frac{\kappa}{\sigma T} \]  

(1.4)

where \( L \) is the Lorentz number \((2.45*10^{-8}\ \text{W/mK}^2)\), \( \sigma \) is the electrical conductivity of the metal, \( \kappa \) the thermal conductivity of the metal and \( T \) is the temperature in degree Kelvin. Thus if electrical conductivity is high so will be the thermal conductivity of the metal, leading to excessive heat being transferred from room temperature to the cold stage of the test bed. This is undesirable as the cooling power of the cold stage of cryocoolers vary from 0.1 W to 1.5 W at 4.2 K. For instance, the test bed used in the current research had a maximum heat removal capacity of 1.5 W at 4.2 K but with the increase in mass due to the addition of the sample mount stage the heat removal capacity decreased below 1.5 W. Thus this challenge was generally addressed by thermally anchoring all the I/O lines to the various stages of the test bed. In the current research all connections were anchored to the 1\textsuperscript{st} stage and 2\textsuperscript{nd} stage to reduce excessive heat load from room temperature. Currently, work is being done to replace the normal metal such as copper alloys, used for the I/O and signal lines with superconducting wires made using high temperature superconducting material such as Yttrium Barium Copper Oxide (YBCO) [31]. Another aspect of the heat due to the wires was the joule heating \((I_b^2R_w)\) due to the bias current
(I_b) and wire resistance (R_w). The use of superconducting wires will allow for large currents without the joule heating component. Thus each cryopackage needs to be custom designed to ensure that the heat load due to joule heating and heat transfer between room temperature and 2nd stage of the test bed are minimized.

The last and most critical aspect of thermal management was removal of heat generated by the SCE chip. Traditionally, the heat dissipation of a SCE chip varies between 2-5 mW, although this is very small compared to semiconductor IC’s, the thermal budget of the test bed and the dependence of the critical current on the temperature highlight the importance of on-chip thermal management. Thus the success of the SCE package was dependent on ensuring that the superconductive effects present in the SCE devices was not degraded due to an undesirable thermal profile on the SCE chip.

Based on the architecture of a single chip superconducting cryopackage, the heat generated by the SCE chip was transferred to the silicon substrate by conduction through the solder bumps. The substrate was maintained at 4.2 K with the aid of the TIM and the cryocooled copper block. Though this arrangement was sufficient for the demonstration of single chip SCE devices a more complex arrangement, such as those employing more than one active SCE chip, required maintaining a uniform thermal profile across multiple SCE chips.

1.1.4. Multi-Chip Module (MCM) Architecture

MCM architecture is the packaging of more than one active IC on a single carrier substrate. In the early seventy’s IBM developed the flip chip bonding process to mount an active IC directly onto a substrate [32]. The flip chip bonding process led to the rapid development of IC packages with smaller foot prints and higher performance due to reduced parasitics and higher speeds. In the mid-90s the semiconductor industry, which continuously reinvented packaging to
enhance performance, developed the MCM package to further increase performance while reducing the foot print of the electronic package. This saw the transition from wire bonded packaging to flip chip bond packages. This transition later led to the development of Ball Grid Arrays (BGA), a form of surface mount technology where the PCB to package connection was through the solder balls rather than through-hole connections [33]. This had several advantages, of which the key advantage were the increased packing density and the reduction in time and cost due to ease of package dismount. This led to further developments in device packaging leading to 2D and 3D stacking of active devices to further reduce package size and cost while increasing packing density and device performance. A more extensive review of current trends in IC packaging have been detailed elsewhere [34].

The superconductor industry is making a similar transition from single chip packages to MCM’s. SCE-MCM’s offer the conventional benefits seen in semiconductor MCMs which are reduced foot print and higher packaging density. But the more critical aspect of SCE-MCMs is the fact that the MCM architecture will provide the flexibility to SCE-IC designers to mount multiple IC’s on a single carrier, thus reducing the complexity in fabrication while increasing the potential for known-good-die (KGD) testing. Figure 7 is a schematic of a highly complex SCE-MCM presented by Abelson et al., which shows 512 SCE-MCMs mounted on to a common cylindrical PCB [35, 36].
Though the concept of MCMs has been around for more than a decade it has only recently seen interest from the superconductor community. This has been due to the fact that the enabling technologies such as cryocoolers, fabrication of reliable JJ based RSFQ devices and the increasing difficulty faced by the CMOS devices in increasing clock speed. But the most significant challenge for the transition of SCE devices from a single chip package to MCMs is the fact that in a single chip package the signal is transmitted from the chip to the substrate via solder bumps. But in MCMs the signal is transmitted from one chip to another chip via solder bumps and transmission lines. A higher than expected temperature delta would result in performance degradation in SCE-MCMs. Thus on-chip clock speed needs to be maintained during the transmission of the SFQ pulses between SCE-ICs packaged in MCM architecture.

Figure 7: Packaging concept for highly complex SCE-MCMs [35, 36]
This can be done efficiently by the optimal design and fabrication of solder bumps and effective thermal management strategies.

Recently Hypres Inc. have demonstrated the transmission of SFQ pulses from one section of a SCE-IC via solder bumps to a SCE carrier chip back to a different section of the SCE-IC via 100 micron (diameter) In-Sn bumps [37]. Though this has been a successful first step the testing was completed in a liquid helium Dewar, which brings the focus back onto the thermal management and performance of SCE devices mounted on a cryocooler.

1.2. Proposed Solution:

As described in sections 1.1.3 and 1.1.4, thermal management in a SCE-MCM is critical for the success of cryopackaging and the development of high end computing application based on RSFQ logic. This issue was thrust to the forefront due to the synergy in the enabling technologies and the challenges faced by CMOS technologies. The current research addressed the thermal management challenge by estimating the material-process-package relationship in a single chip SCE cryopackage through modeling and experimental verification at 4 K. Then the thermal performance of a SCE cryopackage in a multi-chip module SCE cryopackage was demonstrated.

Heat transfer between a SCE-IC and a SCE carrier IC is by two parallel paths. First through the solder bumps and second, the cryogenic underfill. Solder bump material is usually metals or metal alloys which is a better thermal conductor than underfill. To increase the heat removal from the flip chip bonded SCE-IC through the solder bumps the most straightforward approach is to increase the number of solder bumps and to increase the size of solder bumps, but this would defeat the purpose of high density compact SCE cryopackage. Thus the second option is to find a cryogenic underfill which has high thermal conductivity. This is easier said than
done, due to the fact that underfills are generally composed of an amorphous polymer whose thermal conductivity at liquid helium temperatures is extremely low. Thus the approach sought was to integrate thermally conducting particles to enhance the thermal conductivity of the cryogenic underfill. This approach is not new, as currently there are several thermally enhanced underfills that are commercially available from Henkel Inc. and others for room temperature electronics. But underfills for packaging of SCE’s is still a developing area. Due to small interconnect distances between chip and carrier chip the particle size of material used for loading and enhancing thermal properties of underfill is in the nanometer range. Wong et al. and his research team have done considerable work on nanoparticle based underfill for room temperature electronics [38-44].

Based upon this foreknowledge the current research was started with the examination of the material-processing-packaging relationship to the thermal and electrical performance of SCE-MCMs. As the first step the temperature delta of a flip chip bonded SCE-MCM was studied by developing a theoretical model based on literature. The modeling analysis was extended by varying the bump diameter, number of bumps and underfill thermal conductivity to examine the design threshold which enabled the SCE-MCM cryopackage to meet the 50 mK design constraint.

The next phase of the research involved the experimental analysis of the temperature delta of a SCE-MCM. This was accomplished by examining material properties, designing a test setup and experimentally measuring the temperature delta of a flip chip bonded SCE-MCM at 4 K. The flip chip bonded SCE-IC tested had 220 In-Sn bumps of 100 micron diameter. The package assembly process was examined to optimize the package assembly process to enhance the thermal performance of SCE-MCMs.
The next goal of the research was to examine the role of nanomaterial’s in the thermal performance of underfill. Nanomaterials have slowly become an integral part of commercial electronics. As mentioned earlier nanoparticle loaded underfills are currently being used and researched for various room temperature applications. One such novel nanomaterial is a carbon nanotube. The discovery of carbon nanotubes by Iijima in 1991 [45] opened the door for aggressive integration of nanoparticles in mainstream electronics. Particularly, carbon nanotube based products are being explored for applications in photovoltaics, thermal interface materials, fuel cells, and composites. However the integration of carbon nanotubes (CNT) in epoxy as an underfill for the packaging of superconducting electronics is a challenging goal, which until this work had been unexplored.

The integration of CNTs was addressed by purifying single walled carbon nanotubes (SWCNT) and integrating them into a typical cryogenic epoxy adhesive. SWCNT were chosen as they exhibit the highest known thermal conductivity of any known material [46]. The thermal and electrical performance of the SWCNT integrated epoxy was studied as a function of SWCNT loading concentration to determine the optimal loading necessary for an underfill which is thermally conductive but electrically insulating. Additionally, the interfacial resistance between underfill with and without SWCNTs and passivation layer of IC’s was examined to determine the role of interfacial resistance in heat transfer.

Finally, the SWCNT epoxy was integrated as underfill in a SCE-MCM and the thermal and electrical performance was tested at 4.2 K. The critical current ($I_c$) of Josephson Junctions of the SCE devices, which was the primary indicator of the electrical functionality of SCE devices, was measured by completing I-V measurements of the RSFQ based SCE MCM at 4.2 K. Theory indicates that the $I_c$ will decrease with increasing temperature. Thus the $I_c$ was monitored first as
a function of temperature from 4.2 K to 8 K and secondly as a function of applied power to SCE chip at 4.2 K. This was the first practical demonstration of a SCE-MCM flip chip bonded using SWCNT integrated polymer adhesive as underfill.

To understand the thermal performance of the SCE-MCM the thermal analysis was completed by heating the SCE chip with a surface mount heater and monitoring the temperature of the SCE chip and SCE carrier chip. Additionally, to demonstrate a 2D MCM package architecture a test vehicle was designed and fabricated using tantalum as the superconducting metal. Tantalum was chosen as the $T_c$ of tantalum is 4.5 K which is very close to the operational temperature of a SCE-IC based on RSFQ logic. A 2D MCM was constructed by flip chip bonding heater die fabricated from copper onto a superconducting tantalum carrier chip using cryogenic underfill and SWCNT integrated underfill. A silicon carrier wafer was fabricated using thin film processing techniques such as physical vapor deposition (PVD), wet etching, reactive ion etching, photolithography etc. The SC-carrier chip was wire bonded to the silicon substrate using a 25.4 µm aluminum wire wedge bonder. The change in resistance of the chip and the carrier chip was monitored using 4-wire connections. The stage temperature of the test bed was then maintained at 4 K and the electrical resistance of the chip and SC-carrier chip were monitored by heating the chip.

1.3. **Overview of Characterization Tools:**

The following section provides a brief overview of the analytical techniques used in the characterization of material and package.

1.3.1. **Scanning Electron Microscopy**

Scanning electron microscopy (SEM) is a non-destructive analytical technique where a high energy electron beam is focused onto the surface of a sample to image the surface. SEM is
an essential tool to analyze package failures, package interfaces and many other areas where an optical microscope is not sufficient. SEM imaging is usually done at magnifications of 300,000x – 500,000x. SEM operates on the principle where a high energy electron beam is emitted by an electron gun which has a tungsten filament often coated with lanthanum hexaboride. The emitted electron beam is then focused onto the sample with a help of a series of electromagnetic field lenses and a raster scan of the selected area is performed to provide the image and the signature of the material. Secondary electrons are emitted and when the energy of the incident electrons exceeds that of the work function of the sample under test which is collected by the detector. In the current research the ESEM, which stands for Environmental SEM, was used to analyze SCE-MCMs which were diced to study the underfill and bump structure after thermal test. The ESEM is just a modified version of the SEM which allows for imaging of conductive and non-conductive samples. A more detailed overview of the SEM physics, principle of operation and sample preparation procedures is detailed elsewhere [47]. Figure 8 shows the overall architecture of SEM [48] and Figure 9 is a picture of the XL-30 ESEM used in the current research.
1.3.2. Transmission Electron Microscopy

Transmission electron microscopy or TEM is very similar to an SEM where an electron beam of high energy is focused onto a test sample through a series of electromagnetic field lenses except for the fact that the electron beam in a TEM passes through the sample with the image being collected under the sample by a detector. The TEM is a very powerful tool in the fact that the resolution of a TEM is often far greater (0.1 nm) than that of the SEM (1-5 nm). For instance, in the current research the Titan 80-300 S/TEM shown in Figure 10 was used to image SWCNTs and SWCNT integrated underfill which provided a visual confirmation of the SWCNT in the cryogenic underfill and the presence of Fe nanoparticle impurities in the as received
SWCNTs. A complete explanation of the principles, components and techniques of the TEM can be found in several published books and one such book is listed here as reference [49].

1.3.3. Scanning Acoustic Microscopy

The SAM or scanning acoustic microscope is a non-destructive method for imaging materials. It is typically used in the electronics industry to study the effects of voiding between opaque substrates. It employs a ultrasound wave which penetrates into the sample upto several centimeters in depth and, based on the elastic moduli, density and other properties of the material, provides the visual image of the sample. In the current research, the Sonic UHR2000 SAM was used to image flip chip bonded SCE-MCM bonded using cryogenic underfill. Extensive overview of the operating principles of SAM can be found elsewhere [50-52].

Figure 10: Titan 80-300 high resolution TEM used in the current research to image SWCNT and SWCNT integrated underfill
1.3.4. Differential Scanning Calorimetry and Thermogravimetric Analysis

Differential scanning calorimetry (DSC) and thermogravimetric analysis (TGA) are thermal analysis techniques used to study the change in properties of a material when subjected to heat. In other words, a sample is placed in a heated environment and the change in the properties of the sample is evaluated in comparison to a reference sample. Please see reference for complete overview and principle of DSC [53].

In the current research, DSC was used to examine the glass transition temperature of the SWCNT integrated underfill and the TGA was used to study the amount of impurities present in purified SWCNTs. The DSC and TGA experiments were completed simultaneously on a given sample by placing a known quantity of sample usually 4-5 milligrams in weight inside a chamber and heating the sample from -5°C to 100°C at a ramp rate of 10°C/min in a controlled environment. The results were analyzed according to the American Society for Testing and Materials (ASTM) E 1356. The TGA was used to quantify the purity of the purified SWCNTs. A measured weight of SWCNTs (typical values of 10 micrograms) was placed in a sample holder and mounted inside the controlled environment. The sample was slowly heated (5°C/min) from room temperature to 800°C and the change in weight was plotted as a function of temperature. The residual mass in the sample holder was the quantity of impurities (typically Fe nanoparticles) present in the purified sample. This technique was used to optimize the purification process to obtain high purity SWCNTs. A detailed explanation of the TGA principles is beyond the scope of this work and has already been extensively published [54].
1.3.5. Adhesion Analysis – Pull Test

Adhesion analysis is an essential component of underfill testing. There are several ways of testing the adhesion strength of polymer adhesives, namely, peel test, pull test, shear test and tensile test. In the current research, pull test was selected as the means for analyzing the bond strength of cryogenic underfill and SWCNT integrated underfill. In the current research the Sebastian pull tester was used to study the adhesion strength of the underfill. Figure 11 is the picture of the Sebastian pull tester.

Underfill used in cryopackaging is exposed to extreme temperature which could lead to failure due to delamination, the pull test was chosen to study the adhesion strength of the

![Sebastian pull tester used for adhesion strength analysis of underfill](image)

Figure 11: Sebastian pull tester used for adhesion strength analysis of underfill
underfill. ASTM standards have been developed for various adhesion analysis and a more comprehensive overview of the ASTM standards can be found in literature [55].

1.4. Thin Film Fabrication Techniques

As extensive fabrication work was done for the fabrication of the Ta based SC-MCM, a brief overview of the various thin film processing techniques used in the current research is described as part of the current research. Detailed description of the various thin film processing techniques can be found in most micro-fabrication test books [56].

1.4.1. Physical Vapor Deposition:

One physical vapor deposition (PVD) process is a sputter deposition process where a substrate can be coated with any material. In principle, an ionized gas such as Argon (Ar) is introduced into a vacuum chamber which contains the desired film material and the substrate. The film material which is grounded is the source material; the charged Ar ions are accelerated towards the source material and dislodge the atoms from the source which are then deposited on the substrate. In the current research, titanium, copper and tantalum were deposited using a Varian 3180 and a Varian XM8 sputter deposition system. The systems used in deposition process were direct current (DC) sputter systems. The DC sputter systems used in the research work on the same principle as explained before except for the fact that the Ar ions are charged due to bombardment of the electrons from the negatively charged target which are moving towards the anode present inside the chamber. This type of PVD process is often used to deposit metals.

1.4.2. Photolithography

Photolithography is the process of defining the features of devices and circuits. This is one of the key enabling technologies for the advancement of highly integrated dense ICs. The
process of photolithography starts with a clean dry wafer onto which a thin layer of photoresist, which is a light and energy sensitive polymer material, is deposited by spin coating. The coated wafer is then soft baked for a predetermined time based on the type of photoresist used. The soft baked wafer is then aligned using a mask aligner and exposed to ultra violet (UV) light which polymerizes the photoresist which when developed result in the transfer of the features from the mask to wafer. As a note the type of photoresists that is being used to understand what will be transferred onto the wafer should be clearly understood. Photoresists are basically divided into two type’s positive and negative photoresists. In a negative photoresist the area exposed to UV light polymerizes whereas the unexposed area dissolves thereby exposing the underlying metal. A positive photoresist works exactly opposite to that of negative photoresist.

In the current research, an Eaton 6000x spin coater was used to deposit positive photoresist (AZ 4000 series) and the Suss Microtec MA150 contact aligner was used to define features on the sample wafer. The spin speed and thickness of the photoresist was determined based upon established working practices at the High Density Electronic Center (HiDEC). The exposed wafer was developed by dunking the sample wafer for a predetermined time into a bath composed of Tetramethylammoniumhydroxide (TMAH) solution.

1.4.3. Electroplating

Electroplating is a deposition process by which metal ions from a solution are deposited onto a substrate with the help of an electric field. A power supply connected to the anode helps dissolve the metal anode, freeing ions that are directed towards the cathode. As the metal ions travel towards the cathode they disassociate and plate the cathode. The thickness of the deposition is controlled by the current density, age of the plating bath and time of the process. In the current research, nickel and gold were deposited onto the substrate by electroplating. Nickel
and gold formed the under-bump metallization for the deposition of solder bumps which are described under solder bumping process.

1.4.4. Etching

Etching is the process of making permanent the desired features of a circuit. In simple terms etching is the process where the metal exposed after photolithography is removed or attacked and dissolved by an acid. There are two basic types of etching (a) wet etching and (b) dry etching.

1.4.4.1. Wet Etching

Wet etching is an isotropic process where the exposed metal is etched as well as some of the metal covered by the photoresist. A processed wafer is generally loaded into a wafer boat and the wafer boat is then dunked into an etchant tank. The etched wafer is then loaded into a spin-rinse-dry system to remove any residual acid from the wafer. As mentioned before, since this is an isotropic etching process it is generally used for etching features a few microns wide. In the current research, wet etch was used to etch the titanium and copper thin films.

1.4.4.2. Reactive Ion Etching

Reactive ion etching (RIE) is an anisotropic process which is generally used to define features which cannot be etched using wet etch. RIE is also used when the selectivity of the etching process is critical. An RIE process consists of two parallel plates in which the plasma initiated due to the charged Ar ions along with the etchant gas attack the exposed area to remove material. The etch rate of the material depends on the gas, power and time duration for the etching. In the current research, two different RIE processes were used, namely, (a) the Plasma Therm SLR 720 was used to etch the tantalum and underlying titanium during the fabrication of
the SC carrier chip, and (b) the Surface Technology System Advanced Silicon Etcher was used for thru-silicon etching during the fabrication of the carrier substrate on which the SC-MCM test vehicle was mounted.

1.5. Package Assembly Techniques:

In the previous section, the thin film processing techniques used in the fabrication of the tantalum based SC-MCM was detailed. The current section is focused on providing the readers with a brief overview of the various IC packaging techniques used in the current research.

1.5.1. Wafer Dicing

The first step after the fabrication of the SC-MCM wafer is to isolate the SC-chip and the SC-carrier chip. This is done by using wafer dicing. Wafer dicing is the process where the fabricated wafer is mounted onto a wafer holder and placed on a dicing tool. Then based upon the substrate either a metal blade or thermo-carbon based blades is used to dice the wafer at a predetermined speed. In the current research, all fabrication was done on 5” silicon wafers and a metal blade mounted on the Micro Automation MA1100 dicing tool was used for isolating the SC-chip and carrier chip.

1.5.2. Solder Bumping

The first level of interconnection between the SC-chip and SC carrier chip is the solder bump level. Typically, In-Sn is used as solder bumps in SCE devices. A solder dipping process was developed to deposit 100 micron, In-Sn solder bumps on the diced SC-chip. The process was rather simple in which the diced wafer had openings only at the gold bond pads which were opened during the fabrication process. The chip was thoroughly cleaned by a series of treatments with acetone and isopropanol. Then the chip was dunked in a beaker containing a flux which prepares the gold surface by removing contaminants from the surface. The prepped chip was
then dunked in a pot containing molten solder to form the solder bumps. The solder material leached the gold and interacted with the nickel to form spherical solder bumps. The uniformity of the process depended on the quality of the bond pad surface, temperature of the molten solder and time duration of the process. Please see the reference to have a more detailed overview [57].

1.5.3. Flip Chip Bonding

The first level of interconnection in SCE-MCM or SC-MCM is the solder bump level but the technique used to attach the chip and the carrier is called flip chip bonding. This technique was initially developed by IBM corporation in the late 90’s to increase the operation speed by reducing the interconnect length [32]. This technique is currently used for various levels of packaging in the semiconductor industry [34]. The MRSI Model 503 M precision aligner/bonder was used to flip chip bond the SCE-MCM and the SC-MCM. The basic process was to align the chip to the carrier chip by imaging that the solder bumps were aligned onto of the respective contact pads. Once the alignment check was completed the chip was placed on the carrier chip and the solder bumps were reflowed. The reflow of solder bumps created a temporary bond between the chip and carrier chip, after which the underfill was applied between the chip and carrier chip to create a robust package. Figure 12 is the illustration of a flip chip bonded package.

![Figure 12: Illustration of a flip chip bonded package](image-url)
1.5.4. Wire Bonding

Wire bonding is a process similar to the flip chip bonding process which is generally used to provide first level of interconnection between chip and carrier. There are two common wire bonding techniques (a) wedge bonding and (b) ball bonding. The basic components of the wire bonder are (1) the connecting wire which is generally aluminum or gold but recent trend has seen the use of copper wire for wire bonding, (2) the tip or head, (3) the clamp that regulates the wire, and (4) the stage which is controlled by the chestnut which is similar to that of the mouse of a computer.

The wedge bonder and the ball bonder work on the same principle where based on a predetermined pressure, force and time, the first bond was formed on a bond pad. The clamp then releases the wire in order to orient the wire towards the second bond pad to complete the bonding process. The basic difference between the two was that the tip of the wedge bonder was shaped like a wedge and uses the wedge to form the bond, whereas the ball bonder forms a ball which was then placed on the band pad by the tip. Figure 13 is an illustration of two wire bonded packages.

![Figure 13: Illustration of wire bonded package, (a) wedge bond, (b) ball bond.]

1.6. Layout of Dissertation:

This dissertation has been organized into nine chapters. Chapter 1 discusses the background and literature review of the packaging of SCE based on RSFQ devices. It also gives
a brief overview of all the different analytical tools, fabrication and packaging techniques used in the dissertation. Chapter 2 discusses the theoretical and experimental thermal analysis of SCE-MCMs. Chapter 3 discusses the motivation behind SWCNT integrated underfill and the structure properties relationship of SWCNTs. Chapter 4 discusses the thermal, electrical and mechanical properties of SWCNT underfill. Chapter 5 discusses the thermal characterization of the In-Sn solder material at 4 K. Chapter 6 discusses the packaging of SCE-MCM based on RSFQ logic using SWCNT-underfill and the thermal and electrical characterization of the same. Chapter 7 discusses the fabrication of 2D SC-MCM and Chapter 8 discusses the packaging and testing of 2D SC-MCM constructed for demonstration of normal to superconducting transition and in-situ temperature measurement of superconducting module. Finally, Chapter 9 briefly discusses the summary and the future work.
CHAPTER 2: SUPERCONDUCTING MULTIChip MODULE

The single chip SCE module consisted of an active SCE die flip chip bonded onto a passive silicon substrate. The construction and the architecture of the single chip SCE module has been discussed in Section 1.1.2 titled Single Chip Cryopackage Architecture. The concept of SCE-MCMs was realized by replacing the passive silicon carrier substrate with an active SCE carrier chip. The architecture of the SCE-MCM was a replica of the single chip cryopackage where In-Sn solder bumps were used for electrical interconnectivity between the SCE-chip and the SCE-carrier chip. Also a cryogenic underfill, namely, Trabond 2115 was purchased from Henkel Inc. and applied as underfill in the SCE-MCM cryopackage. This chapter details the properties of the materials used for thermal transport between the SCE-chip and SCE-carrier chip. Based upon the literature a theoretical model was developed and analyzed using COMSOL MultiPhysics software and the modeling results were verified by experimental study of the SCE-MCM cryopackage.

2.1. Theoretical overview

The thermal transport in a SCE-MCM was primarily via conduction. Convection and radiation do not play a significant role in thermal transport as the SCE-MCM cryopackage is kept under high vacuum (10^{-7} mTorr) or greater and enclosed using multiple radiation shields. There are two primary avenues for heat conduction from the SCE-chip to the SCE-carrier chip, namely, the In/Sn solder bumps and the cryogenic underfill. But it is well understood that metals, due to their electron dominated conductivity, are better thermal conductors in comparison to polymer based adhesives. But at low temperatures especially in the case of SCE devices which operate at 4 K, In/Sn alloy based solder bumps based upon their composition are expected to make the transition from a normal to a superconducting state [58]. BCS theory was based on the
electron-phonon interaction which leads to the formation of “Cooper pairs” where the electronic conductivity of a superconducting material decreases, thereby reducing the available electrons for heat transport. Thus heat transfer exclusively through the solder bumps could become a “bottle neck” in the realization of SCE-MCMs [59]. Drawing an electrical analogy, two resistive paths which govern the heat transport in the SCE-MCM are present in the current architecture. Figure 14 (a) shows the cross-sectional analysis of a SCE-MCM, (b) equivalent thermal resistive network in a SCE-MCM where $R_1$ was the resistance due to solder bumps and $R_2$ that of the underfill and figure 14 (c) is the illustration of a SCE-MCM cryopackage.
Figure 14: (a) cross-sectional analysis of SCE-MCM, (b) Equivalent thermal network of a SCE-MCM, (c) Illustration of a SCE-MCM cryopackage
Based upon the equivalent network, the thermal resistance between a SCE-chip and SCE-carrier chip can be reduced by modifying $R_1$, $R_2$ or both. The thermal resistance of any material is dependent on three factors (1) the thermal conductivity, (2) cross-sectional area and (3) the length or distance between the hot and cold region. This is clearly illustrated by Fourier’s law of heat conduction which states that “the rate of heat conduction through a surface is proportional to the temperature difference across the layer and the heat transfer area, but is inversely proportional to the thickness of the layer” [60] as shown in equation 2.1

$$\frac{\partial q}{\partial t} = -\kappa A \frac{\partial T}{\partial x} - \kappa A \frac{\partial T}{\partial y} - \kappa A \frac{\partial T}{\partial z}$$  (2.1)

where $\kappa$ is thermal conductivity, $A$ is the cross-sectional area, $\partial T$ is the temperature delta between the hot and cold side, $\partial q/\partial t$ the rate of heat conduction and $dx$, $dy$ and $dz$ are the thicknesses in their respective coordinate. For the current scenario equation (2.1) further simplifies to

$$\frac{\partial q}{\partial t} = -\kappa A \frac{\partial T}{\partial y}$$  (2.2)

When the heat flow is from the SCE-chip to the SCE-carrier chip and the x and z coordinates are negligible as the heat has to be dissipated through the solder bump/underfill configuration leading to an anisotropic flow of heat. Equation (2.2) can be rewritten as

$$Q' = \frac{\Delta T}{R_{th}}$$  (2.3)

where $R_{th}$ is the thermal resistance ($L/\kappa A$) of the path. Literature indicated that the thermal resistance $R_1$ due to the solder bump-metallization path was 25-30 mK/mW [25]. The prior reported work was used a SCE-chip with 48 bumps, each 100 microns in diameter, flip chip bonded to the silicon carrier substrate. Additionally, in the above reported work by Yokoyama et al., the SCE-chip was attached by reflow of the solder bumps and no underfill was used. Thus all the heat generated flows from the SCE-chip to the silicon substrate through the bumps.
Assuming that $R_1$ is 25 mK/mW a power dissipation of 2-5 mW will result in a temperature delta greater than the 50 mK threshold. Furthermore, as the packing density of the SCE-chip increases it is anticipated that the bump diameter will decrease [61]. This decreases the cross-sectional area available for heat transport which increases $R_1$. Based on the background the relationship between the bump diameter and the temperature delta for the SCE-MCM, is shown in figure 15.

**Figure 15: Relationship between the bump diameter and temperature gradient in a SCE-MCM cryopackage**

Figure 15 shows that as the bump diameter decreased the temperature delta of a SCE-MCM would be greater than 50 mK. The temperature delta could be decreased by increasing the number of solder bumps as it would increase the number of paths for heat transport. This was undesirable for two reasons, namely, (1) an increase in number of solder bumps will result in
decreasing the real estate of the SCE-chip, and (2) the probability of failure of the SCE-MCM cryopackage increases with the increase in number of solder bumps. Figure 16 illustrates the thermal resistance of the solder bumps as a result of the number of solders bumps [59].

![Figure 16: Relationship between thermal resistance of bumps to the number of solder bumps](image)

Finally, the temperature delta in SCE-MCMs was estimated as a function of the underfill thermal conductivity. Based upon literature it is well known that polymer materials due to their amorphous structures, have very low thermal conductivity at 4 K [62-68]. Thus for the same chip-carrier configuration the threshold for the underfill conductivity was estimated. It was concluded that if the thermal conductivity of the underfill was 0.04 W/mK or greater, the temperature delta between the SCE-chip and SCE-carrier chip will be within the 50 mK
threshold. Figure 17 shows the relationship between temperature delta and underfill conductivity in SCE-MCM [59].

![Figure 17: Relationship between underfill thermal conductivity and temperature gradient of SCE-MCM](image)

2.2. Thermal modeling of superconducting multichip module

Based upon the theoretical estimates in Section 2.1 the temperature delta of the SCE-MCM was studied using COMSOL MultiPhysics software. Models were created for a 5 mm x 5 mm chip flip chip bonded on a 1 cm x 1cm carrier chip with bump sizes varying from 30 micron in diameter to 100 micron in diameter. Also, the number of bumps was made constant at 220 bumps at 100 micron pitch. One dimensional steady state analysis was used with the bottom of
the SCE-carrier chip being held at 4 K and the SCE-chip power at 80W/m² and 200 W/m². Due to symmetry only one quadrant of the SCE-MCM was modeled. Additionally the role of underfill in affecting the temperature delta of the SCE-MCM was analyzed. The values for the thermal conductivity of the underfill were obtained from previous experimental work [69]. Table 2 shows the parameters of the current COMSOL model.

**Table 2.1: COMSOL Model Parameters:**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip Area</td>
<td>5 mm X 5 mm</td>
</tr>
<tr>
<td>Carrier Chip Area</td>
<td>1 cm X 1cm</td>
</tr>
<tr>
<td>Chip and carrier thermal conductivity</td>
<td>300 W/mK</td>
</tr>
<tr>
<td>Bump thermal resistance</td>
<td>25 mK/mW[25]</td>
</tr>
<tr>
<td>Bump diameter</td>
<td>100 micron</td>
</tr>
<tr>
<td>Bump height</td>
<td>10 micron</td>
</tr>
<tr>
<td># of Bumps</td>
<td>220</td>
</tr>
<tr>
<td>Bump apparent thermal conductivity</td>
<td>1.06 W/mK</td>
</tr>
<tr>
<td>Underfill layer thickness</td>
<td>10 micron</td>
</tr>
<tr>
<td>Pure Underfill (thermal conductivity)</td>
<td>0.03 W/mK [69]</td>
</tr>
<tr>
<td>Thermally enhanced underfill (thermal conductivity)</td>
<td>0.1 W/mK [69]</td>
</tr>
</tbody>
</table>

The temperature delta across the SCE-MCM was examined for bump sizes 30 – 100 microns with no underfill. This has already been illustrated in Figure 15. For the 100 micron bump packages five specific cases were examined for the temperature delta (1) as a function of pure underfill and solder bumps, (2) thermally enhanced underfill and solder bumps and (3) heat flow exclusively through the pure underfill, i.e. no solder bumps, (4) heat flow exclusively through solder bumps and (5) heat flow exclusively through thermally enhanced underfill. The current configurations were chosen as the SCE-MCM cryopackage used in all experiments had
220 bumps each 100 micron in diameter. It was observed that the temperature delta between the SCE-chip and SCE-carrier chip was 19 mK and 13 mK for Case 1 and Case 2. Additionally, when heat flow was modeled for Case 3, 4 and 5, the temperature deltas were 68 mK, 31 mK and 21 mK. The results of the thermal model are shown in Table 2.2. Figure 18 is shown as an example of the modeled temperature delta of a SCE-MCM for Case 4.

Table 2.2: Results of COMSOL Model

<table>
<thead>
<tr>
<th>Heat Flow</th>
<th>Applied Power</th>
<th>Temperature Difference between SCE Chip and Carrier Chip</th>
<th>Thermal Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bumps and pure underfill</td>
<td>5 mW</td>
<td>19 mK</td>
<td>3.88 K/W</td>
</tr>
<tr>
<td>Pure underfill</td>
<td>5 mW</td>
<td>68 mK</td>
<td>13.60 K/W</td>
</tr>
<tr>
<td>Bumps and SWCNT loaded underfill</td>
<td>5 mW</td>
<td>13 mK</td>
<td>2.60 K/W</td>
</tr>
<tr>
<td>Bumps</td>
<td>5 mW</td>
<td>31 mK</td>
<td>6.20 K/W</td>
</tr>
<tr>
<td>SWCNT underfill</td>
<td>5 mW</td>
<td>21 mK</td>
<td>4.20 K/W</td>
</tr>
</tbody>
</table>
The experimental evaluation of the temperature delta across the SCE-MCM was completed by packaging the SCE-MCM using cryogenic underfill and analyzing their thermal performance on the test bed. This involved designing the test vehicle and calibrating the temperature sensors and resistors used in the thermal characterization.

The test setup consisted of the flip chip bonded SCE-MCM being attached to OFHC plate with thermal grease acting as thermal interface material between the bottom of the carrier chip and the OHFC plate. The SCE-MCM was then mounted onto the cold head of the test bed and secured in place with 310 stainless steel screws. The stainless steel screws were chosen as they
have a low thermal conductivity. Additionally, Teflon spacers were used to insulate the SCE-MCM from the stainless steel fixture used for securing the module. A Ruthenium oxide surface mount heater was placed on the SCE-chip and calibrated silicon diode (670SD) Lakeshore temperature sensors were mounted on the chip, carrier chip and copper plate to monitor their respective temperatures. The Ruthenium oxide (RuO$_x$) heater resistance was monitored during initial cool down with the resistance at 4K being 1426 ohms. Additionally, the temperature sensors were mounted on the cold head of the cryocooler and calibrated with respect to each other. The temperature differences between the sensors were found to be 3 mK at 4 K. The error in measurement was thus assumed to be +/- 3 mK. All the connections in the test setup were done using 32 AWG phosphor bronze 4 lead wires. The wires were chosen as they are typically easier to heat sink or thermalize to the 27 K and 4 K stages of the test bed. All wire connections were done using 4-wire measurement techniques. Figure 19 shows the experimental setup for the thermal analysis of the SCE-MCM.
The SCE-chip was heated by powering the RuOx heater with the power being varied from 0 – 5 mW and monitoring the temperature of the SCE-chip and SCE-carrier chip. The temperature difference as a function of the applied power was plotted to determine the linearity of the plot. Within the plotted error bar all measurements were linear agreeing with the assumption that the primary mechanism of heat transfer is conduction. Two flip chip bonded SCE-MCMs were provided by Hypres Inc. for the initial analysis of the temperature delta. Based upon the theoretical estimate a temperature delta less than 50 mK was expected, but the experimental results indicated that the temperature difference varied from 92mK -112mK. The above SCE-MCMs were flip chip bonded using thermo-compression bonding. Additionally, the

Figure 19: Experimental setup for temperature gradient measurement of SCE-MCMs
temperature delta of the SCE-MCM was studied by flip chip bonding the SCE-chip using reflowed bumps and applying the underfill using capillary flow. The temperature delta for the reflowed SCE-MCM with no underfill was 70 mK and that of the module packaged using capillary flow resulted in a temperature delta of 58 – 59 mK. Figure 20 is the plot showing the temperature delta of SCE-MCMs and Table 2.3 summarizes the results of the experimental analysis.

![Temperature gradient measurements of SCE-MCMs](image)

**Figure 20: Temperature gradient measurements of SCE-MCMs**
Table 2.3: Summary of Experimental Measurement of Temperature Delta of SCE-MCMs

<table>
<thead>
<tr>
<th>Test Vehicle</th>
<th>Flip Chip Bonding Process</th>
<th>Heat Transport Medium</th>
<th>Temperature Delta (mK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TV-I</td>
<td>Thermo-compression</td>
<td>In-Sn bumps &amp; Underfill</td>
<td>109</td>
</tr>
<tr>
<td>TV-II</td>
<td>Thermo-compression</td>
<td>In-Sn bumps &amp; Underfill</td>
<td>92</td>
</tr>
<tr>
<td>TV-III</td>
<td>Capillary Flow</td>
<td>In-Sn bumps &amp; Underfill</td>
<td>59</td>
</tr>
<tr>
<td>TV-IV</td>
<td>Capillary Flow</td>
<td>In-Sn Bumps &amp; Underfill</td>
<td>58</td>
</tr>
<tr>
<td>TV-V</td>
<td>Reflowed Bump Bonding</td>
<td>In-Sn Bumps</td>
<td>70</td>
</tr>
</tbody>
</table>

The results in Table 2.3 indicated that for the current SCE-MCM cryopackage architecture the method of assembly was important as evidenced by the difference in temperature delta between the capillary flow bonded module and the modules bonded using thermo-compression bonding. Additionally, the temperature delta between the SCE-chip and SCE-carrier chip for the reflowed module was less than that of the module packaged using thermo-compression bonding. It was hypothesized that the thermo-compression bonding probably led to improper bump contact and higher than expected temperature delta in the SCE-MCM cryopackage. Further the present measurements showed that the thermal resistance of the bump was higher than that estimated by Yokoyama et al.. This could be due to the difference in the
composition of the In-Sn alloy used in their experiment. The characterization of the SCE-MCM is explained in the following section.

2.4. Characterization of module

2.4.1. SEM & SAM Analysis

The SCE-MCM modules which were packaged using thermo-compression were analyzed using the ESEM. First the bonded SCE-MCM was diced using the Micro Automation Model 1100 dicing tool. The diced module was then mounted on the Buehler EcoMet 3000 Polisher and polished through a series of steps using silicon carbide abrasive paper. At each processing step the size of the grit was increased which resulted in the decrease of the coarseness of the abrasive paper which helped provide a smoother finish to the surface. The last step in the polishing process was to use diamond slurry on a polishing cloth such as ChemoMet®. A detailed approach for polishing silicon based microelectronic devices can be found at the technical page on Buehler [70]. The polished module was then coated with very thin gold layer and the module was analyzed using SEM. Figure 21 shows the cross sectional view of SEM micrograph of the SCE-MCM packaged using thermo-compression bonding.
The SEM analysis showed that there were large voids between the SCE-chip and SCE-carrier chip. This would result in a bottle neck effect by forcing the heat flow through the bumps. Since the sample preparation for the SEM analysis was a destructive technique the SAM was chosen to study the extent of voiding in the SCE-MCM package bonded using capillary flow. Figure 22 shows that the voids which were present between the SCE-chip and SCE-carrier chip of the cryopackage bonded using thermo-compression bonding was absent in the cryopackage bonded using capillary flow. This was expected as capillary flow coupled with room temperature cure allows for void free packaging.
Furthermore, an uneven distribution of epoxy underfill can lead to delamination and failure of the SCE MCM cryopackage. It was expected that the presence of voids increased the thermal resistance between the SCE-chip and the SCE-carrier chip. Additionally, even with heat being forced through the bumps, based on the reported properties of the bump resistance the temperature difference between the chip and carrier was still expected to be well within 50 mK. Previous work [59] indicated that the bump contact area was decreased during the package assembly process.

### 2.4.2. Solder Bump Contact Area Analysis:

As already noted, the temperature delta between the SCE chip and SCE carrier chip decreased by 43% when the flip chip bonding process was changed from thermo-compression bonding to capillary flow bonding, it was anticipated that the bump contact area could be affected by the flip chip bonding process. This was studied by fabricating test structures and depositing In-Sn bumps on the test structures.
The test structure consisted of 1 cm x 1 cm chip with contact pads 100 microns in diameter. A 2 micron oxide layer was grown on the 5 inch wafer by thermal oxidation. A 500 angstrom thick adhesion layer of titanium (Ti) was sputter deposited using the Varian 3180 sputter system. The Ti layer was followed by a 2 micron thick copper (Cu) layer followed by another 500 Å thick Ti layer. Upon completion of the metal deposition process the contact pads were defined lithographically with a Karl Suss Microtec MA150 contact aligner using a positive photoresist. The exposed top Ti layer was wet etched using 2% HF/0.5%HNO₃ (Ti-etch) to expose the Cu. A 2 micron thick layer of nickel was electroplated onto the exposed copper which was passivated by a thin layer of gold by flash plating. Upon completion of the gold electroplating the photoresist was stripped and the lithographically defined bump metallization was wet etched using the above Ti-etch and an ammonium persulphate solution (APS 100) as copper etchant. The test wafer was then diced into individual components using the Micro Automation MA1100 dicing tool. An In-Sn solder bath was prepared by melting solder (Ind-alloy 1E) purchased from Indium corporation. The test chips were dunked vertically into a beaker containing solder flux and then slowly dunked into the solder pot containing the molten solder bath. The solder attacked the gold and formed a bond with the underlying nickel so that when the test chip was withdrawn from the solder pot the surface tension of the liquid solder helps form spherical bumps. Figure 23 shows the process flow for the fabrication of In-Sn solder bumps and Figure 24 is the optical image of the deposited solder bumps.
Figure 23: Process flow of In-Sn solder bump fabrication. (1) silicon substrate, (2) thermal oxidation, (3) PVD of metals, (4) Ti-etch, (5) electroplating, (6) wet etch of under-bump metallization, (7) dice and dip coating.
The bump contact area analysis of the thermo-compression bonding process was completed by flip chip bonding the fabricated test structures onto a glass substrate under the same conditions used for the flip chip bonding of the SCE-MCM. Four test chips were flip chip bonded to glass substrate and the bump contact area was inspected using an optical microscope. A total of 20 individual bumps were analyzed from the 4 flip chip bonded test chips. The average bump diameter of the fabricated test chips were 118 microns, upon flip chip bonding to the glass substrate the average bump contact diameter was estimated to be 83 +/- 6 microns. As a result of the thermo-compression bonding process the bump diameter was decreased by an average of 28.87%. This resulted in an average of 49.41% decrease in the bump contact area. Figure 25 shows the optical microscope measurement of the change in bump diameter.
2.5. Discussion and Conclusion

The temperature delta measurements across SCE MCMs varied from 109 mK to 58 mK depending on the method of flip chip bonding and medium for heat transport. The measurements clearly illustrated that there is a need to use capillary flow exclusively for the flip chip bonding of SCE-MCMs but capillary flow was a rather time consuming process and is not ideal for high volume manufacturing. An alternate approach is to calculate the exact amount of underfill required for the flip chip bonding of SCE-MCMs but also ensuring that the cure temperature of the cryogenic underfill is not close to the liquidus temperature of the solder bumps. As shown under the bump contact area analysis, a close match between the above will lead to reduced bump contact and eventually failure due challenges in the reliability of the bump contact. Measurements made in this research show that the cryogenic underfill did play a role in the heat transport between the SCE chip and the SCE carrier chip as evidenced by the decrease in the temperature delta from 70 mK for no underfill bonded SCE-MCM to 58 mK for SCE-MCM bonded using bump and underfill. Finally, the measurements showed a need for thermal enhanced underfill for packaging of SCE-MCMs.

Figure 25: Optical microscope analysis of change in bump diameter of a flip chip bonded test structure
CHAPTER 3: NANOENGINEERED UNDERFILL

Underfill is the material that was dispensed between the chip and carrier in a flip chip package. Flip chip technology initially demonstrated by IBM [32] has been the primary driver for the development of underfill materials and technology. Flip chip technology involves the bonding of an active die onto a substrate, which could be any material from silicon to ceramic, and the electrical interconnection between the die and the substrate was through solder balls. Thus dissimilar materials with different coefficient of thermal expansions (CTE) are brought into close contact and then subjected to the wide temperature range changing from room temperature to liquid helium temperature (4.2 K) can result in failure of the device due to solder ball failure. This was unacceptable as the cost of a cryopackage is significantly higher than those used by generic semiconductor packages. Thus it was imperative that a material be used to enable a more robust package and to protect the solder balls and the die from the environment. Initial cryopackaging efforts did not use underfill and as described by Kaplan et al. [71] demonstrated that the robustness of the flip chip bonded SCE-MCMs was greatly enhanced due to the use of underfill.

3.1. Motivation for nanoengineered underfill

Underfill materials have been integrated with micron size fillers for more than a decade but the continuous reduction in chip substrate standoff has resulted in the need for investigation of nanoparticle sized fillers. Micron sized fillers cannot be used for current SCE-MCMs as the chip substrate standoff was approximately 5-6 micron and expected to go down due to the continuous drive for short interconnects which translates into higher speed and better performance. The common practice was that the size of the filler cannot be greater than \(1/3\)rd the size of chip offset [72]. Additionally, micron size particles alter the flow profile of the underfill.
due to filler settling, which results in voids, cracking, improper solder ball contact, which in the long term will result in failure of the package [72-74]. Additionally, filler settling will also affect the glass transition temperature ($T_g$), cure profile and adhesion strength of the underfill. Thus nanoparticles provide a better alternative as fillers for underfill formulation.

Since the beginning of the 21st century nanoparticles have come to the forefront of research. Nanoparticles due to their size provide the flexibility to tailor the properties of a material. For an instance Sun et al. integrated nano-silica into epoxies to reduce the CTE of the epoxy and thus improve the mechanical properties of underfill [40-42, 58]. Ever since their discovery, carbon nanotubes have played in significant role in transforming the role of nanoparticles in electronics. Carbon nanotubes, which were the primary focus of this work, has been integrated into epoxies, oil, silicon elastomer for thermal and mechanical property enhancement of parent material [75-82]. Furthermore due to its high electrical conductivity have also been examined for the fabrication of transistors, interconnects and solder bumps [83-93]. Based upon the thermal analysis of a SCE-MCM cryopackage it was clearly shown that the packaging and performance of SCE-MCMs would greatly benefit from the use of a filler integrated underfill.

3.2. Structure and properties of SWCNTs

Discovered in 1991 by Iijima, carbon nanotubes can be classified as single walled carbon nanotube (SWCNT), multi walled (MWCNT) and double walled carbon nanotubes (DWCNT). The primary difference between the different forms of carbon nanotubes is the number of layers of graphene present. For instance, SWCNTs consist of a single graphene layer which was rolled to form a hollow cylinder. The typical dimensions of SWCNTs are 1-5 nm in diameter and several microns in length. On the other hand MWCNTs are formed when more than one
The MWCNTs combine to form concentric circles. The diameter of MWCNTs can be as large as 50 to 100 microns and about several microns long. The DWCNTs are basically a modified version of SWCNTs as they form 2 closed hollow cylinders. SWCNTs are one-dimensional nanostructures which are hollow tubes with sp\(^2\) hybridization. The electronic properties of SWCNTs have garnered a lot of interest due to the fact that SWCNTs can either be semiconducting or metallic based upon their chirality, due to which they have been explored for the fabrication of transistors [87, 94]. In the current research, SWCNT was chosen as filler for the development of a novel underfill because of their thermal properties and 1-D nanostructure. SWCNTs due to their strong covalent bonding, have no dangling bonds which allows for ballistic transport of heat. The thermal properties of SWCNTs have been investigated extensively [95-99]. It has been shown that SWCNTs have the highest known thermal conductivity of any material [46] plus the quantization of phonons at low temperature [97] leads to reduced scattering which is desirable in filler material for thermal enhancement of cryogenic underfill. Figure 26 shows the TEM image of a SWCNT bundle.
3.3. Purification of SWCNTs

SWCNT’s are synthesized in various methods such as arc discharge, laser ablation and chemical vapor deposition. But one of the most significant and high volume productions of SWCNTs is high pressure catalytic decomposition of carbon monoxide or HiPCO method. The scope of the current work was not to detail the different methods for growing SWCNTs as that has been studied by several people over the past decade. But since the SWCNTs used in the current research was purchased from an external vendor (Unidym Inc.) who synthesized SWCNTs using the HiPCO method, a brief description of the method is as follows. The use of high pressure (30 – 100 atm.) and temperature (above 1000°C) to disassociate carbon monoxide gas in the presence of iron nanoparticles formed by the decomposition of Fe (CO)₅ gas was basis
for the HiPCO method. SWCNTs nucleate and grow on the Fe nanoparticles and the quality of the SWCNTs was dependent upon the growth conditions. The HiPCO method was developed by Dr. Richard Smalley’s group and has been detailed elsewhere [100, 101]. Thus HiPCO grown SWCNTs have Fe nanoparticles as impurities. Figure 27 shown below is the TEM image of as received SWCNTs from Unidym Inc. The dark spots seen in the image was the Fe nanoparticles which are considered to be impurities.

![Figure 27: TEM image of as received SWCNTs](image)

Prior works has shown that thermal conductivity enhancement due to purified SWCNTs was 80% higher than that seen in as received SWCNTs [80]. Thus it was critical to remove these impurities from the SWCNTs. The purification of SWCNTs consists of two basic steps. First step was that the amorphous carbon shell formed around the Fe nanoparticles needs to be broken and this was done by oxidation. The second step was to detach the SWCNTs from the Fe nanoparticles.
nanoparticle and this was done by acid reflux. In the current research two processes were studied for the purification of SWCNTs, the first was a “one-pot purification” method (Process-1) which used hydrogen peroxide (H₂O₂) as the oxidizing agent and hydrochloric acid (HCl) for the acid reflux process. The second method was a multi-step heat and acid (HCl) reflux treatment process (Process-2). In Process-1, the as-received SWCNTs were sonicated for 5 mins in the H₂O₂/HCl and placed on a hot plate for stirring at an optimal temperature between 70-100ºC. After the stirring process the resulting solution was filtered through a Millipore vacuum filtration setup which uses a VCTP filter. This method was initially demonstrated by Yuhang et al. [102]. Soon after filtration the purified SWCNTs are transferred into a glass container and weighed to analyze the yield of the process. After studying the process it was decided not to use this method as the yield of purified SWCNTs were unacceptable. For an instance, when 30 mg of as received SWCNTs were purified using the Process-1 the resulting purified SWCNT weighed was only 10 -12 mg. Thus Process-2, which involved the use of an oven to anneal the as-received SWCNTs for 24 hours and then subjecting them to acid reflux for 12 hours in 6M concentration of HCl was studied. The resulting solution was then filtered using the Millipore setup. This process was repeated twice to ensure the removal of the Fe nanoparticles. The yield of Process-2 was significantly higher than that of the “one-pot purification” method. For instance, 30 mg of as-received SWCNTs purified using the second method yielded 20-25 mg of purified SWCNTs. Thus Process-2 was used to purify SWCNTs used as filler in cryogenic underfill. Figure 28 shows the experimental setup and SWCNTs floating in the HCl solution during purification indicating the absence of Fe nanoparticle. Figure 29 shows block diagram of the two processes.
Figure 28: a) Shows the Millipore vacuum filtration setup, (b) shows the SWCNTs floating in the HCl solution

Figure 29: Block diagram of the two purification processes examined in the current research
3.4. Characterization of SWCNTs

The final step before the integration of SWCNTs in underfill was the characterization of the purified SWCNTs. The characterization of SWCNTs was done by TEM, TGA and Raman Spectroscopy. The TEM technique was a qualitative analysis of the purity of SWCNTs whereas the Raman Spectroscopy and TGA are quantitative analysis of the purity and properties of SWCNTs. As shown in Figure 27, the TEM image showed the presence of dark spots due to Fe nanoparticles, so the purified SWCNTs were characterized using the HRTEM. Figure 30 shows the TEM image of the purified SWCNTs. The absence of dark spots indicated that the SWCNTs were purified in comparison to the as-received SWCNTs. To further analyze the purity of the SWCNT sample the sample was analyzed using TGA according to the procedure explained in
section 1.4.4. TGA analysis indicated that the residue left after the heat treatment was 26% of initial weight of as-received SWCNTs. This indicates 25% impurity content. Similarly the residue left from the TGA analysis of purified SWCNT resulted in <5% of initial weight yielding impurity content of <5%. Thus the impurity content which was initially well over 25% was reduced to less than 5% by purification Process-2. Figure 31 shows the TGA data of as-received SWCNTs and Figure 32 of purified SWCNTs.

![TGA data of as received SWCNTs from Unidym Corp.](image)

Figure 31: TGA data of as received SWCNTs from Unidym Corp.
The final characterization process was completed by Raman Spectroscopy which showed the diameter of the SWCNTs to be 1.15 nm (248/RBMpeak) and a G-peak/D-peak ratio of 11 – 17, indicating that the disorder in the SWCNT structure was minimal. A more extensive study of the SWCNT structure using Raman Spectroscopy please refer to the article completed by Dresselhaus et al. [103-105]. Figure 33 show the raman plot for the purified SWCNTs clearly showing the respective peaks typical for SWCNTs. Thus the purification and characterization of SWCNTs was completed.

Figure 32: TGA analysis of purified SWCNTs
Figure 33: Raman spectroscopy analysis of purified SWCNTs
CHAPTER 4: EXPERIMENTAL STUDY OF SWCNT UNDERFILL

In the current research SWCNTs were used as filler for increasing the thermal performance of the cryogenic underfill for the reasons explained in the Chapter 3. In previous work, SWCNTs have been integrated into various polymer matrices for thermal, electrical and or mechanical enhancements by various methods [106]. The cryogenic underfills are generally a polymer matrix composed of a polymer resin which was cross-linked with the help of a hardener. In the current research, Trabond 2115 epoxy resin was used as the cryogenic underfill, the primary reason for using the above epoxy was because it created a robust bond between the SCE-chip and substrate. Thus in the current research the purified SWCNTs were integrated into the epoxy resin to form a thermally enhanced underfill.

4.1. Fabrication of SWCNT underfill

Fabrication of SWCNT composites has been done by several methods, but one of the most common methods for SWCNT integration in epoxy resins was to first functionalize SWCNTs using functionalization agents. For instance, Ramanathan et al. used an amide functionalization to enhance the properties of polymer nanocomposites fabricated using SWCNTs [106-108]. Biercuk et al. used N-N dimethyl formamide (DMF) to functionalize SWCNTs for nanocomposites fabrication [81]. Others have used a more direct approach which involved processes such as grinding the SWCNT in composite or using a melt process for integration to fabricate nanocomposites [109-112]. Each of the above techniques have their pros and cons including good dispersion due to functionalization but reduced thermal enhancement due to interfacial resistance, or disordered structure due to grinding and melt processing which led lower than expected property enhancement. Since it was desired to have a method which allows for the in-situ integration of SWCNTs in underfill to create a desired thermal
enhancement, the solution processing method was chosen. Before describing the fabrication of the SWCNT-underfill, the description of the test structures and principle for thermal and electrical characterization are described below.

4.1.1.1. Design and fabrication of test structures

The thermal and electrical characterization of SWCNT integrated underfill was completed at 4 K. This required the use of test structures which were isothermal and exhibited very high conductivity. Based upon this criterion, OFHC blocks were chosen as the material for the fabrication of the test substrate. OFHC blocks were machined into 1 cm X 1cm X 1cm cubes with 4-40 tapped holes for mounting onto the 4 K stage of the test bed and 2-56 tapped holes for the mounting of calibrated Lakeshore temperature sensors (670SD) and surface mount heaters. Fourier’s Law of one-dimensional heat conduction was used to measure the apparent thermal conductivity of the samples (refer to Section 2.1). Since the thermal conductivity measurement depends on the area and thickness of the test sample there was a need to have uniform distribution of the underfill between the OFHC test structures. This required the use of a material which allowed us to hold the OFHC test structures to be held in a parallel orientation to apply the underfill sample using capillary flow while not sticking. Teflon was chosen as the base structure on which the OFHC test structures were held in parallel orientation. Figure 34 shows the setup of the test structure.

![Figure 34: Setup of Test structure](image)
4.1.1.2. Method of SWCNT underfill fabrication

Purified SWCNTs were agglomerated during the VCTP filtration process and after transfer into the glass beaker. So the processing steps involved in the integration of SWCNTs in cryogenic underfill required the SWCNTs to be dispersed uniformly in the underfill. As a first step a known quantity of purified SWCNTs was weighed according to the loading percentage in a glass beaker. A known quantity of Isopropanol (IPA) was added to the beaker and the solution was sonicated for a predetermined time limit. The process of sonication helps disperse the SWCNTs in the IPA solution. After a stable solution was formed which was indicated by the uniformity of the color of the SWCNT-IPA solution a predetermined weight of the epoxy resin was measured into the SWCNT-IPA solution and sonicated for 5-24 hours, depending on the quantity of SWCNT being integrated to form a uniform SWCNT-epoxy dispersion. After sonication the SWCNT-IPA-epoxy mixture was then placed on a stirring hot plate and the solution was maintained at 150°C and constantly stirred using a magnetic stirrer. This process was stopped when all the IPA in the SWCNT-IPA-epoxy and < 5 ml remains. After the evaporation of the IPA from the mixture the hot plate was turned off and the SWCNT-epoxy mixture was stirred until the solution was brought back to room temperature. At this stage the hardener was added to the SWCNT-epoxy mix to crosslink the resin and form the SWCNT underfill. After a 2-3 minute stirring process the SWCNT-underfill was dispensed between the OFHC test structures via capillary flow and allowed to cure overnight making the test samples ready for thermal and electrical characterization at 4 K. The block diagram of the process flow is shown in Figure 35.
4.2. Characterization of SWCNT underfill for cryopackaging

The thermal and electrical characteristics of SWCNT underfill was analyzed at 4 K. The thermal conductivity enhancement due to SWCNT loading and the transition from an electrical insulator to conductor was also determined. The following sections describe the experimental setup, the measurements and the mechanism for the thermal and electrical performance in SWCNT underfill.

4.2.1. Experimental Setup

The test structure consisted of the cryogenic underfill integrated with different loadings of purified SWCNTs sandwiched between two OFHC blocks as described in section 4.1.1 and 4.1.2. The test samples were then screwed onto the sample mount stage of the test bed, which consisted of an OFHC plate mounted on the cold finger of the GM cryocooler. Calibrated silicon
diode temperature sensors (670SD) purchased from Lakeshore Cryotronics were mounted on the stage (sink) and the top surface of the test structure to monitor temperature of the hot side and the cold side of the sample. A 1KΩ power resistor was mounted on the top surface of the copper block using 2-56 screws. The voltage of the power resistor was varied to heat the sample. All electrical connections were made with 32 AWG phosphor bronze wires which were thermalized to the 27K stage and the 4K stage to reduce the effects of parasitic heat load onto the experiments. The tests were completed in 10⁻⁶ mbar vacuum with the help of a Varian turbo pump. The vacuum and the radiation shields reduce the effects of radiation and convection. Once the sample was mounted and the electrical connections were verified the cryocooler was pumped down overnight to 4 K and allowed to stabilize for a period of at least 5-6 hours. A cartridge heater mounted between the cold finger and the sample mount stage provided the heat necessary for the sample mount stage to reach 4 K. Due to the high conductivity of copper and the negligible effects of radiation, convection and heat conduction via the wires at 4 K, the heat flows from the top plate of the OFHC block through the test sample to the bottom plate of the OFHC block to the sample mount stage. Figure 36 is an illustration of the experimental setup.
A typical thermal measurement involved incrementing the heater voltage in five or six steps and measuring the corresponding temperature of the hot stage of the sample and plotting the temperature delta across the sample as a function of applied power. Temperature across the sample was allowed to stabilize between each step over a 2 hour time period and the bulk thermal conductance was extracted from the slope between the applied power ($V^2/R$) versus $\Delta T$. $V$ was the applied voltage across the 1K$\Omega$ heater (R) and $\Delta T$ was the temperature delta across the sample. The experiments were repeated 3 times to determine the repeatability of the data.

Upon completion of the experiment the test bed was allowed to warm to room temperature by turning off the compressor. After the samples and the test bed reached room temperature the sample was removed from the sample mount stage for analysis of the cross-sectional area and thickness of the material. These measurements were completed using a
digimatic vernier caliper which measured with an accuracy of 0.00 mm. The caliper was purchased from Mitutoyo Inc. The apparent thermal conductivity of the samples was then calculated using Fourier’s law of heat conduction. The electrical conductivity of the samples were measured by mounting the test samples on the sample mount stage and replacing the heater and temperature sensor with brass washers which had wires soldered to them. Electrical conductivity measurement was completed using a 4 wire measurement technique.

4.2.2. Thermal conductivity measurement results

Figure 37 is a plot between the temperature delta and the applied power of pure cryogenic underfill. It can be seen that the plot confirms the assumption that one-dimensional conduction was the mode of heat transfer (refer to Equations 2.1, 2.2 and 2.3). The P-value of the current measurement was 3.029*10^{-18} and the R^2 value was 0.9984 indicating measurements were verified theory. The thickness of the sample was 0.52 mm and the cross-sectional area was 9.8 mm X 9.8 mm. Based upon the sample geometry and the slope of Figure 37 the thermal conductivity of the pure epoxy sample was calculated to 0.032 +/- 0.005 W/mK using Equation 2.3. Similar measurements were completed on SWCNT integrated underfill where the loading percentage of the SWCNTs was varied from 0.1 wt% to 1 wt%. Experiments were repeated to examine the deviation in the data. Figure 38 shows the temperature delta measurement of various loadings of SWCNT underfill in comparison to that of the pure cryogenic underfill.
Figure 37: Temperature gradient plotted as a function of the applied power for pure cryogenic underfill.
Figure 38: Temperature delta of varied SWCNT loaded cryogenic underfill as a function of applied power

From Figure 38 it can be seen that the thermal conductance of the cryogenic underfill increased with increased loading of SWCNT. Table 4.2 tabulates the apparent thermal conductivity of the cryogenic underfill as a function of SWCNT loading and Figure 39 shows the thermal enhancement achieved due to the SWCNT loading.
Table 4.1: Apparent thermal conductivity of cryogenic underfill by SWCNT loading

<table>
<thead>
<tr>
<th>SWCNT Loading (wt%)</th>
<th>Average Apparent Thermal Conductivity of Cryogenic Underfill (W/mK)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.032</td>
</tr>
<tr>
<td>.1</td>
<td>0.100</td>
</tr>
<tr>
<td>.2</td>
<td>0.152</td>
</tr>
<tr>
<td>.5</td>
<td>0.272</td>
</tr>
<tr>
<td>.67</td>
<td>0.132</td>
</tr>
<tr>
<td>.75</td>
<td>0.687</td>
</tr>
<tr>
<td>1</td>
<td>0.184</td>
</tr>
</tbody>
</table>

Figure 39: Thermal conductivity enhancement of cryogenic underfill due to SWCNT loading
Additionally, the bulk electrical conductivity of the samples was monitored using the 4-wire measurement technique. The electrical conductivity of underfill samples with 0%, 0.1wt%, 0.2wt% and 0.5 wt% could not be measured with the equipment available, all showing greater than 1.00 E+08 ohms resistance. SWCNT loadings of 0.67wt%, 0.75wt% and 1wt% indicated that the samples were approaching percolation threshold as their electrical resistance was detected using the Keithley DMM. For simplicity, we considered that electrical resistance less than 1.00E+08 ohms as conductive for underfills. Figure 40 shows the electrical resistance of the different SWCNT loaded cryogenic underfill at 4 K. As seen from Figure 40 the insulating nature of the underfill was compromised for SWCNT loading of 0.67wt% and higher.

![Figure 40: 4-wire electrical resistance measurement of SWCNT loaded underfill at 4 K](image)
Additionally, the thermal enhancement seen with 0.1wt% SWCNT loading was sufficient for the industry specified thermal performance of the SCE-MCM. This was demonstrated by comparing the thermal resistance of 0.1wt% SWCNT underfill to that of theoretical thermal resistance of the In-Sn solder ball. For 200 bumps, 100 microns in diameter the total bump area is 1.57 mm² which is 6.28% of underfill area (25 mm²) making the underfill as the medium of choice for heat transfer for the current solder bump material system. Figure 41 shows the comparison of the thermal resistance of 0.1wt% SWCNT underfill and In-Sn solder balls. Thus in the current research 0.1wt% SWCNT underfill was chosen as the loading for all device performance analysis.

![Comparison of the thermal resistance of In-Sn solder balls of varying diameter, pure underfill and 0.1wt% SWCNT loaded underfill](image)

Figure 41: Comparison of the thermal resistance of In-Sn solder balls of varying diameter, pure underfill and 0.1wt% SWCNT loaded underfill
4.2.3. **Interfacial resistance analysis**

The thermal conductance of the cryogenic adhesive was enhanced by ~ 3X for 0.1wt% SWCNT loading in comparison to that of pure cryogenic underfill. This 3X enhancement, when used to estimate the thermal resistance between the SCE-chip and SCE-carrier chip resulted in lowering the temperature delta below the 50 mK design constraint provided the interfacial resistance between the underfill and passivation layer of SCE-MCMs was insignificant. To determine the true thermal conductivity the interfacial resistance between the underfill and the passivation layer was analyzed.

When two dissimilar materials are brought into contact there exists a resistance between the two materials due to surface roughness and intrinsic difference in the properties of the material. This resistance is generally called interfacial resistance or Kapitza resistance named after Kapitza who first discovered this phenomenon in 1941. Since its discovery several researchers have extensively studied their importance for various materials and systems which operate at room temperature or at ultra-cold temperatures of a few mK [113-124]. These studies have led to the use of a new material called Thermal Interface Material (TIM) such as In-foils, Apiezon grease etc., which are specifically used to reduce the Kapitza resistance between two different materials. Additionally, the discovery and integration of nanoparticles has increased the focus on the study of Kapitza resistance in nanocomposites [118, 125-131]. Though most of the above analysis of Kapitza resistance in nanocomposites was either theoretical or at room temperature it does bring the significance of the interfacial resistance in realizing the enhanced thermal transport between different materials.

In this research, the study of interfacial resistance for an underfill-passivation for 4 K applications was significant to understand if the enhancement in bulk thermal conductance due to
SWCNT loading would be seen in the heat transport in SCE-MCMs. Thus the thermal conductivity of the cryogenic underfill was analyzed by studying the role of interfacial resistance between the underfill and the final chip passivation layer for both pure cryogenic underfill and 0.1wt% SWCNT underfill.

The experimental measurement of interfacial resistance between the underfill and passivation layer necessitated the use of oxidized silicon chips. A 125 mm silicon wafer with a 2 micron thermally grown oxide layer provided by HiDEC was used as the sample for all the interfacial resistance measurements. The wafer was diced into 10 mm X 10 mm test chips using the dicing tool. Silicon being an excellent thermal conductor at 4 K, allowed for the treatment of the test chips as isothermal structures which allowed the heat transport from the top chip through the underfill to the bottom chip. This measurement approach was similar to that explained in section 4.2.1. Since silicon chips are fragile and do not allow for the drilling of tapped holes, surface mount heaters were used in the measurements. Figure 42 shows the experimental setup for the measurements.

![Figure 42: Experimental setup for interfacial resistance measurements](image-url)
A Teflon holder was used to hold the test chips in parallel to one another. The Teflon holder enabled control of the thickness of the underfill, and capillary flow along the vertical direction was used to fill the gap between two adjacent test chips. The rest of the experiment was as explained in section 4.2.1. Table 4.3 shows the results of the measurement and Figure 43 shows the plot of the thermal resistance of the underfill as a function of the thickness.

### Table 4.2: Results of Thermal Resistance Measurements of Underfill with varying Thickness

<table>
<thead>
<tr>
<th>Sample Type</th>
<th>Sample Thickness (mm)</th>
<th>Thermal Resistance (K/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 wt% SWCNT Underfill</td>
<td>0.65</td>
<td>330.49</td>
</tr>
<tr>
<td></td>
<td>0.16</td>
<td>152.16</td>
</tr>
<tr>
<td></td>
<td>0.22</td>
<td>135.59</td>
</tr>
<tr>
<td></td>
<td>0.47</td>
<td>318.01</td>
</tr>
<tr>
<td></td>
<td>1.22</td>
<td>496.52</td>
</tr>
<tr>
<td></td>
<td>0.42</td>
<td>345.20</td>
</tr>
<tr>
<td></td>
<td>0.66</td>
<td>390.99</td>
</tr>
<tr>
<td></td>
<td>1.20</td>
<td>533.21</td>
</tr>
<tr>
<td>Pure Underfill</td>
<td>0.59</td>
<td>507.76</td>
</tr>
<tr>
<td></td>
<td>1.20</td>
<td>937.99</td>
</tr>
<tr>
<td></td>
<td>0.75</td>
<td>524.87</td>
</tr>
<tr>
<td></td>
<td>0.95</td>
<td>603.06</td>
</tr>
<tr>
<td></td>
<td>0.25</td>
<td>291.65</td>
</tr>
<tr>
<td></td>
<td>0.67</td>
<td>472.80</td>
</tr>
<tr>
<td></td>
<td>0.17</td>
<td>280.32</td>
</tr>
<tr>
<td></td>
<td>0.04</td>
<td>146.06</td>
</tr>
</tbody>
</table>
Given the fabrication method and the unknown properties of the composite such as CTE, cross-linking density, degree of cure and the role of SWCNT on the above properties make it difficult to predict an exact value for the interfacial resistance. But in order to do a feasibility evaluation of the interfacial thermal resistance of pure underfill and 0.1wt% SWCNT underfill a linear relationship was assumed according to Fourier’s heat transfer [60]. Comparing Equations 4.1 of pure underfill and Equation 4.2 of 0.1wt% SWCNT underfill to the Fourier’s heat transfer Equation shown in 4.3, the Kapitza resistance in both cases was estimated to be 66.445 * 10^-6 m^2 K/W for pure underfill and 65.115 * 10^-6 m^2 K/W for 0.1wt% SWCNT underfill.
\[ R_{th} = 584.95x + 132.89 \quad (4.1) \]
\[ R_{th} = 332.56x + 130.23 \quad (4.2) \]
\[ R_{th} = \frac{L}{\kappa A} + 2R_e \quad (4.3) \]

Additionally, the thermal resistance for the 0.1wt% SWCNT underfill was 1.76 times smaller than that of pure underfill. Though the above enhancement seen is smaller than that seen in earlier measurements, this was expected due to the difference in properties of silicon test structures in comparison to OFHC block used in prior measurements. Thus in the current experiments the heat transfer between SWCNT and the polymer matrix was significant as evidenced by the 1.76X increase in thermal conductance for 0.1wt% SWCNT loaded underfill over pure epoxy underfill in a flip chip silicon test structure. But in both cases the heat transfer between the underfill and the passivation layer is hindered by the interfacial resistance. Based on the current measurements it was seen that there was a need for better coupling between the underfill and the passivation layer in order to take advantage of the thermal enhancement provided by the SWCNT loading in underfill.

4.2.4. Thermal conduction mechanism

Thermal conductivity of polymers and all non-metals is due to phonons or lattice vibrations. The phonon conductivity is dependent on the various intrinsic properties of the polymers such as crystallinity, cross-linking density, filler size and the temperature at which the polymer is used. The low temperature thermal property of polymers has been investigated by several authors as it defines the mechanisms of heat conduction [62-67].

The general consensus is that polymers, particularly, thermosetting polymers which are the primary materials used as underfill, have very low thermal conductivity due to their highly disordered structures. Additionally, it has been demonstrated experimentally that as the filler size
in polymers decrease a corresponding decrease in the thermal conductivity was also observed [66-68]. The primary reason for the decrease in thermal conductivity due to filler size has been attributed to the increase in the Kapitza resistance between the filler particles and polymer matrix. For instance Garrett et al. studied the thermal conductivity of polymers filled with non-metallic powders and concluded that the low temperature (4 K) thermal conductivity of filled polymers was lower than that predicted by theory. Furthermore, he states “At liquid helium temperature there is a profound size effect.” He illustrates in his measurement that the thermal conductivity of 1.8 µm filler size of corundum filled polymer was 62.963% lower than that of pure unfilled and 73.33% lower than that of 63 µm size corundum filled polymer [68]. Araujo et al. in his studies of metal powder filled polymers also demonstrated a similar size dependent thermal conductivity of filled polymers where, the thermal conductivity of unfilled polymer was significantly higher than that of filled polymers [67].

In this research, SWCNTs, which are anisotropic nanofillers, were integrated into the polymer resin for the fabrication of a thermally enhanced underfill. According to theory, there are two primary reasons why fillers can improve the thermal properties of polymer material. First, the integration of fillers reduces the cross-linking density of thermosetting polymers which in turn reduces the junctures for phonon scattering. Second, if the acoustic properties of the filler are similar to that of the polymer then the scattering due to boundaries was also reduced.

The thermal enhancement due to SWCNT loading was shown by the decrease in the thermal resistance of 0.1wt% SWCNT underfill in comparison to pure underfill. Based upon the earlier explanations, it was assumed that the integration of SWCNTs decreased the cross-linking density of the polymer matrix. Additionally, as the temperature decreased the mean free path of phonons increased and in SWCNTs the mean free path of phonons approached that of the length.
of the SWCNTs, leading to quantization of phonons and scattering at the nanotube ends [97, 132]. Furthermore researchers have reported that the density of SWCNTs is 1.3 -1.4 g/cm$^3$ [133] which closely matches that of the polymer underfill which was 1.22 g/cm$^3$ as seen from the data sheet provided by Henkel Corp. Thus the intrinsic thermal conductivity of SWCNTs, the mean free path of phonons and the close match in the physical properties between SWCNT and polymer provides the thermal enhancement observed in the research.

4.2.5. Electrical conduction mechanism

The electrical conduction mechanism was based upon the percolation theory. It is not within the scope of this dissertation to explain the percolation theory as it has been studied with respect to carbon nanotube composites by several authors [38, 75, 76, 88, 126, 134-136]. When conductive fillers such as SWCNTs and metal fillers are integrated into a non-conductive matrix, there is a critical filler concentration after which the conductive particles come into contact with one another forming a closed path. This threshold at which a non-conductive material transitions from an insulator to an electrical conductor was called the percolation threshold. In the current research, the SWCNT loading of 0.5wt% and lower were non-conductive but SWCNT loadings of 0.67wt% and higher were conductive indicating that the percolation threshold was reached. This was clearly shown in Figure 40.

4.2.6. Adhesion testing

The adhesion test was completed using the Sebastian Pull tester described in section 1.4.5. 1 cm x 1cm oxidized (2 µm thick oxide) silicon test chips were used as the substrate. The test chips were cleaned using acetone, IPA and then dry baked in a oven at 120°C for 5 minutes to remove any moisture present on the surface. Aluminum studs purchased from Quad group were cleaned using the same process described above. The stud was dipped into the various
SWCNT loaded underfills; the excess underfill was allowed to drip and the stud was allowed to bond to the test chip with the weight of the stud to form an uniform bond thickness. The samples were cured overnight at room temperature. A minimum of 5 samples were prepared for each underfill. Two conditions were tested for the cured samples. First set of samples were cured and tested using the pull tester whereas the second set of samples after curing were heated to 140°C for 1 hour in the oven and allowed to cool back to room temperature before completing the pull test. The sample heating was chosen to check the effect of temperature on the adhesion strength of the underfill material. Figure 4 shows the steps of the adhesion test and Figure 45 plots the adhesion strength as a function of SWCNT loading for the two conditions.

Figure 44: Shows the steps of the adhesion test. a) Test chip bonded to silicon test chip using SWCNT underfill, b) Test chip mounted on the Sebastian pull tester, c) Sample after completion of the pull test.
From Figure 45 it can be seen that for the underfill samples which were not subjected to heat treatment the adhesion strength decreased with increased loading. This was expected as the inclusion of SWCNTs greatly modifies the cross-linking density of the underfill thereby making it easier to pull the stud from the test chip [137-139]. Comparing the adhesion strength of each SWCNT loadings with respect to the two treatments the heat treated samples show a higher adhesion strength with respect to their room temperature cured counterparts. The increase in adhesion strength can be attributed to a post curing effect which leads to an increase in the cross-linking density where secondary and tertiary bonds are expected to be formed which results in
the increase in adhesion strength. Thus from this experiment it can be concluded that SWCNT inclusion does affect the cross-linking density and adhesion strength of the underfill.

4.2.7. Glass transition analysis

Based upon the observations made during the adhesion tests it was determined that the SWCNT inclusion affected not only the physical property of the underfill but could also affect the chemical property of the underfill. To test this hypothesis the glass transition temperature, which is the temperature at which an epoxy becomes flexible, was chosen as the parameter to be studied as a function of SWCNT loading. The DSC was chosen as the method for analyzing the glass transition temperature of the underfill and the tests were completed according to ASTM E1356. Samples of SWCNT underfill were prepared as per the fabrication process described in Section 4.1.2. The samples were allowed to cure overnight at room temperature after which it was cut into pieces of 10 mg weight. The samples were then subjected to test method described under Section 1.4.4. Figure 46 is a plot of the glass transition temperature of underfill as a function of the SWCNT loading.

Figure 46 indicated that the glass transition temperature of the underfill increased for 0.1wt% and 0.2wt% SWCNT loadings but SWCNT loadings of 0.5wt% and higher resulted in the glass transition temperature being closer to that of pure underfill. This work indicates that SWCNT loading did affect the chemical property of the underfill and requires a more fundamental study to understand the relationship between SWCNTs and the polymer matrix.
Figure 46: Plot of glass transition temperature of underfill as a function of SWCNT loading

4.2.8. Conclusion

The thermal and electrical properties of the cryogenic underfill were studied at 4 K and the mechanical property was analyzed at room temperature. It was concluded that SWCNTs greatly enhances the thermal conductance of the cryogenic underfill due to reduced cross-linking density, reduced acoustic mismatch and one dimensional heat flow along the longitudinal axis of the SWCNTs. Furthermore, the thermal conductance of the cryogenic underfill has been
increased by 1.76X times due to 0.1wt% SWCNT loaded underfill in comparison to pure cryogenic underfill, when tested as in a flip chip bonded silicon test structure making it suitable for application as an underfill material for SCE-MCMs. Thus for future work 0.1wt% SWCNT loading was chosen as the loading concentration for the flip chip bonding of SCE-MCMs. The percolation threshold for the SWCNT underfill was determined to be around 0.67wt%, which opened avenues for the fabrication of SWCNT integrated solder bumps. Based on the findings of the current research it was seen that there are various areas for SWCNT epoxy applications. For instance, loadings of 0.1, 0.2 and 0.5 wt% can be used as underfill for flip chip bonded SCE-MCM. SWCNT loadings of 0.65wt% and greater can be used as die attach and for polymer based bumps and resistors. Figure 47 shows the different areas of value based on the thermal and electrical properties of the SWCNT epoxy and Figure 48 shows the TEM image of SWCNT loaded underfill.
Figure 47: Areas of interest of the SWCNT epoxy for cryogenic applications

Figure 48: TEM image of SWCNTs in epoxy
CHAPTER 5: THERMAL CHARACTERIZATION OF INDIUM-TIN SOLDER BUMPS

5.1. Introduction

The primary difference in thermal transport between metals such as In-Sn and underfill are the dominant charge carriers. In metals the primary carriers for heat are electrons whereas it is the lattice vibrations or phonons which are the primary carriers for non-metals such as underfill. This will be the case for pure metals but as the impurity content in a sample increases there is a corresponding decrease in the thermal conductivity of the metal [140].

At low temperatures there are two important factors which affect the thermal conductivity of metals, namely (a) the impurity content and (b) the interaction between electrons and phonons. Equation 5.1 shows the two components of thermal resistance of metals [140].

\[ W = W_o + W_i \]  

where \( W \) is the total thermal resistance, \( W_o \) the thermal resistance due to phonons and \( W_i \) the thermal resistance due to impurities. In the case of pure metals the electronic contribution dominates the lattice contribution as reported by several researchers [1, 140-150]. Thus the lattice contribution was generally ignored for pure metals but in the case of alloys the scattering due to impurities or the alloys can greatly affect the role of the thermal carriers. For instance, in his study of the thermal conductivity of German silver alloy Berman reports that the electronic contribution to the thermal conductance was decreased due to the presence of impurities [151].

Similarly, in their experimental work Olsen and Rosenberg report that the thermal conductivity due to electrons in alloys was reduced by the presence of impurities to that of the lattice conductivity. Additionally, literature indicates that the In-Sn alloy could transition to superconducting state which further decreases the electronic contribution to thermal conductivity due to the decrease in number of free electrons. This phenomenon was reported by Olsen et al.
during the experimental study of thermal conductivity of Lead. Figure 49 shows the difference in the thermal conductivity of lead at normal and superconducting state [145]. This phenomenon was based on the fundamental theory of superconductivity i.e. when a metal transition to the superconducting state electrons of opposite spin couple together to form an electron fluid which can travel without scattering. Thus it was critical to experimentally measure the thermal conductivity of the In-Sn alloy used in this research.

Figure 49: Thermal conductivity of lead in superconducting and normal state [152]
5.2. Sample preparation

The experimental study of the thermal conductivity of the In-Sn alloy used in this research was completed by first fabricating solder bump cylinders and measuring the thermal conductivity at 4 K. The In-Sn alloy (Ind alloy 1E) used as solder balls in SCE devices was purchased from Indium Corp. The alloy was composed of 52 parts of In and 48 parts of Sn. The material was sold as either spheres of certain diameter which can be directly placed on the SCE-chip or slugs which can be molten using a hot pot and deposited onto the SCE-chip by solder dipping process. In this research the solder balls were deposited via solder dipping so the slugs were purchase.

Three Teflon blocks with holes of diameter of 4 mm was used as the casting block. The height of the Teflon blocks was varied to check the variation in the measured thermal conductivity values. The Teflon block was placed onto a clean oxidized silicon chip which was 10 mm x 10 mm in area. The setup was then placed on top of a hot plate whose temperature was maintained at 125°C. The In-Sn slugs were then dropped into the hole and allowed to melt. In-Sn material was added until the molten material was above the hole. The samples where then cooled to room temperature to form In-Sn cylinders.

5.3. Thermal conductivity measurement

The samples were then placed between two clean 10 mm x 10 mm oxidized silicon test chips and a thin layer of Apiezon thermal grease was applied between the samples and the test chips to fill the voids and reduce the effects of interfacial resistance. The setup was then clamped using setup similar to that used for the temperature delta analysis of SCE-MCMs described in Section 2.3. Surface mount heaters and temperature sensors used in Section 2.3 were used in the current analysis. Figure 50 shows the experimental setup.
The test samples were mounted onto the sample mount stage and cooled to 4 K. The temperature was allowed to stabilize overnight and the measurements were completed by incrementing the applied power in steps and measuring the temperature of the hot and cold side of the samples. The thermal resistance was determined from the plot of the temperature delta across the test samples as a function of applied power. The plots were linear for each sample and the thermal conductivity of the samples were determined from the Fourier’s law for heat conduction. The measurements indicated a dependence of thermal conductivity on the thickness of the samples. For the short samples (~5 mm tall) the calculated thermal conductivity varied from 0.12 W/m-K to 0.19 W/m-K. For the tall samples (~15 mm tall) the calculated thermal conductivity of the In-Sn alloy varied from 0.22 W/m-K to 0.29 W/m-K. This variation indicated

Figure 50: Experimental setup of the thermal conductivity measurement for In-Sn alloy at 4 K
that the sample fabrication, test setup and measurement technique used were not valid for determining the absolute thermal conductivity of the In-Sn alloy.

Table 5.1: Thermal Conductivity of In-Sn Alloy at 4 K

<table>
<thead>
<tr>
<th>Test#</th>
<th>Sample Thickness (mm)</th>
<th>Diameter (mm)</th>
<th>Area (mm$^2$)</th>
<th>$R_{th}$</th>
<th>$\kappa$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>15.20</td>
<td>3.98</td>
<td>12.44</td>
<td>6527.0</td>
<td>0.19</td>
</tr>
<tr>
<td>2</td>
<td>5.11</td>
<td>3.95</td>
<td>12.25</td>
<td>1425.0</td>
<td>0.29</td>
</tr>
<tr>
<td>3</td>
<td>14.98</td>
<td>4.10</td>
<td>13.20</td>
<td>7981.3</td>
<td>0.14</td>
</tr>
<tr>
<td>4</td>
<td>5.01</td>
<td>4.11</td>
<td>13.27</td>
<td>1523.3</td>
<td>0.25</td>
</tr>
<tr>
<td>5</td>
<td>14.94</td>
<td>3.95</td>
<td>12.25</td>
<td>8552.0</td>
<td>0.14</td>
</tr>
<tr>
<td>6</td>
<td>4.89</td>
<td>3.99</td>
<td>12.50</td>
<td>1812.0</td>
<td>0.22</td>
</tr>
<tr>
<td>7</td>
<td>13.98</td>
<td>4.15</td>
<td>13.53</td>
<td>8355.0</td>
<td>0.12</td>
</tr>
<tr>
<td>8</td>
<td>5.20</td>
<td>4.10</td>
<td>13.20</td>
<td>1636.1</td>
<td>0.24</td>
</tr>
</tbody>
</table>

mean 0.20  
deivation 0.06
5.4. Conclusion

The measured thermal conductivity though not an absolute value was compared to the thermal resistance obtained through the thermal analysis of SCE-MCMs where the heat flow was via the solder balls. From Table 2.3 in Section 2.3 the temperature delta for reflow bonded chip was 70 mK for 5 mW of power dissipation. Thus the thermal resistance for the solder ball path was 14 mK/mW. The SCE-MCM tested had 220 bumps and if the expected solder ball contact diameter is 100 µm then the thermal conductivity of a single solder ball was 0.20 W/mK at 4 K, which agreed well with the average value of the thermal conductivity estimated in this measurement. Though the measured thermal resistance was 2X times smaller than that used for modeling, this was not unexpected as the composition (ratio of In-Sn) of the solder balls used in
the literature was unknown. Also, the effects of CTE, pressure, impurity content are also unknown for the current samples.

A more accurate way of estimating the thermal conductivity would be to evaporate In-Sn alloy in a controlled environment onto the test chip. This would prevent the contamination of the sample. Then test chips with the deposited In-Sn solder should be flip chip bonded by using thermo-compression bonding and annealed at the liquidus temperature. This will help the In-Sn alloy form a strong bond and increase the probability for a void free test structure. Finally, the test structure should be placed between holders of known CTE and thermal conductivity to ensure uniformity of pressure and temperature during experimental analysis. Considering the trend towards miniaturization, it seems beneficial to replace the In-Sn solder balls with Cu solder balls to increase thermal and electrical performance of SCE-MCMs.
CHAPTER 6: PACKAGING AND TESTING OF RSFQ SCE-MCM CRYOPACKGE USING SWCNT UNDERFILL

6.1. SCE-Device

SCE test chip and carrier test chip designed and fabricated by Hypres Inc. was provided for packaging and testing. The SCE-chip and carrier chip contained 20 JJ’s for monitoring the critical current of the devices. Additionally the SCE-chip was provided with serpentine heaters for heating the chip to study the change in $I_c$ as function of on-chip power dissipation. Figure 52 show the JJ’s of the SCE test chip and SCE-carrier test chip and Figure 53 shows the image of the serpentine heaters on the SCE-chip.

![Figure 52: Cad image of the JJ’s of the SCE-chip and SCE-carrier chip](image-url)
The SCE-chip was bumped using the solder dipping process and flip chip bonded using thermo-compression bonding to keep the flip chip bonding method similar to that used by Hypres Inc. The single chip SCE-MCM was flip chip bonded using the 0.1 SWCNT underfill developed in this research. The SWCNT integrated SCE-MCM was then tested in a thermal tuning cryo-probe used by Hypres Inc. for testing of their single chip SCE-devices at 4.2 K. The cryo-probe was then immersed in a liquid helium Dewar and the $I_c$ of the SCE-MCM was measured at 4.2 K. An oscilloscope was used to measure the $I_c$ and an Oxford cryogenic
temperature controller was used to monitor the probe temperature. Figure 54 shows the test setup used for the electrical characterization of the SWCNT integrated SCE-MCM cryopackage.

![Figure 54: Test setup for the experimental analysis of the electrical performance of SCE-MCMs at 4.2 K](image)

6.2. Experimental validation of electrical performance of SWCNT integrated RSFQ MCM cryopackage

The first step in the electrical characterization was to measure the I-V characteristics of the SCE-MCM cryopackage. The voltage was increased until the \( I_c \) of the JJ’s was observed on the oscilloscope with respect to the temperature of the cryopackage. The temperature of the cryopackage was varied by positioning the cryo-probe over the liquid helium and allowing the helium vapor to cool the cryo-probe while simultaneously allowing for the heater mounted on the
to heat the cryopackage. The $I_c$ was measured after the temperature was stabilized, which took approximately 30 minutes to an hour for each measurement. The temperature was varied from 4.2 K to 8 K to monitor the trend of the $I_c$ with respect to temperature. Figure 55 shows the $I_c$ of the SCE test chip in the MCM architecture as a function of the cryopackage temperature.

![Figure 55: Plot showing the $I_c$ as a function of temperature for SCE-Chip packaged using SWCNT underfill](image)

The electrical analysis of the $I_c$ as a function of temperature demonstrated that the $I_c$ current and the performance of the SCE-chip and SCE-carrier chip was not affected by the integration of SWCNTs nano-filler in the underfill. The electrical integrity of the SCE-MCM was not affected as the $I_c$ of both the chip and the carrier chip successfully passed the electrical
test. Figure 56 shows the theoretical $I_c$ as a function of temperature. Comparing Figure 56 to Figure 55 shows that the trend in $I_c$ as a function of temperature was similar to theoretical values [6].

Similarly the $I_c$ vs. temperature was plotted for the SCE-carrier test chip of the SCE-MCM. Figure 57 shows $I_c$ vs. temperature was plotted for the SCE-carrier test chip which indicated a similar agreement with the theoretical $I_c$. Additionally, the SCE-MCM was thermal cycled 5 times between room temperature and 4.2 K by dunking the test probe in liquid Helium. The $I_c$ vs. temperature measurement was repeated to see if there was any change in $I_c$ due to thermal cycling. Figure 55 and Figure 57 indicated that there was no detectable change in $I_c$. 

Figure 56: Theoretical $I_c$ as a function of temperature for Josephson Junction of SCE-IC
As the next phase of the electrical analysis, it was chosen to see if the $I_c$ can be used to define the temperature delta between the SCE-chip and SCE-carrier chip. This required varying the temperature in small increments of 0.1 K from 4.2 K to 5 K and monitor the $I_c$ of the SCE-chip and SCE-carrier chip. The $I_c$ of the SCE-chip decreased from 0.285 mA at 4.2 K to 0.259 mA at 5.0 K. Similarly the $I_c$ of the SCE-carrier chip decreased from 0.279 mA at 4.2 K to 0.256 mA at 5.0 K. Due to the use of an oscilloscope for measuring $I_c$ the accuracy of measurements were 5 mA. Figure 58 shows the plot of the $I_c$ of the SCE-chip and SCE-carrier chip as a function of temperature for the temperature range of 4.2 K to 5.0 K.
Finally, it was chosen to examine the I_c as a function of the on chip power dissipation. The on chip heater whose measured resistance was 114.2 ohms was connected to an Agilent power supply and the applied power was varied from 0 Amps to 0.01 Amps. The applied current was varied in steps of 0.001 Amps and the I_c of the SCE-chip and SCE-carrier chip were measured for temperature range of 4.2 K to 5.0 K. Figures 57 and 58 show the plot of I_c for the SCE-chip and SCE-carrier chip as a function of the on chip power dissipation.

![Figure 58: Plot shows the I_c as a function of on-chip power dissipation for SCE-carrier chip](image)

Based up on these measurements the I_c of the SCE-chip and carrier chip were compared to estimate the temperature delta across the single chip SCE-MCM cryopackage. Since the error in the current measurement due to the instrumentation was 5 mA it was not possible to determine
the temperature delta between SCE test chip and SCE carrier test chip. So it was not useful to study the in-situ temperature measurement. Thus the \( I_c \) measurement was used to estimate the nature of the heat transfer in the SCE-MCM cryopackage. Figure 59 shows the \( I_c \) for the SCE carrier test chip as a function of the on-chip power dissipation at 4.2 K.

![Plot showing \( I_c \) as a function of applied power at various temperatures](image)

**Figure 59:** Plot shows the \( I_c \) of the SCE-chip as a function of the on-chip power dissipation.
As the final measurement the $I_c$ was monitored as a function of applied power at 4.2 K. Figure 60 shows that the $I_c$ of the SCE-chip started to decrease at 2 mW of on chip power dissipation and that of the SCE-carrier chip started to decrease at 6 mW. This indicated that there was local heating of the SCE-chip even at 4.2 K which did not affect the performance of the SCE-carrier chip which was cryocooled with an OFHC block. To understand the thermal performance the tested SCE-MCM module was then analyzed on the test bed at Arkansas.

Figure 60: Plot shows the $I_c$ of the SCE-Chip and SCE-Carrier chip as a function of on-chip power dissipation
6.3. Experimental validation of thermal performance of SWCNT integrated RSFQ MCM cryopackage

The single chip SCE-MCM whose electrical performance was studied was used for thermal analysis on the GM test bed. The thermal analysis was completed by mounting temperature sensors and surface heater on the SCE-MCM. The temperature of the SCE-chip and SCE-carrier chip were monitored to study the temperature delta across the SCE-MCM cryopackage. The experimental method and test setup used for the thermal analysis was the same as explained in section 2.3. Figure 61 shows the plot of the temperature delta between the SCE-chip and SCE-carrier chip as a function of applied power.

![Figure 61: Plot between the temperature gradient across the SCE-MCM as a function of the applied power](image_url)
6.4. Discussion and Conclusion

The electrical and thermal analysis demonstrated that SWCNT integration in cryogenic underfill does two things. First the thermal performance of the SCE-MCM is enhanced as indicated in Figure 61. When the results of the thermal performance of SCE-MCM are compared with respect to pure cryogenic underfill, no underfill and 0.1wt% SWCNT loaded cryogenic underfill, the 0.1 wt% SWCNT loaded cryogenic underfill performed better than the pure cryogenic underfill and no underfill. Figure 62 shows the comparison between the thermal performance of a SCE-MCM bonded using pure epoxy and 0.1wt% SWCNT loaded epoxy.

![Figure 62: Plot comparing the performance of SCE-MCM packaged using pure underfill, 0.1wt% SWCNT loaded underfill and no-underfill](image-url)
Second, the integration of SWCNTs in cryogenic underfill did not affect the electrical performance of the SCE-MCMs, which by their nature have been susceptible to performance degradation due to dust and magnetic materials. Third, though this was systematically studied the integration of SWCNTs in cryogenic underfill did not seem to affect the adhesion strength of underfill and cause delamination when thermal cycled between room temperature and 4 K. Thus the goal of integrating SWCNTs and studying the thermal and electrical performance of SWCNT underfill was successfully completed.
CHAPTER 7: DESIGN AND FABRICATION OF 2D TANTALUM SC-MCM

The thermal measurements reported in Chapters 2-6 were made using surface mount heaters and resistors. To study the thermal performance of a SC-MCM in a 2D architecture, the in-situ temperature of the heater chip and superconducting carrier chip were measured. The following sections discuss the design and fabrication of the 2D SC-MCM

7.1. Design and fabrication of 2D MCM test vehicle

The 2D SC-MCM test vehicle consisted of 4 heater chips fabricated with copper as the conductor. The heater chips were flip chip bonded onto a tantalum based carrier chip. Tantalum has a critical temperature of 4.4 – 4.5 K [6]. Thus tantalum was chosen as the metal for the demonstration of transition from normal to superconducting state. The 2D SC-MCM was then mounted on a silicon wafer which was used as the substrate. The in-situ temperature of the heater chip and SC carrier chip were measured by monitoring the change in electrical resistance and using the temperature coefficient of resistance to analyze the thermal performance.

The heater chip was 10 mm x 12 mm with serpentine structures for heating the chip as well as temperature sensing. The carrier chip was 24 mm x 30 mm with serpentine structures for temperature sensing. The silicon substrate was a 125 mm silicon wafer which had bond pads for wire bond connections with the SC-carrier chip and bond pads for input/output connections for room temperature electronic interface. Since the testing required just the basic serpentine structure for heating and temperature sensing, the flip chip mask designed for studying the reliability of conductive polymer flip chip assemblies was used. The heater dimensions were 34.2 cm in length, 0.012 cm in width and 2 μm in thickness. The dimensions of the temperature sensor on the heater chip were 14.25 cm in length, 40 μm in width and 2 μm in thickness. The
temperature sensor on the carrier chip also had dimensions the same as the temperature sensor on the heater chip except that the thickness was 1500 A.

7.2. Fabrication of 2D SC-MCM

The 2D SC-MCM had three distinct process flows for the fabrication of the heater die, superconducting carrier die and the silicon substrate. Each process had a distinct difference in fabrication.

7.2.1. Heater Die

The heater die was fabricated using copper as the conductor. The fabrication process started with a 125 mm oxidized silicon wafer which was rinsed using the Spin Rinse Dry (SRD) tool at HiDEC. The clean wafers were then loaded into the 3180 Varian Sputter and subjected to RF etch to clean the wafer and prepare the wafer for metal deposition. 500°C of Titanium (Ti) was deposited on the silicon oxide followed by 2 µm of Copper. The wafer was removed and loaded back into the sputter to deposit the final Ti layer which was deposited to protect the copper from oxidizing.

The metal deposition was followed by photolithography process where AZ4330 positive photoresist (PR) was spin coated onto the wafer. This was followed by soft bake and exposure using Karl Suss contact aligner. The PR was developed using TMAH solution according to the thickness of the PR used. The exposure opened the areas on the Ti designed for electroplating. The exposed Ti was wet etched using a 2% HF solution. This was followed by Nickel and Gold electroplating (EP) for the under bump metallurgy. After EP the PR was stripped using a combination of re-expose and over develop followed by 3 minutes of oxygen plasma etch to remove any PR residue. This process was used as a standard method for PR stripping. The processed wafer was then cleaned using SRD and PR was applied to define the features of the
heater and temperature sensors for wet etch. The wet etch process was a series of steps used to first etch the exposed Ti, then Cu, and the final layer of Ti. Figure 63 shows a section of the heater die.

![Figure 63: Picture of the Heater chip showing the heater and temperature sensor on the heater chip](image)

### 7.2.2. Superconducting Carrier

The fabrication of the superconducting carrier was started by cleaning the (2 µm) oxidized silicon wafer followed by metal deposition using the XM-8 Sputterer. 500°A of Ti was deposited as the adhesion layer followed by 1500°A of Ta as the superconducting metal. This was followed by a 2 µm copper for under bump metallurgy which was followed by 500 A of Ti.
The second step was photolithography followed by electroplating of Ni and Au. After this the PR was stripped and the electroplated contact pads are protected and the exposed Ti and Cu are etched using wet etch process explained in Section 2.4.2. This was followed by patterning and reactive ion etch of Ta. The etch rate for Ta was determined to be 250Å/min. The exposed Ta was etched using the RIE using SF₆, which etched the Ta and the PR. Thus 8 µ thick PR (AZ4620) was used to ensure that the desired temperature sensor features are protected. After wafer clean the wafers were shipped to Louisiana Tech for the deposition of a 2 µ thick SiO₂ layer. Figure 64 shows the section of the SC carrier chip.

Figure 64: SC-carrier chip with temperature sensor for in-situ measurement of the carrier temperature

7.2.3. Silicon Substrate

The fabrication of the silicon substrate followed the exact process flow used for the fabrication of the heater die except for the use of DRIE process to create a blind trench for
mounting of the SC-MCM. The Bosh process used for thru-silicon-via etching was modified for creating the blind trench. Table 7.1 shows the summary of the process flow for the fabrication of the 2D SC-MCM devices and Figure 64 shows the process flow for the fabrication of the SC-carrier chip.

**Table 7.1: Process flow for the fabrication of 2D SC-MCM devices**

<table>
<thead>
<tr>
<th>Process Steps</th>
<th>Heater Chip</th>
<th>SC-Carrier Chip</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>PVD - Sputter</td>
<td>Ti/Cu/Ti</td>
<td>Ti/Ta/Cu/Ti</td>
<td>Ti/Cu/Ti</td>
</tr>
<tr>
<td>Photolithography</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Wet Etch</td>
<td>Ti</td>
<td>Ti</td>
<td>Ti</td>
</tr>
<tr>
<td>Electroplate</td>
<td>Ni/Au</td>
<td>Ni/Au</td>
<td>Ni/Au (2)</td>
</tr>
<tr>
<td>Photolithography</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Wet Etch</td>
<td>Ti/Cu/Ti</td>
<td>Ti/Cu</td>
<td>Ti/Cu/Ti</td>
</tr>
<tr>
<td>RIE</td>
<td>Ta/Ti</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Passivate</td>
<td>BCB</td>
<td>SiO₂ (PECVD)</td>
<td></td>
</tr>
<tr>
<td>DRIE</td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>
Figure 65: Process flow for the fabrication of SC-carrier chip
CHAPTER 8: PACKAGING AND TESTING OF 2D MCM CRYOPACKAGE

8.1. Introduction

The goal of the current chapter is to discuss the assembly, testing and results of the 2D SC-MCM cryopackage. Each of the above is discussed in detail below.

8.2. Assembly

The assembly of the 2D SC-MCM cryopackage consists of chip level interconnection, substrate level interconnection and 4 K to room temperature interface. For ease of explanation and logical flow the 4 K to room temperature interface is explained first.

The heat flow from room temperature electronics to the 4 K stage should be minimized. All input/output connections to the 4 K stage were made using 4-wire technique using 32 AWG phosphor bronze wire. The I/O wires were thermalized to the 1st stage with OFHC copper clamps. The wires were then brought to the 4 K stage and thermalized to the 4K stage to reduce any external heat load affecting the experiment.

The next level of interconnection was between I/O’s from room temperature electronics to the silicon substrate. 93/7 Pb-Sn solder was reflowed on a hot plate over the 1.2 mm x 1.2 mm gold contact pads fabricated on the silicon substrate. The phosphor bronze wires were held in place over the gold contact pads with the aid of Kapton tape and the silicon substrate was cooled to form the electrical connection between the wires and the silicon substrate.

The interconnection between the SC-carrier chip and the silicon substrate was the next level of interconnection. The electrical interconnection was completed by wire bonding. This required the SC-Carrier chip to be held in position during connection and testing as any movement could result in failure of the wire bond connections. The SWCNT cryogenic underfill was used as die attach between the SC-carrier and the silicon substrate and allowed to cure.
overnight at room temperature. After curing of the die attach the carrier and silicon substrate were placed on the Al-wedge bonder and connected by the 1 mil aluminum wire.

The final level interconnection was between the heater chip and the SC-carrier chip. This interconnection was completed by flip chip bonding of the heater die to the carrier substrate. The flip chip bonding required deposition of solder balls on the heater die. The In-Sn solder balls were deposited by solder dipping process explained in Section 2.4.2. The bump height was measured using the Dektak. Figure 66 shows the Dektak measurements of the bump height.

![Figure 66: Characterization of bump height using Dektak](image)

The heater die was flip chip bonded by reflowing the solder bumps for electrical connection and using capillary flow for underfill application. The underfill was applied until it flowed across the chip-carrier region and came out across the opposite sides. The electrical and thermal analysis was completed on the assembled cryopackage. Figure 67 shows the illustration of the 2D SC-MCM cryopackage architecture and Figure 68 is a picture of the fabricated and assembled 2D SC-MCM cryopackage.
Figure 67: 2D SC-MCM cryopackage architecture

Figure 68: 2D SC-MCM cryopackage
8.3. **Electrical Characterization of 2D SC-MCM Cryopackage**

The objective of the electrical characterization of the 2D SC-MCM cryopackage was to demonstrate that the fabricated 2D SC-MCM cryopackage underwent the transition from normal to superconducting state. The assembled cryopackage consisted of two heater die flip chip bonded using pure cryogenic underfill and two heater die flip chip bonded using 0.1 SWCNT underfill. The 2D SC-MCM cryopackage was then mounted onto the sample mount stage. A thin layer of Apiezon thermal grease was applied between the sample mount stage and the cryopackage to fill voids and reduce the interfacial resistance. The thermal shields and vacuum shroud were mounted on the test bed and the system was pumped down overnight to $9 \times 10^{-7}$ mTorr. The compressor was then started to cool the cryopackage to 4 K. The temperature of the carrier die and the heater die from room temperature to 4 K. The room temperature resistance of the carrier die varied from 10742.37 ohms to 11767.15 ohms at room temperature and decreased as a function of temperature. The 2D SC-MCM successfully showed the transition from normal state to superconducting state with all the resistors of the carrier chip made the transition to superconducting state between 3.6 K and 3.7 K. Figure 69 shows the plot of the resistance as a function of temperature.
8.4. Thermal Characterization of 2D SCMCM Cryopackage

The thermal performance of the 2D SC-MCM was studied by first determining the temperature of coefficient of resistance (TCR), as the TCR greatly varies depending on the deposited thin film [152-154]. Thus in order to determine the TCR for the sputtered tantalum the stage temperature was varied in increments of 0.05 K from 3.7 K to 4.5 K. Using the expression shown in equation 8.1 the TCR for the current sample was calculated. Similarly, the TCR for the sputtered copper was also calculated.

\[ R_f = R_i (1 + \alpha(T-f - T_i)) \]  

(8.1)
where \( R_f \) is the resistance at \( T_f \), \( R_i \) is the resistance at \( T_i \) and \( \alpha \) is the TCR of the material. The TCR used was the mean value obtained from the above calibration method. The TCR for the Ta varied from \( 1.55 \times 10^{-4} \, \text{K}^{-1} \) to \( 1.71 \times 10^{-4} \, \text{K}^{-1} \) and that for the deposited copper was \( 8.8 \times 10^{-5} \, \text{K}^{-1} \). Figure 70 and 71 show the temperature calibration of curves for Ta and Cu measured as a function of the temperature.

Figure 70: Temperature coefficient of resistance calibration curves for tantalum
The 2D SC-MCM was then cooled to 4 K and allowed to stay at 4 K for a period of 5 hours. The heater chip was then powered by varying the applied voltage from 0 V to 1 V and the resistance measured as a function of the applied voltage. Figure 72 is the plot of measured resistances of the carrier with pure epoxy underfill and SWCNT underfill as a function of the applied power. The calculated value for TCR was then used to determine the temperature delta between the chip and carrier to compare the thermal performance of the 2D SC-MCM cryopackage.
8.5. Results and discussion

The temperature difference calculated for the 2D SC-MCM indicated that as the applied power varied from 0 mW to 4.79 mW the 0.1wt% SWCNT underfill indicated a lower temperature delta than the pure epoxy underfill. At 4.79 mW of applied power the temperature delta between the chip and carrier chip for pure epoxy underfill was 3.37 K whereas that for the 0.1wt% SWCNT underfill bonded cryopackage was 1.27 K. Figure 73 shows the temperature delta plot for pure epoxy underfill and 0.1 wt% SWCNT loaded underfill.
When the experiment was repeated but with SWCNT loadings of 0.1wt%, 0.2wt%, 0.5wt% SWCNT loadings, heater die bonded using 0.2wt% and 0.5wt% SWCNT underfill failed to make contact with the carrier die. The higher loadings of SWCNT underfill coupled did not allow for good contact and this was attributed to the increase in viscosity of the underfill due to higher loading of SWCNT. There were several challenges encountered during the packaging and testing of 2D SC-MCM cryopackage.

First, in regard to the packaging of the 2D SC-MCM cryopackage the flip chip bonding process required the use of an underfill whose cure temperature was higher than that of the
current pure epoxy. During the flip chip bonding process several chips failed to make contact to the carrier due to the rapid cure and the use of a manual flip chip bonder. This challenge was overcome by placing the heater chip on the carrier chip and then reflowing the solder balls and then allowing the module to cool down to room temperature and applying the underfill via capillary flow. Though this process was effective for pure epoxy and 0.1wt% SWCNT underfill it did not work for higher loadings SWCNT underfill which did not flow between the chip and carrier.

Second, in regard to testing, while the silicon substrate allowed for the fabrication of multiple SC-MCMs on a single carrier substrate it was also very brittle and the thermal stresses induced during the DRIE process led to cracking of the substrate when cooled from room temperature to 4 K. Additionally, the cleanliness of the test bed, vacuum conditions and the thermal grease applied was critical in order to achieve good thermal contact between the test sample and the test bed. In conclusion, a 2D SC-MCM cryopackage using 0.1wt% SWCNT underfill and pure epoxy underfill was fabricated and the electrical and thermal performance of the cryopackage was demonstrated.
9. CHAPTER 9: SUMMARY AND FUTURE WORK

9.1. Conclusions:

The main focus of the current research work was to study the thermal performance of a RSFQ SCE-MCM cryopackage through modeling and experimentation and to show the thermal and electrical performance of SCE-MCMs in single chip MCM and 2D MCM architecture. The research is summarized below:

- Assembled and calibrated the cryogenic test bed for material and device characterization at 4 K.
- Identified that the temperature delta between a SCE-chip and SCE-carrier chip is significantly higher than the 50 mK threshold when flip chip bonded using thermo-compression bonding.
- Studied the flip chip bonding process for SCE-MCMs and demonstrated the reduction in temperature delta using pure cryogenic underfill.
- Optimized the purification process of SWCNTs and developed a method for integrating purified SWCNTs in the base cryogenic underfill.
- Demonstrated the thermal enhancement of cryogenic underfill due to SWCNT loading.
- Characterized the thermal, electrical and adhesion properties of SWCNT integrated underfill.
- Integrated the SWCNT underfill in an active RSFQ SCE-MCM and demonstrated the electrical and thermal performance of the single chip SCE-MCM.
- Designed, fabricated and packaged a 2D SC-MCM cryopackage using pure cryogenic underfill and 0.1% SWCNT loaded underfill.
- Demonstrated the electrical performance of the 2D SC-MCM cryopackage.
• Packaged 2D SC-MCM using pure cryogenic underfill and 0.1 wt% SWCNT underfill
• Demonstrated the thermal performance of the 2D SC-MCM.

As proven in this research SWCNT integration in underfill enhanced the thermal performance of SCE in both single chip and 2D MCMs. It is believed that this is the first SWCNT-underfill integrated SCE-MCM cryopackage.

9.2. Future Work

Although shown to be an effective process, several modifications of the current research can be made to enhance performance. For instance, the bump deposition process used for solder ball deposition can be replaced by sputter deposited or electroplated solder balls. The In-Sn solder balls can be replaced by either copper stud bumps or gold bumps. Copper or gold solder balls should enhance the thermal and electrical performance of the SCE-MCM cryopackage. It seems beneficial to orient the SWCNTs normal to the chip surface to take advantage of their exceptional thermal properties. As shown in the electrical characterization of RSFQ SCE-MCM cryopackage the internal on chip heat dissipation showed that there needs to be a modification in the arrangement of the resistive layer. It seems to be beneficial to place the resistive layer closer to the solder balls. Finally, SWCNTs need to be functionalized to go to higher loadings to take advantage of their thermal and electrical and mechanical properties.
References:


Appendix A: A Small World of Fun

Nanotechnology was a term given to things which are nanoscale \(10^{-9} \text{ m}\) in size. Nanoparticles are \(1/1000^{th}\) the size of a human hair. Nanotechnology has resulted in research and development of new material for various practical applications such as high strength composites and other.

At the University of Arkansas, PhD student Ranjith John is working with Dr. Ajay Malshe to use these materials in the packaging of advanced electronics. Mr. John noted “I first came in contact with nanotechnology when I moved to Arkansas for my PhD. I was introduced to this black soot which looked like dust. I remember the first time I started working with single walled carbon nanotubes (SWCNTs) and it looked like dust particles and then I placed them in a small beaker and agitated them in IPA and saw them dissociate and the colorless IPA solution took the black color of the SWCNTs, I was fascinated. That is when I realized I could take the SWCNTs and modify the properties of any system.” The challenge then was to examine the properties of cryogenic epoxy due to SWCNT loading for underfill applications. Underfill was an epoxy substance which was found in every iPAD, Laptop, cellphone, iPOD etc. Can you imagine doing something that goes inside a device like an iPAD?

Now think taking something that small and putting into another substance and using it for high speed communication systems which work at 4 K which was -452.2°F. Mr. John said “It was an interesting problem as SWCNTs are good electrical and thermal conductors, but I needed them to be a good thermal conductor but not a good electrical conductor.” The problem was approached strategically by first studying the material properties at 4 K and then creating a polymer material which takes unwanted heat away from devices. Under Dr. Malshe’s guidance the challenge was solved by creating a new method of integrating SWCNTs in epoxies without changing the electrical properties. Mr. John concluded that “The current work has allowed us to improve the heat transport between ICs at 4 K which forms the backbone for high speed communication systems.”
Appendix B: Executive Summary

The objectives of this research were three fold: (1) design and understand the fundamental behavior of single walled carbon nanotube (SWNT, 1D nanostructures) embedded polymer matrix at cryogenic temperature (4K); (2) fabricate and test thermal interfaces in cryogenic superconducting electronic (SCE) packages with and without the CNT based polymers. SCE packages will be in multichip module (MCM) system architecture.

SCE packages are used for high speed communications. The speed and related performance of these circuits depend on the operating temperature of the package and related interfaces in the package. One of the primary challenges in thermal management of SCE cryopackage was the low thermal conductivity of cryogenic underfill ($K_{th}$=0.02W/m$\cdot$K – 0.06W/m$\cdot$K), thermal resistance of the superconducting solder bumps and the thermal interfaces between SCE die and underfill. Thus the above objectives were critical to address the thermal management of SCE cryopackage, achieving miniaturization and reducing signal delays across thermal and physical boundaries to ensure a reliable cryo-MCM system.

In this research, the novel cryogenic underfill exploited the one-dimensional properties of SWNTs and its interaction with the supporting polymer matrix to realize an electrically insulating and thermal conducting underfill. Additionally, the thermal budget for superconducting MCM’s was very small ($\Delta T$~50mK, between SC die and substrate). Due to the thermal resistance due to underfill, solder bumps and interfaces between SC die and substrate there is potential for an undesirable thermal profile ($\Delta T$>50mK) across the SC-MCM cryopackage. Hence, this project was strategically planned to measure the thermal resistance due to unloaded epoxy, SWNT loaded epoxy, SC solder bumps and the thermal interface resistance between SC die and the underfill.
Finally, as the functionality of the SC circuits increases, the number of I/O’s is also expected to increase resulting in reduced bump size with increased power density. Thus the effects of bump size and power density was analyzed for flip chip bonded SC-MCM’s. The design, fabrication and testing of the SC-MCM cryopackage was completed using test heater dies fabricated using well established Hypres Design Rules. The novel features of this research were the use of thermally conducting and electrically insulating SWCNT integrated underfill for flip chip bonded superconducting electronic circuits and the packaging of superconducting electronics in a MCM architecture.

The newly created intellectual property in the current research is as follows

1. The processing of SWCNTs to form electrically non-conductive but thermally enhanced SWCNT epoxy.
2. The processing of electrically conductive SWCNT epoxy which can be used as die attach and printed bumps.
Appendix C: Potential patent, commercialization and societal impact

Potential Patent:

Item 1: Can be patented as it is a new way for creating SWCNT composites which are thermally conducting but electrically insulating.

Item 2: Can be patented as it is a new way for creating conductive polymer composite without the use of any functionalization agent.

Commercialization Potential:

Item 1: Even though the thermally conductive but electrically insulating cryogenic epoxy is worthwhile candidate for patent protection since the data was presented at the Electronics Components and Technology Conference in June of 2010 and at the Applied Superconductivity Conference 2010 it is cannot be protected by a patent.

Item 2: The conductive epoxy has large commercial value as it can be used as die attach which can allow for the separation of an IC from the substrate. But this still requires considerable work before it becomes a valuable commercial product. Additionally the electrically conductive SWCNT epoxy can be explored for the fabrication of bumps, thermoelectric devices for waste heat recovery, quenching of superconducting magnets and for coating of liquid hydrogen storage tanks.

Publications and Presentations


Pending Publications:

• Ranjith John, Muhammad Jahan, Ajay Malshe and Deepnarayan Gupta, “Experimental Study of Kapitza Contact Resistance between Cryogenic Underfill and Silicon Dioxide at 4 K”, Pending–Applied Physics Letters.

Appendix D: Broader Impact:

The electrically conductive epoxy can be used for thermoelectric devices thereby allowing the waste heat energy seen in automobiles and electronic equipment to be converted to useful electrical energy. Additionally, with a few modifications the SWCNT loaded epoxy can be used to enhance the light weight but high strength material for automobiles.
Appendix E: Software used for research:

Computer 1
Model and serial #: Gateway NV57H13u
Owner and Location: Ranjith John, personal laptop
Software 1: Windows XP, Purchased by Ranjith John
Software 2: MS Office, Purchased by Ranjith John

Computer 2
Model and Serial #: Dell T3400, 3TQKTH1
Owner and Location: Dr. Ajay Malshe, Nano Bldg. 202
Software 1: Windows XP, Purchased by MEEG
Software 2: MS Office, Purchased by MEEG
Software 3: Buehler Omnimet 9.0, Purchased by Dr. Ajay Malshe

Computer 3
Model and Serial #: Dell Optiplex, GX280
Owner and Location: Dr. Ajay Malshe, Nano Bldg. 202
Software 1: MS Office, Purchased by MEEG
Software 3: Adobe Acrobat, Purchased by MEEG
Software 4: AutoCAD 2010, Purchased by MEEG
Software 5: COMSOL, Purchased by Dr. Ajay Malshe
Software 6: Labview, Purchased by Dr. Ajay Malshe
Software 7: ImageJ, Openware

Equipment Used in Research:
GM Cryocooler - Model#: SHI-4-15, Serial#: 12226
Vacuum Pump - Varian Turbo –V 300 HT
Lakeshore 340 Temperature Controller
Appendix F: MS Project File
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<th>Start Date</th>
<th>End Date</th>
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<tbody>
<tr>
<td>Write EEE 482 paper</td>
<td>Oct 3, 2010</td>
<td>Dec 1, 2010</td>
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<tr>
<td>Determine the thermal resistance due to bumps</td>
<td>Dec 1, 2010</td>
<td>Mar 1, 2011</td>
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<td>Package Parameter Variations (Widt bumps, Power density)</td>
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<tr>
<td>Develop Theoretical Model</td>
<td>Nov 1, 2011</td>
<td>Jan 1, 2012</td>
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<td>Test Thermal Performance of DC Module with SiNWt underfill</td>
<td>Jan 1, 2012</td>
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<tr>
<td>Fabricate bumps and characterize</td>
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<td>Fabricate bumps on test wafer for thermal characterization</td>
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<td>Nov 1, 2013</td>
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<tr>
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<td>BICM Design</td>
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Appendix G: Plagirism Report from Turnitin