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Environmental Reliability of Thin Film Sealing on Thick Film LTCC

Environmental Reliability of Thin Film Sealing on Thick Film LTCC

A thesis submitted in partial fulfillment
Of the requirements for the degree of
Master of Science in Microelectronics-Photonics

By

Charles R. Bourland
University of Arkansas
Bachelor of Science in Electrical Engineering 2013

May 2015
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

Dr. H. Alan Mantooth
Thesis Director

Dr. Michael D. Glover
Committee Member

Dr. William F. Oliver III
Committee Member

Dr. Simon S. Ang
Committee Member

Dr. Rick Wise
Ex-Officio Member

The following signatories attest that all software used in this thesis was legally licensed for use by Charles R. Bourland for research purposes and publication.

Mr. Charles R. Bourland, Student	Dr. H. Alan Mantooth, Thesis Director

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Dr. Rick Wise, Program Director	Dr. H. Alan Mantooth, Thesis Director

Abstract

As electronic components and systems become more intricate and expand into new realms of use case scenarios, new materials systems must be explored. With new systems comes the balancing acts of cost and reliability. Presented here is a thesis that explores a new hybrid-electronics packaging system using low temperature co-fired ceramics, referred to as LTCC. An LTCC system was designed to explore the environmental reliability of numerous thick film LTCC features and parameters. A key element was to explore how a thin film metallization stack up used to cap or seal underlying thick film structures would decrease environmental susceptibility while at the same time optimizing costs. A material matrix of 16 recipes was developed with 14 primary feature types to be evaluated. It was decided that the LTCC systems undergo five environmental reliability tests which were as follows: lifetime at elevated temperature, thermal cycling, humidity, thermal shock, and corrosion via salt fog spay. All environmental reliability tests were performed in accordance to either MIL or JEDEC standards or specifications. An investigation of occurring phenomena through each environmental test is presented.

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Chapter 1 Introduction

1.1. Overview of Project

This thesis project presents work that was part of a larger collaborative effort between multiple universities (including the University of Arkansas, Kansas State University, and the University of Kansas), Sandia National Labs, and sponsored by the National Security Campus of Honeywell Federal Manufacturing and Technology at Kansas City, MO. The overall goal of the project was a long term oriented plan to further develop the general manufacturability of low temperature co-fired ceramics (LTCC) in microelectronics and to understand how the incorporation of thin film metallization with LTCC impacts long term reliability. Aspects of this development would be the design, materials, processes, packaging, embedded devices, and environmental reliability. The work presented here will focus on environmental reliability of LTCC substrates.

Reliability is a measure of the dependability of a product or device over its expected lifetime. Environmental reliability therefore is the dependability of a product in various or certain environments, which could be (but is not limited to) dry, humid, oceanic, corrosive, elevated radiation, vibrational shock, static or fluctuating temperatures, or any use case scenario using a combination thereof. Any device or product has an intended set of use case scenarios, and for each scenario there are various factors to consider when evaluating reliability. Critical missions in the defense and aerospace sectors look to reliability in designing for mission length and precision. Businesses and developers look to reliability metrics in determining the price point and warranty period of a product. This specific research does not deal with a final product, but rather a system that may potentially be deployed in numerous use case scenarios. Therefore, a

broad spectrum of reliability metrics are important in evaluating the LTCC technologies, processes, and methods discussed in this thesis.

Therefore, this thesis will focus on the environmental reliability testing of pre-designed LTCC parts. These parts, or coupons, were designed with a variety of different structures and features by others on the collaborative project team so as to maximize the quantity of reliability data that could be captured during environmental testing. This data, in turn, could later be utilized to derive design rules for upcoming components, devices, and packages using LTCC that maximize long-term reliability.

A unique aspect of this particular research is that of using evaporated or sputtered thin films, similar to those used in semiconductor manufacturing, in conjunction with the LTCC process. More specifically, the thin film was applied to cover or ‘seal’ the LTCC thick film on the top layer of the coupon. There are several reasons for applying the thin films in this manner. First, the films aid in the reliability of surface structures by ‘sealing’ them for protection. Second, the films can enhance certain electrical characteristics of the underlying thick film, such as increasing conductivity and minimizing RF loss tangents. Finally, to experiment with thin film deposition directly on LTCC substrates in terms of adhesion and performance [1].

The LTCC coupons were fabricated using a number of different materials, layer thicknesses, and metallization. The material system matrix included two LTCC substrate materials, two thick film conductor materials, and four thin film metallization stack-ups. In addition to the material system variations, there are 14 varieties of test structures included on each coupon, including vias of varying diameters, through thermal vias (i.e., vias that go completely through the coupon from top to bottom), triple tracks, a daisy chain via system, and wire bonding pads.

Five different environmental reliability tests were used to evaluate the test coupons. The five tests chosen were: lifetime at an elevated temperature, thermal cycling, humidity testing, thermal shock, and corrosion testing.

1.2. Objectives and Significance

There are a number of key objectives targeted by performing environmental reliability tests on such a variety of materials and features in low temperature co-fired ceramics. The first objective was to determine the feasibility of replacing gold (Au) thick film with silver (Ag) thick film. The second objective would be to characterize the thin film's behavior on ceramics. The third objective was to evaluate the performance of the four thin film stack ups. Another goal would be to evaluate the reliability of the entire LTCC process in extreme environments though the five planned reliability tests. Additionally, the sealing aspect of the thin film over the thick film was to be evaluated. Finally, a goal was to examine any specific phenomena throughout the material matrix after each test, including cross sections of applicable features.

Another significant impact of this research was to help make LTCCs more versatile and cost effective. This project's goal was to do that in two primary ways: first, by aiming to substitute silver in for gold conductors in the LTCC, which would both dramatically reduce the cost of fabrication and enhance many desirable electrical characteristics, especially in HF applications [2]; second, by experimenting with thin film sealing of the thick film as a protection measure from environmental effects, thus improving LTCCs reliability and increasing their use case scenarios. To summarize, the impacts of this research are the potential cost reduction in fabrication if Ag is proven to be as reliable as Au, potential improvement in the reliability of the LTCC substrates for use in harsh environments, and extended applications for HF electronics.

Chapter 2 Theoretical Background

Low temperature co-fired ceramics (LTCC) is a set of specialty ceramic materials designed to be used in the electronics industry. To fully appreciate what LTCC is and how it benefits the current and future needs of the industry, a bit of background into the history and development of ceramics and their introduction into the electronics industry is needed. The most basic question, then, is to ask what a ceramic material is. A ceramic material can be defined as "an inorganic nonmetallic material or article [which] may be polycrystals, glasses, or combinations thereof, or single crystals" [3]. While this definition is rather broad, it is necessary nonetheless. Ceramics are commonly found in bulk form as a powder, which is then sintered together at high temperature.

Much of human history has involved the use of some ceramic compound or another, from art and cutlery of the ancients to components in internal combustion engines and thermionic valves (a precursor to the transistor). One of the earliest ceramics used was that of simple clay. Fast forward to modern day and there are a plethora of options of ceramic materials to choose from, given the desired application. Table 1 has a listing of many of the more common modern day ceramic materials and an example of either their properties or possible uses.

Table 1. Common Modern Ceramic Materials

Ceramic Material	Properties	Possible Uses
Aluminum Oxide	Highly Electrically Insulating	Substrates and Spark Plugs
Barium Titanate	Ferroelectric	Capacitors
Boron Nitride	Isoelectronic to Carbon	Lubricant or Abrasive
Silicon Carbide	Tough and Semiconducting	Extreme Environment Electronics and Cutting Tools
Silicon Nitride	Coarse and Tough	Abrasive Powders
Titanium Carbide	Thermal Resistance	Space Re-entry Vehicles
Zinc Oxide	Piezoelectric	Solar Cells and Varistors
Zirconium Dioxide	High Ionic Conductivity	Fuel Cells and O_2 Sensors

2.1. History of Ceramic Materials in Electronics

Ceramic materials have been researched to be utilized in electronics for nigh on a century now [4]. Ceramics were first utilized in the electronics world as an insulation material for current carrying electrical wires in the mid to late 1800's. Moving into the 20th century, ceramics were further developed for smaller scale electrical insulation and spark plugs for automobiles. Development of ceramic materials played a critical role in the development of the first transistors, which led to the first mobile radios and wireless telecommunication devices. In the 1940's, novel ceramic compounds at the time were used to create capacitors that had a smaller physical footprint but could hold more charge, thus increasing energy density. During the 60s and 70s, aluminum oxide (alumina) allowed for the creation and expansion of high voltage insulation and versatile highly isolative substrates which enabled the proliferation of smaller high frequency (HF) and radio wave (RF) electronics. Alumina also started the path of using ceramics for their mechanical properties in electronics such as substrates and advanced electronic packaging applications. The favorable and durable mechanical characteristics of alumina is what brought high temperature co-fired ceramics (HTCC) to the electronics industry as a packaging solution, specifically for hermetic sealing, radiation hardened, and thermally extreme situations. The advantages of HTCC led to the development of other novel and more versatile ceramics to ease in the manufacturing process, from which low temperature co-fired ceramics (LTCCs) are now a part of. New advances in ceramics are continually enabling smaller, lighter, more dense, and versatile electronics and bringing them into new and diverse fields [5].

2.2. Low Temperature Co-Fired Ceramics (LTCC)

2.2.1. Manufacturing Process

Low temperature co-fired ceramics are fabricated through a rather lengthy series of steps. The steps are as show in Table 2 and accompanied by an illustration by Fig. 2.1. Following the summarized list and illustration will be a detailed overview of each process.

Table 2. LTCC Fabrication Steps

Step	Process
1	Tape Blanking
2	Via Punching
3	Cavity Creation
4	Via Filling
5	Feature Printing
6	Laminating
7	Co-Firing
8	Post-Processing

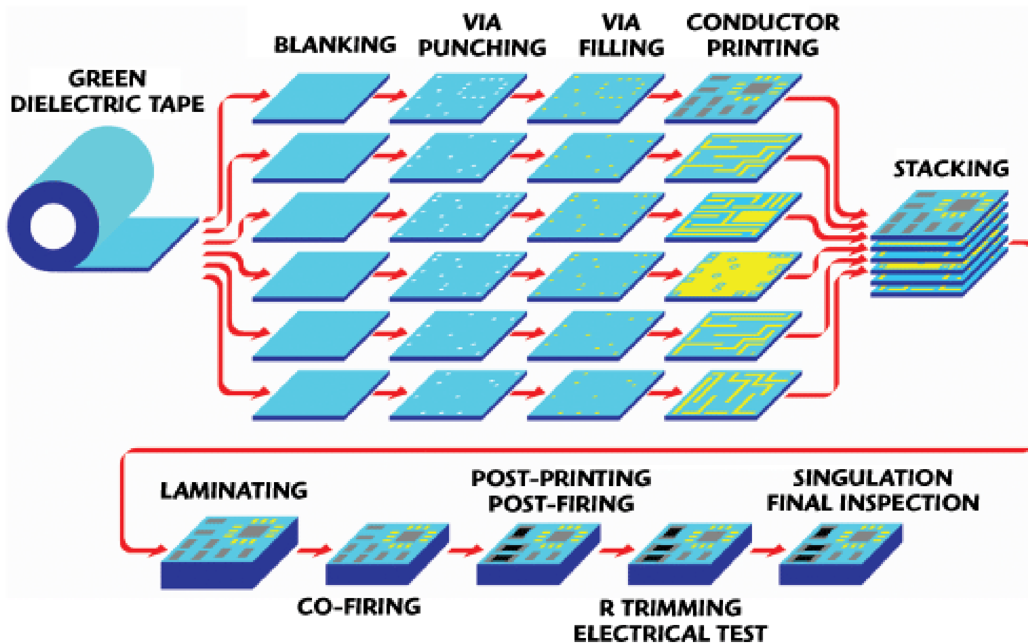

Fig. 2.1. Illustration of the LTCC manufacturing process [6].

Step 1, tape blanking, consists of cutting or punching out the correct size and shape the initial tape should be for one's specific application. This is typically performed through a roll-to-roll operation at the material manufacturer such as DuPont, Heraeus, or Kyocera to name a few of the major players currently providing LTCC materials. However, one could further blank the sheet if needed. Blanking can give square, rectangular, or even circular shapes of various sizes. This process would be considered somewhat analogous to that of semiconductor wafer production.

Step 2, via punching, is where holes of various sizes are quite literally punched though the tape. This operation is performed by a computer automated tool and is directed by 'artwork' that is programed into it. During this process, there are also special markers placed on all tapes for alignment purposes during future processing steps. When the tapes are layered together, holes that overlap form deeper and larger aspect ratio vias. The diameter of vias can vary usually from as small as 2 mils to 50 mils, however the difficulty increases when approaching either extreme. Vias that travel completely through all stacked tapes are typically referred to as thermal vias and usually aid in heat transfer.

Step 3, cavity creation, is the process by which a larger opening or hole is formed in the ceramic. A cavity is typically formed by punching many overlapping holes right together. This cavity could be used to house a discrete electronic device or to aid the design of multi-chip-modules (MCMs). They could also be part of the design of MEMS devices (micro-electro-mechanical-systems) or micro-fluidic channels to address thermal management issues.

Step 4, via filling, consists of using a screen printing apparatus to push a specially made (and often proprietary) conductive paste into the holes to make conductive vias. Conductive pastes vary by intended use case scenarios and manufacturer. These pastes can be made up of

different conductive materials, such as gold, silver, or copper, and are specially designed for via size in that their CTE (coefficient of thermal expansion) or relative volume is changed to accommodate those features.

Step 5, feature printing, is actually very similar to the previous step 4. A screen printing process is used in conjunction with a specialized conductive ink to lay down features. These features could be, but are not limited to, wire traces, embedded passive components (i.e. capacitors or resistors), HF structures, or bonding pads.

Step 6, laminating, could actually be broken into two smaller steps, first the stacking of all the individual layers and second the lamination under high pressure. During the stacking process, each tape is rotated by 90° from the previous layer, this rotation helps with making the shrinkage factor more uniform during the co-firing stage. The purpose of the lamination process is to form a single uniform substrate from the many layers of tape. Lamination is typically performed using the isostatic method, where the layered tapes are put into water at 70 °C and pressurized to 3000 PSI for a certain time period.

Step 7, co-firing, is the final process that turns the malleable and soft tape into its final stage of a hard ceramic material. The low temperature in LTCC comes in at this stage, and indicates a temperature at or around 850 °C. This is an important number as it indicates that more materials can be used in the conductive pastes due to the lower melting point. High temperature co-fired ceramic (HTCC) was the precursor to LTCC, where the high temperature implied upwards of 1200 °C.

Step 8, post processing, is the final step to finish off an LTCC device or component. This step is very broad and may or may not include any number of methods. A few of the more

prominent methods would be final forming wire traces, bonding pads, laser trimming of resistors for tighter tolerances, adding thin film features, or applying cover pads to vias. Many times, LTCC components are not just made one at a time, but rather one panel at a time with multiple duplicates or copies of the part fabricated on each panel, these individual copies are called coupons in this context. A post processing step in this case, if multiple coupons are involved, is dicing the panels into their respective components or coupons.

The eight-step manufacturing process is but a summary and abridged version of everything that there is to consider. Fig. 2.2 gives a cross-sectional view of what a finished LTCC device may look like. For a more complete guide to the materials, processes, and best practices in the fabrication of LTCC please refer to Yoshihiko Imanaka's book entitled *Multilayered Low Temperature Cofired Ceramics (LTCC) Technology* for a more complete overview of the technology and manufacturing process [7].

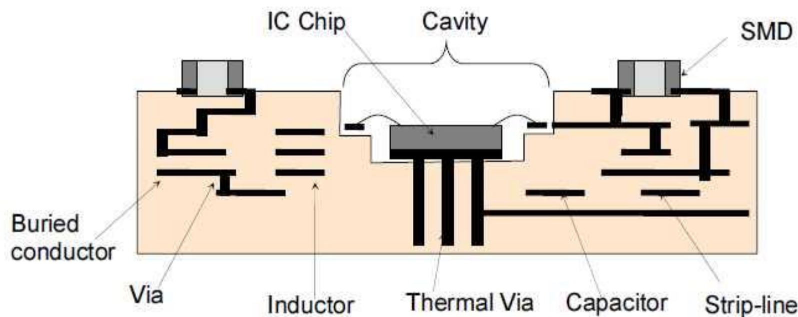

Fig. 2.2. Cross-sectional representation of a finished LTCC device with embedded passive components [8].

2.2.2. Advantages and Challenges of LTCC

Low temperature co-fired ceramics, like most things, have both certain advantages and disadvantages. Many of the pros in favor of LTCCs have nearly become necessities in the

electronics world, especially in the realm of extreme environment electronics. Therefore, the disadvantages that LTCCs face could instead be referred to as challenges to surmount and overcome rather than true cons. Even the existence of LTCCs are attributed to this outlook; extreme environments and high frequency applications necessitated a different set of conductive materials than were capable in the HTCC process, thus low temperature ceramic materials were developed.

There are many advantages to LTCC technologies. The physical volume and footprint is reduced from other traditional packaging technologies such as FR4 printed circuit boards. Along with reduced footprint comes reduced weight as well, this is of special interest to aerospace applications. The ability to have high layer counts in a single package enables designs previously unattainable; more than 80 layers have been successfully realized [9]. Electrical characteristics, such as the dielectric constant, thermal permittivity, and loss tangents are also more desirable than other packaging methods. The ability to embed multiple and various passive electronic components are a key factor to LTCCs popularity. Finally, reliability of LTCCs are favorable in many areas including but not limited to: mechanical stresses, high temperatures, humidity, and radiation.

LTCCs have several glaring challenges facing the maturing technology. The primary challenge of LTCC is that of becoming cost competitive at large scale [10]. There are a fewer number of suppliers for LTCC materials that other electronic and packaging materials, meaning tighter design parameters, longer lead times, and increased cost. Variation and a mediocre yield add to the challenges for high volume manufacturing. Finally, much of the research for LTCCs has been under individual companies and developed as intellectual property, rather than universities and published in the domain of academic journals [11].

2.3. Environmental Reliability

Reliability, as defined in section 1.1, is a measure of the dependability of a product over its expected lifetime. Therefore, environmental reliability is a component's dependability when exposed to one or more harsh environmental conditions during its lifetime. The reason why this is important is simply because each device will have a specialized environment that the part is meant to operate in, this is called a use case scenario. Components meant to be used in an engine bay compartment of a vehicle will face sustained mechanical vibrations and high temperatures. Components used in nautical and navy operations will face humid and corrosive environments for long periods of time. Parts for aerospace, space exploration, and satellites will face many forms of sustained radiation and large temperature swings. Anytime a new design, novel material, or a new use case scenario is explored reliability testing must be performed [12].

Reliability testing also helps designers and manufactures decide when and for how long to set warranties and manage statistical quality control [14]. In reliability theory, there is a graph known as the bath tub curve; this curve is shown in Fig. 2.3. In the short term there is an elevated chance for having an early failure caused by a defect, it is at this point where manufactures want to set their initial warranty periods. Following that shorter time is a much longer time referred to as the timespan of normal use, or steady state reliability. The final stage of the bathtub curve is from wear out failures, when the part has reached its end of life. At this point the item may still be functional, but the chances of catastrophic failure increase rapidly. Another use for the bath tub curve in addition to warranty information is that of mission duration. Take, for example, a space exploration mission where components need to last a minimum of 10 years.

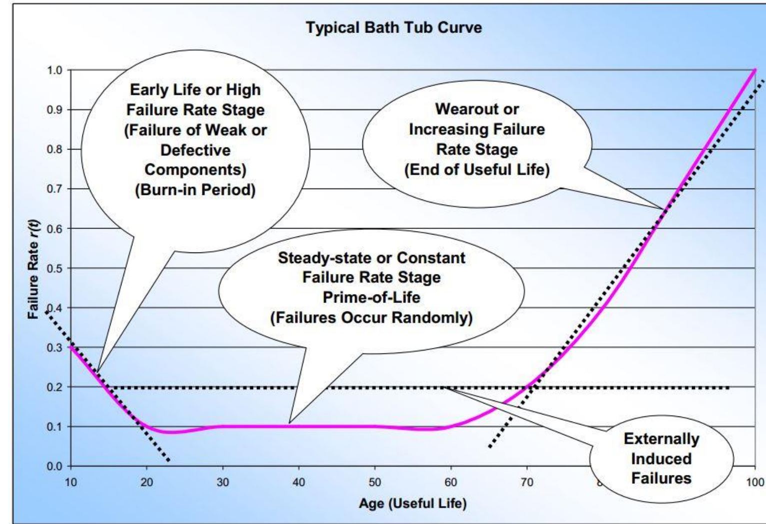

Fig. 2.3. Illustration of a typical reliability bath tub curve [13].

There are many different types of standardized testing that govern the specific environments, procedures, and experimental setups. Guidelines are set up through various literature sources, such as environmental-stress screening (ESS), accelerated life testing (ALT), highly accelerated life testing (HALT), highly accelerated stress testing (HAST), highly accelerated stress audit (HASA), and highly accelerated stress screening (HASS). More guidelines for specific testing apparatuses and acceptable experimental methods can be found in numerous military or industry wide specifications of standards. A few examples of these would be a MIL-STD for military standard or JEDEC SPEC for the a standard from the Joint Electron Device Engineering Council, a global organization devoted to developing open standards in the microelectronics world [15].

Chapter 3 Experimental Design

There were two main components to the experimental design, the physical LTCC coupon design and the material system matrix. A numbering system was put in place to track and inventory all coupons and their associated material systems.

3.1. LTCC Coupon Design

The LTCC coupons used in this project were designed by the Kansas City Plant of Honeywell Federal Manufacturing, with input from Sandia National Labs. The coupons were designed to maximize the amount of information about the process and reliability which could be extracted. Each sample, or 'coupon', included 14 different types of features, which tested parameters such the size of vias, pad-to-via spacing, trace pitch, and reliability of thermal through-vias. Fig. 3.1 shows the design of the LTCC coupon. Fig. 3.2 shows the specific 14 feature groups, and is accompanied by Table 3 for details.

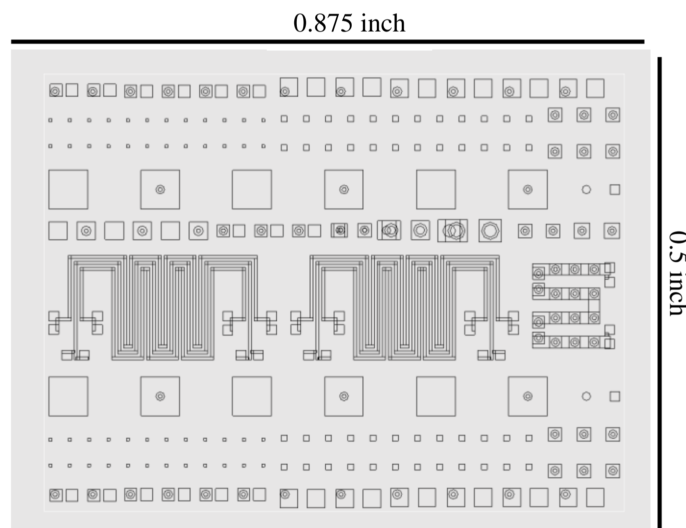

Fig. 3.1. Artwork for the LTCC Coupon 1 design.

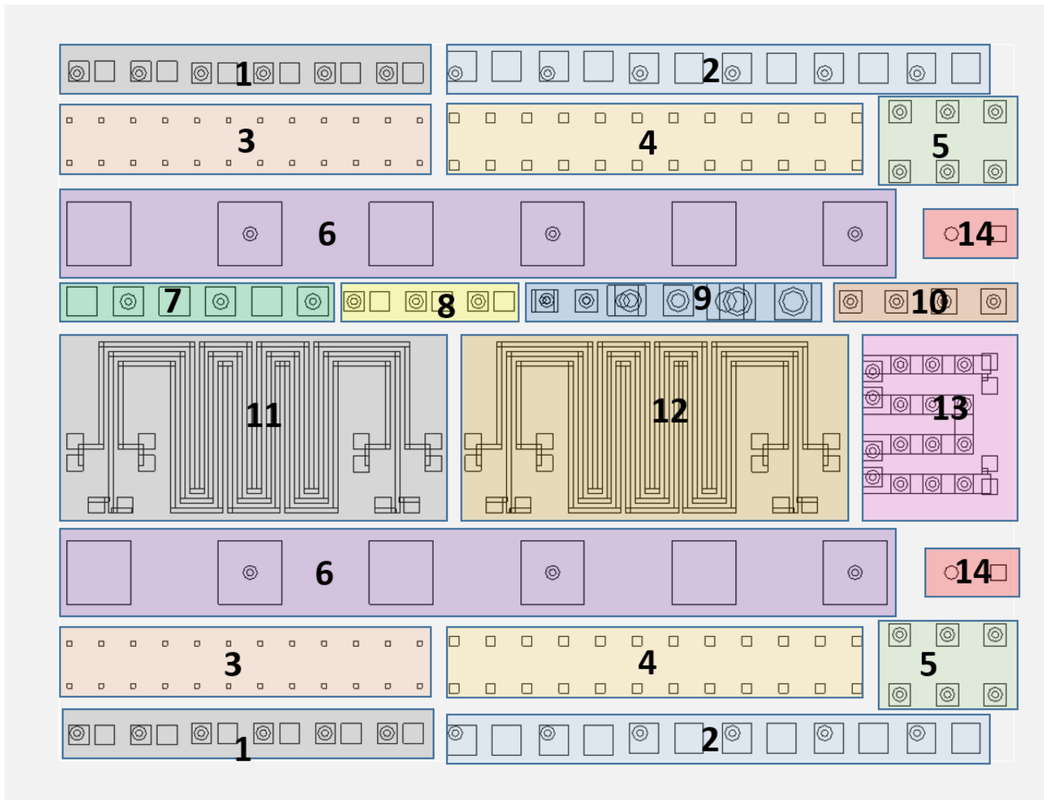

Fig. 3.2. The 14 feature groups on the LTCC Coupon 1 design.

Table 3. Feature Descriptions by Group Number

Feature #	Feature Description
1	0402 SMD area with 15 mil. Vias, 1 and 3 mil safety spacing
2	0603 SMD area with 15 mil. Vias, 1 and 3 mil safety spacing
3	6 mil. by 6 mil. pads, Thin Film only
4	12 mil. by 12 mil. pads, Thin Film only
5	Comparison Pads with 15 mil. Vias
6	Stud Pull Test Pads, with and without vias
7	0603 SMD area with 15 mil. Vias, and Vias Centered
8	0402 SMD area with 15 mil. Vias, and Vias Centered
9	Thermal Vias, 10, 20, and 30 mil, one slug & one shifted each
10	Comparison Pads, with 5 mil. and 7 mil. safety spacing
11	Triple Track, Thin Film Only, Direct on Ceramic
12	Triple Track, Thin Film ON TOP OF Thick Film
13	Daisy Chain with 0603 SMD bridge
14	Thick Film Baseline Elements

The coupons were designed to optimize usage of a single LTCC panel by including multiple copies of the coupon on each LTCC panel. An illustration of a panel is shown in Fig. 3.3. Note that there are nine Coupon 1's and two Coupon 2's; Coupon 2 was reserved for high frequency and microwave applications and were tested elsewhere, thus no testing or analysis was performed on them at the University of Arkansas (UA). The center of the panel was left clear for thin film process monitoring and alignment. Also of note are the circles or holes located in the corners of the panel, these are process alignment marks used during the LTCC tape stacking process.

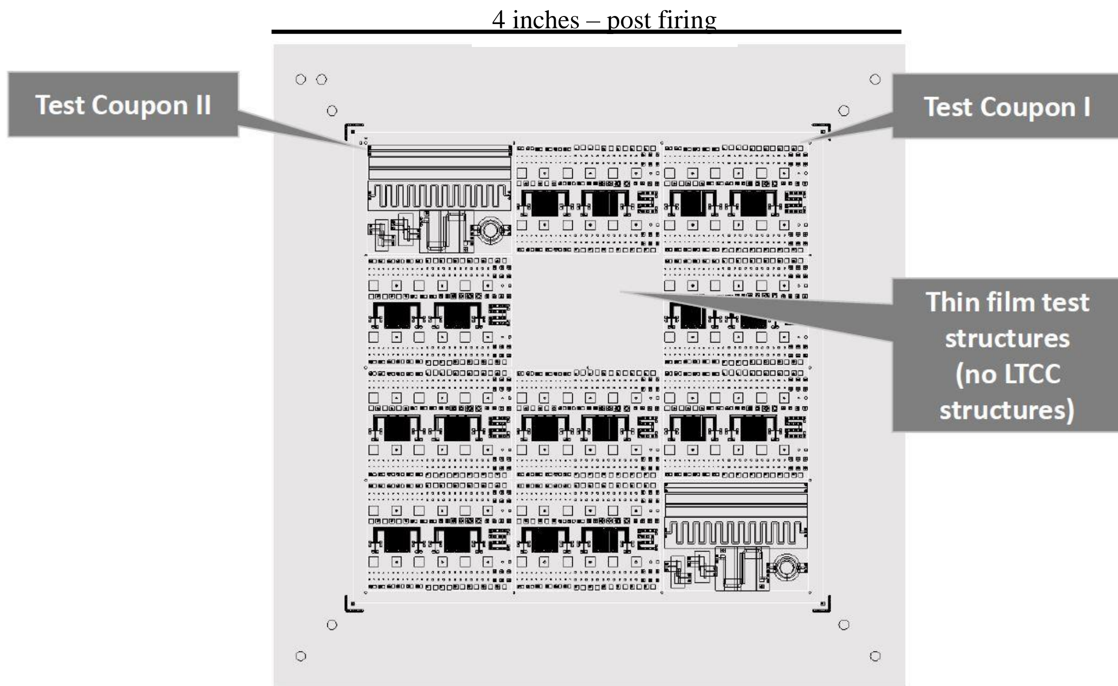

Fig. 3.3. Artwork of the LTCC panel with multiple copies of coupons

A total of 16 panels were delivered to the UA for testing and diced into individual coupons. A K&S 984-10 dicing saw was used with a serrated blade of 20 mil thickness running

at 1,200 RPM. Fig. 3.4 shows an LTCC panel diced into its respective coupons. The dark blue on the backside was the adhesive tape used in the dicing tool.

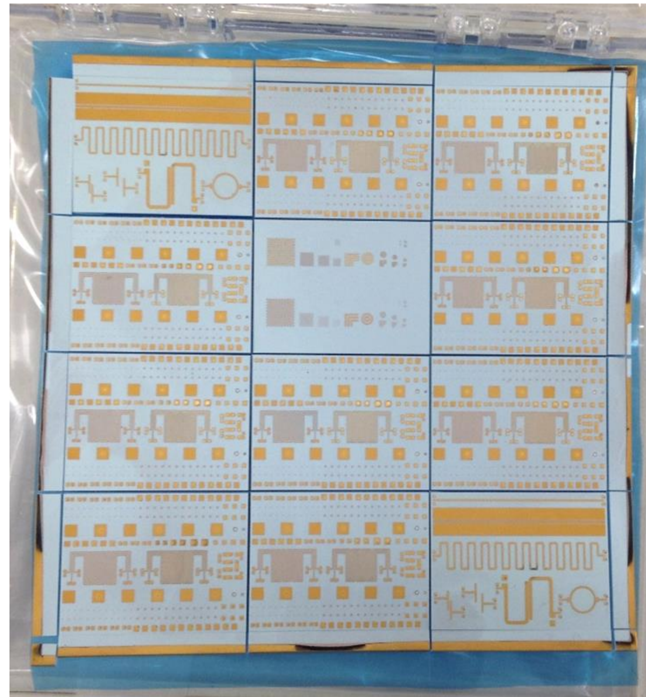

Fig. 3.4. An LTCC panel diced into individual coupons.

3.2. Material System Matrix

The materials used for a low temperature co-fired ceramic (LTCC) substrate design require special consideration depending upon the application. Generally, there are three key material concerns. The first concern is the substrate or ceramic material itself. Parameters such as thermal conductivity, electrical conductivity, hardness, thickness, and surface roughness are considered when selecting the ceramic substrate material. The next concern is that of the choice of via fill conductor paste material. Parameters such as coefficient of thermal expansion (CTE),

electrical properties, and cost are prime considerations. Finally, the choice of thick film conductor paste used for both internal and external conductors must be considered. Electrical characteristics are of particular importance, although cost, CTE, and mechanical attributes are also given consideration. This particular project includes a fourth key area for material selection, which was that of the thin films used on the top layer surface. A four-layer thin film build up was chosen by the Sponsor of the research to provide the desired data on reliability. Mechanical properties, electrical characteristics, and environmental stability were parameters considered when choosing these thin film materials and layer thicknesses.

A summary of the material systems chosen for the project is given in two tables: Table 4 describes the thick film materials system and Table ***5*** describes the thin film recipes. As can be seen in the tables, two ceramic substrate materials were chosen (DuPont 951 and the 9K7) as tape materials. The 951 was chosen for having a proven track record in production, mechanical robustness, and for being a material in which previous design experience was well established. The 9K7 material was chosen for its enhanced electrical characteristics at high frequencies. The two conductor materials chosen for via fill and conductors were gold and silver. Gold was chosen as a baseline, as it is used widely in the LTCC designs for its reliability and for its chemical inertness. Silver was chosen due to its lower cost and lower resistivity. Silver tends to oxidize readily, and the concept of using a thin film "cap" to seal it is one mitigation approach.

Table 4. Material System Matrix, 16 Total Combinations

LTCC Substrate	Thick Film & Via Fill	Thin Film Metallization Stack Up
DuPont 951	Silver (Ag)	Four Systems – *Refer to* Table 5
DuPont 9K7	Gold (Au)	

Table 5. Thin Film Metallization Stack Up

Recipe	A	B	C	D
Material Stack	Ti - Cu - Pt - Au	Cu - Pt - Au	Ti - Ag - Pt - Au	Ti - Cu - Pt - Au
Thickness (μm)	0.2 - 4 – 2- 0.375	4 - 2 - 0.375	0.2 - 4 - 2 - 0.375	0.2 – 2 - 2 - 0.375

Four distinct thin film ‘recipes’ were used in the project. These recipes are described in Table 5. Recipe A, which had a metallization stack up of 0.2 μm Ti, 4.0 μm Cu, 2.0 μm Pt, and 0.375 μm Au, was used as a baseline comparison recipe to the other three. One element of the thin film recipe was varied between recipes B, C, and D. In Recipe B the presence of the Ti layer, which was chosen to promote adhesion between the other thin films and the ceramic substrate, was omitted. In Recipe C, the 4.0 μm layer of Cu was exchange for a 4.0 μm layer of Ag. In Recipe D, the 4.0 μm layer of Cu was reduced to a 2.0 μm layer of Cu. A sketch up of Recipe A can be found in Fig. 3.5; the cover pad illustrated is a thick film element used to mitigate any height differential between a via and the LTCC substrate.

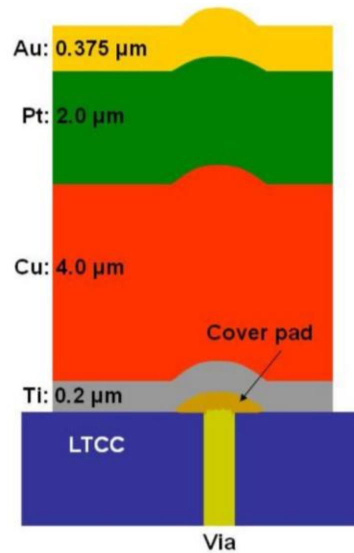

Fig. 3.5. A sketch of the thin film metallization stack up, Recipe A, over a via [1].

3.3. Coupon Inventory System and Naming Convention

A total of over 80 LTCC panels with thick films were fabricated at the UA High Density Electronics Center (HiDEC) for the UA's contribution to this project. These panels were sent to the Sponsor facility for thin film deposition of the various thin film recipes using physical vapor deposition (PVD). The UA was sent back 16 LTCC panels complete with thin film for this particular project, one for each of the material systems mentioned in section 3.2. Each panel contained multiple coupons per panel. Specifically every panel contained nine Coupon 1 designs, two Coupon 2 designs (which were not to be tested during this particular project at the U of A), and a single thin film process monitoring coupon. Every coupon on each panel was fabricated using a recipe from the material system matrix discussed in section 3.2. This yielded a total of nine Coupon 1s in each material system for environmental reliability testing.

Table 6. LTCC Panel Numbering and Inventory System

LTCC & Thick Film Material System		**Thin Film Build Up**				
		Recipe	A	B	C	D
		Thin Film	Ti - Cu - Pt - Au	Cu - Pt - Au	Ti - Ag - Pt - Au	Ti - Cu - Pt - Au
		Thick, µm	0.2 - 4 – 2- 0.375	4 - 2 - 0.375	0.2 - 4 - 2 - 0.375	0.2 - 2 - 2- 0.375
		Ref. #'s	27 & 17	28 & 18	29 & 19	30 & 20
951 Ag	1	**Panel #**	127	128	129	130
9K7 Ag	2		227	228	229	230
9K7 Au	3		317	318	319	320
951 Au	4		417	418	419	420

Chapter 4 Experimental Setup and Procedures

The project was divided into five reliability tests: lifetime at elevated temperature, thermal cycling, humidity, thermal shock, and corrosion. Each of these tests is discussed in detail in the following section. The coupons were divided into groups for reliability testing using the assignment process described further in section 4.2. An overview of the equipment used for data capture and inspection is given in section 4.3.

4.1. The Five Environmental Reliability Tests

All tests were performed in accordance with the military standard (MIL-STD) appropriate for each test; MIL-STD documents used will be referenced where applicable. The primary MIL-STD used was 202G. This MIL-STD contains many methods, one for each of the reliability tests described. A summary of each method used from the MIL-STD is listed in Table 7.

Table 7. Test Methods used from MIL-STD 202G

Method from MIL-STD 202G	Reliability Test
Method 108A	Lifetime at Elevated Ambient Temperature
Method 102A	Thermal Cycling
Method 103B	Humidity Testing
Method 107G	Thermal Shock
Method 101E	Corrosion (Salt Fog Spray)

4.1.1. Lifetime Test at Elevated Temperature

Method 108A in MIL-STD 202G outlines ‘Life (at Elevated Temperature).’ The test was performed in an enclosed oven over a range of temperatures and time periods. Temperatures in the document range from 70 °C to 500 °C. The temperature for the test was chosen based on the anticipated nominal operating environment and the degree of acceleration desired for the test.

The duration of the test can range from 96 hours to 5,000 hours, depending upon the anticipated lifetime of the component in the field. A test of 100 days, or 2,400 hours, at 170 °C was chosen by the Sponsor for the LTCC coupons based on the Sponsor's knowledge of the environmental conditions and specific application.

The lifetime test is meant to stress both electrical and mechanical aspects of components simultaneously. Holding components for long periods of time at an elevated temperature is akin to baking, and essentially accomplishes the same thing. When something is baked for extended time periods, it undergoes chemical and physical changes. For non-organic substances, those changes occur more slowly than their organic counterparts, but the changes are not negligible. At higher sustained temperatures, the materials are closer to their melting or reflow temperatures. Higher temperatures also encourage chemical changes such as oxidation of metals, outgassing of ceramic or plastic materials, and diffusion between materials, thus forming intermetallic compounds or resulting in migration into the substrate material.

4.1.2. Thermal Cycling

Method 102A in MIL-STD 202G describes 'Temperature Cycling,' though it is also referred to as thermal cycling in other literature. This particular method was cancelled in the newest revision of the 202G standard, recommending that method 107G (thermal shock) be used instead. However, the Sponsor believed that it would provide useful data for this project that could be compared to previous test trials, so it was used. Thermal cycling involves ramping the components in an oven up to a high temperature (above room temperature, usually greater than 50 °C) and then decreasing the temperature to a low temperature (room temperature or lower, usually below 0 °C). From high to low and back to room temperature is one cycle. Some examples of this cycling effect in nature are that of the day time night time cycle or the

temperature excursions seen by a satellite that is in orbit. The number of cycles used in the test depends on how extreme the test is designed to be. The number of cycles typically ranges from 50 to 2,500 cycles. Based on Sponsor input, a test of 1,000 cycles from +165 °C to -55 °C was chosen for the LTCC coupons. The method utilized to cool the artificial environment below room temperature was liquid nitrogen.

The action of swinging from high to low temperatures repeatedly causes mechanical stresses on all materials involved, which in turn affects electrical characteristics. As a material becomes hotter its molecules expand due to the increased atomic vibration at elevated temperatures. As a material decreases in temperature its molecules contract due to the slower atomic vibration as the material cools. The material expands and contracts with each temperature cycle, thus causing strain on the atomic lattices and between material layers. Every material has a specific coefficient of thermal expansion (CTE), which is the rate at which the material expands or contracts as it is heated or cooled. When there is a difference in CTE between materials that are joined together, there is a greater strain put onto the interface of the materials as the temperature of the materials is changed. The repetitive nature of temperature cycling induces cyclical stresses at material interfaces, which can lead to both micro and macro scale defects including cracking, divots, increased brittleness, decreased mechanical strength, and material migration.

4.1.3. Humidity Testing

Method 103B of the MIL-STD 202G has the name, Humidity '(Steady State).' The JEDEC SPEC JESD22-A101B was also referenced. This test is often referred to as the "85/85" test, so called because the temperature and relative humidity (RH) levels used during the test are 85 °C and 85%, respectively. The MIL-STD states that the test duration can range from 96 hours

to 1,344 hours. The specification also gives the option of having the parts or components to be tested under an electrical bias, if it is warranted. Through discussions with the Sponsor, a test of 240 hours (10 days) was chosen, with only select parts under a DC bias of 1 V.

The humidity test was performed in a sealed autoclave and acted as an accelerated test for environments with either normal or high humidity. The combination of elevated temperature and high relative humidity is analogous to conditions found in a tropical environment. Some of the possible failure mechanisms to look for during the 85/85 test would be swelling of materials due to absorbed moisture, decreased mechanical strength, and corrosion. Another effect would be material migration, especially true of silver when under a DC bias. Silver under a DC bias, exacerbated by elevated temperature and humidity, tends to form spikes or fractal patterns away from its source referred to as dendrites [16]. These dendrites can lead to increased parasitic resistance and capacitance in a signal path, causing issues in HF applications and potentially leading to shorting with adjacent conductors.

4.1.4. Thermal Shock

Method 107G in MIL-STD 202G has the name, ‘Thermal Shock.’ As the name implies, this test consists of exposing the components to a high temperature then very quickly exposing them to a very cold temperature, literally ‘shocking’ the components from one temperature extreme to the other. This test may be carried out using either an environmental chamber or a liquid bath. The range of temperatures in which the test may be performed are in the range from -65 °C to 500 °C. It is stated that a maximum time of one minute is allowed during the transfer from one extreme to the other. The number of cycles from hot to cold are from 5 up to 100. The parameters chosen for this LTCC research were 25 cycles in a liquid bath environment from -65

°C to +125 °C with a transfer time of 50 seconds each way and a dwell time of 10 minutes in each extreme. Galden fluid was the liquid medium for both extremes.

Though similar in procedures to temperature cycling, thermal shock is more extreme. Thermal shock mandates that there be a maximum of one minute transfer time from one extreme to the other, whereas temperature cycling does not have a specified ramp rate, except where interconnects are concerned and a ramp rate of 15 °C or less per minute is recommended. Common effects of thermal shock are very similar in nature to temperature cycling, however more extreme cases may be seen. Delamination or other mechanical displacement may also be prominent.

4.1.5. Corrosion Testing

Method 101E in MIL-STD 202G is given the name, 'Salt Atmosphere (Corrosion).' The ASTM 117B standard was utilized as a supporting document for more specific test procedures and for testing apparatus setup. This test consists of putting components into a sealed chamber with a temperature of 35 °C and a salt fog or salt spray. The fog is formed by a 5% NaCl solution being sprayed at a given rate through an atomizing nozzle. The duration is specified to be a minimum of 24 hours to a maximum of 240 hours. A test length of 240 hours (10 days) was chosen for this research project of LTCC parts.

A salt atmosphere is indicative of an oceanic or marine atmosphere. The slightly elevated temperature of 35 °C, roughly a warm summer's day, accelerates the corrosive environment. A variety of metals used in electronics, such as gold, copper, tungsten, platinum, aluminum, tin, palladium, chromium, and silver, are all commonly used in both integrated circuits and electronic packaging. Many of these materials are susceptible to corrosion. One of the key research goals of

this project was to evaluate if 'sealing' the thick film metallization, specifically Ag, with a thin film metallization would help protect the underlying thick film from corrosive effects.

4.1.6. Summary of Test Parameters

In summary, there were five environmental reliability tests planned primarily using MIL-STD 202G as the guiding authority. An overview of each of the tests and what could be altered or decided oneself was discussed above. A brief discussion of the particular failure modes and why the test was chosen was discussed in the previous sections. Table 8 summarizes the parameters for each test.

Table 8. Summary of Environmental Testing Parameters

Test #	Test Name	Test Parameters
1	Lifetime at Elevated Temperature	100 days at 170 °C
2	Thermal Cycling	1,000 cycles, from -55 °C to +165 °C
3	Humidity	10 days (240 hours) at 85 °C and 85% RH
4	Thermal Shock	25 cycles from -55 °C to +125 °C
5	Corrosion (Salt Fog)	10 days (240 hours) at 35 °C in 5% NaCl fog

4.2. Coupon Selection

4.2.1 First Round Selection

In the first run of samples, there was a miscommunication with the Sponsor in terms of how the material system matrix was constructed. Because of this discrepancy the coupon selection is described in two sections: the first round of experiments ran prior to this knowledge and the second round of experiments that was run after the issue had been recognized and corrected. Due to this issue in the first round, not every thin film recipe was tested in each of the five reliability tests. Final results are derived from a combination of results from the second

round (in which test coupon selection was better informed) and results from the first run that were applicable.

The UA originally planned for experiments having 36 Coupon 1s for each of the four thick film material systems. A minimum of three coupons per each of the four types were selected for each of the five tests, totaling 12 coupons per test. Table 9 shows the final selection of parts that were tested during the first round in each of the five tests, along with what was later to be found out as their respective thin film recipe type.

Table 9. Test Coupons Selected for First Run

Environmental Test	Panels	Thin Film Recipe Type
Lifetime	27, 17, 28, 18	A & B
Thermal Cycle	17, 27, 18, 28	A & B
Humidity	27, 19, 28,	A & C
Thermal Shock	30, 29, 19, 28, 17	A, B, C, & D
Corrosion	27, 18, 29, 19, 17	A, B, & C

4.2.2 Second Run Selection

As seen in Table 9 and mentioned previously, the testing of each thin film recipe type was incomplete and thus additional testing was required. After a meeting between UA and the Sponsor, a more robust design of experiments was formed that would yield the most complete data set after combining results from the first run. Table 10 shows the total number of coupons from each category that was left to distribute to new tests. Two tests were chosen for the additional run based on the desire of the Sponsor to compare results with similar tests run at other collaborator facilities. These two tests were thermal cycling (300 cycles) and humidity testing (3 days). Table 11 and Table 12 show which coupons were selected for each of the two

tests chosen. There were additional coupons that were held in reserve for additional testing depending upon initial results; these coupons are listed in Table 13.

Table 10. Total Coupons Available for Second Run

Thin Film Recipe Type	Thick Film Material System			
	951 Au	951 Ag	9K7 Au	9K7 Ag
A	5	3	2	1
B	3	3	2	3
C	3	4	7	7
D	9	2	0	6

Table 11. Thermal Cycling (300 cycles) - Second Run Coupon Assignment

Thin Film Recipe Type	Thick Film Material System			
	951 Au	951 Ag	9K7 Au	9K7 Ag
A	2	2	0	1
B	3	3	2	3
C	2	2	2	2
D	2	0	0	2

Table 12. Humidity (3 days) - Second Run Coupon Assignment

Thin Film Recipe Type	Thick Film Material System			
	951 Au	951 Ag	9K7 Au	9K7 Ag
A	2	1	2	0
B	0	0	0	0
C	1	2	2	2
D	2	0	0	2

Table 13. Conditional Holdbacks for Additional Testing Pending Results from Second Run

Thin Film Recipe Type	Thick Film Material System			
	951 Au	951 Ag	9K7 Au	9K7 Ag
A	1	0	0	0
B	0	0	0	0
C	0	0	3	3
D	5	2	0	2

It was found after the second run that one more additional test could be run. Due to the significant degradation of samples during the second run, it was decided that thermal cycling for 50 cycles should be performed to try to better pinpoint when the onset of corrosion and other issues occurred. The coupons used are the same as those listed in Table 13.

4.3. Analysis Equipment and Methods

There were many types of analysis methods utilized to examine the LTCC coupons after they were tested. Table 14 summarizes the methods chosen and the reasons why. Two of the more advanced methods need additional explanation, scanning electron microscopy (SEM) and energy dispersive x-ray (EDX), and are discussed in Sections 4.3.4 and 4.3.5, respectively. The processes used to cross-section samples are discussed in section 4.3.2.

Table 14. Summary of Analysis Methods Utilized

Analysis Method	Reason Chosen
Visual Inspection	Direction of where to go next, quick and simple
Optical Microscopy & Number System	Picture of what happens in the meso to micro scales and gives a direction of where to go next
Scanning Electron Microscopy (SEM)	Detailed picture of what was happing at the surface and for cross sections, giving better depth of field than optical microscopy
Energy Dispersive X-Ray (EDX)	Elemental analysis gives an idea of what happens chemically, checks for intermetallic compounds or oxidation, especially useful for cross sections

4.3.1. Visual Inspection

The visual inspection of the LTCC coupons was simple and straightforward. Each coupon that was tested in the particular test was fully examined visually with human eyes. Any physical phenomena was noted. Examples of what was looked for in this step were: delamination of thin or thick films, physical damage to the edges, surfaces, or film materials, and changes in

color of ceramic or film materials. These changes gave a preliminary indication of how to further proceed with the analysis.

4.3.2. Cross Sectioning

Cross sectioning is the act of cutting a sample through certain features in order to see more than just the surface but to see what is going on in the middle of a sample or coupon. This method was especially useful in examining metal vias and interconnects in this particular research. Fig. 4.1 illustrates the difference between a surface view and a cross section.

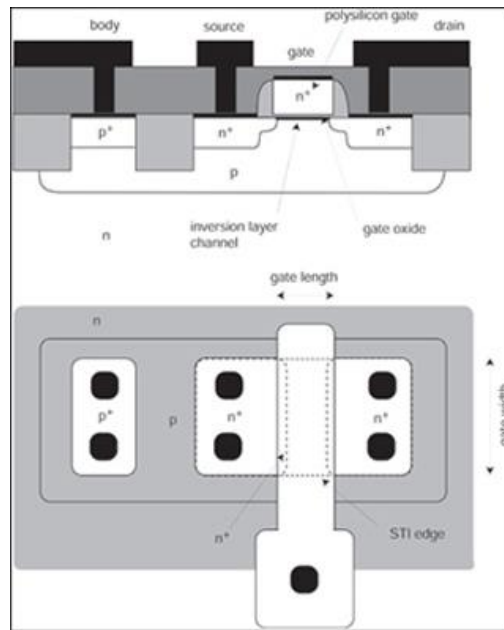

Fig. 4.1. Example of a cross section. On the top is shown a cross section. On the bottom is shown a surface view [17].

Cross sectioning is truly an art that takes much practice to perfect. The following is a description of the methods and practices that were used to cut and polish the LTCC coupons for this project. Each coupon that was cross sectioned was first encased in a cylindrical shaped epoxy resin. Once cured and hardened, the sample was set into a low speed saw where the cross

section line was measured out and aligned then cut. The cut piece was then cleaned and inspected under an optical microscope to ensure proper alignment of the features to be examined.

After cutting came the grinding and polishing process, sometimes referred to as chemical mechanical polishing (CMP). For these LTCC pieces, a manual grinding and polishing method was used. Grinding and polishing must happen sequentially in a number of different steps, where grinding is considered to use low grit abrasive material (e.g. 100-800 grit) and polishing is considered to use a high grit abrasive material (e.g. 1000+ grit). Each step did not have a set amount of time, but rather was checked periodically under optical microscopy for improvement, when the number of lines and scratches on the sample no longer diminished between checks was when the sample was ready for the next step. The process that was developed for these LTCC coupons had six steps. Those steps are summarized in Table 15.

Table 15. Summary of Grinding and Polishing Steps for Cross Sections

Step Number	Details
1	200 Grit Silicon Carbide (SiC) Abrasive
2	320 Grit SiC Abrasive Pad
3	600 Grit SiC Abrasive Pad
4	800 Grit SiC Abrasive Pad
5	1200 Grit SiC Abrasive Pad
6	1μm Alumina Powder on Cloth Pad

4.3.3. Optical Microscopy and Numbering System

The LTCC coupons presented in this research were examined under optical microscopy as a primary method of observation. The microscope used was a Zeiss AXIO which was capable of 5x, 10x, 20x, 50x, and 100x magnification. The second stage, 10x magnification, was used primarily and most often as this was the lowest magnification at which the largest feature would be fully visible and it gave a sufficient view for most phenomena that occurred. High

magnification was utilized for phenomena that were smaller and could not be sufficiently resolved at the standard 10x or when something was of particular interest.

A numbering system was constructed to rate each individual feature on each coupon that was tested; 220 features in all per coupon. This system was designed to assess the severity of any damage caused from the reliability tests by assigning a single number to each feature. There were five numbers chose in all, with a one being pristine and undamaged by the test to a five being the most devastating level of damage to that feature. Table 16 provides a detailed description of each layer and how the feature was assessed. After all of this data was gathered it was decided that a pass fail system was needed to simplify or add to the results. A line was drawn between a damage level of two and a damage level of three, meaning ones and twos passed the reliability tests, whereas threes through fives failed. This is also shown in Table 16. It is important to note that the primary source of error in this system was human error in recognizing the difference between a two and a three rating on each of the particular features. These numbers were compiled by the 14 major feature groups and other design criteria (see section 3.1. LTCC Coupon Design) to gain a better idea of what happened per each design decision.

Table 16. Five Levels of Damage for Assessing Coupons after Completion of Tests

Pass/Fail	Level	Description
Pass	1	No noticeable change observed, pristine
	2	Little change observed, functionality not affected (divots, discoloration, minor migration)
Fail	3	Moderate change, performance degraded (critical divots, corner damage, major migration)
	4	Heavy changes observed, functionality impaired (dendritic growth, via damage, layer damage)
	5	Devastating damage (delamination, corrosion/oxidation, major cracks)

4.3.4. Scanning Electron Microscopy (SEM)

Scanning electron microscopy is a method by which samples are placed into a low vacuum chamber where high energy electrons (~30 keV) bombard the surface at a certain angle. There are several types of modes, however the mode utilized in this research was that of secondary electron detection. The incident stream of electrons interact with the surface levels of the material (around 50 nm depth) and knock stable electrons out of their shell and on an exit path similar to a reflection from the original beam. That 'reflected' beam of electrons is gathered by a detector which measure the incoming angle and forms a detailed two-dimensional image of the surface. Most modern SEMs are able to resolve down to below 10 nm features[18]. The SEM used for this research was the FEI Nova Nanolab 200 located in the Arkansas Nano-Bio Materials Characterization Facility at the UA (see Fig. 4.5 for setup).

4.3.5. Energy Dispersive X-Ray Analysis (EDX)

Energy dispersive x-ray analysis (EDX) is a chemical analysis technique used to examine specific elements that show up in a sample and their relative percent makeup. This method is useful for identifying changes that occur on a molecular scale, such as oxidation, material migration, and the formation of alloys or other intermetallic compounds.

This method works by examining the energy level of photons emitted in the x-ray band from a high energy electron beam knocking out other stable electrons from atoms in the sample, which in turn causes an atom to shift down in energy level thus emitting an energetic photon[19]. EDX is commonly found as an additional mode in existing SEM tools as ejecting a secondary electron creates the atoms downward shift in energy level. This concept is illustrated in Fig. 4.2.

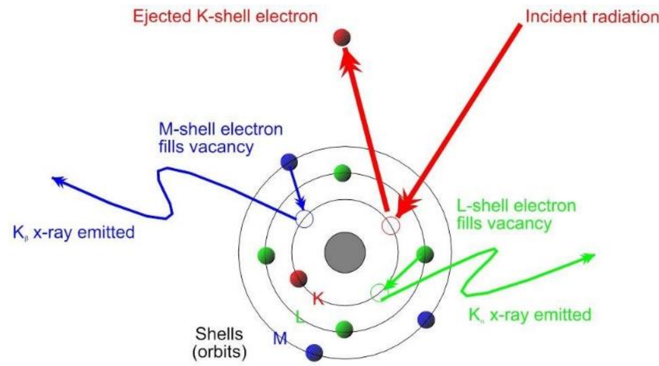

Fig. 4.2. The operating physics of EDX.

EDX analysis gives two type of data outputs. First is a line graph of all energy levels detected, where spikes or peaks in intensity correspond with known elemental signatures. This first type of data output is demonstrated in Fig. 4.3. The second type is called elemental mapping. In this method each element in the selected area of the sample is assigned an arbitrary color and is 'mapped' out and overlaid with selected elements that are being searched for in the sample. This elemental mapping method is shown in Fig. 4.4. The first method is useful in identifying what elements a sample consists of and the second method is useful for identifying where there may be overlap in the elements, indicating an alloy or evidence of oxidation.

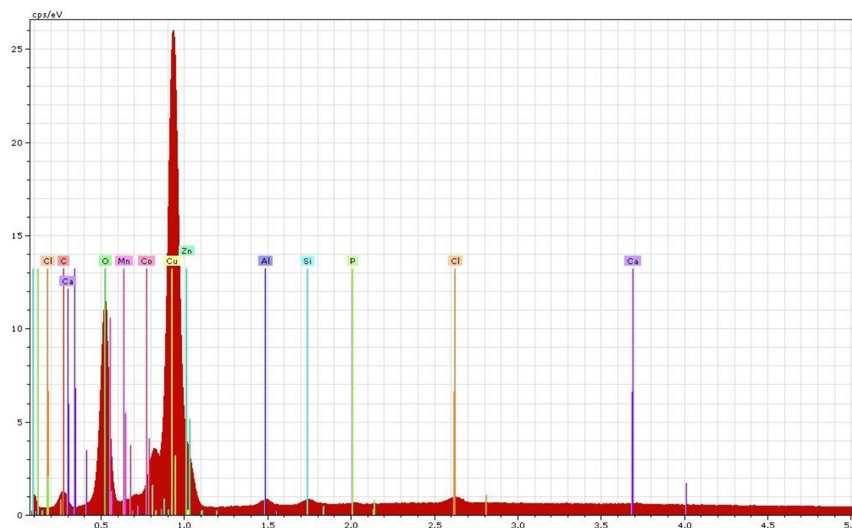

Fig. 4.3. Example of EDX method one for data output.

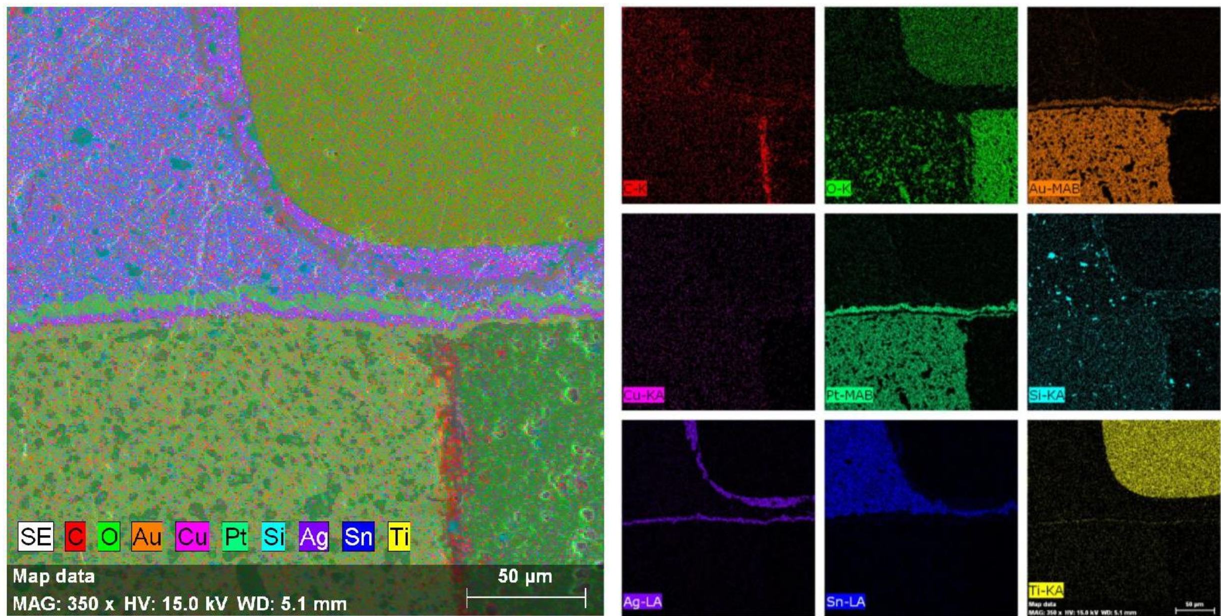

Fig. 4.4. Example of elemental mapping, method two of EDX data output.

In Fig. 4.3, which is the first method of EDX data output, energy level is listed on the x-axis of the graph with the y-axis being intensity. Each value of energy level corresponds with an element, whereas the intensity indicates whether that element is present or not in the sample. Fig. 4.4, the second method of EDX data output, shows each element being broken down by individual color on the right, with all the colors overlaid on top of one another on the left. This particular example shows thin and discrete lines of silver (Ag) where a silver thin film pad was on the outside lining of a surface mount device.

An FEI Nova Nanolab 200 was used for energy dispersive x-ray analysis. This was the same tool that was used for SEM analysis at the UA located in the Arkansas Nano-Bio Materials Characterization Facility. An image of the equipment setup can be found in Fig. 4.5.

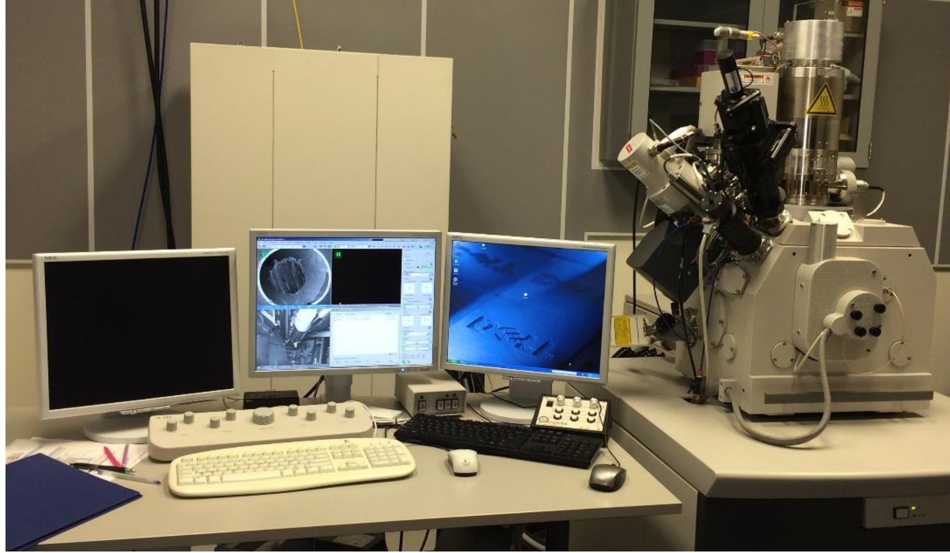

Fig. 4.5. Equipment setup for SEM and EDX analysis using FEI Nova Nanolab 200.

Chapter 5 Experimental Results

The results and findings of all the tests and analysis methods described previously are organized into seven sections. The first section will describe the baseline measurements, observations, and comparisons of all the LTCC coupons. Sections two through six describe each of the five tests, following a cadence of three subsections each: an overview and review of the test, results and observations, and a discussion of the results or observations. The seventh and last section is a discussion of all the results taken as a whole, noting results common across all tests.

5.1. Baseline Observations

A series of observations was performed before any tests were administered for the purpose of establishing a baseline for future observations. A sampling of many of the features will be shown below and given a brief description. Each image will be of part of the 14 major feature groups that were listed in section 3.1 and found in Fig. 5.1. Special attention will be paid to the thermal vias in feature group 9, and the comparison between feature groups 11, 12, and 14. Feature group 11 consisted of thin film directly on LTCC, group 12 utilized thin film sealing of thick film on LTCC, and 14 was a baseline that used thick film elements directly on LTCC. Another area of focus will be the 0402 surface mount device (SMD) pads in feature groups 1 and 8, and the 0603 SMD pads in feature groups 2 and 7. The purpose of these groups was to ascertain if there was any solder diffusion evident in the pads or substrate or if there was any indication that the thin film has diffused into the solder.

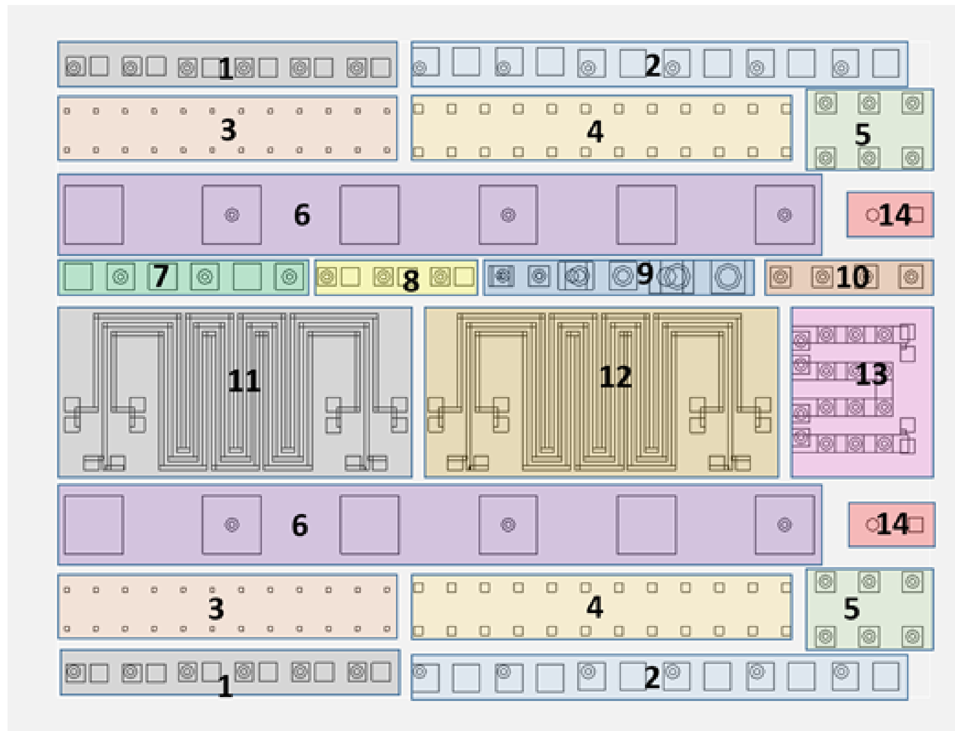

Fig. 5.1. Illustration of the 14 major feature groups of Coupon 1.

In Fig. 5.2 and Fig. 5.3 are shown a pair of 0603 surface mount device pads from feature group 2. Fig. 5.2 shows a simple thin film pad direct on 9K7 LTCC with no via. Fig. 5.3 shows a surface pad with a via, notice the inner dark circle which was the actual via, and the outer dark circle which was a thick film cover pad over the via. This cover pad was there to promote a seamless transition from thick film to thin film as and to help mitigate any difference in height the via may have had with respect to the LTCC substrate surface.

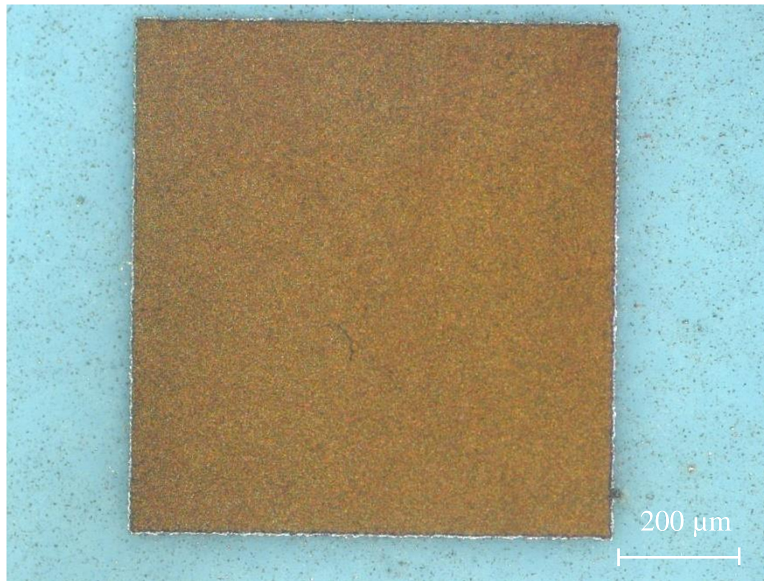

Fig. 5.2. Pristine 0603 SMD surface pad with no via.

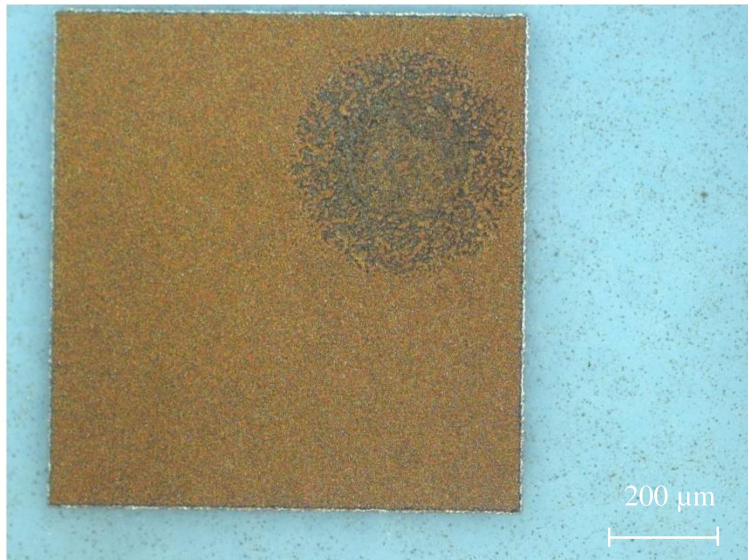

Fig. 5.3. Pristine 0603 SMD surface pad with 15 mil. diameter via.

The next three figures show feature group 9, the thermal vias of 10, 20, and 30 mil diameter, respectively. Fig. 5.4 shows a 10 mil thermal via with thick film cover pad on 951 LTCC substrate. Fig. 5.5 shows a 20 mil thermal via with thick film cover pad on 9K7 LTCC.

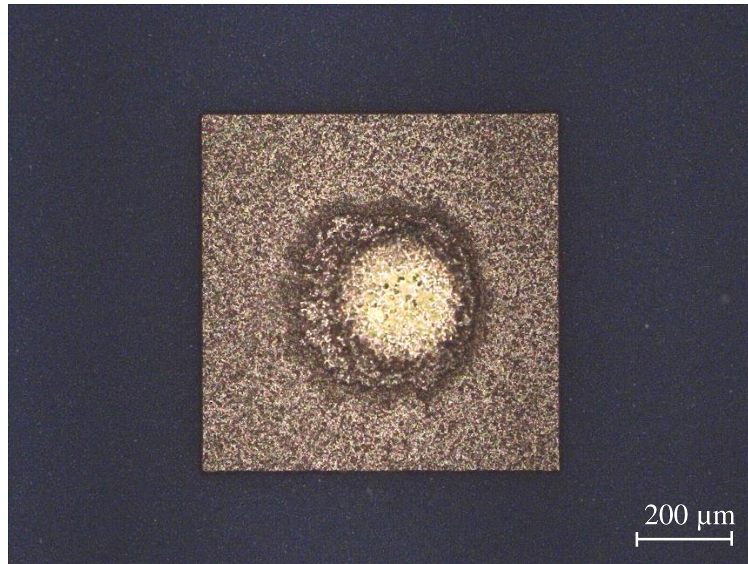

Fig. 5.4. A pristine 10 mil. diameter thermal via.

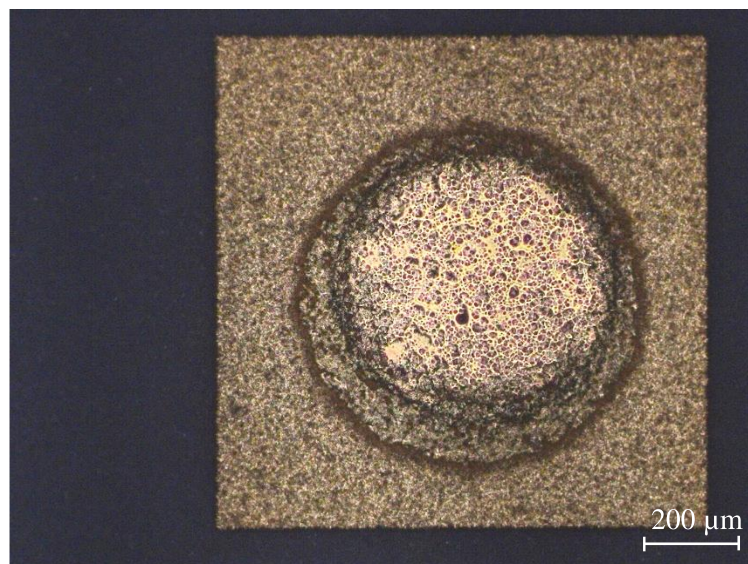

Fig. 5.5. A pristine 20 mil. diameter thermal via.

Fig. 5.6 shows a 30 mil thermal via with cover pad on 951 LTCC substrate. Notice the domed surface of all the thermal vias. Fig. 5.7 shows an example of several small divots left as artifacts between the thermal via and thick film cover pad during processing and fabrication.

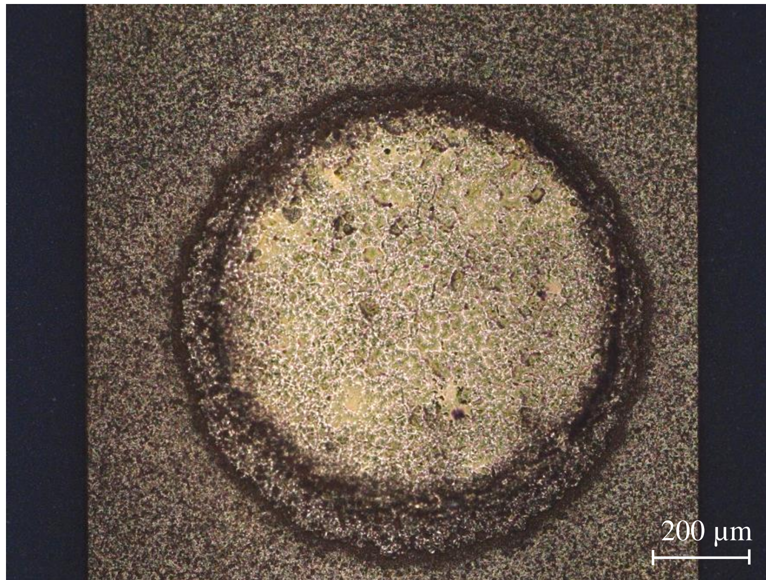

Fig. 5.6. A pristine 30 mil. diameter thermal via.

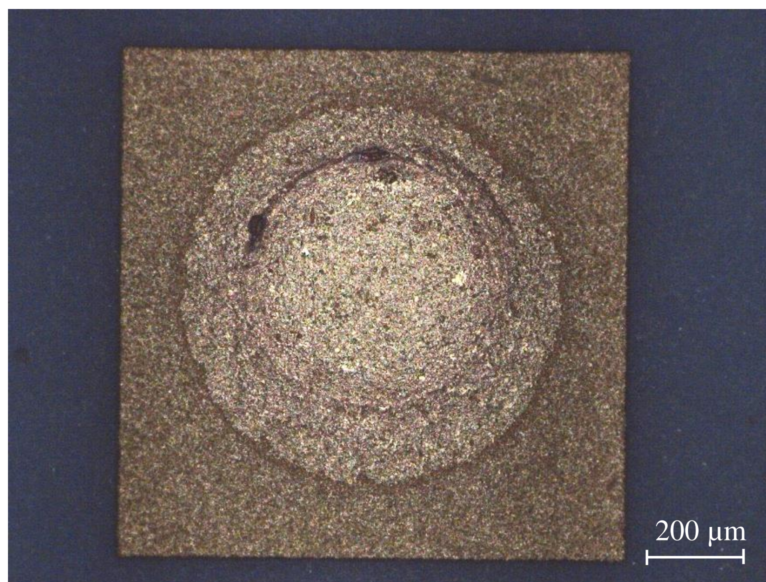

Fig. 5.7. An example of a thermal via cover pad with processing artifacts.

Fig. 5.8 shows feature group 1, which was a 0403 surface mount device pad set with one pad having a via and one with no via. Fig. 5.9 shows feature group 11 which was the triple track system that consisted of thin film direct on the LTCC substrate. Line widths are 6 mils.

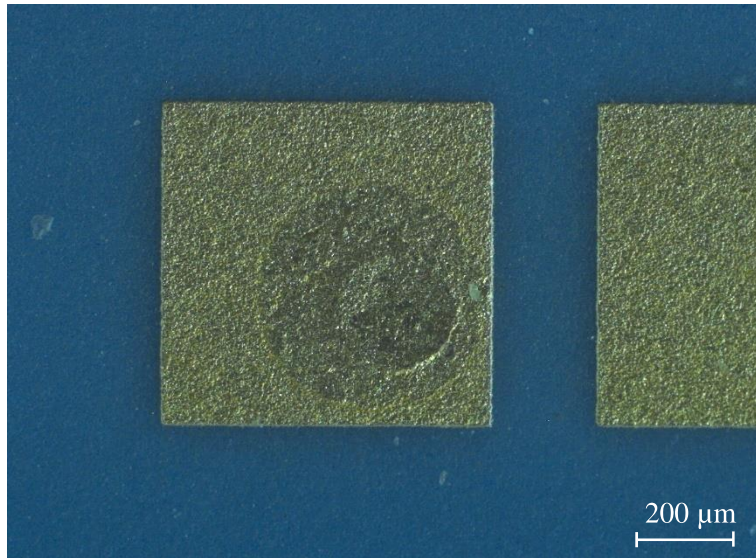

Fig. 5.8. A pristine 0402 SMD set, pad with via on the left and without a via of the right.

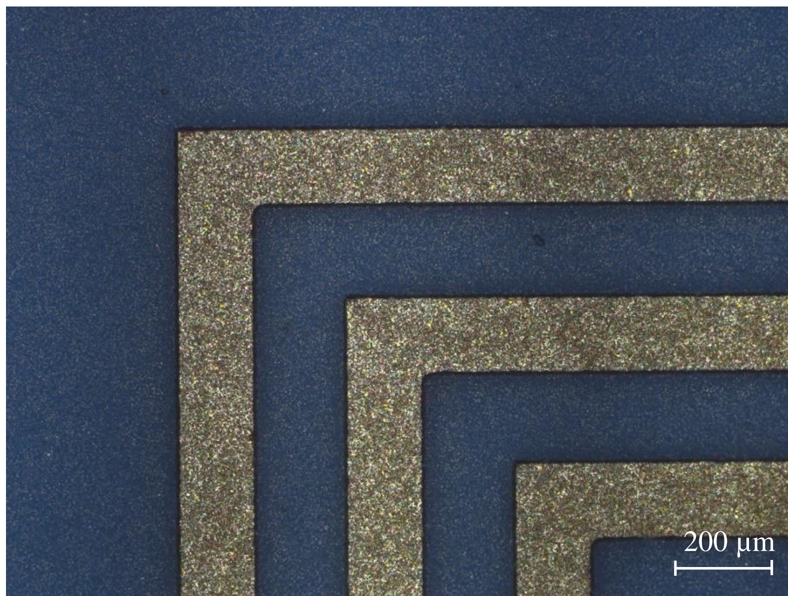

Fig. 5.9. A pristine triple track from feature group 11 (thin film direct on LTCC).

Fig. 5.10 show feature group 12, a triple track system with thin film covering or sealing the thick film layer. Fig. 5.11 shows a processing artifact of misalignment of either the thick or thin film layers.

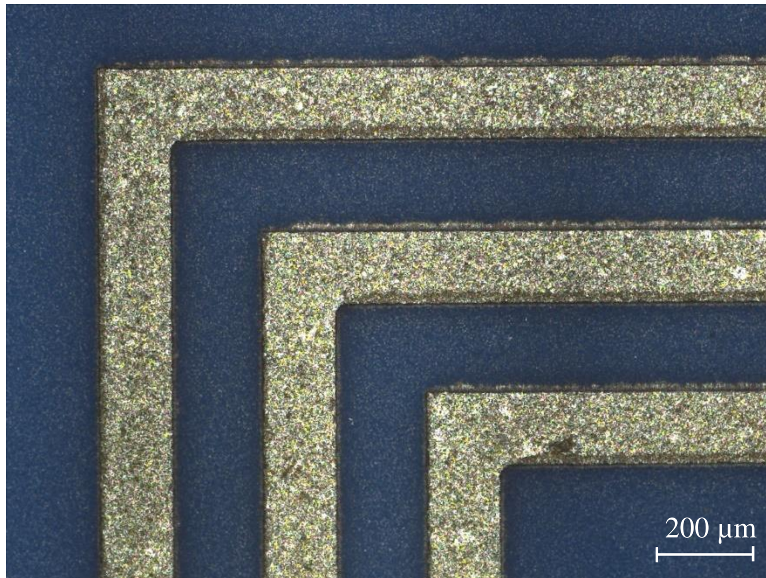

Fig. 5.10. A pristine triple track from feature group 12 (thin film sealing Au thick film).

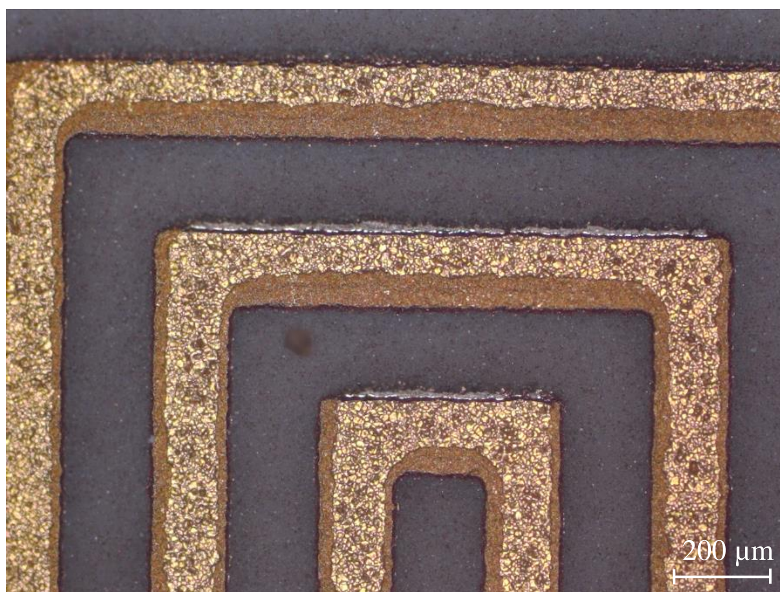

Fig. 5.11. Thin / thick film misalignment, a triple track processing artifact.

The next four figures show the baseline thick film elements from feature group 14. Fig. 5.12 shows a Au thick film pad direct on LTCC. Fig. 5.13 shows an unsealed Au via.

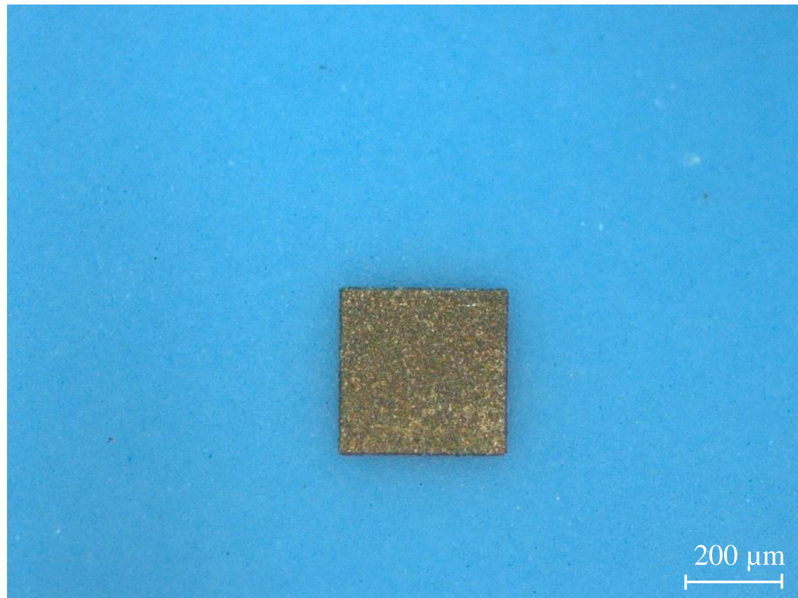

Fig. 5.12. A pristine baseline Au pad thick film element.

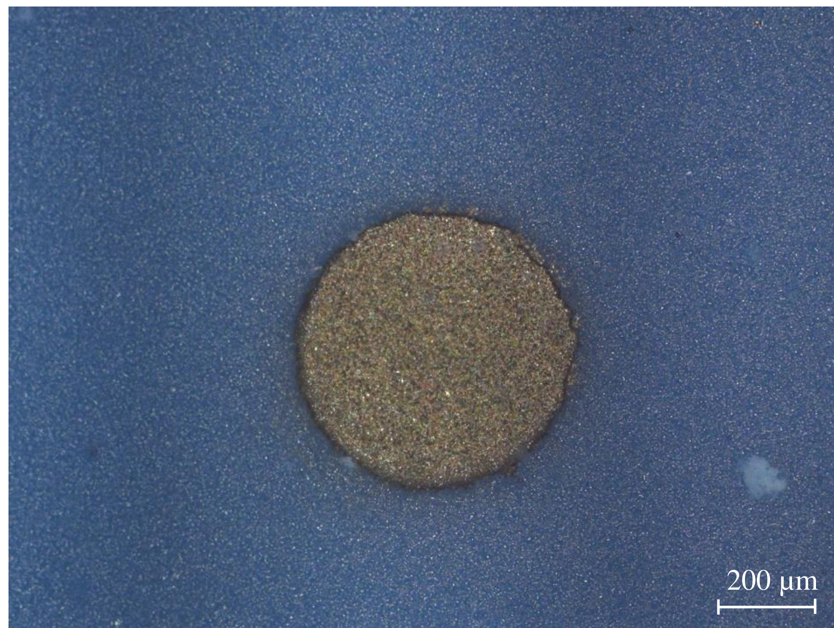

Fig. 5.13. A pristine baseline Au via thick film element.

Fig. 5.14 shows an unsealed Ag thick film via. Fig. 5.15 shows a Ag thick film pad direct on LTCC.

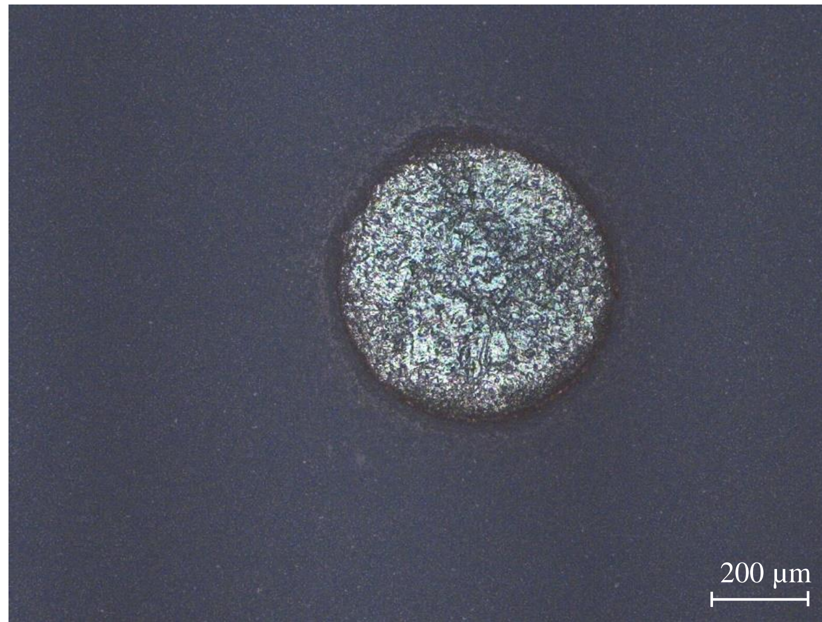

Fig. 5.14. A pristine baseline Ag via film thick film element.

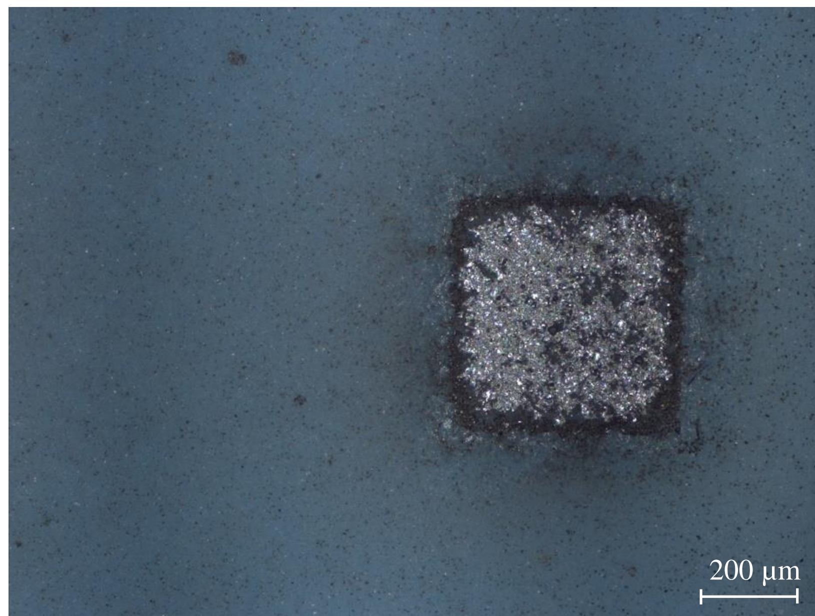

Fig. 5.15. A pristine baseline Ag pad thick film element.

Fig. 5.16 shows feature group 6, which are large pads with and without vias for pin pull testing. Fig. 5.17 shows the beginning via for the daisy chain in feature group 13.

Fig. 5.16. A pristine via covered with large pin pull test pad.

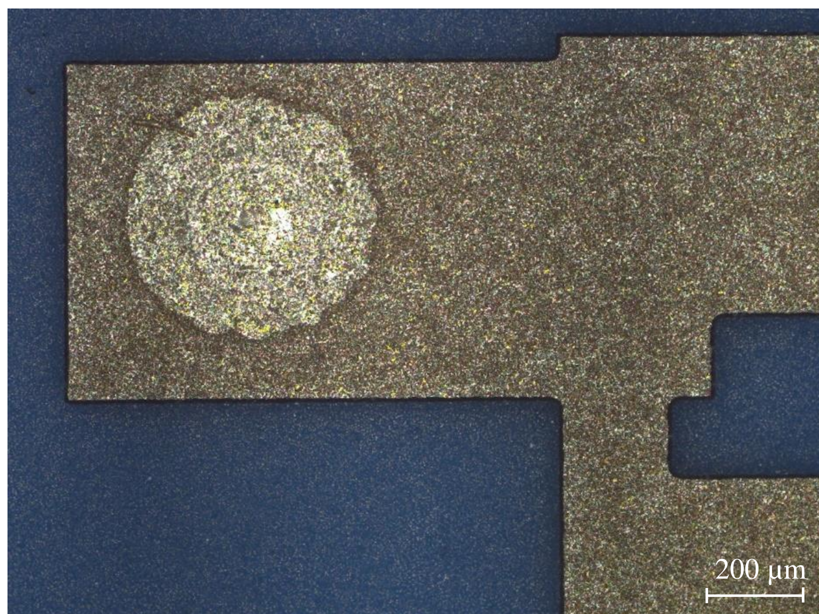

Fig. 5.17. A via as part of the daisy chain feature system.

5.2. Lifetime Testing

5.2.1 Test Overview

Lifetime testing was performed for 100 days at an elevated temperature of 170 °C. There was one power failure at approximately 48 hours into the test when a large lightning storm overloaded circuit breakers in the building. The test was resumed within 12 hours and continued for 98 more full days uninterrupted.

5.2.2 Test Results

What follows is a series of images taken after the full 100 days with observations.

Fig. 5.18 shows a 12 by 12 mil pad from feature group 4, which was thin film direct on LTCC. It was observed that there was color shifting of the thin films, specifically around the edges of features. This could be described as a baking of the metallization stack up. This rated as a level 3 on the rating scale, which was a fail.

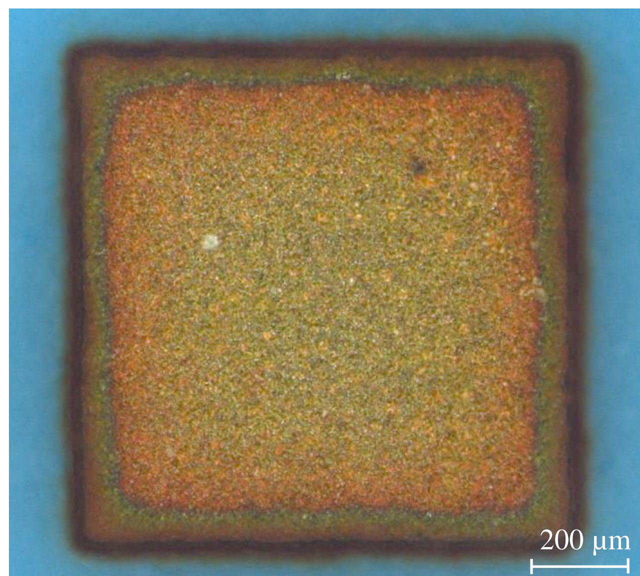

Fig. 5.18. A thin film (recipe A) pad on 9K7 LTCC.

Fig. 5.19 shows divots and cratering around a 30 mil thermal via from group 9, and ranked as a level 4 in terms of damage which was a fail. Fig. 5.20 shows a failure in group 12 of the thin film not being able to seal completely the thick film layer, and rated as level 4 damage.

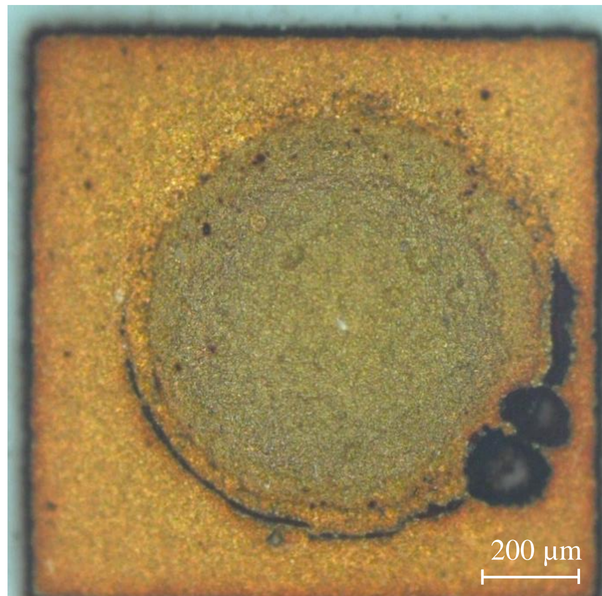

Fig. 5.19. A 30 mil. thermal via showing divots and cratering on sample 227.

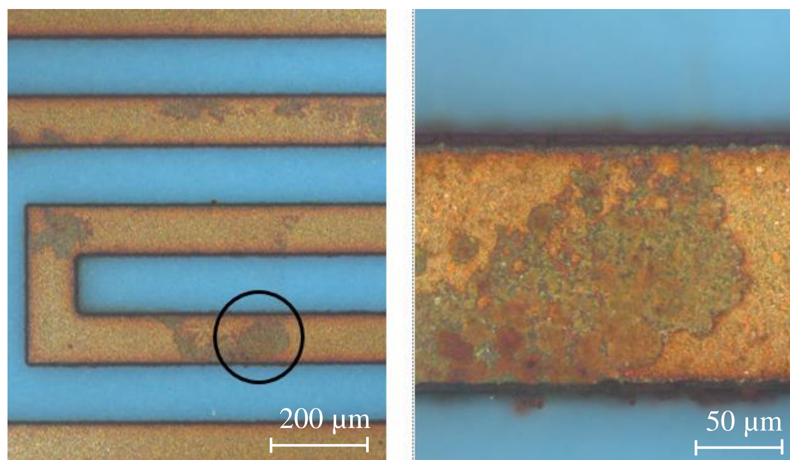

Fig. 5.20. Damage shown on triple track (group 12) on sample 127.

Fig. 5.21 shows a group 14 thick film baseline element with material migration which would rank as a 3 and a fail. Fig. 5.22 shows material migration, color change, and a divot formed in a feature group 2 thin film covered via.

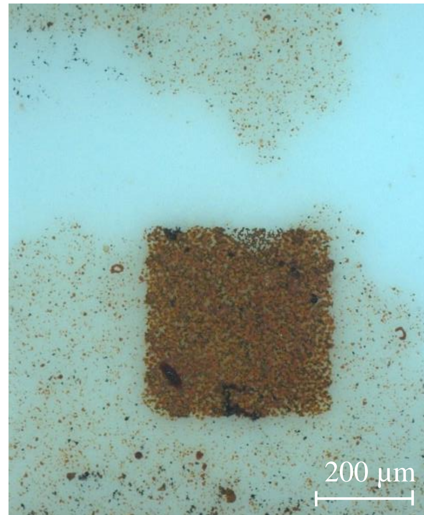

Fig. 5.21. Material migration of Au thick film baseline element from sample 318.

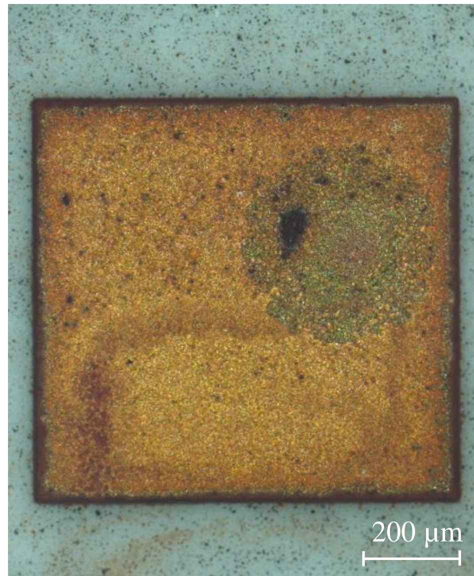

Fig. 5.22. Material migration and divot shown on a thin film covered via from sample 317.

Cross sections of the thermal vias revealed that much of the devoting and cratering was being caused by the metal slugs of the vias separating from the sidewall of the LTCC substrates. Fig. 5.23 shows this happening with the 9K7 substrate and Fig. 5.24 with the 951 substrate.

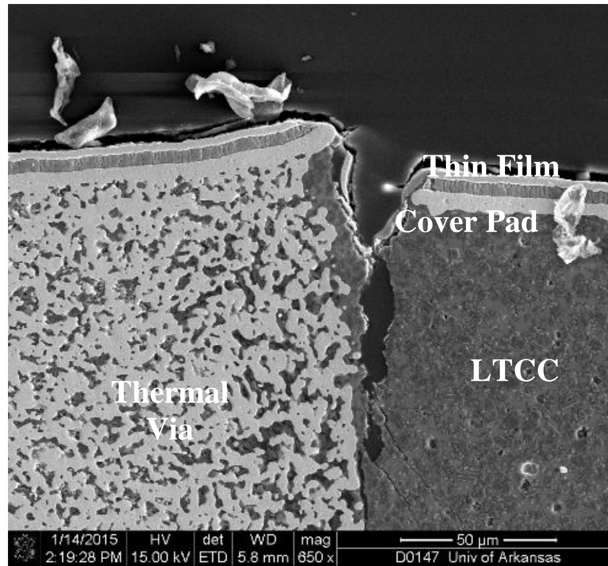

Fig. 5.23. A SEM cross section showing via separation from 9K7 LTCC sidewall.

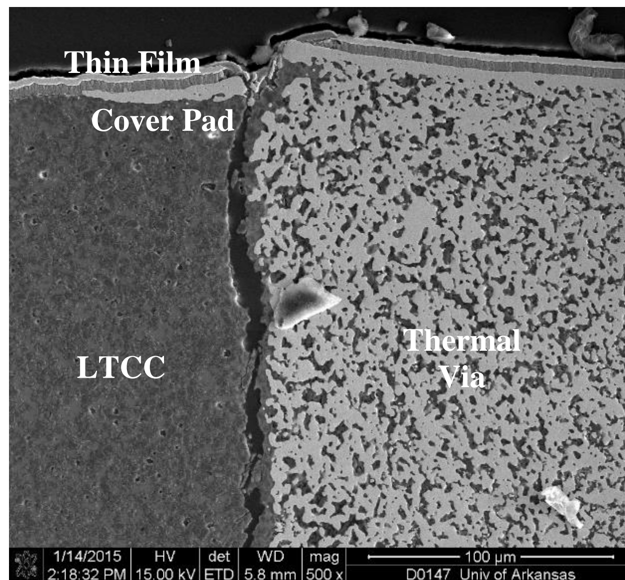

Fig. 5.24. A SEM cross section showing via separation from 951 LTCC sidewall.

Based on the optical microscopy observations and the numbering system, trends could be drawn using the data gathered. What follows is a sampling of the most important, interesting, and pertinent trends from the five levels of damage.

Fig. 5.25 shows a comparison between the DuPont 951 (left) and the DuPont 9K7 (right) substrates across all feature groups and all other material system parameters. The height of the bar corresponds with the percent accumulation and the number indicated the absolute number of features ranked, for example the number of twos for 951 was 756, which correlates to its relative percentage of all ranked 951 features, or about 60% minus 20%, giving about 40% which were ranked a two. This same number also was useful in determining the resolution of and, consequently, the confidence of the data. Knowing there are over 1,700 data points per column in this graph was reassuring. Slicing the data in this manner was useful as it demonstrates that in general, features on the 951 substrate material were more reliable than those on the 9K7

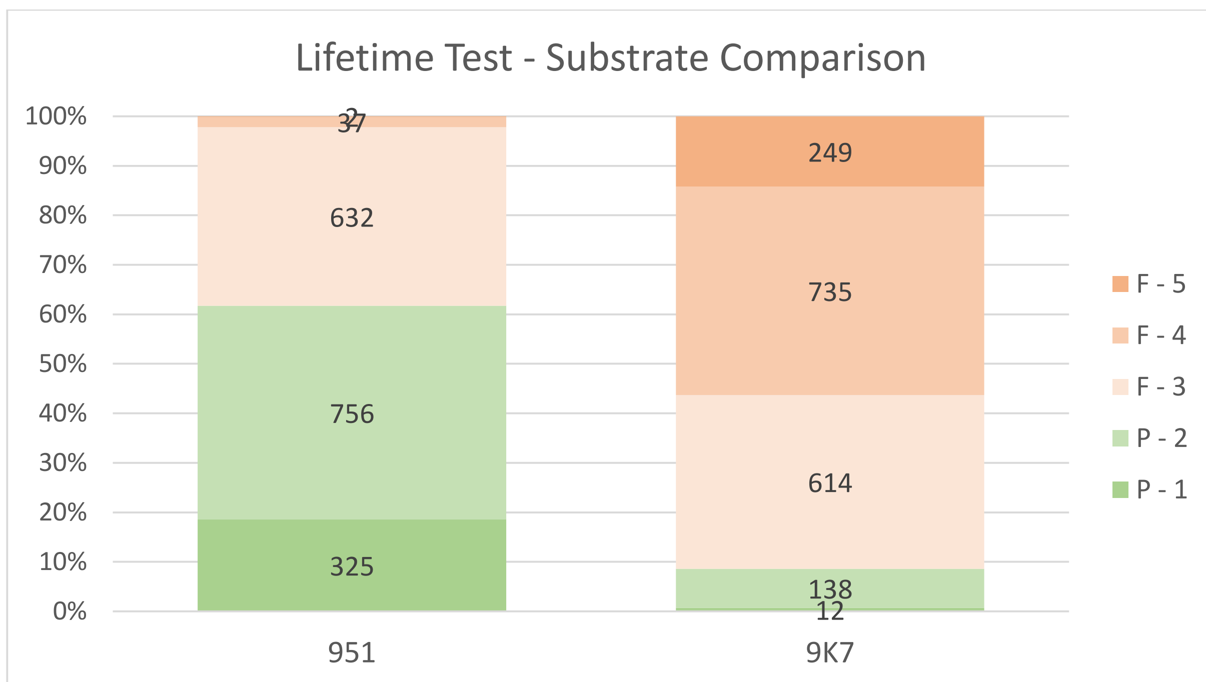

Fig. 5.25. The lifetime test substrate comparison.

substrate. Furthermore, there was a wide disparity between the absolute number of features ranked at the maximums, one or five.

Fig. 5.26 shows a comparison between the two thick film metallizations, Au on the right and Ag on the left, across all feature groups and all other material system parameters. In this instance, the overall pass fail rate was very similar, especially realizing the major source of error occurred between the human perception between twos and threes. However, it was shown that the major differences did not occur between the twos and threes, but rather the ones and fives. This shows that even though the pass rate was similar, Au still held and advantage over Ag thick film due to gold's higher number of level ones and silvers higher number of level fives.

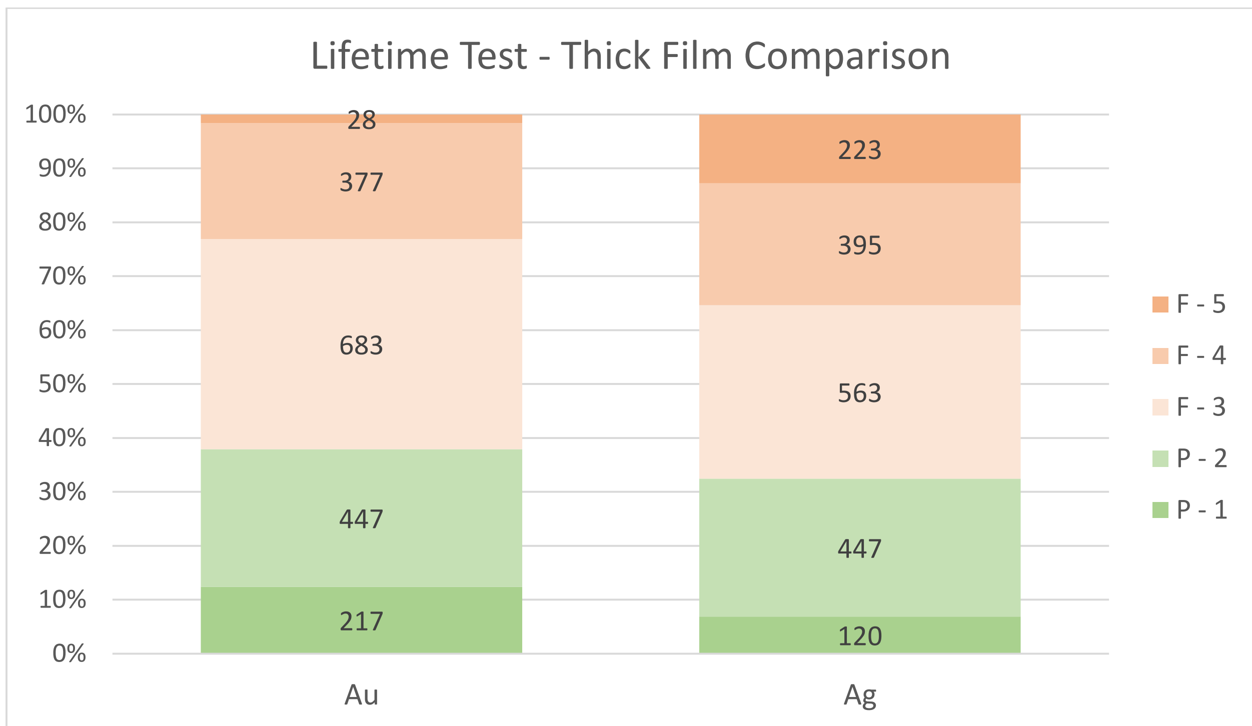

Fig. 5.26. The lifetime test thick film comparison.

Fig. 5.27 shows the comparison between the two thin film recipes present in the lifetime test. Recipe A (left) was the Ti/Cu/Pt/Au stack up with thicknesses of 0.2/4/2/0.375 μm respectively, and recipe B (right) was the same stack up and thicknesses minus the Ti layer. Again, the pass fail rate was very similar between the two, however the major differences are shown in the level one ratings for A and the level 5 ratings for B. This demonstrates that thin film A had an advantage over recipe B in the lifetime test.

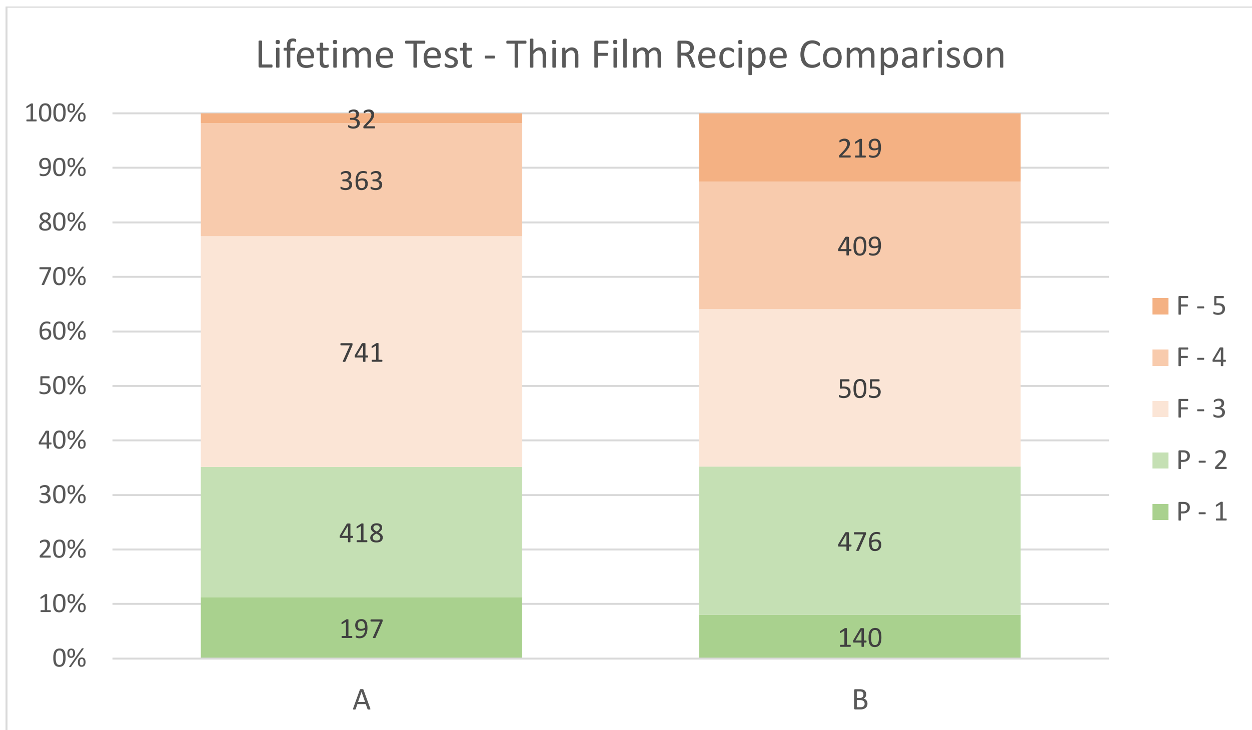

Fig. 5.27. The lifetime test thin film recipe comparison.

Fig. 5.28 shows the comparison between the thermal vias by the three via sizes, 10, 20, and 30 mil diameter vias, respectively. Notice that the resolution of the data, dictated by the number of available points, was reduced from the other comparisons. There were only two thermal vias of each size located per coupon. Given the primary source of error was the repeatability of the human perception between level 2 and level 3, the standard error was high in this comparison. Keeping that in mind, however, the 10 mil via diameter was more reliable than the larger two by an appreciable amount considering the data resolution. No hard conclusion could be drawn between the 20 and 30 mil vias, though it is interesting to note that the 20 mil via had one more level 5 rating than the 30 mil, even though the 30 mil size had 6 more level 4 ratings than the 20 mil size.

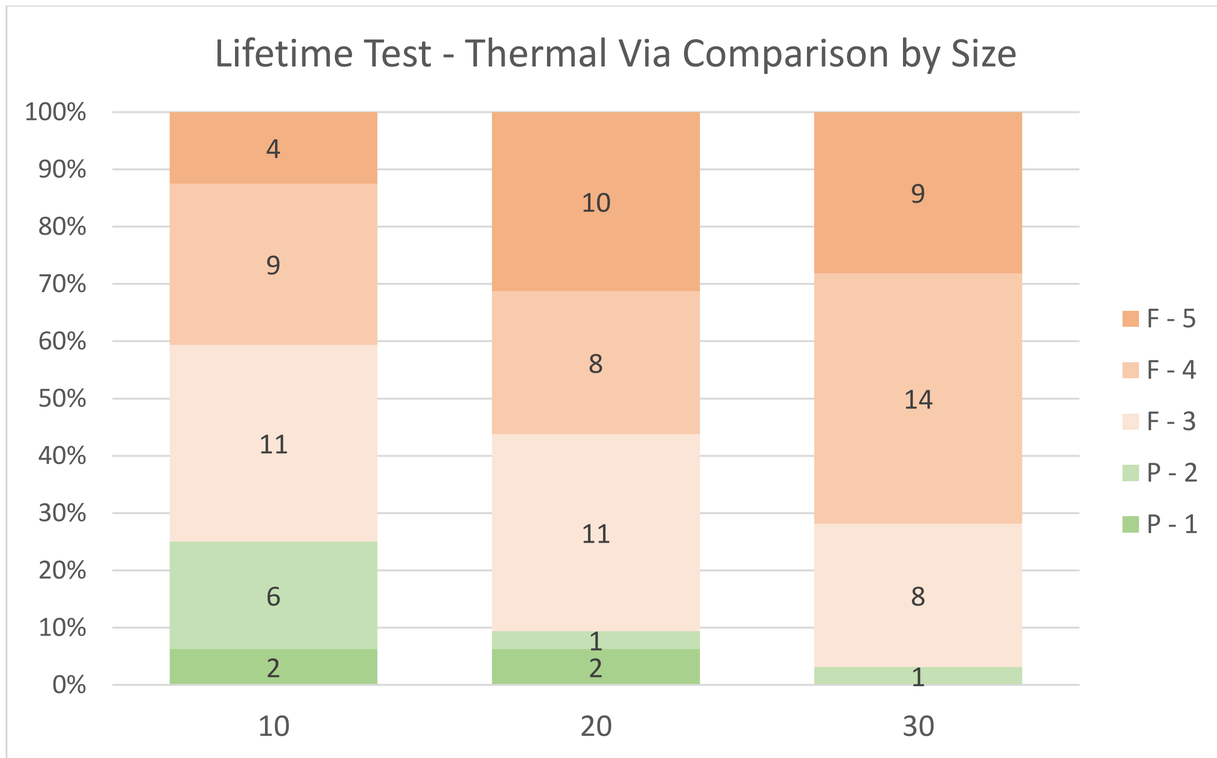

Fig. 5.28. The lifetime test thermal via comparison by size.

Fig. 5.29 compares three feature groups: group 11 which was thin film directly on the LTCC substrate, group 12 which was thin film sealed thick film, and group 14 which was the unsealed and exposed thick film elements. Note the difference in resolution (number of data points per column) of group 14, which was much lower resolution than the other two groups as there were only two data points per coupon for feature group 14. Regardless, there were two primary points that stood out. First was that thin film sealing of thick film was less reliable than thin film on substrate, as accounted by the difference between level ones and twos of groups 11 and 12. Second was that thin film sealing was indeed slightly more reliable in the lifetime test at elevated temperatures than exposed thick films, shown by the 15% difference between the pass fail rate of feature groups 12 and 14.

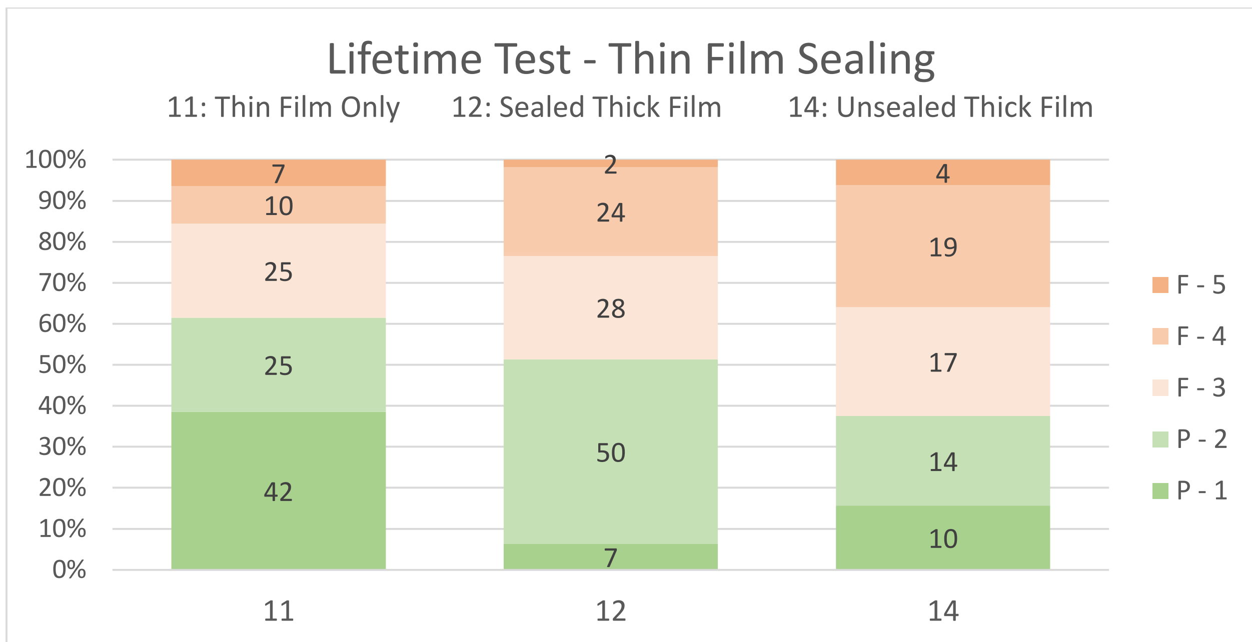

Fig. 5.29. The lifetime test comparison of thin film sealing.

5.2.3 Discussion of Lifetime Results

Reviewing what was discovered in the results for the lifetime at elevated temperature environmental reliability test there are a few things that stand out. First was how susceptible vias were throughout this particular test. Of particular interest was that the larger thermal vias were less reliable than the smaller or standard ones. Secondly was the differences between how the test interacted with the substrates and the thick films. From Fig. 5.25 and Fig. 5.26 it can be concluded that the outcome of pass/fail was more sensitive to the substrate than the thick film metallization. The most reliable LTCC thick film material system was the 951 Au, with the least reliable being 9K7 Ag, which unfortunately would be the most favorable material system for use in real world applications. The outcome of the hypothesis that thin film sealing of thick would improve the overall reliability, while proven true in this scenario, was marginal, and it was interesting to note that a sealed thick film was less reliable than thin film directly on ceramic.

5.3. Thermal Cycling

5.3.1 Test Overview

Thermal cycling was performed for 1000 cycles beginning from a high temperature of +165 °C then to low temperature of -65 °C, with a dwell time of 5 minutes at each extreme. The test was performed in a low thermal mass Delta 5023 oven with liquid nitrogen as the coolant. There were issues in beginning the test, where the oven would heat to 1 °C less than the high set temperature and shut off. This was found to be a problem with the internal memory of the tool needing to be reset from the prior test code loaded into the onboard RAM. There were no further complications in completing the test as specified.

5.3.2 Test Results

What follows is a series of images taken after the full 1,000 temperature cycles.

Fig. 5.30 is a photograph image of the triple track structure in feature group 11 that has delaminated from the surface of the ceramic substrate. Feature group 11 was thin film which was in direct contact with the LTCC. The thin film recipe used for this coupon was the B recipe, which has no Ti layer. The Ti layer was put into the thin film material stack to promote adhesion to the ceramic substrate. Every sample of thin film recipe B in the thermal cycling test had at least some evidence of delamination. Fig. 5.31 was part of another sample of thin film recipe B, where many of the solder and pin pull test pads had lifted off the substrate. Through the examination process was found that many pads were also loose and came off during handling, rather than fully delaminating in the chamber. Regardless, the damage was done.

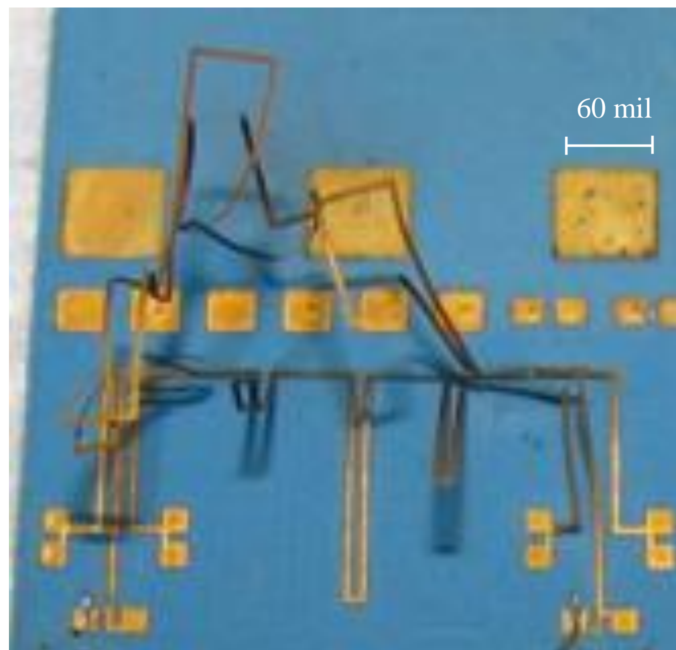

Fig. 5.30. Delamination of thin film direct on LTCC from sample 418.

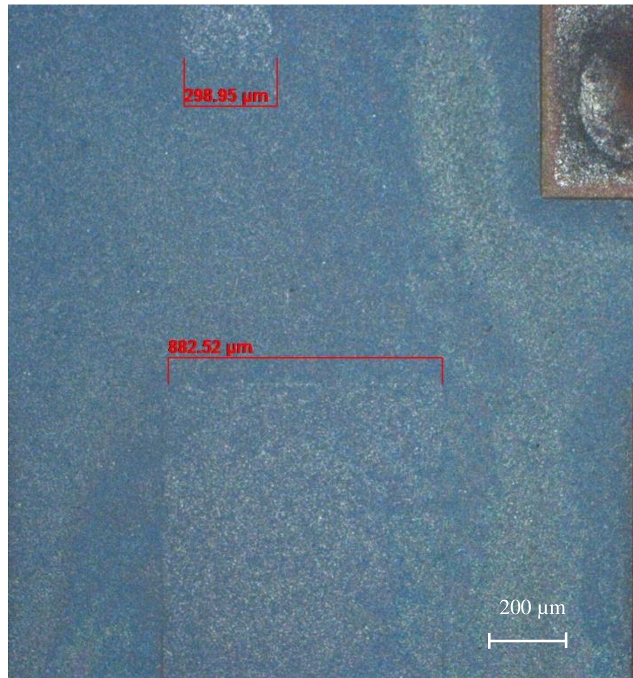

Fig. 5.31. Delamination of solder pads on sample 418.

Fig. 5.32 shows physical damage to the triple track structure in feature group 12. There was a darkening, or ‘charring’, which occurred among many features, ranking as a level 4.

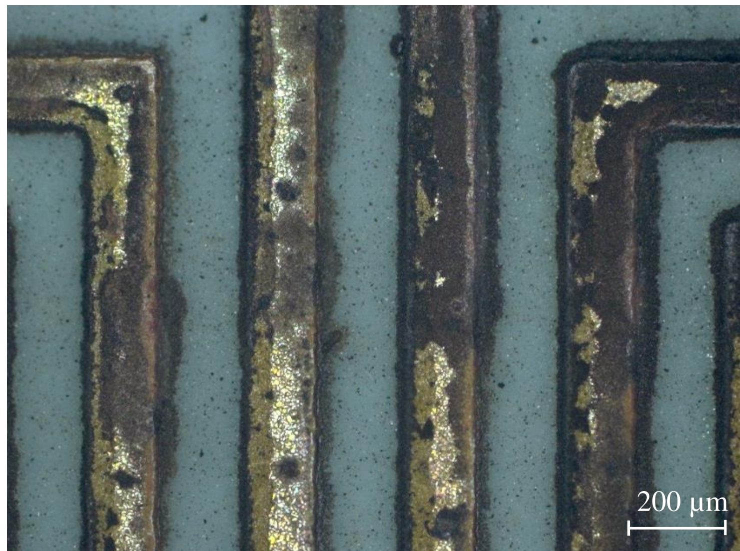

Fig. 5.32. Physical damage and 'charring'' on sealed triple track from sample 227.

Fig. 5.33 shows a triple track system on a 951 substrate material and a Ag thick film. The Ag thick film had migrated or spread across the sample. This was caused simply as a natural result of the test itself; as the silver expanded and contracted with the heat and cold numerous times, it migrated. Though this defect did not cause any electrical shorting in this particular instance, electrical shorting could have been possible under those conditions. This type of damage received a ranking level of 5.

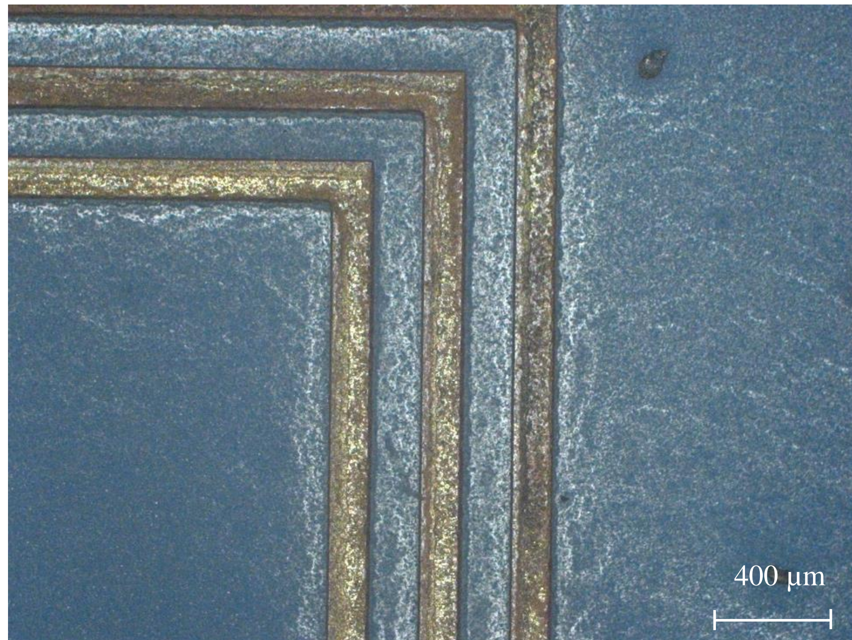

Fig. 5.33. Material migration on unsealed Ag on 951 substrate from sample 417.

Based on the optical microscopy observations and the numbering system, trends could be drawn using the data gathered. What follows is a sampling of the most important, interesting, and pertinent trends from the five levels of damage.

Fig. 5.34 shows the comparison of the two LTCC substrate materials, 951 on the left and 9K7 on the right, for the thermal cycling test. Notice that in this test, the 9K7 had the advantage in reliability over the 951. However, knowing the most significant source of error in this data was the repeatability of the human perception between a level 2 and a level 3 ranking, there was a large standard error in this graph. The 951 substrate though did have many more level five rankings than the 9K7. A conclusion can be drawn when also taking into account the thin film B recipe (no Ti) delaminating along with the 9K7's rougher surface causing the recipe B stack up to have greater adhesion. However, this had problems of its own with thin film discontinuities. Using a focused ion beam and scanning electron microscope, the previous claim was confirmed. See Fig. 5.35 and Fig. 5.36.

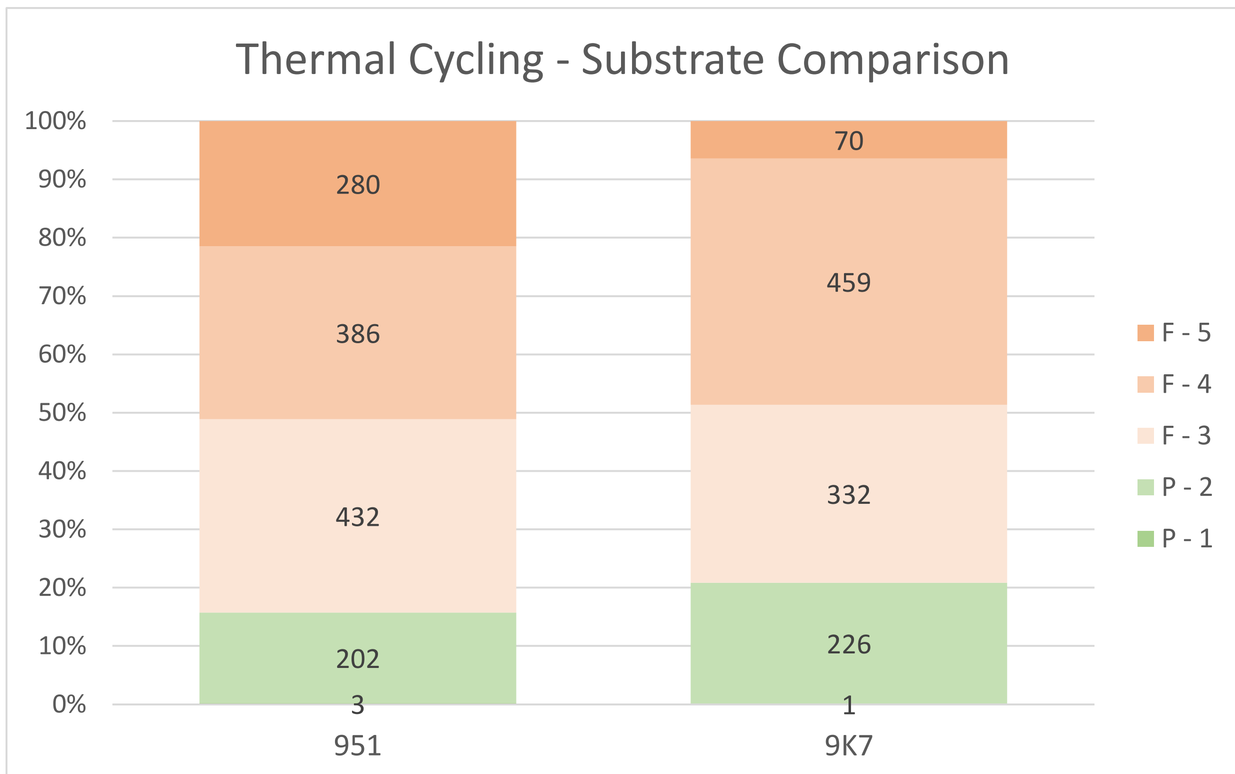

Fig. 5.34. The thermal cycling substrate comparison at 1,000 cycles.

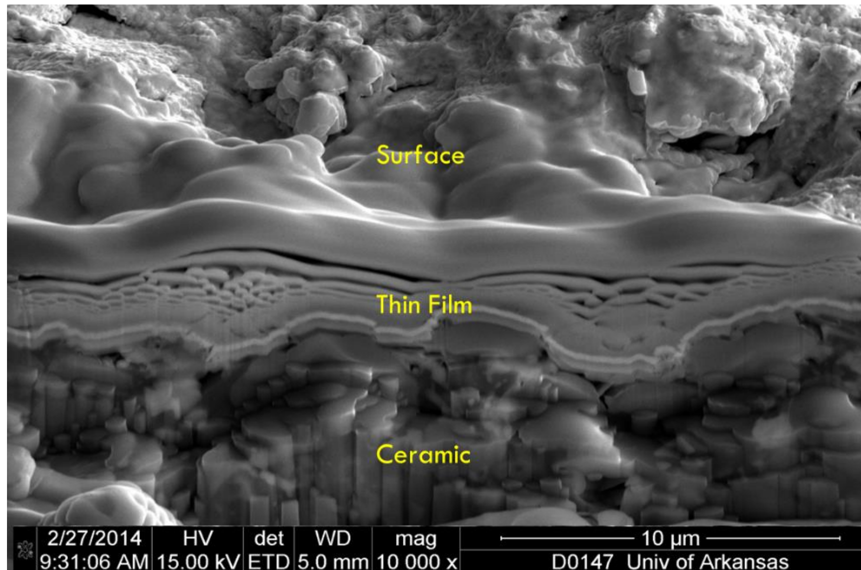

Fig. 5.35. Surface roughness analysis of 9K7 LTCC substrate.

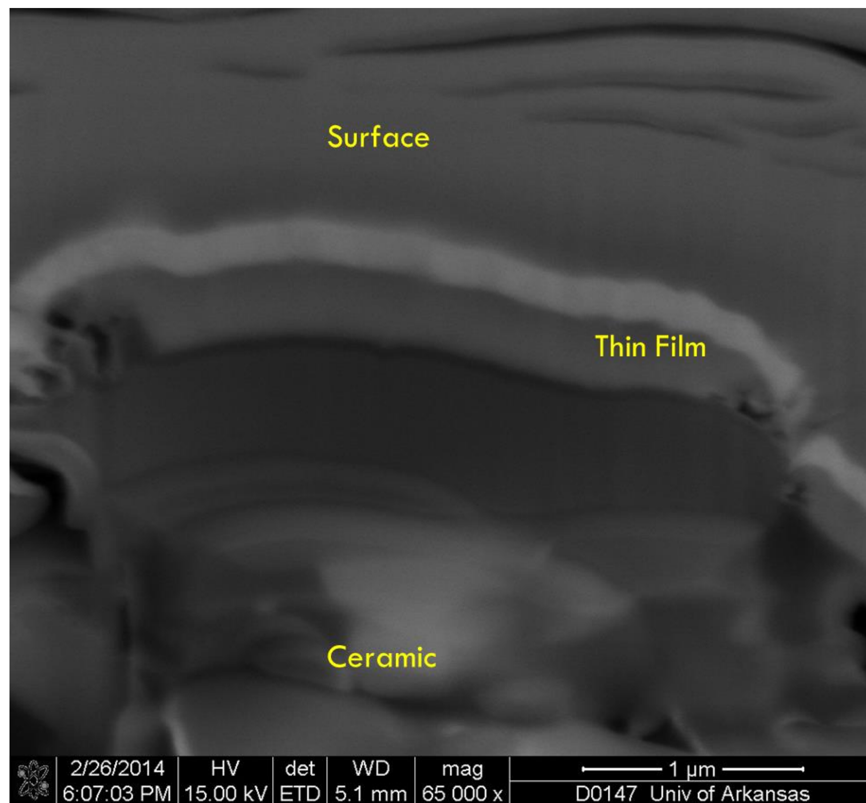

Fig. 5.36. A thin film discontinuity due to surface roughness on a 9K7 substrate.

Fig. 5.37 shows the thick film metallization comparison for the thermal cycling test at 1000 cycles. There was no significant difference in the pass fail rate, though it was interesting to note the difference in the number of level 5 ratings; Au still was more reliable at this level. Thermal cycling was a rough test, and neither thick film was immune from its effects.

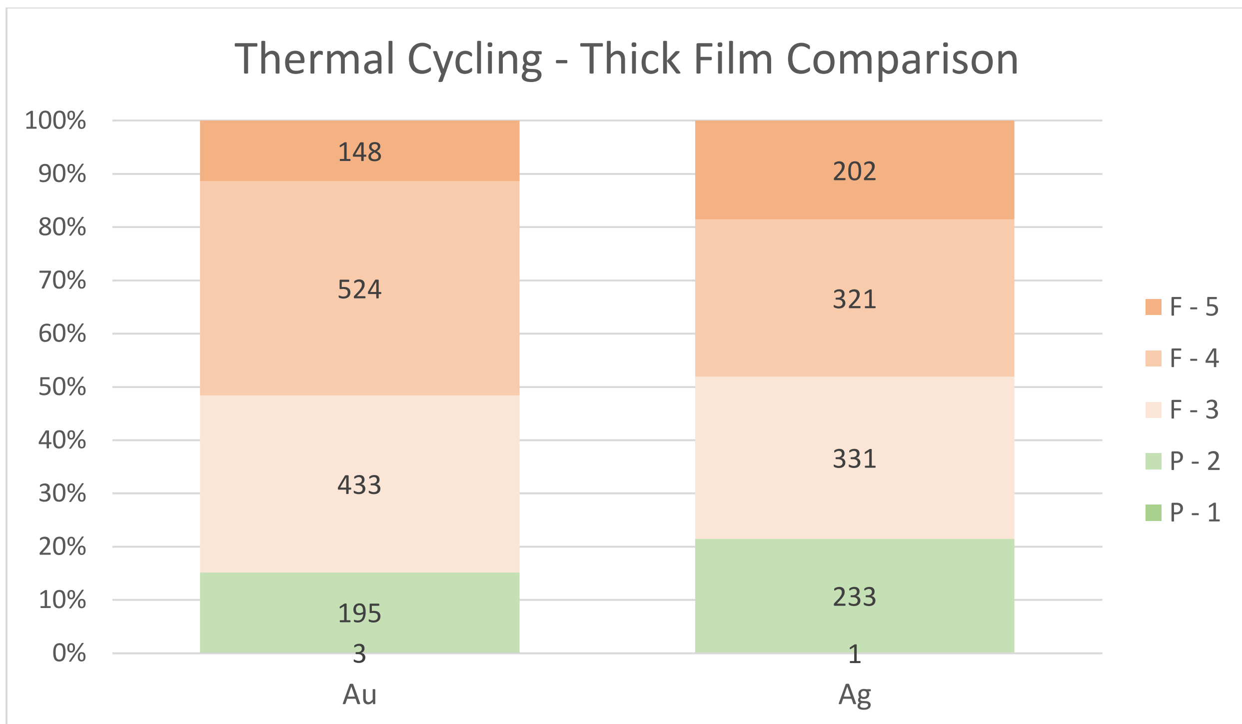

Fig. 5.37. The thermal cycling thick film comparison at 1,000 cycles.

Fig. 5.38 shows the comparison between the thin film recipes present in this thermal cycling test. There was about a 10% difference in the pass fail rate between recipe A (with Ti) on the left and recipe B (without Ti) on the right. The most interesting observation about this graph, however, was the drastic difference in the number of level 5 rankings between the two. Thin film recipe B (without Ti) was less reliable, and when it failed, the failure mode was most often catastrophic. The absolute failure rate was still poor nonetheless, no matter how the data was sliced.

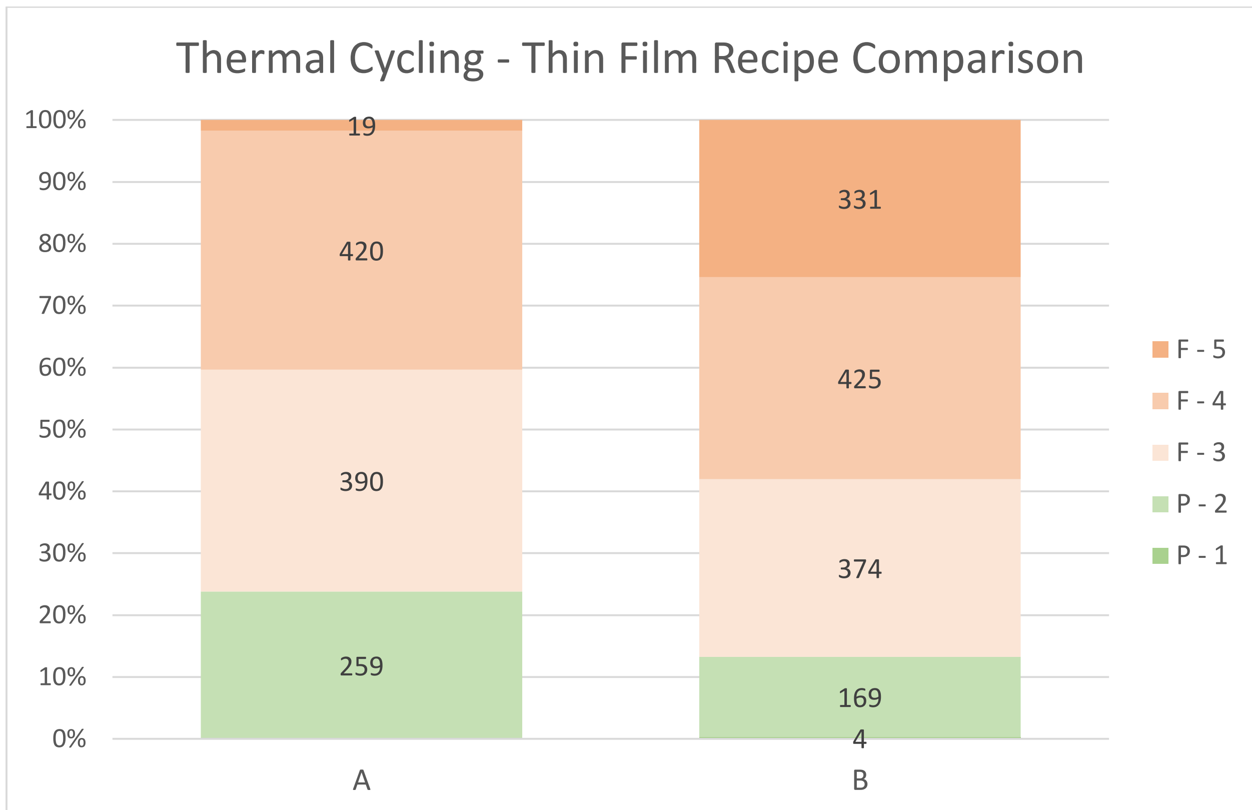

Fig. 5.38. The thermal cycling thin film recipe comparison at 1,000 cycles.

Fig. 5.39 shows the comparison of thermal via, feature group 9, by via diameter. This graph shows that thermal vias were not reliable in an extreme thermal cycling scenario. There was a 100% fail rate, though with the larger diameter vias there were more catastrophic damage. This was caused by the metal slug expanding and contracting with the temperature changes. This also caused divots and cratering around the edges of the vias on the surface, and was confirmed through cross sections that the vias were separating from the LTCC sidewalls.

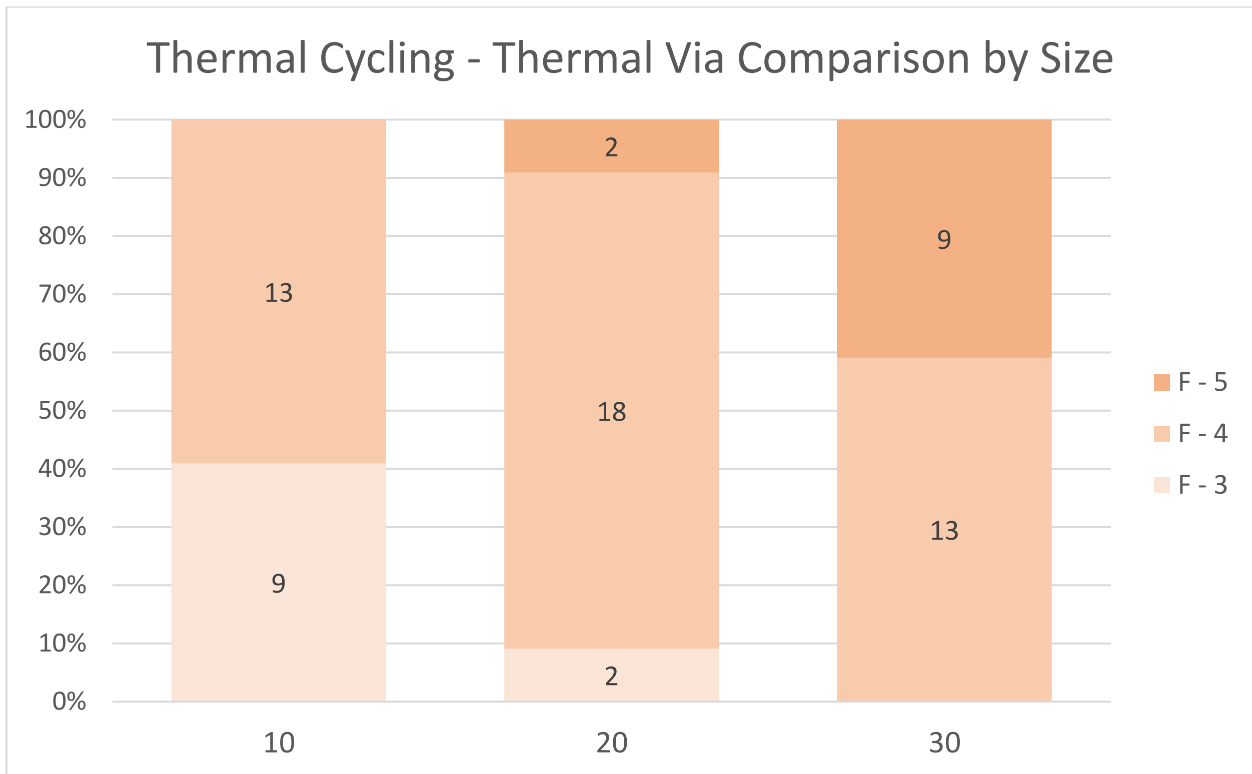

Fig. 5.39. The thermal cycling thermal via comparison at 1,000 cycles.

Fig. 5.40 compares three feature groups: group 11 which was thin film directly on the LTCC substrate, group 12 which was thin film sealed thick film, and group 14 which was the unsealed and exposed thick film elements. Note the difference in resolution (number of data points per column) of group 14, which was much lower resolution than the other two groups as there were only two data points per coupon for feature group 14. Regardless, the pass and fail rates of the three groups were similar. It was of key interest to note that the thick film elements in group 14 actually were more reliable in this test that either the thin film direct on ceramic or the sealed thick film.

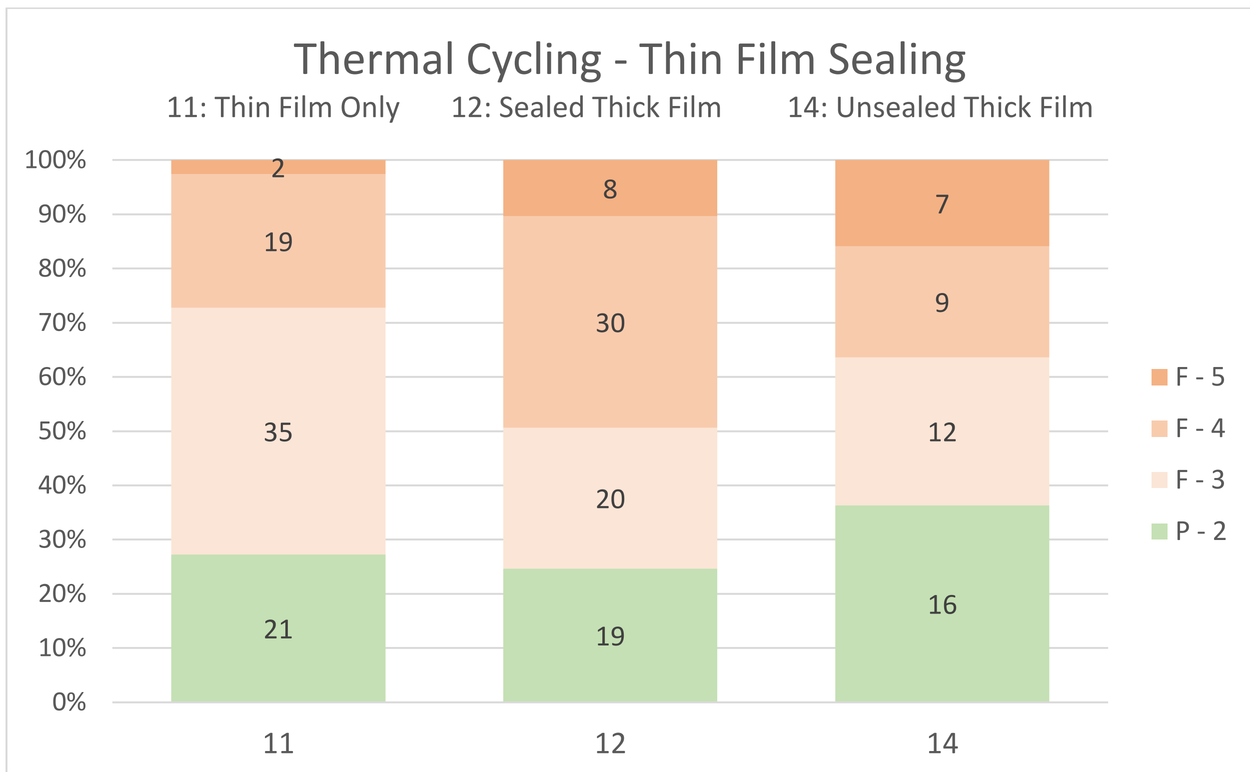

Fig. 5.40. The thermal cycling thin film sealing comparison at 1,000 cycles.

5.3.3 Discussion of Thermal Cycling Results

Thermal cycling was a harsh environmental test, especially when the temperature swing was around or greater than 200 °C. It was observed in the substrate comparison that the 9K7 substrate was overall more reliable. Taking into account the delamination issues that occurred (more frequently on 951), the extreme surface roughness of the 9K7 substrate helped with adhesion, though the thin films were thin enough that the roughness also caused several discontinuities in the thin film stack up. The thick film comparison showed that the pass rate was similar, though it was still more common on Ag to have catastrophic damage over Au. Thin film recipe A (with Ti) proved to be more reliable than recipe B (without Ti) due to the major delamination issues. The thermal vias were not at all reliable during thermal cycling, and the larger the diameter of the via the more dramatic the failure mechanism. It was seen that thin film sealing did not protect the thick film elements to the extent that was anticipated by the hypothesis established for the study.

5.4. Humidity

5.4.1 Test Overview

The humidity test was run in a sealed chamber for 10 days at a temperature of 85 °C and a relative humidity (RH) of 85%. This test is often referred to as the 85/85 test. There were no problems encountered in setting up or running the experiment. A 1 V bias was applied to the triple track features of several coupons. This was done to compare to no bias, especially as Ag tends to grow spikes and dendrites when under a bias. No discernable differences were found between the two groups, and thus no further distinction was made.

5.4.2 Test Results

What follows is a series of images captured after the full 10 day humidity test.

Fig. 5.41 shows a large and deep divot, or crater, along one of the 15 mil vias as a part of 0603 SMD pads, feature group 7. On the left is the full feature, on the right is a close up of the large crater. This was part of the 227 sample, which was 9K7 Ag thick film and a recipe A thin film stack up (0.2Ti/4Cu/2Pt/0.375Au). The humidity seeped into the thin film layers and began eating away at the Cu, as such, the rest of the structures suffered as well. This was ranked a level 5 event. Notice than even though there was a primary crater, there were signs of the thin film being damaged along the edges of the via and in the center of the via.

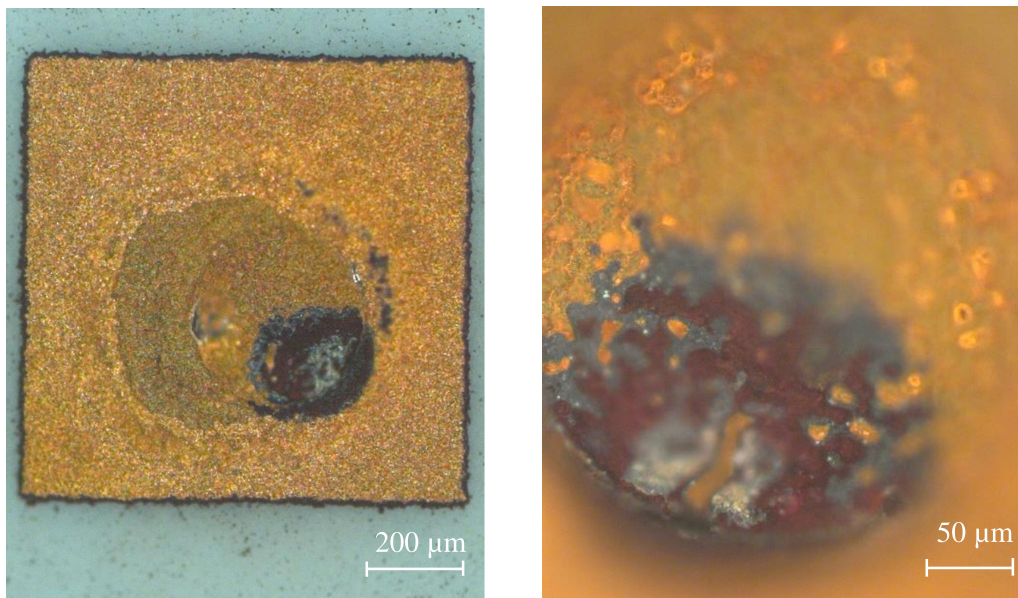

Fig. 5.41. A deep divot on 15 mil. via and 0603 SMD pad on sample 227.

Fig. 5.42 shows misaligned triple track structure from feature group 12, a 951 Ag coupon with thin film recipe A (with Ti) metallization stack up. There were three interesting

observations about this figure. First was the areas where Ag thick film was direct on ceramic were damaged in some way (the black spots and specs). Secondly when the thin film was direct on ceramic there was damage to the edges. Finally, when the thin film was sealing the thick film, both were protected. Thin film sealing in this particular environmental test showed a symbiosis effect when a thin film of this recipe sealed a silver thick film.

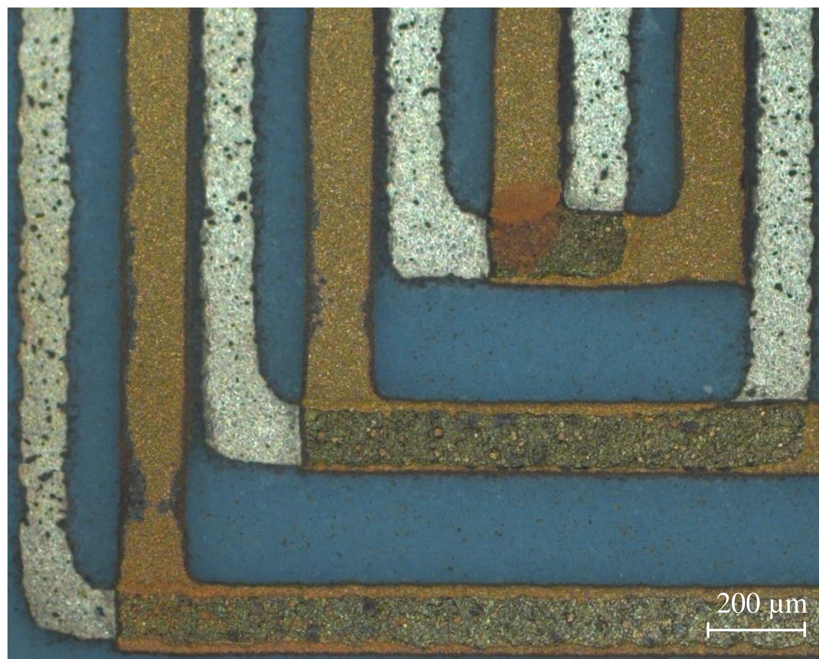

Fig. 5.42. Example of thin film sealing on a triple track structure on sample 127.

Based on the optical microscopy observations and the numbering system, trends could be drawn using the data gathered. What follows is a sampling of the most important, interesting, and pertinent trends from the five levels of damage.

Fig. 5.43 shows a comparison between the DuPont 951 (left) and the DuPont 9K7 (right) substrates across all feature groups and all other material system parameters. The height of the bar corresponds with the percent accumulation and the number indicated the absolute number of features ranked. The 951 had over a 70% pass rate and the 9K7 had just under a 50% pass rate, a difference of over 20% between them. There was also a noticeable separation in the number of level 1 events observed and the number of level 5 events observed between the two substrate materials. This led to the conclusion that the 951 substrate was more reliable under the 85/85 conditions of this test.

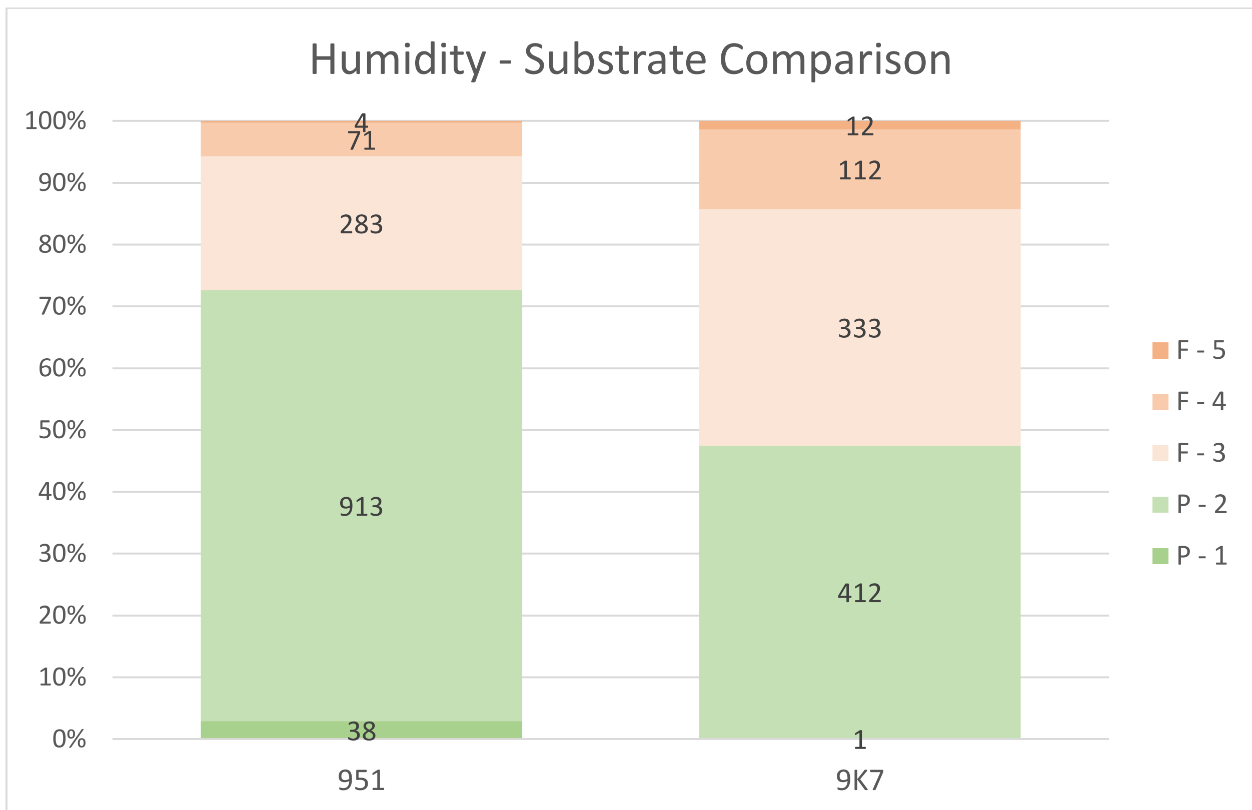

Fig. 5.43. The humidity test substrate comparison.

Fig. 5.44 shows the comparison of the thick film materials across all features and all other material parameters. There was no appreciable difference found between the thick film types under the 85/85 test condition that was not outside the margin for error.

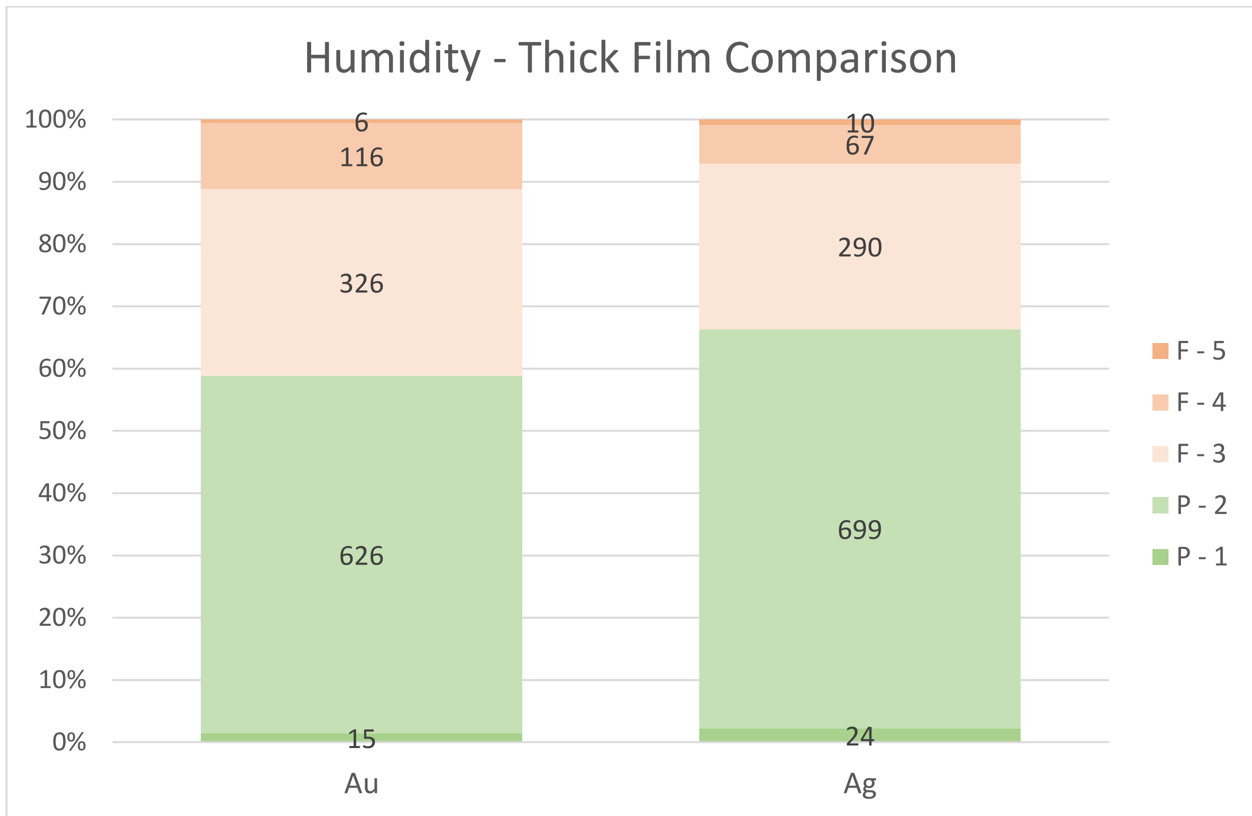

Fig. 5.44. The humidity test thick film comparison.

Fig. 5.45 shows the comparison of the thin film recipes present in this test across all features and all other material parameters. There was no appreciable difference found between the thin film recipes under the 85/85 test condition that was not outside the margin for error.

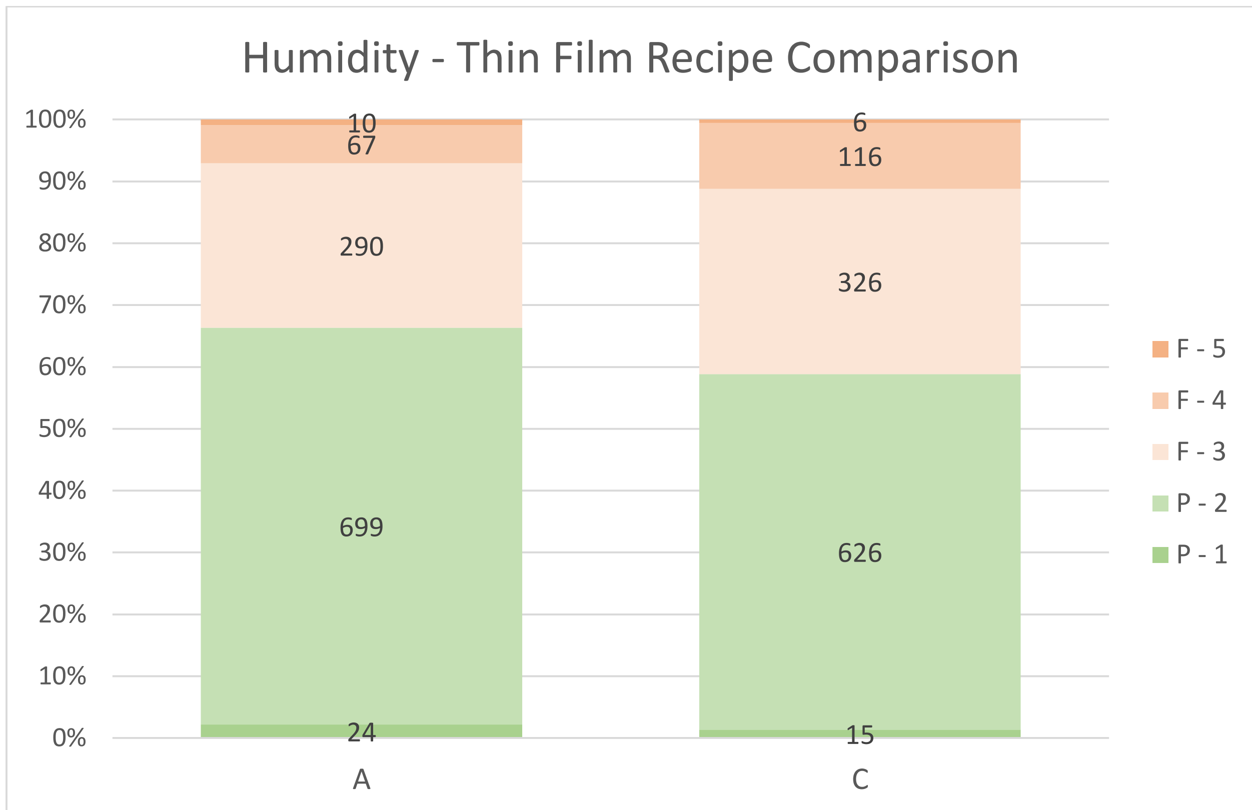

Fig. 5.45. The humidity test thin film comparison.

Fig. 5.46 shows the comparison between the thermal vias by the three via sizes, 10, 20, and 30 mil diameter vias, respectively. Notice that the resolution of the data, dictated by the number of available points, was reduced from the other comparisons. There were only two thermal vias of each size located per coupon. Given the primary source of error was the human perception between level 2 and level 3, the standard error was high in this comparison. Keeping that in mind, there still were appreciable differences in the reliability of the thermal vias that trended with the diameter of the vias. The larger the via was, under the humidity test conditions, the less reliable the thermal via was.

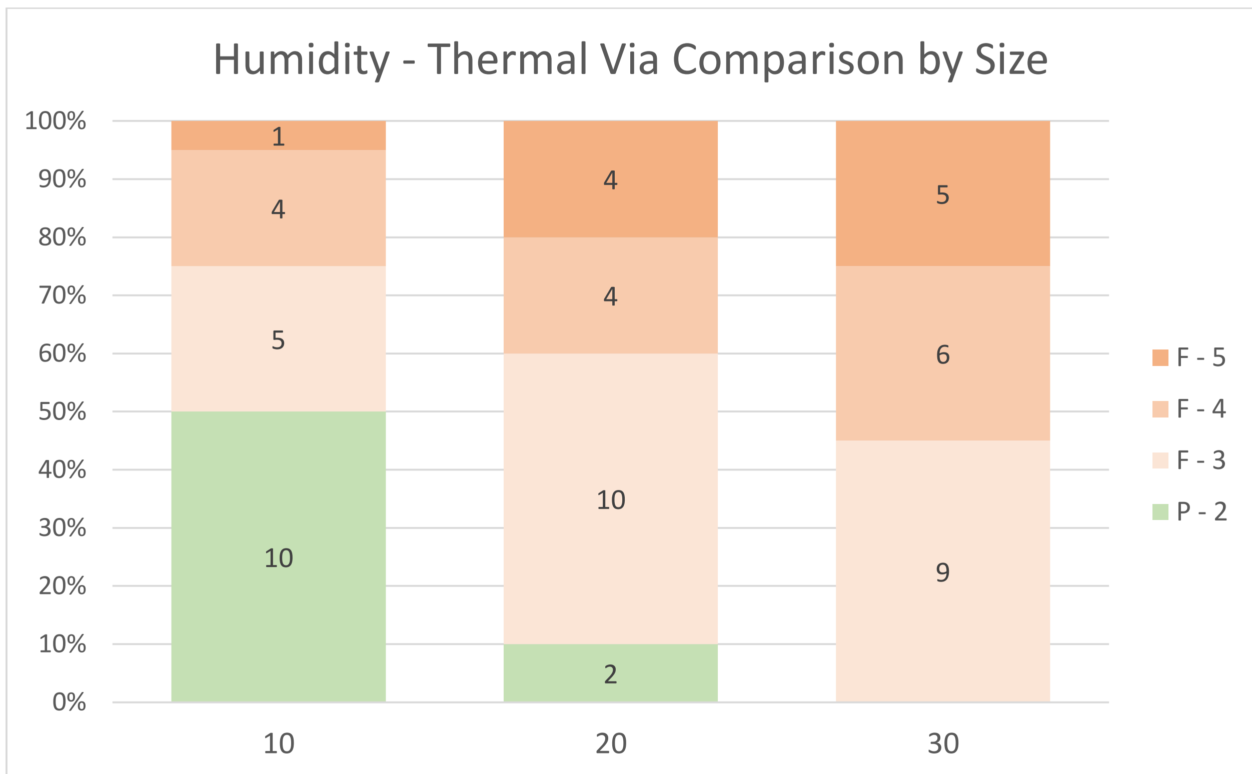

Fig. 5.46. The humidity test thermal via comparison.

Fig. 5.47 compares three feature groups: group 11 which was thin film directly on the LTCC substrate, group 12 which was thin film sealed thick film, and group 14 which was the unsealed and exposed thick film elements. Note the difference in resolution (number of data points per column) of group 14, which was much lower resolution than the other two groups as there were only two data points per coupon for feature group 14. There were two interesting trends to point out. First was that sealing a thick film with a thin film proved less reliable than only having a thin film direct on ceramic, though it was indeed more reliable than leaving thick film exposed and uncovered. Second, it was interesting to note that in group 12, the sealed thick film, had zero level one ratings, whereas the other two comparisons did.

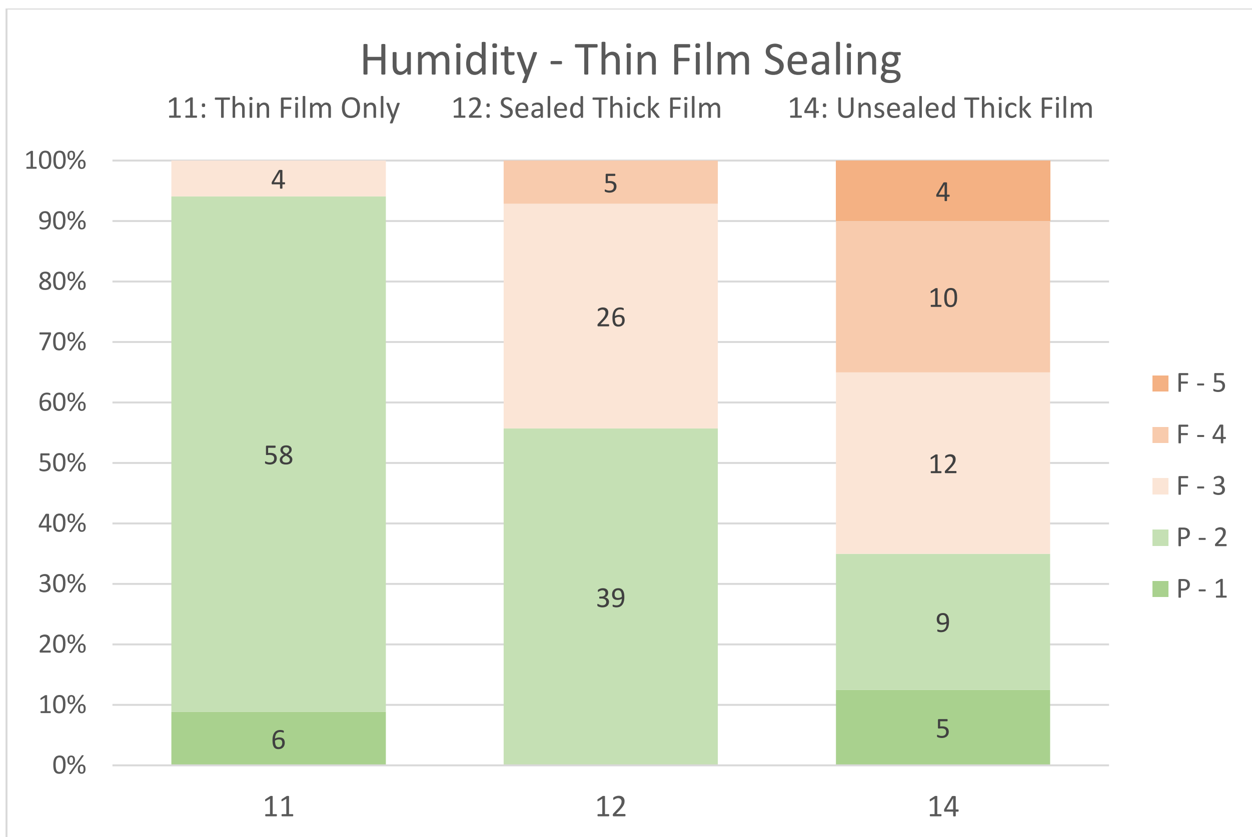

Fig. 5.47. The humidity test thin film sealing comparison.

5.4.3 Discussion of Humidity Results

There are several conclusions that can be drawn from the humidity test data presented. It was shown that the 9K7 substrate was less reliable than the 951 substrate. It was demonstrated that neither the thick film metallization nor the thin film recipes present were more or less reliable than the other. The reliability of thermal vias degrades proportionately with the diameter of the via. The thin film sealing did improve the reliability of the thick film features. The final result mentioned was an interesting one, as there were no level 1s reported in the data for just the sealed thick film in group 12, whereas the number of 1s present in groups 11 and 14 were about equal. It was observed that the sealing aspect made the thin film more susceptible to admitting humidity through it. This caused the humidity to eat away at the Cu or Ag layers in the thin film, thus compromising the rest of the feature.

5.5. Thermal Shock

5.5.1 Test Overview

Thermal shock was performed in a Tabai TSB-1L liquid bath chamber and samples were exposed to temperatures from +125 °C on the high end down to -55 °C on the low end for a total 25 cycles. A dwell time of 10 minutes in each extreme, with a measured 50 second transfer time between the temperature baths. The same Galden fluid was used for both the high and low temperature baths. Samples were checked after every five cycles to make sure no complications had arisen nor any samples destroyed. There were no complications in the setting up or execution of this test.

5.5.2 Test Results

What follows is a series of images captured after all 25 thermal shock cycles.

Fig. 5.48 shows both of the Ag thick film baseline elements, after the thermal shock test. The Ag had oxidized considerable on both, and had taken material away from the pad.

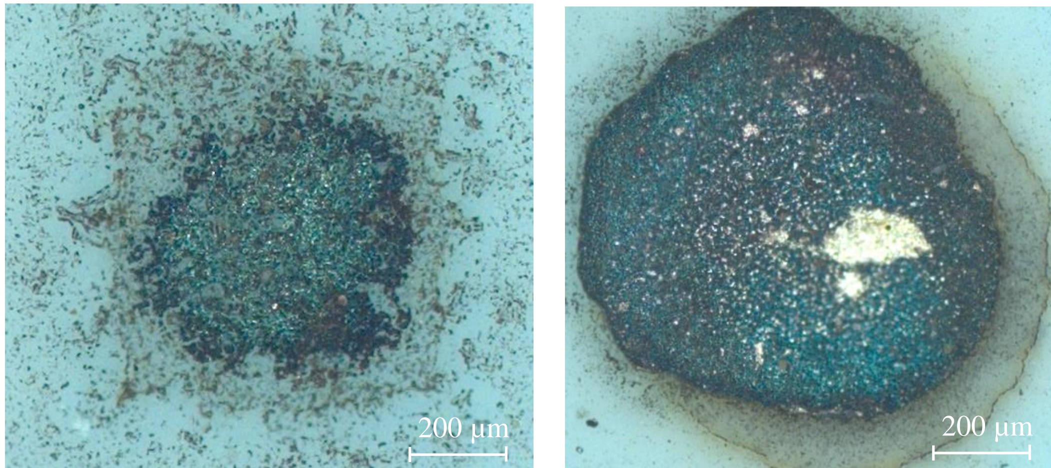

Fig. 5.48. Thick film baseline elements after the thermal shock on sample 230.

Fig. 5.49 shows a number of failure mechanisms on a single feature, in this case a 20 mil diameter thermal via. Notice the divots and cratering all over the place; it was not just restricted to near the sidewalls in this test. Notice the grey deformations of the thin film build up.

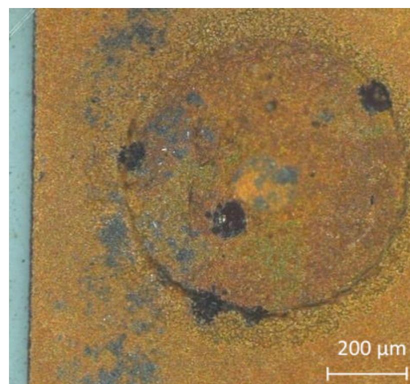

Fig. 5.49. Example of divots and cratering on a 20 mil. thermal via on sample 317.

Fig. 5.50 shows that exposed thick film disintegrates when unsealed on a 951 Ag coupon in the conditions of thermal shock by liquid bath. The thin film and the sealed thick film were unaffected, but when thick film Ag was exposed to the elements, it washed away.

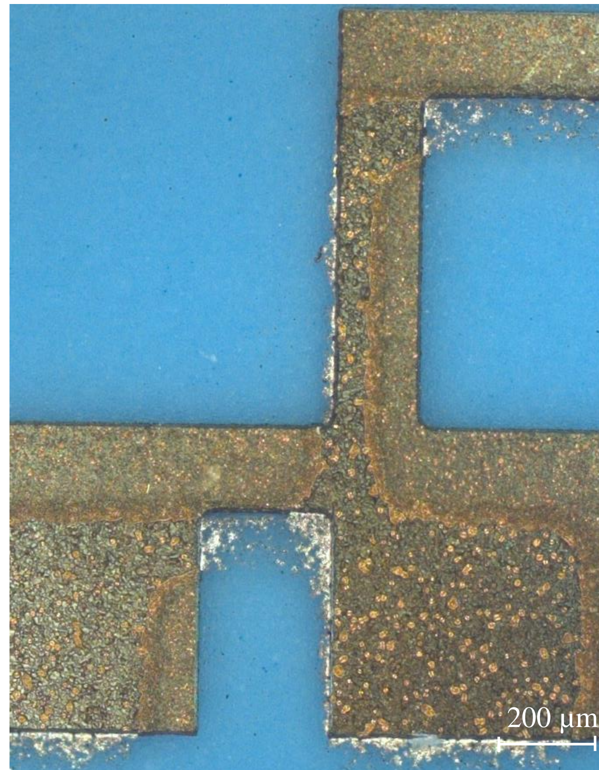

Fig. 5.50. Thin film sealing on a triple track feature from sample 128.

Fig. 5.51 shows a portion of thin film that began to migrate outward from the central pad, taking the other stacked thin films with it. There was also a small divot around the sidewall of the via. Though a different feature, Fig. 5.52 shows via sidewall separation.

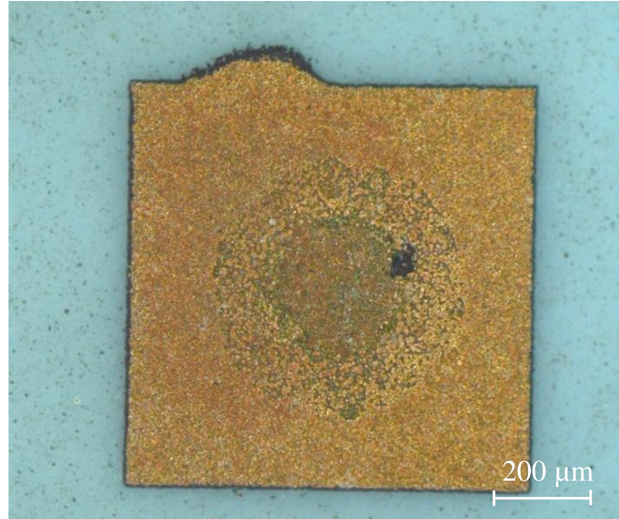

Fig. 5.51. Thin film migration and budging on group 5 feature from sample 317.

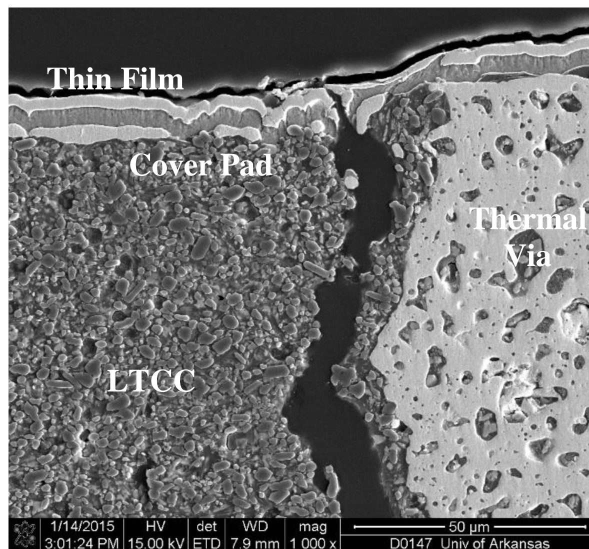

Fig. 5.52. A thermal via separated from the LTCC sidewall.

Based on the optical microscopy observations and the numbering system, trends could be drawn using the data gathered. What follows is a sampling of the most important, interesting, and pertinent trends from the five levels of damage.

Fig. 5.53 shows a comparison between the DuPont 951 (left) and the DuPont 9K7 (right) substrates across all feature groups and all other material system parameters. The height of the bar corresponds with the percent accumulation and the number indicated the absolute number of features ranked. The features on the 951 substrate had a 55% pass rate, whereas those on the 9K7 substrate had a 40% pass rate. While this was notable, there were no other conclusions that could be drawn due to the amount of standard error.

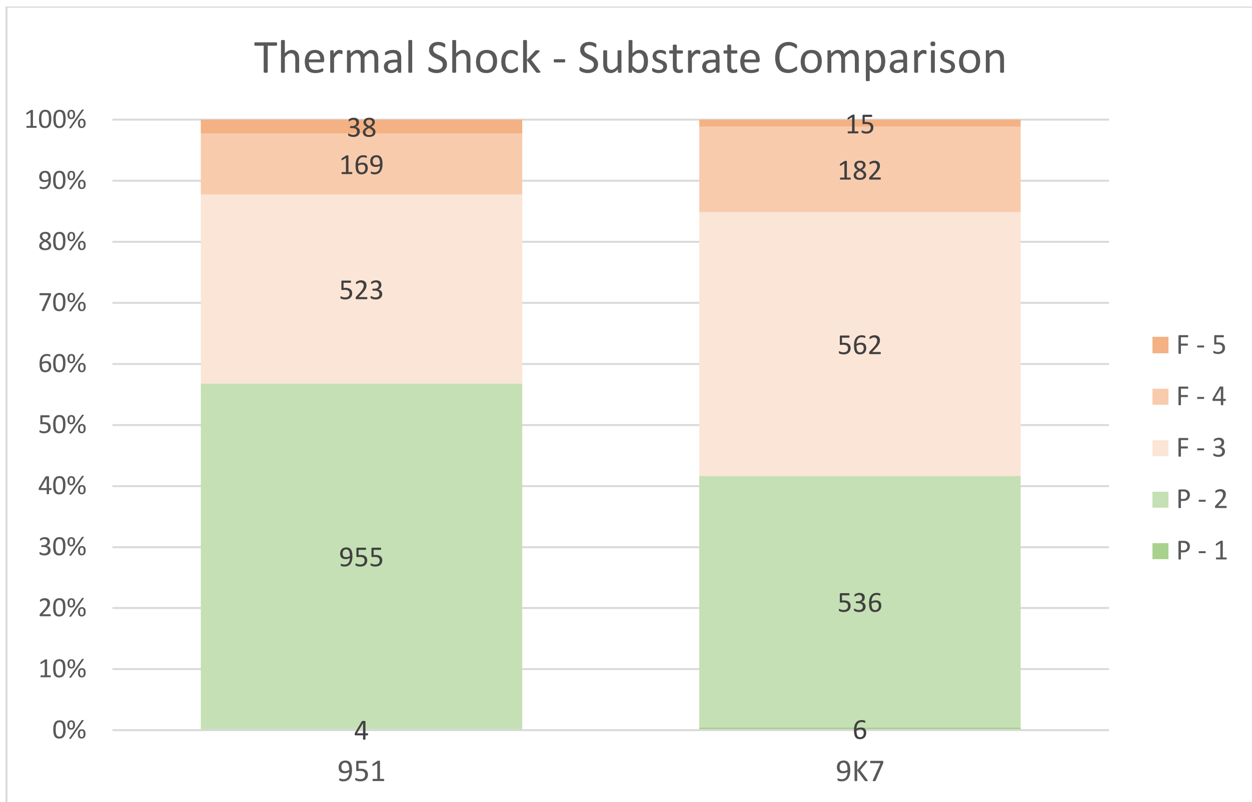

Fig. 5.53. The thermal shock substrate comparison.

Fig. 5.54 shows a comparison between all the features based either on the Au or Ag thick film material systems. The features using the Au thick film had a 60% pass rate, whereas those using the Ag thick film had a 44% pass rate, making the Ag thick film 16 percentage points less reliable than features utilizing the Au thick film. While this was notable, there were no other conclusions that could be drawn due to the amount of standard error.

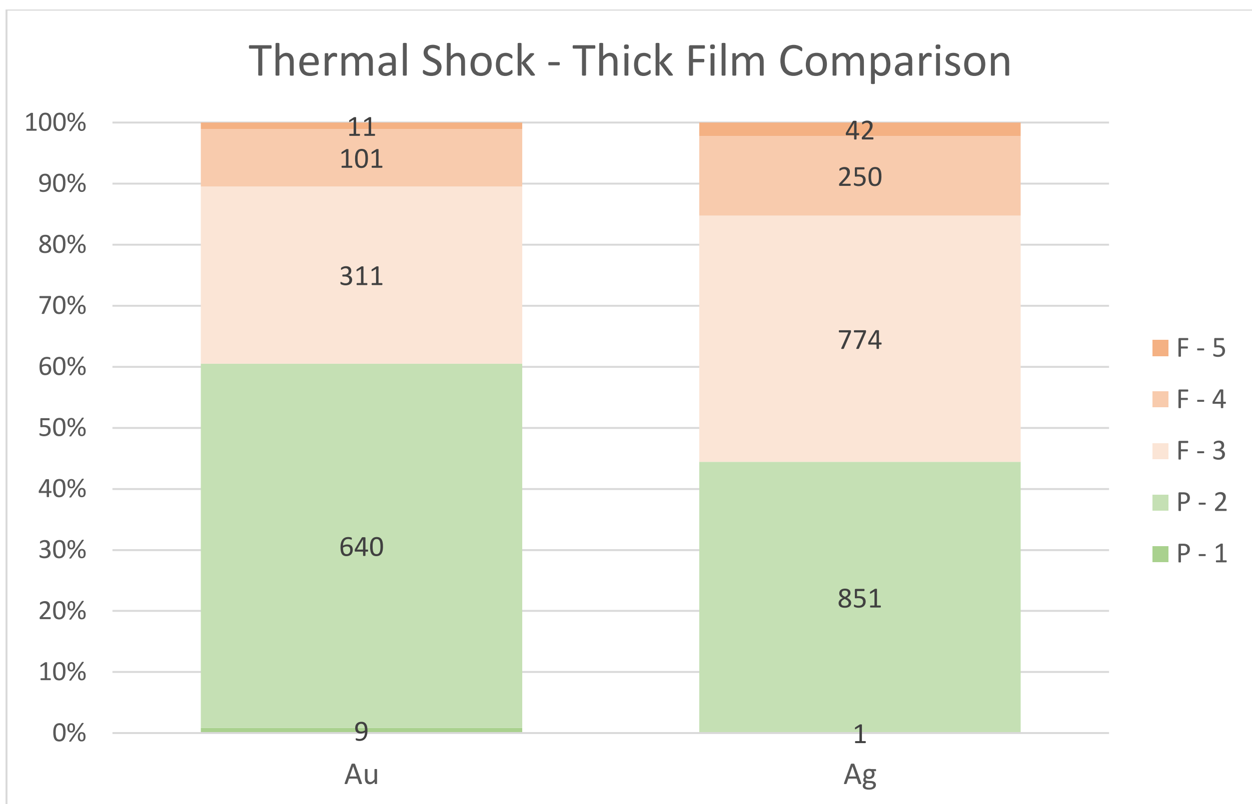

Fig. 5.54. The thermal shock thick film comparison.

Fig. 5.55 shows a comparison between the thin film recipes that were present during the thermal shock test. Thin film recipe B (without Ti) was the most reliable, by 23 percentage points compared to the next most reliable, recipe A. Recipes A and B were both more reliable that either recipes C (replaced Cu with Ag) or D (thinner Cu) under the thermal shock conditions. It was interesting to note that there were exceptionally few features that were ranked as either a level 1 or a level 5. Even taking into account a generous margin for the sources of error introduced into the data, the reliability of thin film recipe B over thin film recipe A was appreciable.

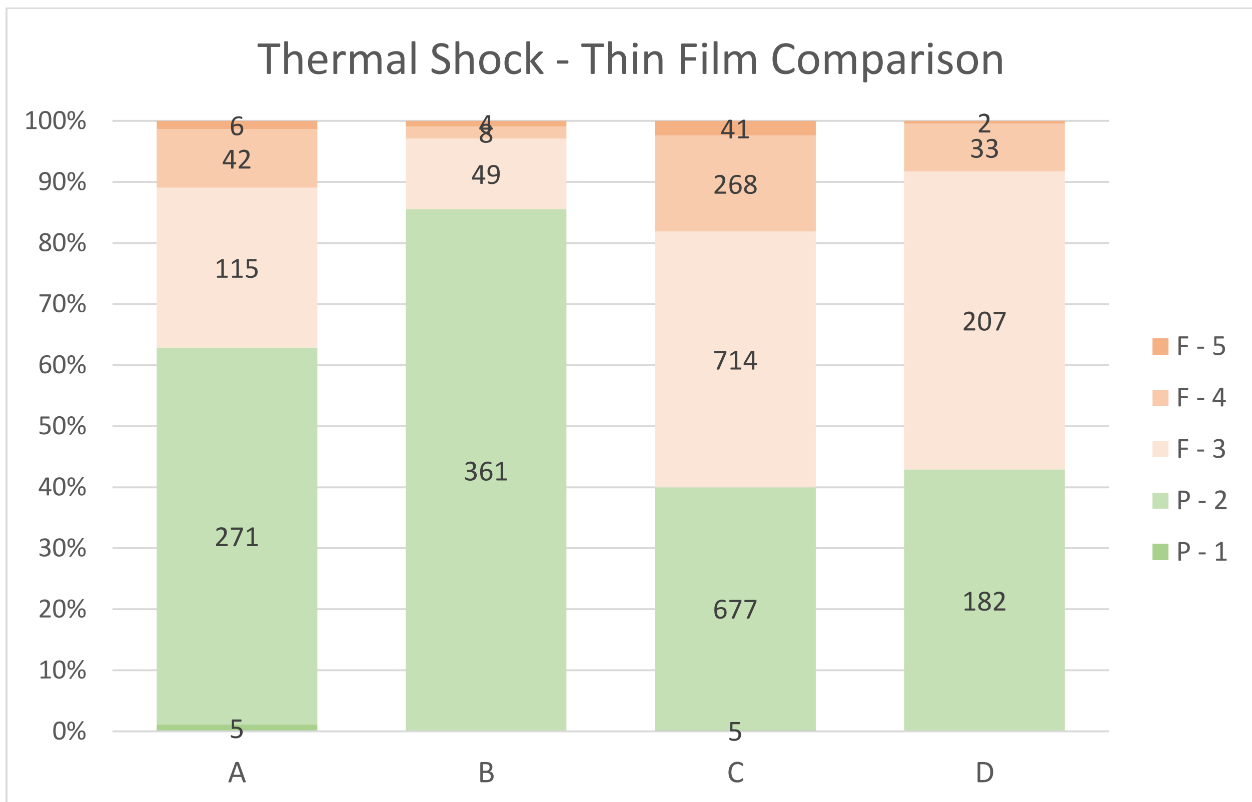

Fig. 5.55. The thermal shock thin film comparison.

Fig. 5.56 shows the comparison between the thermal vias by the three via sizes, 10, 20, and 30 mil diameter vias, respectively. Notice that the resolution of the data, dictated by the number of available points, was reduced from the other comparisons. There were only two thermal vias of each size located per coupon. Given the primary source of error was the human perception between level 2 and level 3, the standard error was high in this comparison. It was shown that the smallest size vias not only had the highest pass rate, but also the least amount of critical or catastrophic failure mechanisms; whereas, the largest vias had the most critical or catastrophic failures. The 20 mil vias were in between those two extremes. Though it was interesting to note that the 20 mil vias did not have a single ranking of level two, meaning 100% of them failed.

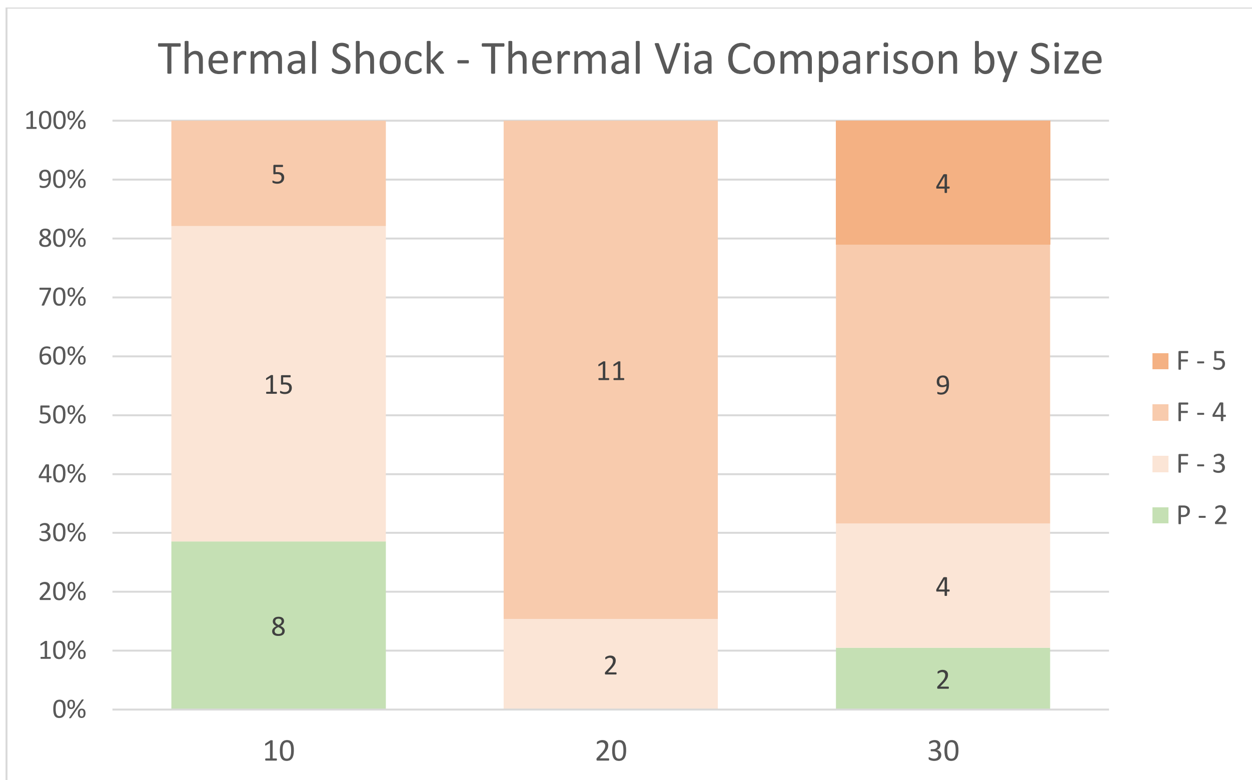

Fig. 5.56. The thermal shock thermal via comparison.

Fig. 5.57 compares three feature groups: group 11 which was thin film directly on the LTCC substrate, group 12 which was thin film sealed thick film, and group 14 which was the unsealed and exposed thick film elements. Note the difference in resolution (number of data points per column) of group 14, which was much lower resolution than the other two groups as there were only two data points per coupon for feature group 14. There were two interesting trends to point out. First was that sealing a thick film with a thin film proved less reliable than only having a thin film direct on ceramic, though it was indeed more reliable than leaving thick film exposed and uncovered. Second, it was interesting to note that both group 11 and group 12 had zero level 1 ratings, whereas group 14, the unsealed and exposed thick film, had three.

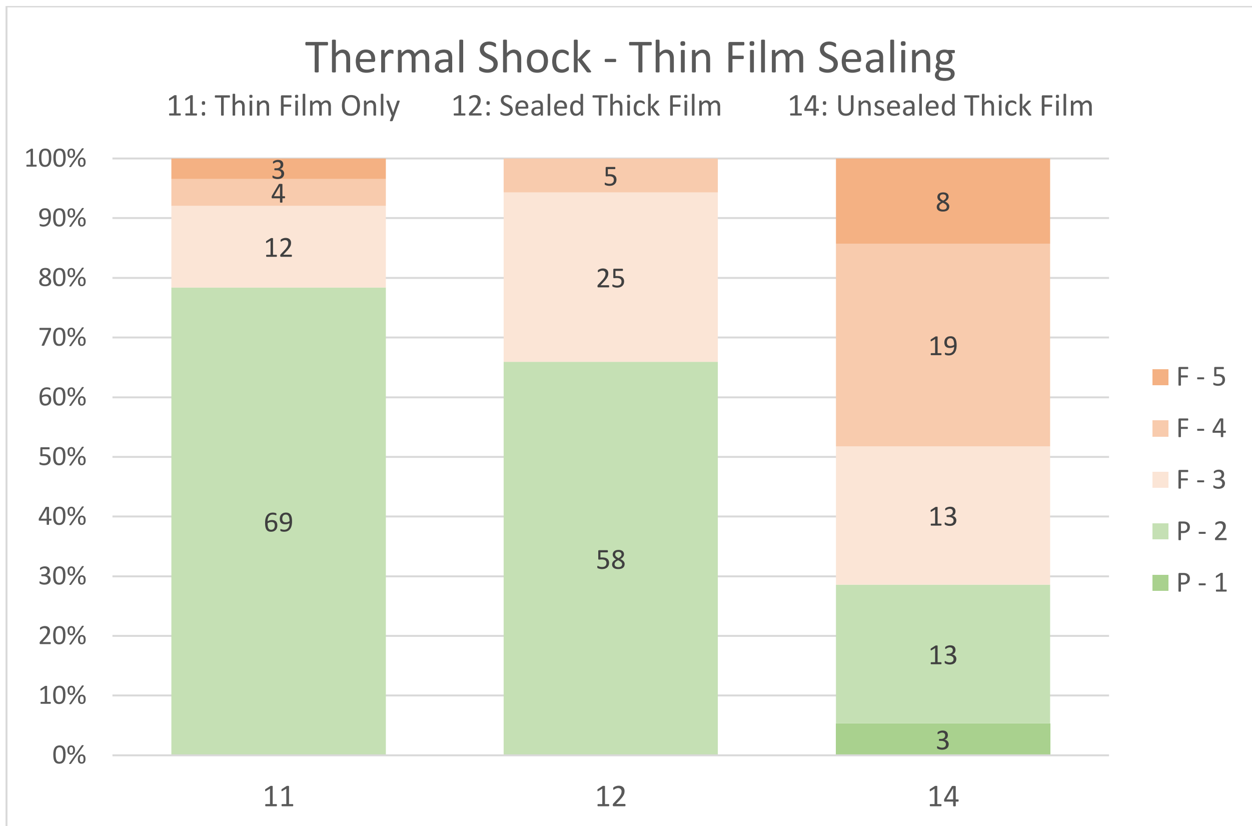

Fig. 5.57. The thermal shock thin film sealing comparison.

5.5.3 Discussion of Thermal Shock Results

Reviewing what was discovered in the results for the thermal shock test, there were several conclusion that could be made. First, both the 951 substrate and the Au thick film metallization we more reliable than their counterparts, 9K7 substrate and Ag thick film metallization, respectively, albeit only slightly. Second, the two thin film recipes with 4 µm thick Cu in the stack up were more reliable than the two recipes that did not. The reliability of thermal vias correlated with the size of the via. Finally, sealing thick film with a thin film did indeed increase the reliability of the thick film features.

5.6. Corrosion

5.6.1 Test Overview

The corrosion test was performed in an industry standard and certified salt fog spray chamber and was run for 10 days at 35 °C with a 5% NaCl salt fog sprayed from an atomizing nozzle. The test ran without issue for the full 10 days.

5.6.2 Test Results

The following is a series of images taken after the full 10 days of the test were finished.

Fig. 5.58 shows a sample of the corrosion that occurred on feature group 2 0603 SMD pad without a via. The sample was on a 9K7 substrate with Ag thick film and thin film recipe A. This sample received a damage level ranking of 5. Notice the stark color change from the gold color on the left to the brow or bronze color on the left. There were portions of the pad that developed a teal color as well.

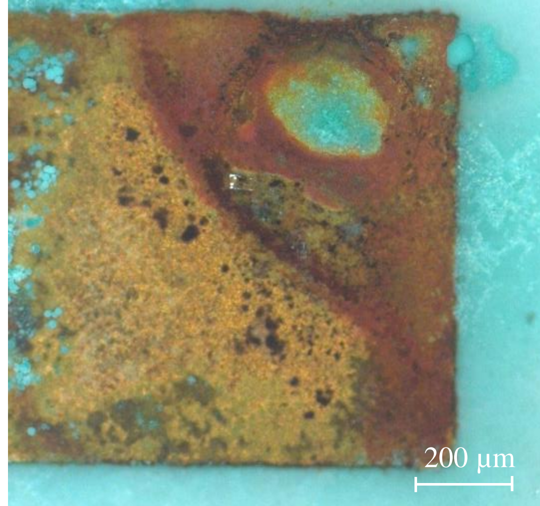

Fig. 5.58. Corrosion observed on a thin film pad from sample 227.

Fig. 5.59 shows cratering and large divots around a 30 mil thermal via. There was some reddening of the surface, primarily located around the via or pad edge. There was also a shift to teal coloring across the entire feature as well. This feature received a damage level rank of 5.

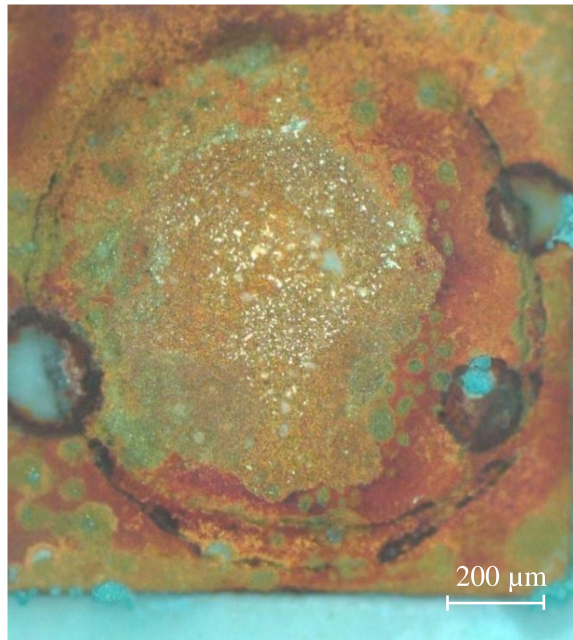

Fig. 5.59. Corrosion, divots, and cratering around a 30 mil thermal via on sample 227.

Fig. 5.60 shows corrosion across the triple track feature of a 9K7 Ag coupon with thin film recipe A. There was evidence of corrosion across the entire width of the feature, accompanied by some material migration. There was a mixture of reds and teals, indicating there were multiple types of metal corroding. If the Cu layer could be reached by any of the salt, then it corroded.

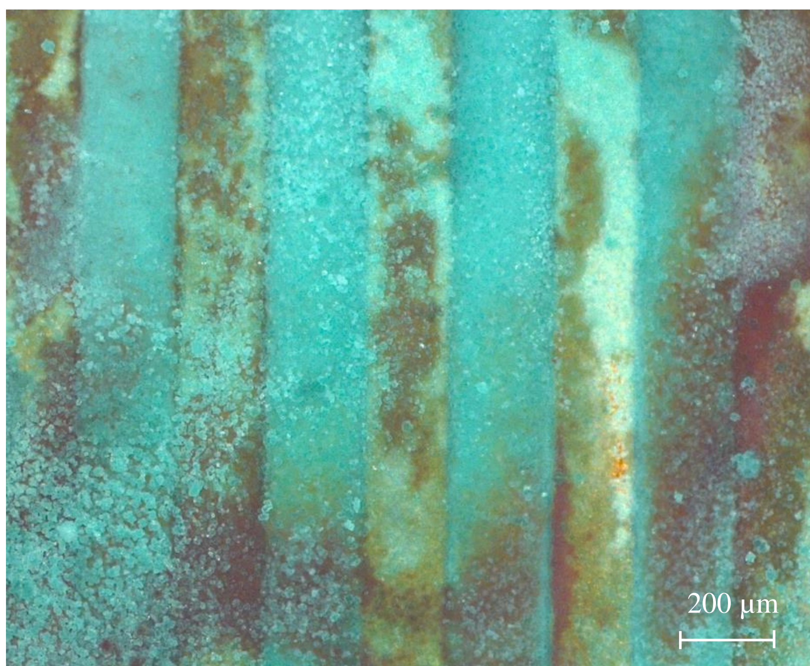

Fig. 5.60. Corrosion across a triple track feature from sample 227.

Fig. 5.61 shows an entire 97 Au coupon after coming out of the corrosion test in the salt fog atmosphere chamber. Nearly every feature on this coupon received either a level 4 or level 5 rating for damage. Portions of the different features or layers of metallization were completely washed away. The corners and edges were the most effected parts of features. Even though the

top layer was Au, the edges and sides where any of the other metals could be effectively reached by the salt solution enabled the corrosion to enter the feature and wreak havoc.

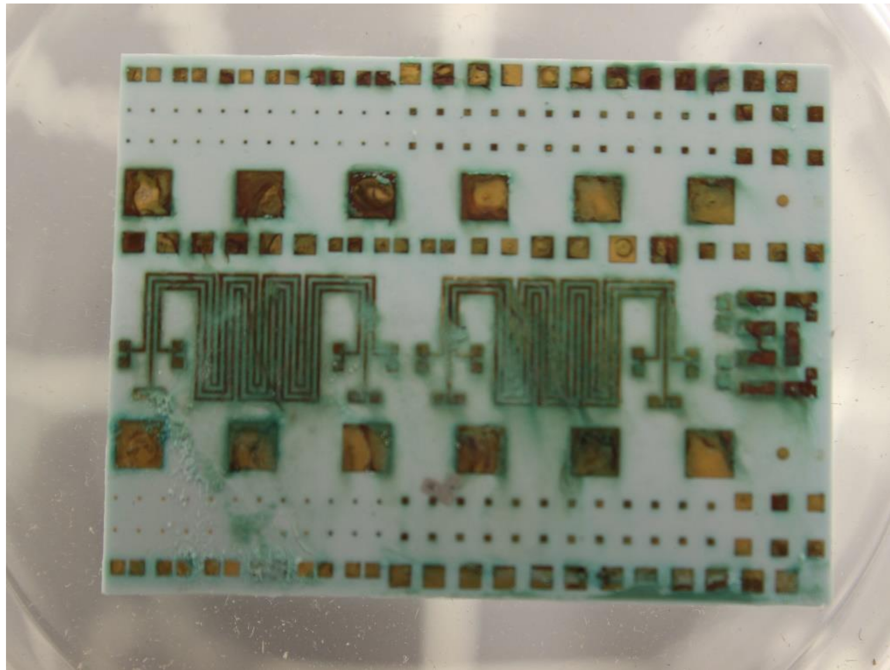

Fig. 5.61. Picture of entire Coupon 1 after the corrosion test.

Based on the optical microscopy observations and the numbering system, trends could be drawn using the data gathered. What follows is a sampling of the most important, interesting, and pertinent trends from the five levels of damage.

Fig. 5.62 shows a comparison between the DuPont 951 (left) and the DuPont 9K7 (right) substrates across all feature groups and all other material system parameters. The height of the bar corresponds with the percent accumulation. The numbers on the bar graph indicate the absolute number of features ranked which give a resolution of the data. It was observed from comparing the substrates in the corrosion test that there was a difference of about 10% in the pass rates between them, with the 9K7 substrate being extremely low at around only a 2% pass rate. The 9K7 substrate also had a much higher rate of major and catastrophic failures. The likelihood a 9K7 would have a major or catastrophic failure was 40% higher than when using the 951 substrate material.

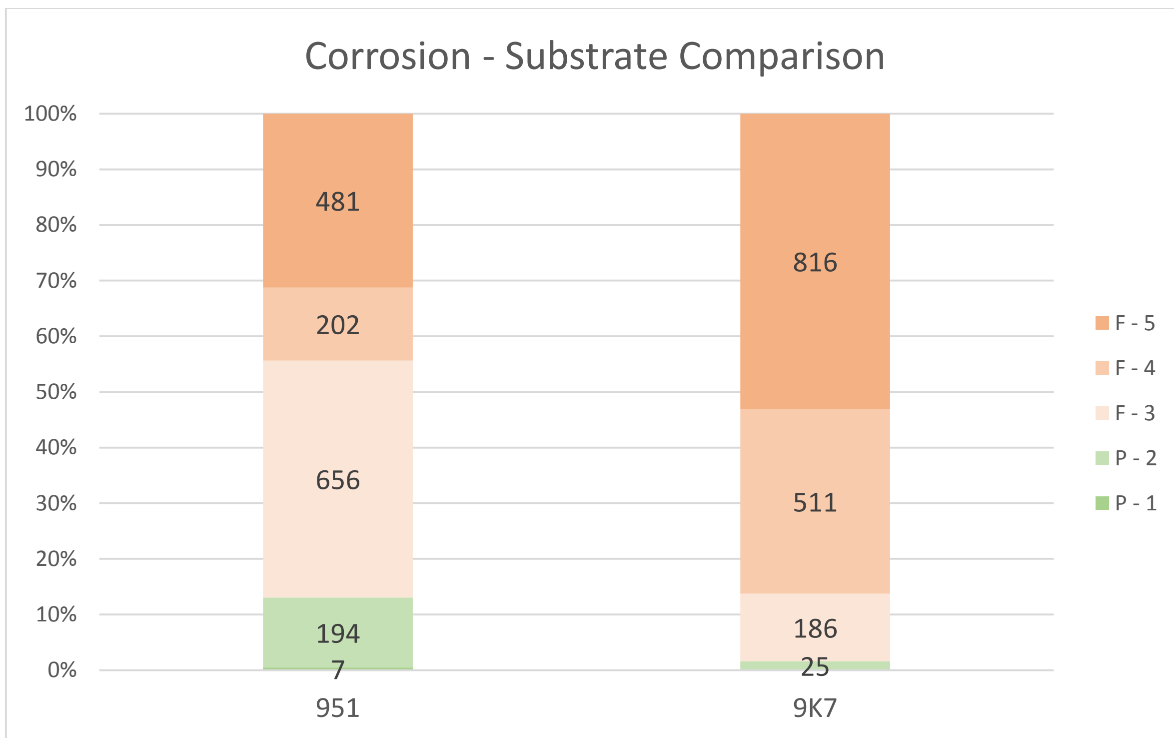

Fig. 5.62. The corrosion test substrate comparison.

Fig. 5.63 shows a comparison between the two thick film metallization materials after the corrosion test. Two trends could be drawn from the data observed. First, neither Au nor Ag had a high pass rate, both being less than 10%. Accounting for the greatest source of error which was the human perception to continually distinguish between a level 2 and level 3 ranking, there was no distinction between the pass rates of the two materials. Second, the Au thick film metallization material had a 15% higher occurrence of catastrophic failures, which gave an advantage to using Ag in this particular test. This was an unexpected observation for the corrosion test. A comparison between the thick film sealing aspect of the feature gave further insight into these observations.

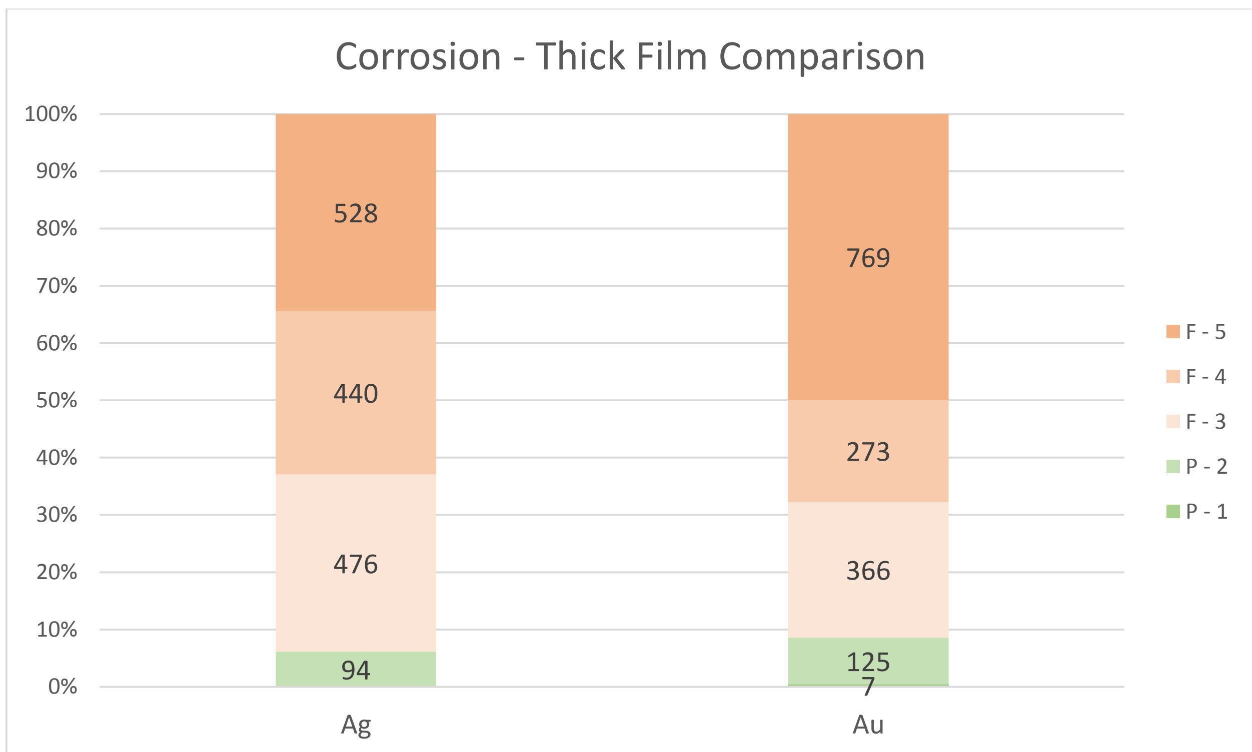

Fig. 5.63. The corrosion test thick film metallization comparison.

Fig. 5.64 shows a comparison of the thin film metallization recipes present in this specific test. It was first observed that none of the three recipes present had an absolute pass rate above 10%. The second observation was rather unexpected; recipe C (0.2Ti/4Ag/2Pt/0.375Au) was the most reliable in terms of both pass rate and major/catastrophic failures. Drawing from those two observations it was concluded that the thin film recipes with Cu were more susceptible to a highly corrosive environment that those which had Ag.

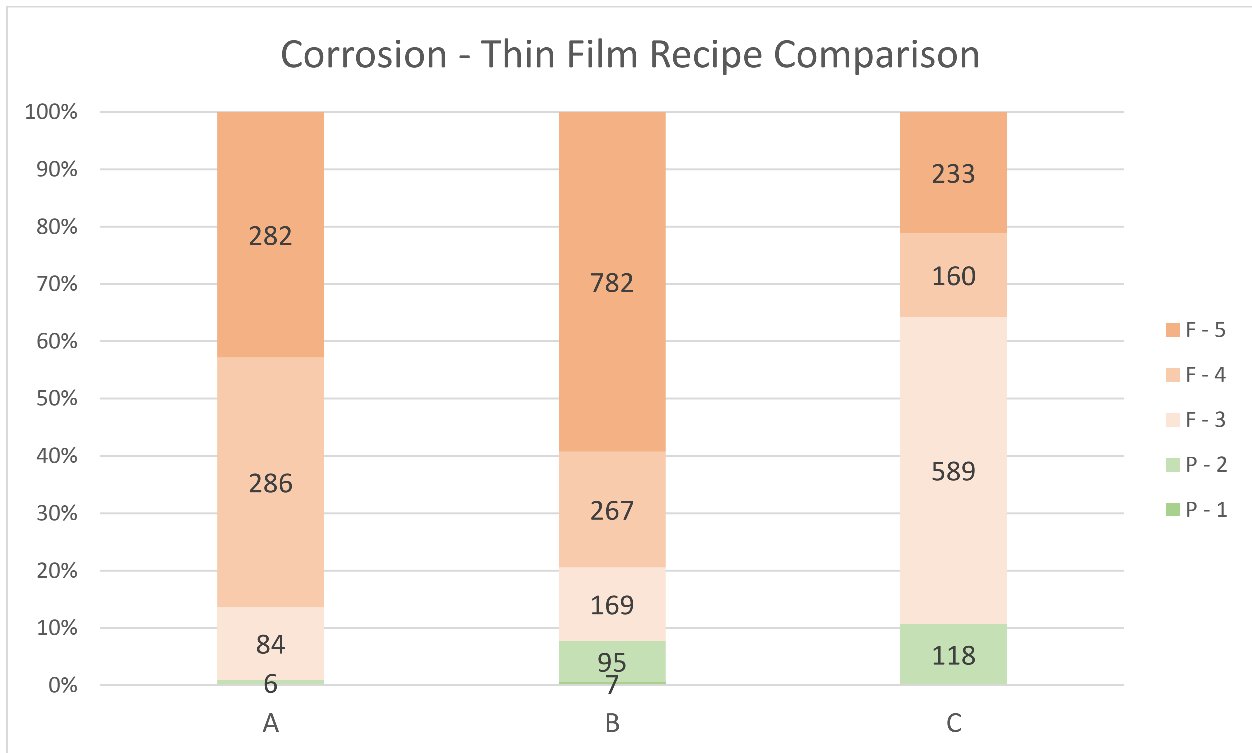

Fig. 5.64. The corrosion test thin film recipe comparison.

Fig. 5.65 shows a comparison between the thermal vias after the corrosion test. It was observed that thermal vias of any of the three sizes represented withstood the corrosive environment with all having a pass rate of less than 5%. Given the low resolution of this data and what was observed there were no other meaningful trends that could be drawn from this graph.

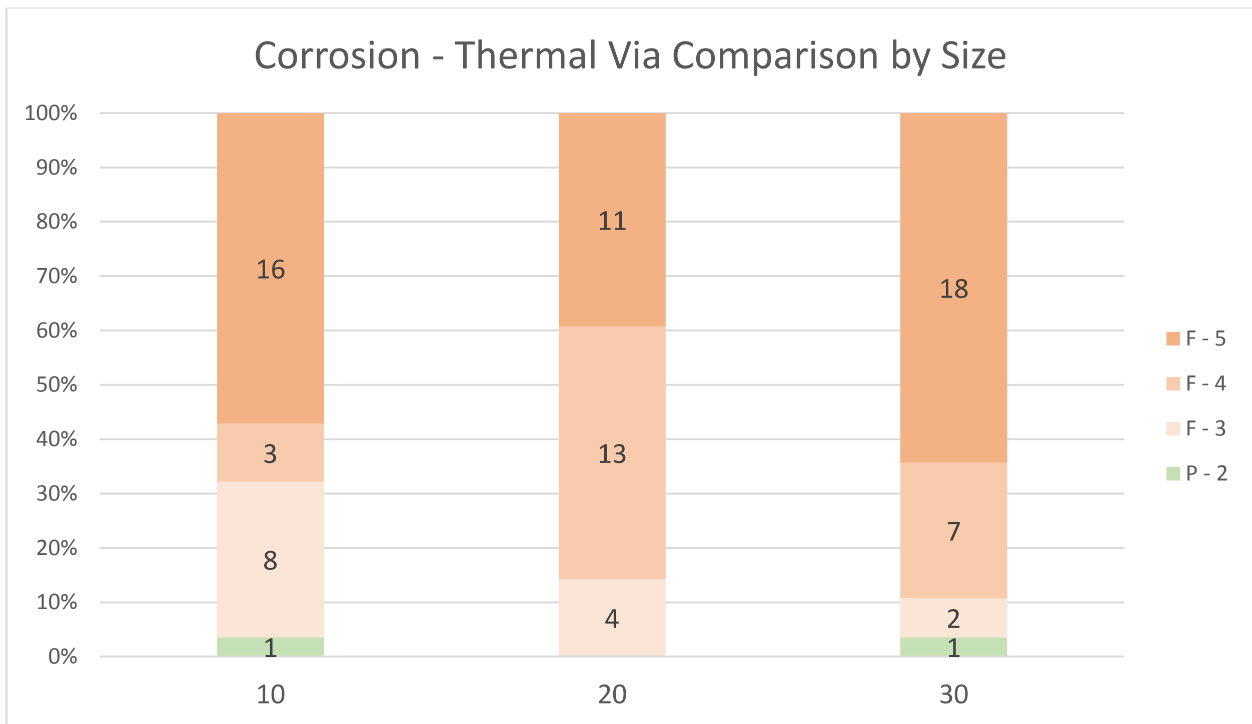

Fig. 5.65. The corrosion test thermal via comparison.

Fig. 5.66 compares three feature groups: group 11 which was thin film directly on the LTCC substrate, group 12 which was thin film sealed thick film, and group 14 which was the unsealed and exposed thick film elements. Note the difference in resolution (number of data points per column) of group 14, which was much lower resolution than the other two groups as there were only two data points per coupon for feature group 14. It was observed in the corrosion test that the thick film features had >15 percentage points better pass rate than either the thin film direct on LTCC or the thin film sealing of a thick film. This was an unexpected observation. As also seen in thin film comparison from Fig. 5.64 and the thick film comparison from Fig. 5.63, the Cu layers in the thin film metallization stack ups were causing more failures than either the Ag thin films or the Ag thick films.

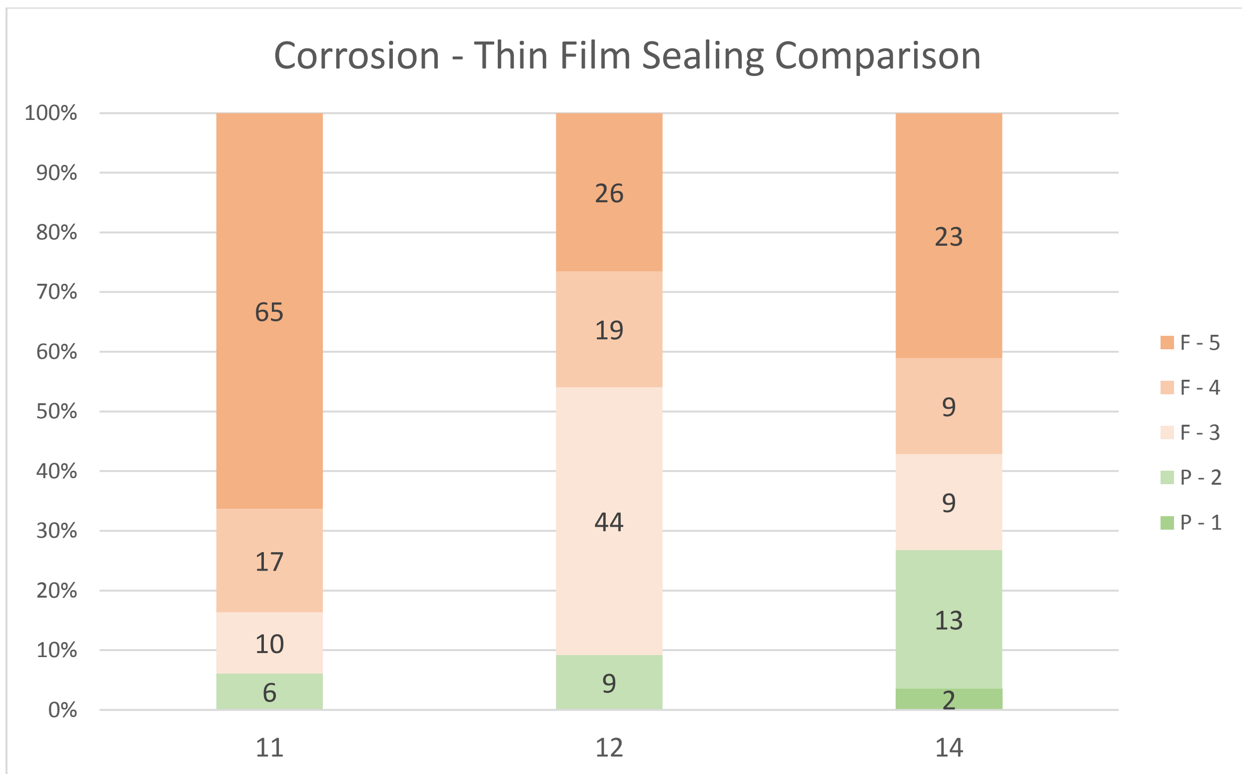

Fig. 5.66. The corrosion test thin film sealing comparison.

5.6.3 Discussion of Corrosion Results

The corrosion test in the salt fog chamber was a high impact test where very few features escaped unscathed. It was surprising though to observe the Ag metallizations, both thick and thin films, were more reliable than the features with either the Au thick films or with Cu used in the thin film metallization stack up recipes. Further, the corrosion test illustrates that these LTCC coupons are not designed to operate in areas that would be highly susceptible to corrosion, such as a marine or navel application.

5.7 Discussion of General Results

This section is devoted to showing the data gathered using the numbering system and optical microscopy and some unique trends throughout the entire set of data across all tests. This information was valuable as it gave a picture of how those processes and materials would react in use case scenarios which encounter multiple of these environmental conditions either simultaneously or across the lifespan of the component. This section contains a series of six comparisons. The first one shows comparison of each test by sealed and unsealed thick film. The second shows a substrate comparison by sealed and unsealed thick film. The third shows a thick film material comparison by sealed and unsealed features. The fourth, fifth, and sixth graphs show the a comparison of the different thin film recipes as compared to recipe A as the standard (e.g. recipe A compared to B, recipe A compared to C, and recipe A compared to D).

Fig. 5.67 shows a comparison between all five environmental tests by the thick film being sealed, feature group 12, or unsealed, feature group 14. Thin film sealing of thick film did make the features much more reliable in the environmental conditions of the thermal shock test, yielding a 35 percentage point improvement. Thin film sealing of thick film did make the features somewhat more reliable in the environmental conditions of the humidity and lifetime at elevated temperature tests, yielding a 20 and 15 percentage points improvement versus unsealed thick film, respectively. Thin film sealing of thick film did not make the features more reliable in the environmental conditions of the thermal cycling and the corrosion tests, yielding a detriment of 10 and 20 percentage points, respectively.

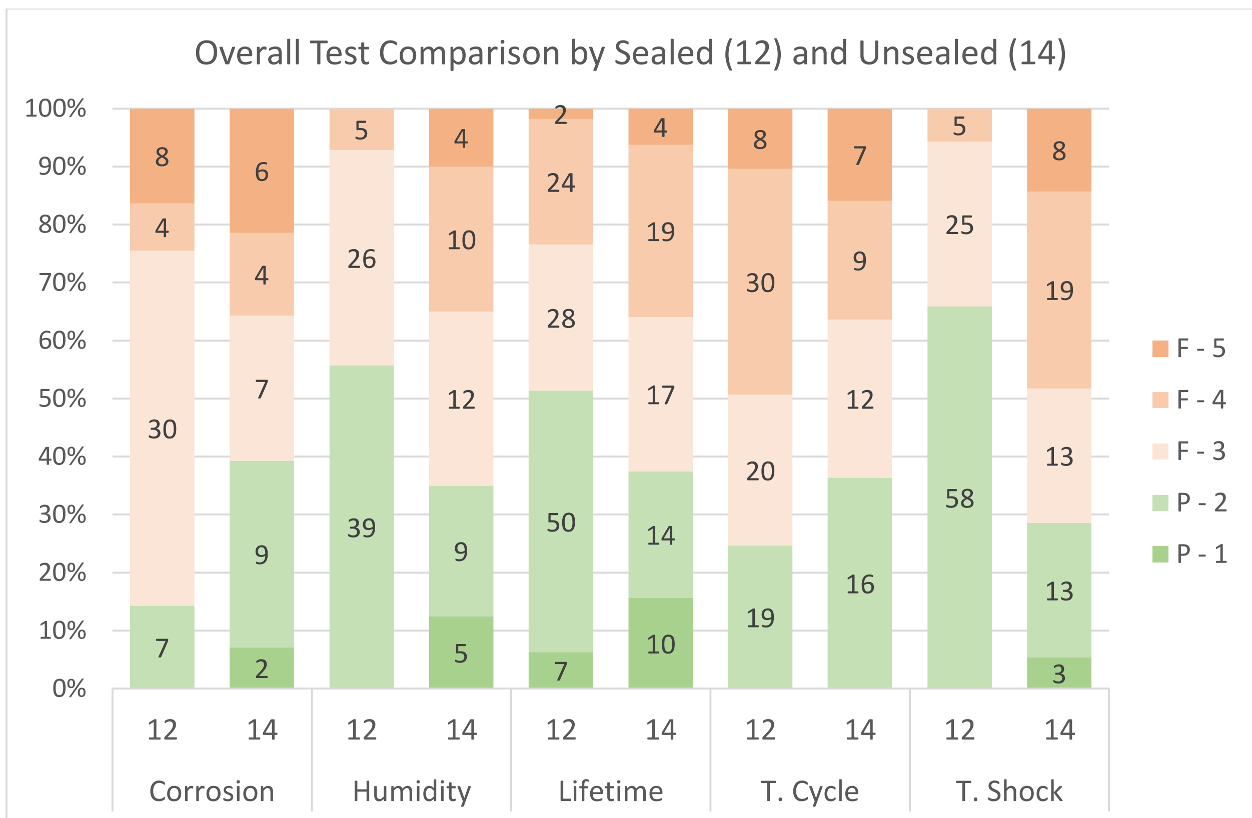

Fig. 5.67. Overall test comparison by sealed and unsealed thin film.

Fig. 5.68 shows a comparison between the two types of substrate materials, 951 being the two columns on the left and 9K7 being the two columns on the right, by thin film sealed thick film versus unsealed thick film. The pass rate for both the sealed and unsealed features on the 951 substrate were about even hovering right at 50%, though the unsealed thick film had a greater number of level 1 rankings (features that remained pristine) and a greater number of features that where catastrophically damaged. The sealed thick film was not as sporadic, but rather had a more predictable behavior. The 9K7 substrate was not as reliable for either the sealed nor unsealed features, however, there was an appreciable increase in reliability when a thin film was sealing thick film rather than thick film remaining exposed.

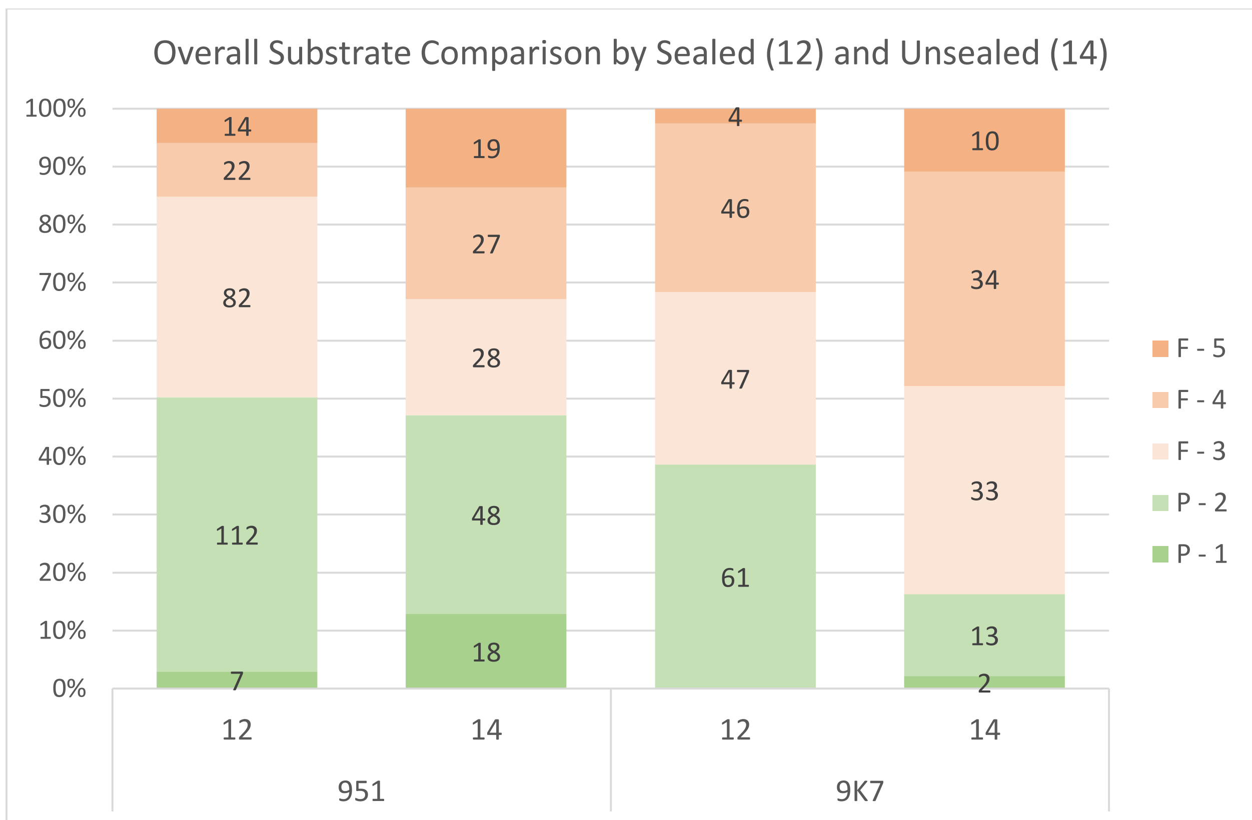

Fig. 5.68. Overall substrate comparison by sealed and unsealed thick film.

Fig. 5.69 shows a comparison between the two type of thick film metallizations, Au being the two columns on the left and Ag being the two columns on the right, and by thin film sealed thick film versus unsealed and exposed thick film. The first thing to notice was that sealing a thick film silver with a thin film build up increased the reliability by three times! However, the overall pass rate for the sealed Ag thick film was less than 50%. On the Au side, it was observed that sealing a thick film actually decreased the features overall reliability by just over 10 percentage points. It was shown that even though the thin film sealing idea did work in certain environments, the process introduced other challenges and obstacles of its own, such has leaving exposed copper on the sidewalls of the thin film build up.

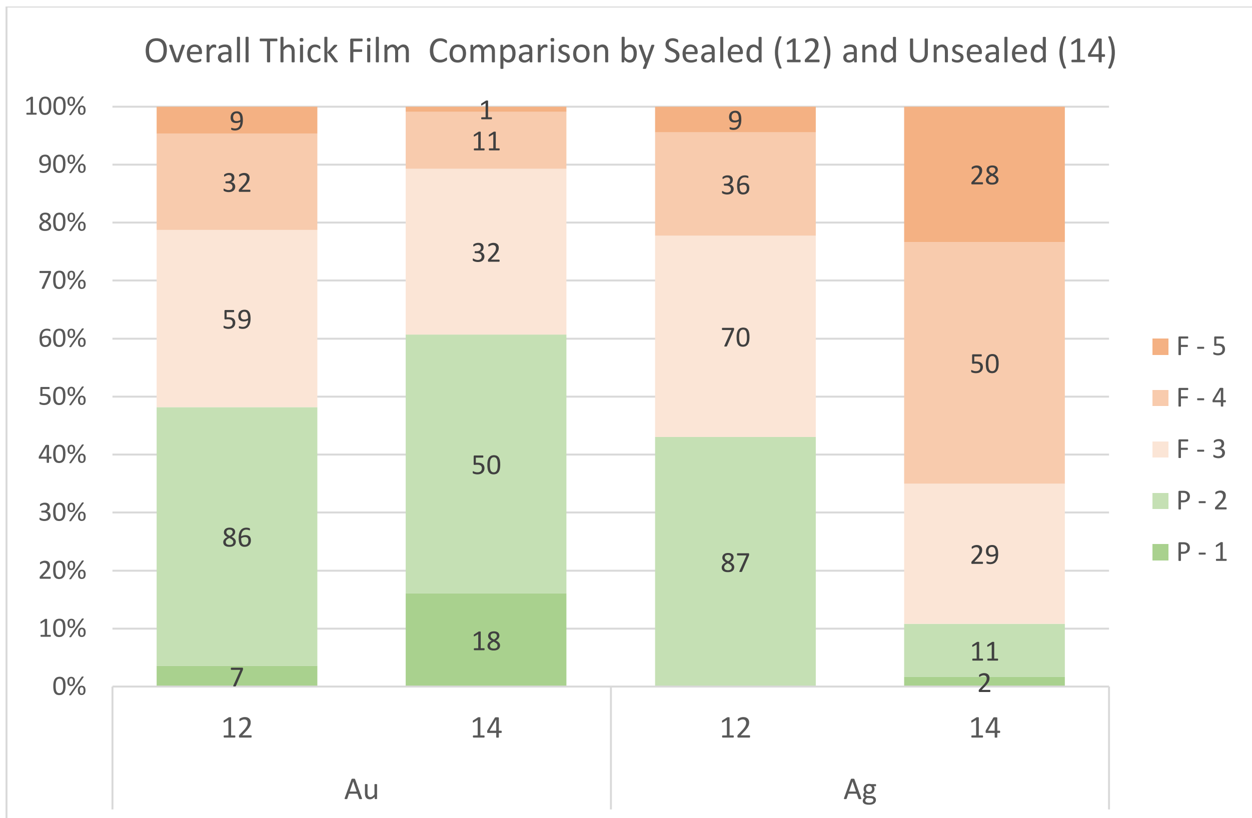

Fig. 5.69. Overall thick film comparison by sealed and unsealed features.

Fig. 5.70, Fig. 5.71, and Fig. 5.72 show the comparison between all four thin film recipes, disregarding all other material parameters except the environmental test exposure. Using Recipe A as the standard, there is a comparison graph for how each recipe compared to Recipe A. Note that not every test recipe was subjected to every environmental test, and there was considerably less resolution for recipe D due to the low number of samples tested.

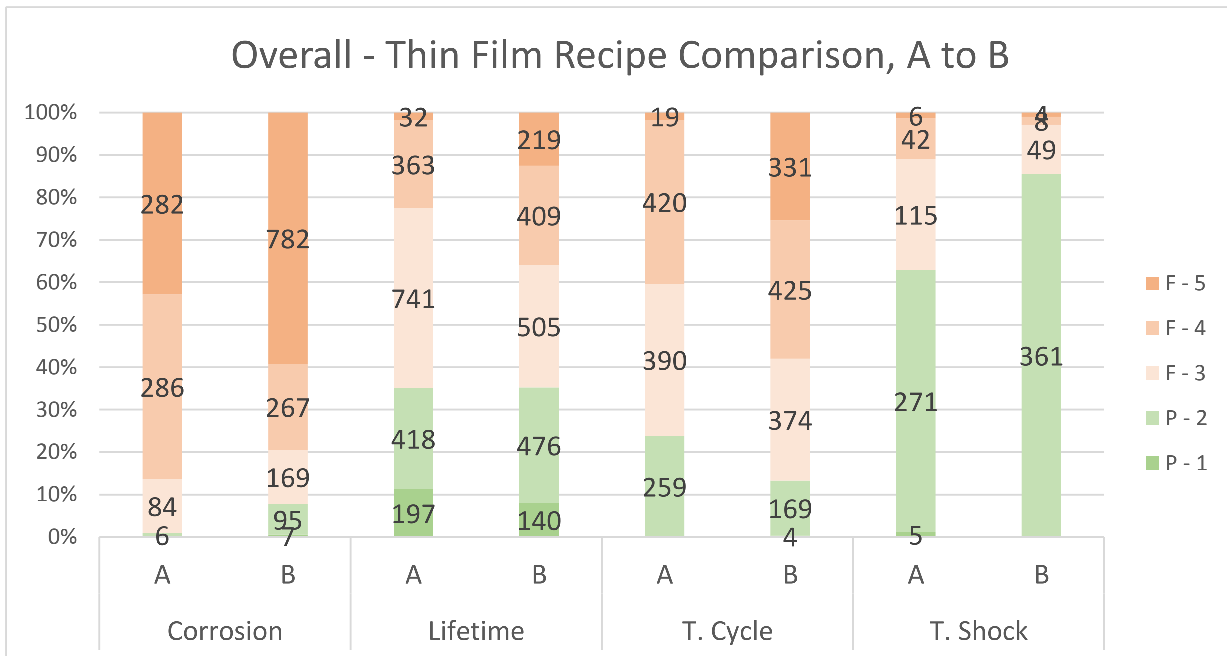

Fig. 5.70. Overall thin film comparison between recipes A and B.

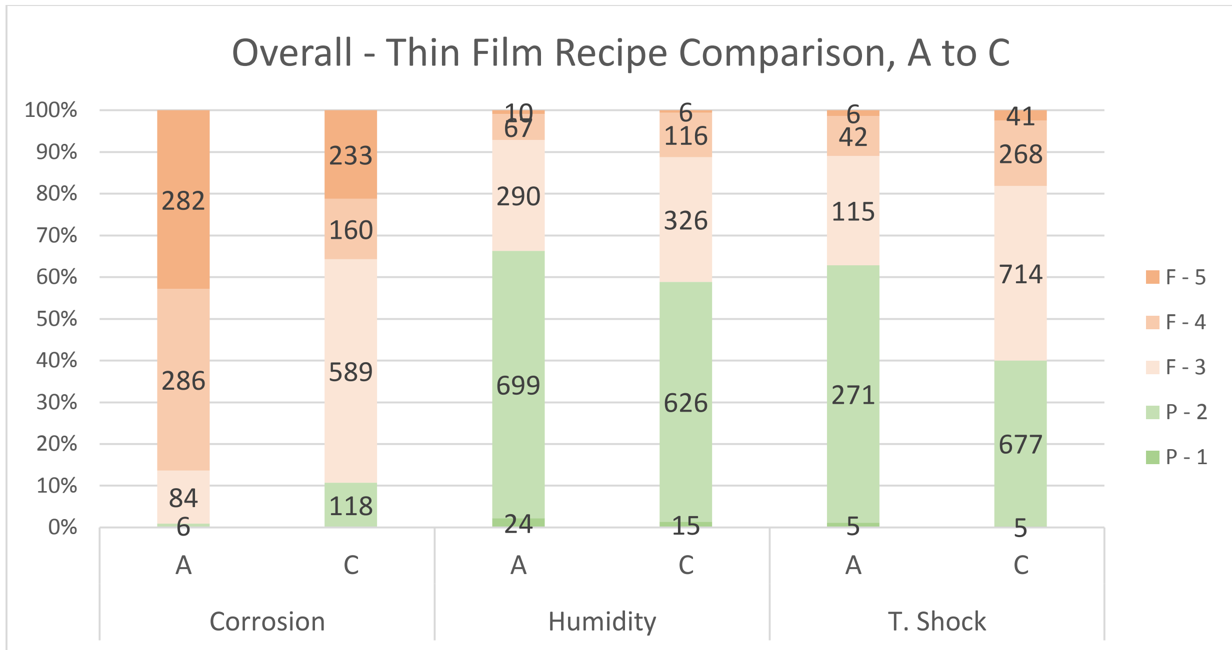

Fig. 5.71. Overall thin film comparison between recipes A and C.

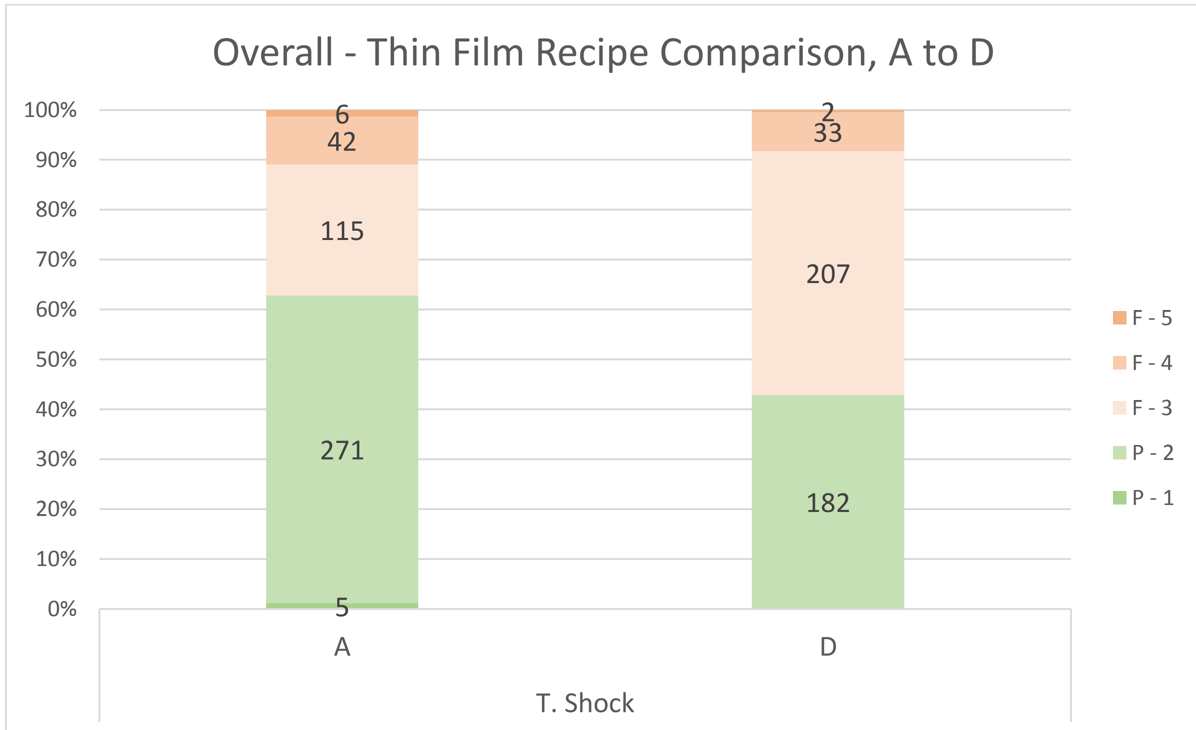

Fig. 5.72. Overall thin film comparison between recipes A and D.

When comparing Recipe A to Recipe B in Fig. 5.70, it is seen that Recipe A was favored in both the lifetime and thermal cycling tests, while Recipe B was preferred in the thermal shock and corrosion tests. In the lifetime test, the pass rate was nearly identical, however, the number of catastrophic failures was dramatically increased for Recipe B, making it less reliable. A similar trend was demonstrated and exaggerated in the thermal cycling test. It was interesting to note that the thermal shock test had a higher pass rate for Recipe B as this was a similar test to thermal cycling. A reason for this observation may have been due to the testing methods utilized; thermal cycling was performed over 30 days in air with liquid nitrogen used as the coolant, whereas the thermal shock test took five days and the samples were immersed in a liquid bath for both the hot and cold temperatures. Neither recipe had greater than an 8% pass rate in corrosion.

When comparing Recipe A to Recipe C in Fig. 5.71, it was seen that Recipe A only slightly favored the humidity and thermal shock tests, while C was favored in the corrosion test. There could be no hard conclusions from the humidity test between recipes A and C due to the high margin of standard error. In the thermal shock environment, Recipe A was more reliable by 20% over Recipe C, and the number of major and catastrophic failures was greater on Recipe C. The corrosion test had a high passing rate for Recipe C. The cause for this is not known at this time as there was no delamination present for the coupons in that test.

When comparing Recipe A to Recipe D in Fig. 5.72, notice that Recipe D was only included in one test for a direct comparison. Recipe A was shown to be more reliable in the thermal shock test by nearly 20 percentage points. It was interesting to note that Recipe A did have more pristine and more catastrophic features, whereas Recipe D was more balanced in the damage level of features.

Chapter 6 Conclusions

In conclusion, environmental reliability tests were designed to test new methods and processes for LTCC materials for use in extreme environments. There were five tests performed in accordance with MIL-STD and JEDEC standards, including lifetime testing, thermal cycling, humidity testing, thermal shock, and corrosion testing. There wa-s a complex matrix of materials to be tested including two substrates, two thick film materials, and four thin film recipes, for a total of 16 possible combinations. There were three primary questions guiding the research performed. First, would the DuPont 9K7 substrate be at least as, or more, reliable than the established DuPont 951 substrate? Second, would sealing or capping thick film base elements on LTCC substantially improve environmental reliability and, thus, keep the economic viability of moving to silver from gold? Third, which thin film recipe of the four evaluated was found to be most reliable?

The observations and data gathered showed that the 9K7 substrate was not as reliable as the 951 substrate. It was observed that the increased surface roughness of the 9K7 substrate was much higher than that of the 951. This was confirmed through the DuPont data sheets for LTCC tapes, with 951 having a roughness of 0.35 μm and the 9K7 of 0.52 μm. Discontinuities in the thin film metallization layers were observed on the 9K7 substrate as a consequence of the surface roughness. Though both the 951 and 9K7 substrates showed via/sidewall separation, the 9K7 sidewall separation was more extreme than the 951. A recommendation for any further research in this area would be to smooth the surface or the 9K7 LTCC substrate prior to metallization, as demonstrated by Miao *et al* [20].

It was concluded based on observations that sealing of a Au thick film conductor with a thin film cap did not increase the reliability of the features, but rather decreased it. However, it

was observed that sealing a Ag thick film conductor with a thin film cap did increase the reliability by over 3.5x based on the evaluation metric used. These results demonstrate that sealing a thick film with a thin film cap does help increase the reliability of the material it is covering, however the thin film cap introduces new sources of potential damage. Precautions to mitigate these extraneous failure mechanisms or to further enhance the reliability of this process could include increasing the margin for overlap of the thin film on the thick film and increasing the thin film layer thickness to more completely cover the sidewalls of the thick films.

The thin film recipes with Ti and Cu in them performed best. Other notable observations show that this particular set of LTCC and metallization layers were not meant to be used in highly corrosive environments for extended periods of time. Recipe A was shown to be the most reliable in all the tests except for the corrosion test, where Recipe C was actually the most reliable. This was due to the fact that the corrosion test attacked the Cu layer more than the Ag.

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Appendix A: Description of Research for Popular Publication

Co-fired Ceramics Lead the Way to More Exciting Automotive Technologies, Reliability in Extreme Environments Key

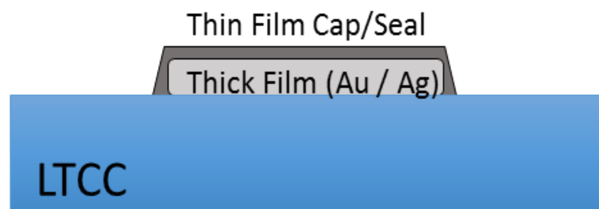
By Charles Bourland

Just sit back and imagine for a moment that your daily commute or the long drive for a vacation were made much easier. Imagine the time any trip took was reduced by a third, and that you could read and respond to emails from the driver's seat or play a game with the family. Imagine you are a highway transportation director and all the roads you've built could be completely full with absolutely no slowdowns during rush hour traffic. Advanced electronic packaging, utilizing a process called low temperature cofired ceramics (LTCC for short) is beginning to make these imaginations a reality.

"Just as Ford's Model A changed the way the public looked at the 'horse-less carriage', so electronic applications being designed with LTCC is going to transform public opinion on advances such as the self-driving car," says Mr. Bourland.

Reliability is a big deal. Knowing how long to expect a component to last influences consumer purchase price, time duration and prices of warranties, and the resell value many years down the road. A survey from Polk Automotive Intelligence says that the average age vehicle on US roads is now over 11 years old, along with the average length of vehicle ownership is up over six years and consumers expect to be able to sell it a minimum of two times [1]. All this information means consumers need vehicles that will last of a minimum of 12 to 18 years. NASA also requires that all electronic equipment put into space be expected to last a minimum of three times the expected mission duration. For example, if a mission were to be planned for 10 years, such as the Hubble Space Telescope, the electronics in the system would need to be certified to last up to 30 years.

All electronics must be 'packaged', that is too say two things: they must be protected from the elements and they must have a way to communicate with the outside world (i.e. any other electronics). Traditionally, methods such as the popular green circuit boards or an epoxy encapsulation have been used for these purposes, but as new capabilities are needed, and are required to be put into more extreme environments, new electronic packaging methods are required. LTCC is one such highly favored and viable option.



LTCC is a layered approach, where many passive electrical elements (such as resistor, capacitors, and inductors) are able to be buried into the material itself, making this approach 3-demensional and eliminating the need for surface mount devices, which further leads to greater reliability and better repeatability on the manufacturing side of things. Unlike its

predecessor HTCC (high temperature cofried ceramics), LTCC has the capability to use higher conductive metals as well, such as gold, silver, and copper as opposed to titanium and platinum. Using silver is of particular interest for the nearly 80% cost reduction and the added benefits of enhanced electrical characteristics at the high frequency and microwave range. However, silver is much more susceptible to environmental conditions. The challenge comes in protecting the silver to make it more reliable while at the same time keeping some of those cost savings.

Dr. Alan Mantooth, a professor of power electronics in extreme environments at the University of Arkansas, was approached with an opportunity to test a newly developed LTCC materials and a process flow for changing from Au to Ag by way of sealing or encapsulating the Au or Ag with a much thinner metallization film stack up. The materials and processes were complete, they just needed to be rigorously tested to see how well this new system would stand up to punishingly harsh environments, such as those found in a vehicle's engine bay, on a space satellite, or in the cockpit of a fighter jet.

Through this testing is was found what type of thin film layers would protect silver most effectively, and what types of surface features could and could not be used in certain environments. It was discovered that a thin film encapsulation did indeed increase the reliability of these electronic systems by 40%. That is not all though, Dr. Mantooth suggests that this research is simply the tip of the iceberg, the first time this method has been demonstrated to be viable saying, "now we can improve on what we saw, and I bet we could get another 40% at least with these improvements." It is an exciting time to see what comes ahead in the realm of electronic packaging.

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Appendix B: Executive Summary of Newly Created Intellectual Property

The intellectual property that was created as a result of this research belongs solely to the Sponsor, the National Nuclear Security Agency Campus of Honeywell Federal Manufacturing. This intellectual property consists of the idea that covering/sealing/capping electronic thick films on an LTCC substrate with a thin film build up does improve the environmental reliability of LTCC passive devices. The specific thin film composition type and build up (including materials and thicknesses of those materials) was optimized.

Appendix C: Potential Patent and Commercialization Aspect of Items found in Appendix B

There were no potential patents that could be pursued from this research.

Commercialization of these methods is possible through introduction into existing processes and products by suppliers and manufacturers of LTCC components. Those places would include but are not limited to: DuPont, Heraeus, Kyocera, Honeywell, other space and defense contractors, and many various automakers. It is difficult to see this intellectual property form in a startup type atmosphere as it needs to be in line, both geographically and chronologically, with existing manufacturing processes.

Appendix D: Broader Impact

D.1. Applicability of Research Methods to Other Problems

The research methods used in the course of this research and thesis are very applicable to a multitude of various other problems. All reliability tests were performed in accordance with MIL or JEDEC Standards or specs, meaning any other electronics (active or passive) could use the same, or slightly modified versions of, test setups and or analysis techniques. The methodology of determining what constitutes a pass or failure for the LTCC system or thin film sealing approach could also be applied to future work and optimization of similar systems.

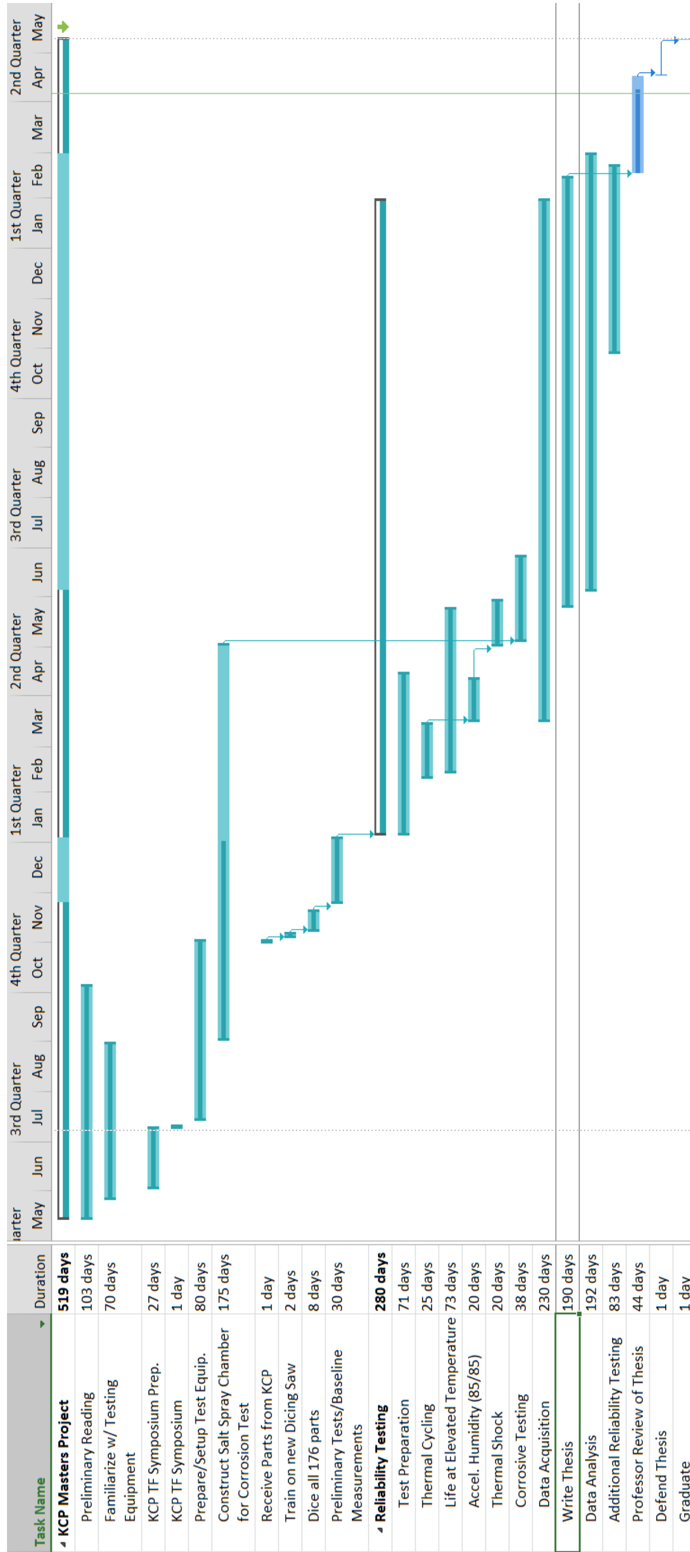
D.2. Impact of Research Results on U.S. and Global Society

The results presented in this thesis could lead to more advanced and reliable electronics for use in automotive applications, aerospace, and space exploration. Specific examples could include automotive radar systems for self-driving vehicles or communications systems for satellites.

D.3. Impact of Research on the Environment

The research presented does have an indirect impact on the environment that is two-fold. First, making electronics more reliable and extending their lifetime will help to reduce waste and lower total carbon footprint from manufacture of fewer devices over time. Secondly, being able to replace FR4 circuit boards in certain applications (e.g. mainboards) and having fewer places for solder attached devices will reduce carbon footprint of manufacture of FR4 and contamination caused by various types of solder pastes, specifically those containing lead.

Appendix E: Microsoft Project Printout for Project Planning



Appendix F: Identification of Software used in Completing Project

Computer #1:
Model Number: Lenovo Y510P
Serial Number:
Location: Home
Owner: Charles Bourland

Software #1:
Windows 8.1
Purchased by: Charles Bourland

Software #2:
Microsoft Office 2013
Purchased by: Charles Bourland

Software #3:
Microsoft Project
Purchased by: University of Arkansas, MSDNAA

Software #4:
AxioVision Rel. 4.8
Purchased by: Free

Software #5:
Zotero
Purchased by: Free

Software #6:
JMP, by the makers of SAS
Purchased by: Free, Limited Academic Trial

Software #7:
Watson Analytics
Purchased by: Free

Appendix G: Publications- Published, Submitted, and Planned

There were no publications or outstanding paper submissions during the course of this research.

There are no future plans for paper submissions.