12-2015

8 Bit Split Array Based Charge Scaling Digital to Analog Converter with Rail to Rail Buffered Output

Sai Kiran Akula
University of Arkansas, Fayetteville

8 BIT SPLIT ARRAY BASED CHARGE SCALING DIGITAL TO ANALOG CONVERTER WITH RAIL TO RAIL BUFFERED OUTPUT

A thesis submitted in partial fulfillment
of the requirements for the degree of
Master of Science in Electrical Engineering

by

Sai Kiran Akula
Jawaharlal Nehru Technological University
Bachelor of Technology in Electronics and
Communication Engineering, 2012
University of Arkansas
Master of Science in Electrical Engineering, 2015

December 2015
University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

Dr. H.Alan Mantooth
Thesis Director

Dr. Simon S. Ang
Committee Member

Dr. Roy A. McCann
Committee Member

ABSTRACT

This thesis presents the design, simulation and layout of a silicon carbide (SiC) 8 bit split array charge scaling digital to analog convertor (DAC). The converter consists of the charge scaling capacitor chain with two operational trans-conductance amplifiers (op amp) in voltage follower configuration. The op amps used in the design have the input common mode ranges of 0 to 11.2 V and 4.7V to 14.5V respectively. Additional logic circuit topologies are designed, which help to switch the op amps when needed to provide a rail to rail unity gain at the output. As the design is based on the charge based approach it has the advantages of low power dissipation (capacitor array does not dissipate DC power), the output is sampled and held and the almost zero offset. The specification of the DAC is (1) power operation less than 200 mW (2) operation up to 1 MHz and (3) with a reset enables, to reset the convertor when needed. The main focus of the thesis is on the monotonicity and to reduce capacitor sizes. The size of the largest capacitor used in the design is 16pF which makes the design as compact as possible. The major area of application of this convertor is at high temperature applications where the silicon based integrated circuits(IC) fail to operate properly.

ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisor Dr. H. Alan Mantooth, Dr. Matt Francis and Kacie Danielle Woodmansee for their valuable guidance and encouragement during my research and writing the thesis. Special thanks are given to Dr. Simon Ang, Dr. Roy McCann, Dr. Hameed Naseem and Dr. Randy Brown for their numerous discussions and lectures on the related topics that helped me improve my knowledge in the area. I would also like to thank Dr. Robert Saunders who supported me throughout the pursuit of my Master's degree at University of Arkansas

Great thanks given Ashfaqur Rahman for his help and suggestions in research and also I would like to thank students of MSCAD group for all their support and help with the use of lab resources and my friends especially shiva, Dr. Jian Lu and dharma for being supportive throughout my masters degree.

DEDICATION

I dedicate this thesis to my parents Kumara Swamy Akula and Jyothi Akula, who encouraged me and provided me with unconditional love throughout my life, my sisters swapna , sangeetha and brother in laws vishal, karthik who always motivated and supported me in my educational pursuits, also, to my friend vaishnavi sunku who inspired me and has been my rock throughout this journey.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

TABLE OF ACRONYMS

ADC	Analog to Digital Converter
CMOS	complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DNL	Differential Non- Linearity
DRC	Design Rule Check
HiDEC	High Density Electronics Center
ICMR	Input Common Mode Range
INL	Integral Non – Linearity
JKFF	JK Flip Flop
LVS	Layout Versus Schematic
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NFET	N- Type Field Effect Transistor
Op- Amp	Operational Amplifier
PCB	Printed Circuit Board
PDK	Process Design Kit
PEX	Parasitic Extraction
PFET	P- Type Field Effect Transistor
SiC	Silicon Carbide

1 - INTRODUCTION

1.1 Converter Overview

Data converters are essential for processing information. The converters are used to create a machine- human or machine- machine interface. For example, computers can understand digital signals, human cannot, nor can speakers or headphones. The better the converter designed, the better the interface will be. The Fig 1.1 below gives a brief idea about why and where the converters are required.

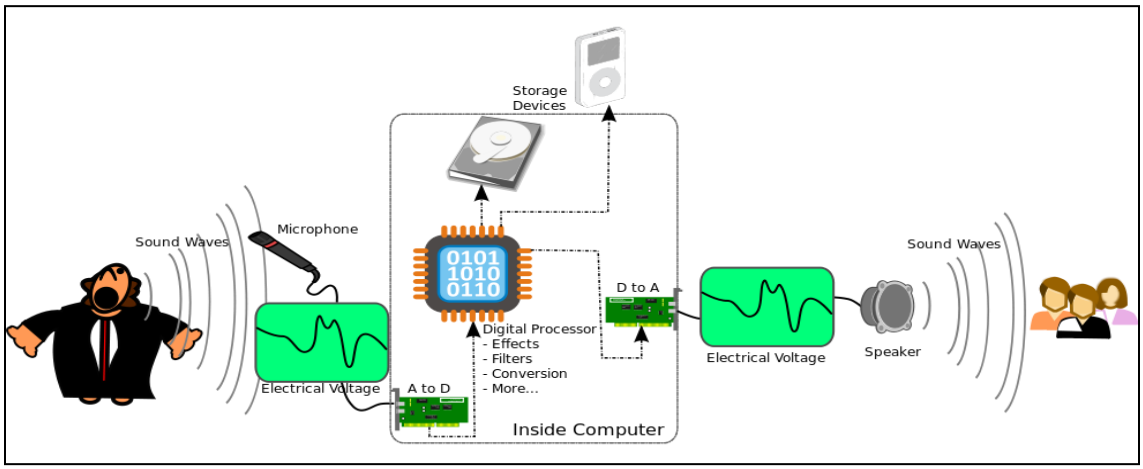


Fig. 1.1. Data Conversion

In the above figure, the start and end users are humans, for processing the information signals must be converted to digital or machine understandable form and it is often required to have the processed data at the output as an analog signal. This is where the digital to analog converter is required.

In order to process information (end to end) in a system without any signal loss a precise converter has to be designed. The performance of the digital to analog converters is mainly measured by two standard error measurements; they are integral nonlinearity (INL) and differential nonlinearity (DNL)[8].

INL (Integral non Linearity): It describes the maximum deviation of the ideal output and the actual output of DAC.

DNL (Differential non Linearity): It is defined as the deviation between two analog values corresponding to adjacent input digital values. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB (Least significant bit) step. The LSB voltage is the minimum change in the voltage required to guarantee change in the output voltage level. A differential non-linearity greater than 1 LSB may lead to a non-monotonic transfer function in a DAC. It is also known as a missing code.

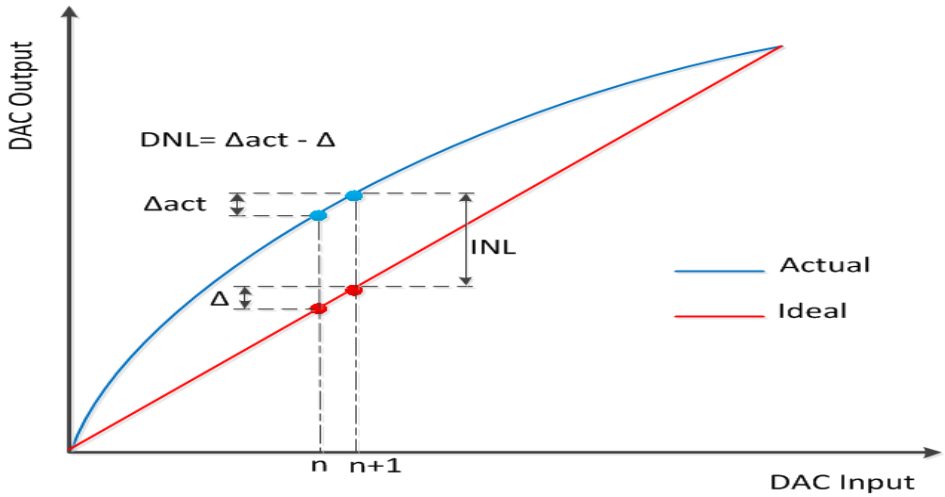


Fig. 1.2. Non-linearity in DAC

1.2 Application

The DACs are used in the field where there is a need for data storage and retrieval, signal transmission. A few applications of the converters are discussed below

(i) Audio

Audio signals are stored in digital format in order to save memory, in order to hear these audio signals conversion has to be done from analog to digital. In most cases the speakers have built-in DACs which play the role of signal conversion. Therefore DACs are present in most electronic gadgets like CD players, music players, USB speakers and pc sound cards. DACs are also found in VoIP(voice over IP) applications, where the analog signal at the senders end is digitized for the transmission by an analog to digital converter(ADC) and is converted to the analog form at the receiving end by a digital to analog converter(DAC).

(ii) Video

A CPU stores information in the digital format. In order to view the data on the analog monitor the data received has to be converted from the memory to its corresponding analog value. DACs are commonly seen in devices such as digital video players, DVD players, DTV and computer displays

(iii) Industrial Control Systems

A widely used control system which incorporates DACs for is the whippletree. It uses a mechanism to distribute force or pressure evenly though the linkages. Other type of control systems where DACs play a prominent role are motor control, valves, and transducer excitation.

(iv)Waveform Function Generators

Very high speed test equipment such as sampling oscilloscopes. These are uniquely designed to capture, display, and analyze repetitive signals

1.3 Digital to Analog Converters

DACs are classified into two categories: parallel and serial. Based on the topologies there are wide varieties of DACs available each having their own advantages and disadvantages. These DACs are further classified based on the conversion speed or by how the binary scale of reference is accomplished. The classification of digital to analog converters can be seen in Fig.1.3 below.

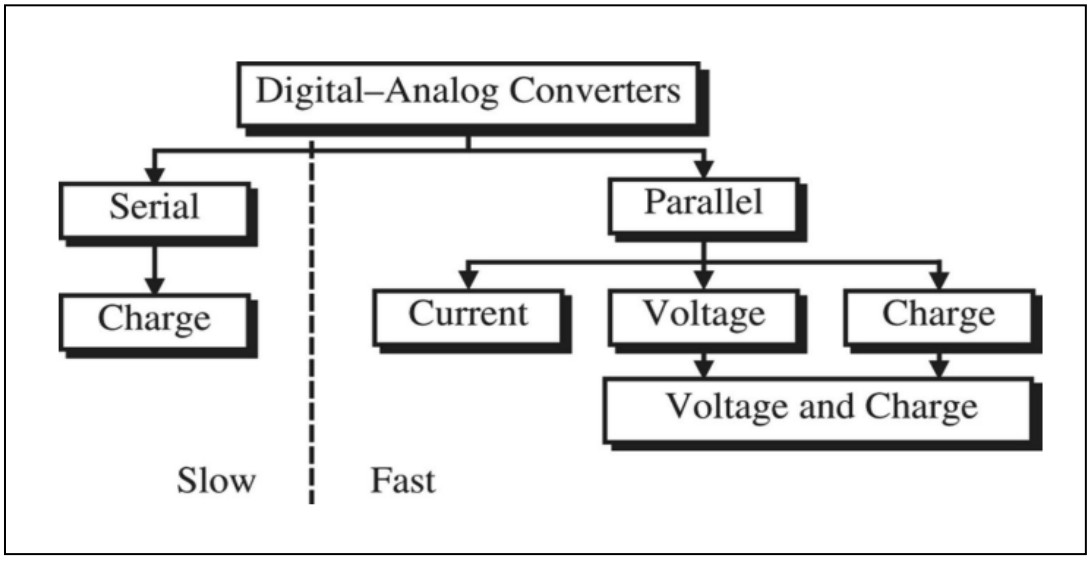


Fig. 1.3. Classification of Digital to Analog Converters [1]

Fig.1.3. shows the hierarchy of classification of DACs in terms of speed. The parallel DACs are very fast as they take the input in a parallel manner and produce an analog output after

processing. These DACs can be implemented using various methods like charge scaling, voltage division and current steering. On the other hand, the serial DACs are very slow. It takes the input in serial order and depending on the given input the capacitor will be charged and discharged to give the final analog output. The serial DACs are implemented only with the charge scaling approach. A popular example of serial DAC is cyclic DAC. The Table 1.1 below gives the advantages and disadvantages of DACs that are commonly used.

Table. 1.1. Differences Between the Commonly available Data Converters[2]

Type of DAC	Components used	Implementation method	Advantages	Disadvantages
Resistor string	Resistors and switches	Voltage division	1.The output is always monotonic 2.Fast for <8 bits	1.Large conversion speed for bits >10 2. Large chip area for high bit resolutions 3. Large power dissipation 4. Requires 2^N Resistors
R-2R Ladder	Resistors	Voltage division	1.Inexpensive and easy to manufacture 2. Faster response time	Small inaccuracies in the higher significant bit resistors can entirely overwhelm the contribution of the less significant bits. This may result in non-monotonic behaviour at major crossings, such as from 01111 to 10000
Generic Current Steering (or) Current steering using Binary weighted current	Precision current sources	Current steering	Faster conversion speed	1. Use of binary weighted current steering DAC.An 8 bit DAC needs 8 current sources with the largest being 2^{N-1} times greater than the smallest 2. Causes glitches

sources				
Charge Scaling DAC'S	Capacitors	Charge scaling	1.Low power dissipation 2.Output is sample and held	1.Requires large capacitor ratios 2.Not inherently monotonic
Cyclic DAC **(paralle)**	Capacitors, operational amplifiers	Charge and discharging of capacitors	1. High accuracy 2. Fast conversion speed 3, Output is sampled and held	1. High power consumption 2.Occupies large circuit space

1.4 Organization of the Thesis

Chapter 2 covers the implementation of the DAC, all the other analog and digital blocks which are used in the design and also it provides the description of the different topologies used. Chapter 3 describes the simulation results of all the individual blocks and also the DAC integrated circuit using different topologies. Chapter 4 presents the actual layout of all the blocks designed. chapter 5 covers the conclusion and the recommendations for future work. Appendix A covers the test plan of the circuits. Appendix B covers the temperature and extracted simulations. Appendix C covers the characterization of Schmitt trigger circuit. Finally Appendix D covers the pipeline based DAC model which is more accurate with some limitations discussed in detail.

2. DIGITAL TO ANALOG CONVERTER DESIGN

2.1 Design Procedure

By comparing all the DAC models shown in Table 1.1, it is found that charge scaling version of DAC is more advantageous to implement because of its inherent characteristics of lower power consumption and output sample and hold. The power consumption is give importance because the DACs are mostly used in the interface systems. If a DAC is designed for lower power consumption helps to reduce the power consumption of overall circuit by significant amount, It is also important for a circuit to hold the data until the input changes again. It also seems to have a disadvantage of large capacitor sizes and non monotonic output. The sizes of the capacitors can be reduced by implementing the DAC with split array model. The split array based approach is used to save the circuit space. The design of a charge scaling split array DAC includes defining the requirements of the design, creating an architectural model, defining the process design kit, hand calculations, simulations, physical design, fabrication, verification and testing. A design is said to be complete when it passes through all these implementation phases. The V diagram shown below gives the brief idea of how a design process works.

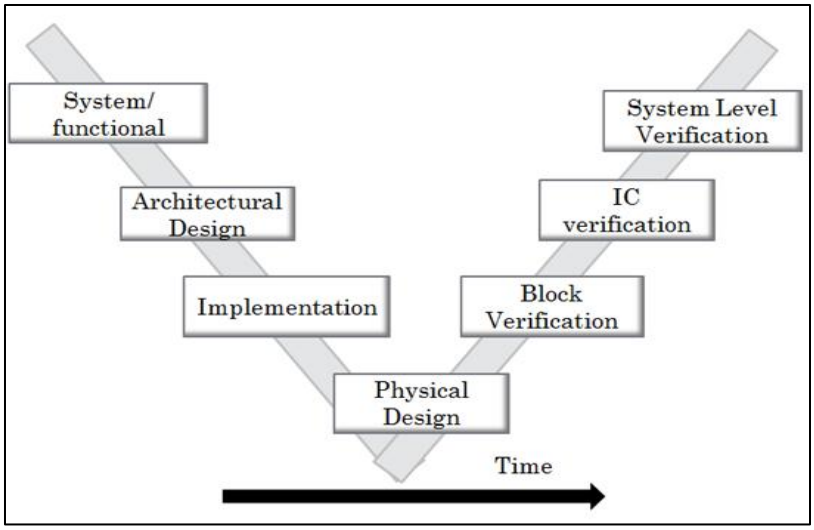


Fig. 2.1. V Diagram [10]

1. The System/ Functional level is the phase in the design where the high level validation of the design is performed. This is the most important level of the design process; if the top level doesn't work then major changes have to be made to the system, so it works as desired. This step saves a lot of time that would be consumed if the implementation is started directly.

2. In the Architectural level model, the specific sub blocks are put in place with accurate connectivity and behavior. This model is an abstract design, but correlates directly to hardware to be built [10].

3. In the implementation phase the circuit is designed with the real transistor models. The simulations are run under varied temperature ranges and process corners. Slight deviations are seen in the outputs when compared to the ideal models which is due to the addition of all transistor parameters to the models like thresholds, gate capacitance etc.,

4. In the physical design phase, the implementation of the schematic is represented in its physical form which is later converted to a .GDSII format (the design in the form of rectangles and polygons), which is sent out for fabrication.

5. The block verification phase checks the consistency of the physical design with the schematic and a set of rules are followed while designing the layouts. The verification of the design for the design rules and the consistency of the layout are carried out in this stage with the help of DRC, LVS error checking tools.

6. In the IC verification phase of design test and verification plans are developed to test the design under real case scenario, compare with the simulation results.

7. In the system level verification phase, the circuit performance is measured as a whole. This is the last step of the design cycle and improvements are made to the design if required before the chips are sent for fabrication.

2.2 Architectural Design

The main purpose of creating the model is to verify how the circuit works at a given frequency and provided specifications. This model helped in determining the capacitor sizes such that the input capacitance of the op amp buffer does not affect the DAC output. The Fig. 2.2 shows the architectural design of the charge scaling DAC. All the sub blocks used in the design have the ideal characteristics.

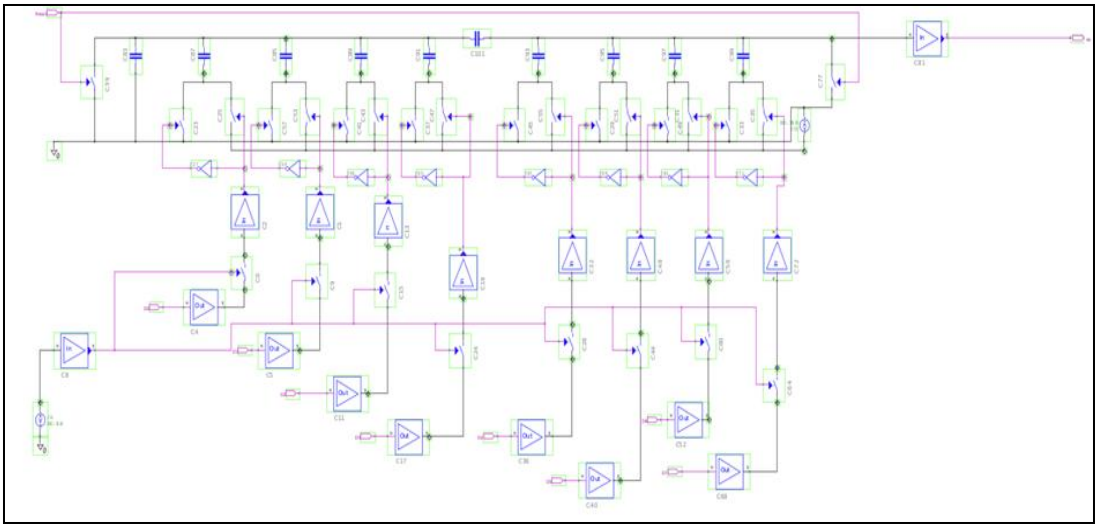


Fig. 2.2. DAC System Level Model

The Table 2.1 provides the specifications for which the circuit is designed. This circuit consumes very low power and operates at frequencies as high as 1MHz.

Table 2.1. Charge Scaling DAC design Specifications

Design Parameters	
Vref	15 V
Vout Range	0 to 14.5 V or binary value
Power consumption	8.3 mW
VDD	15 V

Operating frequency	Upto 1 MHz

The Table 2.2 gives the information of all the sub level blocks of the design. All the blocks are modeled to behave ideally and the circuit internal parameters are not accounted.

Table 2.2. Design Sub Level Blocks

Library	**Model**	**Total Used**	**Type**
eb_Logic	eb_Inverter_VV	8	Built-in-effect
eb_Electrical	eb_Switch	18	Built-in-effect
eb_Electrical	eb_Capacitor	10	Built-in-effect
sl_PortsSubsystems	sl_Inport	17	Built-in-effect
Spice	spl_V_vdc	1	User created effect: Spice DC voltage source

2.2.1 Test Bench

The Fig. 2.3 shows the test bench for DAC architecture model. Pulse divider circuits are used in order to provide a sequential bit pattern to the input of the converter. The frequency of the clock signal is 1 MHz. The simulator tool used is SPICE.

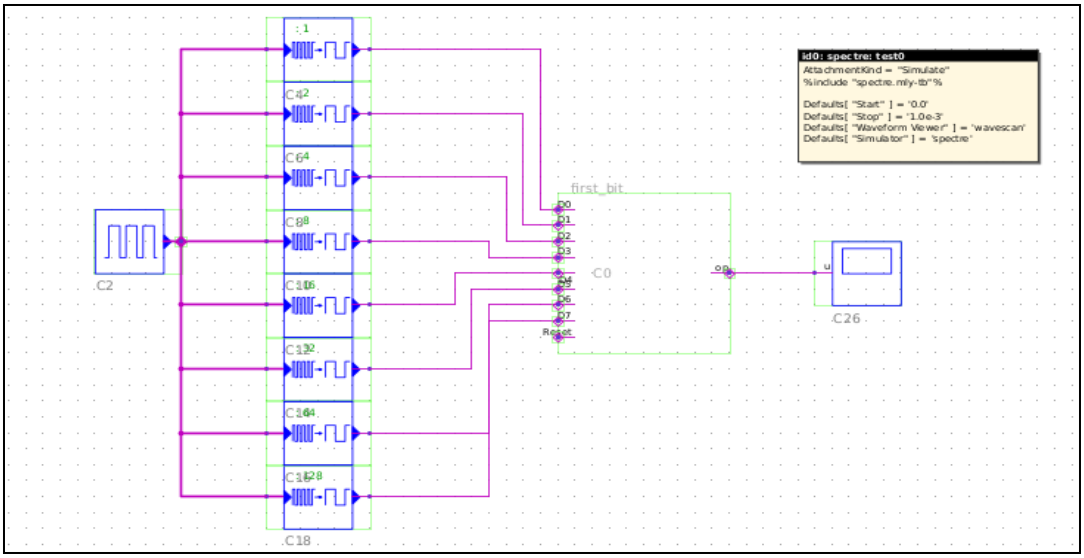


Fig. 2.3. Top Model Test Bench

The plot below shown in the Fig. 2.4 is the representation of output voltage of the DAC versus time. The spikes in the output are caused during the charging and the discharging of the capacitors, which is quite common in all charge based design approaches. These spikes can be eliminated by placing op amp buffers at the output.

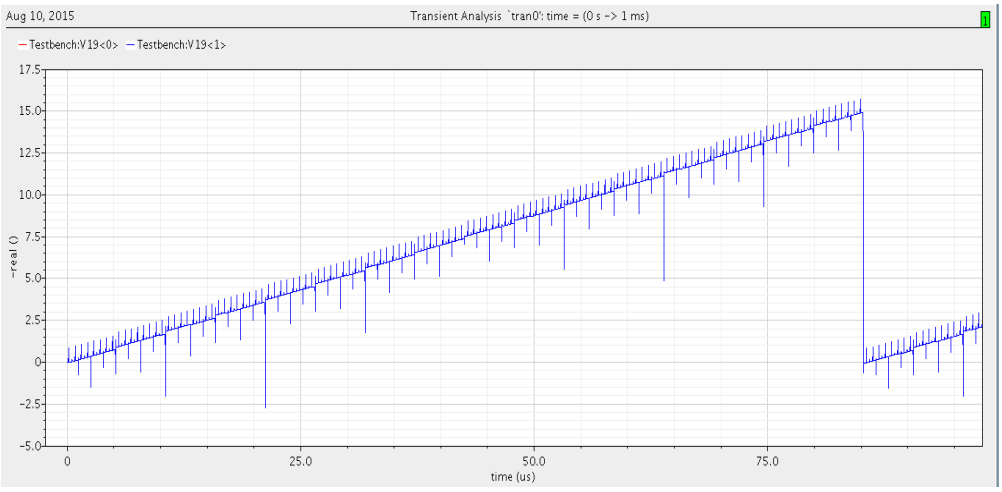


Fig. 2.4. Full Scale Ramp

2.3 Implementation

The Fig. 2.5 below shows the complete topology of DAC. This has three stages. The first stage consists of a charge scaling DAC, the second stage consists of logic circuitry built with sub blocks such as Schmitt trigger, flip flop and transmission gates and the final stage comprises of two op amps in voltage follower configuration.

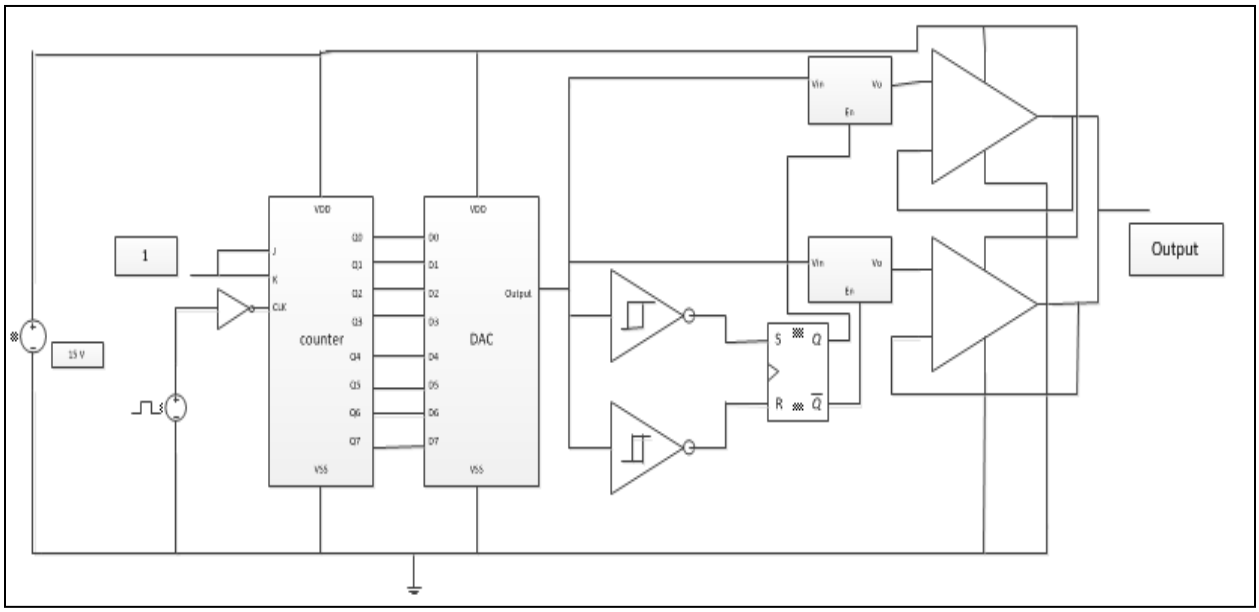


Fig. 2.5. DAC Integrated Circuit

The topology comprises of all the sub blocks designed under analog and digital circuit libraries. The blocks such as DAC, Counter, Schmitt trigger, Inverters, Transmission gates and digital buffered are designed as a part of the Full chip design. The operational amplifiers are used from the previous run with were designed by fellow students. Table.2.3 shows the blocks used in the design.

Table 2.3. Blocks used in the Logic circuit Design

Counter
Charge scaling DAC
SR flip flop
Schmitt trigger
Transmission Gates
Op amp buffers
Digital buffer

The design topology is comprised of three stages, those are basic charge scaling DAC, logic circuitry and the output buffer.

The logic circuitry is comprised of blocks such as Schmitt triggers, transmission gates, digital buffers and SR flip-flop. The main idea of using this topology is to provide rail to rail buffered output. The op amp buffers used in the design have an input common mode range of 0 to 11.2 V and 4.7 to 14.5 V respectively. In order to get a rail to rail buffered output, both the op amps are used in combination and make the transition between them depending upon their ICMR. The SR flip-flop is the heart of the logic circuitry; it is the one which controls the switching between the op amps.

Operation:

The output of the DAC is fed into the transmission gates and the Schmitt trigger. The Schmitt trigger provides the corresponding digital output based on the provided switching threshold levels. The output of the Schmitt triggers is fed into the SR flip flop, which controls the switching states of the transmission gates. These transmission gates acts as the interface between the DAC and the op amp buffers. The Table 2.4 shows different states of the SR flip flop and the corresponding switching of op amps and transmission gates.

Table 2.4. States of SR Flip Flop

S	R	Q	Qbar	Opamp1	Opamp2
0	**0**	**Q0**	**Q0bar**	**Depends upon previous state**	
0	**1**	**0**	**1**	**OFF**	**ON**
1	**0**	**1**	**0**	**ON**	**OFF**
1	**1**	**NA**	**NA**	**Output state is undisturbed**	

2.3.1 Digital Building Blocks

These blocks are designed to create the test bench, and logic circuitry needed for the Digital to Analog Converter design. This section provides more details about the blocks used in the design.

Digital buffer

The digital buffer is a driver for a large load, which is used to isolate the input signal from the output signal preventing the impedance of one circuit altering the other, which improves the drive capability of the circuit [13]. Generally buffers are used to drive output pads of a chip, to drive long wires, and anywhere that a large number of inputs that must be driven rapidly. The digital buffer designed is a basic 3X inverter buffer which has the delay of 14 ns and can drive an output load which is 10 times more than its input capacitance. The main advantage of using this circuit in the design is to provide proper isolation between the input and output terminals.

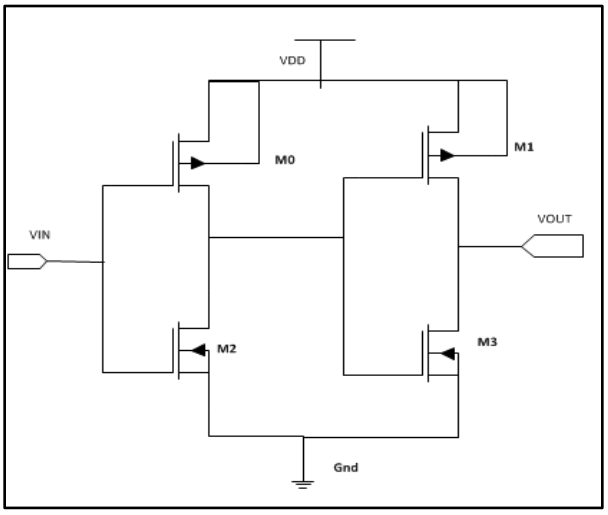


Fig. 2.6. Inverter 3X Digital Buffer

The drive capability of the buffer is given by the equation

$$f = \sqrt[N]{F} \qquad \textbf{(2.1)}$$

The normalized delay of the logic gate can be expressed as a summation of two primary terms, parasitic delay P (delay considered without load) and path effort F, (considered with load). The parasitic delay for the inverter is found to be 1 from Elmore delay model of the inverter. The path effort F, is given by the product of path logical effort G (product of individual logical efforts of the gates), path electric effort H (ratio of the load capacitance to its input capacitance)[13] and the branching factor.

$$F = BGH,\ H = Cload/\ Cin$$

Where, N – Number of inverter stages, G – Logical effort, B – Branching factor

The value of N is chose such that $2< N < 5$. Buffer designed using the N in between this range is found to have least delay.

For the inverter B = G = 1

$$\boxed{Cload/\ Cin = f^N}$$

For a 3X inverter buffer with two inverters in chain

$$\boxed{Cload/\ Cin = 3^2 = 9}$$

The buffer can drive a load which is 9 time higher than its input

Counter[2]

A counter is a sequential circuit; it is a register that goes through a predetermined sequence of states upon the application of input. The counter designed is an 8 bit synchronous counter which can operate at frequencies as high as 1MHz and consumes power of 80 mW (worst possible case). The output bits of a synchronous counter change simultaneously, with no ripple. The state of the signals in a synchronous counter can be changed only with the application of distributed clock signal, which makes the circuit predicTable. Another advantage of using this topology is that the synchronous clock signals are less susceptible to noise, which makes it safer to design and operate. The purpose of designing this counter is to ease the testing of the DAC. The counter is designed using a 1.2 µm SiC process, this improved the rise and fall times of the output pulse when compared to topologies which are designed using 2 µm SiC process in the previous runs. The output pulses of the counter have a rise and fall times of 20 nanoseconds and 16 nanoseconds respectively. The operation of the counter is a very simple. When both the input of the JK flip flop is assigned to logic '1', it makes the output of the flip flop to toggle for each rising edge of the clock pulse provided. The output of the first flip flop is fed to the input of the second one and so on. This make the flip flop switch between the states and provide the

sequential output. The schematic of the counter is shown in Fig. 2.9.

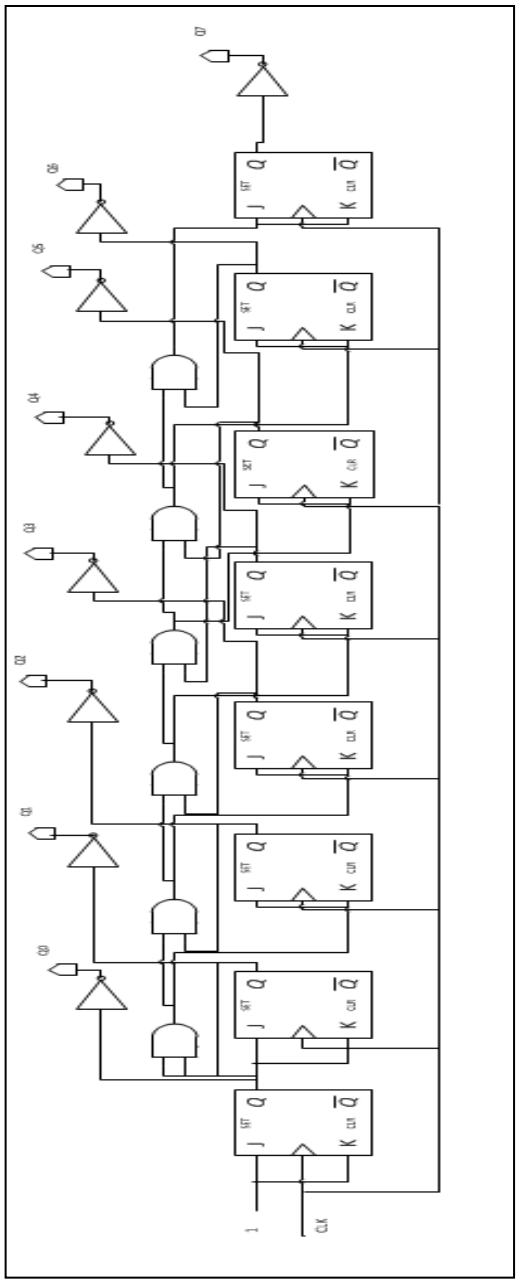
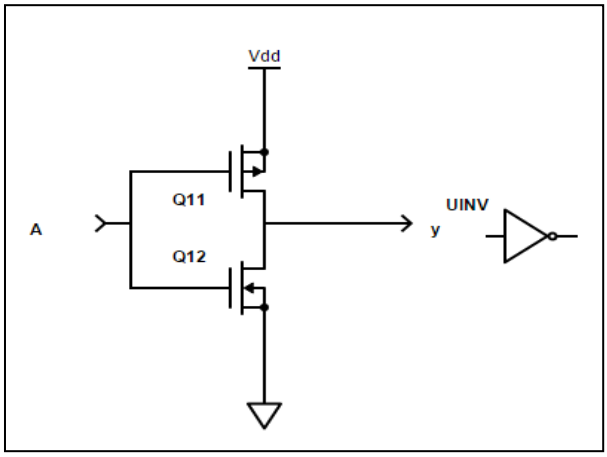
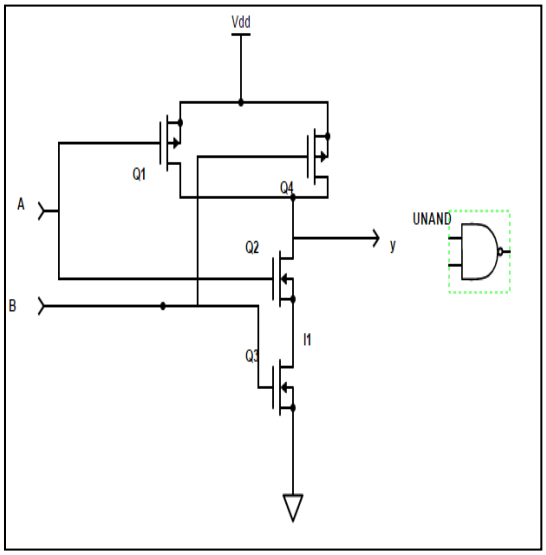


Fig. 2.7. 8 bit sequential up counter

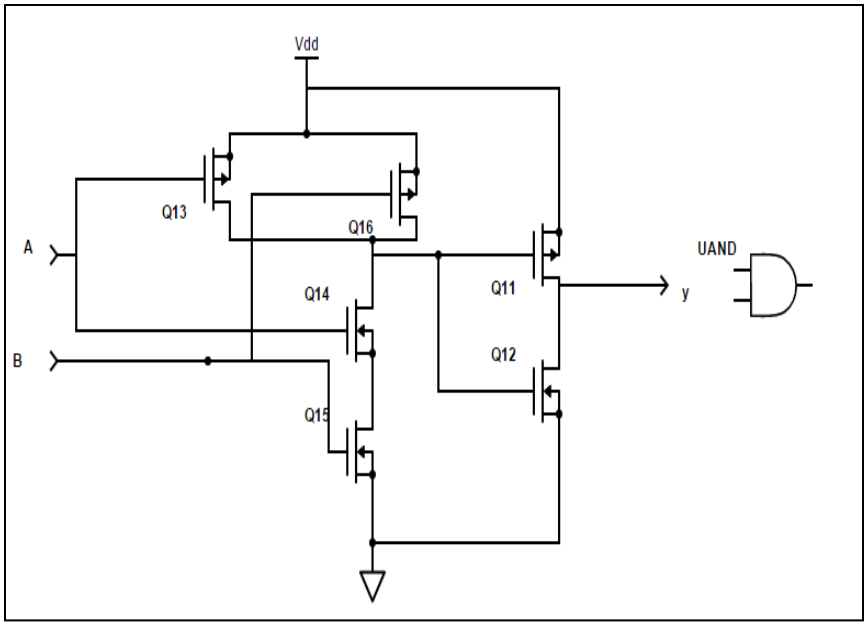
The counter is built using the basic digital gates. The schematics of the inverter, 2 and 3 input NAND, AND the digital cells are given in Fig. 2.10 for completeness



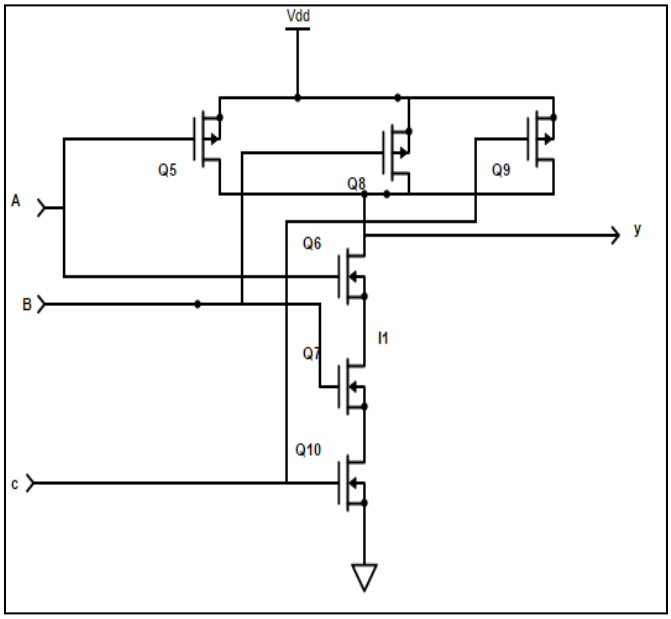
(a)



(b)



(c)



(d)

Fig. 2.8. Digital cell Schematics

JK Flip Flop

The digital sub cell is required to design the counter is JK flip flop. The JK flip is the combination of two and three input NAND gates and inverter [2].

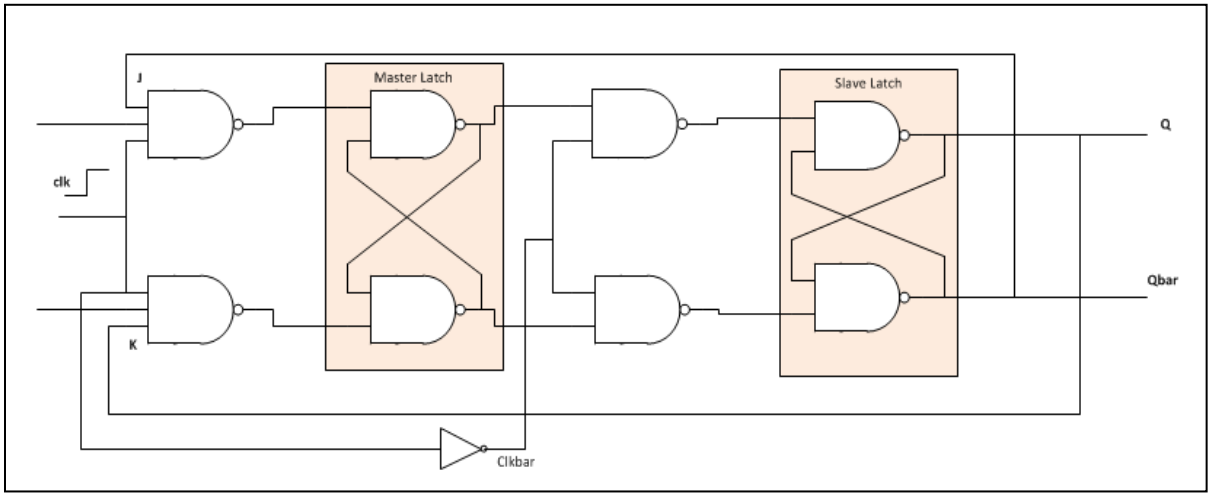


Fig. 2.9. JK Flip Flop Master and Slave

The JK flip flop is the core building block of the counter design. The JK flip flop behaves the same as the SR flip flop except for the state when j=k=1. In this state the output of the flip flop toggles for each and every clock pulse given to it. The flip flop is positive edge triggered, which change states only on the application of positive edge of the clock cycle. The truth Table of the JK flip flop is given in Table.2.5.

Table 2.5. Truth Table JK Flip Flop

J	K	Q	Qnext	comment
0	0	0	Q	Hold state
0	1	0	0	Reset
1	0	1	1	Set
1	1	1	Qbar	toggle

The flip flop is designed to operate with less propagation delay and have high driving capability. The counter circuit is designed to have low rise and fall times. In order to make the counter to operate fast, the sub blocks of the circuit are designed such that the response time of the whole circuit is as low as possible. Uniformity is maintained for the rise and fall times all the circuits in the design, which is in the range of 15 to 20 nanoseconds

2.3.2 Analog Building Blocks

The analog building blocks are spread out in all the three stages of the design. The first stage comprises a charge scaling capacitor chain, the second stage contains the Schmitt triggers and the transmission gates and the final stage has the operational amplifiers in voltage buffer configuration.

Schmitt Trigger

This is the crucial sub-block of the logic circuit. As a part of the design, two Schmitt triggers were used which plays an important role in switching between the op amps when needed. The Fig. 2.12 shows the basic topology of the Schmitt trigger circuit[2].

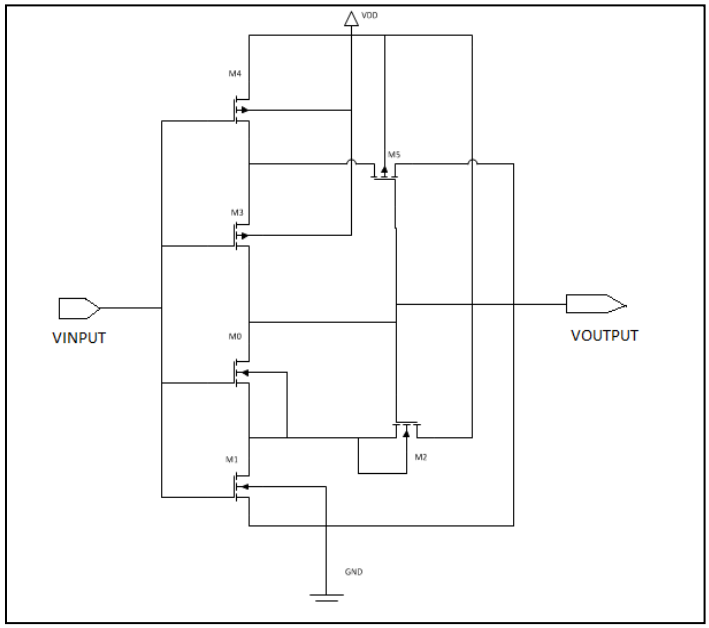


Fig. 2.10. Schmitt Trigger

Analysis:

Assuming the output is high and input is low, the analysis is started from the bottom portion of the Schmitt trigger show in Fig. 2.11. The upper switching point(Vsph) voltage is determined by analyzing the switching states of the MOSFETs. When Vin is 0, MOSFETs M1 and M2 are off, while M3 is on. The source of M3 floats to VDD – Vthn, which is approximately 11.5 V for VDD of 15V.

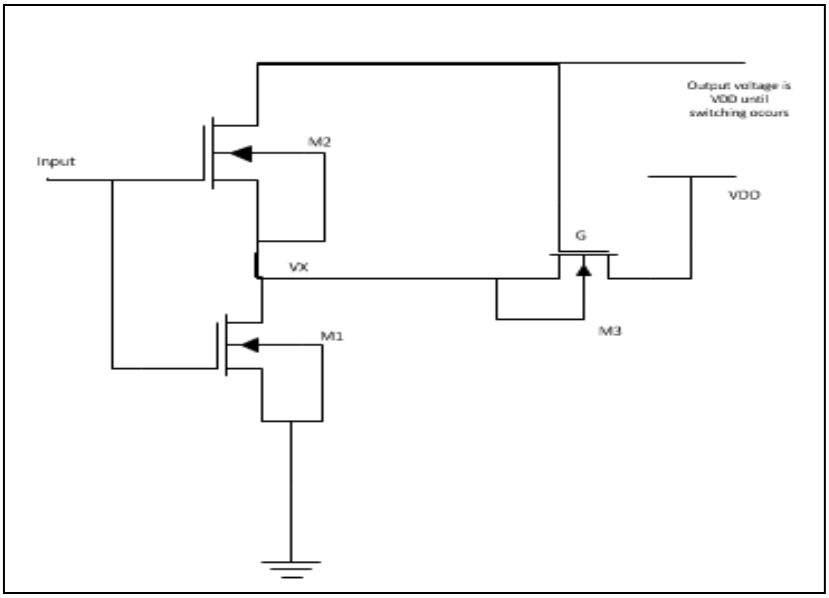


Fig. 2.11. Lower portion of Schmitt Trigger used to calculate upper switch point voltage [2]

When Vin less than the threshold voltage of M1, Vx remains at VDD – Vthn3. As Vin is increased further, M1 begins to turn on and the voltage, Vx, starts to fall towards ground. The high switching point voltage is defined as

$$Vin = Vsph = Vthn2 + Vx \tag{2.2}$$

As M2 starts to turn on, the output starts to move towards the ground, causing M3 to turn off. This causes Vx to fall further, turning M2 on even more. This positive feedback cause the switching to be well defined.

The current flowing through M1 and M3 are essentially the same. Equating these currents

$$\beta_1/2\ (Vsph - Vthn)^2 = \beta_2/2\ (Vdd - Vx - Vthn3)^2 \tag{2.3}$$

Since M2 and M3 are tied together, Vthn2 = Vthn3 , the increase in the threshold voltages from the body effect is the same for both MOSFET.

$$\beta_{1/}\ \beta_3 = W1L3/\ L1W3 = [\ Vdd - Vsph/Vsph - Vth]^2 \qquad (2.4)$$

The threshold voltage of M1, given by Vthn in this equation, is the zero body bias threshold voltage. Given specific upper switching point voltage, the ratio of the MOSFET transconductors is determined by solving this equation. A general design rule for selecting the size of M2, that is, $\beta_{2,}$ is to require that

$$\beta_2 > \beta_{1\ or}\ \beta_3 \qquad (2.5)$$

Since M2 is used as a switch. A similar analysis can be used to determine the lower switching point voltage. The resulting equation is.

$$\beta_{5/}\ \beta_6 = W5L61/\ L5W6 = [\ Vspl/Vdd\ -Vsph - Vthp]^2 \qquad (2.6)$$

Thus, from the equations given above the upper and the lower switching point voltages of the Schmitt trigger can be determined.

The Schmitt trigger topology shown in the Fig. 2.14 is the modified version of the basic Schmitt trigger circuit. Using the BSIM4 models for the design, these are modeled at Cato springs research center at university of Arkansas. These models provide the most accurate characteristics match with fabricated SiC devices. Threshold voltages of PMOS are very high. So, it is always better to have fewer PMOS transistors in the pull up network of the design to get equal raise and fall times with less transistor sizes and this will also improve the circuit switching speeds. The circuit analysis is same as the basic Schmitt trigger circuit except for the lower

switching threshold voltage, which is determined during the simulations and can be set by varying the size of the pull up transistors.

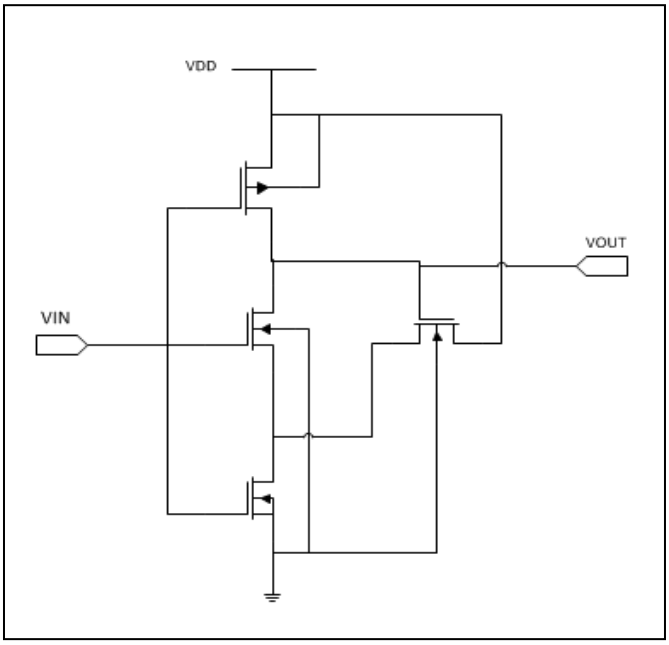


Fig. 2.12. Modified Schmitt Trigger Circuit

Charge Scaling DAC:

A charge scaling DAC requires large sized capacitors when designed for a high resolution, which can be resolved by the split array based DAC. For example the MSB capacitor size required by a 8 bit charge scaling DAC with a unit capacitor size of 2 pF is 256 pF whereas the size of the largest capacitor in the 8 bit split array based DAC is 16pF. The layout area of a 2pF capacitor fabricated using this process is approximately 0.6 X 0.6 μm^2. A lot of design space can be saved by designing the DAC using split array based model.

The Fig. 2.5 shows the implementation of charge scaling DAC. It is built with the basic sub blocks like transmission gates, inverters, and capacitors.

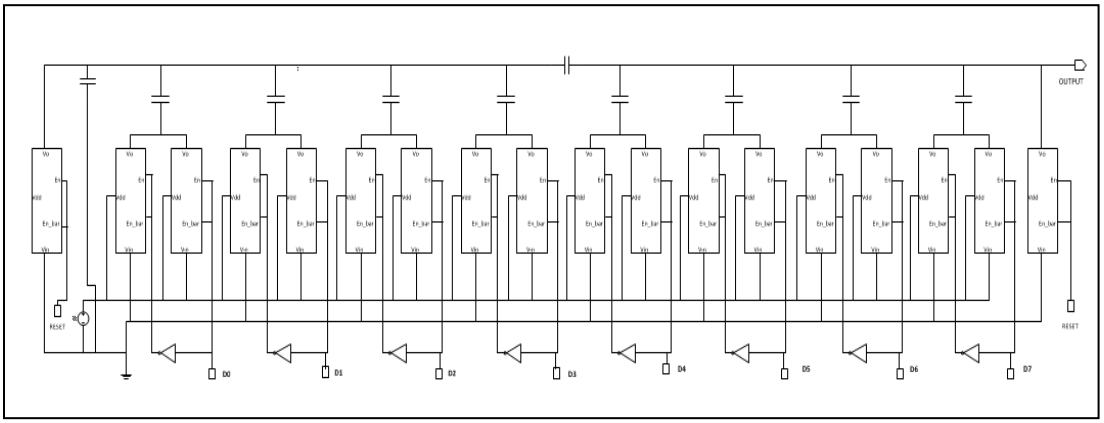


Fig. 2.13. 8 Bit Split Array Based Charge Scaling DAC

The architecture of split array based DAC is different from charge scaling DAC in two ways, the output is taken at the MSB in a split array based DAC where as it is taken at the LSB in the charge scaling DAC. In split array based model an additional capacitor is used to separate LSB from the MSB array. The value of the attenuation capacitor is given by

$$Cattenuation = C2 = \frac{sumof\ LSB\ array\ capacitors}{sumof\ MSB\ array\ capacitors} = \frac{32}{30}C \qquad (2.6)$$

Sum of MSB capacitor sizes is equal to the difference of the sum of LSB array capacitor sizes and the attenuation capacitor size. The value of the attenuation capacitor should be such that series combination of the attenuation capacitor and the LSB array, assuming all bit are zero, equals C (size of minimum capacitor) [3].

To understand the split array based model the circuit is modified to its Thevenin equivalent as shown in the figure below.

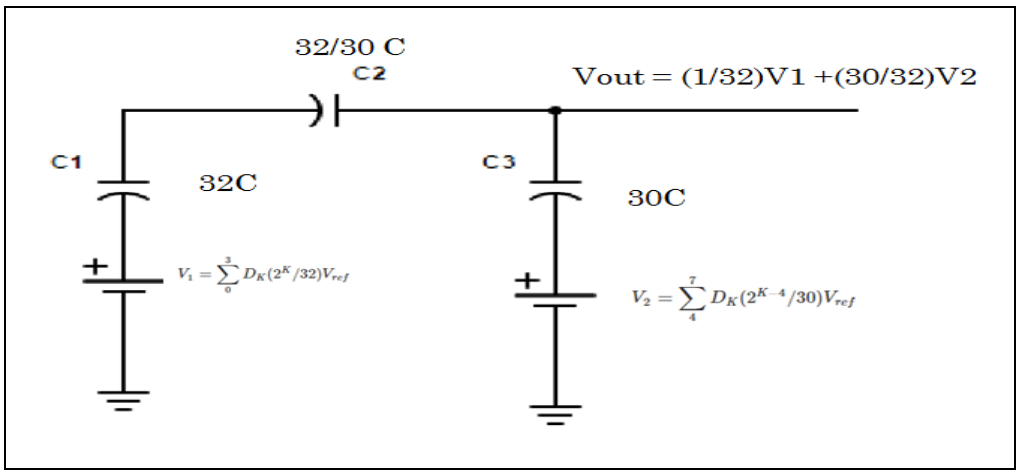


Fig. 2.14. Thevnin Equivalent of Split Array DAC

The equivalent model of split array based charge scaling DAC consists of two capacitors in series with voltage sources which are separated by an attenuation capacitor. The voltages v1 and v2 are given by

$$V1 = \sum_{0}^{3} Dn(2^n/32)Vref$$

$$V2 = \sum_{4}^{7} Dn(2^{n-4}/30)Vref$$

The output of the DAC is given by

$$Vout = (1/32)\,V\,1 + (1/30)\,V2 \qquad (2.7)$$

2.3.3 Transmission Gates

Transmission gates in the design are used to create a charging and discharging path for the capacitors. Capacitors in the circuit are enabled/ disabled by the DAC'S binary input signals.

Transmission Gates can be used to quickly isolate multiple signals with a very less investment of board area and with a negligible degradation in the characteristics of those critical signals [8]. The N- channel pass transistor passes logic ‘0’ perfectly but degrades logic ‘1’, P- Channel pass transistor passes logic ‘1’ perfectly but degrades logic ‘0’. The CMOS transmission gate passes both 1’s and 0’s perfectly. The design does not limit the use of these gates just to pass either logic 0 or logic 1, the gates are needed to pass a wide voltage ranges. Analog design procedure is used to implement these gates. The equivalent model of the transmission gate is shown in Fig. 2.15. , which consists the two resistors in parallel Rp (Resistance of a PFET) and Rn (Resistance of NFET).

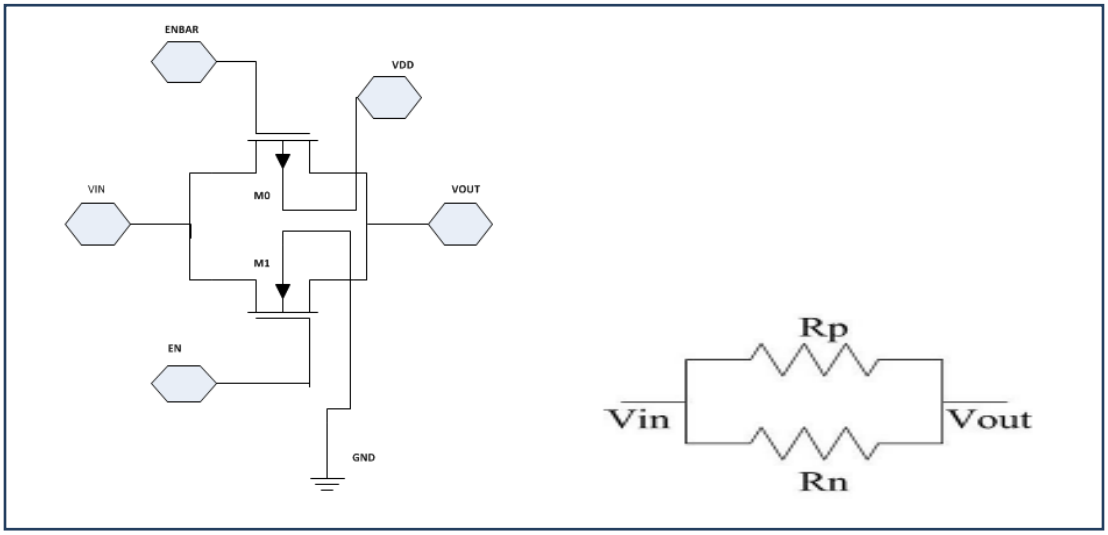


Fig. 2.15. Transmission Gate and its Equivalent Resistive Model

The equivalent resistance of the transmission gate is given by

$$\mathbf{Req = Rp||Rn} \qquad (2.8)$$

The ideal on state resistance of a CMOS transmission gate is zero whereas when the CMOS gate is ‘off’ the resistance is infinity, but the equivalent resistance of the transmission gate is not same as the ideal value. It keeps on changing depending upon the change in the supply voltage. The plot Ron Vs VDD illustrates the relationship between changes of on state resistance with supply voltage change.

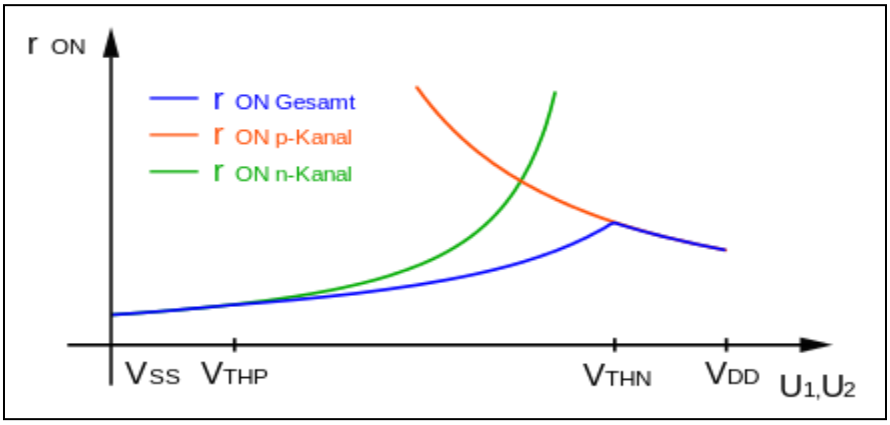


Fig. 2.16. On State Resistance of a Transmission Gate Versus Input Voltage [9]

The plot in the Fig. 2.16 indicated in green, red, blue are on state resistances of NFET, PFET, CMOS transmission gate respectively. The design of the transmission gate should be of minimum transistor sizes and also have as much low on state resistance as possible.

2.3.4 Operational Amplifiers (Designed by fellow students)

The operational amplifiers from the previous runs are used in the output stage of the DAC design. The main idea of the project is to design a DAC with rail to rail buffered output stage. The amplifiers are used in unity gain buffer configuration used to drive a resistive load or a large capacitive load. The op amps used in the design are p channel input op amp (sense low amplifier) and n channel input op amp. The ICMR of these op amps are 0 to 11.2 V and 4.7 to 14.58 V respectively. The topologies of both the op amps are shown below.

P Channel Input Op Amp (Sense Low Amplifier)

The sense low amplifier is designed to have a common mode range of min rail to the 11.2 V the design of this amplifier is based on the basic two stage operational amplifier with some modifications. The N channel input pair is replaced by P channel input pair and the PMOS load is replaced by NMOS current mirror load. An additional resistor and capacitor pair is added in between the stages to provide greater stability.

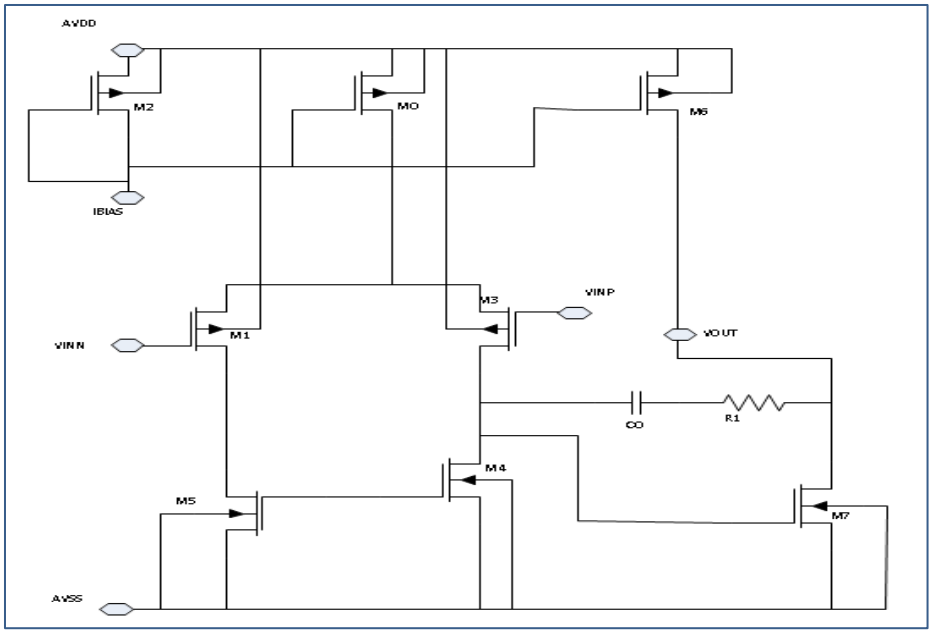


Fig.2.17. P Channel Input Two Stage Operational Amplifier

The design parameters of the op amp are given in Table 2.6 below.

Table 2.6. Design Parameters for N Channel Input Op Amp

Design parameter(Tested results)	
DC Gain	58.44
Phase margin	76.05
Gain bandwidth	1.395 MHz
ICMR	127.6mV – 10.7V

Slew rate	3.962 M

N- Channel Input Op Amp

This is a CMOS SiC based two stage operational amplifier. The first stage is a differential stage followed by the common-source amplifier output stage(second stage). An additional circuit is added between these stages for better stability and improved phase margin. The schematic is shown in the Fig. 2.18.[14]

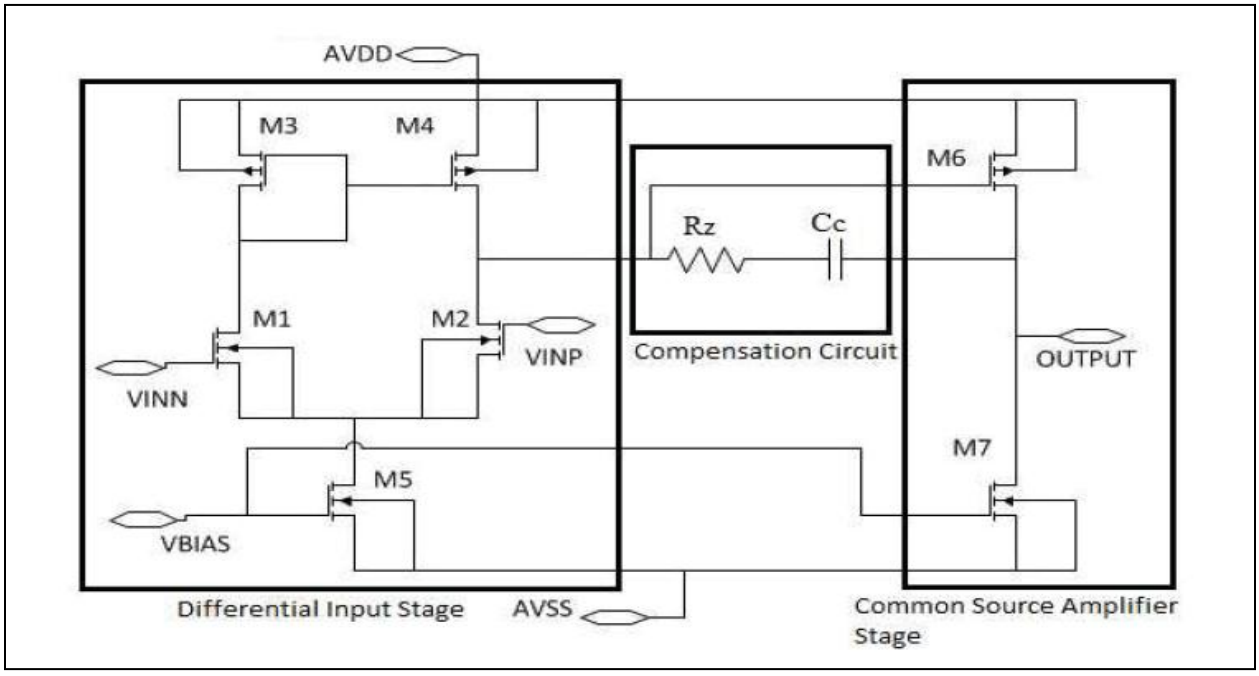


Fig.2.18. N channel Input Two Stage Operational Amplifier [11]

The design parameters of the N channel input trans-conductance amplifier is shown in Table.2.7.

Table.2.7. Design Parameters Two Stage Operational Amplifier

Design parameter(Tested results)	
DC Gain	74.29
Phase margin	40.65
Gain bandwidth	2.164 MHz
ICMR	4.7V – 14.58V
Slew rate	26.41 V/μs

3. SIMULATION

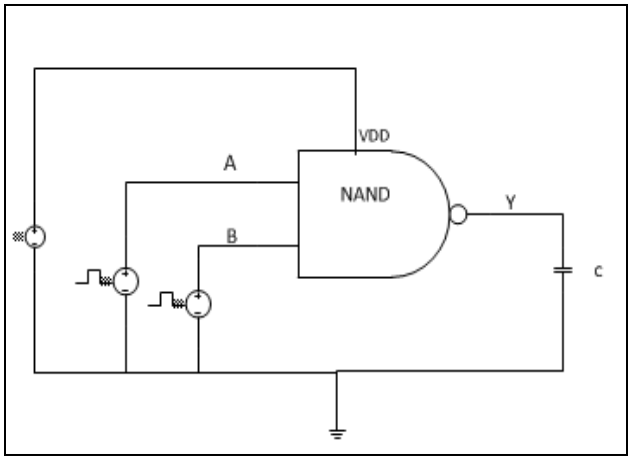
This is the most important step of the design process. The performance of the circuits is validated to match with the design specifications. Test benches are developed to verify the circuit characteristics performance over different process corners and the temperatures (25˚C to 275˚C). Most of the circuits of the design work well at the temperature range above 100˚C and below 200˚C. All the simulations are carried out at 25˚C with TT models. The simulations were run using HSPICE simulator. The models used for the design are BSIM4.

3.1 Digital Simulations

The digital simulations are performed to verify the performance characteristics of the digital blocks such as digital gates, flip flops and counter.

3.1.1 Digital Gates

The test bench for the basic two input NAND gate is given below in Fig. 3.1. The clock signals given to the input of the gate are of frequency 1 MHz and 500 kHz respectively and are in phase with each other. The size of the output load capacitor is chosen as 1 pF to emulate the largest fan-out of any gate expected to encounter. The basic idea is to design the digital gates with the rise and fall times less than 20 ns and with as small delay as possible.



Design Parameters	
Rise time	18ns
Fall time	19 ns

Fig. 3.1 Test Bench for 2 Input NAND Gate

The plot given in Fig. 3.2 shows the NAND gate output and the corresponding input voltages. The rise time and fall times is observed to be 18 and 19 nanoseconds respectively.

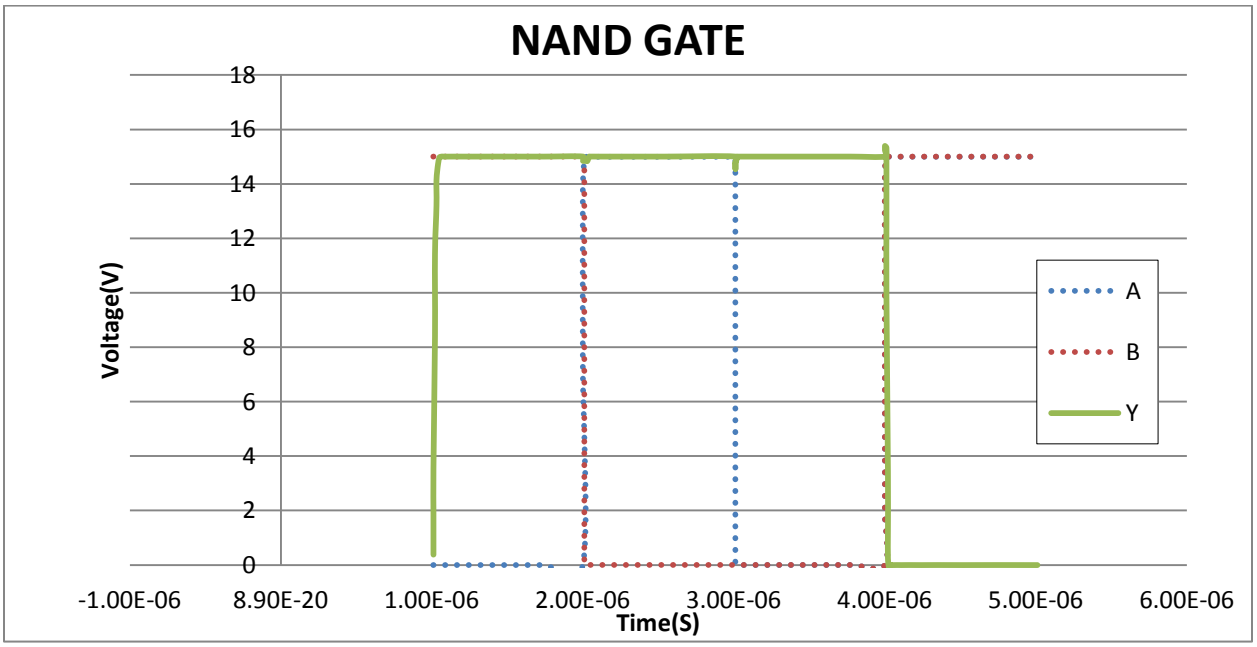


Fig. 3.2 NAND Gate Functionality

3.1.2 JK Flip Flop

This is the most crucial part of the counter. The test bench for the flip flop is given in Fig. 3.3. The pulses are given to the input port J and K to verify all the states of the flip-flop. It is a positive edge triggered flip-flop, the output changes whenever the clock goes high. The pulse inputs used are of 1 MHz frequency and the load capacitance is chosen to be 1 pF.

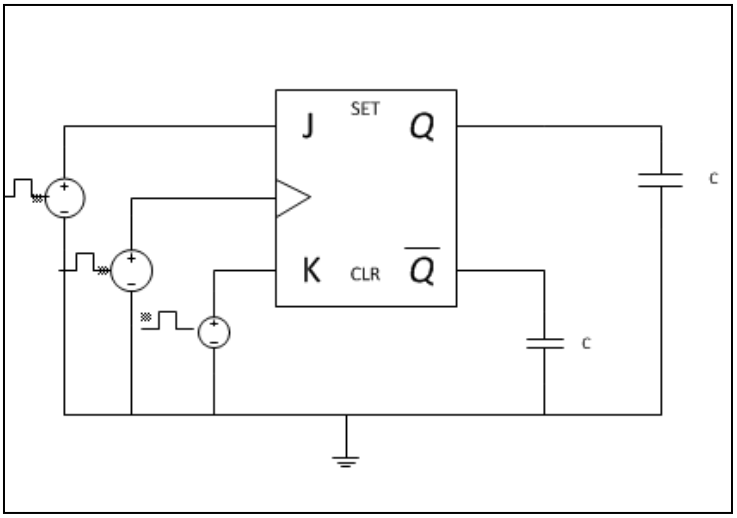


Fig. 3.3. Test bench for JK Flip Flop

The Fig. 3.4 shows the transient characteristics of the JK flip flop. The figure indicates the plot of the inputs and the corresponding output states of the JK flip flop.

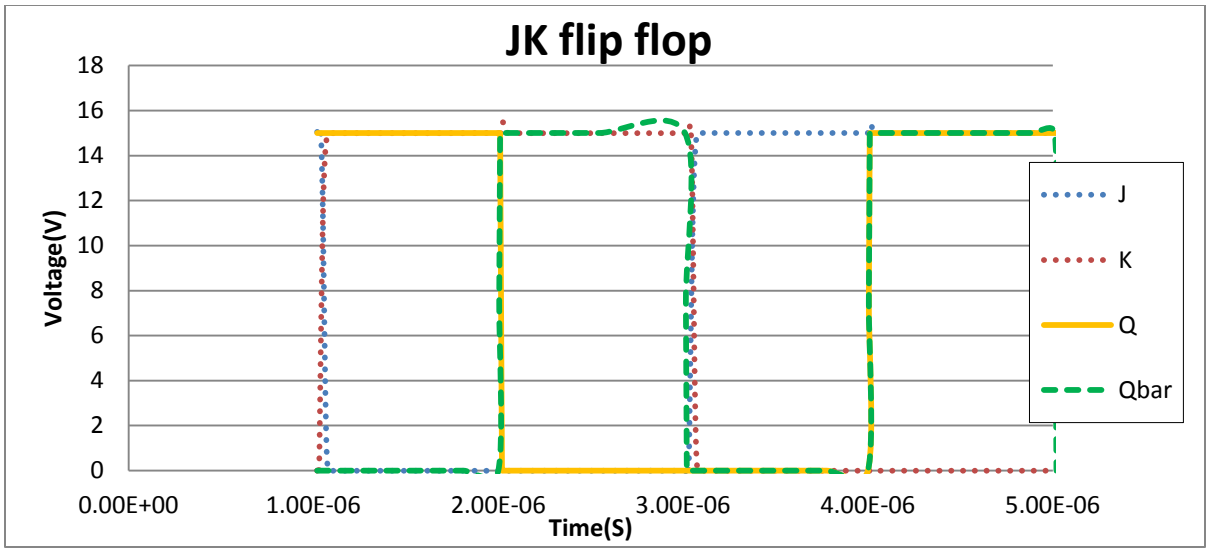


Fig. 3.4 JK Flip Flop Functionality

3.1.3 Counter

The functionality of the basic building blocks of counter is verified. The next step in the design process is to verify the counter circuit as a whole. The counter designed is an 8 bit synchronous up counter. The counter is designed to create the test bench for the charge scaling DAC with works at a frequency of 1MHz. The counter provides an output pulse frequency of 1 MHz. The frequency of the output pulse can be changed when needed by changing the frequency of the clock signal input. The test bench for the counter is shown in Fig. 3.5. A voltage of logic 1 is applied to J and K inputs, the output toggles for every clock cycle. The frequency of the pulse given to the clk input is 2 MHz and the load capacitance is 1 pF. The simulation results are shown in the Fig. 3.6.

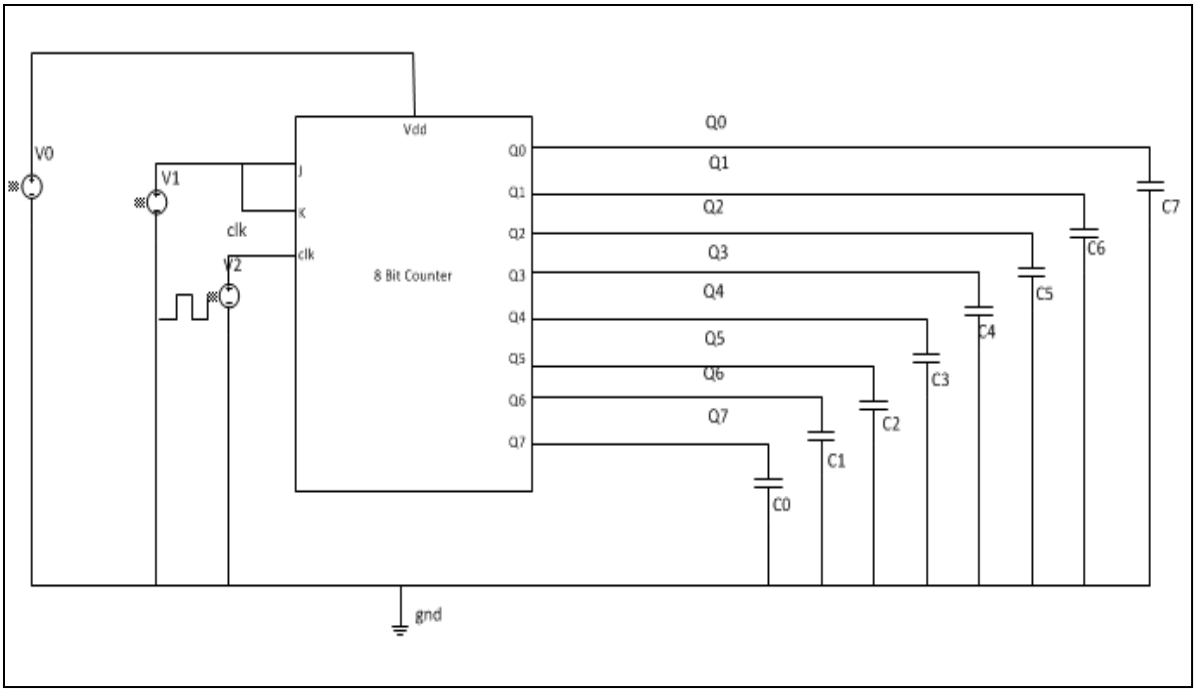
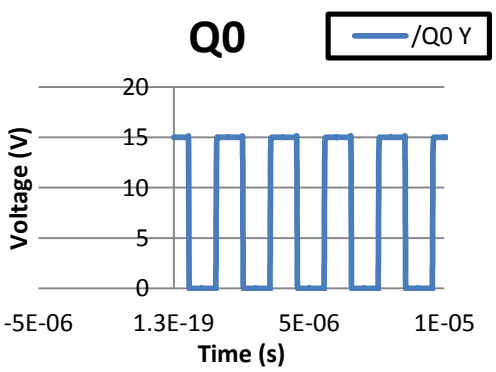
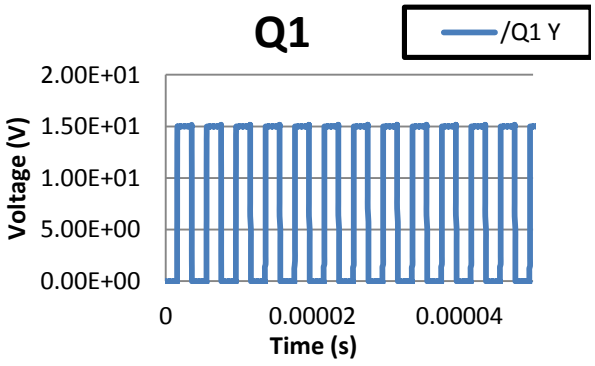


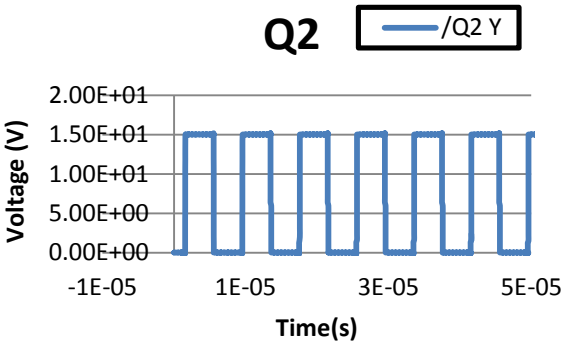
Fig. 3.5 Counter Test Bench



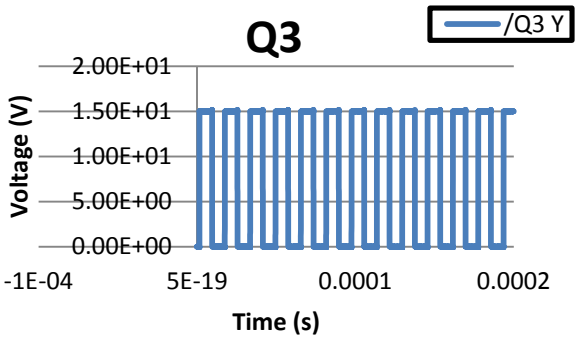
(a)



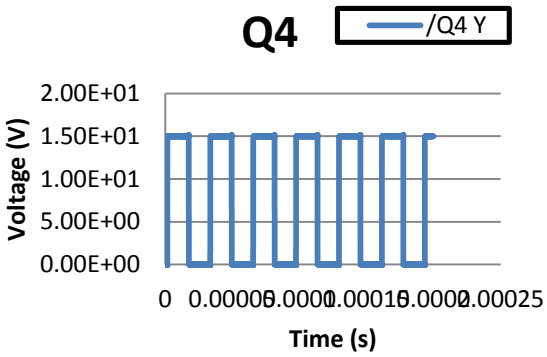
(b)


Q2
/Q2 Y
2.00E+01
1.50E+01
1.00E+01
5.00E+00
0.00E+00
Voltage (V)
-1E-05
1E-05
3E-05
5E-05
Time(s)

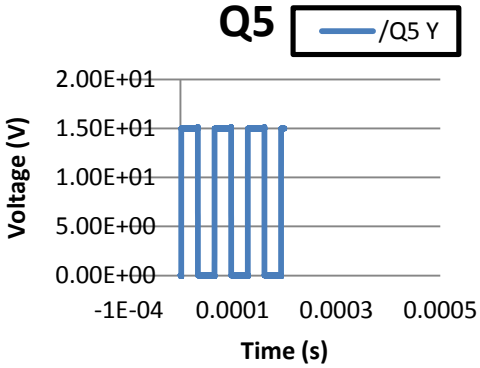
(c)


Q3
/Q3 Y
2.00E+01
1.50E+01
1.00E+01
5.00E+00
0.00E+00
Voltage (V)
-1E-04
5E-19
0.0001
0.0002
Time (s)

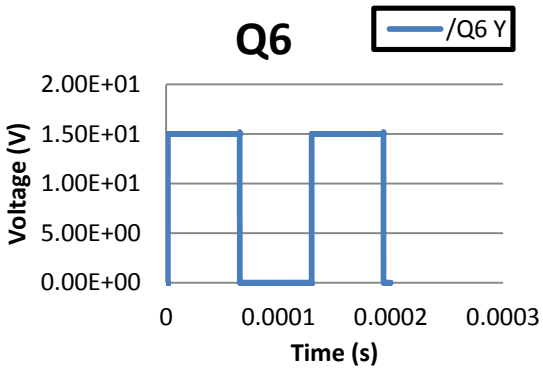
(d)


Q4
/Q4 Y
2.00E+01
1.50E+01
1.00E+01
5.00E+00
0.00E+00
Voltage (V)
0
0.00005
0.00015
0.0002
0.00025
Time (s)

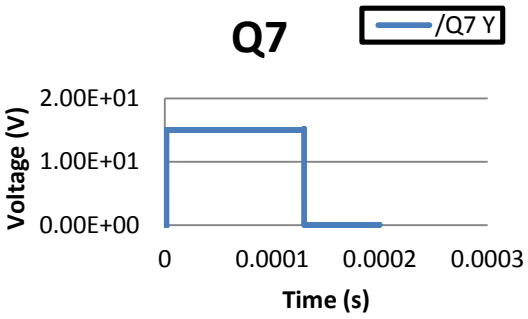
(e)


Q5
/Q5 Y
2.00E+01
1.50E+01
1.00E+01
5.00E+00
0.00E+00
Voltage (V)
-1E-04
0.0001
0.0003
0.0005
Time (s)

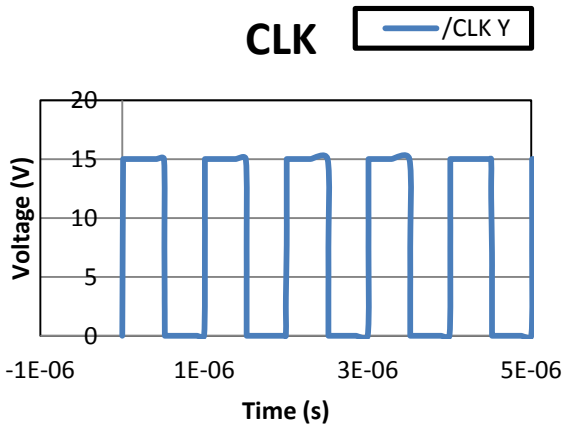
(f)


Q6
/Q6 Y
2.00E+01
1.50E+01
1.00E+01
5.00E+00
0.00E+00
Voltage (V)
0
0.0001
0.0002
0.0003
Time (s)

(g)


Q7
/Q7 Y
2.00E+01
1.00E+01
0.00E+00
Voltage (V)
0
0.0001
0.0002
0.0003
Time (s)

(h)



(i)

Fig. 3.6 Counter Output Bit Sequence

The Table 3.1 provides the details about raise and fall times of the output pulse and also the design parameters of the circuit as a whole.

Table.3.1. Design Parameters of Counter

Design Parameters	
Trise of output pulse	20 ns
Tfall of output pulse	16 ns
VDD	15 V
Power consumption	80m W

3.1.4 Digital Buffer

The test setup for the transient response of the digital buffer is given in the Fig. 3.7. The input pulse is of the frequency 1MHz and the load capacitance is 1 pF.

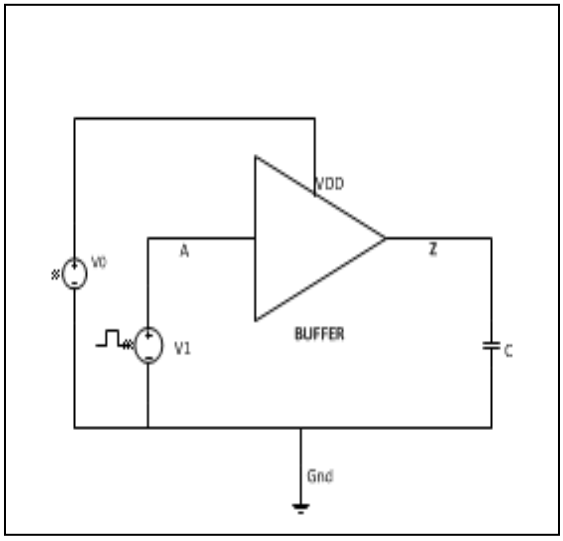


Fig. 3.7 Digital Buffer Test Bench

The Table 3.2 shows the buffer characteristics such as driving capability, rise, fall and delay times.

Table.3.2. Digital Buffer Design Parameters

Design parameters	
Trise	21 ns
Tfall	19 ns

delay	14ns
Cload/ Cin	16

The plot shown in Fig. 3.8 provides the digital buffer characteristics. The rise, fall and delay times of the buffer circuit are 21, 19 and 14 ns respectively.

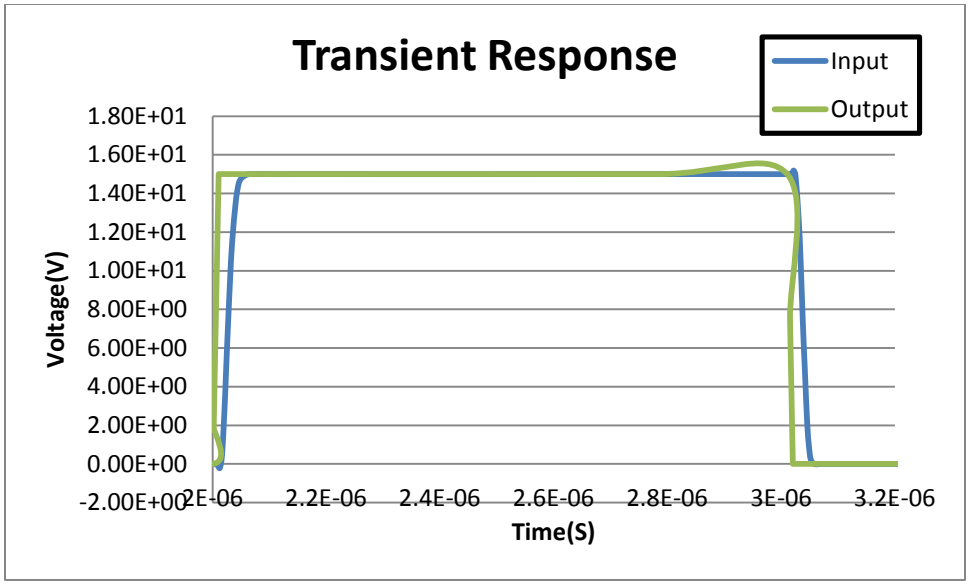


Fig. 3.8 Digital Buffer Transient Response

3.2 Analog Simulations

This section consists of the verification of analog portion of the system. The validation of blocks such as the capacitor chain, Schmitt trigger and operational amplifiers is performed here.

3.2.1 Charge Scaling DAC

Charge scaling DAC is the core block of the design. The Fig. 3.8 below shows the test setup for the DAC, eight pulse sources are taken with varying frequencies to get a bit pattern that starts from 00000000 and counts till 11111111. A transient simulation is run with start and stop times of 0 and 256 µs and with a step size of 100 nanoseconds.

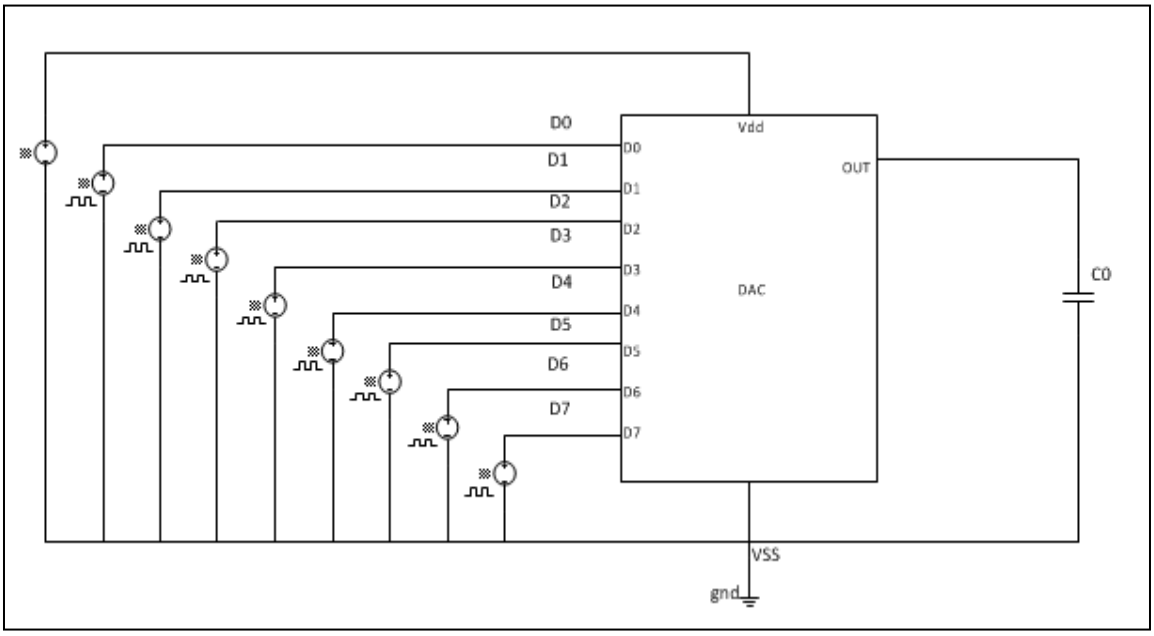


Fig. 3.8 Test Bench Setup for DAC

The Fig. 3.9 shows the full scale output ramp of the DAC, it starts from 0V and reaches 14.49 V. The DAC has an offset of 0.05 mV which is almost negligible. The spikes are caused during the charging and the discharging phases of the capacitors can be eliminated by an output buffer. As all the circuits are integrated together the input to the capacitor chain stops generating

sequence at frequency of 3.5 MHz which makes capacitor chain output deviates from its general behavior.

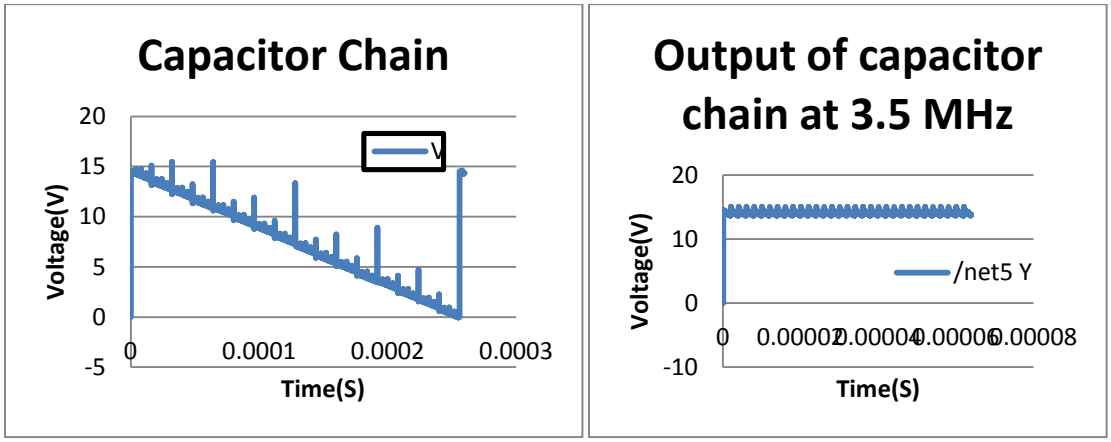


Fig. 3.9 DAC Full Scale Ramp

3.2.2 Schmitt Trigger

The Schmitt triggers are used to provide switching voltages to turn transmission gates on/ off which determines the switching between the op amps.

DC response

The Fig. 3.10 shows the test setup for the DC response characteristics of the Schmitt trigger. The input DC voltage is swept from 0 to 15 V with a step increment of 1 V and the corresponding output voltage is plotted as shown in the Fig. 3.11 which helps to determine the lower switching point. The input DC voltage is sweep from 15 to 0 V which helps to determine the upper switching point.

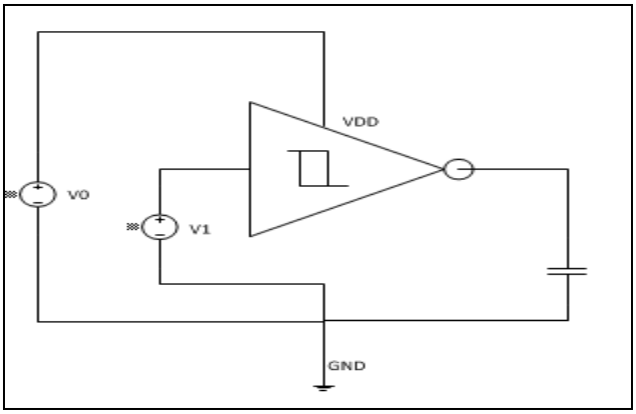


Fig. 3.10. Test Bench Set Up to Determine Hysteresis Width

The Fig. 3.11 below shows the DC characterization to determine the hysteresis width, and it is observed to be 2V with an upper and lower switching point voltages as 8 and 6 V respectively.

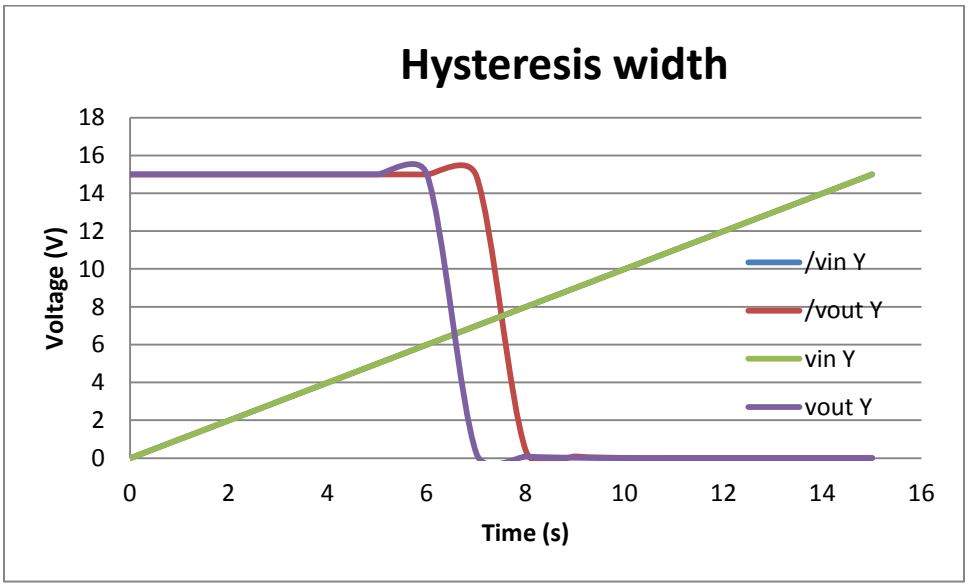


Fig. 3.11. Hysteresis Width

Transient Response

The transient response of the Schmitt trigger helps us to determine the rise, fall and the delay times of the circuit, it also gives information about slew rate. The transient response test bench setup is shown in the Fig. 3.12. The input to the circuit is a pulse wave of frequency 1 MHz and the load capacitance is 1 pF. The Fig. 3.13 gives the transient performance characteristics of the circuit. The rise and fall times of the Schmitt trigger are found to be 8 and 9ns respectively.

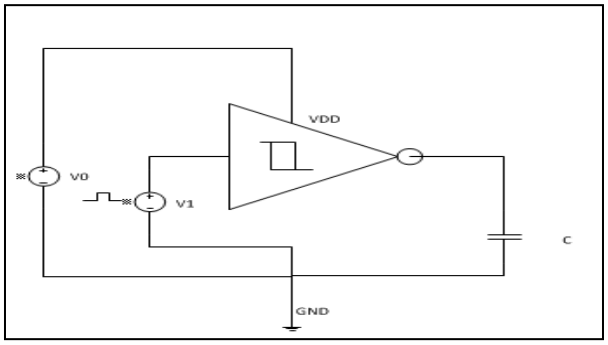


Fig. 3.12. Test Setup for Transient Response Characteristics

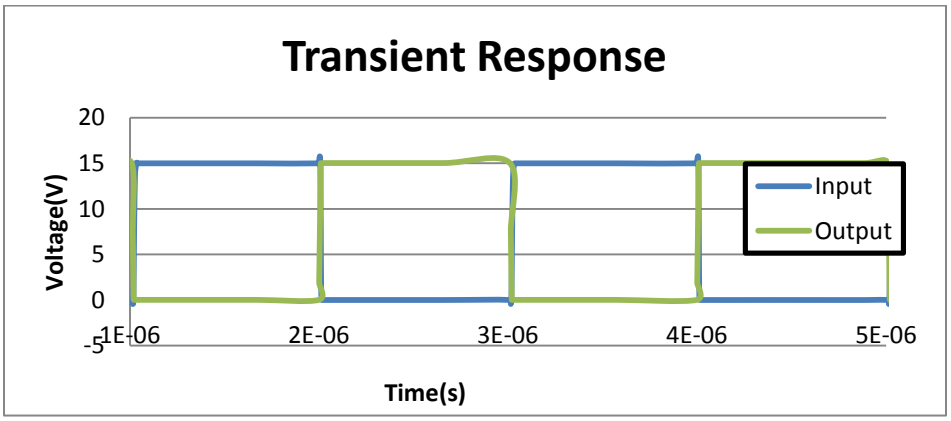


Fig. 3.13. Transient Response

The Table 3.3 shows the design parameters of the modified Schmitt trigger circuits and also the design parameters for the prior Schmitt trigger.

Table.3.3. Design Parameters of Schmitt Trigger

	Modified Schmitt trigger 1	Modified Schmitt trigger 2	Basic Schmitt trigger	unit
Upper switching point	**6**	**5**	**5.4**	**V**
Lower switching point	**8**	**7**	**9.2**	**V**
Rise time	**8**	**7**	**196**	**ns**
Fall time	**9**	**10**	**131**	**ns**
Power consumption	**7.5**	**15**	**0.89**	**mW**
Slew rate	**396**	**265**	**80.6**	**V/μs**

3.2.3 Operation Amplifiers

Two op amps in voltage follower configuration are used at output stage of charge scaling DAC. The circuits were designed by the fellow students in the previous run using the BSIM3 models. In the current design more emphasis is given to the ICMR of the op amps. The Figs. 3.14 and 3.15 Show the ICMR test benches for the two op amps used in the design. Simulations are done using the BSIM4 models. The input common mode ranges of the two op amp circuits used are given in the Table3.6.

Table.3.4. ICMR of Operational Amplifiers

	BSIM3	**BSIM4**
N Channel input two stage amplifier	4.7 – 14.7 V	5.2- 11.1 V
P channel input two stage amplifer	127.6m – 10.7 V	127.6m – 9.7 V

Fig. 3.14. shows the test setup configuration for finding ICMR. Here the op amp is a voltage – follower configuration. The current bias is 100μA sinking current and the supply voltage is 15 V. In the voltage follower configuration the output of the amplifier is connected with the negative input. This forces the output to be equal to the input. The minimum ICMR is found to be 127.6m V and the maximum ICMR is found to be 9.7 V.

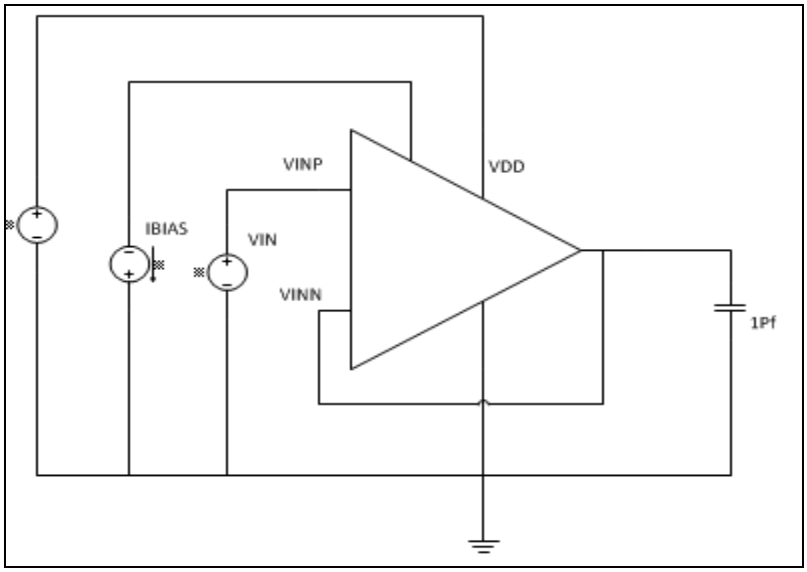


Fig. 3.14 ICMR Test Setup for P Channel Input Op Amp

From the Fig. 3.15 it can be inferred that the output voltage is equal to the input voltage until the input voltage reaches a value of 9.7 V, after this point the operational amplifier no longer acts as a unity gain buffer, Vin is not equal to Vout. This is due to the higher threshold voltages of PMOS transistors.

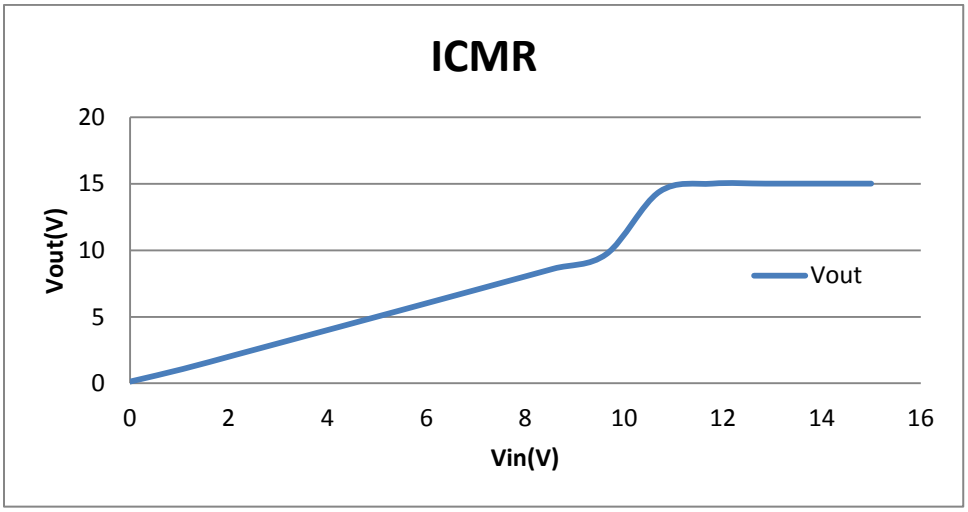


Fig. 3.15 ICMR Plot for P Channel Input Op Amp

Fig. 3.16 shows the test bench setup to determine ICMR of the op amp. This op amp is designed in the Raytheon tape out 1 using the SiC process. The bias voltage is set to 3.5 V and the DC voltage sweep is applied as the input to the circuit and it is determined that the op amp acts as the voltage follower circuit within the range 4.7 (min ICMR) to 14.5 (max ICMR).

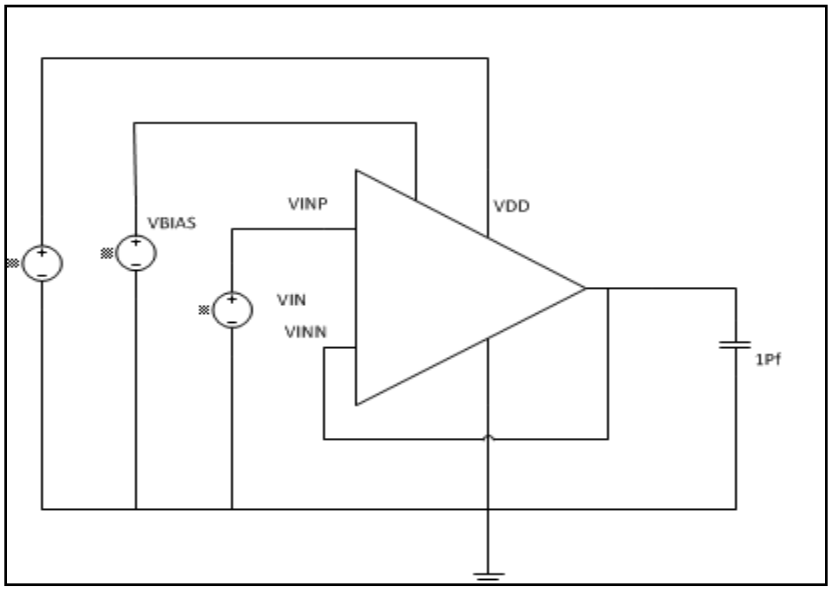


Fig. 3.16 ICMR Test Setup for N Channel Input Op Amp

The Fig. 3.17 shows the plot of input voltage vs the corresponding voltage and also the supply current. This data is useful to determine the ICMR and the total DC power consumption of the op amp.

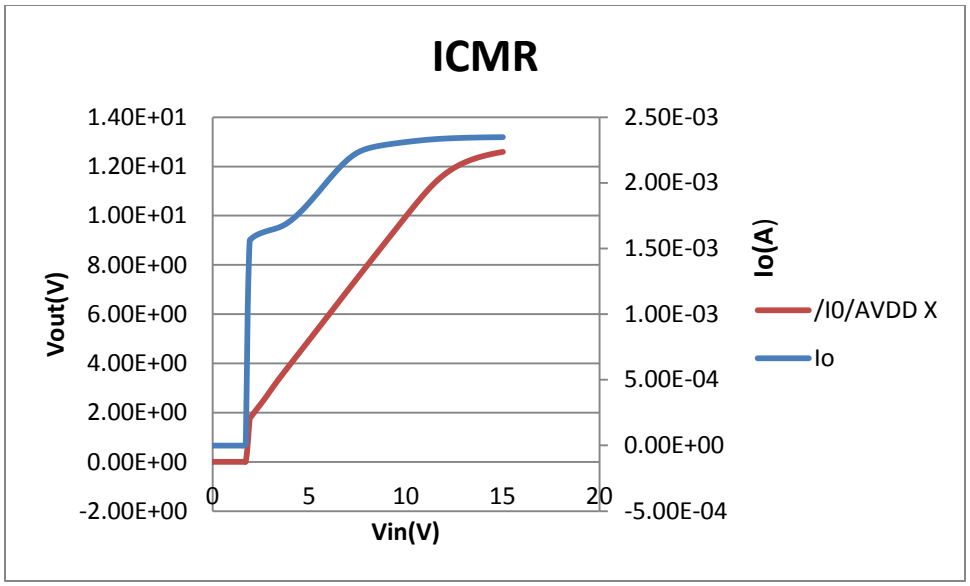


Fig. 3.17 ICMR Plot for N Channel Input Op Amp

The circuits are designed using BSIM4 models, these models have higher thresholds for the PMOS which decreased the ICMR of the circuits when compared to the ICMR of the amplifiers simulated using BSIM3 models.

3.3 DAC Integrated Circuit

After all the individual blocks are validated, the final step is the implementation process. Fig. 3.18 shown below is the test bench configuration for the full circuit. The input to the counter is a clock pulse of frequency 500 kHz, the counter produce the sequence of bits from 00000000 to 11111111. The capacitor chain converts these input bits into corresponding output. This output is further filtered by the op amps at the output stage.

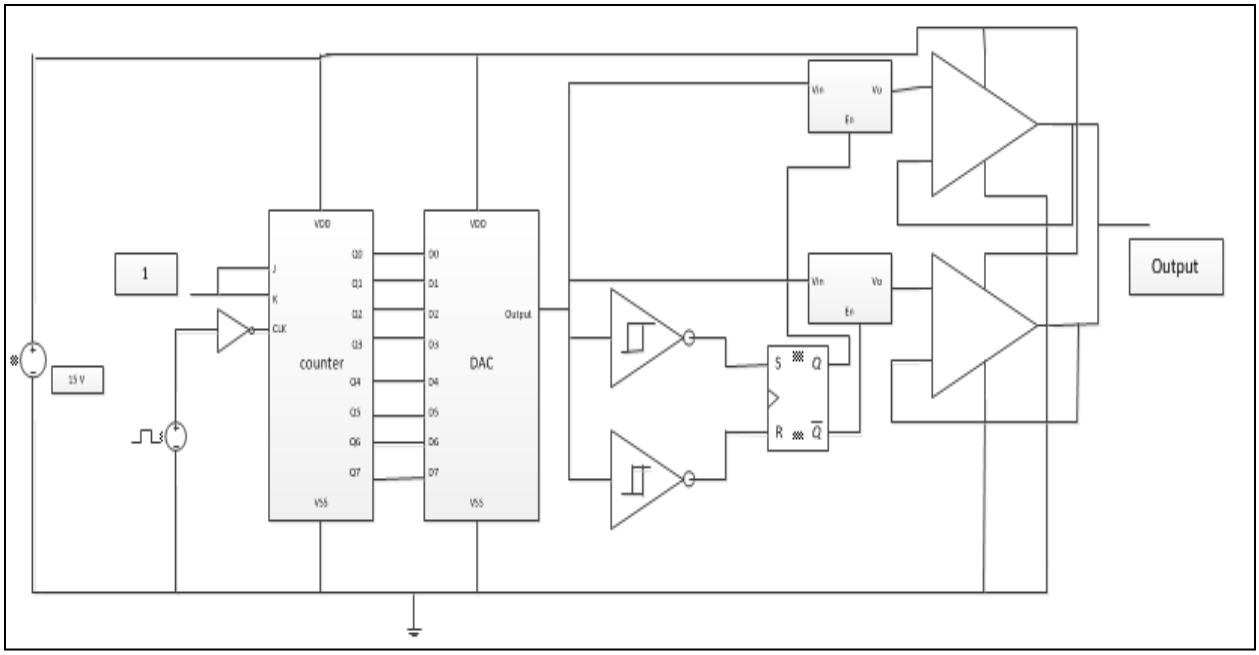


Fig. 3.18. DAC Circuit with Output Buffer

The Fig. 3.19 below is the plot of output digital voltage with respect to time. The graph is plotted on a time scale of range 0 to 255 µs, each µs corresponds to a digital input starting from 00000000 to 11111111.

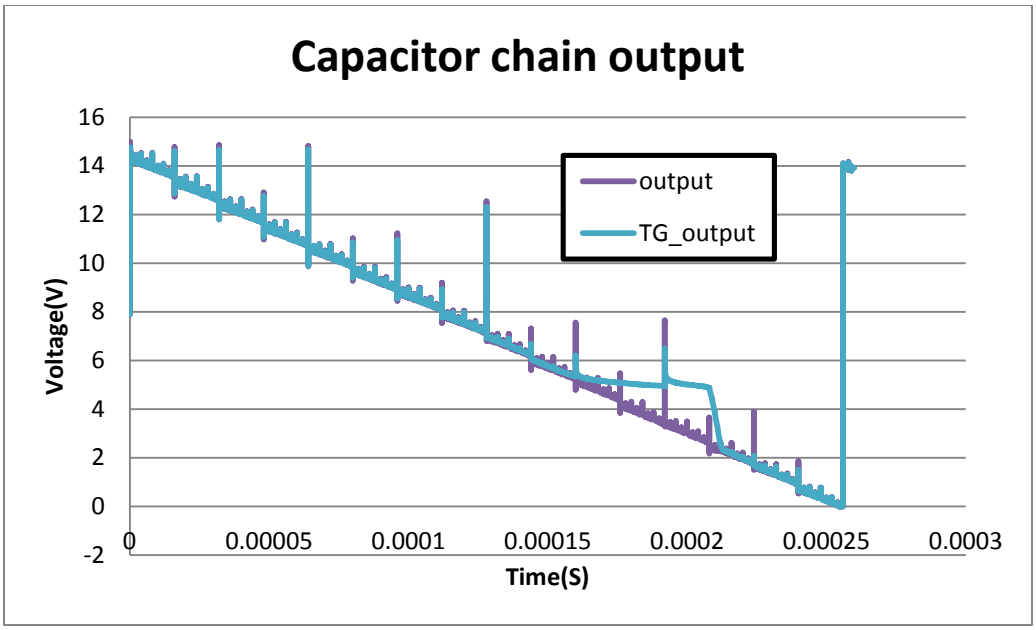


Fig. 3.19 Full Scale Output Ramp Through TG

From the plot in the Fig. 3.19 it is seen that there is a distortion in the output voltage when the ramp is passed through a transmission gate. This is caused due to the high on-state resistance of the transmission gate when one transistor is partially on and the other is partially off. Due to the high threshold of the BSIM4 transistor models the on-state resistance of the transmission gate is found to be 3.2 GΩ when the input is 7.5 V. The Fig. 3.21 shows the plot of transmission gate on state resistance versus input voltage.

Transmission gate

The figure below shows the test bench setup for determining the transmission gate on state resistance. DC voltage is supplied as the input to the transmission gate. The input voltage is swept from 0 to 15 V. The value of the output voltage V3 is set to 7 V, drain – source current is measured and the value of on state resistance is calculated by using the equation provided below

$$Rds(on) = Vds/ Ids \quad (3.1)$$

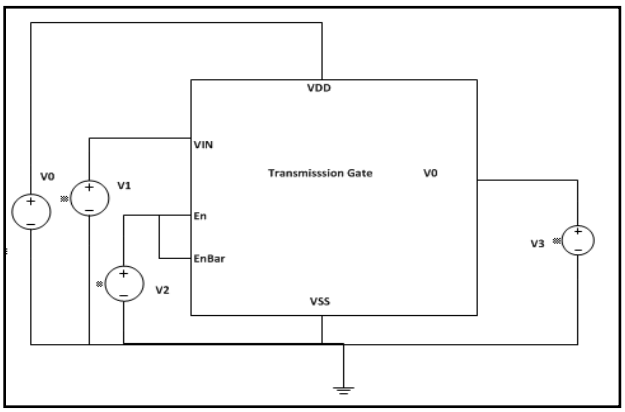


Fig. 3.20. On State Resistance Test Setup for TG

The plot in the Fig. 3.21 determines transmission gate on state resistance for the corresponding input voltage. From the plot it can be inferred that the on state resistance is very high when the input voltage is 7.5 V, this causes the output to be distorted when a ramp is passed through the transmission gate.

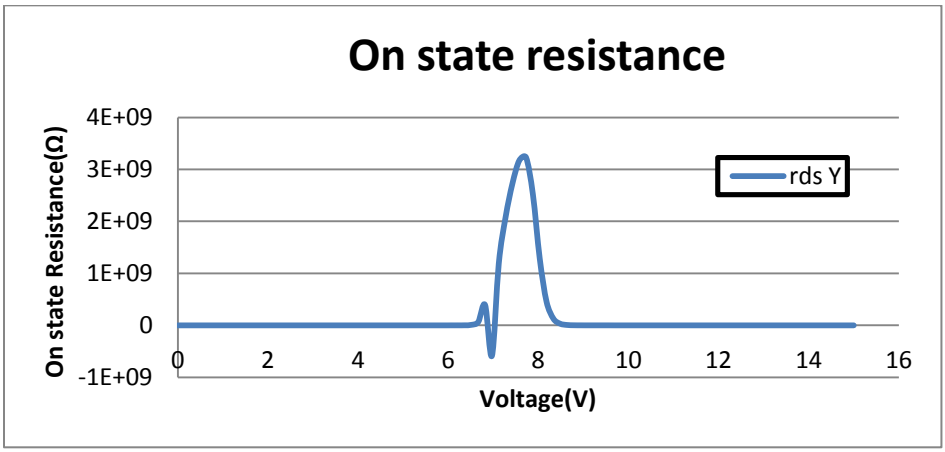


Fig. 3.21 On State Resistance Vs Input Voltage

3.3.1 Modified Design Topology

From Fig. 3.19 it can be seen that when a ramping voltage is passed through the transmission gate it gets distorted at the output. The circuit is modified as shown in Fig. 3.22 in which the transmission gates are used to control the switching between the op amps rather than passing the signal through it. The Schmitt trigger control the on/ off state of the TGs which in turn turns the op amps on/off.

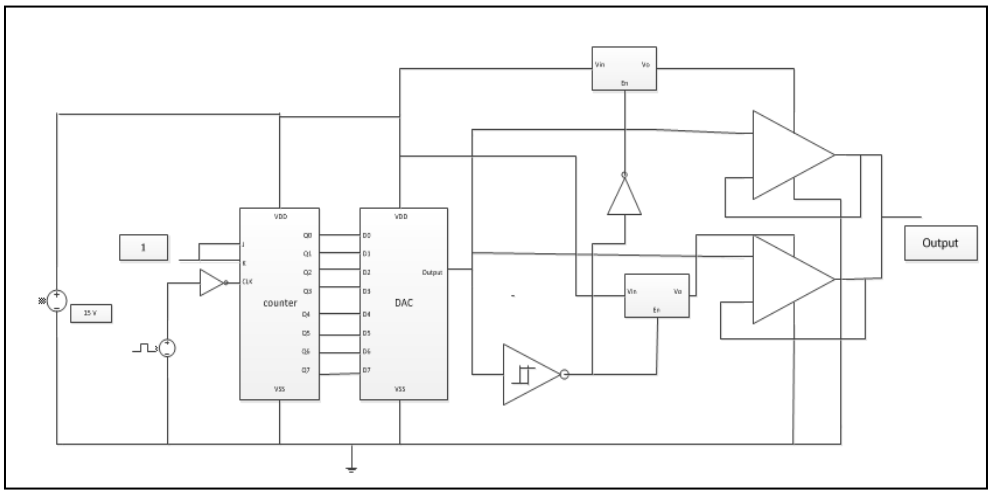


Fig. 3.22. Modified Topology I

The Fig. 3.23 is same as the modified topology except for TGs are replace by digital buffers and supply voltage to the op amps is determined by the Schmitt trigger high/ low switching voltage levels.

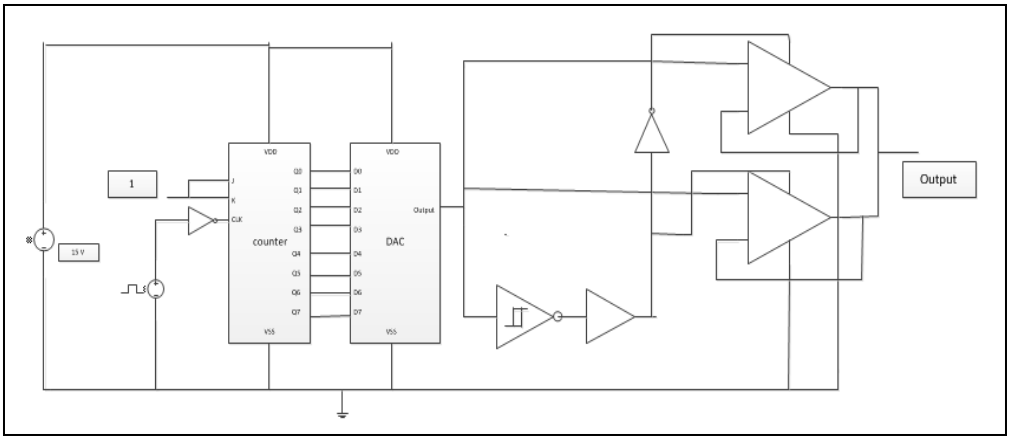


Fig. 3.23. Modified Topology II

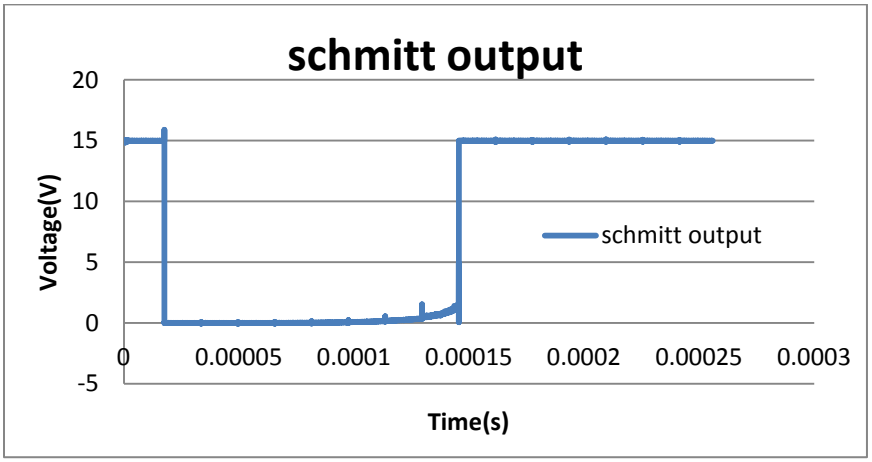


Fig. 3.24. Output of Schmitt trigger switching at 6V

The Fig. 3.25 is the buffer output of the DAC. The graph marked in red is when the P-channel input op amp is acting as the voltage buffer, N- channel input op amp is off and the plot which is marked in blue is when the N- channel input op amp is acting as the voltage buffer, P-channel input op amp is off. The transition between the op amps is made 6 V. This is voltage that is common in the ICMR of both the op amps.

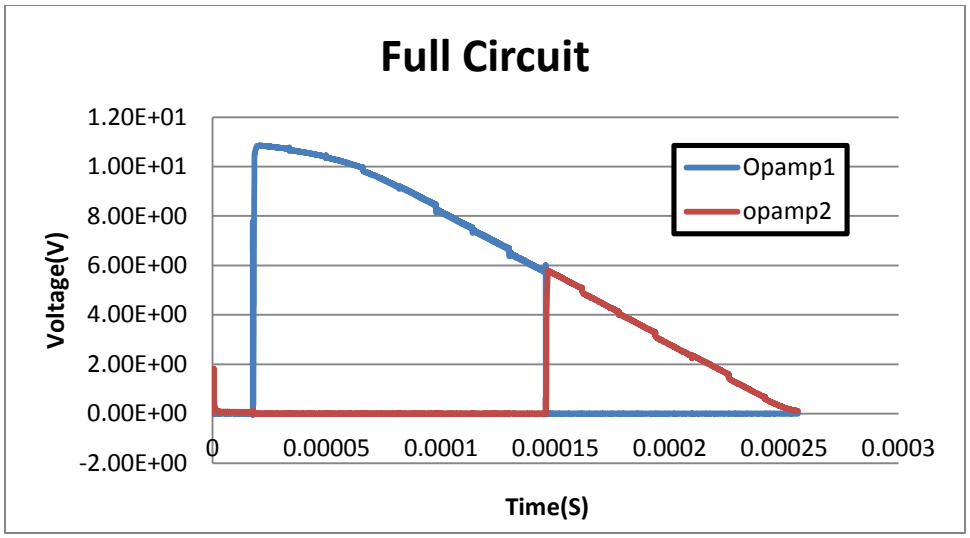


Fig. 3.25. DAC Buffered Output

3.3.2 Error Checking

The verification of the DAC functionality is validated using two error checking methods INL and DNL.

DNL (Differential Non Linearity)

To determine the DNL error the output is sampled at the switching points for 256 steps. Once the waveform is acquired it is compared with the ideal waveform switching points and the difference per step between the two waveforms gives the resulting DNL. The resolution of the DAC is 0 to 14.5 over 256 steps resulting in a step size 0.056V. Fig.3.26 shows the DNL error versus the corresponding digital input code. The output range of the op-amp is between 126.7 m V to 10.3 V. The worst case DNL is found to be 3.5 LSBs. The DNL is given by the equation

$$\text{Differential nonlinearity (DNL)} = (Vcx - Vs/Vs) \times 100\% = (Vcx/Vs - 1)\ \text{LSBs} \quad (3.2)$$

Where Vs is the ideal change and is given by, $Vs = Vfsr/ 2^N$,Vcx is the actual change in voltage on a bit to bit basics

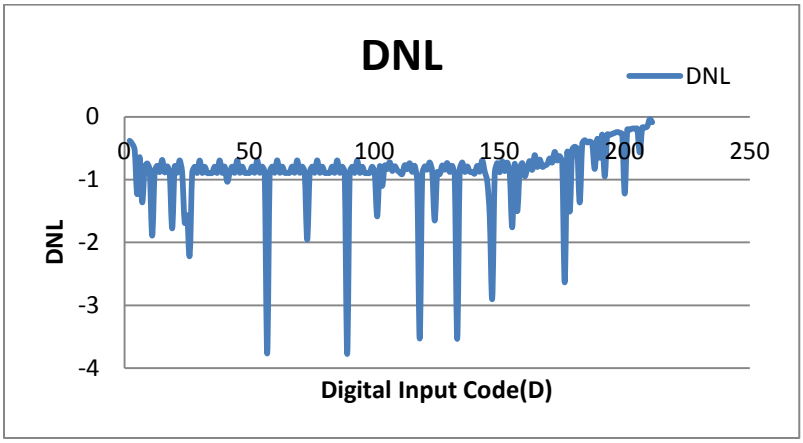


Fig. 3.26. DNL error

INL (Integral Non Linearity)

Fig. 3.26 shows the INL error versus the corresponding digital input code. INL observes the error over the full scale range, opposed to step by step. The INL error can be determined by the deviation over the full scale range of the simulation data as compared to an ideal best fit line. Fig.3.27 shows the plot of simulated values and ideal best fit line over the time scale. The output range of the op-amp is between 126.7 m V to 10.3 V. The worst case INL is observed to be 0.37 V.

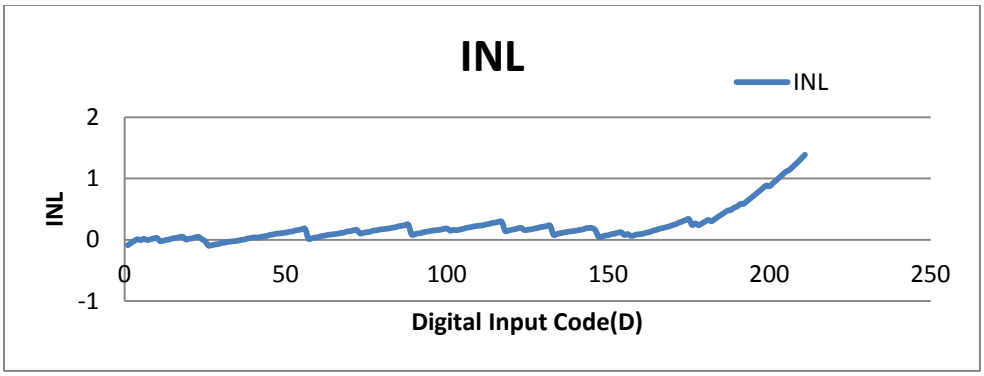


Fig. 3.27. INL error

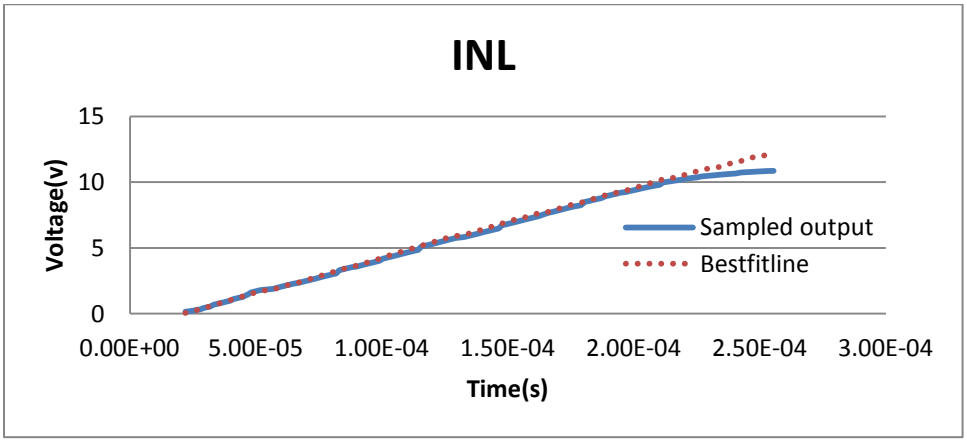


Fig. 3.28. Calculation of INL using Best fit line Method

4. PHYSICAL DESIGN

The performance of the circuit can be varied based of the physical design, IC layout or mask design. The IC layout is the representation of the integrated circuit components in the form of geometric shapes which represents the fabrication layers of the circuit's components. After the layout verification is completed, it is converted into a standard format (GDS II), and sent out for fabrication. It is always important to consider the effects of layout on the design system.

Table 4.1. Layer Map

Blue	Metal 1
Red	Polysilion
Green/ yellow	Pdiff/Ndiff(Active Region)
Dark yellow	Contacts

The performance and precision directly depend on the matching of devices. Layout designers should be more cautious while doing physical design and always keep in mind about the mismatches that might hinder the proper functioning of the circuit. There are many causes of mismatches like microscopic fluctuations in dimensions, doping, oxide thickness and other parameters which affect the component values. Though mismatches can't be eliminated completely, the design can be made in such a way that, it will have a limited variation.

Table 4.2. Layout rules for basic layers

Minimum metal width	2.4 µM
Minimum metal spacing	1.2 µM
DPoly to Dpoly spacing	1.6 µM
Dpoly2 to Dpoly2	1.4 µM
Minimum Poly width	2.2 µM

4.1 Digital Layout

The layout of digital blocks used in the DAC is discussed in this section.

4.1.1 Compact Layout Style

Digital Layout is simple when compared to analog, as it has complementary (CMOS) gates and are symmetrical. All the gates are constructed using cadence Layout suite version IC6 and the verification was executed in caliber. The layout procedure is explained using the design of a unit inverter with the width of PFET is twice of NFET. The layout of the complex digital gates is executed in 5 steps as shown.

Y = A nand B

1) Label all the nodes

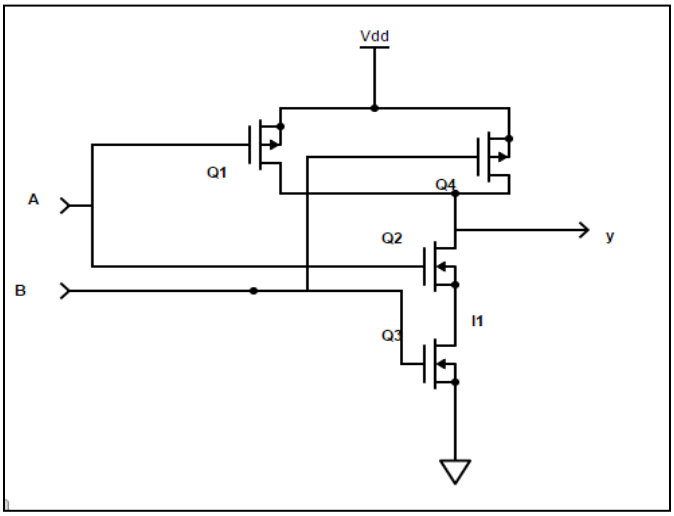
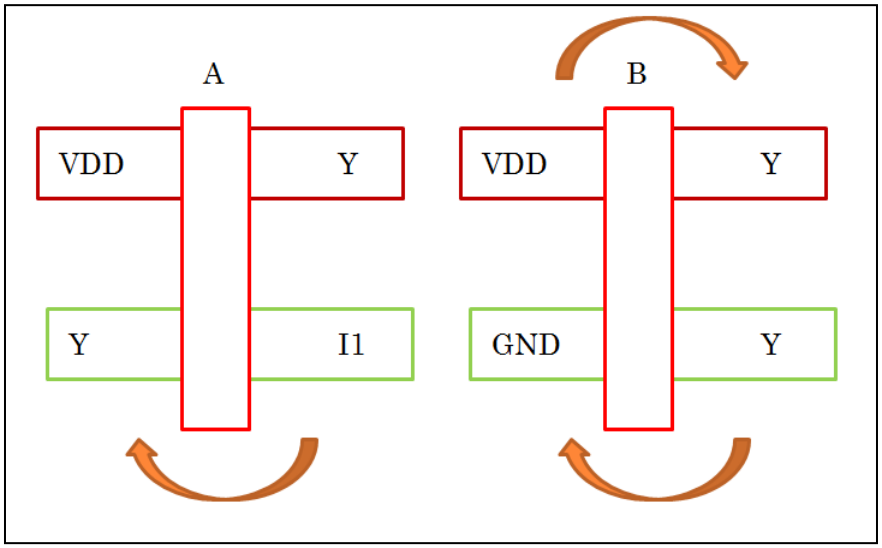


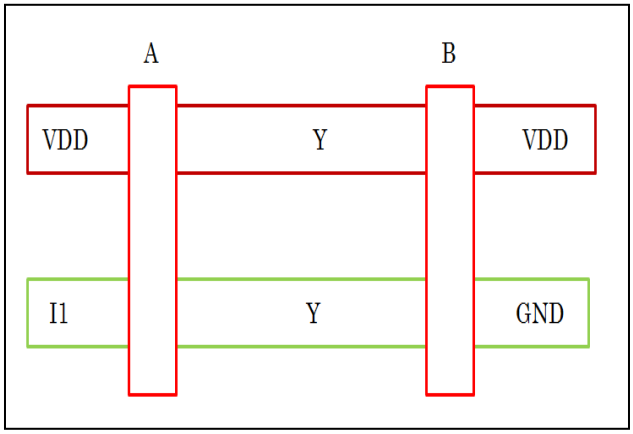
Fig. 4.1. Two Input NAND Gate Schematic

2) Make transistors crudely and label their connections, use the symbolic diagram or stick diagram.



3) Some wires can be eliminated by flipping transistors. Many redundant connections can be removed by abutment.

4) Draw the final layout except NWELL, substrate contacts.



5) Make the connections between the transistors with the metal layers and poly layers.

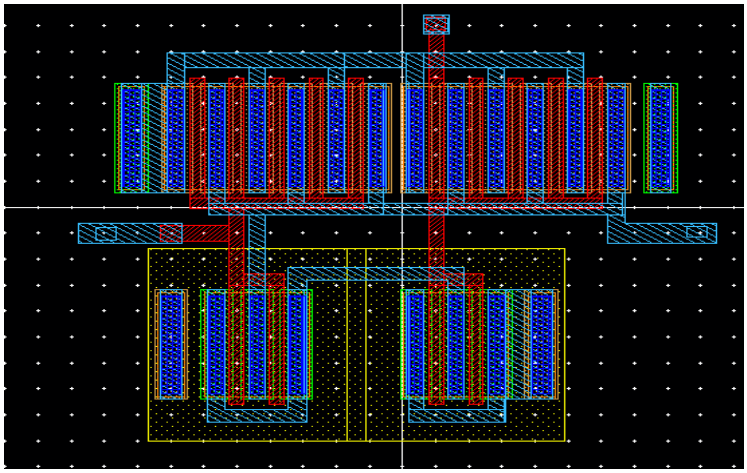


Fig. 4.2. NAND Gate Physical Design

6) Check the layout. Perform LVS, DRC and parasitic extraction.

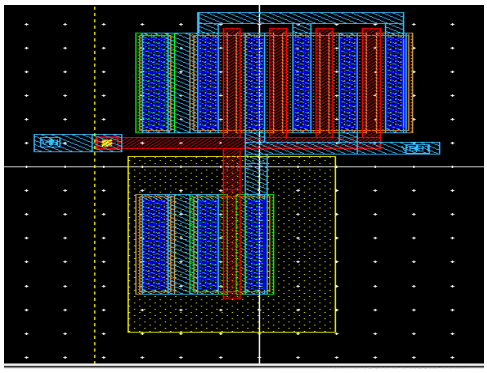
4.1.2 Counter Layout

The counter is the important circuit in the design of test bench for the charge scaling DAC. The counter is comprised of all the basic sub blocks designed under digital circuit library. Table 5.3 shows the digital cells used in the design of the 8 bit counter.

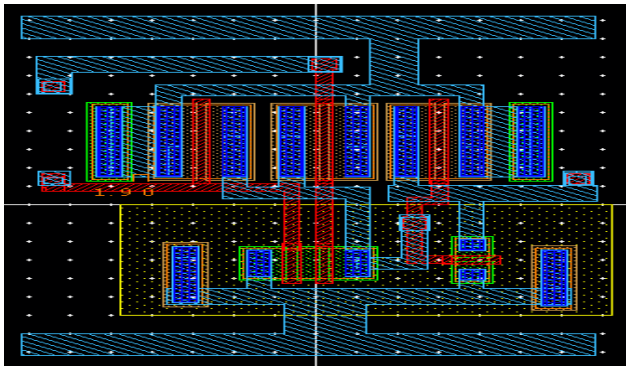
Table 4.3. Sub Blocks of Counter

Gate Name
Inverter
2- input NAND gate
3 Input NAND gate
2- Input AND gate
JK flip flop

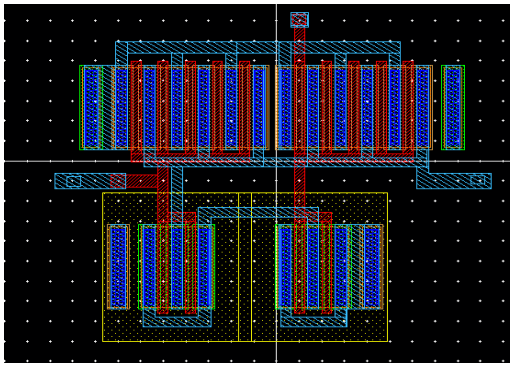
The Fig. 4.3, 4.4 shows the layout of the sub blocks and the counter as a whole.



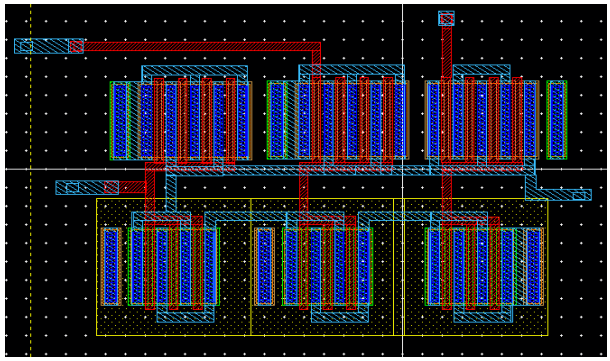
(a)



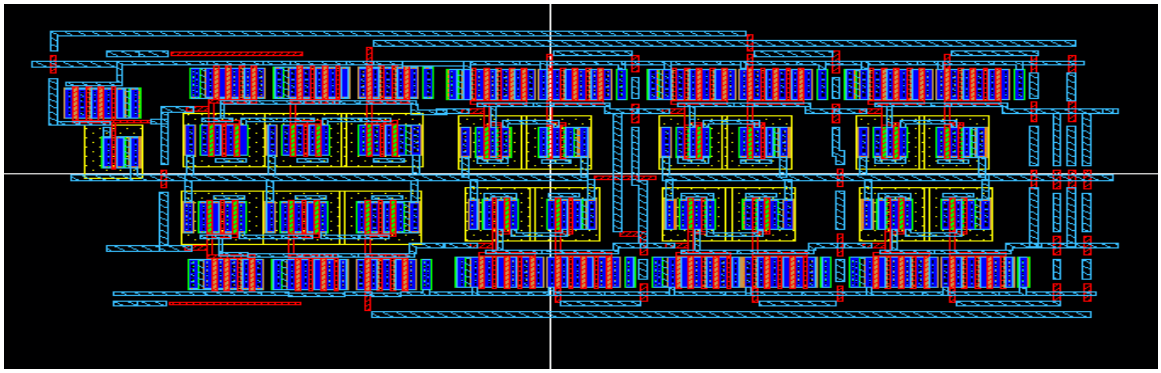
(b)



(C)



(d)



(e)

Fig. 4.3. Physical Design of (a) Inverter (b) 2 Input AND (c) 2 Input NAND (d) 3 input NAND (e) JK Flip Flop

The design idea of behind the counter is to make it as compact as possible. The physical design of the counter is shown in Fig. 4.4. The aspect ratio is 1147µm X 931µm

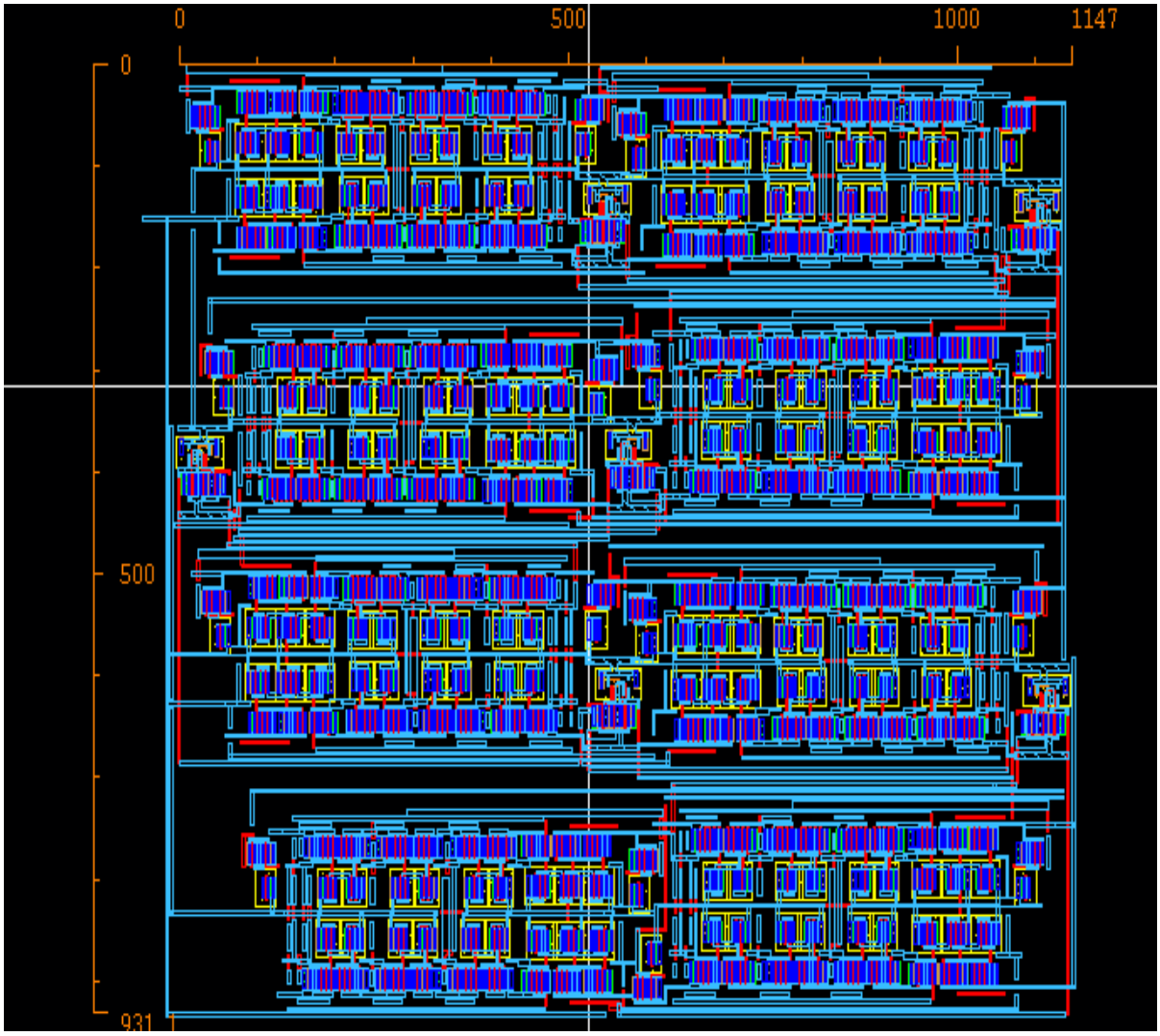


Fig. 4.4. Counter Physical Design

4.2 Analog Layout

The layout of analog blocks used in the DAC is discussed in this section.

4.2.1 Capacitor Chain

The blocks used in the design of the capacitor chain are transmission gates and the capacitor array. The Fig. 4.5 shows the physical design of the transmission gate. The main idea of the design is: Each branch of a capacitor chain has two transmission gates to provide the charging and discharging path to the capacitor. The design is made in a way that using two transmission gates together occupies as little space as possible as shown in Fig. 4.7.

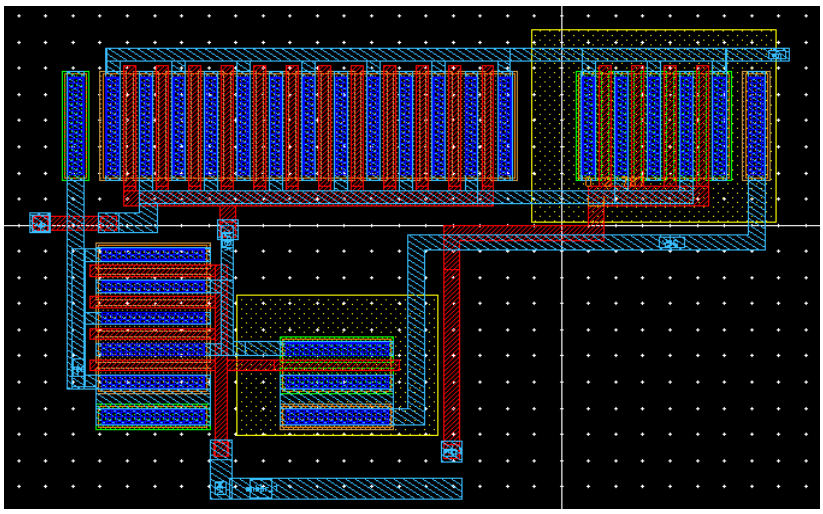


Fig. 4.5. Transmission Gate Physical Design

The layout of the capacitor chain is shown in Fig. 4.6. The aspect ratio is 613µm X800µm.

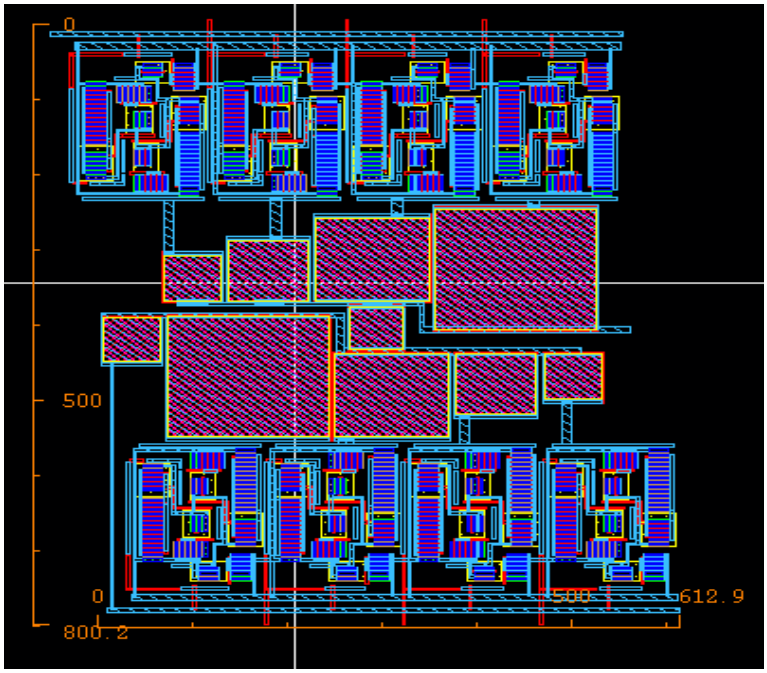


Fig. 4.6. Charge Scaling DAC

4.2.2 Schmitt Triggers

The layout of the modified Schmitt circuit is given in Fig. 4.9. The aspect ratio is 174 µm X 73 µm.

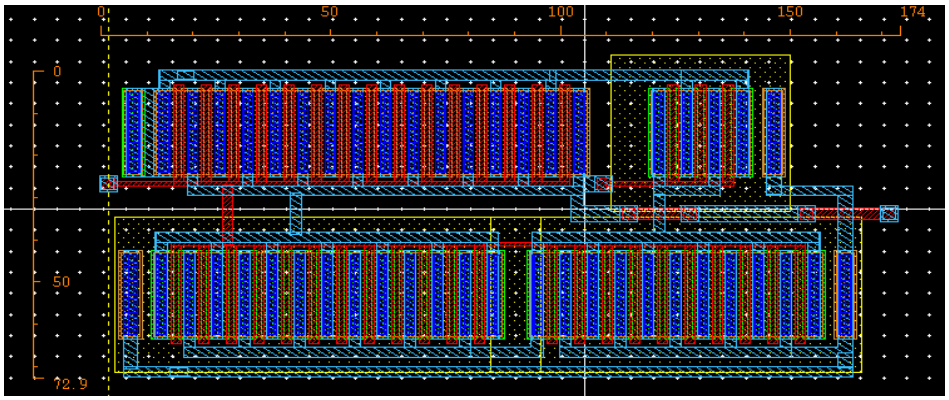


Fig. 4.7. Modified Schmitt Trigger Layout

The Schmitt trigger layout with digital pad frame and the corresponding actual reticle is shown in Fig. 4.7 and Fig. 4.8 respectively, which was design for Raytheon tape out 1. The driving capability of the circuit is further enhanced, as the digital pad frame has a built-in buffer. The aspect ratio of the circuit is 109µm X 178 µm without the pads.

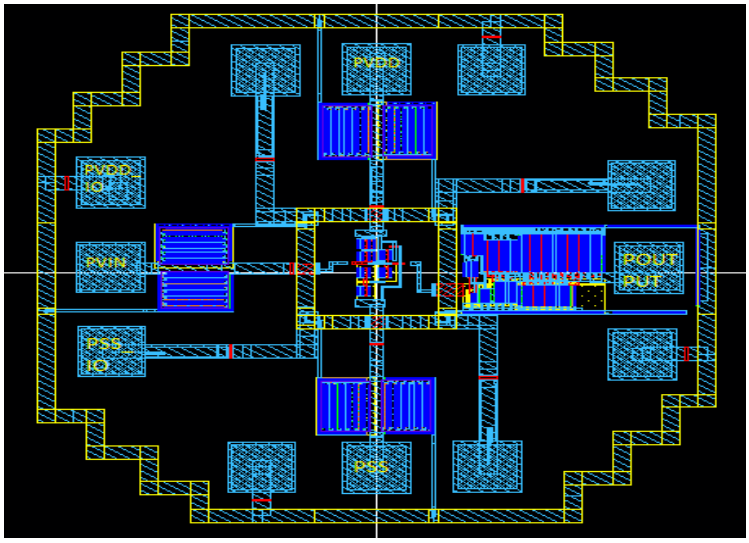


Fig. 4.8. Schmitt Trigger with Digital Pad Frame

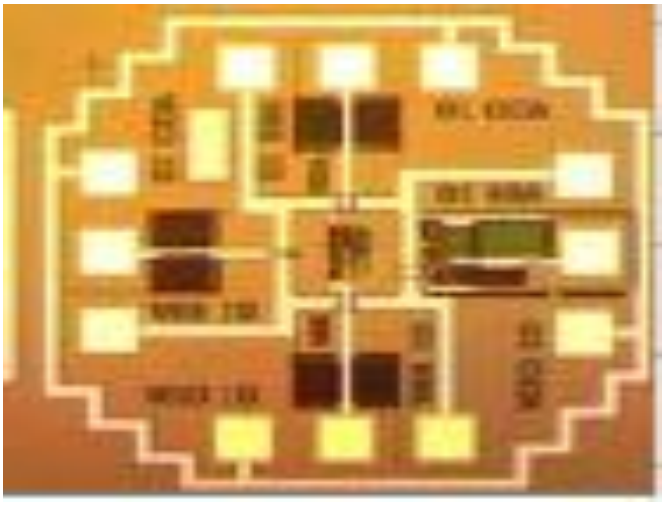


Fig. 4.9. Actual Reticle Image of Schmitt Trigger

4.3 Full Chip Layout

The aspect ratio of the Full chip is 953 µm X 2731 µm. Single metal process is used, it quite challenging to design the full chip layout with very less poly (which adds more resistance). The figure below shows the full chip circuit with probe pads.

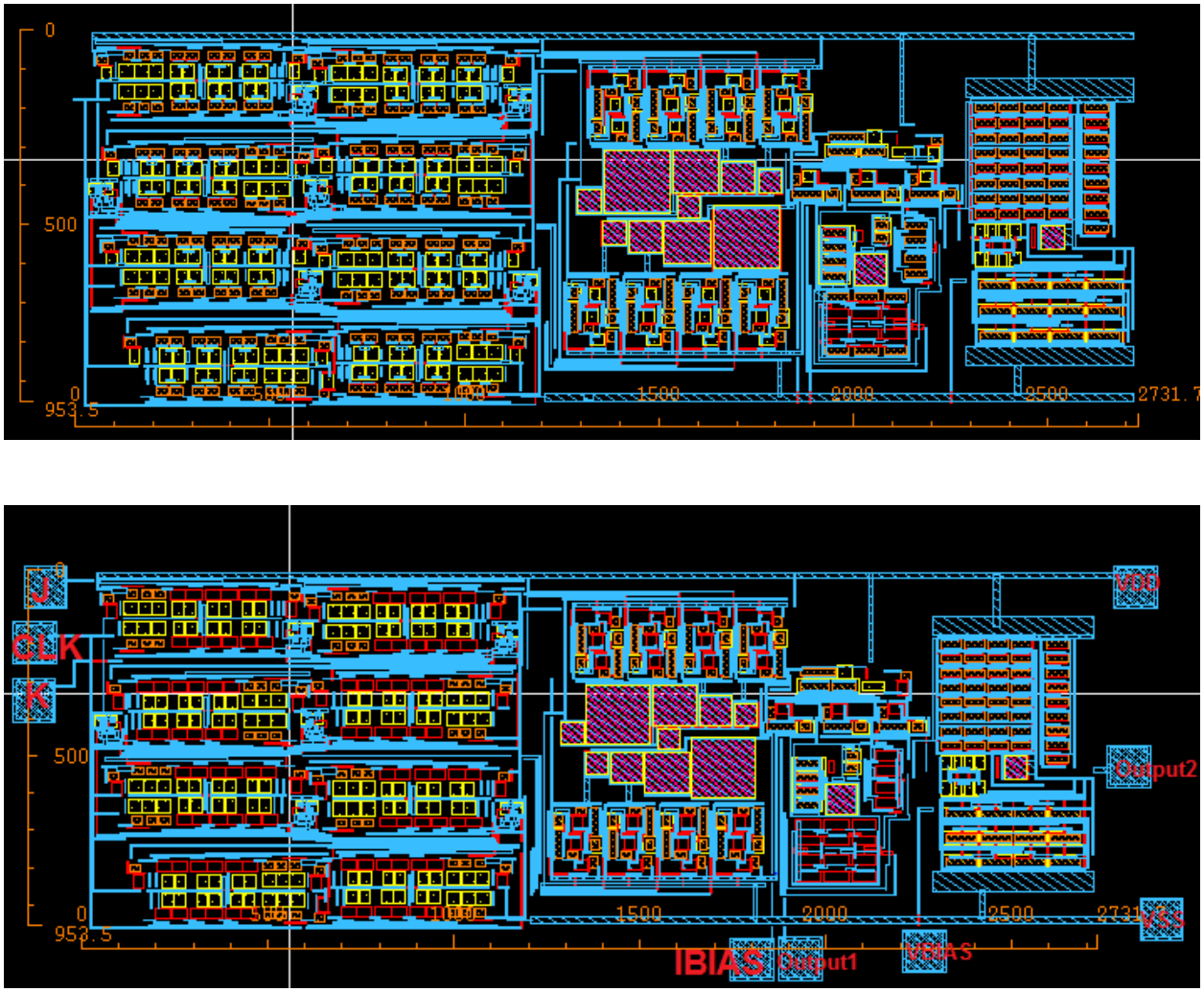


Fig. 4.10. Full chip Layout With probe pads

5. CONCLUSION

5. 1 Summary

This thesis presents the overall design flow of a charge scaling DAC with rail to rail buffer output. The charge scaling DAC is the first of its kind designed in SiC CMOS technology which operate in high temperature ranges is an added advantage to the circuit. The design uses the BSIM4 models.

The Charge scaling DACs have an inherit advantage of lower power consumption and fairly decent conversion speeds. The circuit design is made in such a way that it behave monotonically and the sizes of the capacitor are reduced to save the chip area. The size of the largest capacitor in the design is 16pF. The sizes of the capacitors are chosen in a way that the input capacitance of the op amp doesn't impact the functioning of the capacitor chain.

The DAC is functional at frequencies as high as 1 MHz and have good performance characteristics. The output is buffered in the range of 127.6 m V to 10.2 V. The power consumption of the whole topology is less than 200m V. As a 1.2µm process is used, the conversion speed of overall all circuit is improved.

5.2 Significance

Most of the cases an op amp buffer is used at the output stage of the DAC to improve the driving capability of the circuit. It is difficult to design an op amp with a rail to rail input common mode range (ICMR). Without the proper output buffered stage the usage of the DAC will not be

fulfilled to a full extent. The approach used to get rail to rail buffered output is applicable to all the circuit which need a full range buffered output.

5.3 Future Work

The design does not have any disadvantages except for the ICMR range of the two stage n channel input operational amplifier. As the max ICMR of the op amp is 11.2 V the usage of the DAC is limited to this voltage itself. If an op amp is designed having a minimum ICMR of 5 to8 V and the maximum ICMR nearly equal to the top rail, then it is possible to get the rail to rail buffered output. The circuits are yet to be sent for fabrication and packaged. Temperature testing is needed to see the behavior of the circuit at high temperatures. The transmission gates on state resistance implement the design with the full circuit topology with SR flip flop; this provides more control over the switching between op amps. If the accuracy of the circuit is given more importance the DAC can be implemented with pipeline based approach shown in appendix D, which provides a more accurate analog output at the expense of chip space. The circuit can be tested by following the test plan shown in Appendix A.

BIBLIOGRAPHY

[1] Philip E.Allen, Douglas R. Holberg CMOS Analog Circuit Design, 2nd ed, Oxford University Press 2003

[2] R.Jacob Baker, CMOS circuit Design, Layout, and Simulation, 3rd ed, A John Wiley & Sons, INC., Publications

[3] Weste, Neil H.E. and Harris, David (2005). CMOS VLSI Design: A Circuits and Systems Perspective, 3rd Edition

[4] Modlyng Lynguent

[5] Cadence Virtuoso. Cadence Design Systems Inc., 2013.

[6] Mentor Graphics Calibre, Mentor Graphics, 2013.

[7] A.Hastings, The art of analog layout. Upper Saddle River, NJ: Pearson/Prentice Hall, 2006.

[8] "INL/DNL Measurements for High- Speed Analog-to- Digital Converters Tutorial- Maxim." Avaliable: "http://www.maximintegrated.com/app-notes/index.mvp/id/283".

[9] A.Sedra amd K.Smith, Microelectronic Circuits Theory and Applications, New Delhi: Oxford University Press, 2009.

[10] Peter Wilson and H. Alan Mantooth MODEL- BASED ENGINEERING for COMPLEX ELECTRONICS SYSTEMS, 1ST ed, Newnes 2013

[11] Shaila, A. (2012). Design of two stage operational amplifier using SiC process (Master's thesis). Retrieved from ProQuest Dissertations and Theses.

[12] Hubert Kaeslin Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication, 1st ed, Cambridge University Press 2008

[13]Randy Brown. Elmore's delay model
Avaliable:http://comp.uark.edu/~rlb02/IntroToICDesign/Lectures2013/logical_effort.pdf

[14] "A family of CMOS Analog and Mixed Signal Circuits in SiC for High Temperature Electronics" IEEE Aerospace conference- 2015

Appendix A. Test Plan

A. Circuit Overview

The DAC to be tested is designed in a 1.2 μm SiC process. The process voltage is 15V.

There are different kinds of sub-circuit block of DAC to be tested.These are

- Schmitt triggers
- Counter
- Full chip DAC

These circuits are to be tested over temperature range, transient behavior and current consumption. The load capacitance used for the simulation is 1pf. The simulation results of the circuit are shown in Appendix B. For the Schmitt trigger circuit follow the test bench setup shown in Appendix C.

B. Test Equipment

Table A.1. Test Equipment used

Agilent Hewlett Packard HP 54645D 100 MHz 2-16 Channel Mixed Signal Oscilloscope
Oscilloscope probes 1pf
Tektronix AFG3022B Dual Channel Arbitrary/ Function Generator 25 MHz
Agilent E3631A Triple Output DC Power Supply
Cole Parmer STable Temp hotplate
Hewlett Packard 3458A Multimeter

Marconi Instrument 10 KHz, 2.7 GHz signal Generator 2031
Keithley 4200 SCS
Semi Probe Station M-6

C. Counter

Table A.2. Counter pin I/O description

Pin out name	Connection description
VDD	Power supply: 15.0 V_{DC}
VSS	Circuit ground: 0 V_{DC}
Clk	Power supply: 15.0 Pulse
J	Power supply: 15.0 V_{DC}
K	Power supply: 15.0 V_{DC}
Q0	Lower significant Output bit D0
Q1	Output bit D1
Q2	Output bit D2
Q3	Output bit D3
Q4	Output bit D4
Q5	Output bit D5
Q6	Output bit D6
Q7	Most significant bit D7

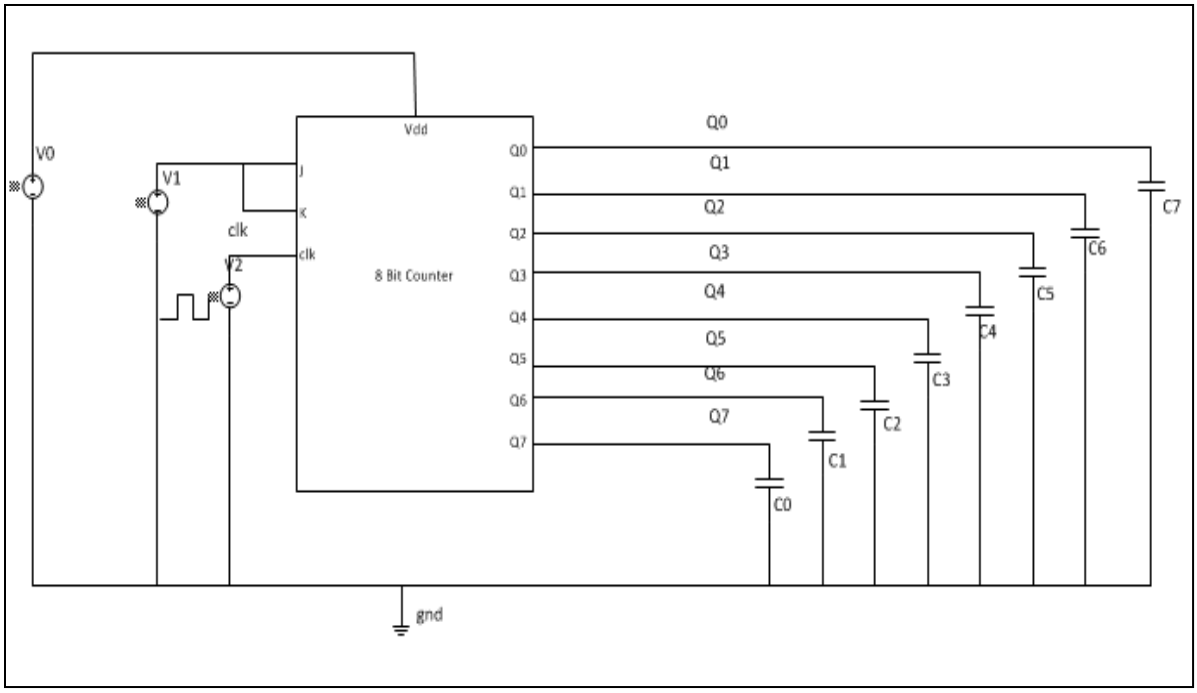


Fig. A.1 Test Setup for counter

Testing Procedure

The goal of the test setup is to measure the output of the 8 bit sequential up counter over temperature.

Steps for setting up the bench

1. Connect the grounds to all the VSS pins of the counter

2. Connect the 15V Voltage Supply from the HP 6216A to VDD, Pad VDD

3. Connect the 15V Voltage supply from HP E3631A to the J an K ports of the counter

4. Generate input square signal with a peak value of 15V using the arbitrary waveform generator. The amplitude to 7.5 Vp-p with a offset of 7.5 V, and the frequency to 500 KHz.

5. Connect the output of each output bit line to the oscilloscope (one bit at a time) and measure the frequency, output rise and fall times.

6. Vary the temperatures and repeat the process and Record the values

7. Turn off the power supplies.

D. Full chip DAC

Table A.3. Full chip DAC pin I/O description

Pin out name	Connection description
VDD	Power supply: 15.0 V_{DC}
VSS	Circuit ground: 0 V_{DC}
Clk	Power supply: 15.0 Pulse
J	Power supply: 15.0 V_{DC}
K	Power supply: 15.0 V_{DC}
Output	Voltage output

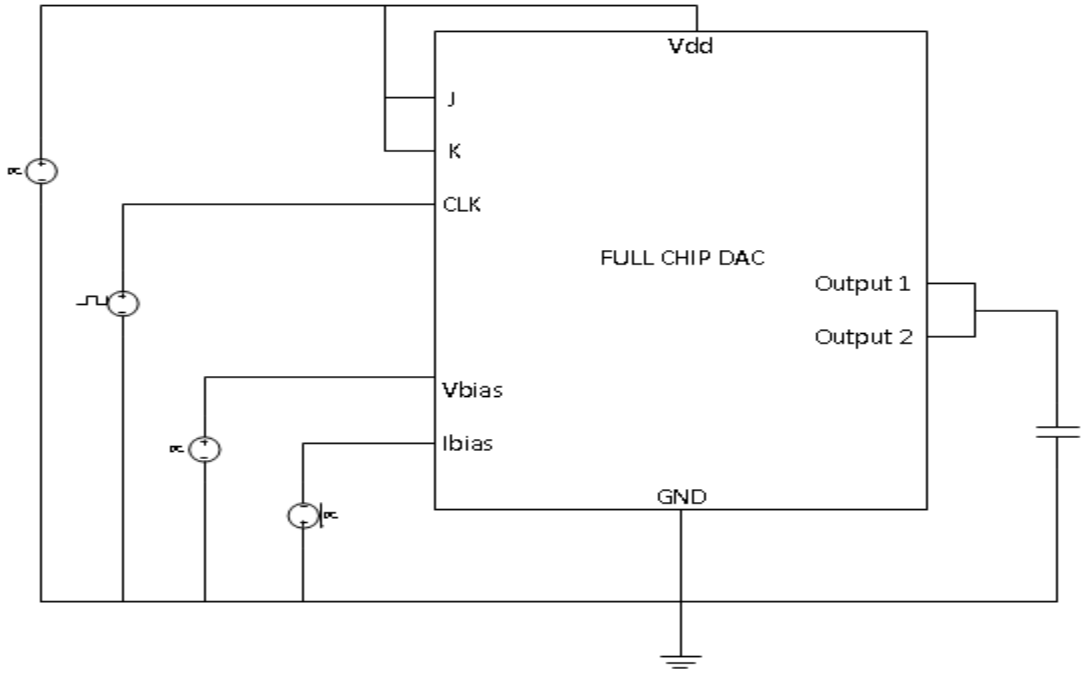


Fig. A.2 Test Setup for DAC circuit

The layout below shows the full chip design indicated I/O ports on the pads.

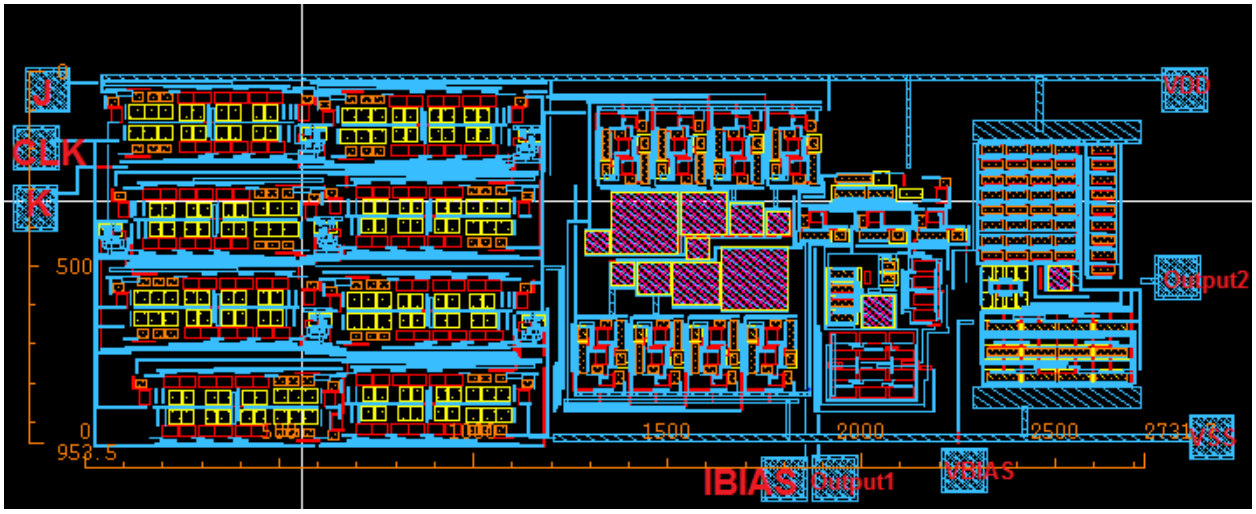


Fig. A.3 Layout of the Chip

Testing Procedure

The goal of the test setup is to measure the output of the Full chip DAC over temperature. The measure of INL and DNL error are to be calculated from the recorded data.

Steps for setting up the bench

1. To test on probe station, place the reticle on the chuck

2. Connect the probe tips to the pads, turn the vaccum on and mark which coaxial cable connects to which pad.

3. Create a Project folder to save data into the Keithey

4. Connect all the VSS pins of the DAC to the GND port of keithley

5. Connect the pin J,K and supply to the SMU 1 port of keithley at set the voltge as 15V.

6. Connect the CLK to the SMU 2 of keithley and set a pulse voltage input with a peak value of 15 V and the frequency to 500 KHz.

7. Measure the output by connecting the port to SMU 4 port

8. Set the connection on keithley

6. Run the transient simulation for 0 to 300 µsec and plot the output voltage versus time graph

7. Save the file

8. Raise the probe tips, increase the temperature of the chuck and lower the probe tips.

9. Run the simulation again. Repeat this process at temperatures 25, 100, 200, 300˚ C and save the data.

10. Raise the probe tips lower chuck, turn the vacuum off and remove reticle from the probe station.

11. Get the data from the keithley and analyze the values by calculating DNL, INL errors using excel.

Appendix B. Temperature and Extracted simulations

This section of the document provides information on circuit behavior with temperature and simulation with parasitic extraction from the layout.

A. Split Array DAC

The figure below shows the DAC's un buffered output at varying temperatures. It is observed that the output varies less than 0.2 V when the temperature changes from 100˚C to 300˚C.

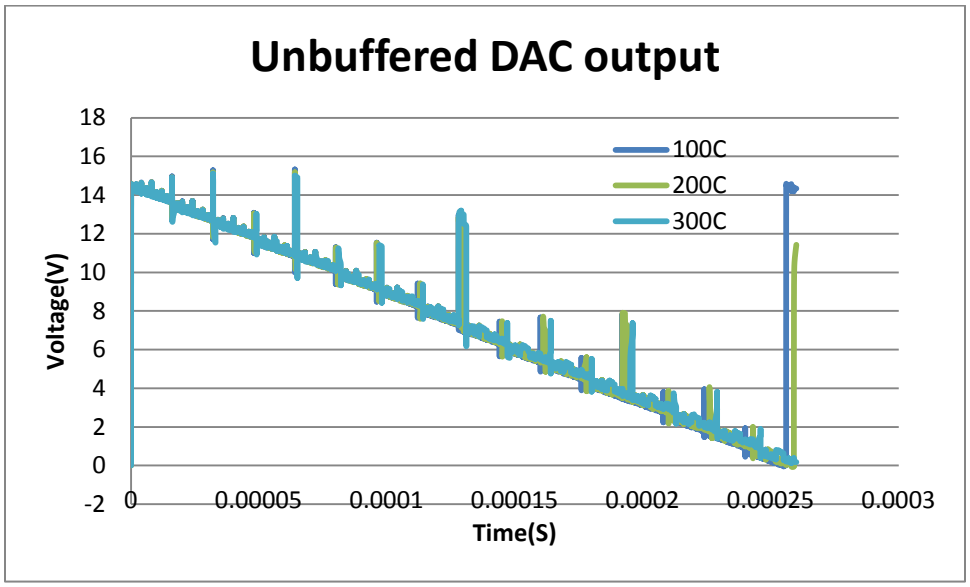


Fig. B.1 Unbuffered DAC Output Over Temperature

Simulation Results With PEX and Without PEX

The plot marked in blue resembles the simulation with out considering the parastics and the one with red is with the parasitics. The extraction results shows almost same characterstics as that of the testing results.

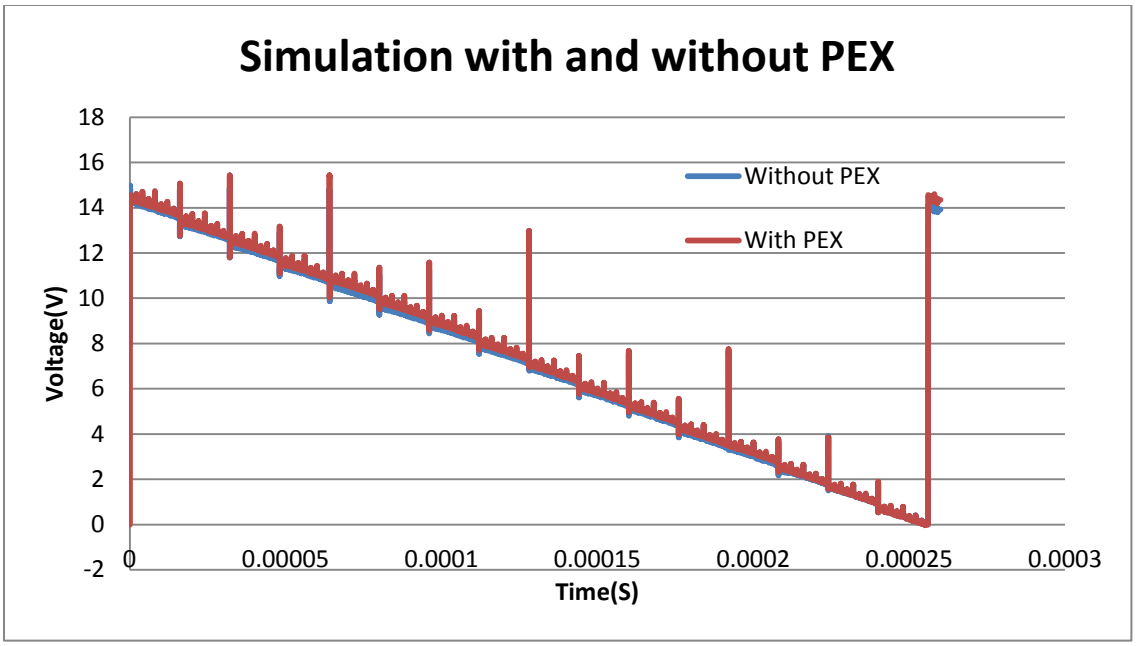


Fig. B.2 Simulation With and Without PEX

B. Schmitt Trigger

The Table.B.1 provide the information about the variation in schmitt trigger characterstics with PEX and without PEX over temperature

Table. B.1. Simulated Schmitt Trigger

Parameter	Temperature	Without PEX	With PEX	Unit
Hysteresis width	25	2.1(5.1,7.2)	2.2(5.1,7.3)	V
	100	2.3(4.9,7.2)	2.15(4.9,7.05)	
	200	1.8(5.3,7.1)	1.9(5.3,7.2)	
	300	2.6(4.7,7.3)	2.8(4.6,7.4)	
	25	7	8	ns
	100	6	6	

Rise Time	200 300	5 9	6 7	
Fall Time	25 100 200 300	10 6 3 4	9 5 5 4	ns
Power consumption	25 100 200 300	21 30 31.5 29	16.5 20.55 21 14	mW

C. Counter

The fig. B.3 shows the extracted simulation of the counter circuit. The output pulse rise and fall times are found to be 22 and 17 nanoseconds respectively. The simulated and extracted characteristics don’t seem to show much variation.

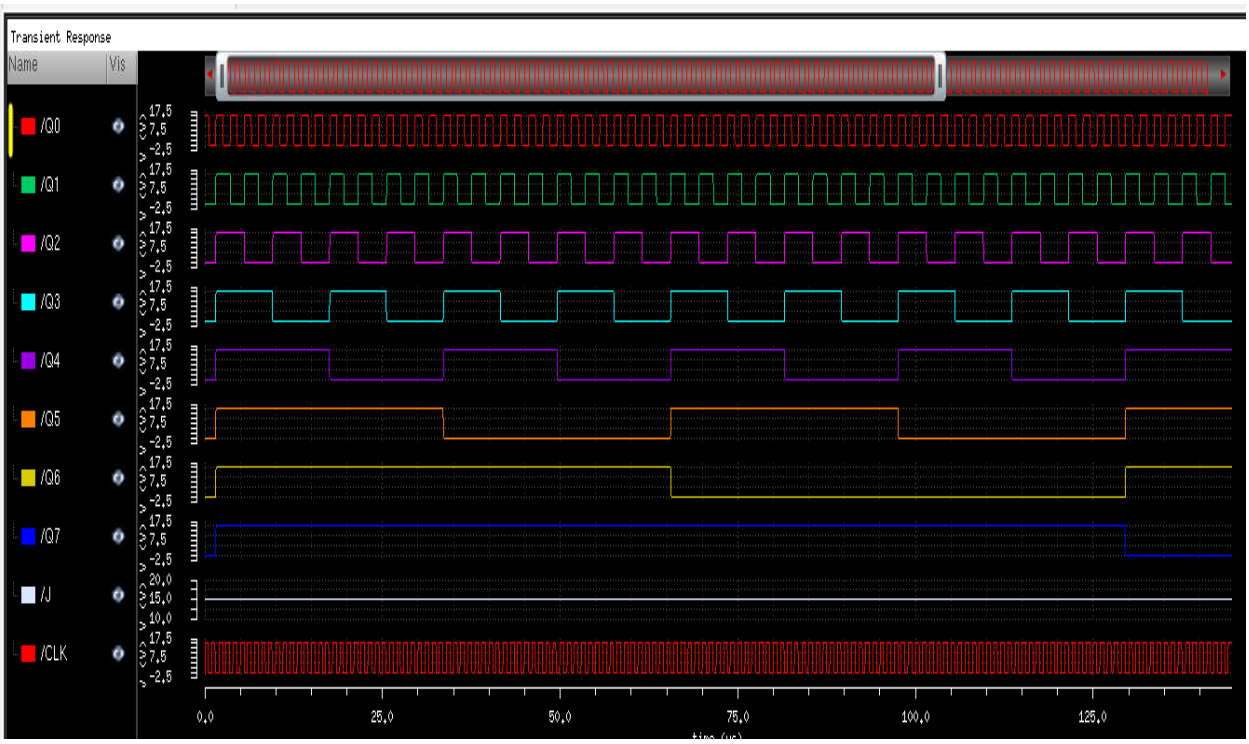


Fig. B.3 Extracted Simulation of Counter

D. Full chip

The figures below shows the comparison between buffered DAC output with and without parasitic extraction. The extracted results are very much quite same as that of the simulation results without parastics.

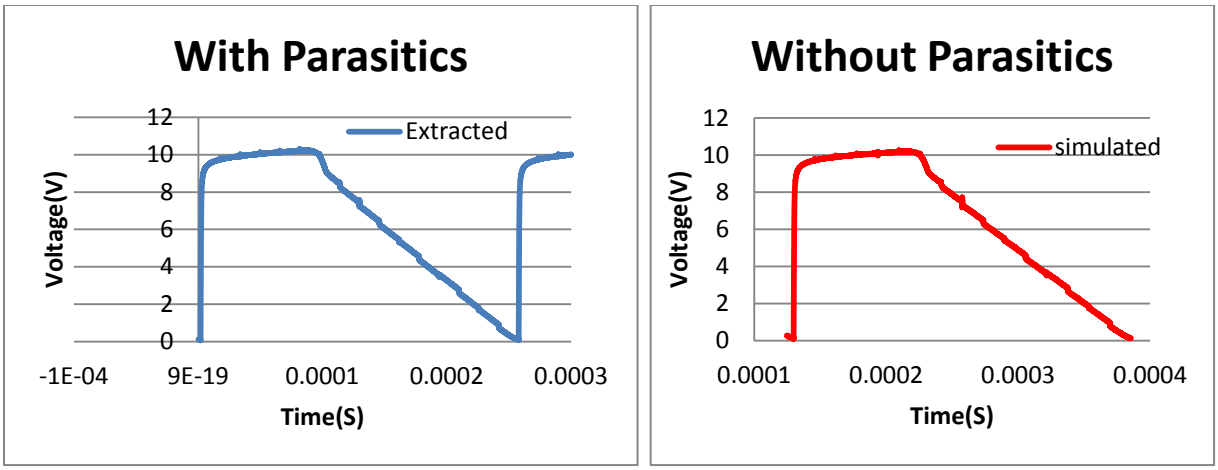


Fig. B.4 Full chip DAC buffered output with and without PEX

Temperature Simulations Error checking

DNL and INL

The plot shows the DAC's linearity measure with respect to varying temperatures. From the plots it can inferred that the DNL and INL errors doesn't change much with temperature.

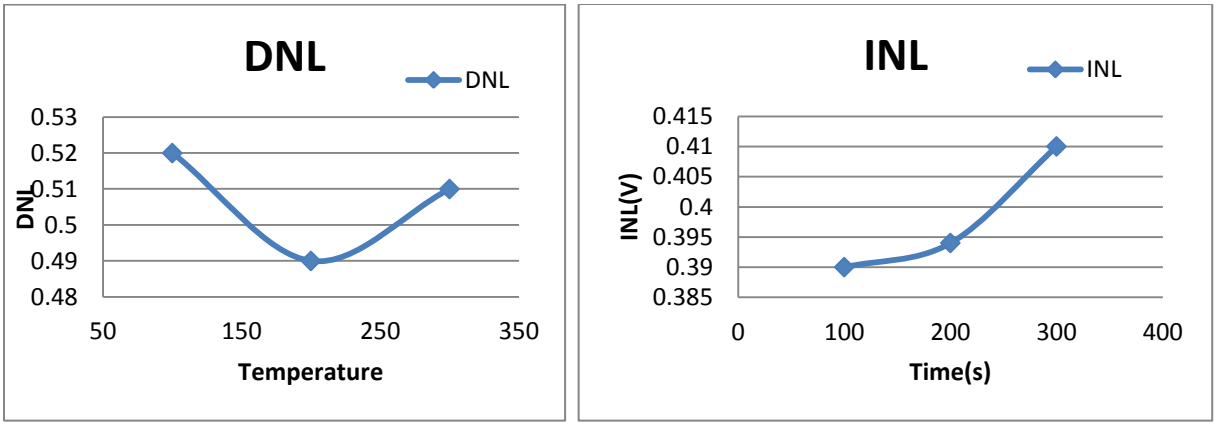


Fig. B.5 Error checking at varying temperatures

Appendix C. Testing and characterization of Schmitt trigger circuit

The Schmitt trigger designed for the Raytheon tape out 1 was sent to fabrication. The testing results of the fabricated chip give the clear idea of how a circuit which is designed in silicon carbide process responds to temperature changes. A wide range of bonding and packaging plans that are compatible with the high temperature testing were considered.

A. Bond Wire and Packaging

The wire bonding and the packaging was accomplished at High Density Electronics center (HiDEC) at the University of Arkansas. The Fig. C.1 shows the Schmitt trigger on the die.

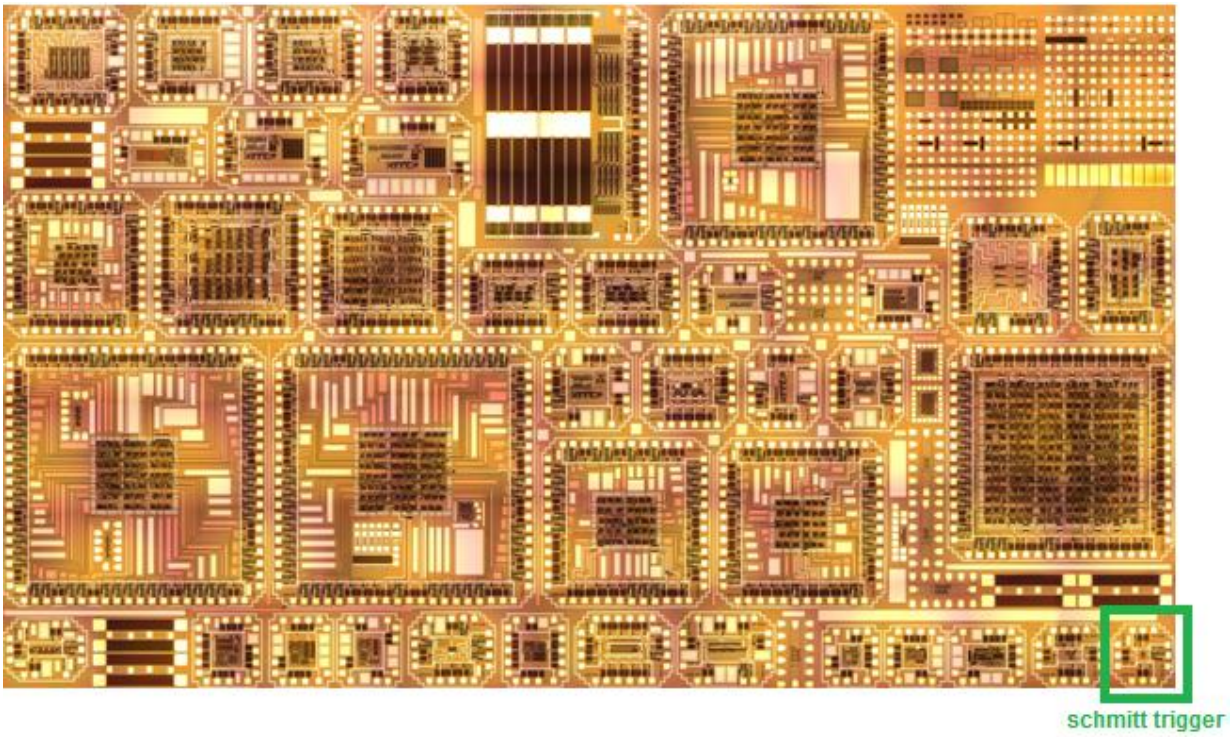


Fig. C.1. Schmitt Trigger Circuit on the Die

There is a specific sequence of steps to be followed for packaging the chip. The first step is to dice the Schmitt trigger reticle from the die shown in the above figure. In the second step the die is attached into the 64- pin ceramic quadpack package using epoxy which can with stand high temperatures. The package was kept in a vacuum oven at 150˚C for 4 hours, which will allow the epoxy to settle down and die will be attached to the package. The third step was wire bonding. The pads of the circuit were bonded to the package by using 1 mil gold wire. Fig. C.2 shows the bonding plan of the Schmitt trigger. The reticle is placed at the bottom left corner of the package. The pin out information is detailed in Table C.1

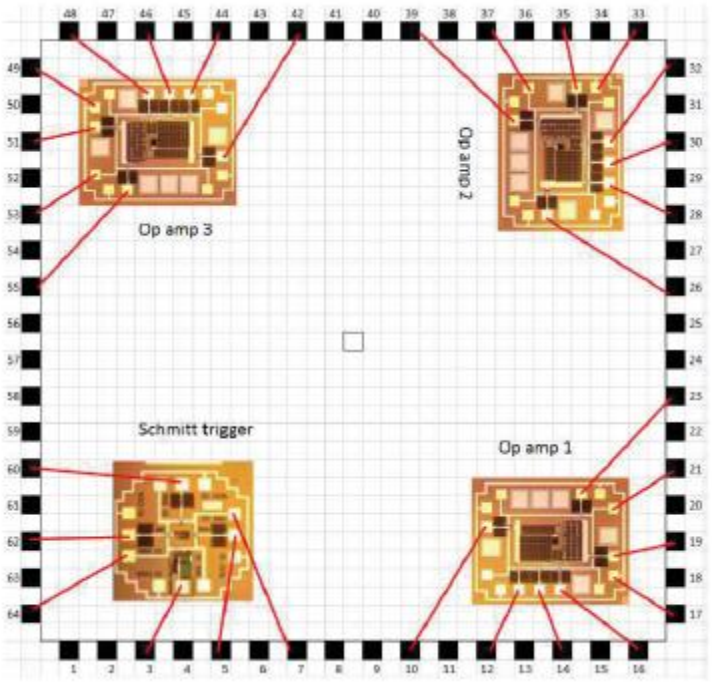


Fig.C.2. Bonding Plan

Table C.1. Bonding diagram pin configuration

PIN name	PIN on package
PVDD	60
PVSS	3
PVDD_IO	6
PVSS_IO	63
PVIN	62
PVOUT	5

The final step packing is soldering the package to the printed circuit board (PCB) and verifies the connections. The PCB can withstand the temperature as high as 300˚C. The Fig..A.3 shows the packaged chip.

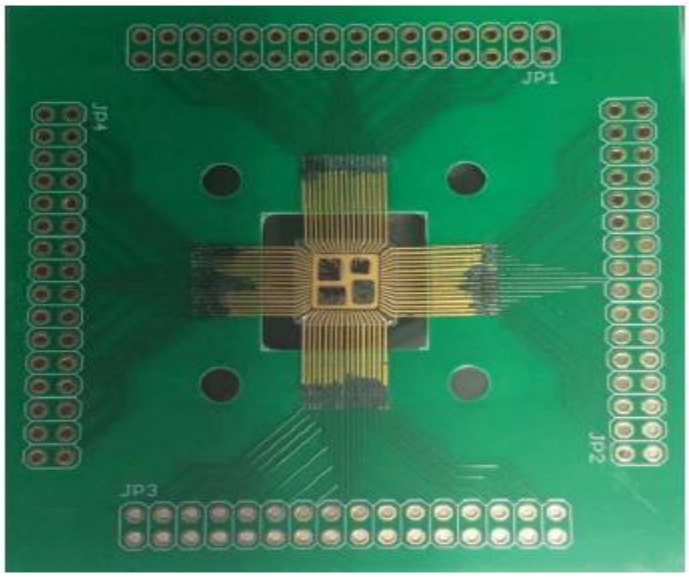


Fig.C.3. Packaged Circuit [11]

B. Test Setup

Fig.C.4. Semiprobe Station M6 150mm Test Setup

The test equipment is shown in Table 5.3. The circuit characteristics are measured at varying temperature from 0 to 300˚C and compared with the simulation results. Active probes are used to reduce the loading effect of the circuit.

Table C.2. Testing equipment

Agilent Hewlett Packard HP 54645D 100 MHz 2-16 Channel Mixed Signal Oscilloscope
Oscilloscope probes 10 Pf
Tektronix AFG3022B Dual Channel Arbitrary/ Function Generator 25MHz
Agilent E3631A Triple Output DC Power Supply
Cole Parmer STable Temp hotplate
Hewlett Packard 3458A Multimeter
Marconi Instrument 10KHz, 2.7GHz signal Generator 2031

C. Test Results

The circuits fabricated are tested and characterized under varying temperature and supply voltage variations.

DC Characterization

By performing the DC Characterization on the chip, the performance characteristic like DC power consumption, upper and lower switching voltages of the chip can be determined.

I. Measurement of Hysteresis Width:

The Fig. A.5 shows the Test Bench setup for measuring Hysteresis width followed by testing procedures.

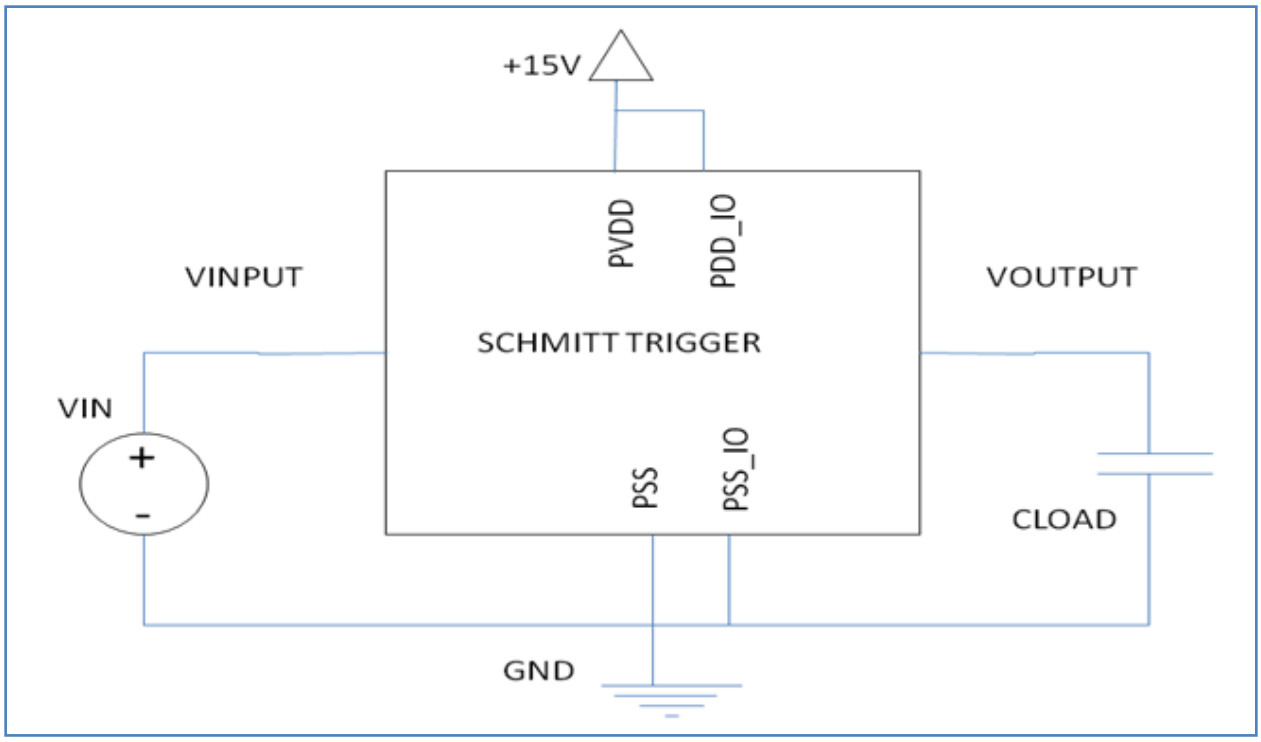


Fig.C.5. Test bench for Measuring Hysteresis Width

Procedure

a) Connect the board as shown in the Fig.C.5.

b) Follow the general power up procedure.

c) Set the Transient triangular power supply with time period of 1us and peak voltage of 15V starting from 0 V and measure the hysteresis width by noting down the Upper Threshold and Lower Threshold Voltage by observing the intersection points of the triangular waveform with the output waveform in the oscilloscope.

d) Repeat c) for varying power supply and varying temperatures (25 -300^{0}C)

e) Note down the values

The Fig..C.6 shows the plot of the hysteresis width with the varying temperature. It observed hysteresis width is within the +/- 10% range of the simulated value.

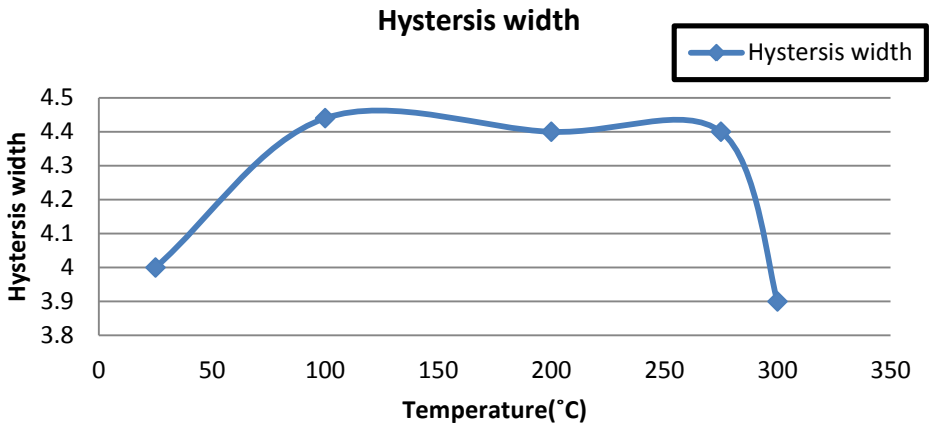


Fig.C.6. Hysteresis Width Vs Temperature

Transient Characterization

By performing the Transient Characterization on the chip, the performance characteristics such as slew rate, rise, fall and delay times can be determined

II. Measurement of Rise, Fall and Delay Times

The Fig. C.7 shows the Hysteresis setup for measuring Hysteresis width followed by testing procedures.

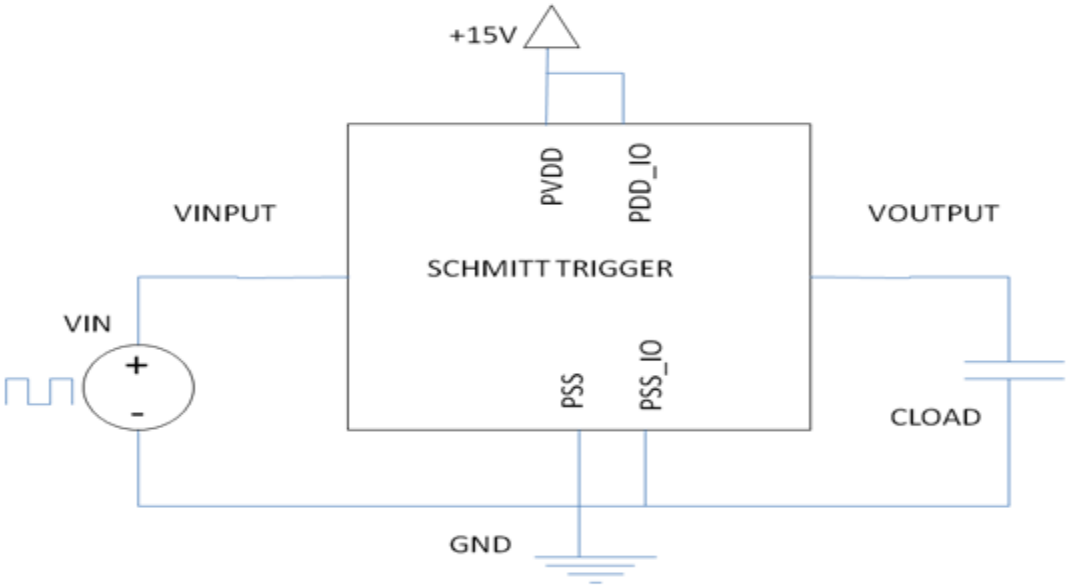


Fig.C.7. Test Bench for Measuring Rise and Fall Times

Procedure

a) Connect the board as shown in Fig..A.7.

b) Follow general power –up procedure.

c) Generate the input square signal with a peak value of 15V using the arbitrary waveform generator. The amplitude to 7.5Vp-p with an offset of 7.5, and the frequency to 500KHz initially and increase it up to 3MHZ.

d) Monitor the rising and falling edge of the output signals.

e) Measure the rising and falling slope to calculate each slew rate.

f) Measure the rise time by calculating the time taken by the signal to reach 90% of its final value from the 10% of the final value.

g) Measure the fall time by calculating the time taken by the signal to reach from 90% of its final value to the 10% of the final value.

h) Measure the delay time by observing the time difference between the input and output.

i) Increase the temperature of the die from 25^{o}C to 300^{o}C in gradual increments.

j) Repeat the measurement following steps c) to f) for each temperature step.

Note down the measured values in the Table

The plots below show the variation of rise and fall times with respect to temperature. The rise and fall times didn't vary much with the temperature.

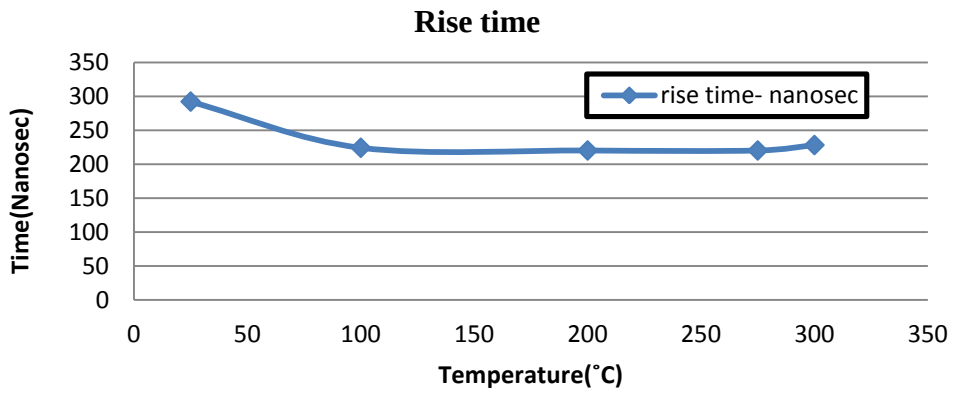


Fig.C.8. Rise time Vs temperature

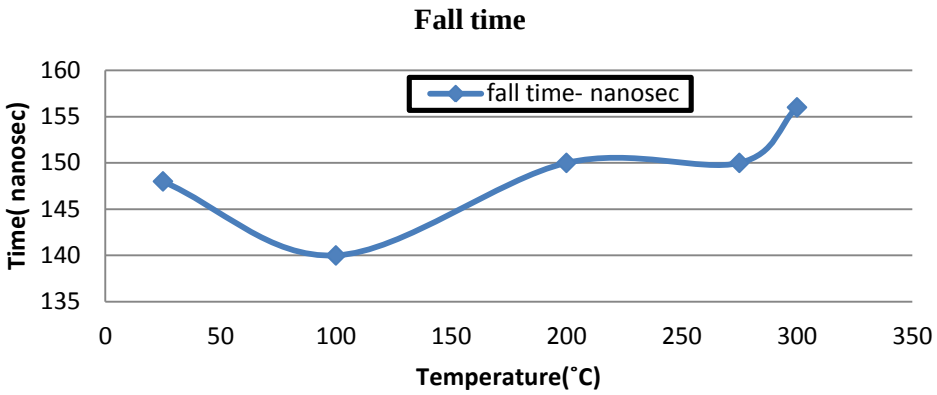


Fig.C.9. Fall time Vs temperature

Table. C.3. Simulated and measured values of Schmitt Trigger

Parameter	Temperature	Simulated value	Measured value	Unit
Hysteresis width	25	3.78	3.98	V
	100	3.9	4.43	
	200	3.56	4	
	275	3.4	4	
	300	3.4	3.9	
Rise Time	25	196	294	nanosec
	100	182	218	
	200	174	210	
	275	172	212	
	300	169	225	
	25	131	147	
	100	126	140	

Fall Time	200 275 300	115 111 107	151 150 156	nanosec
Power consumption	25 100 200 275	0.89 1.25 1.637 1.637	56.2 94 112.2 131.6	mW

Appendix D. 8 BIT PIPELINE DIGITAL TO ANALOG CONVERTER

A. Introduction

The split array based charge scaling DAC have advantages of lower power consumption, output is sampled and held, but when come to the point of error checking it is found that the max INL and DNL errors are 6 LSB and 3 LSB respectively. If more accurate converter is needed with DNL and INL less that +/- 2 LSB the pipeline based design approach can be used at the expense of large circuit space. Pipeline based DAC uses the charge scaling implementation. The accuracy of the output mainly depends on the op amps used in the design. An 8 bit pipeline DAC consists of sub circuits like sample and hold, gain and switches which make the design a bit more bulky. The main advantages of this topology are fully monotonic, high conversion speed and a high resolution can be achieved by varying amplifier gain. The only disadvantage of this DAC is it occupies a large chip area[2]. This topology can be used in areas where high accuracy is needed and does not have much restriction with the circuit space and power consumption.

Table. D.1. Design Specifications of the Pipeline Based DAC

Design Parameters	
Vref	2.5 V
Vout Range	0 to 15 V or binary value
VDD	15 V

Operating frequency	Upto 1 MHz
Offset	< 0.1 mV
Conversion speed	Converts for every clock cycle after the first N clock cycles
INL and DNL error	< 0.5 LSB

B. Technical Approach

The design of the DAC is carried out in three levels. In the level 0, the inner sub blocks of the DAC are designed and modeled, simulated by giving the digital input and observed the corresponding output. In the level 1, error checking is performed and also a few adjustments are made in the design to make the output accurate. The DAC is checked for the production of the sine wave at the output when the ADC output is connected to the input of the DAC. The level 2 is a custom based approach; the DAC is modeled with verilog A and added few effects such as offset, rise time, fall time and time delay.

Table. D.2. Levels of Design Approach

Level	Approach	Description
Level 0	Effects	In this level I have designed the circuit based upon the pipeline based topology and simulated it by giving an input square wave for the corresponding digits and check the output, whether it is analog or not.
Level 1	Effects	In this level of design I have tested the DAC for non ideal effects like INL and DNL and also checked whether the DAC is reproducing the sine wave at the output when the ADC output is connected to the input of DAC.
Level 2	Custom based	In this level I have modeled the DAC by using sequential code for the branch used in the model and added some effects such as offset, rise time, fall time and time delay.

C. Implementation

Sample and Hold Circuit

The design starts by the implementation of the sample and hold circuit with is the most crucial sub block of the pipeline based DAC. The operation of the circuit is quite simple to analyze. When the input to the circuit is logic 0 the capacitor starts discharging to the ground. When the input is logic 1 the capacitor charges towards the reference voltage.

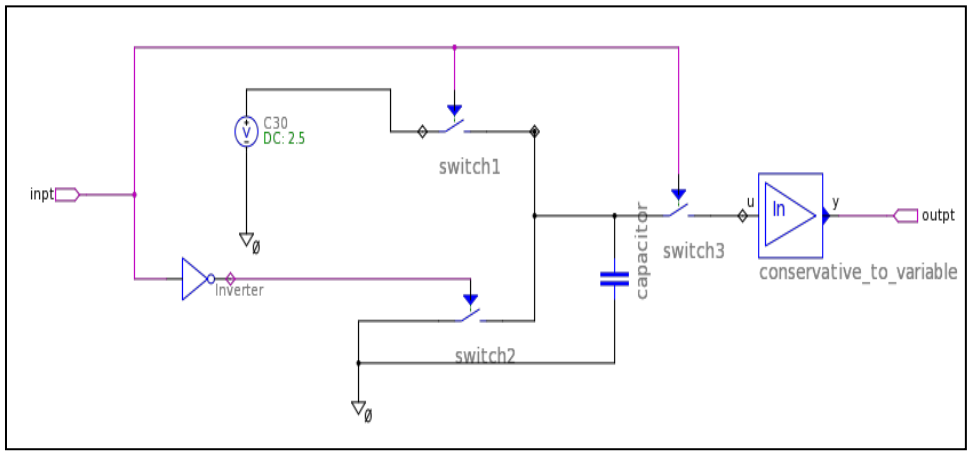


Fig. D.1 Model of a Sample and Hold Circuit

The Table below shows the sub block used in the model design. All the sub blocks are built and behaves ideally.

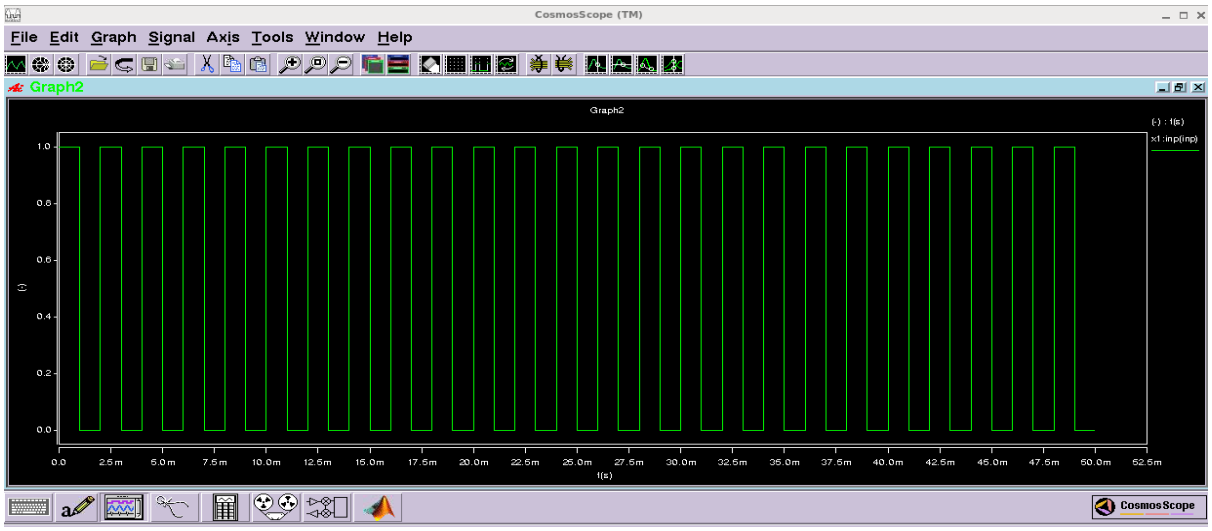
Table. D.3. Sub Blocks of Sample and Hold Circuit

Library	Model	Total Used	Type
eb_Logic	eb_Inverter_VV	1	Built-in-effect
eb_Electrical	eb_Switch	3	Built-in-effect
eb_Electrical	eb_Capacitor	1	Built-in-effect
sl_PortsSubsystems	sl_Inport	1	Built-in-effect
Spice	spl_V_vdc	1	User created effect: Spice DC voltage

			source

Simulation

The plot marked in green is the input to the sample and hold circuit, has two states either ‘0’ or ‘1’. When the input is ‘0’ the capacitor is discharged toward ground, when the input is ‘1’ the capacitor is charged to the reference voltage. The plot shown in blue is the output of sample and hold circuit.



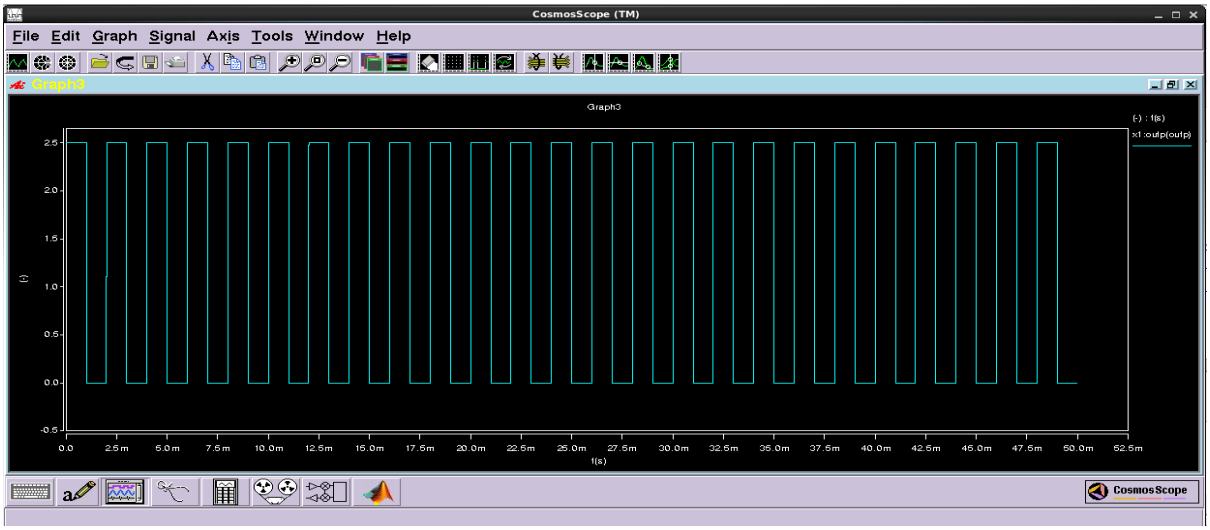


Fig. D.2 Sample and Hold Circuit Functionality

Pipeline DAC

The Fig. D.3. is shows the design topology of pipeline based DAC. The signal from one stage is passed down to the next one, each stage does the processing. In an 8 bit pipeline based DAC the conversion starts after 8 clock cycles, this is the time taken for the signal to pass down from the initial stage to the output of the converter. After this delay time, conversion takes place at every clock cycle. The output of the N stage pipeline based DAC is given as

$$Vout(n) = [Dn-1 * Vref + Vout(n-1)] * 0.5$$

Equation B.1

The operation of the converter is as follows, when an input bit is 1, add the Vref to the output of the previous stage, divide it by two and pass on to the next stage. When the input is 0, the output of the precious stage is divided by two and passed on to the next stage.

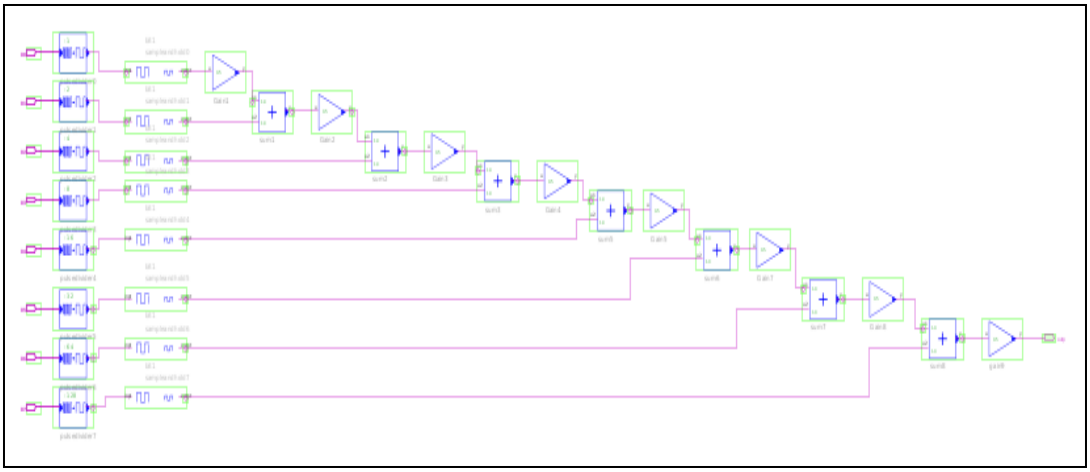


Fig. D.3. Pipeline Based Digital to Analog Converter

The Table below provides the information about the sub blocks used in the design topology and the type of effect.

Table. B.4. Sub Blocks of Pipeline Based DAC

Library	Model	Total Used	Type
Level0	Bit1	8	User created effect: sample and hold using switches
eb_EventDriven	eb_PulseDivider_AV	8	Built-in-effect
Sl_MathOP	Sl_Sum	7	Built-in-effect
Sl_MathOP	Sl_Gain	8	Built-in-effect

Simulation

The plot shows the analog voltage of the DAC for the corresponding digital bit input. The output is a full scale ramp starting at 0 V and reaches the reference value. The offset voltage is 0 V for this ideal model.

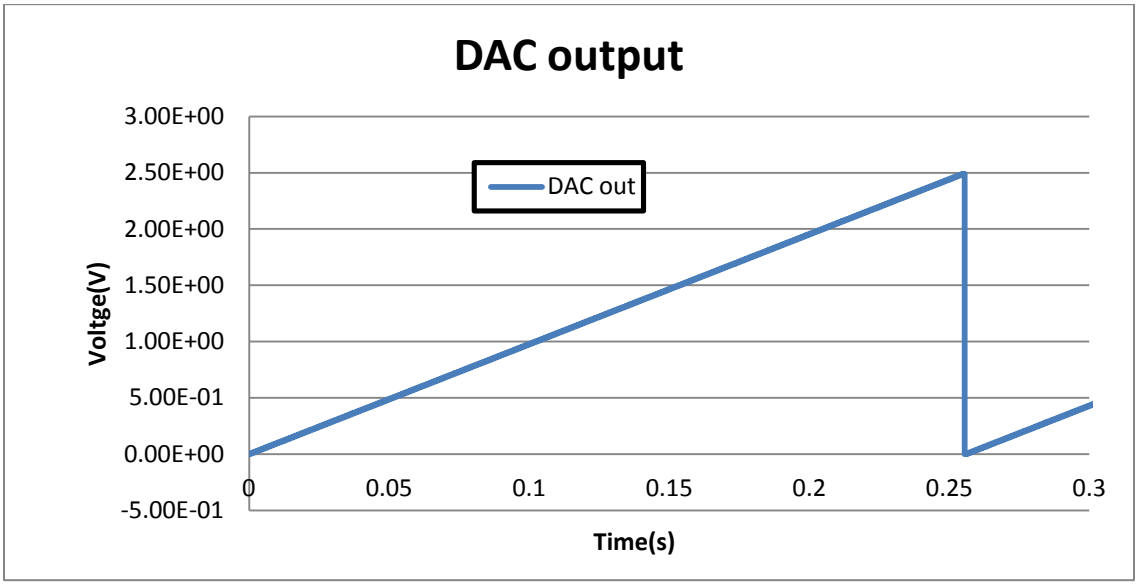


Fig. D.4.Full Scale buffered Output

Linearity

Linearity is defined as the difference between the actual analog output and the desired output over the full range of values. It can be defined by two main specifications INL and DNL. The accuracy of the DAC depends of linearity. The DAC with INL observed to be less than 0.5 LSB and DNL values less than 3 LSB are considered to be more accurate. The Fig. B.5 and Fig. B.6 shows the DNL and INL errors of the converter.

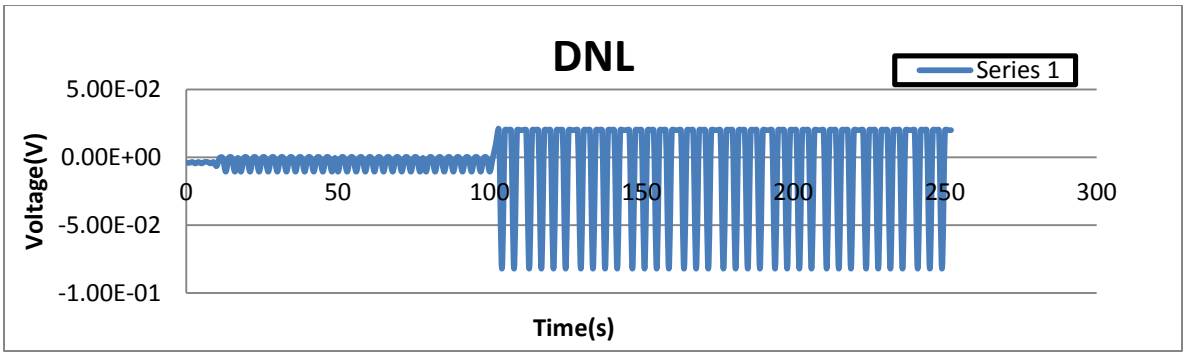


Fig. D.5. Error Checking DNL

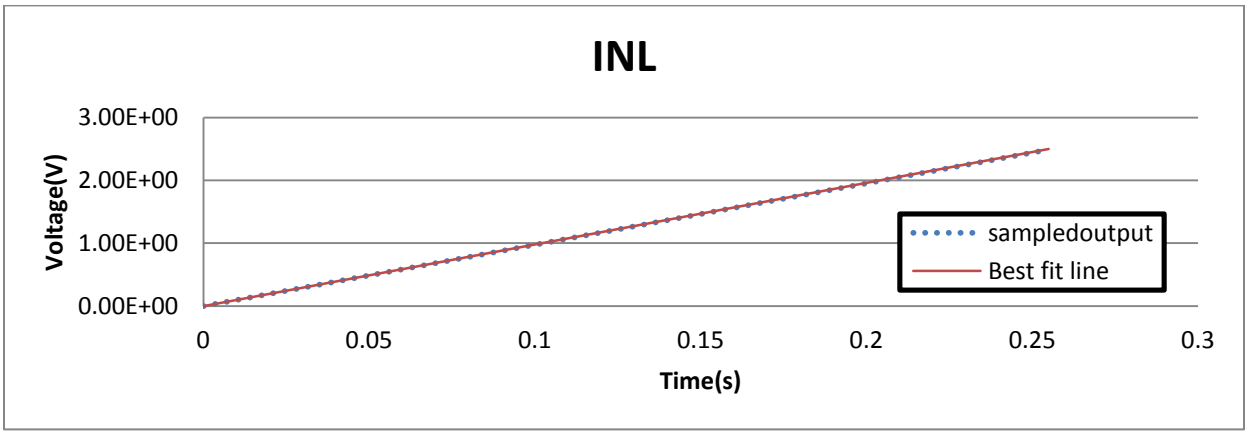


Fig. D.6. Error Checking INL

D. Conclusion

The performance characteristics of ideal DAC model are validated, the linearity error is found to be less than 4 LSB. The design is can be implemented with real models, if provided with enough circuit space and power supply.