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Control Design of a Single-Phase DC/AC Inverter for PV Applications

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Control Design of a Single-Phase DC/AC Inverter for PV Applications

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Abstract

This thesis presents controller designs of a 2 kVA single-phase inverter for photovoltaic (PV) applications. The demand for better controller designs is constantly rising as the renewable energy market continues to rapidly grow. Some background research has been done on solar energy, PV inverter configurations, inverter control design, and hardware component selection. Controllers are designed both for stand-alone and grid-connected modes of operation. For stand-alone inverter control, the outer control loop regulates the filter capacitor voltage. Combining the synchronous frame outer control loop with the capacitor current feedback inner control loop, the system can achieve both zero steady-state error and better step load performance. For grid-tied inverter control, proportional capacitor current feedback is used. This achieves the active damping needed to suppress the LCL filter resonance problem. The outer loop regulates the inverter output current flowing into the grid with a proportional resonant controller and harmonic compensators. With a revised grid synchronization unit, the active power and reactive power can be decoupled and controlled separately through a serial communication based user interface. To validate the designed controllers, a scaled down prototype is constructed and tested with a digital signal processor (DSP) TMS320F28335.

Acknowledgements

I am very fortunate to have performed my master's level graduate study at the University of Arkansas, where I met erudite professors and collaborative colleagues. I would like to give my special thanks to my academic advisor, Prof. Alan Mantooth, who inspires me to achieve my academic goals with his experience, professional ethics, and leadership. Without his guidance and mentorship, I could not have completed my graduation requirements. I am also very grateful for the opportunities and diverse work environment he has created for us.

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Chapter 1 Introduction and Theoretical Background

1.1 Introduction and Motivation

Energy generation and exploitation are drawing increasing interest worldwide. There are three genres of electricity generation: fossil fuel, nuclear energy, and renewable energy resources. Fossil fuels, known as conventional power generation resources, release multiple harmful gases when they are burnt to generate electricity [1]. The emission of carbon dioxide and sulfur oxides are respectively the main cause of global warming and acid rain [2]. To avoid environmental detriment and meet the increasing energy demand, renewable energy resources such as solar, wind, biomass, hydropower, biofuels, and geothermal are deployed and investigated. According to the U.S. Energy Information Administration's statistics of the U.S. renewable energy supply shown in Fig. 1-1, the total energy generated by renewable energy resources are in the trend of increasing [3]. Meanwhile, wind and solar energy are rapidly providing a greater percent of the total renewable energy supply each year.

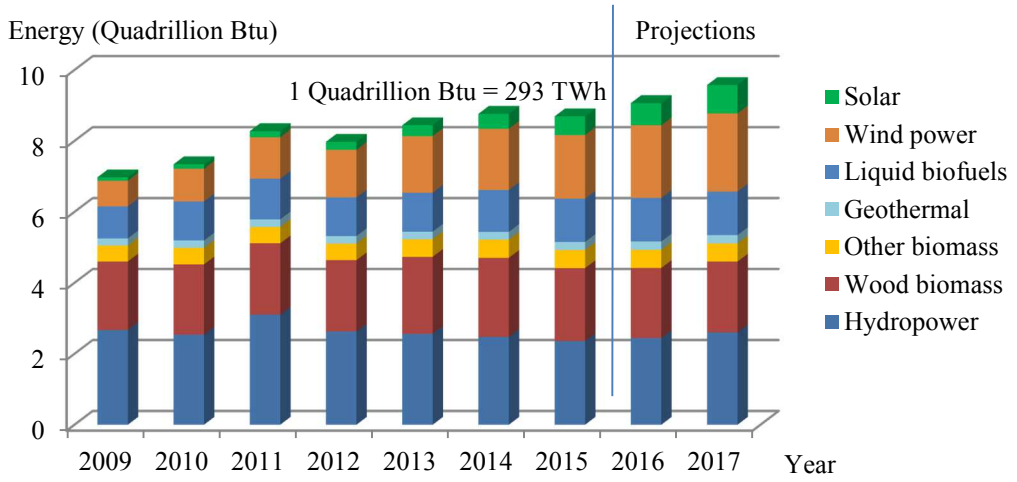

Fig. 1-1: U.S. market renewable energy usage [3]

Since renewable energy such as solar energy, fuel cell, wind energy, and hydro energy could be substituted for traditional energy generation resources, extensive research has been done on converting renewable energy into electric energy [4-14].

Numerous U.S. families have a residential stand-alone solar powered system installed in their homes. The direct benefits go to the power consumer, known as the user. The main service of a residential renewable energy system is to help the user reduce consumption of electricity supplied by the utility. However, making renewable energy systems that are beneficial to both the utility and the user is the goal of this thesis project. In a microgrid, each grid-tied renewable energy generation system is a distributed power generator. Those systems can help to improve the grid power factor by acting as reactive power compensators. Moreover, the systems can also perform as sub-generations that receive real power dispatch commands from the utility through communications. This means that the user can sell extra PV generated power back to the grid. When connected with the grid, the renewable energy systems are centrally controlled to serve the utility and the user, no matter where the energy system is located. Take a PV system as an example, the maximum power point tracking (MPPT) unit estimates instantaneous maximum PV power generation of each PV inverter system. The utility can allocate the active power dispatch command based on the PV power estimations from the MPPT and load power consumption estimations.

The scope of this thesis includes a literature review, an inverter circuit configuration design, controller designs for 2 kVA inverter stand-alone operation, controller designs for grid-tied mode operation, and a communication interface. The thesis is organized as follows. Chapter 1 addresses research background and motivation. In addition, it presents a literature review on the PV modeling, prominent PV inverter configurations, inverter filter topologies, and inverter

control strategies. Hardware component calculation and selection are also given at the end of the chapter. Chapter 2 describes different control resolutions for island mode inverter operation. To eliminate steady-state error, synchronous frame PI controller and proportional resonant (PR) controller are investigated. Chapter 3 discusses the grid-tied inverter controller design, and compares some grid synchronization techniques. Chapter 4 shows experimental results for stand-alone inverter and grid-connected inverter operations. A serial communication link has been established between the graphical user interface (GUI) and digital signal processor for the power flow manipulation. Finally, Chapter 5 contains the conclusion of this thesis and describes some future work which could be investigated.

1.2 Theoretical Background

1.2.1 Solar Energy

Solar energy systems convert the energy of the sun directly to electrical energy. Solar energy farms can generate a significant amount of electricity to feed the electrical systems [1]. Scaled-down solar systems can provide sufficient energy for residential and business utilization [9-11]. The solar cell is similar to a diode, and a practical model of the solar cell [6] is given in Fig. 1-2. The milliohms level resistance R_S represents the collector traces and external wires, and the parallel kilohms level resistance R_C is the internal resistance of the crystal [1].

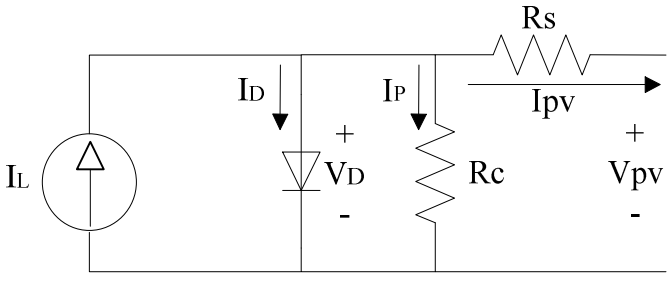

Fig. 1-2: Equivalent circuit of a solar cell

The PV cell output current is derived as (1.1) [6]. The source current I_{L} is dependent on the solar irradiance. Since the thermal voltage V_{T} and the reverse saturation current I_{S} are dependent to the temperature, the PV output current I_{PV} is dependent on the temperature. Thus, the PV output current is actually a function of irradiance and environmental temperature. Based on the practical solar cell model, PV output current-voltage (I-V) and power-voltage (P-V) curves are plotted with different irradiances and temperatures. The PV output I-V (Fig. 1-3) and P-V (Fig. 1-4) curves are created by varying irradiance. In Fig. 1-3, I_{sc} is the short circuit current and V_{oc} is the open circuit voltage. The PV output I-V (Fig. 1-5) and P-V (Fig. 1-6) curves are created by varying temperature.

$$I_{PV} = I_L - I_D - I_p = I_L - I_S\left(e^{v_D/\eta V_T} - 1\right) - \frac{v_D}{R_C} \tag{1.1}$$

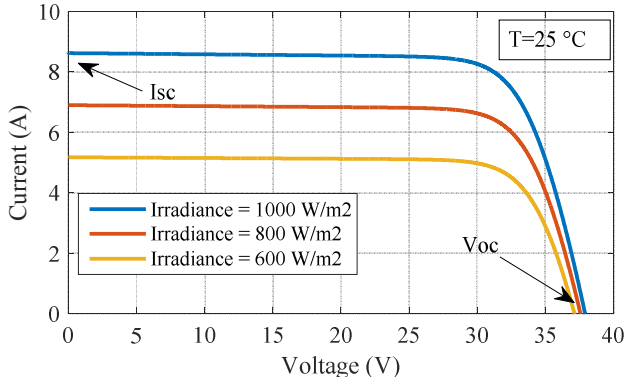

Fig. 1-3: I-V curves of a PV string (constant temperature)

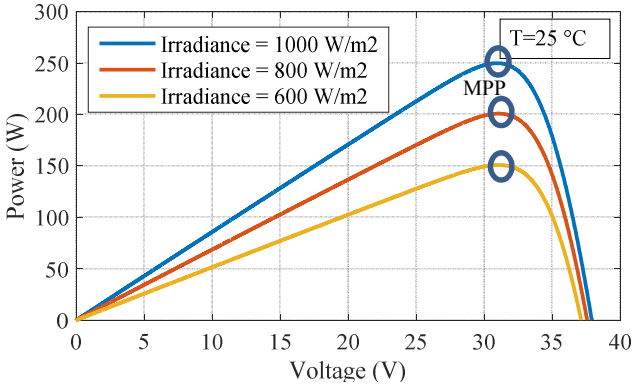

Fig. 1-4: P-V curves of a PV string (constant temperature)

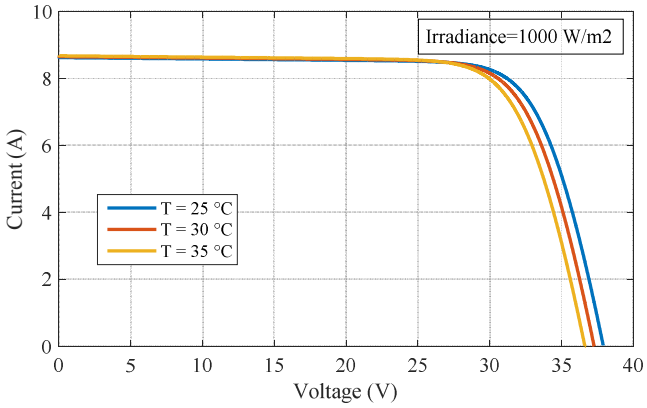

Fig. 1-5: I-V curves of a PV string (constant irradiance)

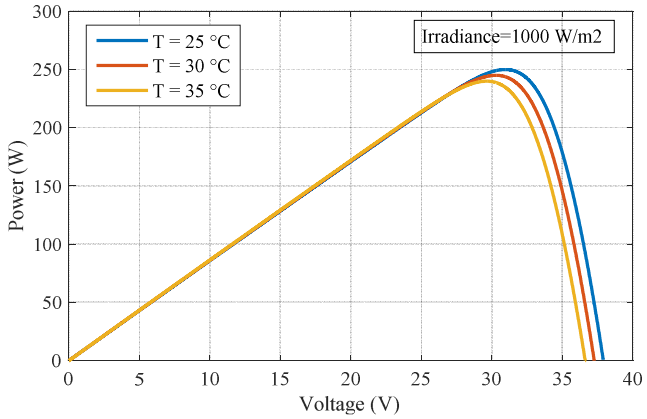

Fig. 1-6: P-V curves of a PV string (constant irradiance)

Since the maximum power output of PV changes as the irradiation and environmental temperature varies, maximum power point tracking algorithm must be implemented in PV applications to obtain the maximum power from a PV string for the sake of conversion efficiency. Many MPPT algorithms have been proposed and implemented [15]. The most common and basic MPPT techniques are perturb and observe (P&O) algorithm, incremental conductance algorithm, and fractional open-circuit voltage algorithm [15, 16].

There are many other maximum power point tracking techniques based on fuzzy logic and neural networks. However, the MPPT techniques are not the focus of this thesis. More related information can be found in [15].

1.2.2 Solar System Configurations

Photovoltaic modules feed DC current and voltage into the power electronics system. DC to DC converters are often used to amplify the low voltage generated by PV modules. And the inverters are utilized to convert the high level DC voltage to the AC voltage to supply the normal loads. The solar panel configuration affects the power electronics systems design. As to what configurations to choose, it depends largely on the residential environment and cost budget. Four basic solar system configurations are listed and discussed in the following session.

1.2.2.1 Single-Stage Centralized Inverter

In this configuration, PV panels are connected in series to form a PV string, in order to reach a higher voltage. These PV strings are then connected in parallel with power diodes to achieve higher power generation. This configuration is shown as in Fig. 1-7.

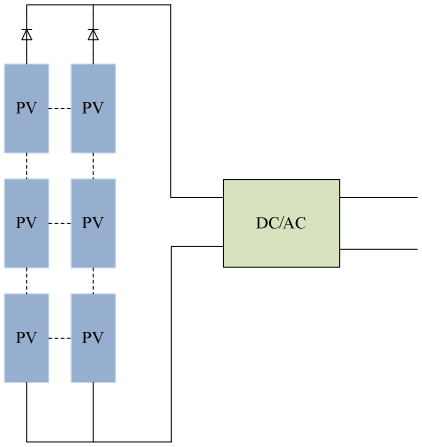

Fig. 1-7: Single-stage centralized inverter

In this configuration, it can be seen that all the PV strings are in parallel, and thus all the PV strings share the same voltage. Because of the irradiation shading or panel mismatch problems, the operating voltage may not be the maximum power point for all the PV strings [7]. This may result in poor energy harvesting. The benefit of choosing this configuration is its low cost [17].

1.2.2.2 Single-Stage String Inverter

Another single-stage PV inverter configuration is shown in Fig. 1-8. In this configuration, each PV string can have its own maximum power point if there is any partial shading or panel mismatch. Each string inverter is supposed to handle its own maximum power point tracking and power conversion control. For the power harvesting performance, string inverter configuration is superior compared to the single-stage centralized inverter. However, the string inverter configuration increases the total installation cost because an inverter is applied to each PV string [17].

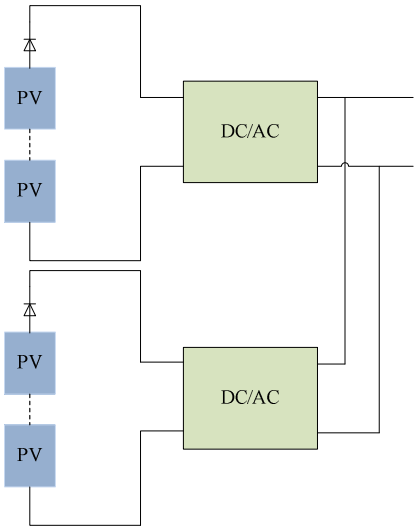

Fig. 1-8: Single-stage string inverter

1.2.2.3 Two-Stage String Inverter

A two-stage string inverter configuration is shown in Fig. 1-9. This configuration is popular due to its improved energy harvesting capability, modularity, and design flexibility [7]. Each PV string contains less solar panels which increases the system robustness. The first stage is to amplify the low DC voltage generated by solar panels to a higher level DC bus. The DC to DC converter should also handle the maximum power point tracking. The second stage controls the power conversion from DC to AC.

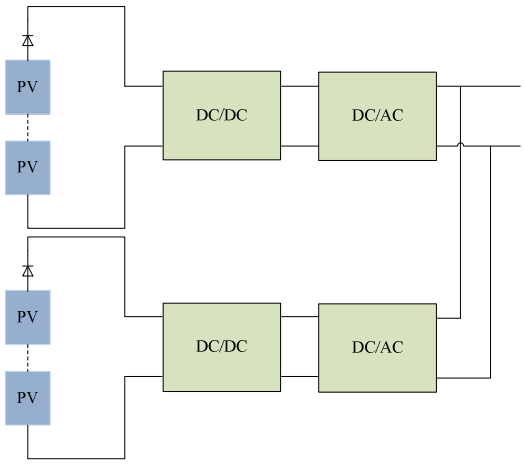

Fig. 1-9: Two-stage string inverter

1.2.2.4 Two-Stage Centralized Inverter

A two-stage centralized inverter configuration is shown in Fig. 1-10. The first stage is a modularized DC voltage amplification stage. The DC to DC converter handles the maximum power point tracking for the connected PV string. The second stage is a centralized DC to AC inverter. The following inverter design of this thesis is based on two-stage inverters. Using this configuration may reduce the cost of inverter stage; however, the centralized inverter can be larger.

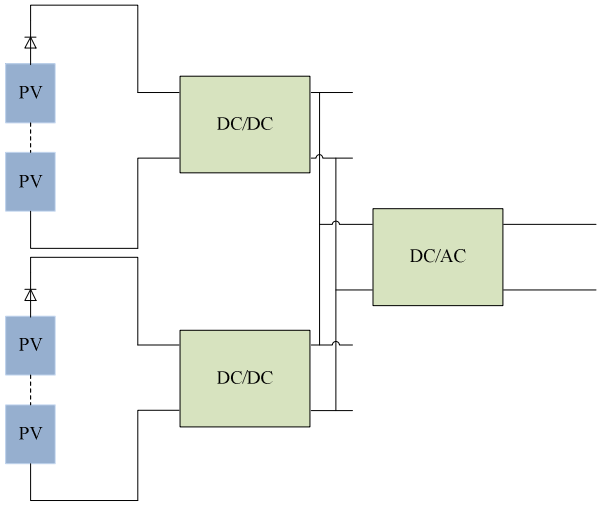

Fig. 1-10: Two-stage centralized inverter

1.2.3 DC/AC Inverter Topologies

There are many different single-phase inverter topologies. Based on the switch leg numbers, inverters can be sorted as a half-bridge inverter or a full-bridge (H-bridge) inverter. Based on the input sources, inverters can be divided into a current source inverter or a voltage source inverter [1, 18]. Comparing the inverter output peak voltage amplitude and input voltage amplitude, inverters can be organized as a boost inverter, buck inverter, or buck-boost inverter [1, 12]. In this thesis, an H-bridge inverter topology is chosen due to its simplicity and high efficiency. The H-bridge inverter is a full-bridge buck type voltage source inverter (VSI). The topology of an H-bridge inverter is shown in Fig. 1-11.

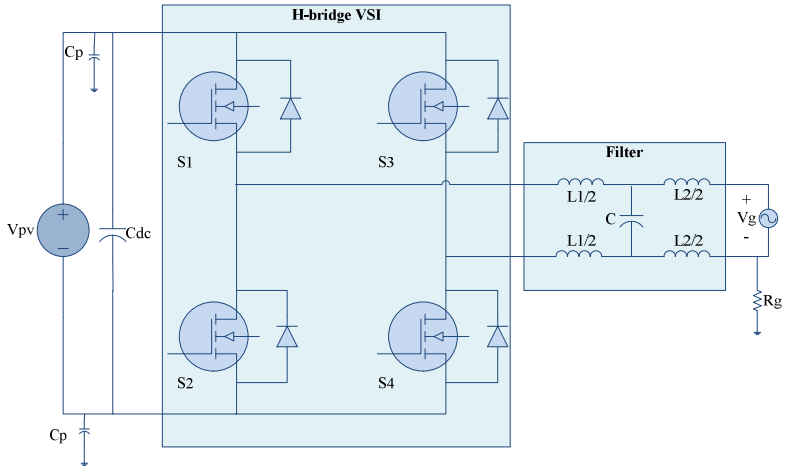

Fig. 1-11: Single-phase H-bridge inverter topology

1.2.4 Inverter Filter Topologies

For all H-bridge inverters, a low-pass output filter is needed to obtain the fundamental frequency output. Generally, there are four different types of H-bridge inverter filters. They are L filter, LC filter, LCL filter, and LLCL filter, respectively [13, 19].

The L type filter, shown in Fig. 1-12, consists of an inductor only. Over the entire frequency range, L type filters have an attenuation of -20 dB/dec. In order to suppress the output

current harmonics, a high value inductor is needed. A large inductance leads to a larger filter size and higher cost. The high voltage drop over the big inductor worsens the system dynamics [13].

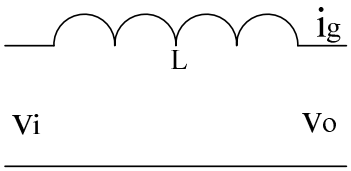

Fig. 1-12: L type filter

The LC filter, shown in Fig. 1-13, is a second-order filter with an attenuation of -40 dB/dec [2]. The LC filter design process is fairly easy. The trade-off of the design is that a higher capacitance may help reduce the cost of the inductor. However, the system may encounter inrush current and high reactive current flow into the capacitor at the fundamental frequency [13]. If an inverter is tied to the grid through an LC filter, the resonance frequency of the filter becomes dependent upon the grid impedance [20]. However, the LC filter is good fit for stand-alone inverters due to its compact size and good attenuation performance.

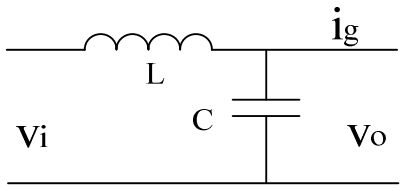

Fig. 1-13: LC type filter

The third-order LCL filter, displayed in Fig. 1-14, is widely used with grid-connected inverters due to its high attenuation beyond resonance frequency. Compared to the LC filter, the LCL filter gives a better decoupling capability between the filter and the grid impedance [13]. The design process of the LCL filter has to consider the resonance of the filter and the current ripple flowing through the inductors. Detailed LCL filter design procedures are given in the following section.

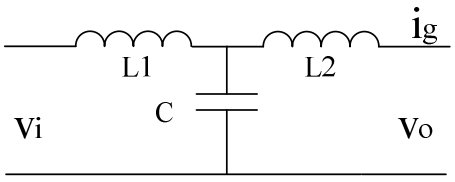

Fig. 1-14: LCL type filter

Another inverter filter configuration, the LLCL filter, is developed based on the LCL filter. A very small inductor is placed in series with the filter capacitor [19]. The structure of this LLCL filter is shown in Fig. 1-15. Compared to the conventional LCL filter, the LLCL filter can further reduce the grid-side inductance with a tuned trap at the switching frequency [19, 21]. However, the design and modeling process of the LLCL filter is relatively complex due to its high-order nature.

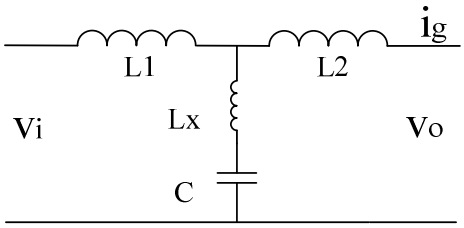

Fig. 1-15: LLCL type filter

The Bode plot shown in Fig. 1-16 displays an L filter, LCL filter, and LLCL filter in frequency domain. It can be seen that the LLCL filter has the same frequency response characteristics as the LCL filter at the low frequency. Both of the two filters require design attention to the resonance frequency, which may lead to an unstable system.

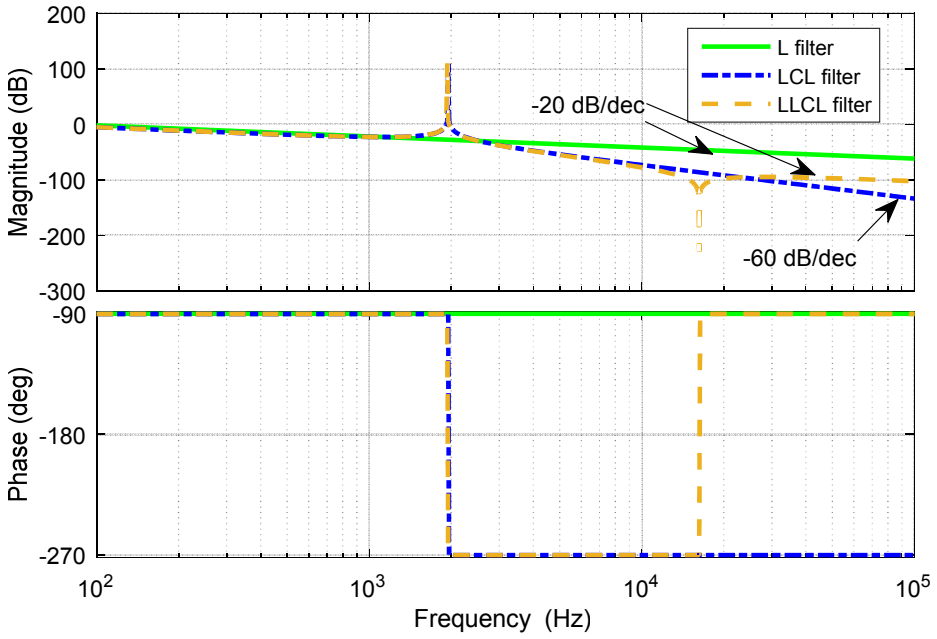

Fig. 1-16: Bode plot of different filter types

1.2.5 LCL Filter Design Considerations

Based on the above inverter filters review, a LCL type filter is chosen due to its good performance and relative simplicity. The LCL filter design procedures are described and discussed in [13, 22-24]. Typically, the filter design requirements for the grid-tied mode are stricter than the design requirements for the stand-alone inverter. The filter designed for the grid-tied inverter will satisfy the stand-alone inverter operation. The inverter-side filter inductance selection is based on the allowable maximum current ripple and harmonic current attenuation. The capacitance is selected based on the reactive power absorbed at the rated conditions.

To design an LCL filter, there are some guidelines to follow. The total inductance ($L_1 + L_2$) should be less than 10 % of the system base inductance to avoid large voltage drop across the inductors [23]. The current ripple should be limited to 20 % of the rated current. The capacitance can neither be too large nor too small. A small value capacitance diminishes the attenuation capability of the LCL filter; however, a large value capacitance leads to a high reactive power

[23]. The resonance frequency of the LCL filter should always be designed within the range of (1.2) to ensure good system dynamics and avoid resonance problems [24]. In (1.2), f_g represents the grid fundamental frequency and f_s is the inverter sampling frequency. The grid-side inductance L_2 should only be a fraction of the inverter-side inductance $L_1$to ensure the system stability. Last but not least, the inverter current output harmonics should be limited according to IEEE 519-1992 [25].

$$10f_g < f_{res} < 0.5f_s \tag{1.2}$$

Ignoring the parasitic resistances of the inductors and capacitor, the resonance frequency of the LCL filter can be calculated as in (1.3).

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_1+L_2}{L_1L_2C}} \tag{1.3}$$

The PWM modulation type affects the inverter filter design. Unipolar modulation is popular due to its higher efficiency. With the same carrier frequency, the equivalent switching frequency of the unipolar modulation is doubled compared to the switching frequency of the bipolar modulation method [26]. Thus, the LCL filter size is smaller when unipolar modulation is applied. However, bipolar modulation has much less leakage current than unipolar modulation in a PV inverter without galvanic isolation [27]. With the configuration as in Fig. 1-11 (R_g = 0.4 Ω, C_p = 5 nF), a comparison of the leakage current in the PV inverter is performed between unipolar and bipolar switching with the same equivalent switching frequency. The pink line in Fig. 1-17 shows the leakage current in a PV inverter when unipolar switching is applied, whereas the pink line in Fig. 1-18 shows the leakage current in a PV inverter when bipolar switching is used. In this thesis, bipolar modulation is adopted, since the inverter is mainly designed for a two-stage PV inverter without galvanic isolation.

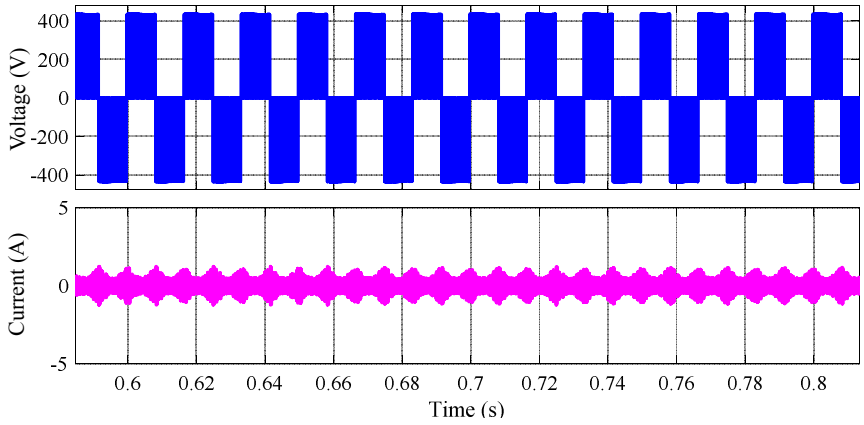

Fig. 1-17: PV inverter leakage current with unipolar switching

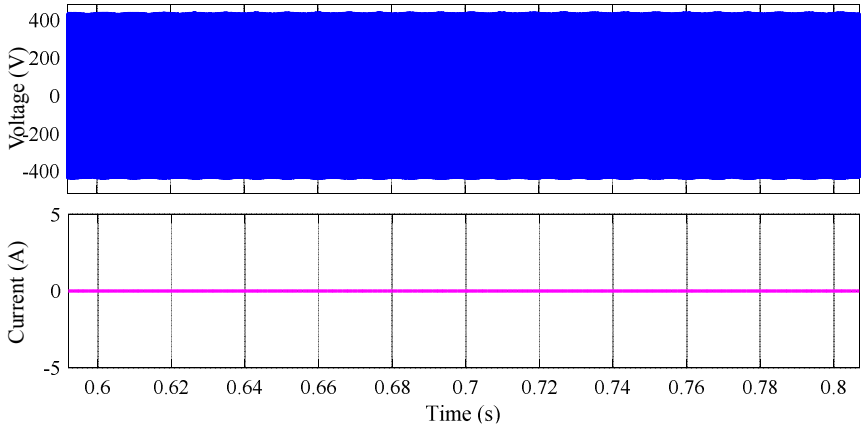

Fig. 1-18: PV inverter leakage current with bipolar switching

To derive the LCL filter transfer function, the grid voltage is considered to be an ideal source which is a short circuit for all harmonics [19]. Thus the grid voltage is set to be zero. The derived LCL filter transfer function is shown as (1.4). The resonance frequency is shown in the undamped LCL filter Bode plot. The resonant poles introduced by the LCL filter may affect the system stability [28], a passive damped LCL filter is often used in the conventional PV inverter design [7]. The damping resistor is either placed in parallel with the filter capacitor or in series with the filter capacitor as illustrated in Fig. 1-19. The damped LCL filter transfer function is derived as in (1.5) when the damping resistance is in series with the filter capacitor. The passive

damped LCL filter frequency response is shown in Fig. 1-20. However, it is obvious that the damping resistor reduces the efficiency of the overall system. Thus, an active damping method is preferred.

$$H_{LCL}(s) = \frac{i_g(s)}{v_i(s)} = \frac{1}{L_1L_2Cs^3+(L_1+L_2)s} \tag{1.4}$$

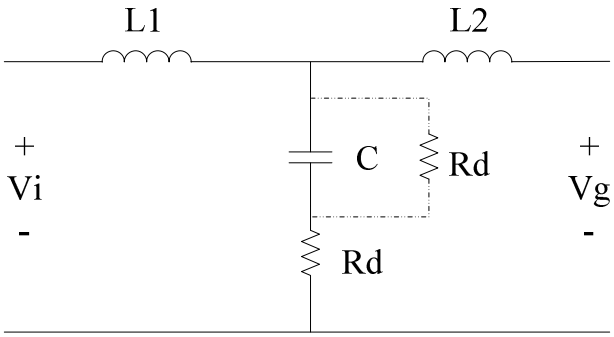

Fig. 1-19: LCL filter passive damping resistance placement

$$H_{d-LCL}(s) = \frac{i_g(s)}{v_i(s)} = \frac{R_dCs+1}{L_1L_2Cs^3+(L_1+L_2)R_dCs^2+(L_1+L_2)s} \tag{1.5}$$

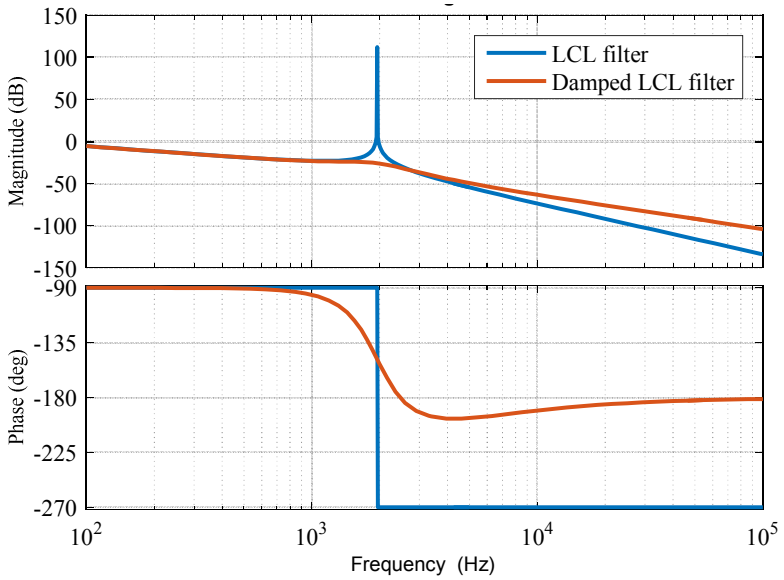

Fig. 1-20: LCL filter with passive damping resistance

1.2.6 Active Damping

For LCL filters, the resonance frequency should fall into either the region shown in (1.6) or the region in (1.7). It is proven in [28-29] that the LCL filters with a resonance frequency higher than one sixth of the controller sampling frequency does not require damping for the resonance. However, for the LCL filters whose resonance frequency falls into the region in (1.6), a resonance damping technique is necessary [28-29]. Many active damping techniques have been proposed and studied [28-42]. Even when the damping is not required, applying resonance damping can improve the system performance [41]. Those active damping techniques can be roughly divided into the notch filter method and the virtual resistance method.

$$10f_g < f_{res} < \frac{f_s}{6} \tag{1.6}$$

$$\frac{f_s}{6} < f_{res} < \frac{f_s}{2} \tag{1.7}$$

1.2.6.1 Notch Filter

An effective active damping method is to design a notch filter within the current control loop. The control block can be found in Fig. 1-21. G_c is the transfer function of the current loop controller and G_{notch} represents the transfer function of the notch filter. The transfer function of a notch filter is given by (1.8).

$$G_{notch} = \frac{s^2+(2\pi f_{res})^2}{s^2+2k_a+(2\pi f_{res})^2} \tag{1.8}$$

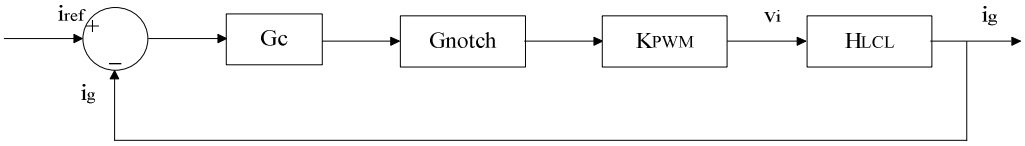

Fig. 1-21: Active damping technique with a notch filter

The essential idea of the notch filter active damping method is to tune a second order filter with a notch frequency that is equal to the LCL resonance frequency as illustrated in Fig. 1-22. Since the notch filter is usually designed at a fixed frequency, using the notch filter damping

technique may result in poor performance when the grid impedance largely varies [38]. In addition, the filter parameters may not perfectly match the initial design. As shown in Fig. 1-22, when the grid-side inductance L_2 increases 50 %, the designed notch filter loses its damping effectiveness. In [39], a more robust notch filter with a wide bandwidth is proposed and simulated.

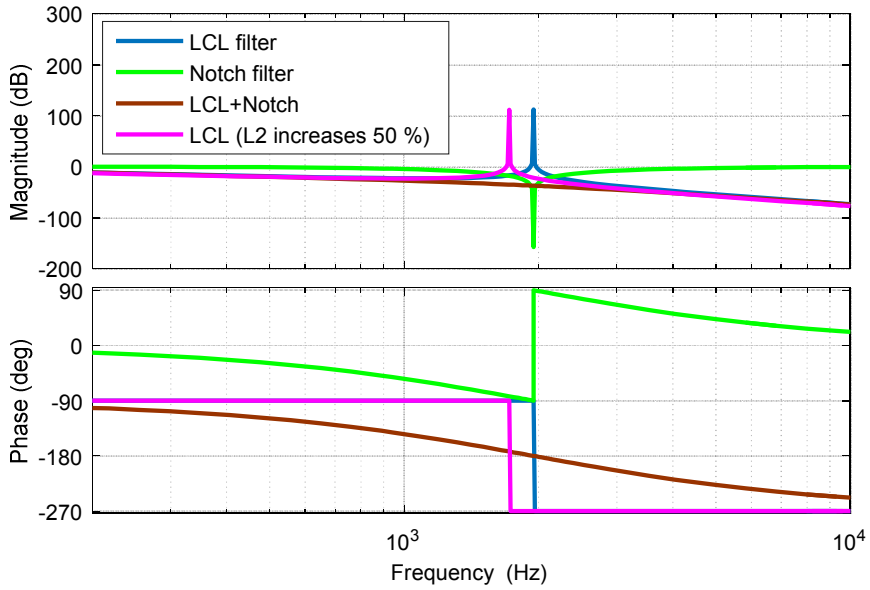

Fig. 1-22: LCL filter active damping with a notch filter

1.2.6.2 Virtual Resistance

There are two popular virtual resistance active damping techniques. One is to use the grid current and filter capacitor current as feedback signals and the other one is to use grid current only to achieve damping [41-42]. Adding the filter capacitor current feedback as in Fig. 1-23, is equivalent to adding the virtual impedance Z_1 in parallel with the filter capacitor as shown in Fig. 1-24 [34]. The control strategy only using the grid current feedback is given in Fig. 1-25. Its equivalent circuit is derived in Fig. 1-26 [42]. The virtual impedance Z_2 is added in parallel with the grid side inductor. The method shown in Fig. 1-23 requires two current sensors, whereas the

control method in Fig. 1-25 only requires one current sensor. However, the control method in Fig. 1-25 contains a high pass filter in the feedback loop which may amplify the high frequency noise.

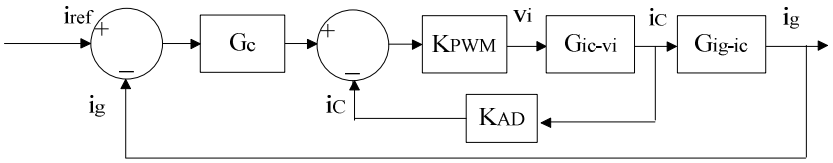

Fig. 1-23: Active damping with the grid injected current and filter capacitor current

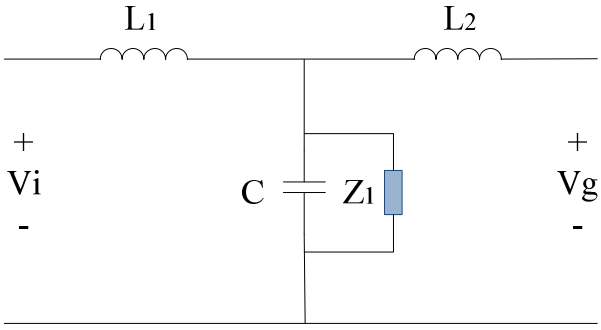

Fig. 1-24: Equivalent circuit with filter capacitor current feedback

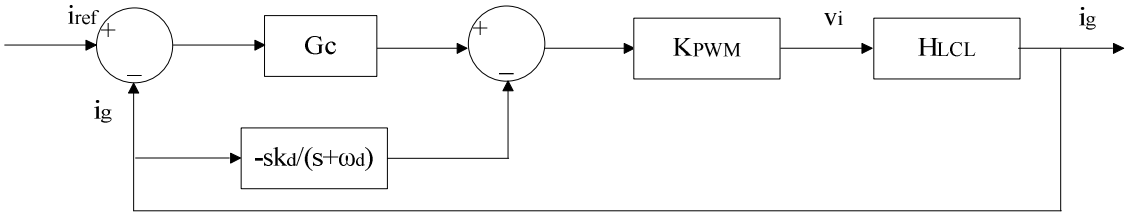

Fig. 1-25: Active damping with the grid injected current only

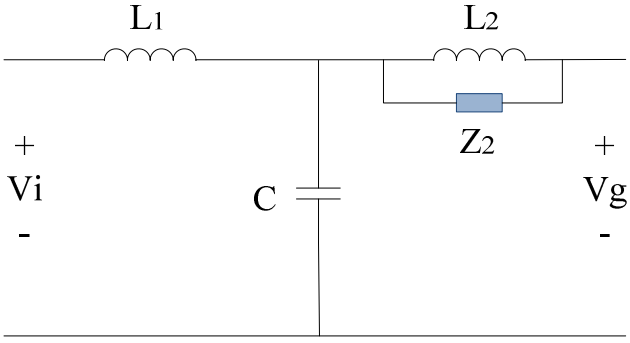

Fig. 1-26: Equivalent circuit with high pass filtered grid current feedback

1.3 Hardware Component Sizing

According to [22], the formula used to calculate the minimum inverter-side filter inductance L_1 is given in (1.9).

$$L_1 > \frac{\varepsilon V_{DC}}{4 f_{sw} I_{rated} \xi} \tag{1.9}$$

When the inverter is unipolar modulated, the coefficient ε is 1. When the inverter uses bipolar modulation, the coefficient ε is 2. In (1.9), f_{sw} represents the switching frequency and I_{rated} is the inverter rated current. ξ is the allowable current ripple ratio, and V_{DC} represents the DC input voltage. In this thesis, the allowed current ripple ratio ξ is chosen to be 20 %.

The maximum total inductance ($L_1 + L_2$) should be less than the 10 % system base inductance to avoid large voltage drop across the inductors, as shown in (1.10). In (1.10), S_{rated} is the system rated apparent power, and V_{rated} is the rated AC output voltage. Based on the calculation results from (1.9) and (1.10), the inverter-side inductance L_1 should be at least 1.9 mH, and the total inductance of the LCL filter should be less than 7.6 mH. As previously discussed, the capacitance is limited by (1.11). Using (1.12) to decide the grid-side inductance L_2. The coefficient γ is chosen to be 0.5 in (1.12).

$$L_1 + L_2 < 10\% \frac{{V_{rated}}^2}{2\pi f_g S_{rated}} \tag{1.10}$$

$$C < 20\% \frac{S_{rated}}{2\pi f_g {V_{rated}}^2} \tag{1.11}$$

$$L_2 = \gamma L_1 \tag{1.12}$$

Let inverter output voltage and current be,

$$v_o(t) = \sqrt{2} V_{o\_rms} \sin(\omega_0 t) \tag{1.13}$$

$$i_o(t) = \sqrt{2} I_{o\_rms} \sin(\omega_0 t + \varphi) \tag{1.14}$$

Thus, the inverter instantaneous output power is,

$$p_{out}(t) = v_o(t) \times i_o(t) = V_{o\_rms} I_{o\_rms} cos\varphi - V_{o\_rms} I_{o\_rms} \cos(2\omega_0 t + \varphi) \tag{1.15}$$

In (1.15), there is a double line frequency ($2\omega_0$) component in the inverter output power. This double line frequency harmonic is also seen in the inverter input. Thus, a DC-link capacitor should be utilized to limit the double grid line frequency voltage ripple at the inverter DC input. Sufficient capacitance would help to lower DC-link voltage fluctuations and reduce the inverter output current distortion, which is undesirable for power decoupling [7]. However, choosing an oversized DC-link capacitor increases design cost. The following analysis shows how to size the capacitance of a DC-link film capacitor for inverters.

Since the apparent power S_{rated} is,

$$S_{rated} = V_{o\_rms} \times I_{o\_rms} \tag{1.16}$$

Rewrite the output power as,

$$p_{out}(t) = S_{rated} cos\varphi + S_{rated} \cos(2\omega_0 t + \varphi) \tag{1.17}$$

The inverter input power is,

$$p_{in}(t) \cong V_{dc} \times [I_{dc} + i_r(t)] = V_{dc} I_{dc} + V_{dc} i_r(t) \tag{1.18}$$

Neglecting circuit power loss,

$$p_{in}(t) = p_{out}(t) \tag{1.19}$$

Since the DC-link capacitor filters out high frequency components, the double-line frequency component is expressed as,

$$V_{dc} i_r(t) = S_{rated} \cos(2\omega_0 t + \varphi) \tag{1.20}$$

Thus, the double-line frequency current component at the DC side is,

$$i_r(t) = \frac{S_{rated}}{V_{dc}} \cos(2\omega_0 t + \varphi) = I_r \cos(2\omega_0 t + \varphi) \tag{1.21}$$

Assume the dc side maximum ripple voltage to be 5 % of the DC nominal voltage. The minimum DC-link capacitance is calculated as,

$$C_f = I_r / 2\omega_0 V_{r\_max} = S_{rated} / 4\pi f_0 V_{dc} V_{r\_max} \tag{1.22}$$

Based on the analysis and calculations shown above, a minimum capacitance of 500 μF capacitor is needed. All the parameters for the system is given in Table 1-1. The simulations conducted in the following chapters are based on the parameters in Table 1-1.

Table 1-1: Designed parameters for the single-phase inverter

Parameter	Value	Parameter	Value
DC bus V_{dc}	400 V	Sampling frequency f_{s}	30 kHz
Switching frequency f_{sw}	30 kHz	L_1	2 mH
C	10 μF	L_2	1 mH
C_{f}	500 μF	Resonance frequency f_{res}	1.95 kHz

Chapter 2 Controller Design of Stand-Alone Inverter

Residential inverters are expected to be able to work off-grid to support critical loads as uninterruptible power supplies. The design of a dual-loop controlled stand-alone inverter is described in this chapter. The inner loop regulates current, and outer loop regulates inverter output voltage across the capacitor of the filter. The inner current control loop can either regulate the current flowing through the inverter-side inductor, or current flowing through the capacitor of the filter. Since traditional PI controllers cannot achieve zero steady-state error while tracking sinusoidal signals, direct quadrature (DQ) frame controllers and PR controllers are investigated and applied. Using the synchronous frame outer control loop, a comparison on the control performance between the two inner current feedback methods is performed. The island mode inverter circuit and conventional control diagram is given in Fig. 2-1. Simulation results are provided within this chapter.

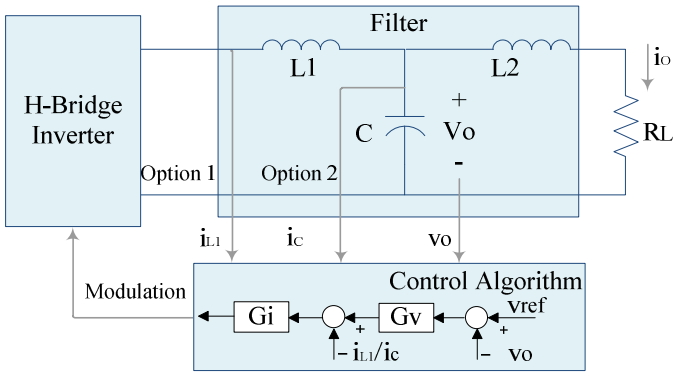

Fig. 2-1: Island mode inverter circuit diagram

2.1 Inner Current Loop Design

Generally, the current inner loop has two options. One is to use the inverter-side inductor current i_{L1} as the feedback value [2]. The other one is to adopt the current flowing through capacitor i_C as the feedback value. The control diagrams of inner feedback systems using both options are shown in Fig. 2-2 and Fig. 2-3, respectively. Comparing these two control diagrams,

it is seen that the capacitor current feedback control method includes the load current within the control loop. Thus, by using capacitor current feedback method, the system can obtain better performance when load changes. According to [2], the worst control design condition for stand-alone inverter is in no load condition. Therefore, the load current is assumed to be zero in Fig. 2-3. Thus, the control plants in Fig. 2-2 and Fig. 2-3 are identical.

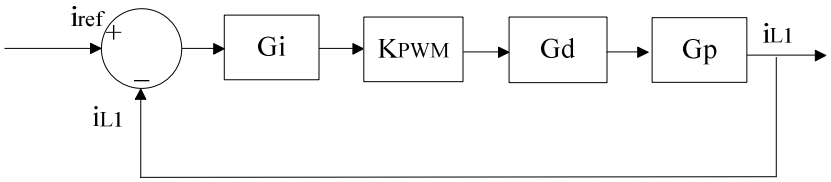

Fig. 2-2: Inner control system diagram using inverter-side inductor current i_{L1} feedback

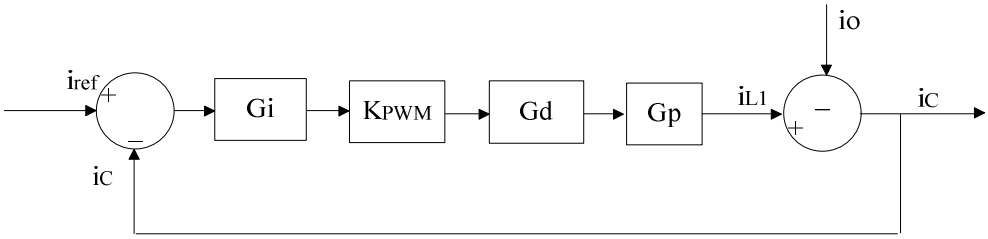

Fig. 2-3: Inner control system diagram using capacitor current i_C feedback

At least one switching period delay T_s should be considered for digital implementation since the modulation signal will not update until the next switching cycle [40]. The delay block G_d shown as (2.1) is a second order Pade approximation of the pure switching cycle delay. According to the derived small-signal mode in [2, 43], the inverter stand-alone mode control plant G_P is given as (2.2). The control diagram shown in Fig. 2-3, the uncompensated inner control loop plant can be derived as (2.3). A PI controller is used as the compensator for the inner control loop. The compensated open loop is derived as (2.4) in the Laplace frequency domain.

$$G_d = e^{-sT_s} = \frac{12-6sT_s+(sT_s)^2}{12+6sT_s+(sT_s)^2} \tag{2.1}$$

$$G_p = \frac{1}{sL_1} \tag{2.2}$$

$$G_{ip} = K_{pwm} G_d G_p \tag{2.3}$$

$$G_{ip\_c} = \frac{k_p s + k_i}{s} G_{ip} \tag{2.4}$$

The PI compensator is designed to boost the phase margin of the uncompensated transfer function (2.3) to increase the system stability. The crossover frequency of the compensated system should be less than one tenth of the switching frequency for good switching noise rejection, and higher than ten times of the grid frequency for fast dynamics [4]. The desired phase margin and gain margin are larger than 45 degrees and 7 dB, respectively. The uncompensated and compensated Bode plots are shown in Fig. 2-4. The blue line is the Bode plot of the uncompensated plant. The green line shows the open-loop Bode plot of the compensated system. As we can see from Fig. 2-4, the phase margin is 48.4 degrees, the gain margin is 8.14 dB, and the crossover frequency is designed to 2.9 kHz. The stability of the compensated system is verified by Nyquist stability criterion. The PI compensator is given as (2.5). The unit step response is shown in Fig. 2-5. The step response overshoot is 24.6 % and the settling time is 0.831 ms.

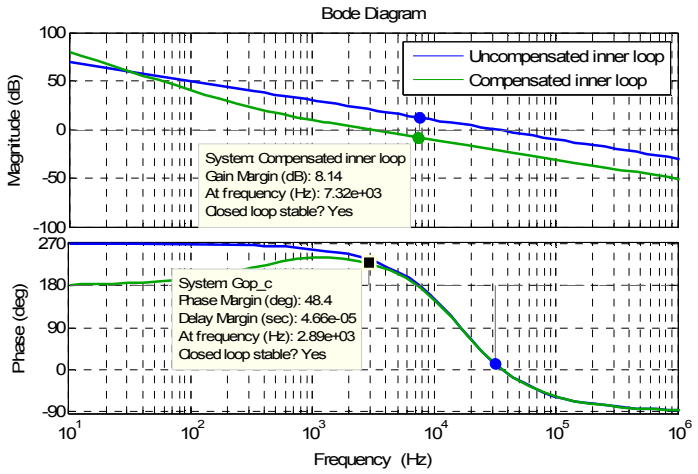

Fig. 2-4: Bode plots of the uncompensated and compensated inner loop

$$G_i = \frac{0.09s+200}{s} \tag{2.5}$$

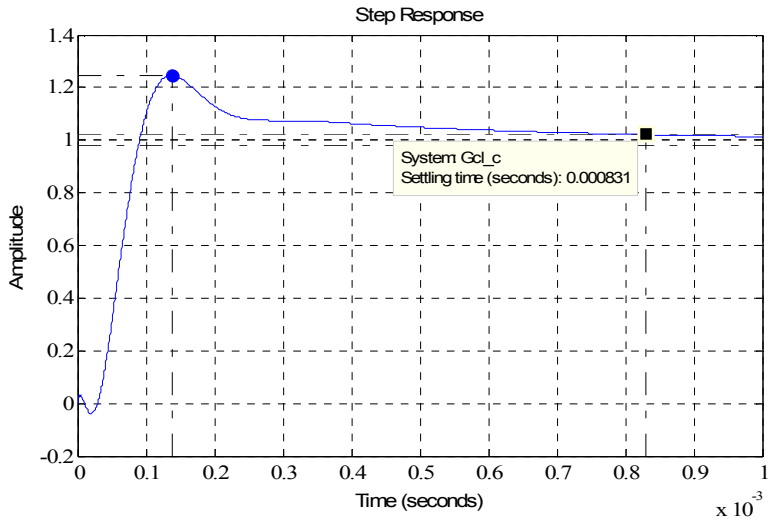

Fig. 2-5: Step response of the compensated inner control loop

2.2 Outer Current Loop Design

The outer control loop is designed to regulate the inverter output voltage across the filter capacitor C. The simplified control diagram is shown in Fig. 2-6.

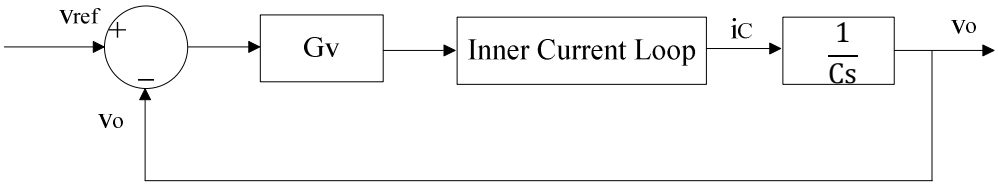

Fig. 2-6: Outer loop control diagram

The outer loop PI controller is designed to provide a satisfactory phase margin for the uncompensated plant to achieve the system stability. The crossover frequency of the dual-loop compensated system should be approximately ten times larger than the grid fundamental frequency and less than the inner loop crossover frequency. The uncompensated and compensated Bode plots are shown in Fig. 2-7. The blue line is the Bode plot of the uncompensated plant. The green line shows the open-loop Bode plot of the compensated system.

As we can see from Fig. 2-7, the phase margin is 62.2 degrees and the gain margin is 13.7 dB. The crossover frequency is about 725 Hz. When the gain of the compensated open-loop system is higher than 0 dB, there is no negative or positive phase crossing through the +/- 180º phase line. The number of the compensated open-loop system RHP poles is zero. According to Nyquist stability criterion, the compensated closed-loop system is stable. The PI compensator is given as (2.6). The unit step response is shown in Fig. 2-8. The step response overshoot is 16.4 % and the settling time is 2.32 ms. Apply the designed current loop PI controller and voltage loop PI controller to the Matlab™ Simulink circuit model, the outer loop voltage tracking error is shown in Fig. 2-9. The voltage tracking error shown in Fig. 2-9 has a peak value of 22 V at the fundamental frequency. To eliminate the voltage tracking error, a synchronous rotating frame DQ control [9] or a stationary reference frame proportional resonant control should be adopted [7]. More detail is given in the following sessions.

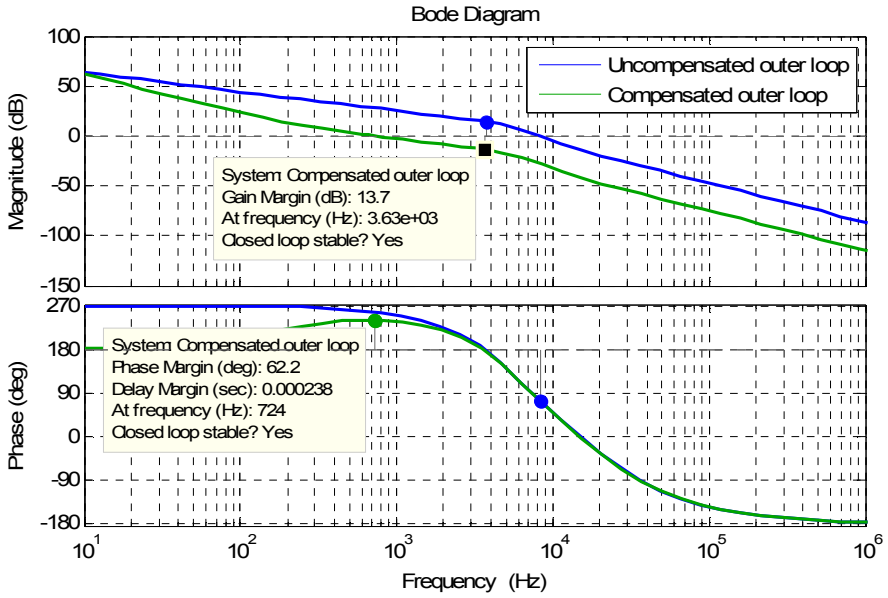

Fig. 2-7: Bode plots of the uncompensated and compensated outer voltage loop

$$G_v = \frac{0.039s+50}{s} \tag{2.6}$$

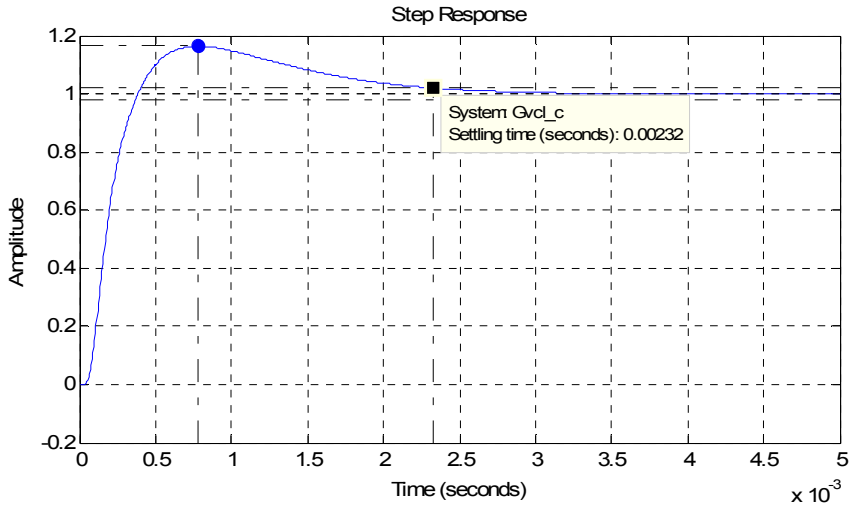

Fig. 2-8: Step response of the compensated outer voltage loop

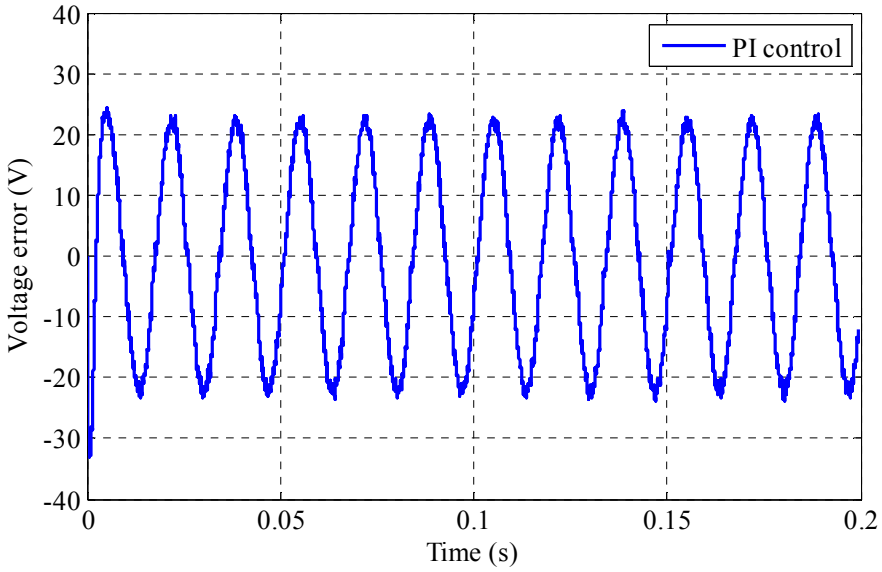

Fig. 2-9: Dual-PI controlled inverter voltage tracking error

2.3 DQ Frame Control

Synchronous rotating frame DQ control can be used to eliminate tracking error for AC quantities in dual-loop control systems [9, 10]. In the DQ rotating frame, the AC quantities in the αβ stationary frame become DC quantities as the DQ frame rotates at the same fundamental angular frequency as the AC quantities [2]. Traditional systems with DQ control method perform both the current and voltage loops in synchronous rotating frame. Alternative methods have been

reported in [2, 9]. Those methods only apply DQ based control to outer voltage loop. The obvious advantage of those methods is that those controls are easy to implement without generating β components. The control diagram is shown in Fig. 2-10. The state-space form equations shown as (2.7) and (2.8) describe the relationship between synchronous rotating frame and stationary reference frame [9, 10].

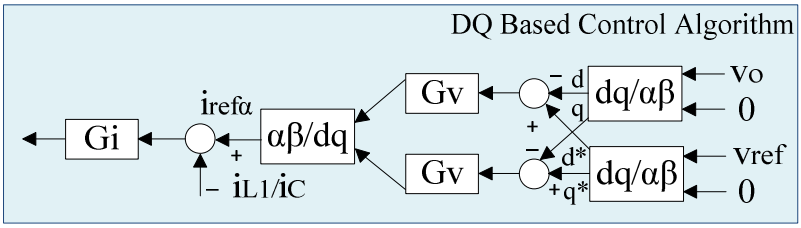

Fig. 2-10: A DQ based control diagram of single-phase inverters

$$\begin{bmatrix} y_d \\ y_q \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) \\ -\sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{2.7}$$

$$\begin{bmatrix} y_\alpha \\ y_\beta \end{bmatrix} = \begin{bmatrix} \cos(\omega t) & -\sin(\omega t) \\ \sin(\omega t) & \cos(\omega t) \end{bmatrix} \begin{bmatrix} x_d \\ x_q \end{bmatrix} \tag{2.8}$$

Applying the DQ frame control to the single-phase H-bridge inverter, a comparison of the control performance between the two inner current feedback methods (as shown in Fig. 2-2 and Fig. 2-3) is performed. The comparison result is given in Fig. 2-11. At 0.05 s, the load changes to 1 kW from no load condition. The load reaches 2 kW at 0.1 s, and drops back to no load condition at 0.15 s. The capacitor current feedback control method shown in Fig. 2-3 is adopted since it provides more robust performance when load changes. In [2], the step load performance is improved by adding an additional load current feedback besides the inverter-side inductor current inner loop feedback. Doing so will increase the overall design cost since two current sensors are utilized. The voltage and current responses with step load change are shown in Fig. 2-12 and Fig. 2-13, respectively. The voltage tracking error of the H-bridge inverter, where DQ frame control is applied, is shown in Fig. 2-14. The total harmonics distortion (THD) of the

inverter voltage output is: 0.39 % with 1 kW load, 0.37 % with 2 kW load, and 0.40 % with no load.

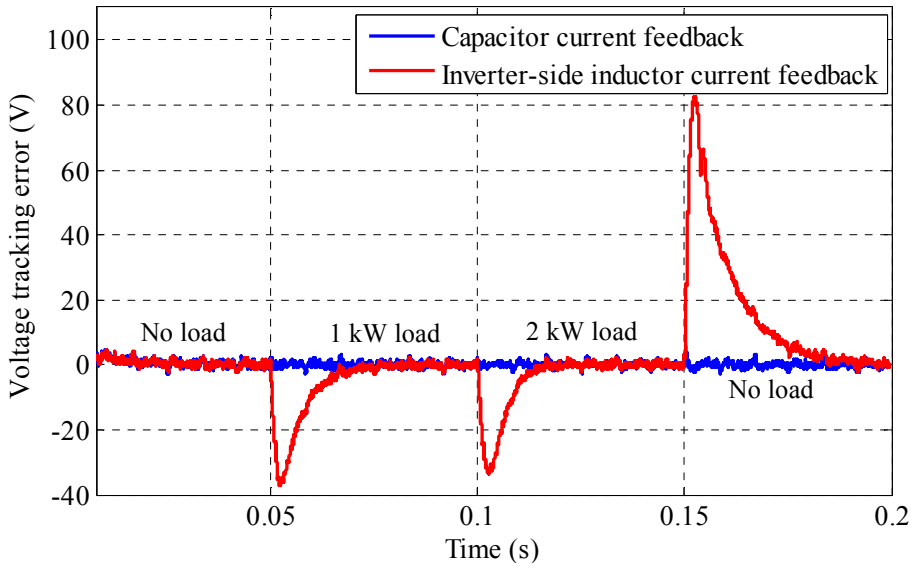

Fig. 2-11: Comparison of control performance between the two inner feedback methods

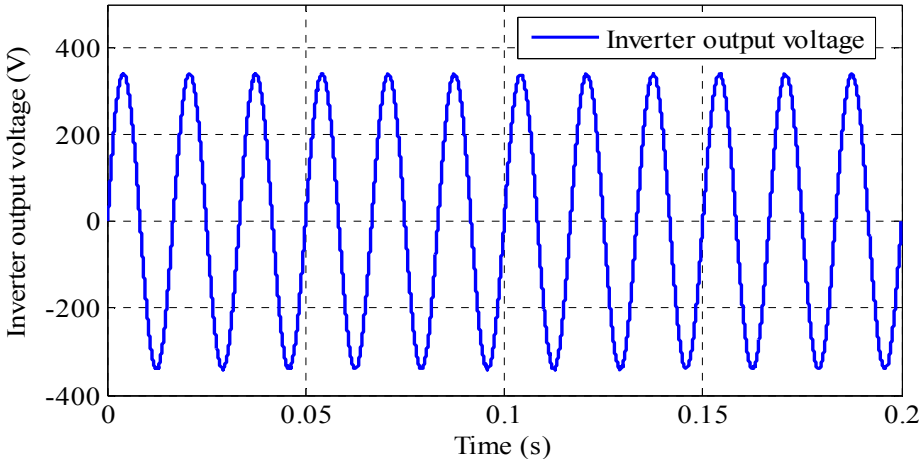

Fig. 2-12: Inverter output voltage

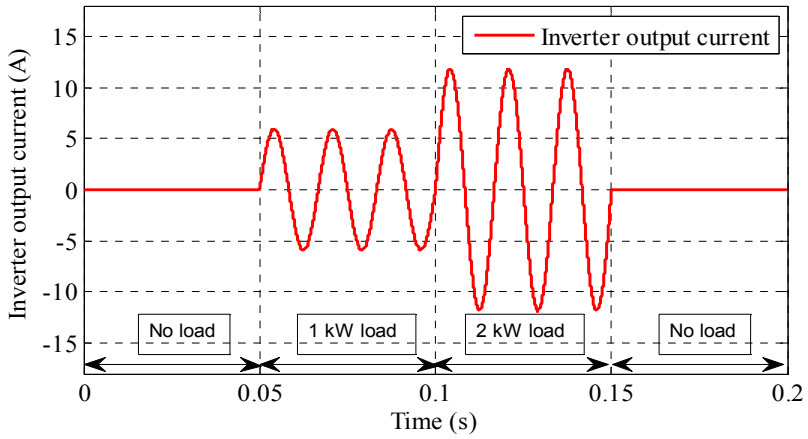

Fig. 2-13: Inverter output current

Fig. 2-14 shows that the DQ frame control enables the single-phase H-bridge inverter control system to achieve zero steady-state tracking response. Thus, the DQ frame control improves the inverter voltage output quality compared to the dual-PI control.

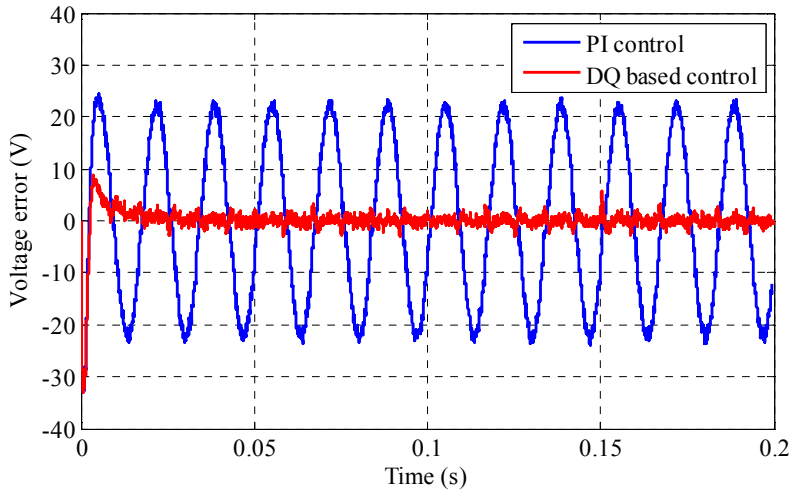

Fig. 2-14: Voltage tracking error comparison between PI control and DQ frame control

Generally, the power factor for a 2 kVA stand-alone inverter is between 0.707 and 1. The inverter step load output performance with 1.4 kW resistive load and 1.4 kVar inductive load is shown in Fig. 2-15. The THD of the inverter voltage output is 0.09 %. The inverter step load output performance with 1.4 kW resistive load and 1.4 kVar capacitive load is displayed in Fig. 2-16. The THD of the inverter voltage output is 0.34 %.

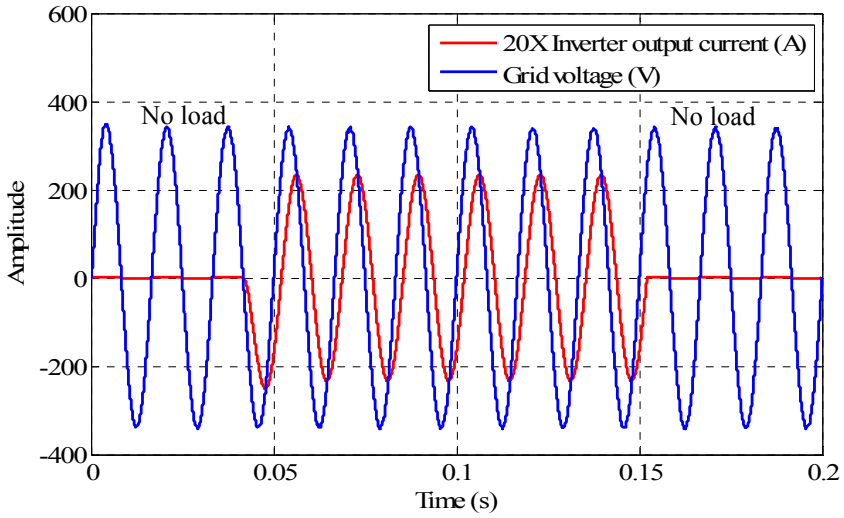

Fig. 2-15: Inverter output with 1.4 kVar inductive load and 1.4 kW resistive load

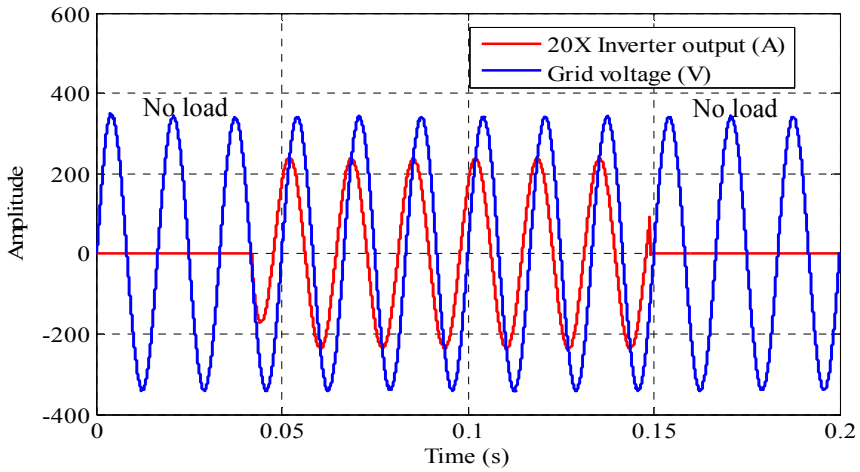

Fig. 2-16: Inverter output with 1.4 kVar capacitive load and 1.4 kW resistive load

2.4 Proportional Resonant Control

An alternative control method to achieve system zero steady-state error is using a proportional resonant controller [44]. (2.9) shows the transfer function of a PR controller. The k_{p} is the proportional gain term and the k_{i} parameter is the integral gain term. The ω_0 is the resonant angular frequency which is set to be the line angular frequency.

Fig. 2-17 and Fig. 2-18 are Bode plots of PR controllers with the same proportional gain term and Bode plot of PR controllers with the same integral gain term, respectively. From Fig. 2-

17 and Fig. 2-18, one can observe that the magnitude of the base of PR controller increases as the integral gain term k_{i} increases and the magnitude of the resonant part of the PR controller accrues as the proportional gain term k_{p} increases. It can also be seen that the PR controller can provide infinite gain at the fundamental frequency which is the reason that PR controller can eliminate steady-state tracking error. In the αβ stationary frame, a PR controller is equivalent to a PI controller in the synchronous DQ frame. A detailed analysis is given in [2]. It is well known that the PR controller described above is sensitive to resonance frequency drift due to the implementation error caused by Tustin transformation [2]. The nonideal PR controller shown as (2.10) provides a bandwidth for the resonant control part [44, 45]. A nonideal PR controller is less sensitive to resonance frequency drift. The ω_{b} is the bandwidth around the resonance frequency. Fig. 2-19 shows PR controllers with the same proportional gain term in the frequency domain. Fig. 2-20 shows PR controllers with the same integral gain term in the frequency domain.

$$G_{PR}(s) = k_p + \frac{k_i s}{s^2+\omega_0^2} \tag{2.9}$$

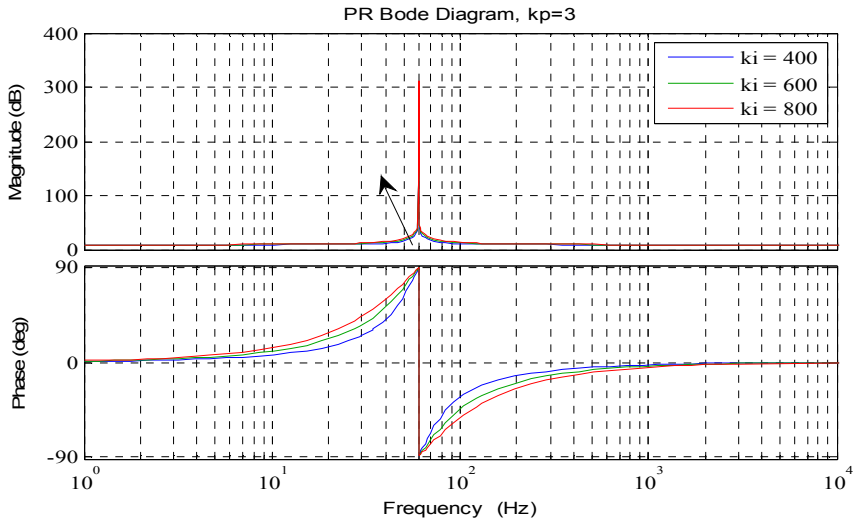

Fig. 2-17: Bode plot of PR controllers with a fixed proportional gain term

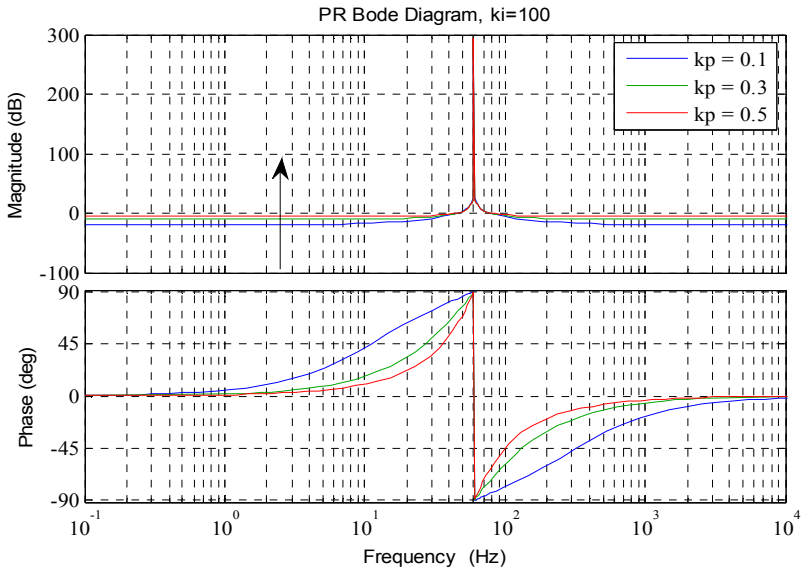

Fig. 2-18: Bode plot of PR controllers with a fixed integral gain term

$$G_{PR}(s) = k_p + 2k_i \frac{\omega_b s}{s^2 + 2\omega_b s + \omega_0^2} \tag{2.10}$$

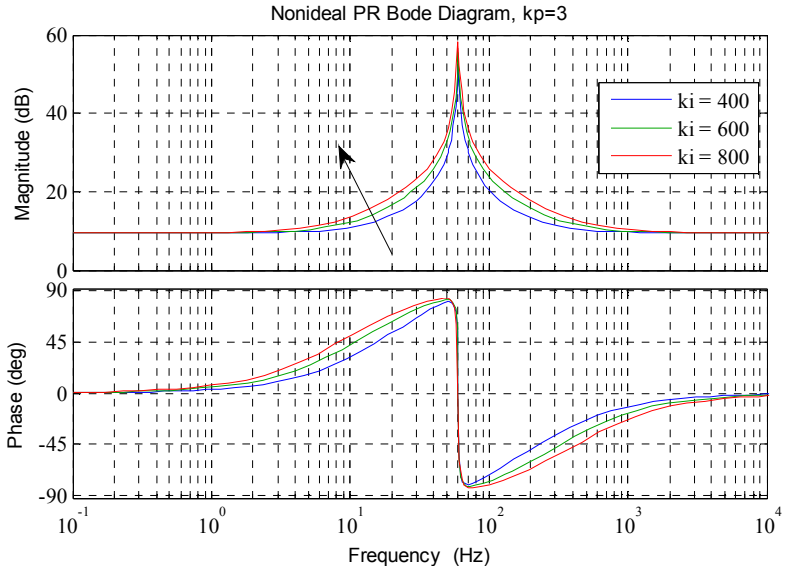

Fig. 2-19: Bode plot of nonideal PR controllers with a fixed proportional gain term

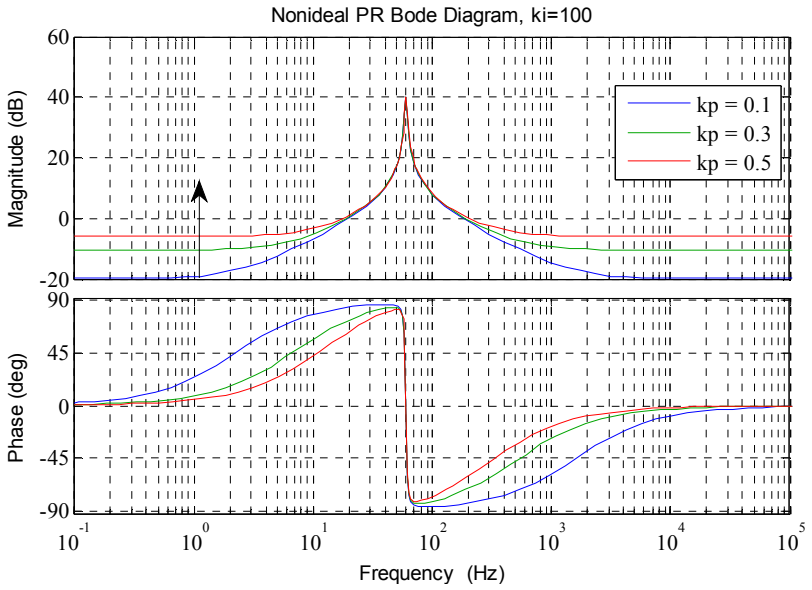

Fig. 2-20: Bode plot of nonideal PR controllers with a fixed integral gain term

To apply a nonideal PR controller to the outer voltage loop. The uncompensated and compensated Bode plots are shown in Fig. 2-21. The blue line is the Bode plot of the uncompensated plant. The green line shows the open-loop Bode plot of the compensated system with nonideal PR control. As we can see from Fig. 2-21, the phase margin is 49.7 degrees and the gain margin is 9.64 dB. The crossover frequency is approximately 1.1 kHz. The nonideal PR controller is given by (2.9). The unit step response is shown in Fig. 2-22. The overshoot is 23.8 %, and the settling time is 1.17 ms. The closed-loop Bode diagram of the nonideal PR based control is shown in Fig. 2-23. The voltage tracking error is given in Fig. 2-24. As we can see in Fig. 2-24, the inverter output voltage achieves zero steady-state tracking error using the nonideal PR control method. The nonideal PR control strategy can obtain the same control performance as the DQ frame control method.

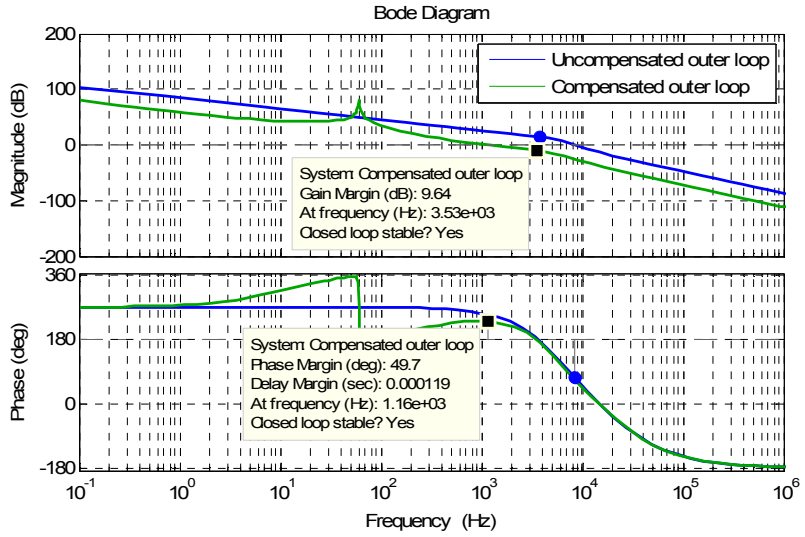

Fig. 2-21: Bode plots of the uncompensated and nonideal PR compensated outer voltage loop

$$G_v = 0.06 + 35\frac{4s}{s^2+4s+(120\pi)^2} \tag{2.9}$$

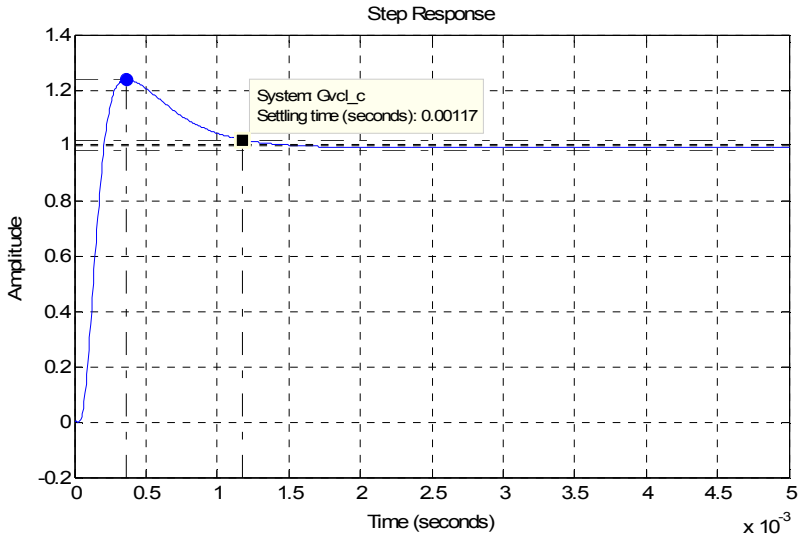

Fig. 2-22: Step response of the compensated outer voltage loop with nonideal PR control

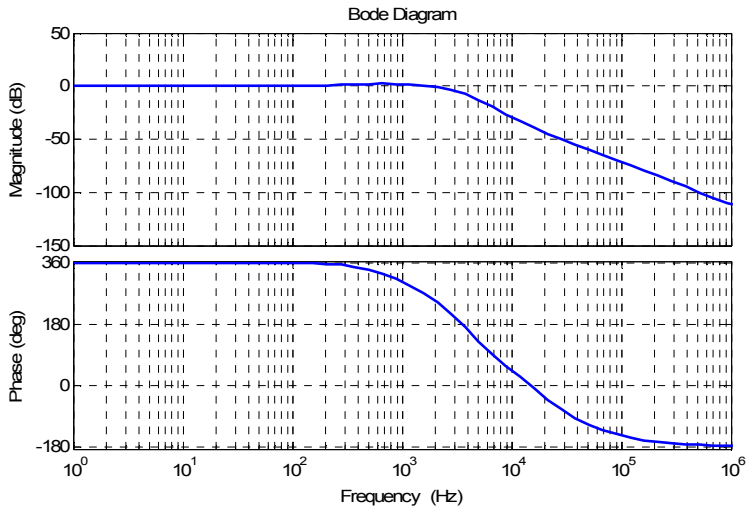

Fig. 2-23: Closed-loop Bode plot of the dual-loop system with nonideal PR control

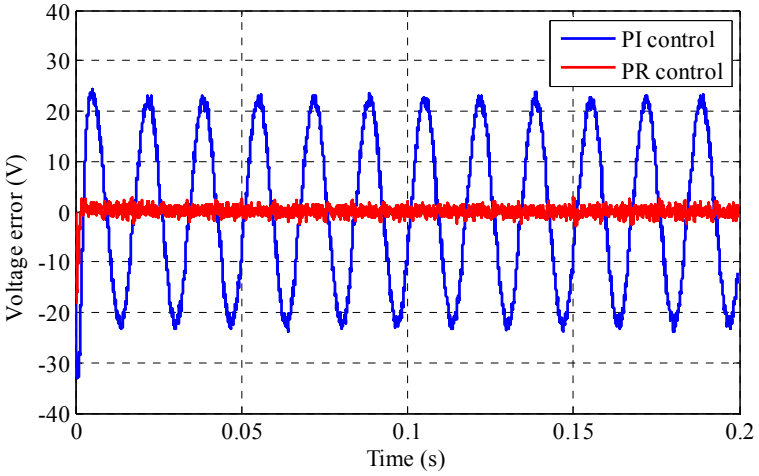

Fig. 2-24: Voltage tracking error comparison between PI control and nonideal PR control

2.5 Summary

In this chapter, the control design of a dual-loop controlled single-phase H-bridge inverter in stand-alone operation mode is discussed. To eliminate the zero steady-state control error, both the synchronous rotating frame with a DQ transformation and stationary reference frame PR controller are investigated. However, the DQ frame control mentioned above is easier for digital implementation, especially when the dual-loop PI controllers have already been designed. Applying the DQ transformation to the outer voltage control loop, a simulation based

comparison on the control performance between the two inner current feedback methods is performed. Using the DQ transformation and capacitor current feedback, the designed controllers can achieve both zero steady-state output voltage tracking error and good step load performance.

Table 2-1: Island mode inverter control comparison

Controller	Zero steady-state error	Load immunity	Implementation
Conventional PI with inverter-side inductor current feedback	√	√	√√√
Conventional PI with capacitor current feedback	√	√√√	√√√
DQ based control with inverter-side inductor current feedback	√√√	√	√√
DQ based control with capacitor current feedback	√√√	√√√	√√
PR based control with inverter-side inductor current feedback	√√√	√	√
PR based control with capacitor current feedback	√√√	√√√	√

Chapter 3 Controller Design of Grid-Tied Inverter

Besides working as stand-alone power supplies, residential inverters are expected to send extra generated power back to the utility. In this chapter, the control design of grid-tied inverters is discussed and performed. In [12, 46-48], the grid-tied inverters are controlled as a voltage source. However, the current output of the voltage controlled grid-tied inverter largely depends on the grid voltage quality. In this thesis, the grid-tied mode inverter is seen as a current source from the grid side, and the inverter output current is directly controlled. The proportional capacitor current feedback method is used to achieve active damping for the inverter with an LCL filter. The outer loop regulates the current flowing into the grid. A feed-forward loop is adopted to reduce the grid fluctuation disturbances. For grid-tied inverters, sensing the grid voltage phase information is necessary. An amplitude detection based method is investigated to provide the in phase with the grid component and in quadrature phase with the grid component. By utilizing amplitude detection method, no phase locked loop controller is needed. A PR controller is adopted for outer control loop regulation to achieve the zero steady-state tracking error in the grid-tied mode, as it is easy to implement active harmonics compensators (HC) in the PR controller for better quality of the inverter output current [5]. The grid-connected mode inverter circuit and control diagram is given in Fig. 3-1.

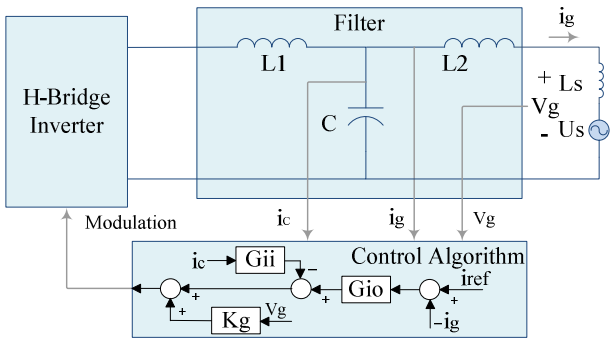

Fig. 3-1: Grid-tied inverter circuit diagram

3.1 Current Controller Design

As mentioned in Chapter 1, the capacitor current feedback loop with a simple proportional controller K_e is added to achieve active damping for the grid-tied inverter with an LCL filter. Neglecting the feed-forward loop, the Laplace frequency domain block diagram of the control method is illustrated in Fig. 3-2. The transfer function of the capacitor current I_C to the inverter output voltage V_i is given in (3.1). The transfer function of the grid current I_g to the inverter output voltage V_i is given in (3.2). The inverter equivalent transfer function with one switching period pure delay [40] is described as (3.3). Ignoring the internal resistance in inductors, the transfer function (3.4) of the grid current I_g to the capacitor current I_C is derived from (3.1) and (3.2) [37]. The outer loop PR controller is shown as (3.5). For simplicity, the harmonic compensators are not considered in the design process. However, they are used in simulation and practical implementation.

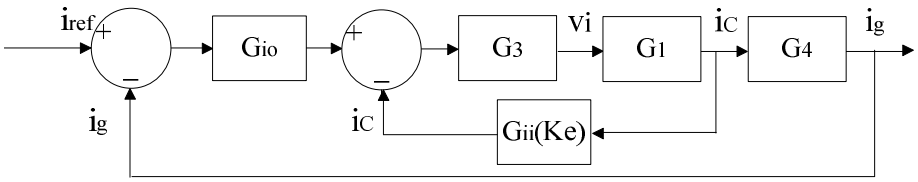

Fig. 3-2: Grid-tied inverter control block diagram

$$G_1 = \frac{I_c(s)}{V_i(s)} = \frac{L_2 Cs}{L_1 L_2 Cs^2 + (L_1 + L_2)} \tag{3.1}$$

$$G_2 = \frac{I_g(s)}{V_i(s)} = \frac{1}{L_1 L_2 Cs^3 + (L_1 + L_2)s} \tag{3.2}$$

$$G_3 = K_{pwm} G_d \tag{3.3}$$

$$G_4 = \frac{I_g(s)}{I_c(s)} = \frac{1}{L_2 Cs^2} \tag{3.4}$$

$$G_{io} = G_{PR}(s) = k_{p1} + 2k_{i1} \frac{\omega_{b1} s}{s^2 + 2\omega_{b1} s + (\omega_0)^2} \tag{3.5}$$

The inner loop controller K_e is related to the LCL filter damping performance. The outer loop PR controller is designed to enlarge the phase margin and gain margin to ensure the stability

of the dual-loop control system. According to the guidance given in [28], the inner loop controller gain K_e is tuned to 0.08 for satisfactory damping. The Bode plot displayed as Fig. 3-3 shows how inner loop controller K_e affects the damping performance. The Bode plots of the compensated and uncompensated actively damped systems are shown in Fig. 3-4. By applying a PR controller, the gain margin is increased to 11 dB and the phase margin of the system reaches 49 degrees. The crossover frequency of the compensated open-loop system is 658 Hz. The number of the compensated open-loop system RHP poles is zero. According to Nyquist stability criterion, the compensated closed-loop system is stable.

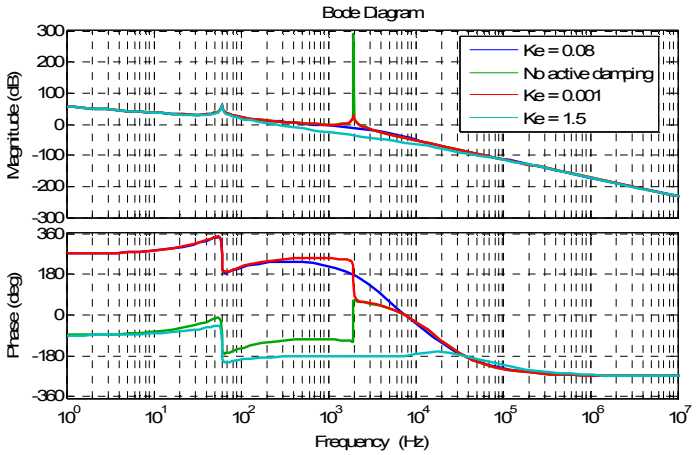

Fig. 3-3: Inner loop controller selection

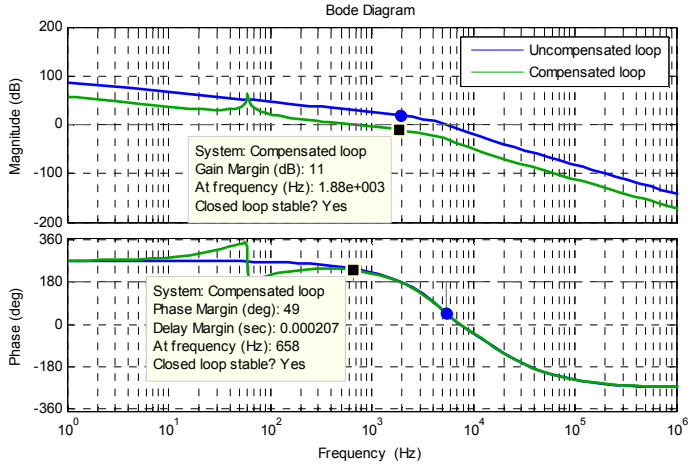

Fig. 3-4: Bode plots of the compensated and uncompensated systems

The Bode diagram Fig. 3-5 shows that as proportional gain K_{p1} decreases, the gain margin increases, however, the crossover frequency and phase margin decreases. The practical system may become unstable. The Bode plot in Fig. 3-6 illustrates that a higher integral gain of PR controller K_{i1} adds more negative phase shift around the resonance frequency, and a much lower K_{i1} degrade the high gain at the resonant frequency, which is set to be the grid frequency 60 Hz. Decreasing the high gain at the grid frequency results in a larger steady-state sinusoidal tracking error. The designed controller is given as (3.6). With the designed controllers, when the grid side inductance L_2 changes within 50 %, which mimics the changes of the grid impedance, the system is still robust as shown in Fig. 3-7.

$$G_{io} = G_{PR}(s) = 0.032 + 6.4\frac{2s}{s^2+4s+\omega_0^2} \tag{3.6}$$

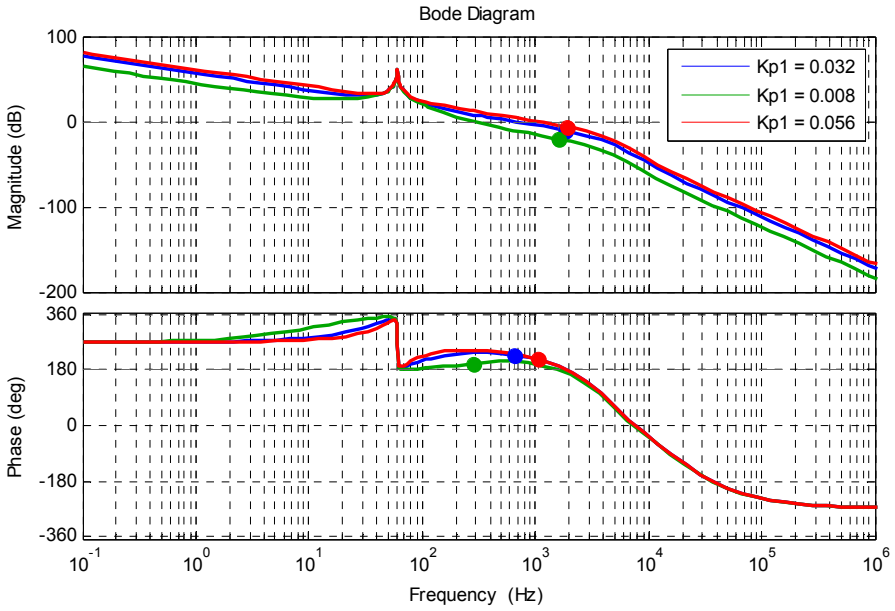

Fig. 3-5: Bode plots of the compensated systems with various K_{p1}

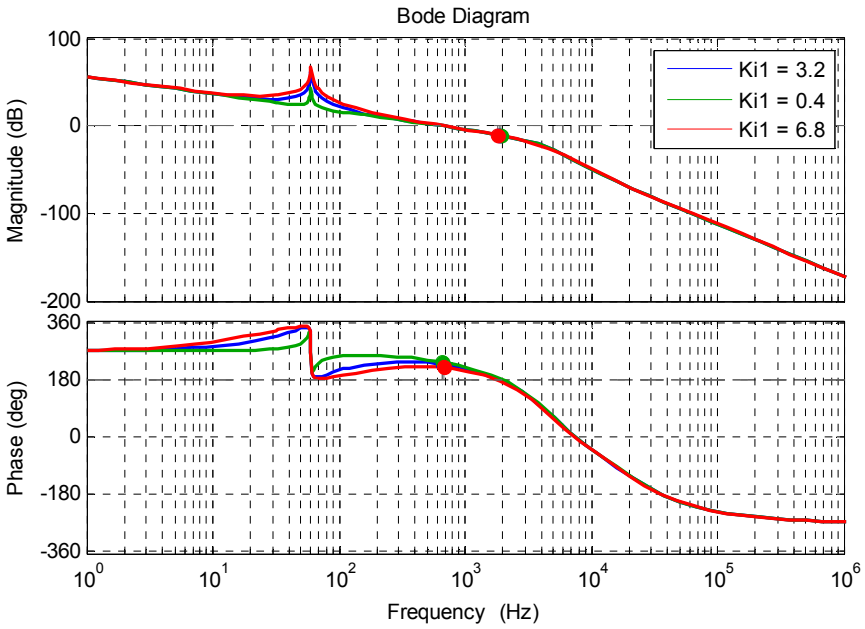

Fig. 3-6: Bode plots of the compensated systems with various K_{i1}

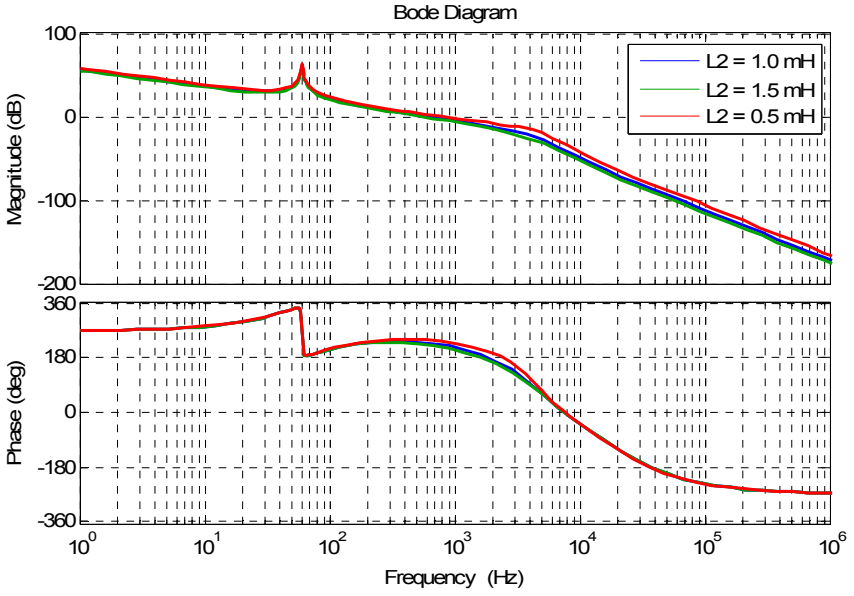

Fig. 3-7: Bode plots of the compensated systems with various L_2

With the designed controller, the system step response is given as in Fig. 3-8. The settling time of the system response is 7.8 ms and the overshoot is 24 %. Fig. 3-9 shows the designed control system tracks a 60 Hz sinusoidal signal with zero steady-state error. The blue line in Fig. 3-9 is the sinusoidal control reference.

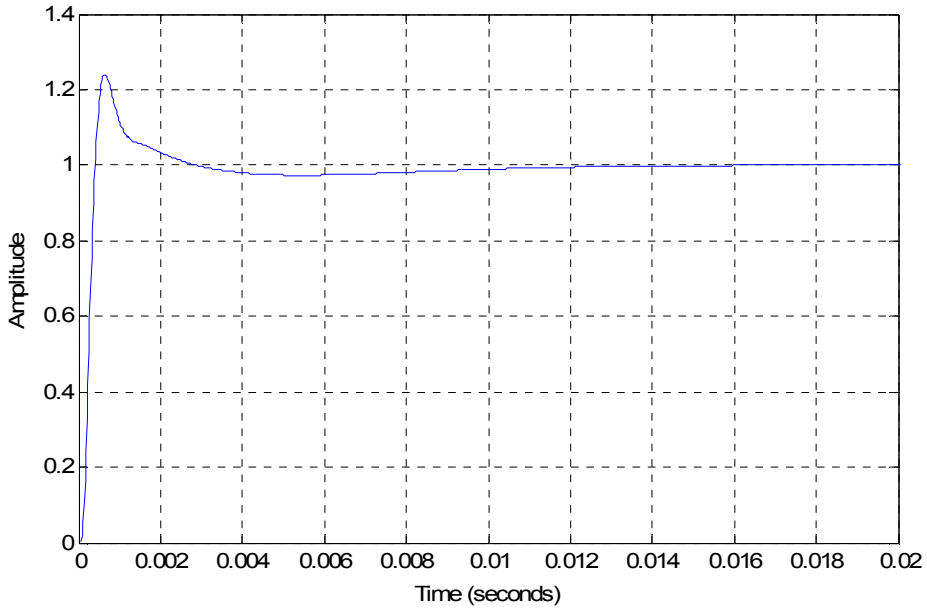

Fig. 3-8: Step response of the dual-loop control system

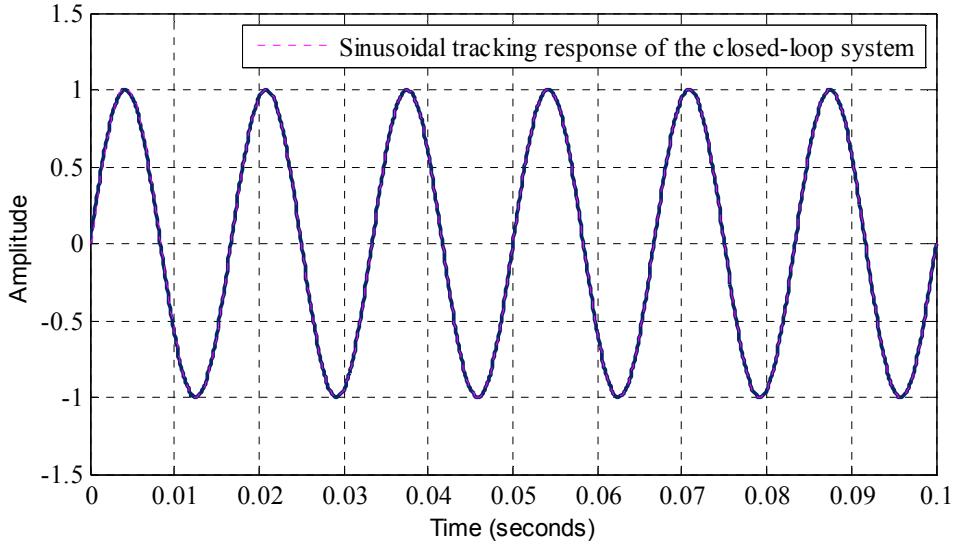

Fig. 3-9: Sinusoidal signal tracking response of the designed system

3.2 Phase Locked Loop and Amplitude Detection

In the grid-connected mode, it is essential to have a phase locked loop (PLL) module for inverters. The PLL component takes measured grid AC voltage as a reference to generate an estimated grid frequency $\widehat{\omega_g}$, and an estimated phase angle $\hat{\theta}$, in order to control the phase of the inverter output signal. Thus, a PLL is a closed-loop servo system to minimize the output phase

and the reference phase error [49]. The PLL module performance affects the grid-connected inverter operation directly.

Zero-crossing detection is a conventional phase tracking method. A zero-crossing based PLL structure is given in Fig. 3-10. When the reference signal v_g passes zero towards to positive value, θ is reset to 0. When the reference signal falls past zero, θ is reset to π. This type of PLL module only detects reset points at half of the grid frequency. It is unable to provide good dynamic performance. Moreover, the zero-crossing based PLL performance is susceptible to grid harmonics and distortions. Thus, this kind of PLL is unfit for inverter grid-tied applications.

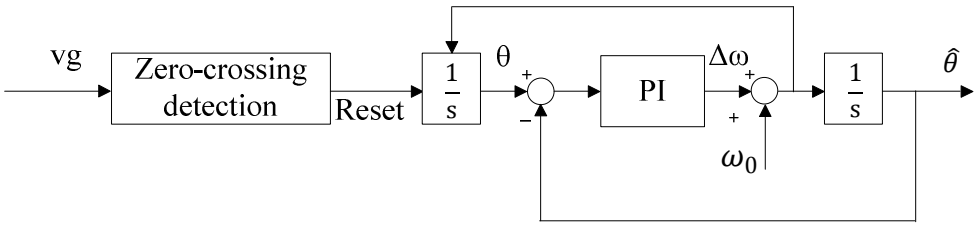

Fig. 3-10: Zero-crossing detection based PLL

Another PLL structure [50], which is commonly used for inverter grid-connected applications, is shown in Fig. 3-11. The structure contains a phase detection (PD) unit, a low bandwidth PI based loop filter (LF), and a voltage controlled oscillator (VCO). The PD unit is used to detect the phase difference between the input signal and the reproduced output signal.

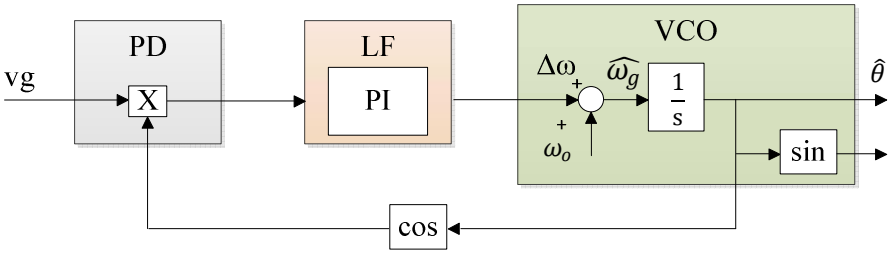

Fig. 3-11: Basic phase error detection based PLL

Let the input grid measurement be

$$v_g(t) = \sqrt{2}V_{g\_rms}\sin(\theta_g) = \sqrt{2}V_{g\_rms}\sin(\omega_g t + \varphi_g) \quad (3.7)$$

The output signal of the PD unit is

$$v_{PD}(t) = \sqrt{2}V_{g\_rms}\sin(\theta_g)\cos(\hat{\theta}) \quad (3.8)$$

To further expand (3.8), the $v_{\mathrm{PD}}(t)$ can be expressed as,

$$v_{PD}(t) = \frac{\sqrt{2}}{2}V_{g\_rms}\sin[(\omega_g - \widehat{\omega_{\mathrm{g}}})t + (\varphi_g - \hat{\varphi})] + \frac{\sqrt{2}}{2}V_{g_{rms}}\sin[(\widehat{\omega_{\mathrm{g}}} + \omega_g)t + (\hat{\varphi} + \varphi_g)] \quad (3.9)$$

The PD unit output signal is divided into a low frequency component and a high frequency component as shown in (3.9). When the PD unit output signal passes through LF unit, the high frequency component is filtered out. Then, the LF unit output is,

$$v_{LP}(t) = \frac{\sqrt{2}}{2}V_{g\_rms}\sin[(\omega_g - \widehat{\omega_{\mathrm{g}}})t + (\varphi_g - \hat{\varphi})] \quad (3.10)$$

Through the PI controller, the estimated frequency can be obtained. In the steady state, $v_{\mathrm{LP}}(\mathrm{t})$ approaches to zero, as $\widehat{\omega_{\mathrm{g}}} = \omega_{\mathrm{g}}$ and $\hat{\varphi} = \varphi_{\mathrm{g}}$. The phase of the output signal is locked with the input grid measurement.

The PLL structure mentioned above has a LPF component in loop filter unit to filter out double line frequency. An alternative way to realize PLL is to use a rotating reference frame PLL. The PLL block diagram [12, 49] is shown below in Fig. 3-12. It consists of an orthogonal signal generator (OSG), Park's transform, a low bandwidth PI, and a VCO unit.

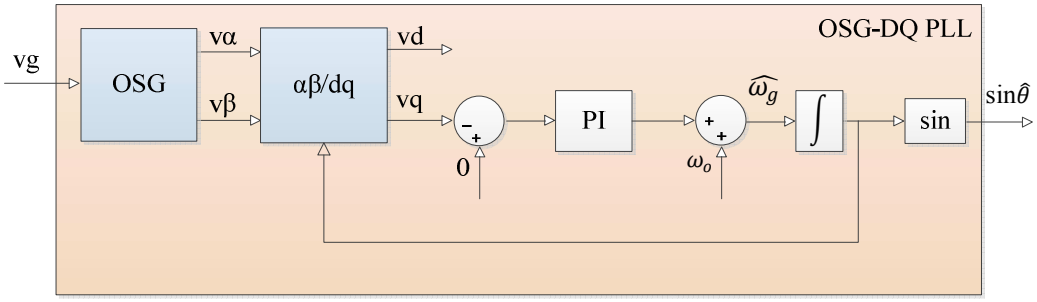

Fig. 3-12: OSG based single-phase PLL

The second order generalized integrator (SOGI) based OSG block, which is capable of filtering out grid harmonics, contains a second order band pass filter (BPF) and a second order low pass filter. The state-space form of the SOGI module is given in (3.11) and (3.12).

$$\begin{bmatrix} \dot{x_1} \\ \dot{x_2} \end{bmatrix} = \begin{bmatrix} -K_{p2}\omega_g & -\omega_g \\ \omega_g & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} K_{p2}\omega_g \\ 0 \end{bmatrix} \begin{bmatrix} v_g \end{bmatrix} \tag{3.11}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{3.12}$$

$H_{\mathrm{d}}(\mathrm{s})$ is defined as $\frac{V_\alpha(\mathrm{s})}{V_{\mathrm{g}}(\mathrm{s})}$, and $H_{\mathrm{q}}(\mathrm{s})$ is defined as $\frac{V_\beta(\mathrm{s})}{V_{\mathrm{g}}(\mathrm{s})}$. The Bode plots of $H_{\mathrm{d}}(\mathrm{s})$ and $H_{\mathrm{q}}(\mathrm{s})$ with variations of K_{p2} are shown in Fig. 3-13 and Fig. 3-14, respectively.

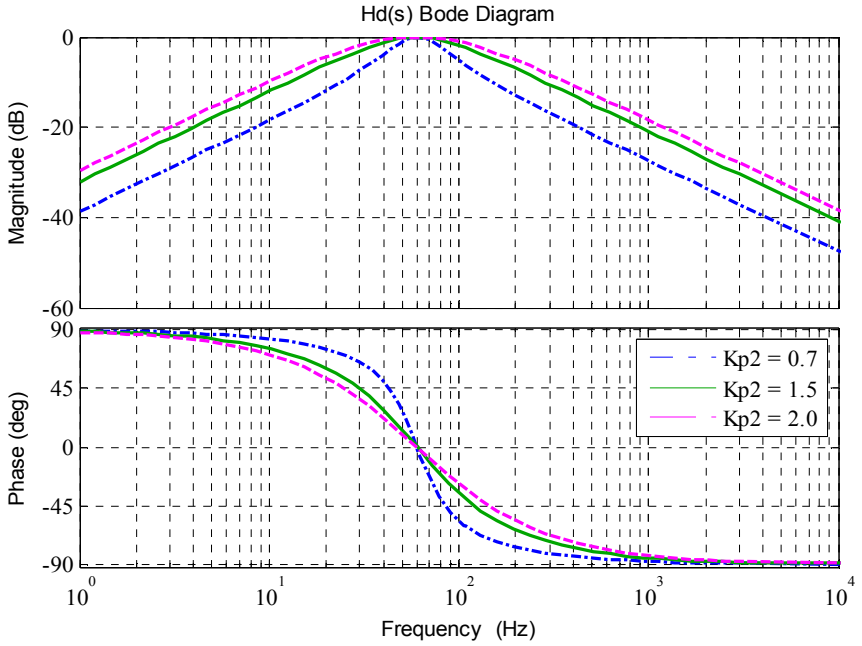

Fig. 3-13: Bode plot of $H_{\mathrm{d}}(\mathrm{s})$

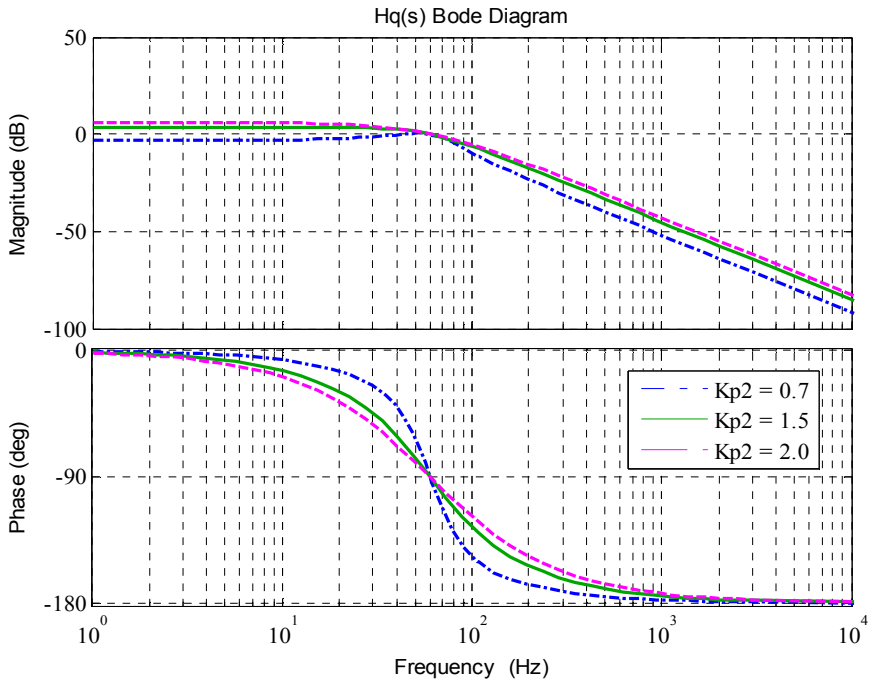

Fig. 3-14: Bode plot of $H_{\mathrm{q}}(\mathrm{s})$

Both Fig. 3-13 and Fig. 3-14 show that the parameter K_{p2} decides the OSG frequency selectiveness and bandwidth. A smaller K_{p2} in the second order generalized integrator helps to increase immunity to harmonics, but it can degrade the response of the SOGI [49]. Considering the trade-off, K_{p2} is chosen to be 1.5 for simulations. Comparing Fig. 3-13 to Fig. 3-14, $H_{\mathrm{d}}(\mathrm{s})$ rejects the DC offset component in the sensed grid voltage, while $H_{\mathrm{q}}(\mathrm{s})$ does not. Numerous research projects [51, 52] have been done to enable $H_{\mathrm{q}}(\mathrm{s})$ to reject the DC component in the sensed grid voltage. In this design, a second order LPF is added into the SOGI based OSG loop [51]. The original OSG structure [12] shown in Fig. 3-15 is then changed to the structure as in Fig. 3-16.

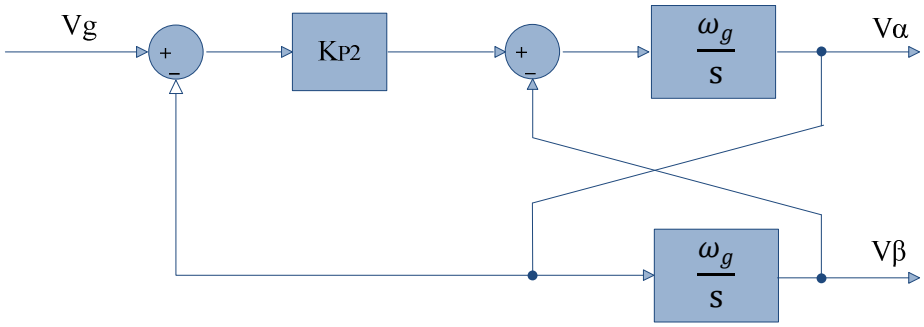

Fig. 3-15: Second order generalized integrator for the OSG unit [12]

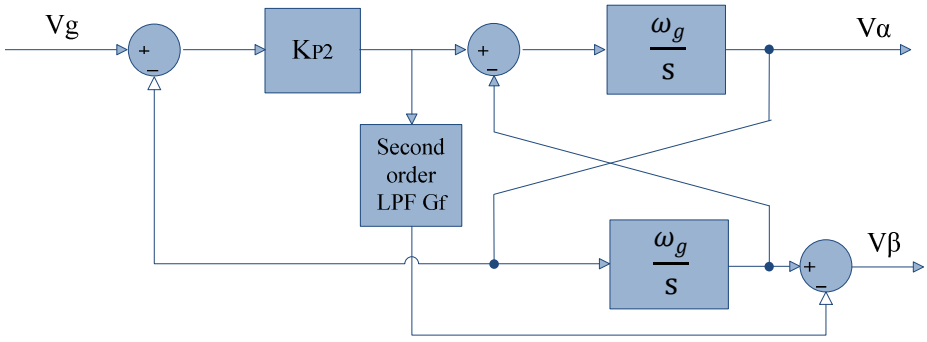

Fig. 3-16: Revised SOGI for the OSG unit

A second order LPF filter is described as

$$G_f = \frac{1}{(s/\omega_f)^2+(s/Q\omega_f)+1} \tag{3.13}$$

The cut-off frequency is chosen to be $\omega_{\mathrm{f}} = 2\pi f_{\mathrm{f}} = 376.8$ rad/s, and the quality factor Q is set to be 0.71. The Laplace transfer function of the revised $H_{\mathrm{q}}(\mathrm{s})$ is given as (3.14). The revised Bode plot of $H_{\mathrm{q}}(\mathrm{s})$ is illustrated in Fig. 3-17. By adding a second order LPF, $H_{\mathrm{q}}(\mathrm{s})$ is capable of rejecting the grid DC offset. Adding the second order LPF in the SOGI also increases the ability of harmonic rejection. However, as the bandwidth becomes narrower, the response of the SOGI becomes slower. It is a trade-off between frequency selectiveness and response speed.

$$H_q'(s) = H_q(s) - G_f K_{p2}(s^2 + {\omega_g}^2)/(s^2 + K_{p2}\omega_g s + {\omega_g}^2) \tag{3.14}$$

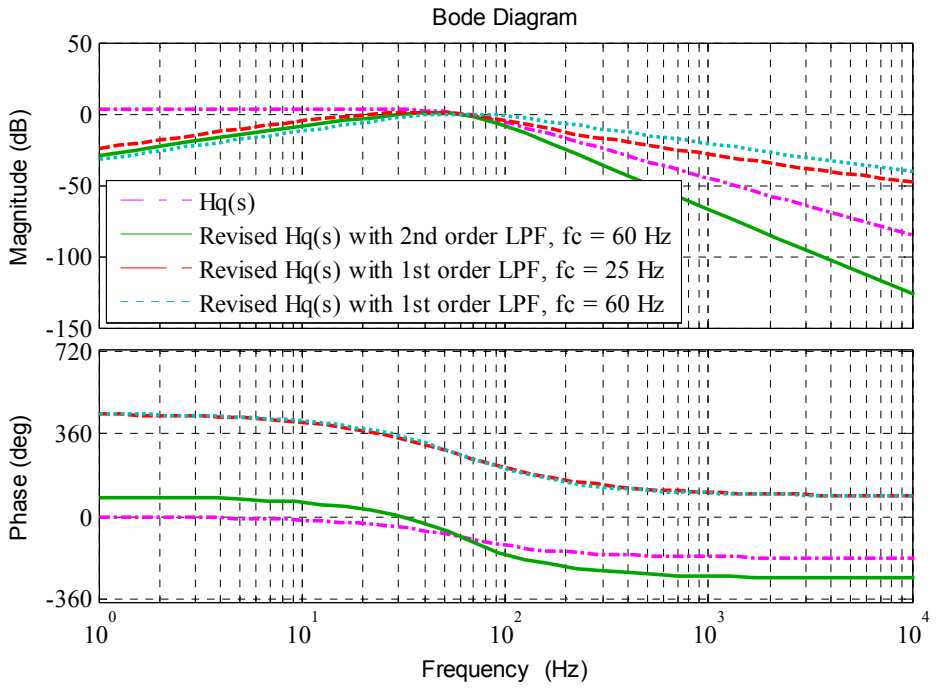

Fig. 3-17: Bode plot of $H_q'(s)$

The grid amplitude can also be obtained through the SOGI-OSG module. The calculated grid peak voltage is shown as (3.15).

$$|V_g| = (v_\alpha{}^2 + v_\beta{}^2)^{0.5} \tag{3.15}$$

Based on this grid peak voltage detection method [7, 53], the in phase with the grid and in quadrature phase with the grid components can be achieved without the additional phase locked loop. This method uses a constant ω_g in (3.11), which is set to be grid angular frequency. Considering the grid frequency changes slightly from 59.4 Hz to 60.6 Hz, according to IEEE-1547 [54]. The error resulting from the grid peak detection method is negligible. The peak amplitude detection based grid synchronization illustration diagram is shown in Fig. 3-18.

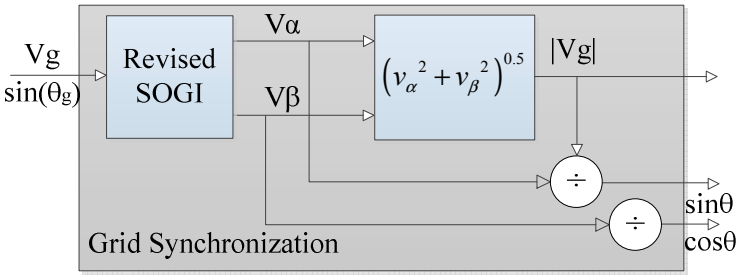

Fig. 3-18: Peak detection based grid synchronization

The performance of the revised SOGI-OSG can be evaluated through various grid fault conditions. Fig. 3-19 shows the performance of the revised SOGI on grid peak voltage detection and quadrature signals generation when there is a frequency drift from 60 Hz to 60.6 Hz at 0.05 s. The grid frequency recovers to nominal at 0.1 s. In Fig. 3-19, the black line represents the grid voltage. The pink and blue lines represent the generated orthogonal signals. The red line shows the calculated grid peak voltage. The settling time for peak detection is within two grid cycles. It can be noticed that there is a double line frequency component in the detected peak voltage during the grid frequency deviation. It is caused by setting ω_g as the nominal grid angular frequency in the revised SOGI module. The steady-state maximum voltage of the ripple is 341.5 V and the minimum voltage is 335 V.

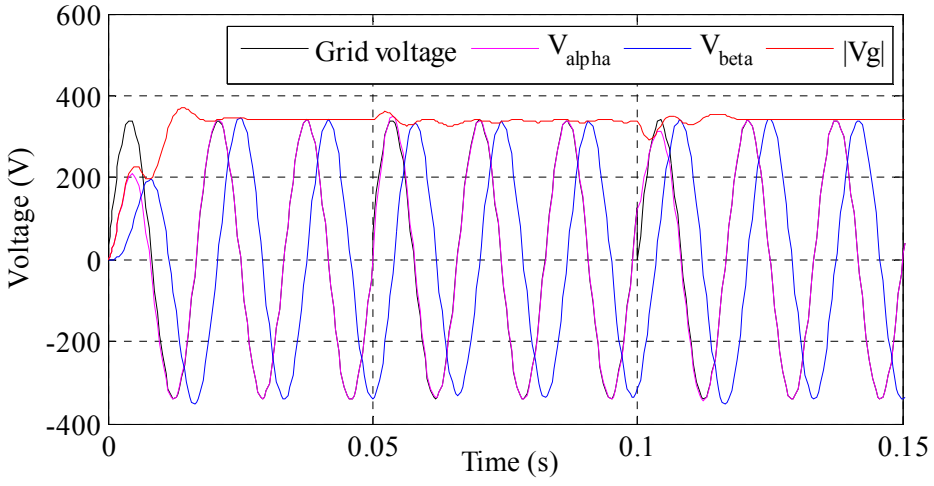

Fig. 3-19: Revised SOGI performance under frequency drift

Fig. 3-20 shows the performance of the revised SOGI on grid peak voltage detection and quadrature signals generation when the grid voltage drops to 90 % of nominal voltage at 0.05 s. The grid voltage comes back to nominal at 0.1 s. The settling time for peak detection is also within two grid cycles.

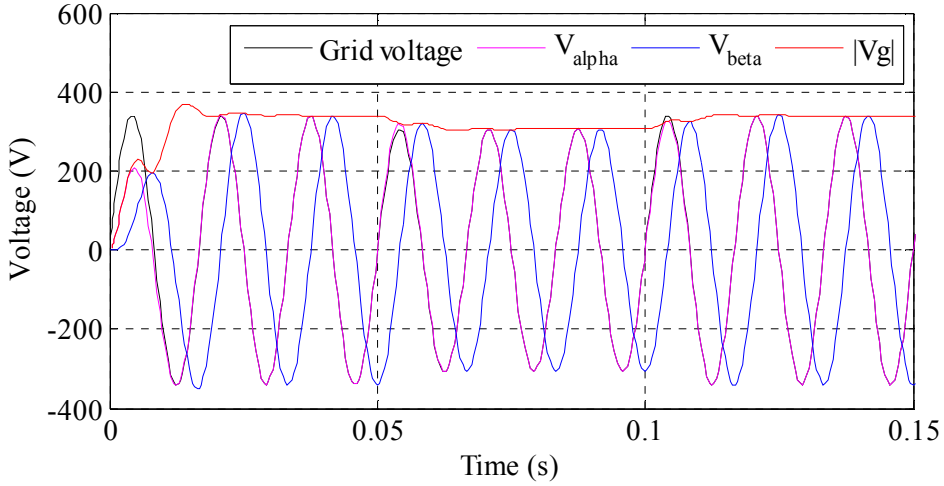

Fig. 3-20: Revised SOGI performance under voltage sag

Fig. 3-21 shows the performance of the revised SOGI on peak voltage detection and quadrature signals generation when the grid voltage is polluted with harmonics and DC offset. The grid voltage used for this simulation is given by (3.16). In Fig. 3-21, the black line shows the polluted grid voltage. The pink and blue lines are the generated orthogonal signals. The red line gives the calculated grid peak voltage. The settling time for peak detection is within two grid cycles. In steady-state, the maximum voltage of the ripple is 347.7 V and the minimum voltage of the ripple is 335.7 V. The calculated voltage deviated from the nominal grid peak voltage is within 3 %.

$$v_g = 340(0.1 + \sin(2\pi\omega_g t) + 0.05\sin(2\pi \times 3\omega_g t) + 0.05\sin(2\pi \times 5\omega_g t) + 0.03\sin(2\pi \times 7\omega_g t) + 0.01\sin(2\pi \times 9\omega_g t) + 0.01\sin(2\pi \times 23\omega_g t) \quad (3.16)$$

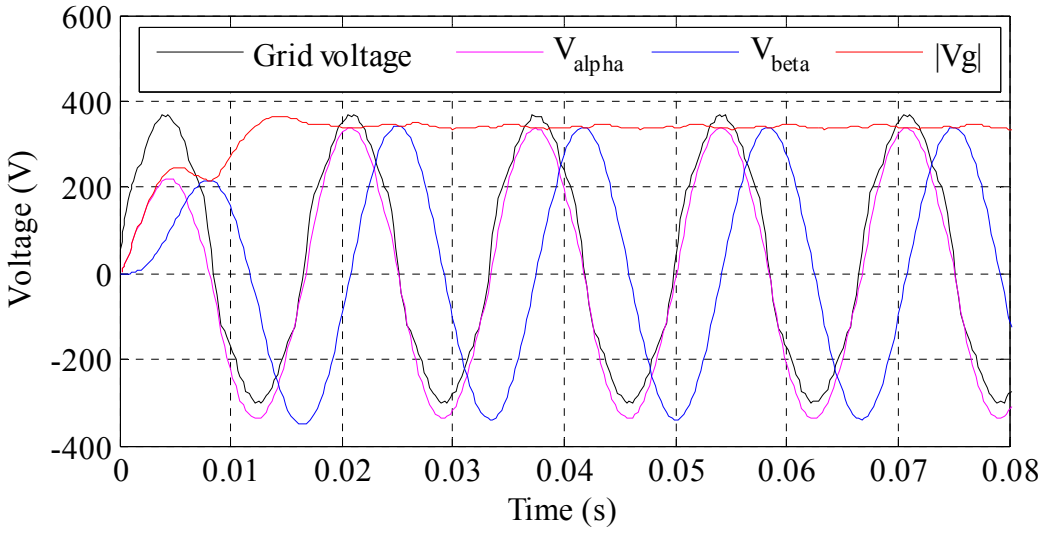

Fig. 3-21: Revised SOGI performance under harmonics and DC offset polluted grid

3.3 Active and Reactive Power Flow Control

It is known that the inverter active power output is proportional to the current in phase with the grid voltage, and the reactive power output is proportional to the current in quadrature phase with the line voltage [45, 55]. Thus, the current reference i^*, as shown in (3.17), can be divided into two components: active power current reference (i_{P}^*) and reactive power current reference (i_{Q}^*). According to (3.18) and (3.19), (3.17) can be further expanded to (3.20). Meanwhile, I_{P}^* and I_{Q}^* are the peak values of the current references and θ is estimated phase angle of the grid voltage. With given specific active power and reactive power commands, the current reference, which is used to control the single-phase inverter output current, can be obtained as (3.21).

$$i^* = i_P^* + i_Q^* \tag{3.17}$$

$$i_P^* = I_P^* \sin(\theta) \tag{3.18}$$

$$i_Q^* = I_Q^* \cos(\theta) \tag{3.19}$$

$$i^* = I_P^* \sin(\theta) + I_Q^* \cos(\theta) \tag{3.20}$$

$$i^* = \sqrt{2}\left(\frac{P^* \sin(\theta)}{V_g} + \frac{Q^* \cos(\theta)}{V_g}\right) \tag{3.21}$$

According to (3.21), a robust active power controller PI3 and reactive power controller PI4 can be designed through the control block expressed in Fig. 3-22 and Fig. 3-23, respectively.

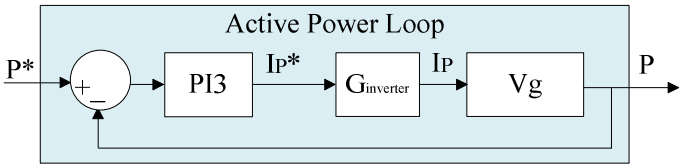

Fig. 3-22: PI based active power control loop

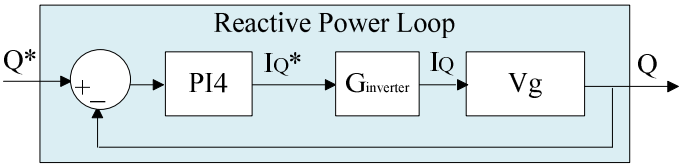

Fig. 3-23: PI based reactive power control loop

Instantaneous power estimation for active power and reactive power in stationary frame can be obtained from (3.22) and (3.23) [45]. According to (3.20)-(3.23), a robust active and reactive power controller can be expressed in Fig. 3-24.

$$P = \frac{(v_{g\alpha} i_{g\beta} + v_{g\beta} i_{g\alpha})}{2} \tag{3.22}$$

$$Q = \frac{(v_{g\beta} i_{g\alpha} - v_{g\alpha} i_{g\beta})}{2} \tag{3.23}$$

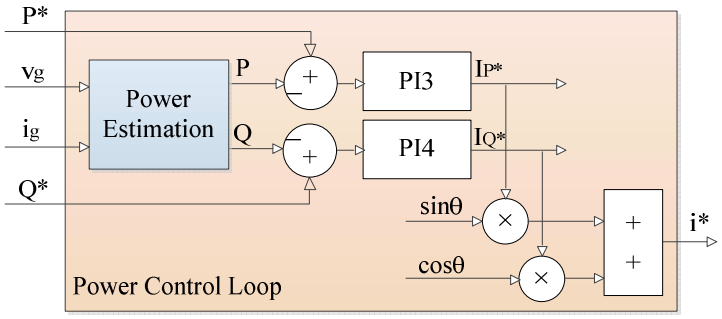

Fig. 3-24: Active and reactive power controller

There are three goals for designing the P controller and Q controller. The PQ control loop system should be under damped with no overshoot. The active and reactive power adjustments should be able to reach steady-state within three grid cycles. There should be zero steady-state

error for power commands tracking during the nominal grid condition. The designed P controller and Q controller are given as (3.24) and (3.25), respectively.

$$G_{PI3} = \frac{0.00019s+0.352}{s} \tag{3.24}$$

$$G_{PI4} = \frac{0.00019s+0.352}{s} \tag{3.25}$$

3.4 Simulation Results

The grid-tied H-bridge inverter with designed controllers is simulated in Matlab™ Simulink. The inverter is controlled by dual current control loop. The outer loop PR controller is added with third, fifth, and seventh order harmonic compensation as shown in (3.26). The output current of the inverter flowing into the grid is directly controlled by the reference generated from the PQ controller to satisfy the expected output active and reactive power. The inverter output current waveform is displayed in Fig. 3-25, when the inverter outputs 2000 W active power. The THD of the inverter output current is 1.08 %. The steady-state tracking error between the current reference signal and inverter current output is shown in Fig. 3-26. The result is also compared to a simulation of the inverter with a PI based outer loop controller. The steady-state error is largely reduced by using the designed PR controller. The inverter output active and reactive power estimated by (3.22) and (3.23) are shown in Fig. 3-27 and Fig. 3-28, respectively. The settling time for both active power and reactive power control is within 0.05 s.

$$G_{io} = G_{PR}(s) = k_{p1} + 2k_{i1}\sum_{h=1,3,5,7}\frac{\omega_{b1}s}{s^2+2\omega_{b1}s+(h\omega_0)^2} \tag{3.26}$$

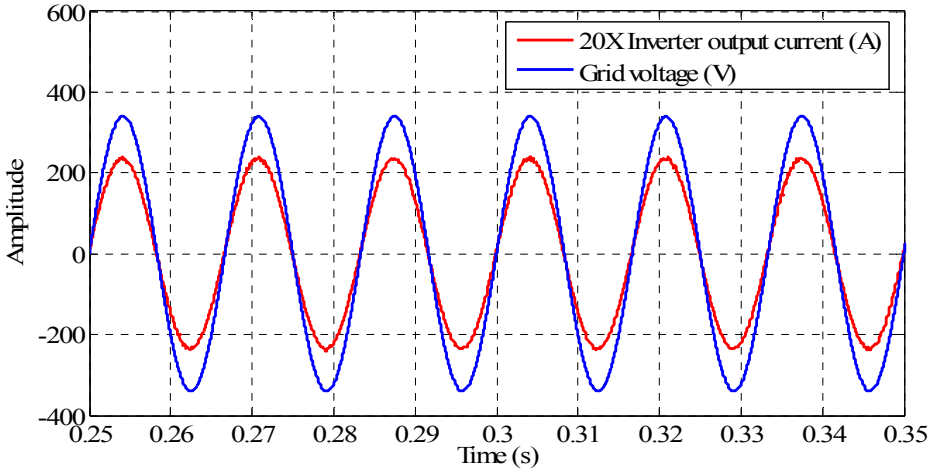

Fig. 3-25: Inverter output current

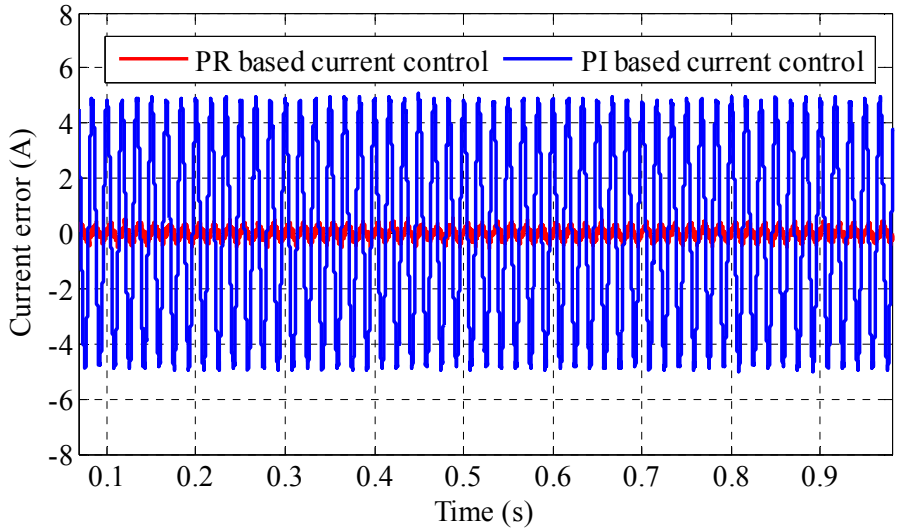

Fig. 3-26: Steady-state tracking error of the inverter current controller

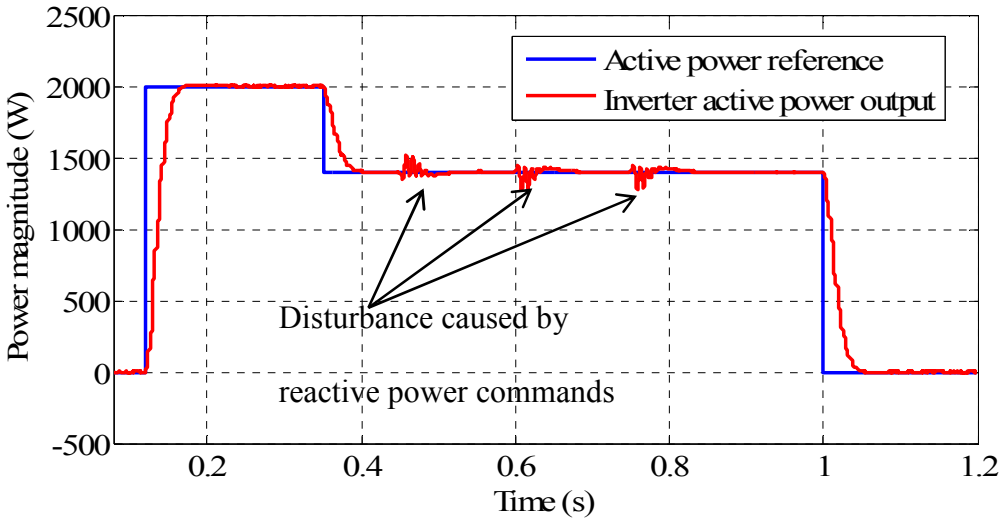

Fig. 3-27: Active power flow control performance

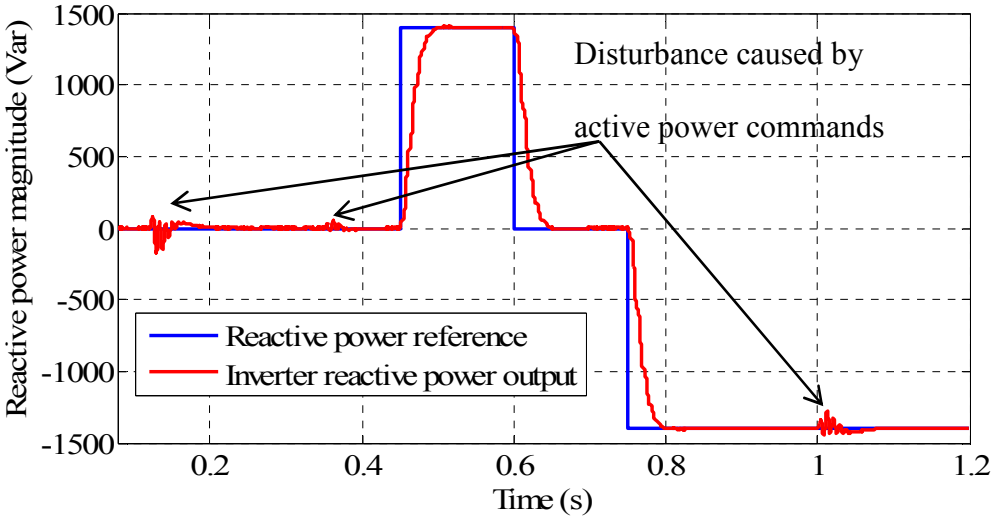

Fig. 3-28: Reactive power flow control performance

The grid may operate in numerous fault conditions. The grid frequency may drift slightly between 59.4 Hz and 60.6 Hz [54]. The magnitude of the grid voltage can either drop to 90 %, or swell to 110 % [54]. There may contain up to 0.1 % DC offset in the grid voltage [56]. The grid can also contain higher order harmonics. The following simulations are completed during grid distortion conditions.

The simulation results displayed in Fig. 3-29 and Fig. 3-30 show that the inverter operates during frequency changes. The grid voltage and inverter output current are given in Fig. 3-29. The active power and reactive power are depicted in Fig. 3-30. At 0.1 s, the grid frequency steps up to 60.6 Hz from 60 Hz. The grid frequency steps down to 60.3 Hz at 0.22 s. The THD of the inverter output current is 1.87 % during 60.6 Hz frequency. The THD of the inverter output current is 1.40 % during 60.3 Hz frequency.

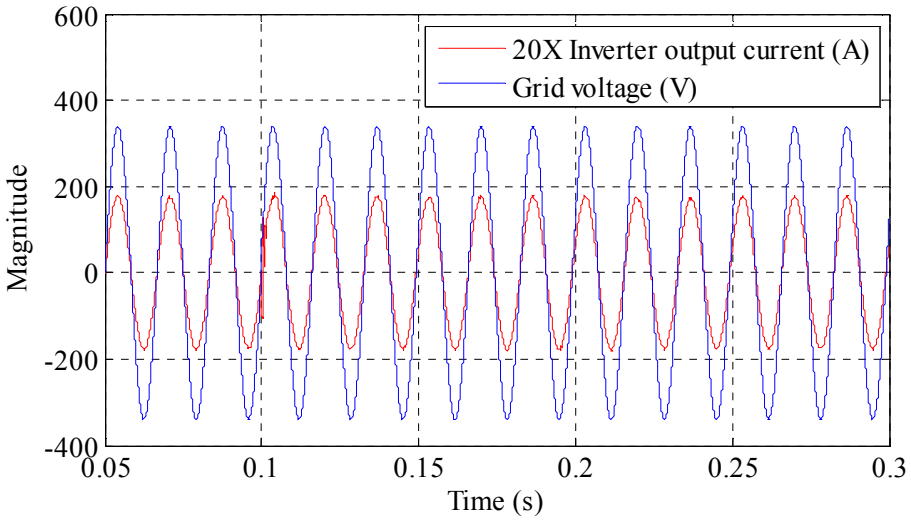

Fig. 3-29: Grid voltage and inverter output current during frequency changes

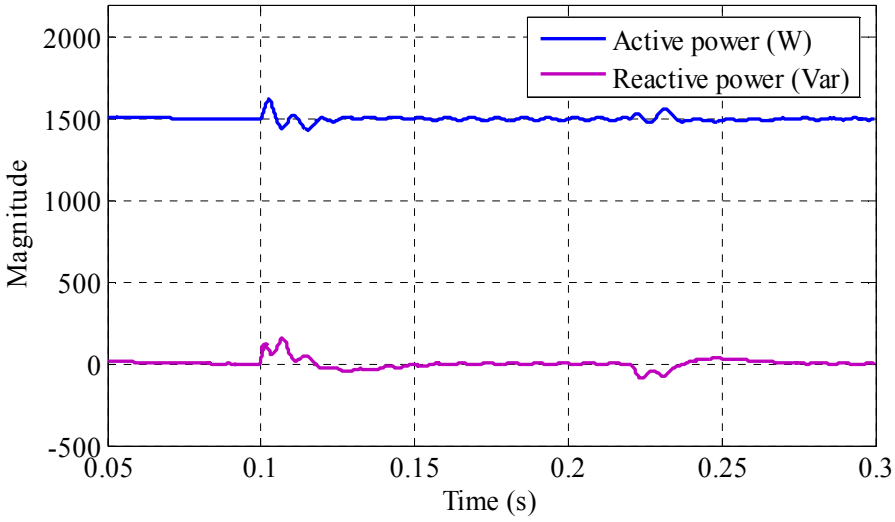

Fig. 3-30: Calculated active and reactive power during frequency changes

The simulation results displayed in Fig. 3-31 and Fig. 3-32 show that the inverter operates during 10 % voltage sag. The grid voltage and inverter output current are given in Fig. 3-31. The instantaneous active power and reactive power are depicted in Fig. 3-32. At 0.1 s, the grid magnitude drops to 90 % of nominal voltage, and it recovers back to 240 V at 0.22 s. The THD of the inverter output current is 0.99 % during the voltage sag.

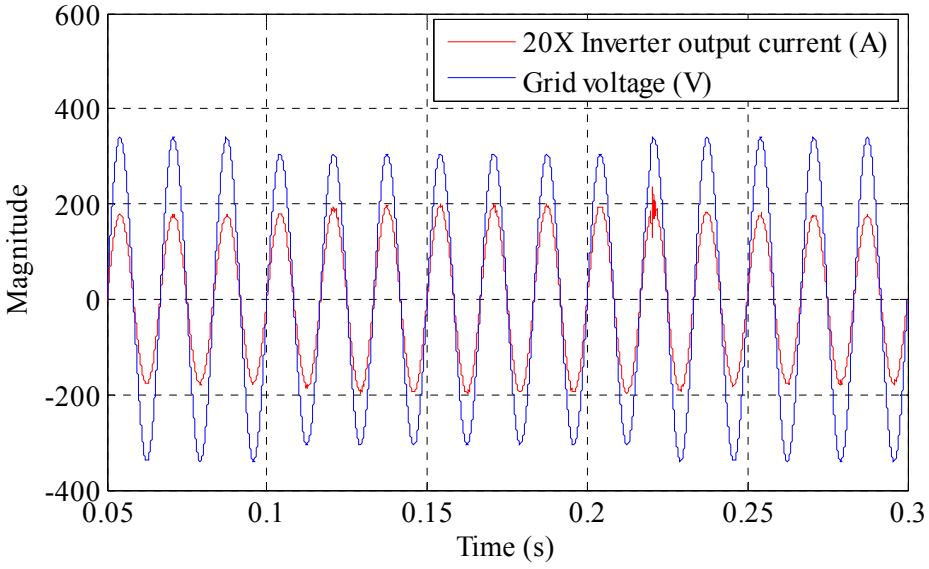

Fig. 3-31: Grid voltage and inverter output current during voltage sag

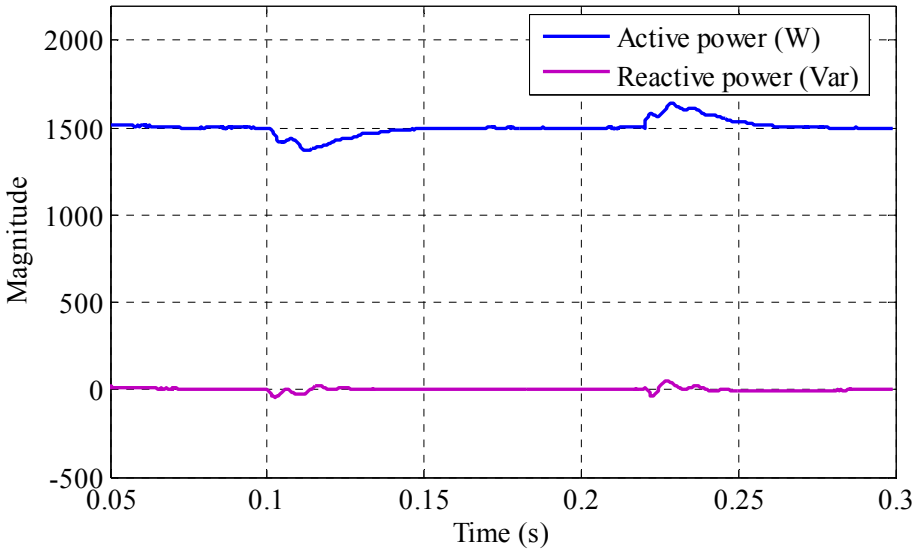

Fig. 3-32: Calculated active and reactive power during voltage sag

The grid can be polluted by up to 0.1 % DC offset [56]. However, voltage sensing circuits can also introduce DC offset to a certain level to introduce substantial DC components in the inverter output current. The grid voltage and inverter output current are shown in Fig. 3-33. The instantaneous active power and reactive power are given in Fig. 3-34. The grid voltage is polluted by 5 % of the nominal grid voltage DC component at 0.1 s, and it recovers back to nominal grid voltage at 0.22 s. The THD of the inverter output current is 1.21 % during the period where the grid is injected by DC components.

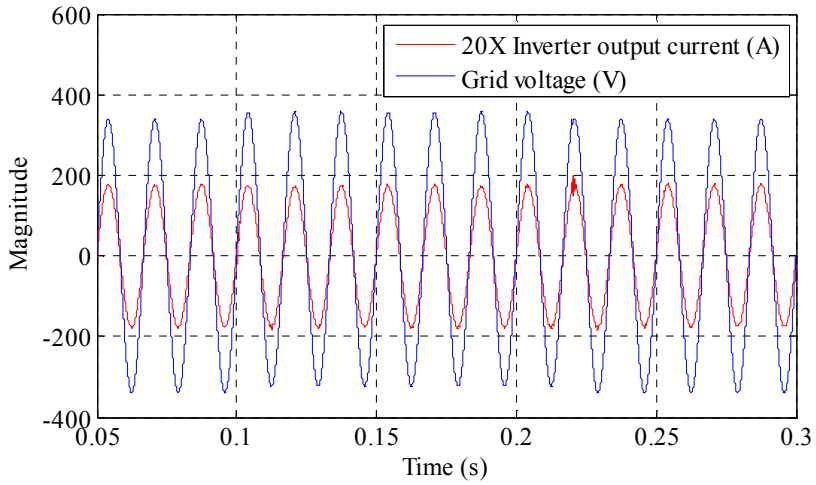

Fig. 3-33: Grid voltage and inverter output current under DC influence

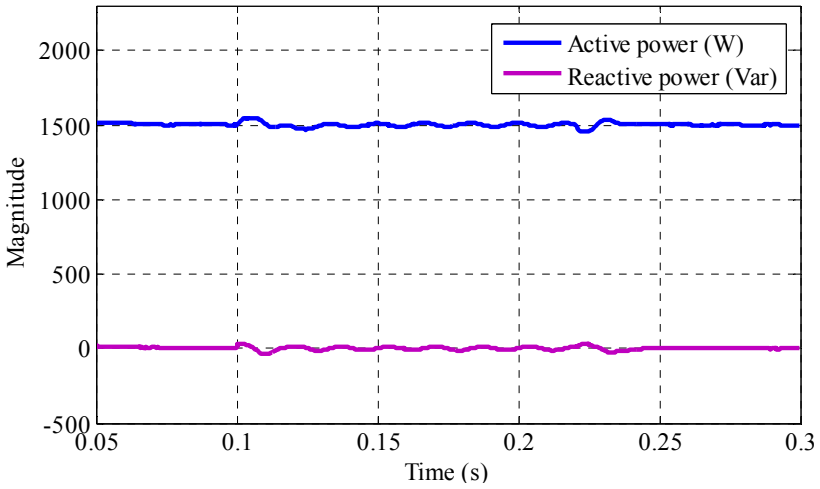

Fig. 3-34: Calculated active and reactive power under DC influence

The simulation results displayed in Fig. 3-35 and Fig. 3-36 show that the inverter operates during the grid polluted by 3 % third order, 2 % fifth order, and 1 % seventh order harmonics. Grid voltage and inverter output current are given in Fig. 3-35. The instantaneous active power and reactive power are displayed in Fig. 3-36. The harmonics injected grid condition starts at 0.1 s and ends at 0.22 s. The THD of the inverter output current is 1.87 %.

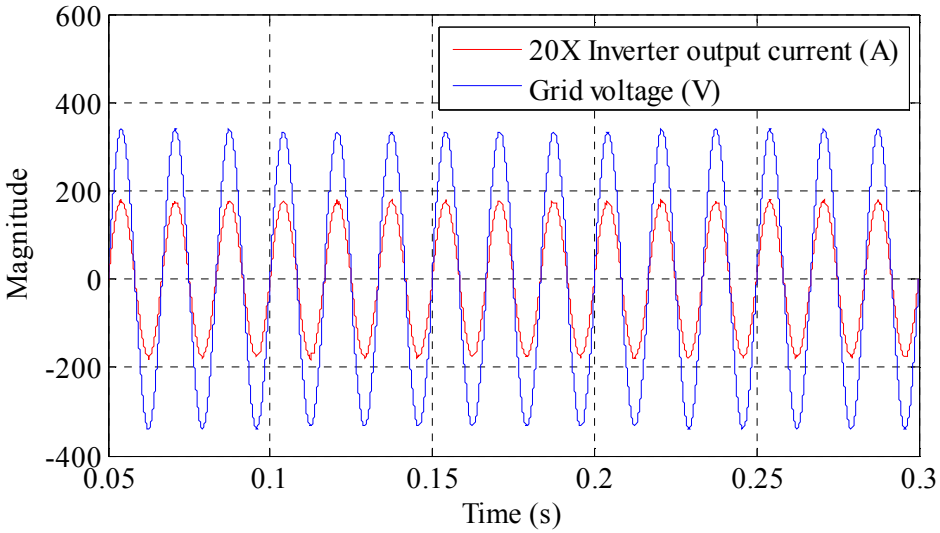

Fig. 3-35: Grid voltage and inverter output current under grid distortion

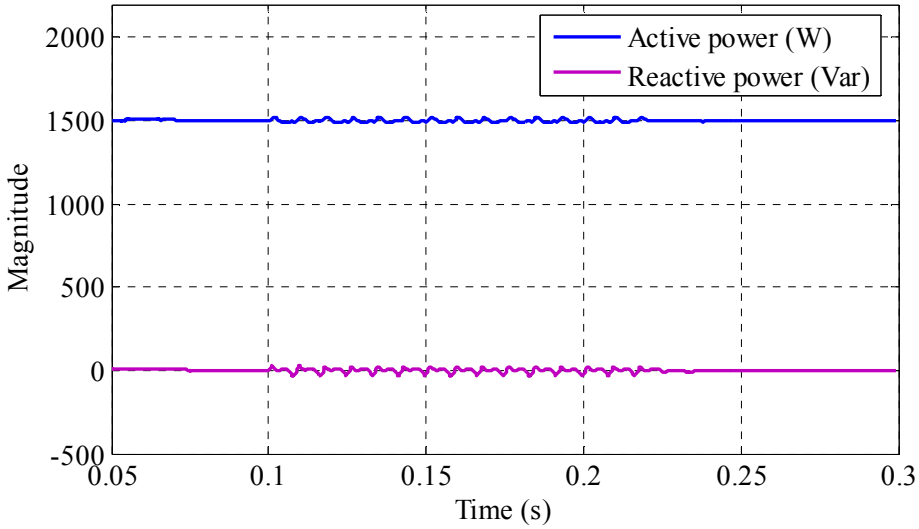

Fig. 3-36: Calculated active and reactive power under grid distortion

3.5 Summary

In this chapter, the control design of a grid-connected single-phase H-bridge inverter has been discussed. The grid synchronization is achieved based on the grid peak amplitude detection through a revised orthogonal signal generation. Since the grid phase angle is not provided directly, a PR controller with harmonic compensations is adopted over a DQ frame control to achieve the zero steady-state inverter output current. A PQ controller with stable and robust performance is also described. Based on the simulation results, the active and reactive power can be well controlled and decoupled under various grid fault conditions such as grid frequency drift, grid voltage sag and swell, and grid voltage distortion.

Chapter 4 Experimental Test Results

4.1 Experimental Test Station

To validate the control design performed in previous chapters, a scaled-down prototype, as shown in Fig. 4-1, is constructed. The parameters used are given in Table 4-1. The H-bridge is built with evaluation boards from Cree® [57]. The LCL filter and sensing circuits are built on breadboards. A DC supply has been used to provide the high DC voltage bus. The controllers and serial communications are implemented on a 32-bit float point digital controller, TI's F28335. A variable transformer is connected between the inverter and the grid for grid-tied inverter mode test to provide isolation. Off-grid and On-grid tests are conducted.

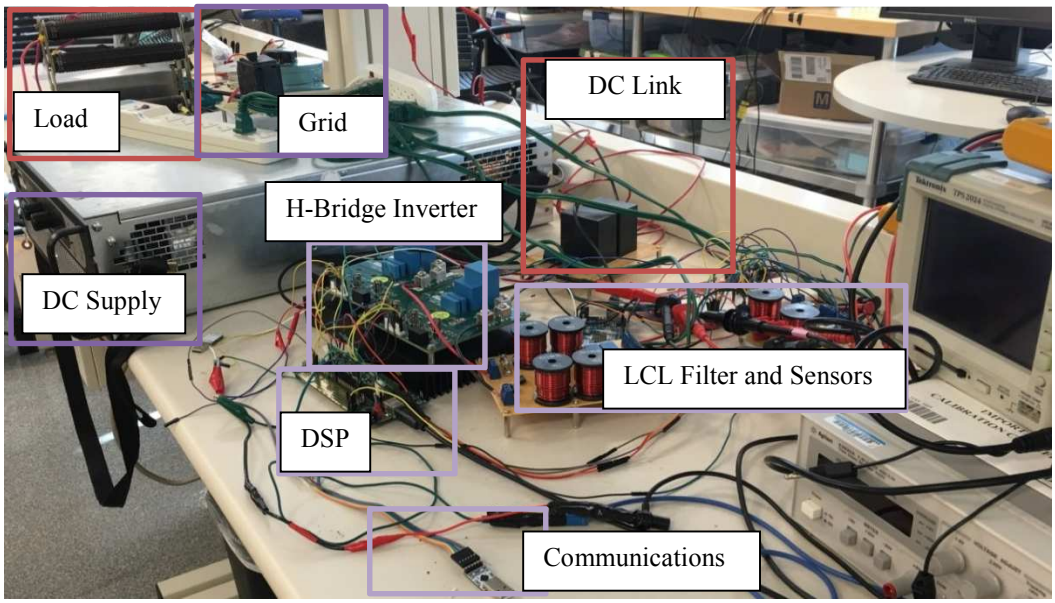

Fig. 4-1: Experiment test station of a single-phase inverter with LCL filter

Table 4-1: Parameters used for experimental test

Parameter	Value	Parameter	Value
DC bus V_{dc}	200/400 V	Sampling frequency f_s	30 kHz
Switching frequency f_{sw}	30 kHz	L_1	2.2 mH
C	9.8 µF	L_2	1.1 mH

4.1.1 Stand-Alone Mode

This section shows the test results of the stand-alone inverter operation. As discussed in Chapter 2, the synchronous frame PI control is implemented. The inverter is tested to output 120 VAC and 240 VAC when the DC bus is 200 VDC and 400 VDC, respectively. The closed-loop inverter with 120 VAC output at no load condition is shown in Fig. 4-2. In Fig. 4-2, CH1 (100 V/div) is the inverter output voltage, CH2 (40 V/div) is the DC supply voltage, CH3 (2 A/div) is the load current, and CH4 (1 A/div) is the DC supply current. When the inverter generates 120 VAC output with no load, the THD of the inverter output voltage is 3.93 %, as shown in Fig. 4-3.

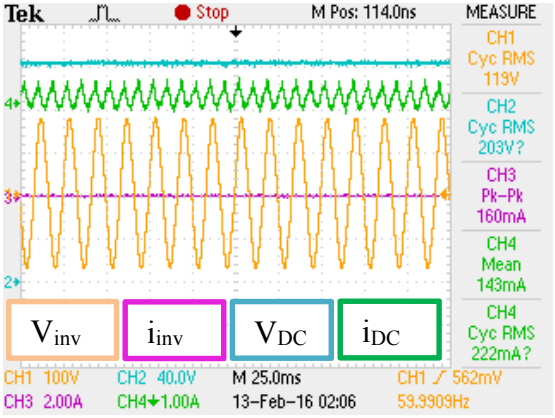

Fig. 4-2: 120 VAC stand-alone inverter output with no load (synchronous frame PI)

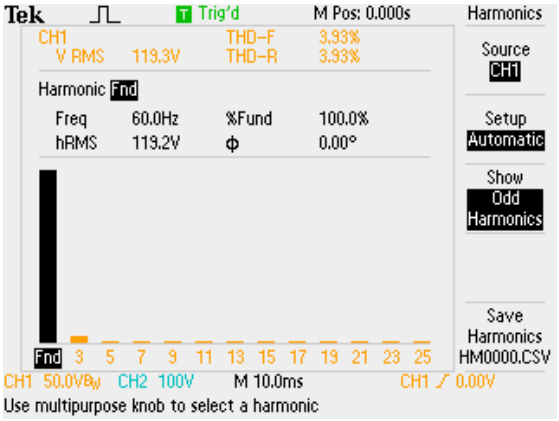

Fig. 4-3: The THD of the stand-alone inverter output with no load at 120 VAC

When a 135 W resistive load is added to the inverter output, the steady-state performance of the inverter is shown in Fig. 4-4. The THD of the inverter output voltage is 2.56 % when the inverter is connected with a 135 W resistive load, as shown in Fig. 4-5.

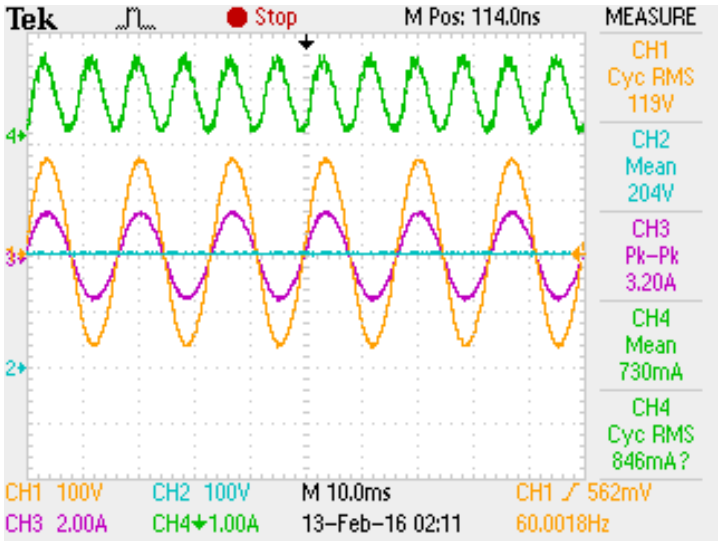

Fig. 4-4: 120 VAC stand-alone inverter output with a 135 W load

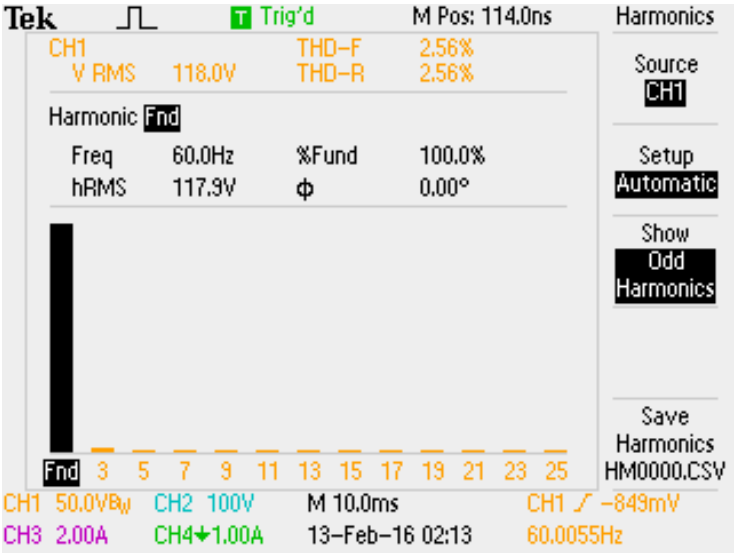

Fig. 4-5: The THD of the120 VAC stand-alone inverter output with a 135 W load

The load step transient response of the inverter output from no load to a 135 W load is given in Fig. 4-6.

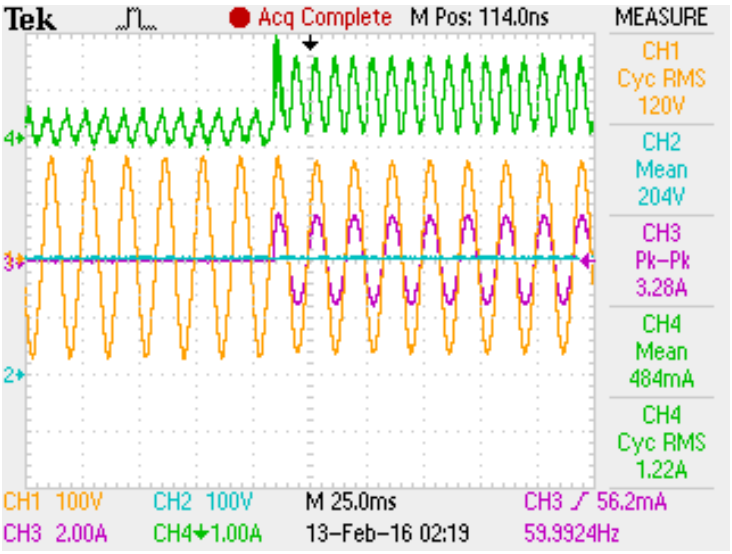

Fig. 4-6: Step load response of the stand-alone inverter

The inverter with 240 VAC output at no load condition is shown in Fig. 4-7. The THD of the inverter output voltage with no load is 2.40 %, as shown in Fig. 4-8.

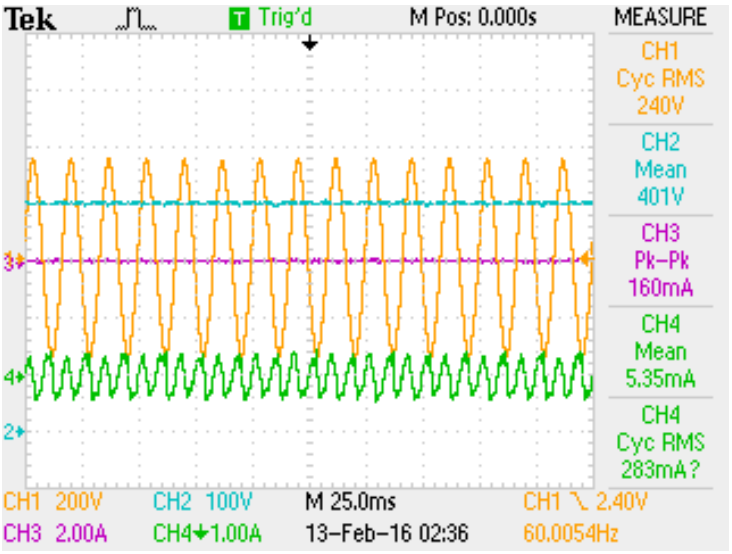

Fig. 4-7: 240 VAC stand-alone inverter output with no load

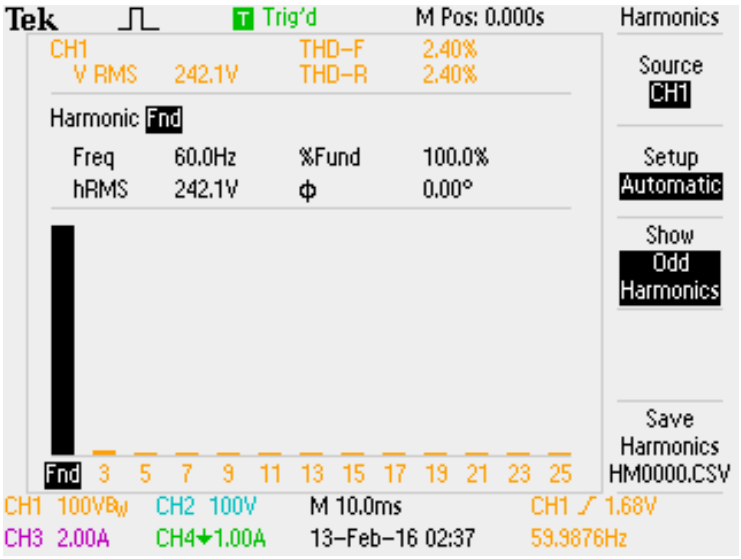

Fig. 4-8: The THD of the stand-alone inverter output with no load at 240 VAC

When a 500 W resistive load to the inverter output, the steady-state performance of the inverter is shown in Fig. 4-9. The measured system efficiency is 94.9 %. The load step transient response of the inverter output from no load to a 500 W load is given in Fig. 4-10.

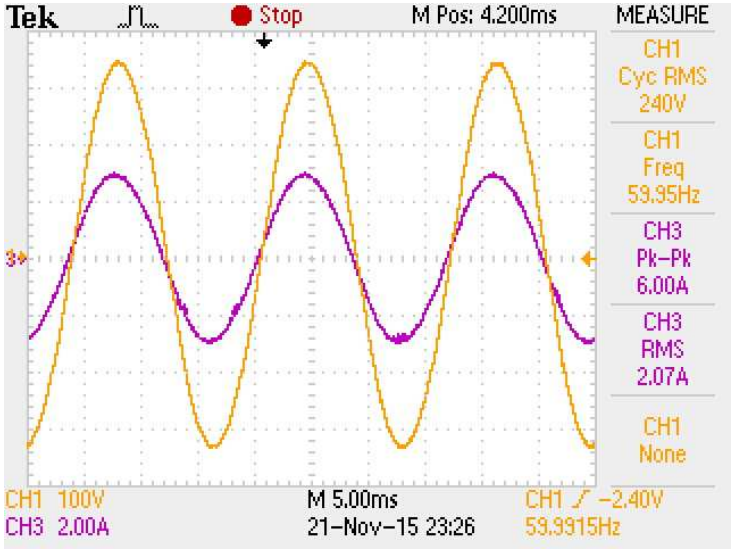

Fig. 4-9: 240 VAC stand-alone inverter output with a 500 W load

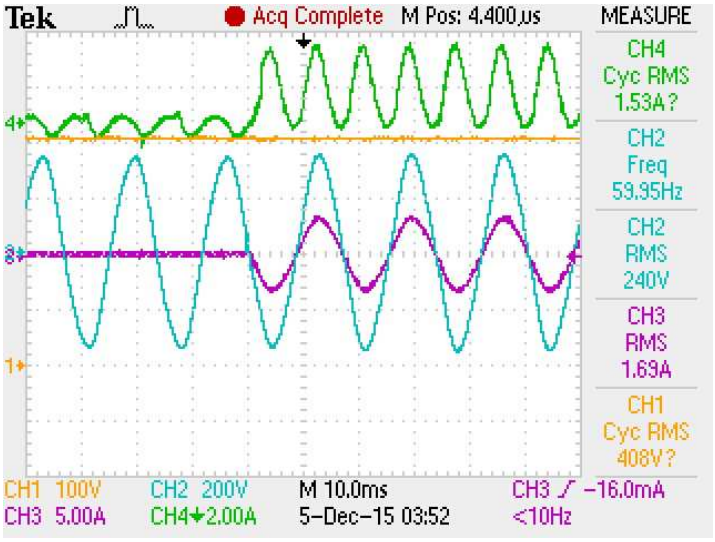

Fig. 4-10: 500 W step load response of the stand-alone inverter at 240 VAC

4.1.2 Grid-Tied Mode

This section shows the test results of the grid-tied inverter operation. The inverter is first configured to output 120 VAC when it is tied to the grid through a variable transformer (0 ~ 140 VAC). The control references are the current references. The current references are given through a serial communication based user interface built in LabView®. The serial communication is set to be 115200 baud rate, 8 data bits, and 1 stop bit. The user interface is displayed in Fig. 4- 11. Due to the time constraint, the PQ control is not implemented. However, by varying the current references, the active power and reactive power can also be decoupled and controlled. When the I_P^* reference is increased to 3 A, the inverter sends 270 W real power to the grid as shown in Fig. 4-12. CH1 (100 V/div) is the grid voltage, CH2 (100 V/div) is the voltage across the filter capacitor, and CH3 (5 A/div) is the current flowing into the grid. In Fig. 4-12, CH3, which represents the current flowing into the grid, is 10 A/div.

Fig. 4-11: Serial communication based user interface

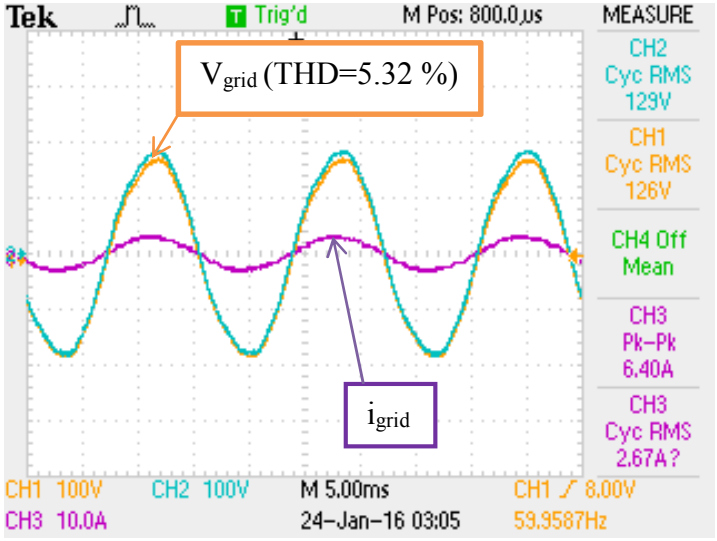

Fig. 4-12: Grid-tied inverter with 270 W output (PR+HC control)

As discussed in Chapter 3, the inverter can also handle delivering or sinking reactive power. Keeping the active power output constant and varying the I_Q^* reference to 2 A, the inverter sends 269 W real power and 180 Var to the grid as shown in Fig. 4-13. Negating the current reference I_Q^*, the inverter is able to receive 178 Var from the grid as displayed in Fig. 4-14. Fig. 4-15 shows the THD of the inverter output current at the current condition is 4.32 %.

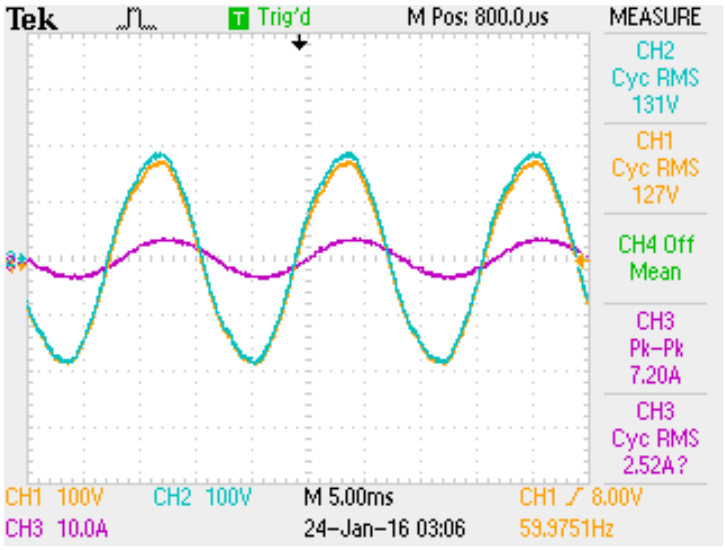

Fig. 4-13: Grid-tied inverter with 269 W and 180 Var output

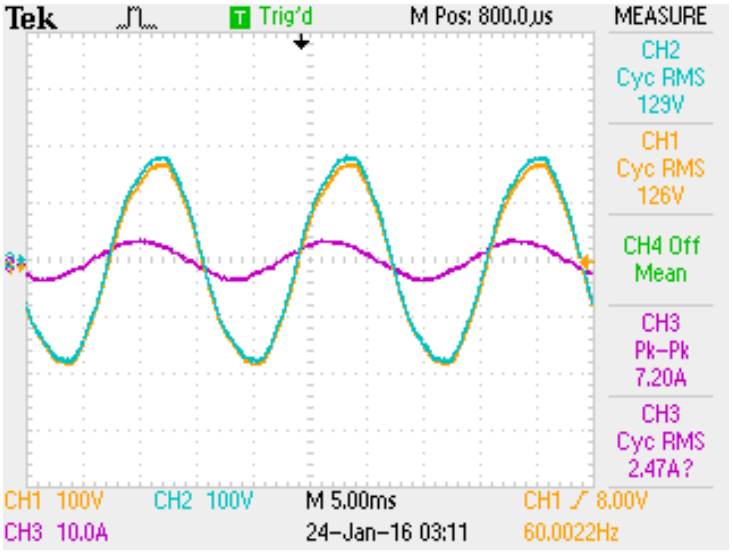

Fig. 4-14: Grid-tied inverter with 267 W and -178 Var output

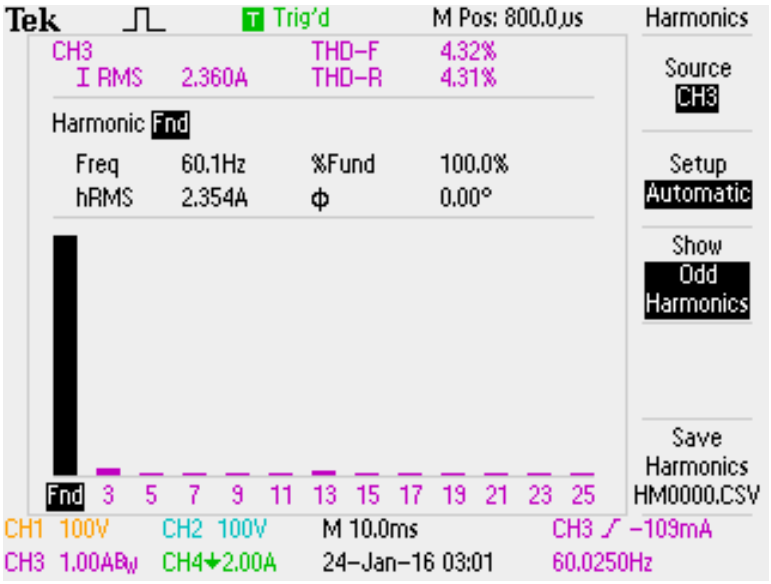

Fig. 4-15: The THD of the inverter output current

The inverter is then tied with the grid at 240 VAC. When the I_P^* reference is set to be 4.5 A, the inverter sends 750 W real power to the grid with 0.99 power factor, as shown in Fig. 4-16. CH1 (200 V/div) is the grid voltage, CH2 (10 A/div) is the inverter output current, and CH4 (100 V/div) is the high voltage DC bus. The THD of the inverter current is 3.71 %, as shown in Fig. 4-17.

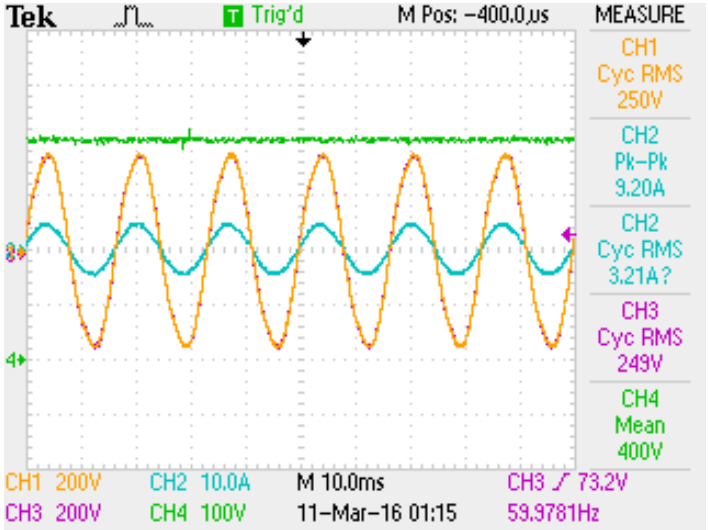

Fig. 4-16: Grid-tied inverter with 750 W output

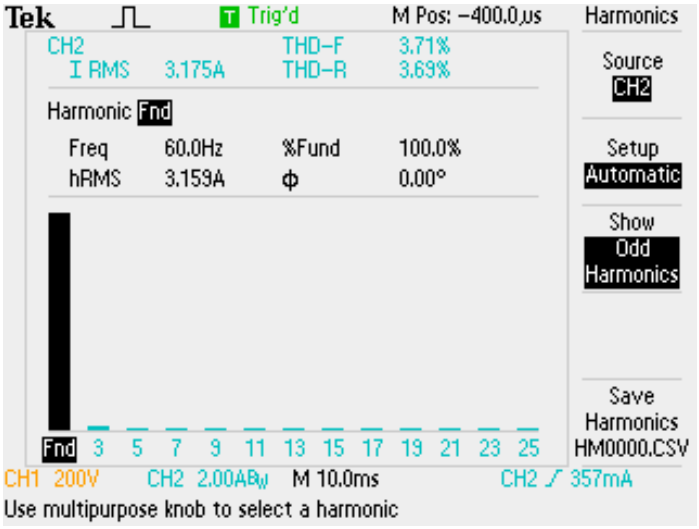

Fig. 4-17: The THD of the inverter output current (750 W)

The inverter is also tested to deliver reactive power and to sink reactive power. Fig. 4-18 shows the experimental result when the I_P^* reference is set to be 4.0 A, and the I_Q^*reference is set to be 2.0 A. In Fig. 4-18, the inverter outputs 663 W real power and 324 Var reactive power to the grid. The power factor is 0.90 lagging, and the phase angle difference between inverter output voltage and current is 26.04º.

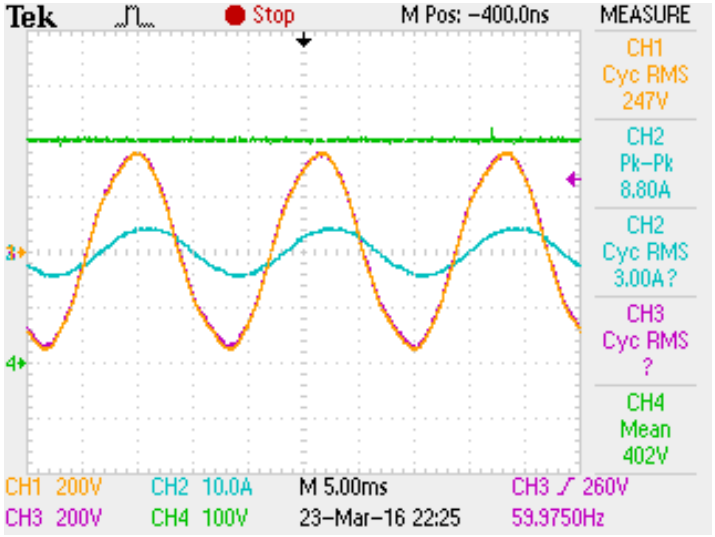

Fig. 4-18: Inverter current output with 0.90 lagging power factor

Fig. 4-19 shows the experimental result when the I_P^* reference is set to be 4.0 A, and the I_Q^* reference is set to be -1.0 A. In Fig. 4-19, the inverter outputs 618 W real power and sinks 193 Var reactive power to the grid. The power factor is 0.95 leading, and the phase angle difference between inverter output voltage and current is 17.33º.

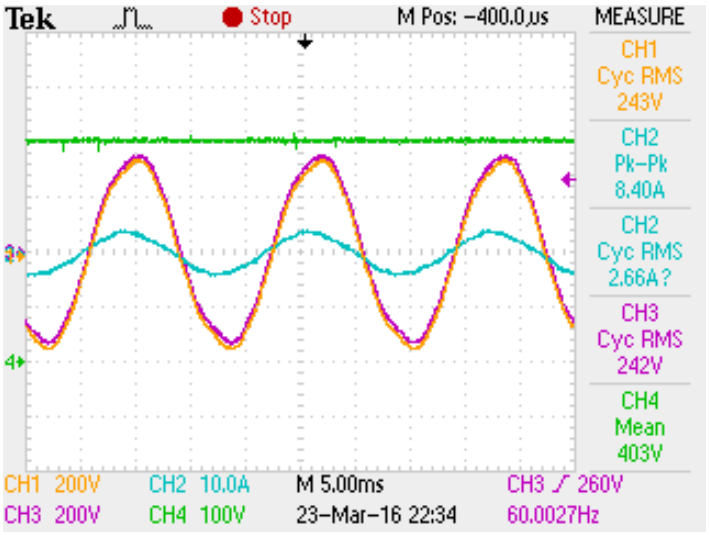

Fig. 4-19: Inverter current output with 0.95 leading power factor

Chapter 5 Conclusion and Future Work

5.1 Conclusion

This thesis presented controls of a single-phase inverter for residential PV application. This thesis reviewed solar energy, PV inverter configurations, and inverter filter topologies. Passive hardware component parameters design was discussed. Controllers were designed for both stand-alone mode and grid-tied mode single-phase inverter. The modeling and control design were verified by the simulation and experimental results. For stand-alone inverter control, the outer control loop regulates the filter capacitor voltage. As to the inner loop feedback signal, a comparison was made between choosing the inverter-side inductor current and using the capacitor current. Theoretically, the load current is included within the inner control loop when using the filter capacitor current feedback. Therefore, the system can achieve more robust transient response during load changes. This analysis was verified in the simulation, which showed that regulating the capacitor current as the inner loop had a superior transient response when the resistive load changes. Synchronous frame DQ control and PR control were proposed in other previous publications for systems to achieve zero steady-state error when tracking sinusoidal references. The zero steady-state tracking performance was verified by the simulation and experimental test performed in this project. Using the designed control, both the simulation and experimental results showed that the THD of the inverter output voltage, which is less than 5 %, satisfied IEEE 519-1992 standard. For grid-tied inverter control, the proportional capacitor current feedback is used to achieve active damping. The outer current loop directly regulates the current that goes to the grid. A serial communication based user interface is developed to feed the control references. With the designed PR controller, the current injected into the grid could accurately follow the given sinusoidal control references in both simulation and experimental test.

Several PLL methods have been reviewed and analyzed, and the SOGI based grid synchronization has been chosen for its superior harmonic filtering capability, fast response, and simplicity. The simulation and test results validated that the active power and reactive power were decoupled with the grid synchronization unit and the reactive power could be either injected into the grid or absorbed from the grid. In the test, the maximum reactive power absorbed from the grid is 299 VAR, and the maximum reactive power sent out to the grid is 435 VAR. The tested power factor ranges from 0.86 leading to 0.80 lagging. Both the simulation and experimental results showed that the THD of the grid-tied inverter output current, which is less than 5 %, satisfied IEEE 519-1992 and 1547 standards for distributed resources.

5.2 Future Work

This project can be continued and extended to design a high efficiency DC/DC converter stage and a reliable MPPT technique as future work. Seamless transitions between island mode and grid-tied mode need to be developed. To realize the transitions, the frequency estimation of the grid voltage will be needed. In addition, a practical PCB can be created for the rated power inverter. The PQ controller developed in the simulation can also be implemented in the hardware. For future experimental test, PV modules can be used and the DC bus can be provided by the DC/DC conversion stage instead of a DC supply. When PV modules are used, the range of reactive power compensation needs to be revaluated due to the equivalent impedance change on the DC side. The project can also extend to design energy storage units like batteries and super capacitors to store the harvested solar energy for utilization at night. Furthermore, the serial communication can also be improved and replaced by Ethernet communication for extended connectivity and faster communication speed. Since the active power and reactive power can be controlled, research on power management can also be conducted as future work.

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