Modeling and Simulation of 1700 V 8 A GeneSiC Superjunction Transistor

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Modeling and Simulation of 1700 V 8 A GeneSiC Superjunction Transistor

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Microelectronics-Photonics

by

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Bachelor of Science in Physics, 2011

August, 2016
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Dr. Rick Wise, Program Director       Dr. H. Alan Mantooth, Thesis Director
ABSTRACT

The first-ever 1.7kV 8A SiC physics-based compact SPICE model is developed for behavior prediction, modeling and simulation of the GeneSiC “Super” Junction Transistor. The model implements Gummel-Poon based equations and adds a quasi-saturation collector series resistance representation from a 1.2 kV, 6 A SiC bipolar junction transistor model developed in Hangzhou, China. The model has been validated with the GA08JT17-247 device data representing both static and dynamic characteristics from GeneSiC. Parameter extraction was performed in IC-CAP and results include plots showing output characteristics, capacitance versus voltage (C-V), and switching characteristics for 25 °C, 125 °C, and 175 °C temperatures.
ACKNOWLEDGEMENTS

This work was made possible under the leadership and advisement of Dr. H. Alan Mantooth and Ranbir Singh at the GeneSiC Semiconductor Company. Ranbir and GeneSiC were extremely generous in providing devices for testing within our device modeling lab. Acknowledgement is also due to Tom Vrotsos for his continuous involvement and guidance for the duration of this project.

Lastly, a Special Thanks to Michael Leonard, Shamim Ahmed, Sonia Perez, and Dr. Matt Francis for their roles of support.
DEDICATION

This thesis is dedicated to the people that believe I can do anything, thanks Emanuel III and Darla Brooks (whom I affectionately call Mom and Dad) for your unwavering faith in me and my abilities; also, to all Friends and Family that have supported this journey.

This work is especially dedicated to my one true love and biggest encourager, Travis Adams. Thank you for being my strength through this process and letting me cry, but not letting me quit.

I am eternally grateful for the life we get to share together.
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CHAPTER 1: INTRODUCTION

1.1 Semiconductor Device Modeling

Developments in semiconductor technology have created a dynamic increase in the need for accurate device models for proper circuit simulation. Semiconductor device models vary in complexity, ranging from physics-based models to simple equivalent circuit models. While both serve respective purposes for modeling, they each come with limitations. Physics-based models often delve into the fundamental physics of device operation; and while it is detailed and accurate, the user sacrifices simulation and analysis speed. Equivalent circuit models are generally limited in use because of non-linear behavior and dependencies on DC bias and frequency. Equivalent circuit models thrive, however, in that they are substantially less difficult to implement and analyze [1].

1.1.1 Purpose and Importance of Device Modeling

Models allow a user to predict device behavior and are used in the circuit design process. Ease of the circuit design process relies heavily on models, whether computer-based or by hand, enabling the user to determine if a proposed design will work correctly. Accurately modeling devices ensures proper simulation analysis for integrated circuits which has a direct effect on time efficiency and fabrication expense. Regardless of engineering field, models aid in the modern engineering design process [2].

Device models differ in levels of complexity. Varying needs allow for varying-level models as not every effect is necessary for every circuit simulation. Semiconductor device models are often universally recognized to fit into one of six levels [3].
Level-0: The Level-0 model is an ideal behavioral model with no real physical representation. Often an ideal electrical switch, this level model is used for basic proof of concept allowing for fast (in the micro- to nano-second ranges), rough simulation.

Level-1: A basic behavior model, Level-1 models the basic properties of the device. This level is suitable for basic circuit methodology testing and validation.

Level-2: Level-2 models mark the beginning of physical representation within semiconductor operation. These models are one dimensional and actively describe dynamic characteristics. The model described in this work is a Level-2 model.

Level-3: Typically fully physics-based, Level-3 models accurately describe the device physics. Level-3 models often include self-heating effects.

Level-4: Level-4 models are complete, complex models representing all relevant physical parameters of a device. These models should be able to provide two- or three-dimensional representation of device design and provide information on failure behavior.

Level-5: Level-5 models account for long-term radiation, degradation, and many other effects due to power or thermal cycling. Very few Level-5 models exist for semiconductor devices due to model complexity.

1.1.2 Model Simulators and HDLs

Simulation is defined as the “imitation of the operation of a real-world process or system [over time]”. Computer simulators are programs that enable a computer to execute such an “imitation”. Device models aim to accurately describe physical and electrical behaviors by means of mathematical real-world representation through simulation. Electrical and electronics
computer-aided design (CAD) uses numerous simulator programs including but not limited to the following: variations of SPICE: HSPICE, Berkley-SPICE, PSPICE, Spectre, Saber, etc.

Hardware description languages (HDLs), specifically within electronics, are computer “languages” that are used to program the structure, design, and operation of electronic circuits. The simulator and language used for this work was Spectre and Verilog-A.

**Spectre**

Electronic circuit simulation invokes the use of physical mathematical models to describe the behavior of an electronic device. Design efficiency is improved with the ability to simulate device and circuit behavior. Spectre is an industry standard SPICE circuit simulator developed at Cadence Design Systems. The simulator provides SPICE analyses and supports the Verilog-A HDL.

**Verilog-A Hardware Description Language**

Verilog is a standardized HDL used to model electronic systems. Since its first appearance in 1984, variations and subsets of the language have emerged. Verilog-AMS is a derivative of the Verilog language that incorporates analog and mixed-signal extensions (hence the ‘AMS’) in effort to describe analog and mixed-signal behaviors. Verilog-A allows circuit designers to create behavioral blocks in a circuit and mathematically define the behavior between the currents and voltages.

**1.2 GeneSiC “Super” Junction Transistor**

GeneSiC Semiconductor has, in recent years, developed and released a 1700-V class of silicon-carbide (SiC) “Super” Junction Transistors (SJT). These SJTs are described as being gate-oxide free, normally-off, quasi-majority carrier devices exhibiting a square reverse biased
safe operating area (RBSOA) capable of 250 °C operation. GeneSiC has been aggressively
developing these devices in voltages ranging from 1.2 kV to 10 kV with current gains measuring
at 88 and switching speeds of less than 20 ns. GeneSiC Semiconductor aims to increase power
conversion efficiency and reduce the size, weight, volume of commercial power electronics
through incorporation of these SiC SJTs [4-8].

Note: Though these devices are bipolar transistors, the GeneSiC datasheet labels the device
terminals as “gate, source, and drain”. However, for brevity and consistency, this work will use
the bipolar transistor terminal references of “base, collector, and emitter.” Also, the device used
for the work presented is an NPN bipolar transistor.

1.2.1 Semiconductor Superjunction Device Theory

Semiconductor power devices aim to keep specific on-resistance values as low as
possible while maintaining large breakdown voltage values. This is often a difficult task. Dr.
Tatsuhiro Fujihi, current Chief Technology Officer of Electronic Devices for Fuji Electric Co.,
Ltd., in Japan, developed the semiconductor “superjunction” (SJ) device theory to address and
overcome the trade-off relationship between the two within conventional semiconductor devices.
Essentially, SJ devices employ alternately stacked, heavily doped, p- and n-type layers [9].

According to the SJ theory, the structure then operates as a p-n junction with low on-
resistance and high breakdown voltage by controlling the degree of doping and thickness of the
p- and n-type layers. Analysis based on the SJ formulas, for ideal specific on-resistance and
breakdown voltage, and simulation shows that the on-resistance of SJ devices can be reduced by
two orders of magnitude to that of conventional semiconductor devices [9]. This theory has been applied in recent years in the development of CoolMOS (SJ MOSFETs)[10-13].

GeneSiC SJTs are fabricated with n-type drift epilayers fashioned for 1.2 kV blocking and “optimally designed” for achieving current gains as high as 88 and on-resistance as low as 5.8 mΩ-cm². [4].

1.2.2 GeneSiC SJT Device Applications

GeneSiC Semiconductor SJTs have an array of relevancy within power electronics. The 1.2 kV to 10 kV range allows use for high efficiency power conversion within the varying areas of aerospace engineering, defense, down-hole oil drilling, and inverter applications [5].

1.3 Thesis Structure

This thesis has been structured as follows:

Chapter 2: SiC as a Device Material- A brief overview of SiC material and electrical properties is given as well as the role of SiC in power electronics.

Chapter 3: BJT Principle Overview- Basic Power BJT operating principles are discussed.

Chapter 4: SiC SJT Model Description- A description of the SiC bipolar junction transistor model is presented for use of characterizing the GeneSiC SJT device (GA08JT17-247)

Chapter 5: Model Characterization and Validation- Results and validation of the model through simulation are presented.

Chapter 6: Conclusions and Future Work- A summary with key contributions and drawn conclusions of the work is provided.
CHAPTER 2: SiC AS A DEVICE MATERIAL

2.1 SiC in Power Electronics

Si power devices have been the long-reigning material of choice for power electronics. However, there are properties of Si that make it less appealing for use. The narrow bandgap, low thermal conductivity, and low breakdown voltage of Si create limits for power devices in areas of high power and high temperature operations.

SiC is deemed advantageous for use in power electronics applications. Though silicon (Si) is still relevant as a device material, SiC provides a wide bandgap, high critical electric field, and high thermal conductivity in comparison to Si, providing opportune circumstance for improved power device performance.

2.2 Material and Electrical Properties

2.2.1 SiC Structure and Polytypes

SiC is composed of two group-IV elements, Si and Carbon (C). A covalent bond is made by the sharing of electrons between one Si atom and four C atoms. The bond length between Si and C atoms is approximately 1.89Å and the length from Si to Si (or C-C) is approximately 3.08Å (Fig. 2.1)[14].

Fig. 2.1: Basic crystal structural unit of SiC [14].
SiC is a polytypic material, meaning that the material has variant subdivisions of crystalline structures. Each variant SiC structure is called a polytype. The most common SiC polytypes are 3C, 4H and 6H; so defined and named by the stacking sequences [14]. Figure 2.2 displays the different stacking sequences for 3C, 4H, and 6H crystal structures in SiC. 3C is a cubic structure with ABC stacking sequence while 4H and 6H are hexagonal structures with ABAC and ABCACB sequences, respectively [14]. 4H-SiC has been the most widely used polytype because of its high mobility and bandgap in comparison to 3C-SiC and 6H-SiC, and is the variation of SiC used for this work.

2.2.2 Wide Bandgap

The bandgap, or energy gap, in semiconductor materials is described as the energy difference (in electronvolts – eV) between the top of the valence band and the bottom of the conduction band. In solid-state physics, the bandgap is a region where no electron states exist. The bandgap represents (in eV) the energy requirement to create a mobile carrier within the semiconductor by freeing a valence electron from orbit, allowing free movement.
4H-SiC has a wide bandgap of 3.26 eV in comparison to 1.12 eV of Si. The larger bandgap of SiC results in smaller thermal generation of carriers in the depletion region allowing for less leakage current for a given blocking voltage than Si. Table 2.1 shows a comparison of the SiC polytype band gaps to Si as well as comparison of other varying electrical properties. The bandgap variation with temperature for 4H-SiC is represented in Eq. (2.1) [15].

\[ E_g = 3.26 - 7.02 \times 10^{-4} \frac{T^2}{(T + 1300)} \text{ eV} \quad (2.1) \]

Thermally generated electron-hole pairs, at any given temperature \( T \), determine the intrinsic carrier concentration. The intrinsic carrier concentration of Si increases from \( 1.4 \times 10^{10} \text{ cm}^{-3} \) at room temperature to \( 1.0 \times 10^{15} \text{ cm}^{-3} \) at 540 °K compared to the low intrinsic carrier concentrations of SiC of \( 6.7 \times 10^{-11} \text{ cm}^{-3} \) at room temperature and only \( 3.9 \times 10^7 \text{ cm}^{-3} \) at 700 °K, as shown in Fig. 2.3. The ability of the intrinsic carrier concentration of SiC to stay low at elevated temperatures, because of the wide bandgap, makes SiC the favorable material over Si for high temperature applications [15].

Fig. 2.3: Intrinsic carrier concentration comparison of Si and 4H-SiC over temperature [14].
2.2.3 Critical Electric Field

Aside from the intrinsic carrier concentration, another bandgap-dependent property of 4H-SiC is the critical electric field. Power devices can be designed for optimal performance with the same blocking voltages due to the critical electric field of SiC being approximately ten times higher than that of Si. For the same blocking voltage, SiC offers specific on-resistance more than 300-times lower than that of Si. Also, the thinner and more highly doped devices enable SiC devices to operate at higher frequencies than Si.

2.2.4 Thermal Conductivity

The high thermal conductivity of SiC makes it advantageous for high power densities. A notable advantage to SiC devices is that heat can dissipate faster, reducing the need for heavy heat sinks and complex thermal packaging, due to the three-times higher thermal conductivity than that of Si. This allows the device to maintain a maximum power output, enabling long-term reliability.

Table 2.1: Electrical properties of SiC in comparison to Si [15].

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>3C-SiC</th>
<th>4H-SiC</th>
<th>6H-SiC</th>
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<tr>
<td>Energy Bandgap, $E_g$ (eV at 300 °K)</td>
<td>1.12</td>
<td>2.4</td>
<td>3.26</td>
<td>3.0</td>
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<tr>
<td>Critical Electric Field, $E_c$ (V/cm)</td>
<td>$2.5 \times 10^5$</td>
<td>$2 \times 10^6$</td>
<td>$2.2 \times 10^6$</td>
<td>$2.5 \times 10^6$</td>
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<tr>
<td>Thermal Conductivity, $\lambda$ (W/cm • K at 300 °K)</td>
<td>1.5</td>
<td>3-4</td>
<td>3-4</td>
<td>3-4</td>
</tr>
<tr>
<td>Electron Mobility, $\mu_n$ (cm²/V•s)</td>
<td>1350</td>
<td>1000</td>
<td>950</td>
<td>500</td>
</tr>
<tr>
<td>Hole Mobility, $\mu_p$ (cm²/V•s)</td>
<td>480</td>
<td>40</td>
<td>120</td>
<td>80</td>
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<tr>
<td>Saturated Electron Drift Velocity, $V_{sat}$ (cm/s)</td>
<td>$1 \times 10^7$</td>
<td>$2.5 \times 10^7$</td>
<td>$2 \times 10^7$</td>
<td>$2 \times 10^7$</td>
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<tr>
<td>Dielectric constant, $\epsilon_r$</td>
<td>11.9</td>
<td>9.7</td>
<td>10</td>
<td>10</td>
</tr>
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CHAPTER 3: BJT PRINCIPLE OVERVIEW
3.1 Basic Operation of BJT

First introduced in 1947, the bipolar transistor is a three terminal device—terminals are labeled Base, Collector and Emitter (B, C, E)—consisting of two “back-to-back” p-n junctions. The principle operation of a BJT relates to its function as a controlled source of constant current [16]. This work utilizes the BJT as a switch. Because each p-n junction composing the device can either be forward- or reverse- biased, there are four biasing possibilities for the BJT (Fig. 3.1) [17-18].

![Diagram showing the four BJT modes of operation](image)

**Fig. 3.1: The four BJT modes of operation.**

**Normal Active Mode:** When the base-emitter junction is forward-biased and the base-collector junction is reverse-biased, the BJT operates in normal active mode. This is the principle operation for the device. The reverse biased base-collector junction serves as a current source and the forward-biased base-emitter junction provides a controlled current to the base-collector junction.
Cutoff: If neither the base-emitter junction nor the base-collector junction is forward-biased, the BJT is in cutoff mode; all terminal currents are zero and the output is an open circuit. Essentially, the BJT is a switch of "off" mode.

Saturation: The BJT is in saturation mode when both junctions are forward-biased. In reference to BJTs, a device in saturation operates as a switch in “on” mode; the output voltage and output current do not change with the input base-emitter voltage.

Inverse Active Mode: The inverse active mode is noted by a forward-biased base-collector junction and reverse-biased base-emitter junction. Operating as a controlled current source, the collector releases carriers that are gathered by the emitter.

3.2 Power BJT

3.2.1 Power BJT Structure and Operation

Structure

The basic structure for an NPN BJT is shown in Figure 3.2. The power transistor structure adds a lightly doped N-Drift region that allows for elevated blocking voltages to the $N^+$ emitter and P- base regions in comparison to the standard low-power BJT. The vertical structure is often given preference over the lateral device for power transistors. This is because the vertical structure allows for a maximized cross-sectional area for device current to flow through, minimizing on-state resistance, power dissipation, and also thermal resistance of the transistor [19]. The doping levels and thickness for each transistor layer directly affect characteristics of the device. The $N^+$ emitter region is usually large (typically $10^{19}$ cm$^{-3}$), whereas the P- base region is doped moderately (typically $10^{16}$ cm$^{-3}$) in comparison. The N-Drift region, formed by the collector half of the collector-base junction, is lightly doped (typically $10^{14}$ cm$^{-3}$) and the
$N^+$ region that terminates the drift region is doped similarly to that of the emitter. The N-Drift region thickness determines the breakdown voltage of the transistor. The P- base region thickness is typically engineered as small as possible in order to produce satisfactory amplification capabilities but must not be made too small as to not compromise the breakdown voltage capability [19].

![Diagram](image_url)

Fig. 3.2: Basic power BJT structure. $J_1$ represents the base-emitter junction and $J_2$ represents the base-collector junction.

**Operation**

Operation of a BJT is caused by the collection of minority carriers in a separate junction after the injection of minority carriers across a first junction [15]. When the collector terminal is positively biased, the collector-base junction, noted by $J_1$ in Fig. 3.2, becomes reverse biased and supports the voltage. Current flow is prompted by forward-biasing the emitter-base junction, $J_2$, in order to begin the injection of electrons. Illustrated in Fig. 3.3, electrons are injected by forward-biasing the base-emitter junction, causing current flow. The injected electrons diffuse through the P-base region and arrive at the base-collector junction creating a base current $i_B$. When reverse-biased, electrons captured by the base-collector junction are swept across the depletion region, producing a collector current $i_C$ [15].
3.2.2 Operating Principles

Current Gain

Fig. 3.4 labels the internal currents of the transistor. $I_{pe}$ is the diffusion current stemming from holes injected into the emitter from the base and $I_{ne}$ is the diffusion current from electron injection from the emitter to the base. As briefly mentioned before, these electrons then diffuse across the base and those that endure recombination arrive at the collector-base depletion layer; these are excess electrons. These electrons are then swept across the depletion layer in to the collector, represented by the $I_{nc}$ current. The gain beta ($\beta$) is characterized by the ratio of the collector current, $i_c$, to the base current, $i_b$, and the terminal currents, $I_C$ and $I_B$, can be expressed in terms of the internal currents [19].

The collector current is represented by:

$$I_C = I_{nc}$$  \hspace{1cm} (3.1)
and the base current is expressed as:

\[ I_B = -I_C - I_E = -I_{nc} + I_{ne} + I_{pe} \] (3.2)

Beta is then expressed in terms of current as:

\[ \frac{I_B}{I_C} = \beta = \frac{I_{ne} - I_{nc}}{I_{nc}} + \frac{I_{pe}}{I_{nc}} \] (3.3)

Assuming that the transistor is operating in the active region, the base-emitter junction is forward biased and the collector-base junction is reverse biased. Minority carrier distributions, shown in Fig. 3.5, are produced by electrons injected into the base from the emitter and holes injected into the emitter. Injected electrons from the emitter to the base are likely to exit the base through the collector as opposed to the base terminal. The base region thickness is made small compared to electron diffusion length in the base so electrons are not likely to recombine in the base. Also, the collector region is larger than the emitter and base contact; therefore, electrons
diffusing away from the emitter have a higher probability of encountering the collector because of the short distance from the emitter to collector [19].

There are three main requirements for large values of beta in a bipolar transistor:

1) heavy doping of the emitter,
2) long minority-carrier lifetimes in the base, and
3) short base thickness.

![Diagram](image)

**Fig. 3.5:** Stored charge distribution in BJT normal active region.

For beta to have a large value, the internal current numerators of the terms in Eq. 3.3 need to be small in comparison to the $I_{nc}$ denominator. The $I_{ne} - I_{nc}$ term notes the difference in electrons injected into the base at the base-emitter junction and the electrons swept across the collector-base junction into the collector and is created by the recombination of some of the injected electrons in the base region. This difference can be minimized by having increased minority carrier lifetimes and shortening the thickness in the base region. The $I_{pe}$ term can be minimized by heavily doping the emitter so that the stored hole distribution becomes smaller.

These factors, however, conflict with other desirable device characteristics (such as switching times) and trade-offs must be considered [19].
3.2.3 Output Characteristics

The typical output characteristics for a power bipolar transistor can be seen in Fig. 3.6. The varying curves are distinguished by the values of the applied base current. The most notable observable difference in the power bipolar transistor and its low-power logic-level counterpart is the quasi-saturation region. Low-power transistors do not possess a drift region and therefore do not exhibit the quasi-saturation effect; otherwise, the major transistor features are shared.

Quasi-saturation Region

One major difference between the power BJT and the low-power BJT is noted in the saturation region seen in the output characteristics. The saturation region can, in fact, be separated into two regions: “hard” saturation and “quasi-saturation” noted in Fig. 3.6. The quasi-saturation effect, specific to power transistors, is noted as the gradual transition between the saturation and forward active regions and is the result of introducing the lightly-doped drift region, lacking in the low-power BJT structure. In the quasi-saturation region, the base-collector junction is forward biased but excess minority carriers fail to short out the drift region; also, resistivity in the region is affected by the base current. During quasi-saturation, the total drop in voltage across the device is greater than that of saturation.

In the event of quasi-saturation, it is again assumed that the transistor is initially in the active region. The collector-emitter voltage drops due to an increased voltage drop across the collector load. This is caused by a rise in collector current in response to a rising base current. There is, however, a simultaneous increase in the voltage drop in the drift region as a result of its ohmic resistance due to the increase in $i_c$, meaning the reverse bias across the collector-base junction is getting smaller and the junction will eventually become forward biased. Space charge
neutrality requires that electrons be injected into the drift region in approximately the same proportion as the holes and electrons are obtained from the number of electrons being supplied to the collector-base by injection from the emitter and diffusion across the base. Quasi-saturation region is entered as the excess carrier build-up in the drift region ensues. If the ohmic resistance of the drift region is $R_d$ and $v_{CE}$ is the collector-emitter voltage, then the boundary between the quasi-saturation region and the active region is given by:

$$i_C = \frac{v_{CE}}{R_d}$$  (3.4)

![Diagram showing the output characteristics of a power transistor.](image)

Fig. 3.6: Output characteristics of power transistor.

### 3.2.4 Switching Characteristics

Bipolar power transistors were developed for power circuit applications including motor control. In these circuits, the device regulates the current being delivered to a load by serving as a switch between the on- and off-states. The loads can be either resistive or inductive in nature. Assuming an inductive load, the device switches from the blocking state to the on-state while supporting the collector supply voltage, with a voltage drop during the turn-on transient. The device switches from the on-state to the collector supply voltage during the turn-off transient. These transitions determine the power losses incurred when the bipolar power transistor is operated at high frequencies [15].
CHAPTER 4: SJT MODEL
4.1 Current State of SiC BJT/SJT Models

4.1.1 SiC BJT Models

Since the inception of the Si BJT, device models have been formulated to describe the physical and electrical behavior. One of the first (Si) BJT models was developed by Ebers and Moll in 1954 [20]. Though the mathematical simplicity of the model encourages ease of use, the Ebers-Moll (EM) model neglects many effects that occur in BJTs. The GP model was introduced in 1970 by Gummel and Poon [21]. It is the most used model (as it is built in to many simulators such as HSPICE and Spectre) and addresses the effects that the EM model does not. Neither the EM nor the GP models were designed for SiC devices. Recently, other more advanced BJT models (though mostly for Si) have been used in the semiconductor industry, each with advantages and shortcomings; while they, many of them being physics-based models, address more device effects, longer simulation times are required. A main objective in device simulation is to use the simplest model that will accurately complete the job. Integrated circuit design heavily relies on compact device models for circuit simulation. The industry standard bipolar transistor modeling is based on SPICE GP model (SPG). Though several limitations exist for SGP model, few widely accepted alternatives are available to replace it. Several advanced models, such as vertical bipolar inter-company (VBIC), high current (HICUM) and MEXTRAM have been proposed and utilized [20-24].

With this in mind, it is useful to note some differences between current bipolar models. A brief description and comparison a few models and the device characteristics they feature is discussed.

The large signal equivalent circuits for all the models are in part based on the EM transport model. All models include a transfer current source, diodes for both ideal and non-ideal
base current components, and series resistances.

In comparison to the SPG model (version Spice3G2), newer models’ large signal equivalent circuits utilize a split B-E junction, split base resistance, a split B-C junction, a B-C avalanche current model and a self-heating network. A more detailed comparison of the large signal equivalent circuit model components can be seen in Table 4.1 [25-26].

Table 4.1: Bipolar transistor model comparison for the large signal equivalent circuit model components for SGP, VBIC, HICUM, and MEXTRAM.

<table>
<thead>
<tr>
<th>Component</th>
<th>SGP (Spice3G2)</th>
<th>VBIC</th>
<th>HICUM</th>
<th>MEXTRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>External B-E base current</td>
<td>-</td>
<td>$I_{BEX}$</td>
<td>$I_{JBE}$</td>
<td>$I_{B1S}$</td>
</tr>
<tr>
<td>B-E tunnel current</td>
<td>-</td>
<td>Part of $I_{BE}$</td>
<td>$I_{BET}$</td>
<td>-</td>
</tr>
<tr>
<td>Split base resistance</td>
<td>-</td>
<td>$R_{BX}$, $R_{B1}$</td>
<td>$R_{BX}$, $R_{B1}$</td>
<td>$R_{BC}$, $R_{B1B2}$</td>
</tr>
<tr>
<td>Charge parallel to $R_{BI}$ for AC current crowding</td>
<td>-</td>
<td>-</td>
<td>$Q_{RBI}$</td>
<td>$Q_{B1B2}$</td>
</tr>
<tr>
<td>Collector current source</td>
<td>-</td>
<td>$I_{RCI}$</td>
<td>-</td>
<td>$I_{C1C2}$</td>
</tr>
<tr>
<td>External B-C junction</td>
<td>-</td>
<td>$I_{BE}$</td>
<td>$I_{BCX}$</td>
<td>$I_{EX}$, $X_{IEX}$</td>
</tr>
<tr>
<td>BC avalanche current</td>
<td>-</td>
<td>Part of $I_{BC}$</td>
<td>$I_{AVL}$</td>
<td>$I_{VAL}$</td>
</tr>
<tr>
<td>Base resistance for PNP</td>
<td>-</td>
<td>$R_{PB}$</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Differences in models in terms of quasi-saturation representation are as follows in Table 4.2. Initially, SGP models did not address quasi-saturation; models have since been modified to address the phenomenon.
Table 4.2: Quasi-saturation model comparison for SGP, VBIC, HICUM, and MEXTRAM.

<table>
<thead>
<tr>
<th>Model</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>SGP</td>
<td>n/a</td>
</tr>
<tr>
<td>VBIC</td>
<td>Quasi-saturation effect is modeled with the KULL-Model [25-26]</td>
</tr>
<tr>
<td>HICUM</td>
<td>Quasi-saturation effect is included in operating point dependency of the forward minority charge $Q_{FT}$ [25-26]</td>
</tr>
<tr>
<td>MEXTRAM</td>
<td>Quasi-saturation effect is modeled with a modified KULL-Model [25-27]</td>
</tr>
</tbody>
</table>

4.1.2 SiC SJT Models

While there are many Si BJT models available, there are few SiC BJT models. GeneSiC Semiconductor utilizes a GP model for generic characterization of the unique SJT devices [28]. Because GeneSiC Semiconductor’s SJT device is fundamentally a [modified] BJT, this work aims to present a modified GP model specifically for the characterization of a GeneSiC Semiconductor 1700 V, 8 A junction transistor.

4.2 Model Description

The work presented is a compact model developed for the GeneSiC Semiconductor SiC 1700 V, 8 A SJT. The specific device is noted as GA08JT17-247. The model presented has been written in Verilog-A modeling language and is supported by a variety of simulators and has been implemented using a Berkeley Spice3f5-based GP model. The basic structure of the model and the equivalent circuit were adopted from a 1200 V, 6 A SiC BJT model developed at the Zhejiang University in Hangzhou, China [29] and can be seen in Fig. 4.1. Throughout this work description, the model parameters have been written in all-capital bold letters (such as BF) and
constant values and calculated variables are written with the italicized name of the variable (such as \( V_{BC} \)). Temperature scaled values are noted with a subscript \( T \) (such as \( BF_T \)).

The software used for the development of the model was a tool, developed at the University of Arkansas, titled Paragon 2. The Paragon 2 software enables the capture of equations, data, curves, variables, and expressions, all in a graphical form allowing the program to utilize models in a variety of languages [2].

![Fig. 4.1: Symbol and Equivalent Circuit for use of SJT model.](image)

**4.2.1 Static Equations**

This work addresses the second-order effects of low-current drop in \( \beta \), a thorough description of base-width modulation, and high-level injection. The proposed model equivalent circuit is shown in Fig. 4.1. The aforementioned low-current drop in \( \beta \) is modeled by the addition of two non-ideal diodes (\( I_{LE} \) and \( I_{LC} \)) to the two ideal diodes (\( I_{BF} \) and \( I_{BR} \)). The four diodes are components of the base current associated with the bias on each junction. The ideal exponential
current term, $I_{BF}$, accounts for the recombination in the inactive base region and carriers injected into the emitter. Non-ideal exponential voltage term, $I_{LE}$, is predominant at lower biases caused by recombination in the emitter junction spaced charge region; likewise for emission and recombination near the collector junction, represented by $I_{BR}$ and $I_{LC}$.

The four total diodes currents ($I_{BF}$, $I_{BR}$, $I_{LE}$, $I_{LC}$) are represented by the following equations[17-18][20]:

$$I_{BF} = \frac{I_S}{BF} \left( e^{qV_{BE}/NFkT} - 1 \right)$$  \hspace{1cm} (4.1)

$$I_{BR} = \frac{I_S}{BR} \left( e^{qV_{BC}/NRkT} - 1 \right)$$  \hspace{1cm} (4.2)

$$I_{LE} = I_{SE} \left( e^{qV_{BC}/NEkT} - 1 \right)$$  \hspace{1cm} (4.3)

$$I_{LC} = I_{SC} \left( e^{qV_{BC}/NCkT} - 1 \right)$$  \hspace{1cm} (4.4)

where $q$ is the electron charge, $k$ is Boltzmann’s constant and $T$ is the user-defined temperature parameter.

The saturation current is noted by $I_S$ and the non-ideal base-emitter and base-collector saturation currents are defined as $I_{SE}$ and $I_{SC}$, respectively. These are variations of standard diode equations with the addition of forward and reverse current emission coefficient parameters, $NF$ and $NR$, and non-ideal low-current base-emitter and base-collector emission coefficients, $NE$ and $NC$. In addition to these parameters, the diode current equations are exponentially dependent on the base-collector and base-emitter voltages $V_{BE}$ and $V_{BC}$ [16-17].
Early Effect

The Early effect is another characteristic specifically described in this model. The collector current increases with an increase in the collector-emitter voltage, and therefore also an increase in the collector-base voltage, caused by the effective shortening of the base width due to the depletion-layer expansion. The effect is described inside the model with the addition of forward Early voltage and reverse Early voltage parameters, \( V_{AF} \) and \( V_{AR} \), which can be seen within the equations for variables \( q_{1s} \) and \( q_{2s} \) as components of base charge factor, \( nqb \).

High Level Injection Effect

High level injection in the bipolar transistor occurs when the injected minority carrier concentration in the base region is larger than the doping concentration when the device is operating at high current densities. To satisfy charge neutrality, majority carrier concentration in the base increases under high-level injection conditions, enhancing the injection of holes from the base into the emitter. This reduces injection efficiency and current gain of the device. The parameters \( IKF \) and \( IKR \) are added to address high-level injection in the collector and base and represent forward- and reverse-beta high-current roll-off. [16-17].

\[
nqb = \frac{q_{1s}}{2} \ast (1 + \sqrt{1 + 4q_{2s}}) \quad (4.5)
\]

where

\[
q_{1s} = \frac{1}{\left(1 - \frac{V_{BC}}{V_{AF}} - \frac{V_{BE}}{V_{AR}}\right)} \quad (4.6)
\]

and

\[
q_{2s} = \frac{I_{BF}}{IKF} + \frac{I_{BR}}{IKR} \quad (4.7)
\]
The base and collector terminal currents are then mathematically represented as follows[17]:

\[
I_C = \frac{I_{BF} - I_{BR}}{nqb} - \frac{I_{BR}}{B_R T} - I_{LC} \quad (4.8)
\]

\[
I_B = \frac{I_{BF}}{B_F T} + I_{LE} + \frac{I_{BR}}{B_R T} + I_{LC} \quad (4.9)
\]

where \(BF_T\) and \(BR_T\) are user-defined ideal forward- and reverse-current gains (\(\beta\)).

This work also takes into account the current dependence of the base resistance. The base resistance rests between the external and internal base nodes and consists of two separate resistances noted by parameters \(RB\) and \(RBM\). \(RB\) represents the extrinsic base resistance made of the contact resistance and sheet resistance of the external base region. \(RBM\) is the intrinsic resistance of the internal base region, lying directly underneath the emitter. The total base resistance is represented in Eq. 4.10 as follows:

\[
R_B = RBM + 3(RB - RBM) \left( \frac{\tan z - z}{z \tan^2 z} \right) \quad (4.10)
\]

where

\[
z = \frac{-1 + \sqrt{1 + 144I_B / \pi^2 IRB}}{(24 / \pi^2) \sqrt{I_B / IRB}} \quad (4.11)
\]

and \(IRB\) is the current where the base resistance halfway to its minimum value.

4.2.2 Quasi-Saturation Model

The quasi-saturation effect is the gradual transition between the saturation region and the forward active region of a bipolar transistor. In this model, the quasi-saturation effects are accounted for by describing the collector resistance as shown in Eq. 4.12 [23]. The variable \(V_{BX}\) represents the voltage flowing from internal base node to the external collector node and the value of \(\frac{4ni^2}{NEPI^2}\) is commonly noted as gamma \((\gamma_{epi})\), where \(ni\) is the intrinsic carrier
concentration and \textbf{NEPI} is the epitaxial impurity concentration, and \textbf{RCO} is the zero bias collector series resistance.

\[
R_c = \frac{\text{RCO}}{\frac{1}{2} + \frac{1}{4} \sqrt{1 + \frac{4ni^2}{\text{NEPI}^2} \exp(qV_{BC}/kT)} + \frac{1}{4} \sqrt{1 + \frac{4ni^2}{\text{NEPI}^2} \exp(qV_{BX}/kT)}}
\]  

(4.12)

The quasi-saturation model is based on a model created by G.M. Kull and L.W. Nagel in 1985 [22]. The quasi-saturation effect is modeled by the epitaxial current source, \(I_{\text{epi}}\), as seen in Fig. 4.1 and is described by the following equation:

\[
I_{\text{epi}} = \frac{F_i - F_x - \ln \left( \frac{1 + F_i}{1 + F_x} \right) + \frac{q(V_{BC} - V_{BX})}{\text{EPXCO} k T}}{\text{EPXCO} k T \left( \frac{|V_{BC} - V_{BX}|}{V_O} \right)}
\]  

(4.13)

where \(F_i\) and \(F_x\) are variables described as follows:

\[
F_i = \left[ 1 + \gamma_{\text{epi}} \frac{e^{qV_{BC}/\text{EPXCO} k T}}{1 + \gamma_{\text{epi}} e^{qV_{BC}/\text{EPXCO} k T}} \right]^{1/2}
\]  

(4.14)

\[
F_x = \left[ 1 + \gamma_{\text{epi}} \frac{e^{qV_{BX}/\text{EPXCO} k T}}{1 + \gamma_{\text{epi}} e^{qV_{BX}/\text{EPXCO} k T}} \right]^{1/2}
\]  

(4.15)

In Eq. 4.13 \text{EPXCO} notes the epitaxial region emission coefficient and \(R_c\) is the series resistance adopted from [23], shown in Eq. 4.12, and \(V_O\) is the carrier velocity saturation voltage [16].

\textbf{4.2.3 Dynamic Equations}

Two depletion capacitors can be used to model the incremental fixed charges stored in the depletion regions of the bipolar transistor for changes in the associated junction voltages. Each junction capacitance is a nonlinear function of change in voltage across its respective junction. Because both the base-emitter and base-collector junctions are not forward biased heavily in normal condition, the capacitance model proposed in [20] and used for this work neglects the capacitance due to diffusion capacitances. Therefore, the junction capacitances (\(C_{BE}\) and \(C_{BX}\)) and respective charges (\(Q_{BE}\) and \(Q_{BX}\)) are represented as follows [20]:
\[ Q_{BE} = CJE \int_0^{V_{BE}} \left( 1 - \frac{V}{V_{JE}} \right)^{-ME} dV \]  

\[ C_{BE} = \frac{CJE}{\left(1 - \frac{V_{BE}}{V_{JE}}\right)^{ME}} \]  

\[ Q_{BX} = CJC(1 - X_{JC}) \int_0^{V_{PBX}} \left( 1 - \frac{V}{V_{JC}} \right)^{-MC} dV \]  

\[ C_{BX} = \frac{CJC(1 - X_{JC})}{\left(1 - \frac{V_{PBX}}{V_{JC}}\right)^{MC}} \]  

for \( V_{BE} < FC \times V_{JE} \) and \( V_{BX} < FC \times V_{JC} \), and:

\[ Q_{BE} = CJE \cdot F_1 + \frac{CJE}{F_2} \int_{FC \times V_{JE}}^{V_{BE}} \left( F_3 + \frac{ME \cdot V}{V_{JE}} \right) dV \]  

\[ C_{BE} = \frac{CJE}{F_2} \left( F_3 + \frac{ME \cdot V_{BE}}{V_{JE}} \right) \]  

\[ Q_{BX} = CJC(1 - X_{JC}) \cdot F_1 + \frac{CJC(1 - X_{JC})}{F_2} \int_{FC \times V_{JC}}^{V_{PBX}} \left( F_3 + \frac{MC \cdot V}{V_{JC}} \right) dV \]  

\[ C_{BX} = \frac{CJC(1 - X_{JC})}{F_2} \left( F_3 + \frac{MC \cdot V_{PBX}}{V_{JC}} \right) \]  

for \( V_{BE} \geq FC \times V_{JE} \) and \( V_{BX} \geq FC \times V_{JC} \), where:

\[ F_1 = \frac{V_{JE}}{1-ME} \left[ 1 - (1-FC)^{1-ME} \right] \]  

\[ F_2 = (1-FC)^{1+ME} \]  

\[ F_3 = 1 - FC(1 + ME) \]  

for the base-emitter junction, and:

\[ F_1 = \frac{V_{JC}}{1-MC} \left[ 1 - (1-FC)^{1-MC} \right] \]  

\[ F_2 = (1-FC)^{1+MC} \]  

\[ F_3 = 1 - FC(1 + MC) \]  

for the base-collector junction.
CJE and CJC represent the values of the zero-biased capacitance parameters at the base-emitter and base-collector junctions. The built-in potential parameters are noted by VJE and VJC and the pn grading factor parameters ME and MC. Parameter FC is the coefficient for forward-bias depletion capacitance used to compute the voltage in the forward-biased region, FC × VJE and FC × VJC, respectively, and is valued between zero and one. An approximation of the distributed resistance and capacitance at the base collector junction is addressed in this model with the capacitance between the internal base and external collector (CBX). Parameter XCJC specifies the ratio between the separation of junction capacitance at the base-collector junction and ranges between zero and one [17].

4.3 Temperature Scaling

Initial data for the model is assumed to have been taken at approximately 25 °C. However, the model allows for users to view device behavior across a range of temperatures. This work simulates device behavior from 25 °C to 175 °C, adjusting the simulation temperature by changing the value of parameter T.

In order to reflect changes in temperature, some device parameter and variable equations are modified. These parameters, variables, and their temperature dependent equations can be seen in Table 4.3. In the following equations, T1 is the default nominal temperature, 25 °C, and T2 represents the newly user-specified simulation temperature created by changing parameter T.
Table 4.3: Temperature-scaled parameters and variables with respective equations.

<table>
<thead>
<tr>
<th>Parameter/Variable</th>
<th>Temperature-Scaled Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation Current, IS</td>
<td>$IS_T = IS(T_1) \left( \frac{T_2}{T_1} \right)^{XTI} \exp \left[ \frac{q \cdot EG}{k \cdot T_2} \left( 1 - \frac{T_2}{T_1} \right) \right]$</td>
</tr>
<tr>
<td></td>
<td>where parameter XTI is the saturation current temperature exponent, usually at a value of 3.0</td>
</tr>
<tr>
<td>Energy Gap, EG</td>
<td>$EG_T = EG - \frac{(7.02 \times 10^{-4})T_2^2}{1300 + T_2^2}$</td>
</tr>
<tr>
<td>Forward and Reverse Beta, BF and BR</td>
<td>$BF_T = BF \left( \frac{T_1}{T_2} \right)^{XTB}$ $BR_T = BR \left( \frac{T_1}{T_2} \right)^{XTB}$</td>
</tr>
<tr>
<td></td>
<td>where parameter XTB is the forward and reverse beta temperature coefficient</td>
</tr>
<tr>
<td>Base-Emitter and Base-Collector Leakage Saturation Current, ISE and ISC</td>
<td>$ISE_T = ISE \left( \frac{T_2}{T_1} \right)^{-XTB} \left[ \frac{IS_T}{IS} \right]^{1/NE}$ $ISC_T = ISC \left( \frac{T_2}{T_1} \right)^{-XTB} \left[ \frac{IS_T}{IS} \right]^{1/NC}$</td>
</tr>
<tr>
<td>Base-Emitter and Base-Collector Built In Potential, VJE and VJC</td>
<td>$VJE_T = \frac{T_2}{T_1} VJE - 2 \frac{k \cdot T_2}{q} \ln \left( \frac{T_2}{T_1} \right)^{1.5} - \left[ \frac{T_2}{T_1} EG - EG_T \right]$ $VJC_T = \frac{T_2}{T_1} VJC - 2 \frac{k \cdot T_2}{q} \ln \left( \frac{T_2}{T_1} \right)^{1.5} - \left[ \frac{T_2}{T_1} EG - EG_T \right]$</td>
</tr>
<tr>
<td>Base-Emitter and Base-Collector Zero-Bias Capacitance, CJE and CJC</td>
<td>$CJE_T = CJE \left{ 1 + ME \left[ 400 \times 10^{-4}(T_2 - T_1) - \frac{VJE_T - VJE}{VJE} \right] \right}$ $CJC_T = CJC \left{ 1 + MC \left[ 400 \times 10^{-4}(T_2 - T_1) - \frac{VJC_T - VJC}{VJC} \right] \right}$</td>
</tr>
</tbody>
</table>
Table 4.4: Temperature-scaled parameters and variables with respective equations.

<table>
<thead>
<tr>
<th>Parameter/Variable</th>
<th>Temperature-Scaled Equation</th>
</tr>
</thead>
</table>
| Voltage in Forward-Biased Regions, $FCPE$ and $FCPC$ | $FCPE_T = FC \times VJE = \frac{FCPE VJE_T}{VJE}$  
$FCPC_T = FC \times VJC = \frac{FCPE VJC_T}{VJC}$ |
| Variable $F_1$ For Capacitance Calculation      | $F_{1_T} = F_1 \frac{VJE_T}{VJE}$  
$F_{1_T} = F_1 \frac{VJC_T}{VJC}$ |
| Quasi-Saturation Collector Resistance, $R_C$    | $R_{C_T} = R_C \left(\frac{T_2}{T_1}\right)^{BEX}$  
where $BEX$ is the temperature exponent for the quasi-saturation collector resistance |
| Carrier Velocity Saturation Voltage, $VO$       | $V_{O_T} = VO \left(\frac{T_2}{T_1}\right)^{BEXV}$  
where $BEXV$ is the temperature exponent for the carrier velocity saturation voltage |
| Variable $\gamma_{epi}$ Used For Collector Resistance Calculation | $\gamma_{epi_T} = \gamma_{epi} \left(\frac{T_2}{T_1}\right)^{XTI} \exp \left[-\frac{q EG}{k T_2} \left(1 - \frac{T_2}{T_1}\right)\right]$ |
CHAPTER 5: MODEL SIMULATION AND VERIFICATION

This chapter provides the simulated and verified results of the GeneSiC 1.7 kV, 8 A SiC SJT from the model presented in this work. Model verification consists of validating the model with real device data. The model must be mathematically accurate and properly formulated for accurate simulation results and for convergence under different bias conditions. Verification also includes affirmation of model convergence and satisfactory simulation times.

Evaluating Model Performance

Selected parameter values for the GA08JT17-247 1.7 kV, 8 A SiC power super junction transistors are available on the GeneSiC Semiconductor website [28]; however, these parameter values are for standard bipolar models. Super junction device data measurements were taken from the GA08JT17-247 datasheet, as well as C-V and switching measurements provided from GeneSiC, for the evaluation of model performance through comparison of simulated results to measured data. For model validation, simulated results should be reasonably accurate against measured data. Simulation and parameter extraction for the output characteristics and C-V curves were performed in IC-CAP, an industry standard modeling tool. Switching characteristics were simulated in Paragon 2 as IC-CAP does not support switching analysis.

5.1 Parameter Extraction and Simulation Analysis

5.1.1 Parameter Extraction

The presented model was developed in a manner that allows for parameter extraction using available device datasheets. There are nominal parameters and temperature-dependent parameters that affect the scaling of the nominal parameters. Parameter extraction often consists
of three main steps: taking physical device measurements (or digitizing data from a datasheet),
extractions of parameters at room temperature, and then extraction of temperature scaled
parameters. The parameter extraction strategy for this work was followed by using data from the
GA08JT17-247 device datasheet. Data presented in datasheets are often mean-valued data sets
and variation in data from one device to another is expected.

It is generally easier to extract model parameters in groups; for example, extracting DC
parameters, ohmic parasitics, and C-V parameters. Each parameter group then becomes the
initial condition for each extraction step thereafter.

Though IC-CAP includes a built-in parameter extraction and optimization sequence, the
presented work extracted parameters manually starting with initial values identified from the
GeneSiC GA08JT17-247 datasheet seen in Table 5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Definition</th>
<th>GeneSiC Datasheet Initial Value (25 °C)</th>
<th>Extracted Parameter Values</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IS</strong></td>
<td>Transport saturation current</td>
<td>3.73E-47 (A)</td>
<td>3.49 E-47</td>
</tr>
<tr>
<td><strong>BF</strong></td>
<td>Ideal maximum forward beta</td>
<td>63</td>
<td>63</td>
</tr>
<tr>
<td><strong>BR</strong></td>
<td>Ideal maximum reverse beta</td>
<td>0.55</td>
<td>0.552</td>
</tr>
<tr>
<td><strong>NR</strong></td>
<td>Reverse current emission coefficient</td>
<td>-</td>
<td>1.048</td>
</tr>
<tr>
<td><strong>NF</strong></td>
<td>Forward current emission coefficient</td>
<td>1.0</td>
<td>1.095</td>
</tr>
<tr>
<td><strong>IKF</strong></td>
<td>Forward-beta high-current roll-off “knee” current</td>
<td>200.0 (A)</td>
<td>250.0</td>
</tr>
<tr>
<td><strong>IKR</strong></td>
<td>Reverse-beta high-current roll-off “knee” current</td>
<td>- (A)</td>
<td>100</td>
</tr>
<tr>
<td>Parameter</td>
<td>Definition</td>
<td>GeneSiC Datasheet Initial Value (25 °C)</td>
<td>Extracted Parameter Values</td>
</tr>
<tr>
<td>-----------</td>
<td>----------------------------------------------------------</td>
<td>----------------------------------------</td>
<td>---------------------------</td>
</tr>
<tr>
<td>ISE</td>
<td>Base-emitter leakage saturation current</td>
<td>5.50E-27 (A)</td>
<td></td>
</tr>
<tr>
<td>NE</td>
<td>Base-emitter leakage emission coefficient</td>
<td>2.201</td>
<td></td>
</tr>
<tr>
<td>ISC</td>
<td>Base-collector leakage saturation current</td>
<td>- (A)</td>
<td></td>
</tr>
<tr>
<td>NC</td>
<td>Base-collector leakage emission coefficient</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>VAR</td>
<td>Reverse Early voltage</td>
<td>- (V)</td>
<td></td>
</tr>
<tr>
<td>VAF</td>
<td>Forward Early voltage</td>
<td>- (V)</td>
<td></td>
</tr>
<tr>
<td>RCO</td>
<td>Zero-bias collector series resistance</td>
<td>- (ohm)</td>
<td></td>
</tr>
<tr>
<td>NEPI</td>
<td>Epitaxial impurity concentration</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>VO</td>
<td>Carrier velocity saturation voltage</td>
<td>- (V)</td>
<td></td>
</tr>
<tr>
<td>EPXCO</td>
<td>Epitaxial region emission coefficient</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>BEX</td>
<td>Temperature exponent for RCO</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>BEXV</td>
<td>Temperature exponent for VO</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>RB</td>
<td>Zero-bias (maximum) base resistance</td>
<td>6.0 (ohm)</td>
<td></td>
</tr>
<tr>
<td>RBM</td>
<td>Minimum base resistance</td>
<td>0.9 (ohm)</td>
<td></td>
</tr>
<tr>
<td>IRB</td>
<td>Current where base resistance equals (RB+RBM)/2</td>
<td>1.0E-4 (A)</td>
<td></td>
</tr>
<tr>
<td>CJE</td>
<td>Base-emitter zero-bias capacitance</td>
<td>8.23E-10 (F)</td>
<td></td>
</tr>
<tr>
<td>VJE</td>
<td>Base-emitter built-in potential</td>
<td>2.945 (V)</td>
<td></td>
</tr>
<tr>
<td>MJE</td>
<td>Base-emitter grading factor</td>
<td>0.498</td>
<td></td>
</tr>
<tr>
<td>FC</td>
<td>Forward-bias depletion capacitor coefficient</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

Table 5.1: Parameter values for GA08JT17-247 device model, cont’d.
Table 5.1: Parameter values for GA08JT17-247 device model, cont’d.

| Parameter | Definition | GeneSiC Datasheet Initial Value (25 °C) | Extracted Parameter Values
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CJC</td>
<td>Base-collector zero-bias capacitance</td>
<td>2.77E-10 (F)</td>
<td>2.77 E-10</td>
</tr>
<tr>
<td>VJC</td>
<td>Base-collector built-in potential</td>
<td>3.023 (V)</td>
<td>3.02</td>
</tr>
<tr>
<td>MJC</td>
<td>Base-collector grading factor</td>
<td>0.461</td>
<td>0.461</td>
</tr>
<tr>
<td>XCJC</td>
<td>Fraction of base-collector capacitor connected to internal RB</td>
<td>0.0</td>
<td>0.0</td>
</tr>
<tr>
<td>XTB</td>
<td>Forward and reverse beta temperature exponent</td>
<td>-0.7</td>
<td>-0.7</td>
</tr>
<tr>
<td>EG</td>
<td>Bandgap voltage</td>
<td>3.26</td>
<td>3.26</td>
</tr>
<tr>
<td>XTI</td>
<td>Temperature exponent for IS</td>
<td>3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>TEMP</td>
<td>User defined measurement temperature</td>
<td>- (C)</td>
<td>(300.15)</td>
</tr>
</tbody>
</table>

Model parameter extractions are conducted under the concept that parameter sets uniquely simulate device performance under certain specified conditions. DC bias extractions and junction capacitance characteristics are basically independent of each other. Switching simulation performance is highly dependent on junction capacitance simulation and series resistance extractions are dependent on DC and capacitance parameters. Table 6 describes the parameter extraction sequence. The device setup, related extracted parameters, and phenomena modeled or areas affected are also noted.
Table 5.2: Device setup, related extracted parameters, and phenomena modeled or areas affected for parameter extraction sequence.

<table>
<thead>
<tr>
<th>Sequence</th>
<th>Characteristic</th>
<th>Measurement</th>
<th>Parameter</th>
<th>Phenomenon Modeled or Area Affected</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DC Large Signal</td>
<td>$I_C \text{ vs } V_{CE}$</td>
<td>IS</td>
<td>Hard saturation region of output curves</td>
</tr>
<tr>
<td></td>
<td>Forward Bias</td>
<td></td>
<td>BF</td>
<td>Low level non-ideal currents/ spacing between output family of curves</td>
</tr>
<tr>
<td></td>
<td>DC Large Signal</td>
<td>$I_B \text{ vs } V_{BE}$</td>
<td>IKF</td>
<td>Variation in forward beta at high collector currents/ “knee” of curve in Forward Gummel plots</td>
</tr>
<tr>
<td></td>
<td>Reverse Bias</td>
<td></td>
<td>NF</td>
<td>Deviation of emitter base diode from ideal</td>
</tr>
<tr>
<td></td>
<td>DC Large Signal</td>
<td>$I_C \text{ vs } V_{CE}$</td>
<td>ISE</td>
<td>Variation of forward beta at low base currents</td>
</tr>
<tr>
<td></td>
<td>Reverse Bias</td>
<td></td>
<td>NE</td>
<td>Variation of forward beta at low base currents</td>
</tr>
<tr>
<td></td>
<td>DC Large Signal</td>
<td>$I_C \text{ vs } V_{CE}$</td>
<td>VAF</td>
<td>Forward Early voltage/ base collector bias on forward beta and saturation current</td>
</tr>
<tr>
<td></td>
<td>Reverse Bias</td>
<td></td>
<td>BR</td>
<td>Low level non-ideal currents/Saturation and reverse regions</td>
</tr>
<tr>
<td></td>
<td>DC Large Signal</td>
<td>$I_B \text{ vs } V_{BE}$</td>
<td>IKR</td>
<td>Variation in reverse beta at high emitter currents/ “knee” current at reverse beta high-current roll-off</td>
</tr>
<tr>
<td></td>
<td>Reverse Bias</td>
<td></td>
<td>NR</td>
<td>Deviation of base collector diode from ideal</td>
</tr>
<tr>
<td></td>
<td>DC Large Signal</td>
<td>$I_C \text{ vs } V_{CE}$</td>
<td>ISC</td>
<td>Variation in reverse beta at low base currents/models base current at low base-collector voltage</td>
</tr>
<tr>
<td></td>
<td>Reverse Bias</td>
<td></td>
<td>NC</td>
<td>Variation in reverse beta at low base currents/models base current at low base-collector voltage</td>
</tr>
<tr>
<td></td>
<td>DC Large Signal</td>
<td>$I_C \text{ vs } V_{CE}$</td>
<td>VAR</td>
<td>Reverse Early voltage/emitter base bias on reverse beta and saturation current</td>
</tr>
</tbody>
</table>
Table 5.2: Device setup, related extracted parameters, and phenomena modeled or areas affected for parameter extraction sequence, cont’d.

<table>
<thead>
<tr>
<th>Sequence</th>
<th>Characteristic</th>
<th>Measurement</th>
<th>Parameter</th>
<th>Phenomenon Modeled or Area Affected</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>Quasi-Saturation Model</td>
<td>$I_C vs V_{CE}$</td>
<td>RCO</td>
<td>Hard and Quasi-saturation regions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>NEPI</td>
<td>Hard and Quasi-saturation regions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VO</td>
<td>Hard and Quasi-saturation regions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>EPXCO</td>
<td>Hard and Quasi-saturation regions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>BEX</td>
<td>Hard and Quasi-saturation regions</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>BEXV</td>
<td>Hard and Quasi-saturation regions</td>
</tr>
<tr>
<td>3</td>
<td>Series Resistance</td>
<td>$I_B vs V_{BE}$</td>
<td>RB</td>
<td>Parasitic resistance in base</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>RBM</td>
<td>Variation in base resistance as base current varies</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>IRB</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Junction Capacitance</td>
<td>$C_{BE} vs V_{BE}$ and $C_{BE} + C_{BC} vs V_{CE}$</td>
<td>CJE</td>
<td>Base-emitter capacitance/switching times</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VJE</td>
<td>Base-emitter capacitance variation with bias</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MJE</td>
<td>Base-emitter capacitance variation with bias</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_{BC} vs V_{CE}$ and $C_{BE} vs V_{BE}$, $C_{BE} + C_{BC} vs V_{CE}$ and $C_{BC} vs V_{GE}$</td>
<td>CJC</td>
<td>Base-collector capacitance/switching times</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VJC</td>
<td>Base-collector capacitance variation with bias</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>MJC</td>
<td>Base-collector capacitance variation with bias</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>FC</td>
<td>Provides continuity between forward and reverse biased capacitance</td>
</tr>
<tr>
<td>5</td>
<td>Temperature Effects</td>
<td>All</td>
<td>XTB</td>
<td>Variation of beta with temperature</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>EG</td>
<td>Energy gap for modeling temperature effects/temperature variation of saturation currents in collector and base-emitter and collector-base diodes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>XTI</td>
<td>Variation of saturation current with temperature</td>
</tr>
</tbody>
</table>
5.1.2 Simulation Results and Verification

For the simulated results presented in this work, corresponding data was provided from GeneSiC Semiconductor across the following conditions at room temperature:

- **Setup 1: Output characteristics (\( I_C \) vs \( V_{CE} \))**
  
  \( I_B \) is swept from 0 mA to 300 mA in steps of 100 mA
  
  \( V_{CE} \) is swept from 0 V to 5.9 V in steps of 50 mV

- **Setup 2: C-V characteristics (\( C_{BE} \) vs \( V_{BE} \)) and (\( C_{BC} \) vs \( V_{CE} \))**
  
  \( V_{BE} \) is swept from -10 V to 3.3 V in steps of 10 mV
  
  \( V_{CE} \) is swept from 0 V to 1 kV in steps of 1 V

- **Setup 3: Switching characteristics (Turn-off and Turn-on)**

  *Ideal resistive load circuit with varying user-defined added parasitics.*

  The output characteristics were simulated by application of a base current. The voltage across the collector and emitter was swept and the current at the collector terminal was measured. The reference circuit for the output characteristics is seen in Fig. 5.1a. The base-emitter C-V simulation was achieved by measuring the capacitance across the base-emitter terminals while sweeping a voltage across the base-emitter terminals. Likewise, base-collector C-V simulations were achieved by measuring the base-collector capacitance and the sum of the base-emitter and base-collector capacitances, respectively, while sweeping a voltage across the base-collector terminals. Accurate fitting of the C-V data is essential for accuracy in switching verification. The switching characteristics were captured with use of an ideal resistive load schematic noted in Fig. 5.1d. Parasitic inductances and other passives will be specific to mimic the user testbench schematic in order to introduce ringing for a more practical simulation.

  Variations of measurement conditions to account for temperature scaling are as follows:
• Setup 1: Output characteristics for 125 °C (\( I_C \) vs \( V_{CE} \))

\( I_B \) is swept from 0 mA to 1 A in steps of 200 mA

\( V_{CE} \) is swept from 0 V to 8.5 V in steps of 50 mV

• Setup 1: Output characteristics for 175 °C (\( I_C \) vs \( V_{CE} \))

\( I_B \) is swept from 0 mA to 1 A in steps of 200 mA

\( V_{CE} \) is swept from 0 V to 15 V in steps of 50 mV

• Setup 2 and 3: C-V characteristics and Switching characteristics (Turn-off and Turn-on)

Displayed negligible effects during temperature variation

Fig. 5.1: Simulation test bench circuits used for (a) output characteristics (b) base-emitter C-V (c) base-collector C-V and (d) switching simulations.
In order to verify the model, values from the GA08JT17-247 datasheet and, released technical articles, were digitized and used in comparison to simulated results [28]. The model parameters were then adjusted from their initial values to ensure optimal agreement against the digitized measured data.

**Output Characteristics**

The simulated and measured output characteristics of the SJT at 25 °C are shown in Fig. 5.2. For simulation, base currents of 0 mA, 100 mA, 200 mA, and 300 mA were applied to the base terminal, the collector-emitter terminal voltage ($V_{CE}$) was swept from 0 V to 5.9 V, and the collector current ($I_C$) was measured and plotted against $V_{CE}$ using the circuit shown in Fig. 5.1a.

![Graph showing SJT output characteristics](image)

**Fig. 5.2:** SJT output characteristics at room temperature (25 °C).
The family of curves show close agreement between the measured and simulated data. The linear region is accurately represented in both hard and quasi-saturation. Overall, the family of curves for the output characteristics at 25 °C is considered a good fit.

**C-V Characteristics**

**Base-Emitter Capacitance**

In order to verify the C-V simulation capabilities of the proposed model, measured data of the C-V characteristics was provided by GeneSiC Semiconductor and compared to simulated results. Simulation of the base-emitter C-V characteristics were obtained by applying a voltage across the base-emitter terminals, swept from -10 V to 3.3 V and measuring the capacitance across the base-emitter terminals; the simulation testbench circuit is noted in Fig. 5.1b. The results for the base-emitter C-V characteristics are given in Fig. 5.3a.

The simulated C-V curve for the base-emitter junction shows an extremely good fit when verified against the measured data. Nearly seamless simulation is noted until close to 2 V confirming simulation performance acceptance.

**Base-Collector Capacitance**

Simulation of the base-collector C-V characteristics were obtained by applying a voltage across the collector-emitter terminals, swept from 0 V to 1 kV and measuring capacitance across base-collector terminals; simulation testbench is noted in Fig. 5.1c and the results for the base-collector C-V characteristics are shown in Fig. 5.3b. An excellent fit was obtained when verified against the measured data.
Fig. 5.3: (a) Base-emitter and (b) base-collector C-V characteristics.
Switching Characteristics

Because bipolar transistors are most often used as switches, it is the switching behavior that could be considered most important to accurately model and simulate the device. The C-V characteristics of the device tend to dominate switching characterization. Because of the well-validated base-emitter and base-collector capacitance simulations, verification of the switching characteristics was done with ease.

Switching simulation was achieved by use of the simulation testbench noted in Fig. 5.1d. A resistive load circuit was utilized. The resistive load of 138 Ω was applied. The base voltage was pulsed from -5 V to 20 V for turn on, and then reversed for turn-off. A bus voltage of 1100 V was applied across the collector-emitter terminals. Rise and fall times of 14 ns and 23 ns, respectively, were applied and turn-on and turn-off delay times of 12 ns and 20 ns were applied per the GA08JT17-247 datasheet. Original results were deemed too ideal and parasitics were added to better mimic the testbench parasitics for a less-ideal switching simulation. The turn-on and turn-off switching characteristics verified against measured data provided by GeneSiC Semiconductor are seen in Fig. 5.4 and Fig. 5.5.

Both turn-on and turn-off results show excellent agreement with provided data. The model shows the same overshoot that the turn-on data shows and the undershoot to almost -2 A as seen in the turn-off data. Slight discrepancies in switching times are likely due to testbench conditions. While the resistive load value and rise and delay times were available on the GA08JT17-247 datasheet, the parasitics added to the resistive load simulation testbench had to be approximated to accommodate the unique oscillations of the provided data. It is likely that these factors play a part in any discrepancies; though, overall, the results are deemed a good fit.
Fig. 5.4: SJT turn-on switching (a) current characteristics and (b) voltage characteristics at room temperature.
Fig. 5.5: SJT turn-off switching (a) current characteristics and (b) voltage characteristics at room temperature.
5.1.3 Temperature Scaled Results

Initial input data for simulators assumes that device measurements were taken at nominal temperature of 25 °C. However, it is essential for effective modeling and circuit design for device models to accurately predict device behavior across elevated temperatures. The device simulations for 125 °C and 175 °C are discussed in the following sections.

Output Characteristics

Output characteristics for elevated temperatures were simulated using the same testbench for the room temperature simulation as seen in Fig. 5.1a. TEMP was appropriately changed within the model and model parameters were then extracted for optimal results across the risen temperatures.

The simulated output characteristics for 125 °C were obtained by applying a base current from 0 A to 1 A in steps of 200 mA and sweeping the collector-emitter voltage from 0 V to 8.5 V. Similarly, the simulated output characteristics for 175 °C were obtained by applying a base current from 0 A to 1 A in steps of 200 mA and sweeping the collector-emitter voltage from 0 to 15 V. Good agreement is seen again between simulated and measured data for output characteristics at both 125 °C and 175 °C. Overall, the verified results shown in Figs. 5.6a and 5.6b are deemed acceptable.
Fig. 5.6: Output Characteristics for (a) 125 °C and (b) 175 °C.
5.2.2 C-V and Switching Characteristics

Junction capacitance has negligible variation across temperature, therefore the C-V data and simulation for 125 °C and 175 °C are the same as 25 °C. Likewise, turn-on and turn-off switching measured data, provided by GeneSiC Semiconductor, showed negligible variation across temperature, therefore switching simulation verification does not change from 25 °C, 125 °C, or 175 °C. Evidence of such can be seen by comparing measured switching data provided by GeneSiC at 25 °C and 175 °C as shown in Figs. 5.7 through 5.14 and through verification of the switching current and voltage characteristics at 175 °C. The switching testbench parasitics were not changed in value at all from 25 °C to 175 °C and slight divergence in simulation versus measured data is seen at the elevated temperature. The increase of 0.8 A in the collector current noted in the turn-on and turn-off current characteristics could be rectified by parasitic adjustments in the testbench. The oscillations noted in the switching characteristics are likely due to a mixture of phenomena occurring within the structure of the device, circuit parasitics, and minority lifetimes.
Fig. 5.7: Turn-on current characteristics temperature comparison for 125 °C and 175 °C.

Fig. 5.8: Turn-on current characteristics simulated at 175 °C.
Fig. 5.9: Turn-on voltage characteristics temperature comparison of 125 °C and 175 °C.

Fig. 5.10: Turn-on voltage characteristics simulated at 175 °C.
Fig. 5.11: Turn-off current characteristics temperature comparisons for 125 °C and 175 °C.

Fig. 5.12: Turn-off current characteristics simulated at 175 °C.
Fig. 5.13: Turn-off voltage characteristics comparison for 125 °C and 175 °C.

Fig. 5.14: Turn-off voltage characteristics simulated at 175 °C.
CHAPTER 6: SUMMARY AND CONCLUSIONS

The work presented in this thesis aimed to develop the first temperature-scaled compact model for use of a 1.7 kV, 8 A GeneSic SiC SJT. The benefits of SiC as a device material were discussed by describing the material and electrical advantages over its Si counterpart. A model was developed using a GP based model represented in [23] and with a Verilog-A implementation derived from the Berkeley Spice3f5 implementation. The model was then validated and verified in IC-CAP and Paragon2 for the output, C-V, and switching characteristics.

SiC SJTs offer the ability to reduce the size and increase efficiency of power electronics applications. Use in micro-grids, electric vehicles, solar inverters and many more applications will be innovated by use of SJTs operating at high voltages, frequencies, and temperatures with low on-resistances. These SJTs aim to be competitors to SiC MOSFETS. GeneSiC has optimally designed these devices with characteristics similar to those of SiC MOSFETs including fast switching capabilities, a square reverse-biased safe operating area, as well as temperature-independent transient energy losses and switching times. A main distinguishing factor of these devices is that they are capable of being driven by commercially available gate drivers, unlike other SiC switches.

With advances in SiC technology and the rise of newly engineered bipolar transistors as MOSFET competitors, having accurate compact models is a tremendous asset. This work successfully laid a solid foundation for modeling and simulation of GeneSiC’s line of SiC Junction Transistors.

Future Work

Though this work has laid a solid foundation for modeling of GeneSiC’s SJTs, further work could be done to improve model performance for this and other bipolar transistors. The
results from the model compared to real world data were effective at capturing the ideal transistor characteristics. However, for added efficiency and accuracy, the base of the model could be converted from the SGP model to a more advanced bipolar model. The Mextram model would serve as a reasonable alternative to the SGP model once modified for super-junction applications.
REFERENCES


[27] F. Sischka, “The VBIC Model.”


APPENDIX A: DESCRIPTION OF RESEARCH FOR POPULAR PUBLICATION

Transistors are electronic devices generally used to perform as switches in electronic circuits. GeneSiC Semiconductor has, in recent years, developed and released a 1700 V class of silicon-carbide (SiC) “Super” Junction Transistors (SJTs). GeneSiC Semiconductors aims to increase power conversion efficiency and reduce the size, weight, volume of commercial power electronics through incorporation of these SiC SJTs.

SiC SJTs offer the ability to reduce the size and increase efficiency of power electronics applications. Use in micro-grids, electric vehicles, solar inverters and many more applications will be innovated by use of SJTs operating at high voltages, frequencies, and temperatures while maintaining low on-resistances.

The first-ever 1.7 kV, 8 A SiC physics-based circuit model is developed for behavior prediction, modeling and simulation of the GeneSiC “Super” Junction Transistor. The model is designed to predict and simulate the SJT behavior under performance conditions defined by the user. Model accuracy is paramount in successfully describing the device behavior.

Transistor modeling and simulation for device performance is not a new concept. Therefore, an already-existing model served as a base for this work. The Gummel-Poon transistor model was used and a modified quasi-saturation model was added to accurately describe the SJT behavior.

The model provided accurate and acceptable simulations of the GeneSiC 1.7 kV 8 A SJT. With advances in SiC technology and the rise of newly engineered bipolar transistors, having accurate compact models is a tremendous asset leading to improved manufacturing efficiency and productivity.
APPENDIX B: EXECUTIVE SUMMARY OF NEWLY CREATED INTELLECTUAL PROPERTY

There is no newly created intellectual property within this work.
APPENDIX C: POTENTIAL PATENT AND COMMERCIALIZATION ASPECTS OF LISTED INTELLECTUAL PROPERTY ITEMS

No potential patents or commercialization opportunities were created with this work.
APPENDIX D: BROADER IMPACT OF RESEARCH

D.1 Applicability of Research Methods to Other Problems

SiC is deemed advantageous for use in power electronics applications. SiC provides a wide band gap, high critical electric field, and high thermal conductivity in comparison to Si, providing opportune circumstance for improved and more efficient power device performance. SiC BJTs provide more stable operation across a wider temperature range than Si counterparts.

Providing accurate device models maintains pivotal in circuit design and electrical efficiency. By producing well-developed models, SiC devices are able to be utilized in circuits that improve and impact overall electricity consumption worldwide.

D.2 Impact of Research Results on U.S. and Global Society

Bipolar transistors are the device of choice for many analog circuits and in discrete circuit design. SJTs increase conversion efficiency and reduce the size, weight, and volume of power electronics. Higher switching frequencies these devices are able to achieve allow for cost savings on a systems level as well, which impacts the economy. These devices affect a plethora of applications including DC micro-grids, telecom and networking power supplies, and industrial motor control systems.

D.3 Impact of Research Results on Environment

The availability of fully-functioning and accurate device models allows for efficiency-sustaining manufacturing. Solar inverters, wind power systems, and electric vehicles, and other measures of renewable energy applications benefit from these devices and their models.
APPENDIX E: MICROSOFT PROJECT FOR MS MICROEP DEGREE
Appendix F: IDENTIFICATION OF ALL SOFTWARE USED IN RESEARCH AND THESIS GENERATION

Computer #1:
  Model Number: Dell Optiplex 980
  Serial Number: HJNDPP1
  Location: CSRCW47
  Owner: Dr. Alan Mantooth

Software #1:
  Name: Paragon2
  Created by: University of Arkansas

Software #2:
  Name: IC-CAP
  Purchased by: Dr. H. Alan Mantooth

Software #3:
  Name: Adobe Acrobat Professional 10.0
  Purchased by: University of Arkansas Site License

Software #4:
  Name: Microsoft Office 2010
  Purchased by: University of Arkansas Site License

Computer #2:
  Model Number: Acer Aspire Z3-605 Windows 10 Home Version 1511
  Serial Number: 00326-10000-00000-AA625
  Location: Personal residence
  Owner: Brooks

Software #5
  Name: Microsoft Office 2010
  Purchased by: Brooks

Computer #3

Software #6
  Name: Microsoft Office 2010
  Purchased by: Brooks