12-2014

A Phase-Locked Loop in High-Temperature Silicon Carbide and General Design Methods for Silicon Carbide Integrated Circuits

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A dissertation submitted in partial fulfillment
of the requirements for the degree of
Doctor of Philosophy in Electrical Engineering

by

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December 2014
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ABSTRACT

Silicon carbide (SiC) has long been considered for integrated circuits (ICs). It offers several advantages, including wider temperature range, larger critical electric field, and greater radiation immunity with respect to Silicon (Si). At the same time, it suffers from challenges in fabrication consistency and lower transconductance which the designer must overcome. One of the recent SiC IC processes developed is the Raytheon High-Temperature Silicon Carbide (HTSiC) complementary MOSFET process. This process is one of the first to offer P channel MOSFETs and, as a result, a greater variety of circuits can be built in it.

The behavior of SiC MOSFETs has some important differences with Si MOSFETs. Models such as the Shichman-Hodges, EKV, and Short-channel models have been developed over time to address the important behaviors observed in Si MOSFETs, but none of these captures all of the important effects in SiC. In this work, an improved Shichman-Hodges model that incorporates the body-charge effect, mobility reduction, and a nonlinear channel modulation is developed for SiC CMOS IC devices. The importance of considering these effects is demonstrated with a simple design exercise.

This dissertation also describes the design and testing of the first-ever phase-locked loop (PLL) in SiC. This PLL is suitable for use as a general circuit building block such as in a clock recovery circuit. The fabricated circuit operates between 600 kHz and 1.5 MHz, and at temperatures up to 300 ℃. Testing results also show that output jitter and locking are negatively impacted at higher temperatures, and an improved design is proposed and analyzed.

ACKNOWLEDGEMENTS

Every doctoral student is product of the environment in which he or she works. The University of Arkansas Mixed-Signal CAD lab is very much a community and a team. I would like to thank Dr. Alan Mantooth for his foresight and leadership in creating and growing this program and for finding the unique individuals and research opportunities that exist here. I would also like to thank the students who were both co-workers and comrades-in-arms: Caleb Gutshall, Kacie Woodmansee, Chris Lee, Mihir Mudholkar, Javier Valle-Mayorga, Michael Glover, Matt Barlow, Nick Chiolino, Ashfaqur Rahman, Andrew Taylor, Dillon Kaiser and others.

Through research partnerships with industry, I have also had the opportunity to learn a great deal from several individuals outside the UA: Ty McNutt at APEI, Nance Ericson at ORNL, Adam Barkley and Sei-Hyung Ryu at Cree, and Ewan Ramsey and Robert A. R. Young at Raytheon.

Finally, I would like to thank Dr. Matt Francis and Jim Holmes at Ozark Integrated Circuits. They have been both mentors and friends during my academic career.

Perhaps more important than the academic support a doctoral student receives is the personal support. For that I can never give enough thanks to my sister, Dr. Stephanie Shepherd, and my wife, Laura-Rose Russell Shepherd.

DEDICATION

This dissertation is dedicated to my daughter, River April Shepherd, who will always be my greatest contribution to the world.

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TABLE OF ACRONYMS

APEI	Arkansas Power Electronics International
BJT	Bipolar Junction Transistor
BSIM	Berkley Short-Channel IGFET Model
CAD	Computer-Aided Design
CMOS	Complementary Metal-Oxide-Semiconductor
DC	Direct Current
EKV	Enz, Krummenacher, and Vittoz
ESR	Equivalent Series Resistance
FET	Field-Effect Transistor
FOM	Figure of Merit
HTSiC	High-Temperature Silicon Carbide
IC	Integrated Circuit
IGFET	Insulated-Gate Field-Effect-Transistor
JFET	Junction Field-Effect Transistor
LET	Linear Energy Transfer
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NFET	N-channel (MOS) Field-Effect Transistor
NMOS	N-channel Metal-Oxide-Semiconductor (FET)
NPN	N-type/P-type/N-type
NRZ	Non Return-to-Zero
ORNL	Oak Ridge National Laboratory
PD	Phase Detector
PFD	Phase-Frequency Detector

PFET	P-channel (MOS) Field-Effect Transistor
PLL	Phase-Locked Loop
PMOS	P-channel Metal-Oxide-Semiconductor (FET)
RC	Resistor-Capacitor
SEE	Single-Event Effects
SPICE	Simulation Program with Integrated Circuit Emphasis
SR	Set-Reset
TID	Total Ionizing Dose
UA	University of Arkansas
VCO	Voltage-Controlled Oscillator

CHAPTER 1 – INTRODUCTION

Silicon carbide (SiC) has a long history as a semiconducting material, but has mostly been eclipsed by silicon Each decade, new research has pushed the state of the art in SiC materials and devices further, but these advances also reveal new challenges in material processing, device design, consistency, and even our understanding of the device physics [1]–[6]. With the commercial availability of discrete SiC power devices emerging over the last seven years, SiC integrated circuits finally appear close to delivering on the long held promise of commercial applicability. Significant work has recently taken place at the University of Arkansas in the field of SiC complementary metal oxide semiconductor (CMOS) integrated circuits (ICs) [7]–[9]. The work in this dissertation reflects another step in the development of SiC IC design processes, design-tools and methods, and is the first ever implementation of a phase-locked loop (PLL) in SiC.

1.1 Applications of Phase-Locked Loops

Phase-locked loops are a class of circuits that appear in a multitude of systems. They may be completely analog, completely software, mixed-signal, or even some combination of these [10]. In work to develop a class of SiC integrated circuits for power electronic systems, a PLL was developed as a fundamental building block [11].

Phase-locked loops have several applications useful for power electronics. A PLL can be used as a motor drive as shown in Fig. 1.1a, encompassing the power electronics, load, and control circuitry.

PLLs can also be used to synchronize a receiver with an incoming data stream. Transmission of serial data without a clock is particularly beneficial in power electronics where voltage isolation may be necessary since it results in fewer isolation components as seen in Fig. 1.1(b). PLLs can also be used to generate control signals via phase or frequency modulation [12].

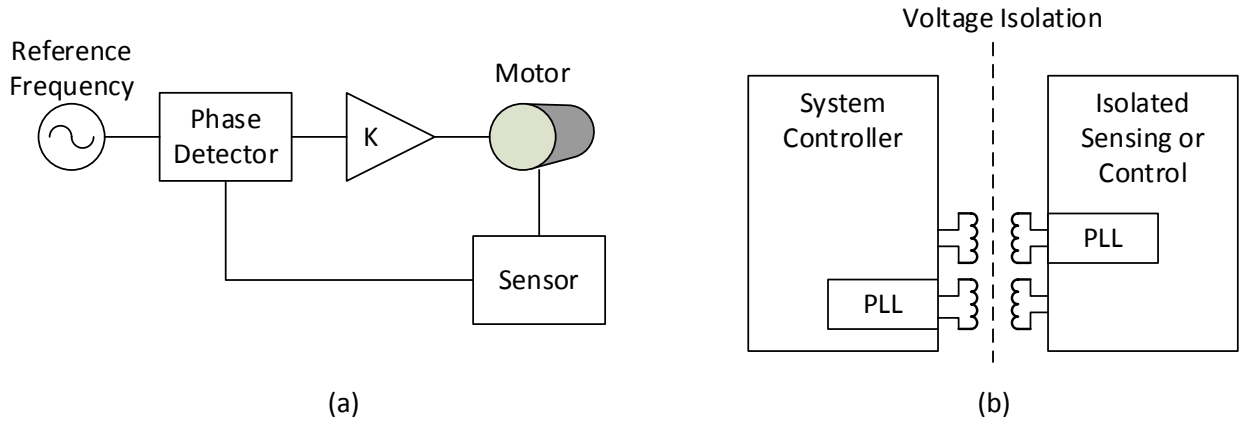


Fig. 1.1. (a) A PLL motor speed control system and (b) PLLs used in a serial data communication scheme

Although there are many applications for a PLL with additional or modified internal components, the PLL to be described in this dissertation can be applied in the system described in Fig. 1.1(b) without modification. Fig. 1.2 shows a block diagram of a receiving element as shown in Fig. 1.1 (b). The coil drives a comparator which generates a square-wave output. The square-wave output can be duty-cycle encoded, with the positive transitions as the clock edges, and the duty cycle less than or greater than 50% indicating a digital 0 or 1, respectively. The PLL generates a nearly 50% duty cycle clock signal from the input, and then a D flip-flop can generate a clocked logic signal from the duty-cycle encoded square wave. The only requirements are that the input frequency fall within the tuning range of the PLL and the duty cycles chosen for encoding be sufficiently far away from 50% that there are no timing errors.

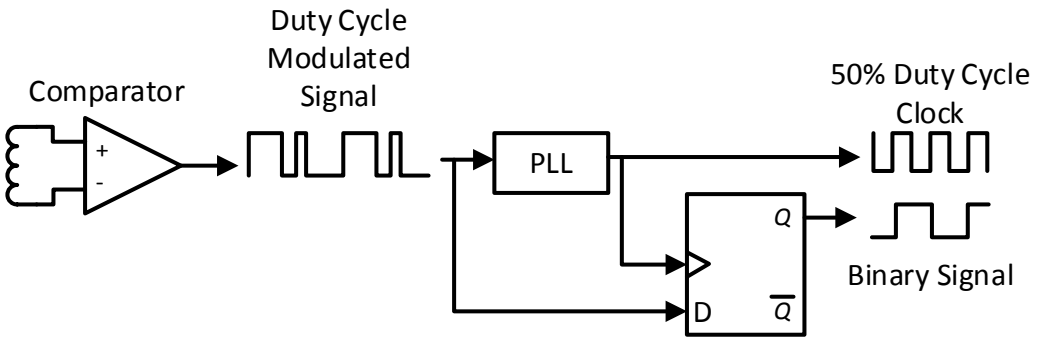


Fig. 1.2. An isolated data transmission system utilizing the described PLL along with a comparator and D flip-flop.

1.2 Organization of this dissertation

This dissertation is organized in a topical, not chronological, format. Chapter 2 covers a wide range of topics informing and leading up to the design of the phase-locked loops in SiC. Chapter 3 describes the state of the art in hand analysis of circuits using SiC MOSFETs, and proposes several ways in which existing models may be improved to lend additional precision and increase the designer's intuition. In addition, the important behaviors identified in Chapter 3 provide a platform for discussion between design engineers, fabrication engineers, and model developers for future work on SiC CMOS processes.

Chapters 4 through 6 trace the development of the phase-locked loop in SiC, and much of the work does not rely on the work in Chapter 3. This is for two reasons. The first is that the work of Chapter 3 took place throughout the design process, including after the final design submission took place. The second, and equally important, reason was the significant variability that still exists in SiC IC processes. By selecting topologies which did not rely on accurate device parameters to function, the probability of a functioning circuit in the presence of large variability was greatly improved, and the design process could be further improved by the

lessons learned in these pioneering circuits. Chapter 4 discusses the initial design of the PLL, Chapter 5 discusses the testing of the first fabricated PLL, and Chapter 6 describes changes made to the design in light of the findings of Chapter 5 and improved device models.

A comment about plots of measured MOSFET data in this dissertation is in order. In many cases, measured MOSFET data is compared to a mathematical model. In order to visually demonstrate the sampled nature of the MOSFET data, a □ (box symbol) is used at each data point without connecting lines between data points. Mathematical models are denoted by lines that may be solid or dashed. For consistency, the MOSFET data is always shown the same way, even when no mathematical model is shown in the plot. Sampled data from circuit simulations often have fewer data points, and linear connecting lines between data points are used to make plots easier to interpret.

CHAPTER 2 - BACKGROUND

2.1 Wide Bandgap Materials

The term “wide bandgap” refers to semiconductors with a bandgap energy significantly greater than that of silicon (Si). SiC and gallium nitride (GaN) are the most common wide bandgap materials in use at this time. Bandgap energy is the amount of energy that is necessary to raise electrons from the valence band to the conduction band, thus allowing current to flow. This increased energy threshold has implications for critical electric field, thermal capability, and radiation susceptibility. SiC can form in multiple polytypes, but, unless otherwise noted, only the 4H polytype is described in this dissertation. Table I compares properties for Si, SiC, and GaN [13].

TABLE I.
COMPARISON OF MATERIAL PROPERTIES FOR SI, SIC, AND GAN

Parameter	Silicon	4H-SiC	GaN
Bandgap Energy W_g (eV)	1.12	3.26	3.39
Critical Electric Field E_{crit} (MV/cm)	0.23	2.2	3.3
Relative Permittivity ε_r	11.8	9.7	9.0
Electron Mobility μ_n ($cm^2/V \cdot s$)	1400	950	800/1700 †
Intrinsic Carrier Concentration n_i at 300 K (cm^{-3})	1e10	8e-9	2e-10
Thermal Conductance λ ($W/cm^2 \cdot K$)	1.5	3.8	1.3 ‡
Baliga FOM $\varepsilon_r \mu_n E_C^3$ ($V^2/cm \cdot s$)	2.0×10^{20}	9.8×10^{22}	2.6×10^{23} (bulk)

† The lower value is for bulk doped GaN, and the higher value is for the 2-Dimensional Electron Gas that forms the channel of a GaN/AlGaN High-Electron Mobility Transistor.

‡ This value is for epitaxial GaN grown on a dissimilar substrate, which is far more common than bulk GaN.

The higher critical electric field of wide bandgap materials leads to improvements in both power and low-voltage semiconductor devices. For both lateral and vertical insulated-gate devices, the gate oxide is the primary limitation on the gate-source voltage. To achieve drain-source voltage (blocking voltage) ratings significantly more than the gate-source voltage, an additional separation between the gate and drain of the devices, termed the drift region, is necessary. The cost of adding the drift region is additional on-state resistance ($r_{DS,on}$), and optimizing the tradeoff between blocking voltage and $r_{DS,on}$ is fundamental to the design of the device. The specific on-resistance of the ideal drift region is described by Baliga in [14], and is given by:

$$\boldsymbol{R_{on-ideal} = \frac{4BV^2}{\varepsilon_r \mu_n E_C^3}} \qquad (2.1)$$

As can be seen, the critical electric field, E_C, is a cubic term in the denominator, and therefore has a large effect on the on-resistance of the drift region. The Baliga Figure of Merit (BFOM) is the denominator of Eq. (2.1), and is included in Table I. The ideal on-resistance of a SiC device is nearly 500 times lower than that of a Si device. Fig. 2.1 shows the location of the drift region in both lateral and vertical MOSFETs.

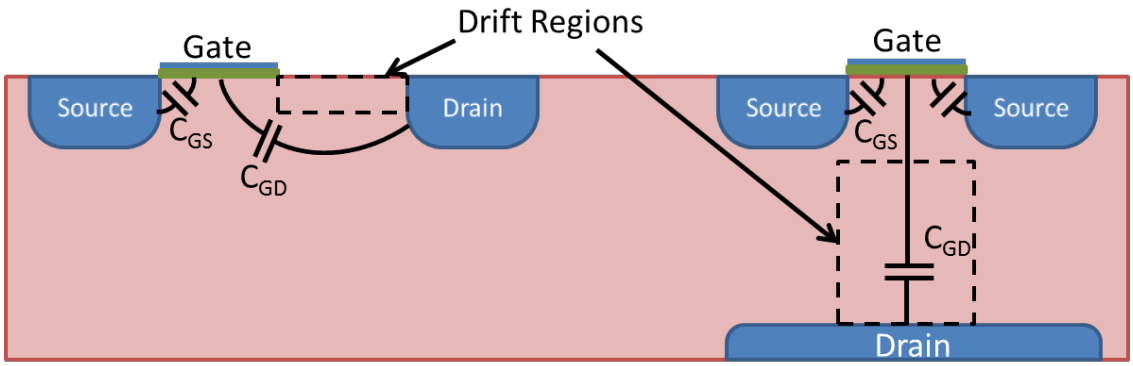


Fig. 2.1. Drift Regions in Lateral and Vertical MOSFETs.

A larger critical electric field allows SiC devices to have shorter drift regions for the same blocking voltage as Si devices. Although SiC has a lower mobility than Si (Table I), this is outweighed by the reduced drift length and the device will ultimately have a lower on-resistance. For vertical devices, the channel area can also be reduced, corresponding to a reduced gate area and ultimately, total gate capacitance. The disadvantage of reducing the drift-region length in vertical devices is an increase in gate-drain capacitance with respect to the gate-source capacitance. The change in this capacitance ratio allows Miller currents to charge the gate-source capacitance to a higher voltage, and increases the device's susceptibility to parasitic turn-on.

As seen in Table I, the intrinsic carrier-concentration (n_i) of wide bandgap materials is much lower than Si. This is the source of the increase in thermal capability of these materials. A doped semiconductor is effective as long as the n_i is much lower than the doped (extrinsic) carrier concentration (n_o) [15]. Wide bandgap materials will not reach this crossover point until much higher temperatures.

Radiation effects in integrated circuits are categorized into three primary categories: displacement damage, single-event effects (SEE), and total-ionizing dose (TID). Displacement

damage is a physical change in the crystal lattice of the material due to strikes by energetic particles. The Si-Si dissociation energy of 310 kJ/mol, whereas the dissociation energy of Si-C is 447 kJ/mol, both at 298 K [16]. This indicates that SiC will be less susceptible to displacement damage than Si. Single-event effects occur when radiation strikes generate currents in devices through the mechanism known as linear energy transfer (LET). The larger bandgap of SiC indicates that a larger LET is necessary to create the same current. Both of these effects are reduced with respect to Si directly by the material properties of SiC. TID is caused by an accumulation of charge in the oxide for insulated-gate devices such as MOSFETs and has the effect of shifting the threshold voltage of the device. Although TID is not inherently reduced in SiC, the reduction of transconductance and increase of power supply and threshold voltage reduce the influence of TID [17].

SiC has long been considered as a viable material for ICs [1], [18]. The first integrated circuits began to appear in the 1990s and utilized the 6H polytype of SiC. This period of interest lasted from the mid-1990s through the early 2000s, and was concentrated at a few places like Cree, Purdue University and Cornell University [19]–[22]. Since that time, the 4H polytype has, for the most part, supplanted 6H, and several new groups have contributed to the body of work. The variety of integrated circuit processes spans bipolar transistors, JFETs, and MOSFETs, with NPN BJTs, N-type JFETs and MOSFETs being common, and depletion-mode NFETs or PFETs being available as a complementary device in some processes, but only processes with PFETs can be considered true CMOS technology.

A group at Case Western University has focused on JFET-based ICs in 6H SiC, and has demonstrated operation at temperatures in excess of 550 °C [23]. At the GE Global Research

Center, they have focused on both analog and digital NFET-based circuits including packaging them for high temperature operation and reliability [24]. A partnership between the University of Arkansas, Oak Ridge National Lab, and Cree was driven by a desire to integrate low-voltage processing and control with a high-voltage power device [25]–[27]. Finally, previous work at Raytheon System Limited UK (the foundry) has focused on creating a more commercially-viable high-temperature SiC (HTSiC) CMOS IC process [28], [29]. The work described in this dissertation utilizes a variant of the Raytheon HTSiC CMOS process.

There are several challenges common to all SiC IC processes which must be overcome to design functional circuits. First and foremost, SiC MOSFETs exhibit transconductances significantly lower than might be assumed by examining the material bulk mobility [30]. Referring back to Table I, the bulk electron mobility of 4H SiC is around 2/3 that of bulk Si. Instead of the observed transconductance being 1/3 less than common Si integrated NFETs, it may be around a factor of 100 less. Transconductances in SiC and Si PFETs follow a similar trend.

The diffusion coefficient of SiC is also extremely low, and high-energy ion implantation is the only feasible way of creating selectively doped regions necessary for the drains and sources of MOSFETs. After implantation, a high temperature (1200-1800 ℃) anneal is necessary to activate the dopants and repair damage to the lattice from the implantation. This high temperature step destroys oxide and polysilicon, so the gate must be applied afterwards [30]. The gate must overlap the source and drain regions by a significant amount so that a misalignment during processing will not reduce device yield. This is unlike modern Si processing, where the gate is used as a masking layer for source and drain diffusion, commonly referred to as a self-

aligned gate. The result is increased gate-drain and gate-source capacitance with respect to Si. This, combined with the limited current drive due to lower transconductance, significantly limits the high-speed operation of SiC ICs.

2.2 The Raytheon Silicon Carbide CMOS Process

The HTSiC CMOS process utilizes an n-type substrate suitable for creating PFET devices. In this substrate, a p-well can be implanted as a base for NFET devices. The lack of an isolated n-well means that all PFET devices have their body terminals connected to the positive voltage supply. The process uses a polysilicon (poly) gate similar to Si processes, and there is a second polysilicon layer which can be used in conjunction with the lower poly to form a capacitor, or grown with high resistivity to form resistors. The process offers one metal layer. A simplified process cross-section is shown in Fig. 2.2.

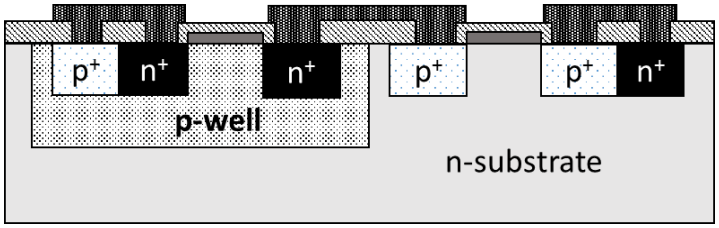


Fig. 2.2. Simplified cross-section of the Raytheon HTSiC CMOS process.

The Raytheon HTSiC process, like all SiC IC processes, is still undergoing development. The test devices that were delivered to the University of Arkansas during Winter 2013 consisted of a variety of fabrication profiles and performances. The circuit design team (consisting of the UA and Ozark Integrated Circuits) identified a set of performance targets for the NFET and PFET devices, focusing on device lengths of 1.2, 2, 5, and 10 μm. After discussion with the foundry, several NFET and PFET device models were generated at the UA. The NFET device

models were based on specific test devices, whereas the PFET device models were based on a set of devices, but integrated expected improvements in behavior with respect to existing devices. Fig. 2.3 shows the measured data from the chosen test devices at room temperature.

Several challenges in using the HTSiC process were observed while measuring devices for modeling efforts. The target NFET and PFET devices were chosen from different wafers, so at design time, it had not been proven that these device profiles could be fabricated on the same wafer. The PFET data in Fig. 2.3 show a flat slope unusual for a MOSFET. This portion of the data was not modeled, since Raytheon expected to remove this behavior in the circuits fabrication run (referred to as Tapeout 1 throughout the remainder of this dissertation).

Circuit designers usually use one of several simplified models to help them understand the devices available for circuit design. Foremost among these is the Shichman-Hodges model, which states that for a MOSFET in saturation (see Eq. (2.2)), the current is inversely proportional to L. Fig. 2.4 shows the normalized current through a long (L= 10 μm) and short (L=2 μm) device. Some difference will be expected since the channel modulation parameter, λ, is a function of length. The vertical offset observed in Fig. 2.4 indicates that the transconductance, *k'*, is also a function of length.

$$i_D = \frac{k'}{2}\frac{W}{L}(v_{GS} - V_t)^2\left[1 + \lambda\left(v_{DS} - v_{gs} + V_t\right)\right] \quad v_{DS} \geq v_{GS} - V_t \qquad (2.2)$$

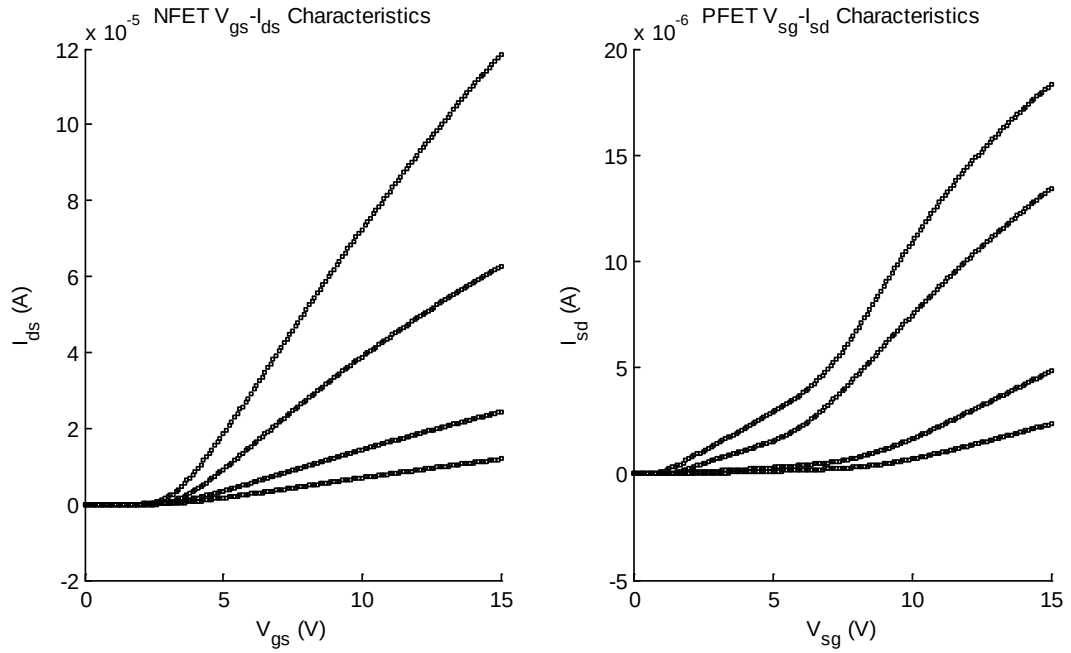


Fig. 2.3. NFET and PFET characteristics at V_{gs} (V_{sg}) = 5 V at room temperature. W/L = 20 µm/1.2 µm, 20 µm/2 µm, 20 µm/5 µm, and 20 µm/10 µm.

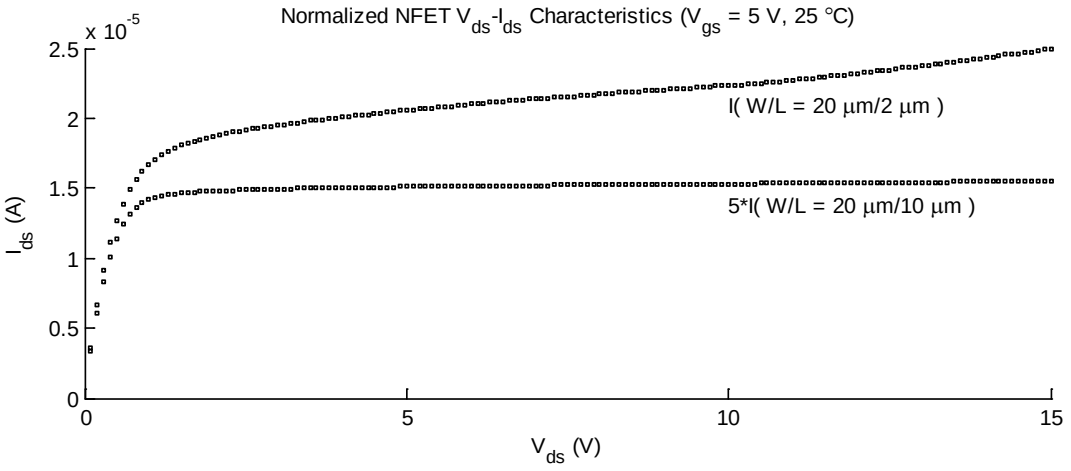


Fig. 2.4. NFET V_{ds}-I_{ds} curves normalized for W/L.

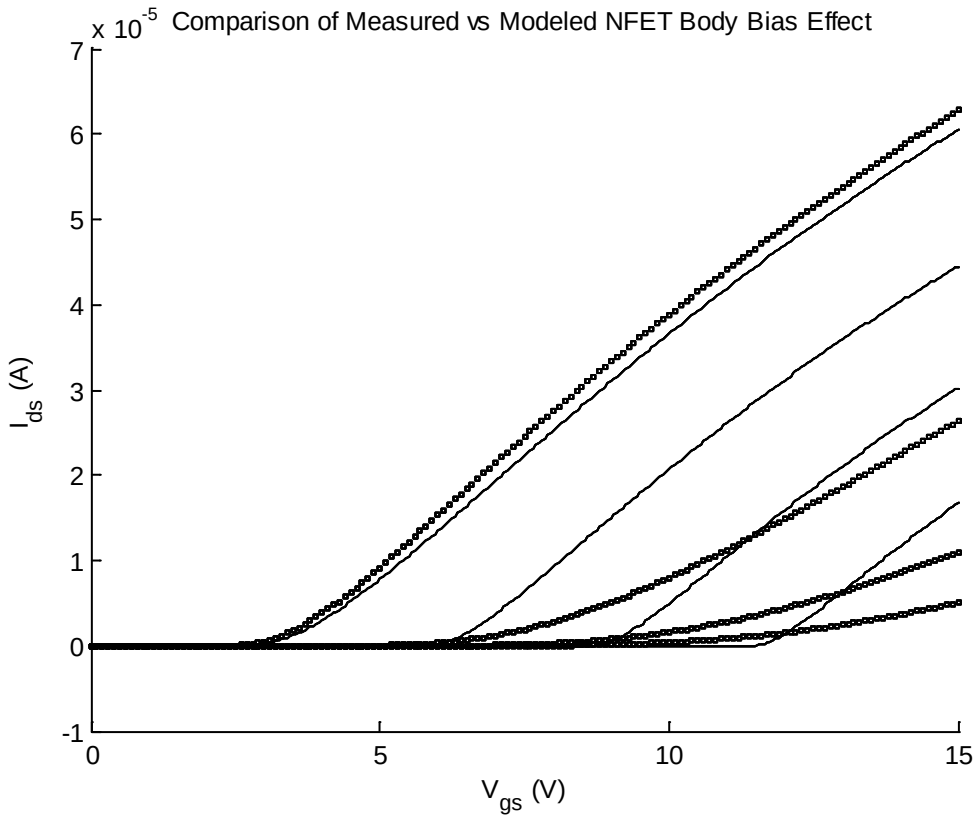


Fig. 2.5. Comparison of measured and modeled body bias effects in the NFET with W/L = 20 µm/2 µm at V_{gs} = 5 V. V_{sb} = 0 V, 3 V, 6 V, and 9 V.

Fig. 2.5 shows a challenge that became apparent during the device modeling. The BSIM3v3 model that was used could not be accurately fit to the observed body-bias effect. This meant that simulations could not be expected to predict device performance when the transistors had $V_{SB} \neq 0$ V.

2.3 Phase-Locked Loops

PLLs are a fundamental building block of many types of systems. There are many variations of PLLs but, at their core, they are control systems which seek to force an output signal to have the same phase as an input or reference signal. The derivative of phase with

respect to time is the instantaneous frequency, so a PLL is also a control system which forces the output (or feedback) frequency to match the input frequency [31].

Fig. 2.6 shows the topology of a PLL suitable for implementation in a CMOS integrated circuit. The input, u_1 is a nominally periodic signal with properties radial frequency, ω, and phase, θ. The phase detector, which serves the function of generating an error signal, has an output u_d, which is electrical, and has properties of both voltage and current. The loop filter acts on the signal u_d and to produce output u_f. The voltage-controlled oscillator (VCO), will have a MOSFET input, so the input u_f will have a negligible current. The VCO generates another nominally periodic signal, u_2, as the loop output. In the feedback path, there may be a feedback block which converts u_2 into another signal u_2'. This feedback block is most commonly a divide-by-N counter, which will make the output signal, u_2, N times greater than the input signal u_1.

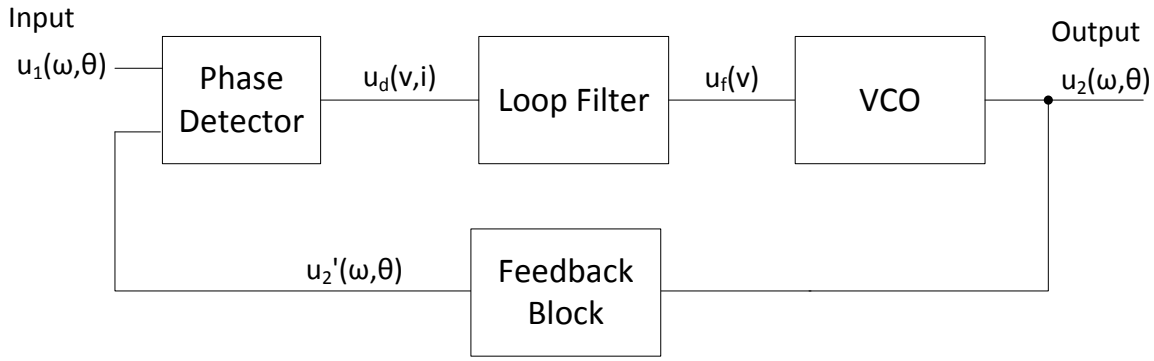


Fig. 2.6. General control-loop topology of a PLL.

The charge-pump PLL, shown in Fig. 2.7, is a circuit implementation of the general topology shown in Fig. 2.6. The loop filter in Fig. 2.6 is split into two separate blocks, a mixed-signal block called the charge pump, and a passive block consisting of resistor(s) and capacitor(s). The charge pump nomenclature should not be confused with a capacitor-based DC-to-DC converter which is also commonly used in ICs and referred to as a charge pump. In the

case of a PLL, the charge pump is actually a digitally controlled current source/sink. The loop filter in a charge-pump PLL is a series RC circuit, which converts the current sourced or sunk by the charge pump into the voltage which drives the VCO input. In Fig. 2.7, the gains K_D, K_P, and K_O correspond to the digital phase frequency detector (PFD), the charge pump, and the VCO, and have units 1/(2π radians), Amps and (radians/second)/volt. The Laplace-domain transfer function is Eq. (2.3) and the characteristic frequency and damping coefficient are Eqs. (2.4) and (2.5).

$$H(s) = \frac{K_D K_P K_O (1+sRC)}{s^2 NC + sK_D K_P K_O RC + K_D K_P K_O} \tag{2.3}$$

$$\omega_n^2 = \frac{K_D K_P K_O}{NC} \tag{2.4}$$

$$\zeta = \frac{\omega_n RC}{2} \tag{2.5}$$

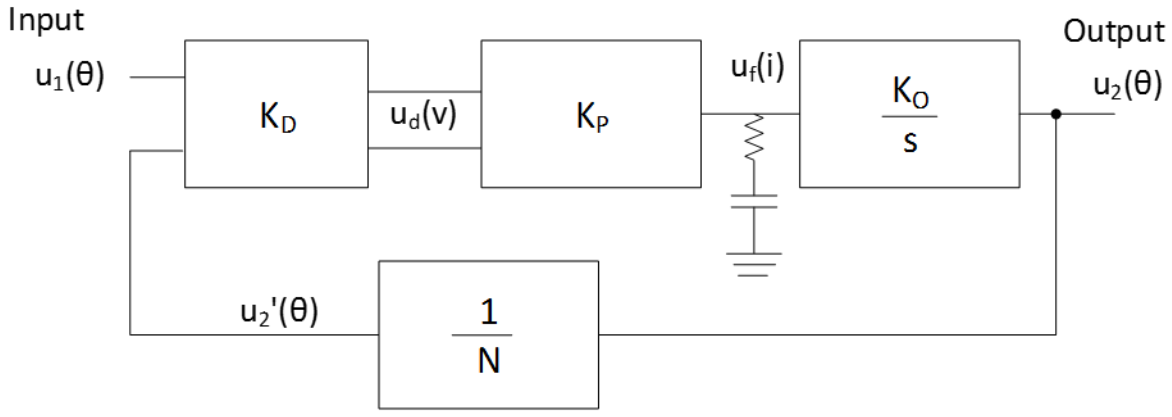


Fig. 2.7. Control loop implementation of the charge-pump PLL and the resulting Laplace-domain transfer function, natural frequency and damping ratio.

2.3.1 Phase Frequency Detectors

Best describes four types of phase detectors (PDs): Multipliers, EXOR gates, JK-flip-flop gates, and Phase-Frequency Detectors in [10]. The multiplier PD is the only one appropriate for sinusoidal input signals, but it can also be used with square wave (digital) input signals. Although it is very flexible, it is also much slower than the Phase-Frequency Detector to achieve lock.

The EXOR and JK-flip-flop PDs are the digital gates one would expect, without any extra circuitry. The EXOR PD achieves lock when the input and output signals are near 90° out-of-phase, while the JK-flip-flop achieves lock with input signals in-phase. Both of these types have a single, logic-level output which is used to drive the loop filter.

The final type of phase detector is the Phase-Frequency Detector or PFD. The complete operation of the PFD is described in Chapter 4, but it is the only PD that has a tri-state output capable of driving a charge pump. The three states of the PFD are 0, +1, and -1, which indicate the frequency requires NO CHANGE, speed UP, or slow DOWN (or DN). For this work, a charge-pump PLL topology was chosen, so the phase detector was a PFD. Fig. 2.8 shows the state transition diagram. The PFD starts at NO CHANGE, and transitions to UP or DN when the CLK and DCLK signals are asserted, respectively. After that, the PFD holds its' state until the other input signal is asserted (DCLK or CLK following the pattern described). The PFD then enters a transient reset state before returning to the NO CHANGE state.

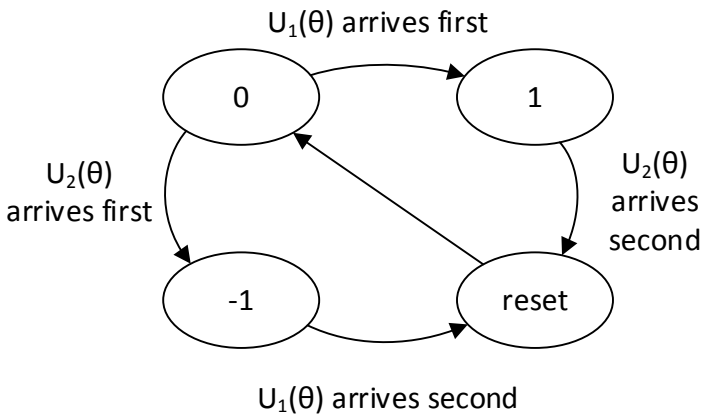


Fig. 2.8. State Diagram of the PFD.

Fig. 2.9 shows a comparison of the output functions for these three PDs. The EXOR and JK PDs are often used with active filters which can remove the DC offset in the transfer function. Without an active filter, the phase error of PLLs incorporating these PDs will not be zero except when the output frequency corresponds to a PD output of 0.5. The PFD, being bipolar, does not require an active amplifier in the loop filter in order to achieve theoretical zero phase error if it is driving a charge pump.

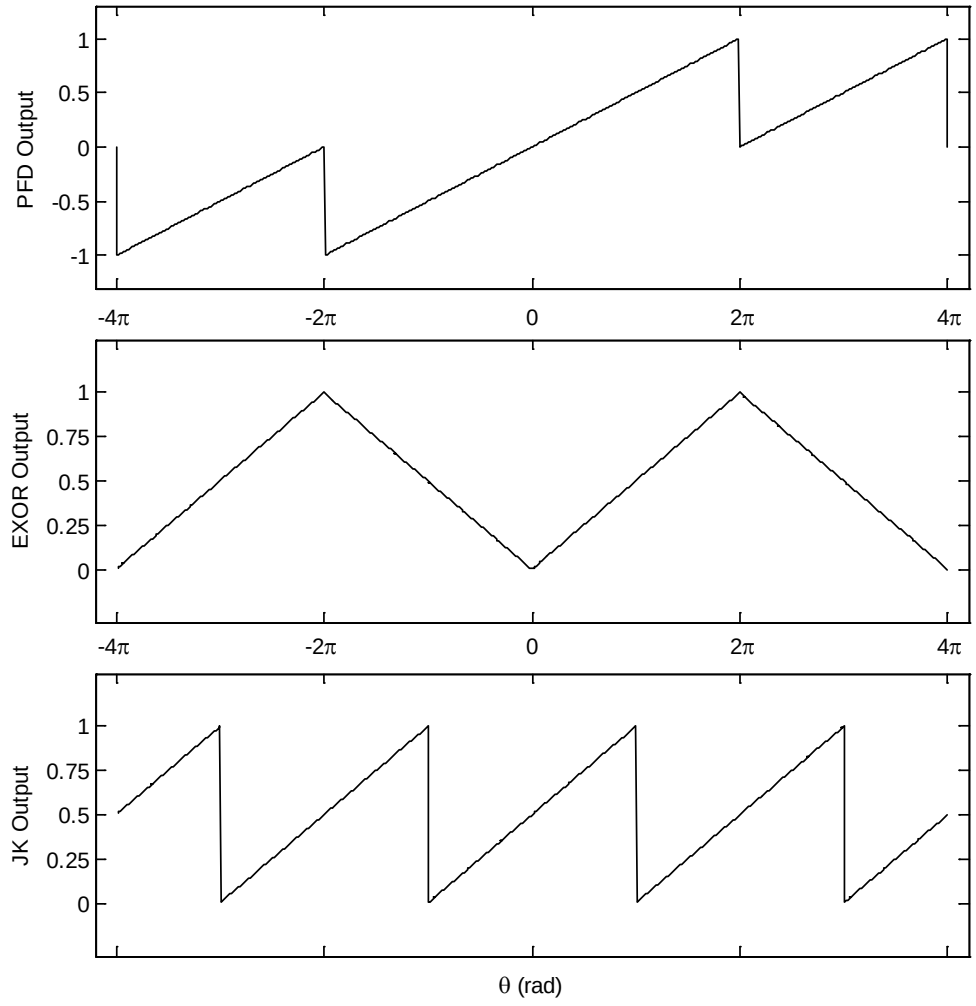


Fig. 2.9. Time-averaged output functions for different phase detectors versus input phase.

2.3.2 Charge Pumps

The charge pump can only be paired with a PFD-type of phase detector. It requires the bipolar input, but in return, it offers a high-impedance state when the input is zero. The high-impedance state allows the PFD-charge pump combination to achieve theoretically zero phase error at any frequency. Fig. 2.10 shows the simple functional diagram of the charge pump. The current output of the charge pump (which can be positive or negative), is converted into a voltage by the RC network to ground as seen in Fig. 2.7.

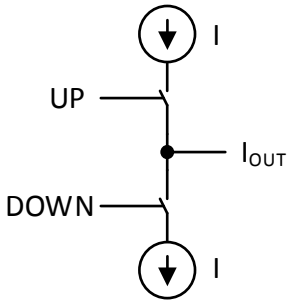


Fig. 2.10. Functional diagram of the charge pump.

2.3.3 Voltage-Controlled Oscillators

The VCO is the heart of the phase-locked loop. The perfect VCO has several characteristics:

- Large tuning range
- Low tuning gain (to minimize the effect of input noise)
- Low internal timing jitter/phase noise (High Q)
- Low supply-noise sensitivity

These characteristics are not universally achievable, and in fact, large tuning range and low tuning gain are somewhat exclusive. Ultimately, though, the VCO must provide the needed output frequency for the PLL, and not vary significantly due to input noise, internal noise, or power supply noise. The various topologies available for VCOs balance these requirements against complexity, size, and the ability to be fully integrated on an integrated circuit.

In [32], the authors classify VCOs into three categories: resonant-tank, relaxation, and ring oscillators. Resonant-tank oscillators can be built with either a crystal or LC tank. Crystals are not available in IC processes, and inductors are generally not practical for integration on ICs

for frequencies below 1 GHz. Even then, the low Q associated with IC inductors reduces the benefit of the resonant-tank oscillator: minimum jitter (maximum Q). Resonant-tank oscillators also have limited tuning range due to the methods of realizing variable capacitors on-chip. Relaxation oscillators may be the most space efficient depending on the energy storage element (usually a capacitor). They also have a much wider tuning range than resonant-tank oscillators. The downfall of relaxation oscillators is that they utilize a regenerative switching element which increases the timing jitter. Ring oscillators strike a balance between larger area and higher complexity with respect to relaxation oscillators, while being fully realizable on an IC and having a broader tuning range than resonant-tank oscillators. Examples of all three types of voltage controlled oscillators are shown in Fig. 2.11.

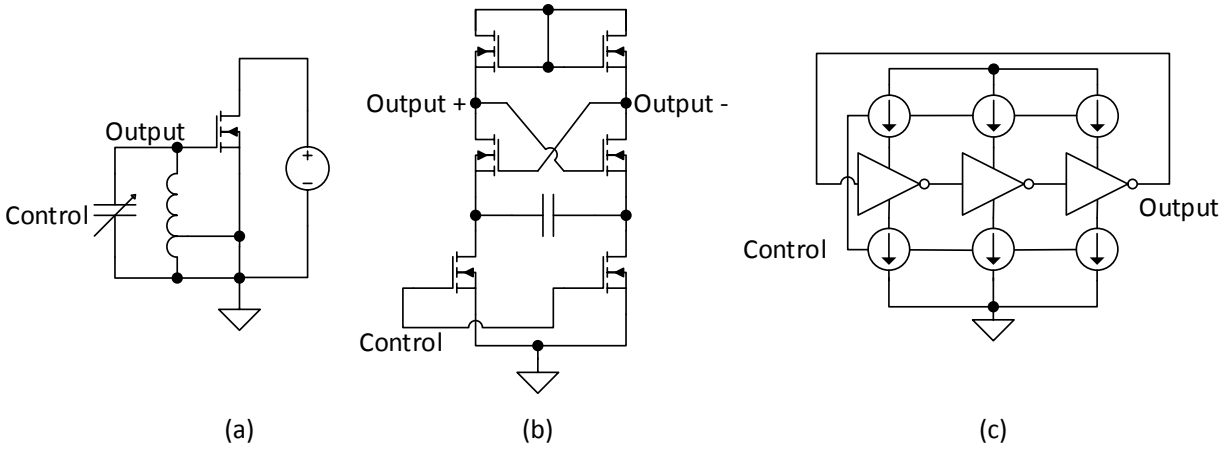


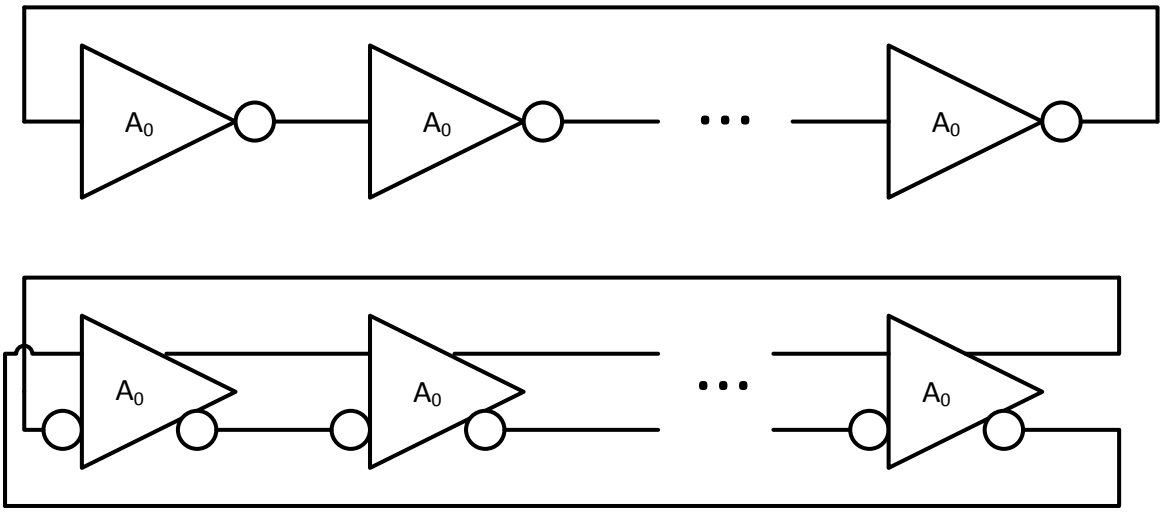
Fig. 2.11. LC Tank (Hartley) Oscillator (a), Relaxation (Source-Coupled) Oscillator (b), and Ring (Current-starved Inverter) Oscillator (c).

Voltage-controlled ring oscillators may be either single-ended or differential, and consist of a number of individual stages (called delay stages). To be classified as a ring oscillator, the number of delay stages must be three or more. The Barkhausen stability criterion, originally identified in the 1920s, assumes a linear system, and therefore cannot be considered an accurate

predictor of oscillation frequency. It remains, however, a useful heuristic to design the gain stages of a ring oscillator to support spontaneous oscillation. The Barkhausen criterion relates the forward loop gain A to the feedback gain β, and can be considered a necessary, but not sufficient, condition for oscillation:

$$|\beta A| = 1 \quad \angle \beta A = 2\pi n, n \in 0,1,2,3, \ldots \tag{2.6}$$

Since each delay stage will have a finite, but non-zero, time delay t_d, it will have an equivalent phase delay at its frequency of operation, $\Delta\Phi$. If a ring oscillator is connected so that the angle criterion is inherently satisfied, which is the case when a single-ended ring oscillator has an even number of stages ($2n\pi$ for n stages), then $\Delta\Phi$ must be zero, which is equivalent to a finite non-zero delay only at DC. Hence, single-ended ring oscillators must always have an odd number of stages. Similarly, differential ring oscillators must have an inversion present in the ring, but this is created by cross connecting the signals at one stage, and any number of stages greater than two can be used. Fig. 2.12 shows the Barkhausen criterion as it applies to both single-ended and differential ring oscillators.



$\beta=1$ $A=NA_0$ $\Delta\Phi=2\pi\omega/t_d$

Single Ended: $\angle A= N\pi + N\Delta\Phi$ Differential: $\angle A= \pi + N\Delta\Phi$

Fig. 2.12. Barkhausen criterion applied to single-ended and differential ring oscillators of N stages.

Further, the Barkhausen criterion equations are often used to determine the minimum gain necessary to stimulate oscillation from a quiescent condition. The delay stages are assumed to have a first order response with a -3 dB frequency ω_0, and the gain at the oscillation frequency A_{osc} must be 1. The minimum DC gain is calculated for N stages:

$$\Delta\Phi = \frac{\pi}{N} = tan^{-1}\,{}^{\omega_{osc}}\!/_{\omega_0} \tag{2.7}$$

$$\omega_{osc} = \omega_0\, tan\frac{\pi}{N} \tag{2.8}$$

$$1 = |A_{osc}| = \frac{A_{DC}\omega_0}{\sqrt{\omega_0^2+\omega_{osc}^2}} = \frac{A_{DC}\omega_0}{\sqrt{\omega_0^2+\omega_0^2\, tan\frac{\pi}{N}}} \tag{2.9}$$

$$A_{DC} = \sqrt{1+\left(tan\frac{\pi}{N}\right)^2} \tag{2.10}$$

The equality in Eq. (2.10) is often generalized as a minimum, and the equation rewritten as

$$A_{DC} \geq sec\left(\frac{\pi}{N}\right) \qquad (2.11)$$

Eq. (2.11) is referred to as the secant criterion [33], [34]. The result of this analysis shows a minimum DC gain of 2 for three stages, $\sqrt{2}$ for four stages, and so on asymptotically approaching a DC gain of 1 for an infinite number of stages. This minimum gain is not trivial in SiC IC processes, and can be used as one method to test the robustness of the delay stage design.

2.2.4 Delay Stage Topologies

Several delay cell topologies are popular for voltage-controlled ring oscillators. The simplest is the current-starved inverter as shown in Fig. 2.11(c). The individual delay stage schematic is shown in Fig. 2.13. This delay cell is a popular single-ended delay stage for use in ring oscillators. At the center of the stack is an inverter, and the top and bottom FETs act as current sources to limit the slew rate going into the parasitic load capacitance. Ring oscillators built from current starved inverters have several benefits: simple biasing, compact layouts, rail-to-rail signal swing and straightforward design. The current-starved inverter ring oscillator suffers from the same drawbacks as all single-ended ring oscillators, namely poor supply-noise rejection and the requirement for an odd number of stages.

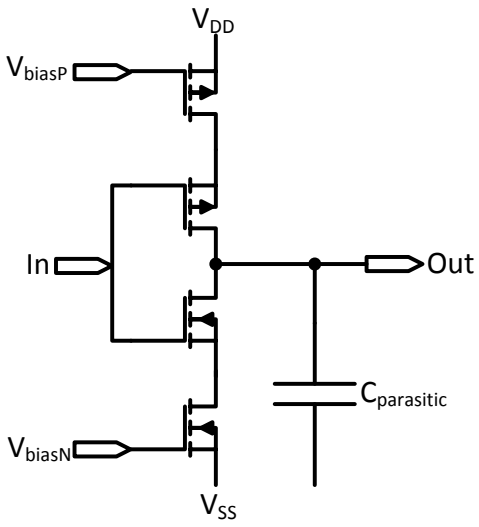


Fig. 2.13. Current-starved inverter delay stage.

Another class of delay cells are the differential delay cells. These cells generally resemble differential-pair amplifier stages, although there are many variations [35]. Fig. 2.14 shows the simplest of these: a differential input cell with resistive loads. The delay can be controlled by adjusting the bias voltage to the tail current source, with smaller currents causing greater delays. The capacitive loading on this cell is the input gates of the next cell, just as it was for the current-starved inverter.

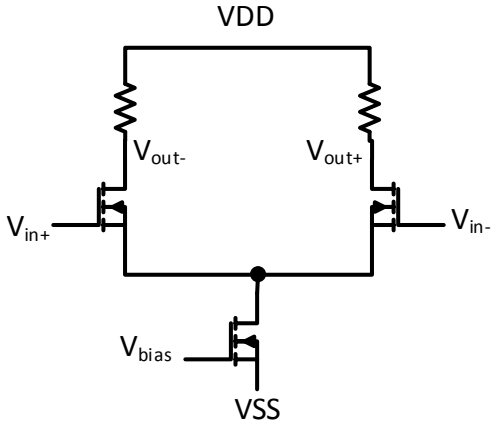


Fig. 2.14. Differential delay cell with resistive loads.

The Maneatis delay cell (Fig. 2.15) is extremely popular in the design of differential VCOs [33], [35]–[38]. This differential delay cell utilizes a load described as a symmetric load. Each leg has a pair of equally-sized PMOS devices, one diode-connected, and one separately-connected. The name "symmetric load" comes from the fact that the I-V characteristic is odd-symmetric about the middle point of the output voltage swing. Fig. 2.16 shows the I-V characteristic of a notional symmetric load including a finite output resistance. In the symmetric load, V_{cntrl} must be generated by a special biasing circuit to achieve the desired output swing when all of the cell current ($2I_D$) is passing through a single load. Two versions of this biasing circuit, called a half-buffer replica, are shown in Fig. 2.17 [39].

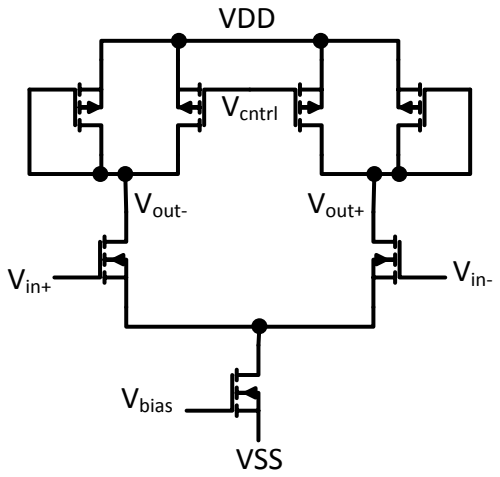


Fig. 2.15. Maneatis delay cell found in differential VCOs.

The bias of the symmetric load can be generated in two different ways. In many cases, the control voltage input of the PLL is used to generate a bias voltage for the tail current sources in the Maneatis delay cells as shown in Fig. 2.17(a) [36]–[38]. It is also possible to use a fixed value for V_{ref} to set the swing of the delay cells while controlling the tail current independently, as shown in Fig. 2.17(b) [40].

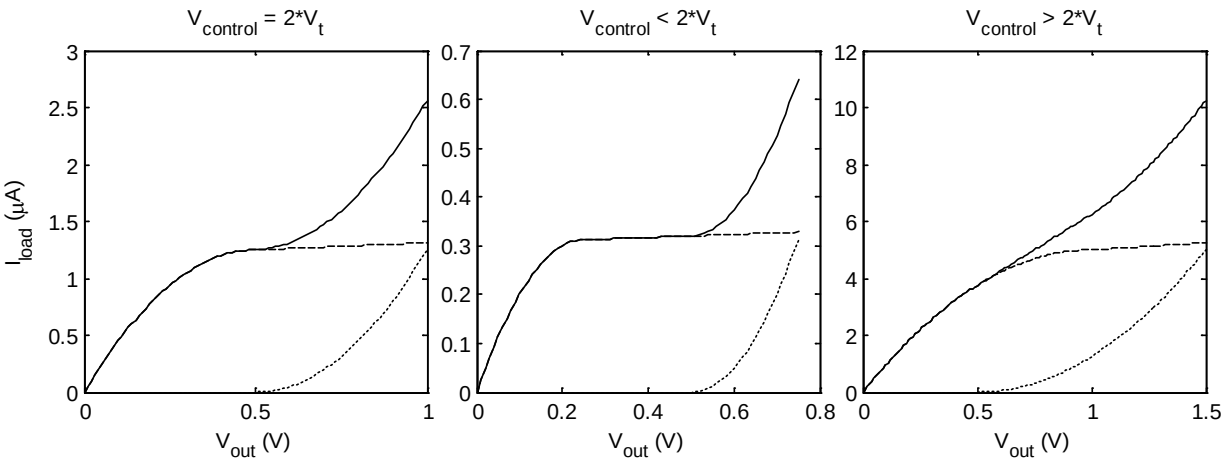


Fig. 2.16. Symmetric load output behavior at different values of $V_{control}$ with respect to V_t.

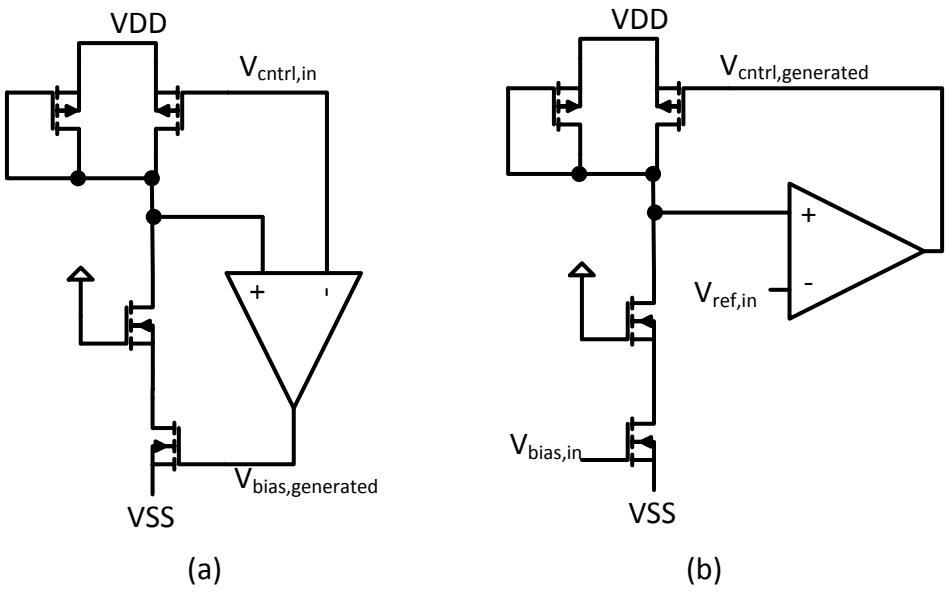


Fig. 2.17. Half-buffer replica biasing circuits for the Maneatis delay cell. The circuit in (a) has a single control input voltage that sets the bias current and the delay cell output swing, while the circuit in (b) forces the output swing to be fixed at V_{ref}, and $V_{bias,in}$ is provided to the delay cells as well.

CHAPTER 3 – DEVICE PARAMETERS FOR SILICON CARBIDE CMOS

Despite the existence of advanced models for computer simulation, and algorithms for computer-based circuit design, effective hand-design models and methods are still very valuable. Hand-design work allows the designer to develop intuition, investigate design trade-offs, and prove important causal relationships while investigating a circuit topology. Since its publication in 1968, the Shichman and Hodges Insulated Gate FET model[1] has been the standard bearer for designing circuits with these devices [41].

$$I_D = \begin{matrix} \mu C_{ox}\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right](1+\lambda V_{DS}) & V_{DS} \le V_{GS}-V_T \\ \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS}-V_T)^2(1+\lambda V_{DS}) & V_{DS} > V_{GS}-V_T \end{matrix} \qquad (3.1)$$

As device channel lengths grew smaller and smaller, Shichman and Hodges' model became inaccurate for predicting MOSFET behavior. Work done in the first half of the 1980s by individuals at MIT, Bell Labs, and UC Berkeley showed that carrier velocity saturation led to a very different equation for drain current [42], and the omnipresent UC Berkeley modeling and simulation group further developed this into a model suitable for short channel MOSFETs in 1996 [43]. This work is the seed for all short-channel design methods since that time [40]. Short channel devices can be described physically as devices where the gate length is comparable to the source and drain depletion region width, indicating that edge effects cannot be ignored in

[1] In modern texts, it has become common to drop the lambda term in the triode equation ($V_{DS} \le V_{GS} - V_T$) because the primary physical mechanism that defines lambda, channel pinch-off, only occurs in the saturation region. The original Shichman and Hodges model, however, includes lambda in both regions. The SPICE level 3 model *also* includes lambda in both equations in order to avoid a discontinuity in the first derivative. In this work, both versions are used, but the modern version, where the triode equation has no lambda term and the saturation equation lambda term is $1+\lambda(V_{DS}-V_{GS}+V_T)$ is used unless otherwise noted.

analyzing their behavior. Empirically, short channel devices show several effects not seen in long channel devices. These include, among others, velocity saturation, drain-induced barrier lowering (DIBL), the short channel effect (which has a similar behavior to DIBL), mobility reduction, and bulk-charge effects.

Arguably, the single effect which defines the difference between short- and long-channel behaviors is velocity saturation. Mobility is defined as the relationship between the drift velocity of the charge carrier and the applied electric field:

$$v_d = \mu E \tag{3.2}$$

Without velocity saturation, the drift velocity increases linearly with electric field, the mobility stays constant, and the drain current increases with the square of v_{gs}-V_t as seen in Eq. (3.1). When the carrier velocity saturates, however, the observed mobility has a negative slope which cancels the increase in electric field. Drain current is no longer dependent on device length, and is approximately linearly dependent on applied gate voltage [42]:

$$I_d = W C_{ox} v_{SAT} (v_{gs} - V_t - V_{ds,sat}) \tag{3.3}$$

Other models, such as the EKV model, have been proposed for both short- and long-channel devices [44]. These generally address specific deficiencies in the basic models such as the sub-threshold region. While these models enable new design methods in Si ICs, it will be demonstrated here that significant improvements can be made without abandoning the Shichman-Hodges framework.

A brief inspection of SiC MOSFET output curves in Fig. 3.1 shows what these devices *are not*. SiC MOSFETs of the type described in this work *do not show signs of velocity*

saturation. They are clearly not short-channel devices from this perspective. At the same time, they begin to show signs of saturation at drain-source voltages much less than the overdrive voltage, v_{gs}-V_t, and there is no exactly identifiable transition point between triode and saturation operation. This soft transition between triode and saturation has been observed in at least one other SiC IC process [8], [9]. In this dissertation, a variety of approaches to understanding the SiC MOSFET are examined, and an improved Shichman and Hodges model is formed empirically. This analysis forms the basis of designs and methods presented in later chapters.

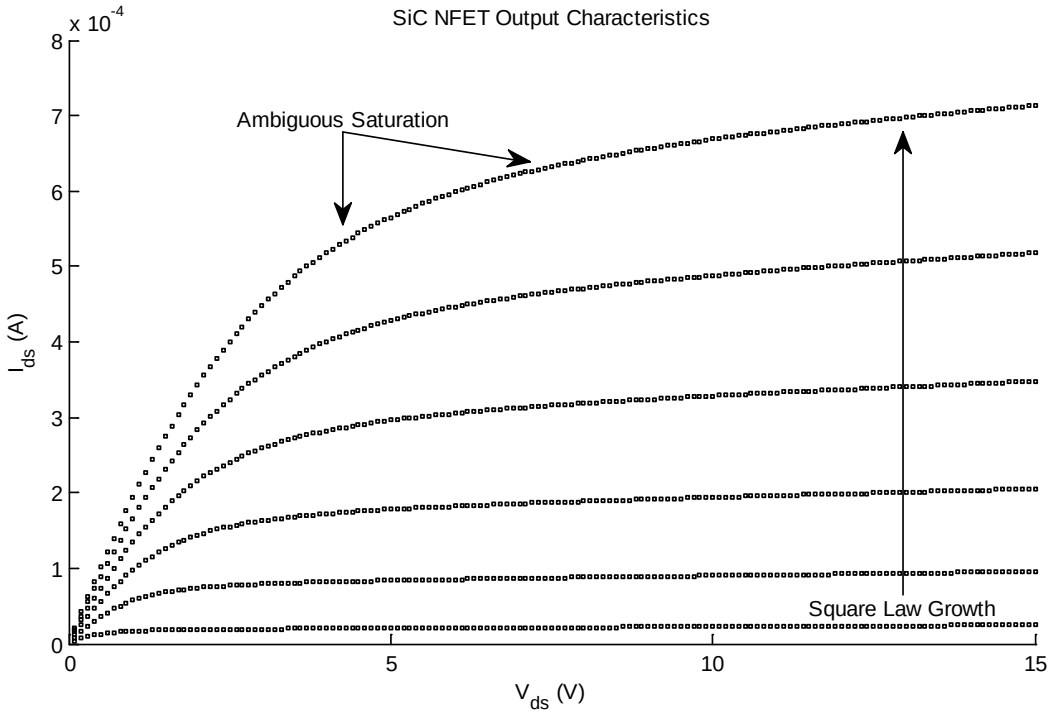


Fig. 3.1. Measured output characteristic of a SiC N-channel MOSFET at V_{gs} values of 5, 7, 9, 11, 13, and 15 V.

3.1 Using the Standard Shichman-Hodges Model with SiC

The documentation provided even for commercially available long-channel Si IC fabrication processes often does not contain recommended values for the Shichman-Hodges parameters k_p', k_n', λ_p, λ_n, $V_{t,p}$, and $V_{t,n}$. For long channel processes, these parameters are easily extracted from simulation. For short channel processes, a target operating point is usually selected, and the small-signal parameters are estimated for this bias point from simulation data [40].

When trying to fit SiC devices, the poor fidelity to the existing long channel models limits the range that can be used with hand-design parameters. Early SiC IC design efforts relied on a level 3 SPICE model, so parameters were extracted over the entire operating range of the devices, whether it fit actual device behavior or not [45], [46]. Experience at the University of Arkansas has shown that emulating the short-channel method, where a device operating point is selected from data, and small- and large-signal parameters matching the local region around this operating point, can lead to successful designs [8], [9]. In preparing for the first tapeout with the HTSiC process, a similar method was utilized. In contrast with previous methods employed at the UA, a graphical method of estimating parameters was used, which also gave an intuitive understanding of where these parameters would be more and less accurate.

3.2 Parameter Estimation, Bias Point Selection, and Standard Device Sizes in the Standard Shichman-Hodges Model

Before beginning the design process, the simulation device models most likely to be used for analog design (W = 20 μm, and L=2 μm and 5 μm) were characterized using a simulation testbench. This process involved developing estimates for the basic Shichman-Hodges

parameters k_p', k_n', λ_p, λ_n, $V_{t,p}$, and $V_{t,n}$. The goal was to allow hand calculations using the parameters which would give a reasonable match to the bias-point and transient results obtained during simulation.

The first parameter estimated, λ, was calculated from Eq. (3.4). This calculation could be done without assumptions about any other Shichman-Hodges parameters, since it only requires sweeping v_{DS} and measuring i_{DS} of the device model. To obtain the best estimate of λ, v_{GS} of the devices was stepped from 5 to 15 V, and a single value that would approximately minimize error was chosen visually. For the PFET case, values were kept positive, and the sources were connected to apply v_{SG} and v_{SD} instead. The visual estimations based on calculated λ curves for NFETs and PFETs are shown in Fig. 3.2 and Fig. 3.3, respectively.

$$\lambda = \frac{\partial i_D}{\partial v_{DS}} * \frac{1}{i_D} \qquad (3.4)$$

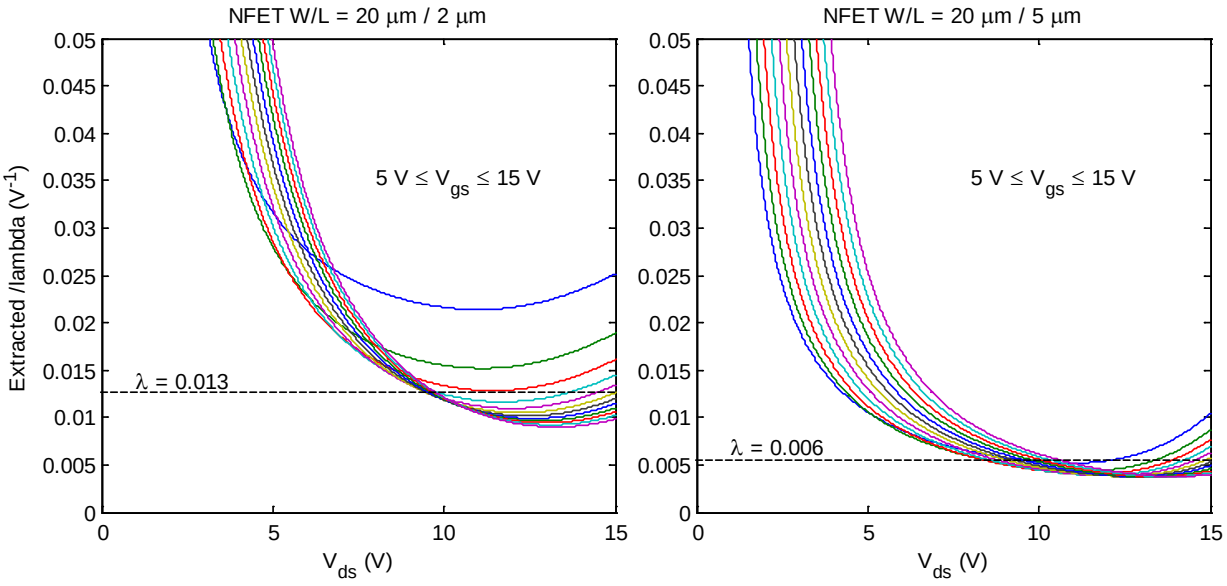


Fig. 3.2. Estimation of λ for NFETs.

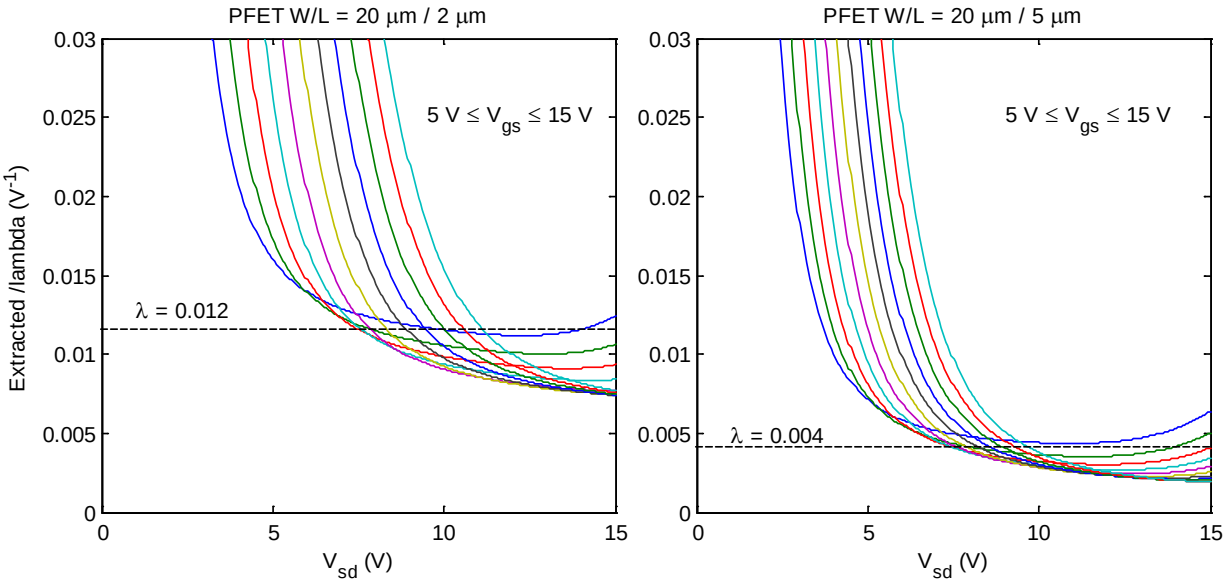


Fig. 3.3. Estimation of λ for PFETs.

With an estimation of λ complete, two different methods of estimating V_t and k' were used. The first, corresponding to the modern channel modulation formulation in the saturation equation (Eq. (3.5)) and the second corresponding to the original formulation (Eq. (3.6)).

$$i_D = k' \frac{W}{L} (v_{GS} - V_t)^2 \left[1 + \lambda \left(v_{DS} - (v_{GS} - V_t)\right)\right] \quad v_{DS} \geq v_{GS} - V_t \qquad (3.5)$$

$$i_D = k' \frac{W}{L} (v_{GS} - V_t)^2 [1 + \lambda v_{DS}] \quad v_{DS} \geq v_{GS} - V_t \qquad (3.6)$$

To obtain the estimations of V_t and k', v_{DS} was swept, and V_t was stepped in 50 mV steps (effectively "guessing" a value of V_t at each step). The value of v_{gs} was set equal to $v_{DS}+V_t$ to maintain the devices exactly in saturation (and negating λ for the modern formulation). For NFETs, V_t was stepped from 2.5 to 3.35 V. And for PFETs V_t was stepped from 3.2 to 4 V. To select an estimate of V_t, the plots were visually inspected and the V_t corresponding to the flattest

line was chosen. Then, a value of *k'* was selected visually to approximately minimize the error. Fig. 3.4 through Fig. 3.7 show these simulation results and parameter estimations. The modern channel-modulation formulation is labelled "No λ".

Table II contains the parameter values selected for the four devices after the procedure described above. These values were selected from the plots using the modern channel modulation formulation.

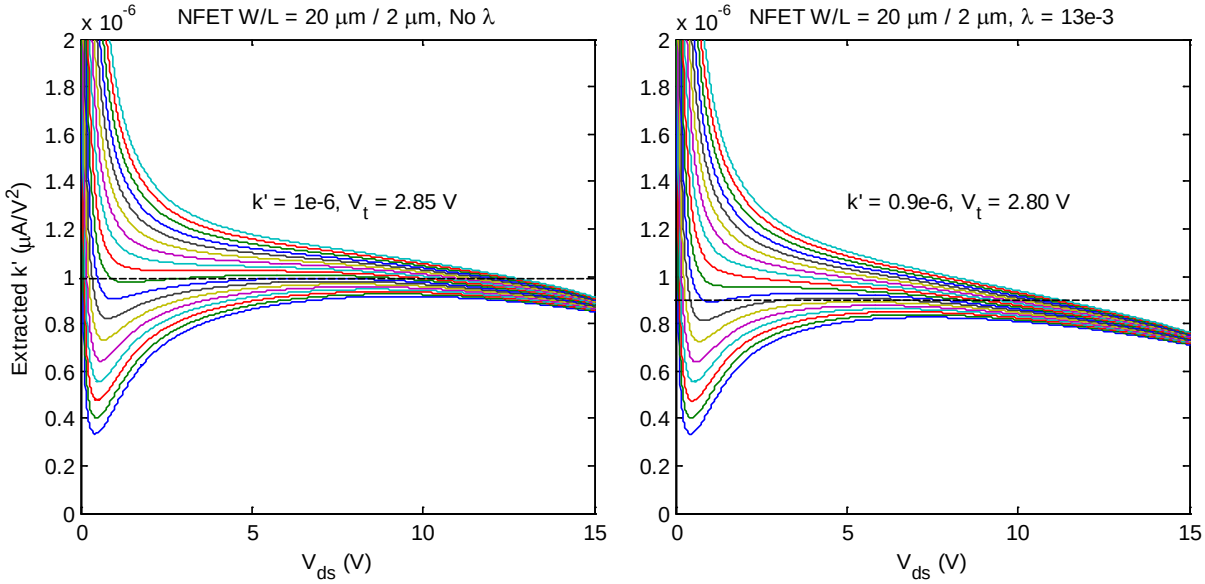


Fig. 3.4. Estimation of V_t and k' for 20 µm / 2 µm NFETs.

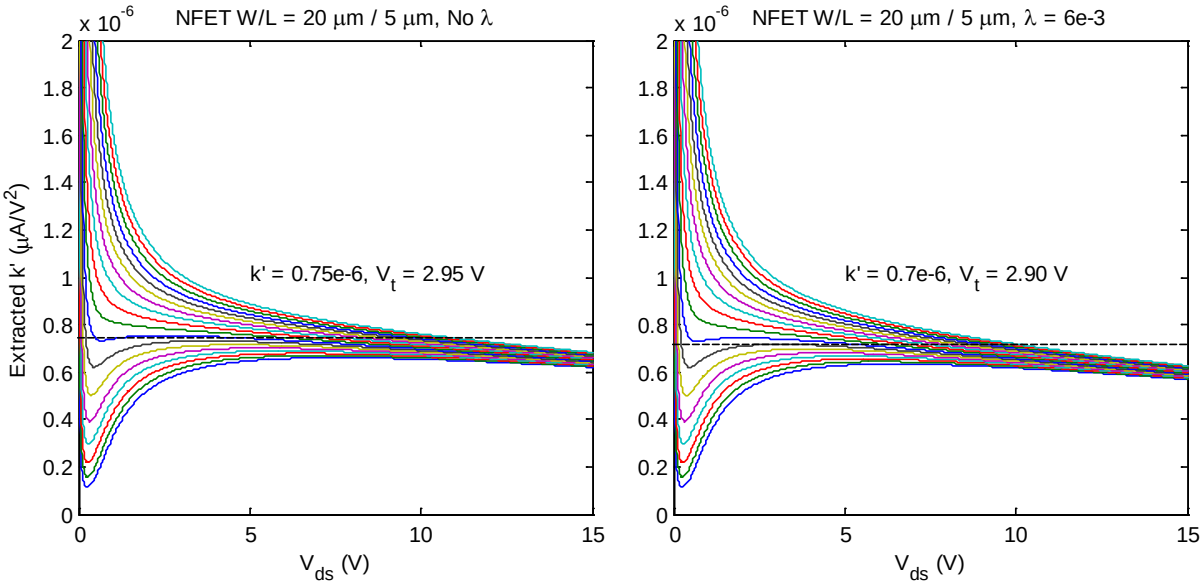


Fig. 3.5. Estimation of V_t and k' for 20 µm / 5 µm NFETs.

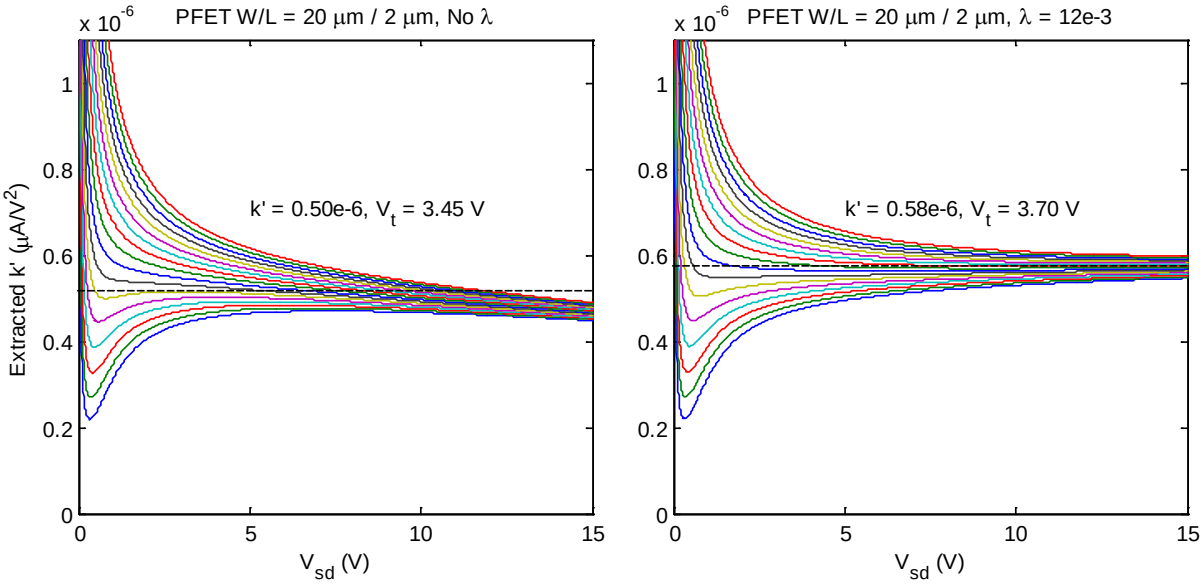


Fig. 3.6. Estimation of V_t and k' for 20 µm / 2 µm PFETs.

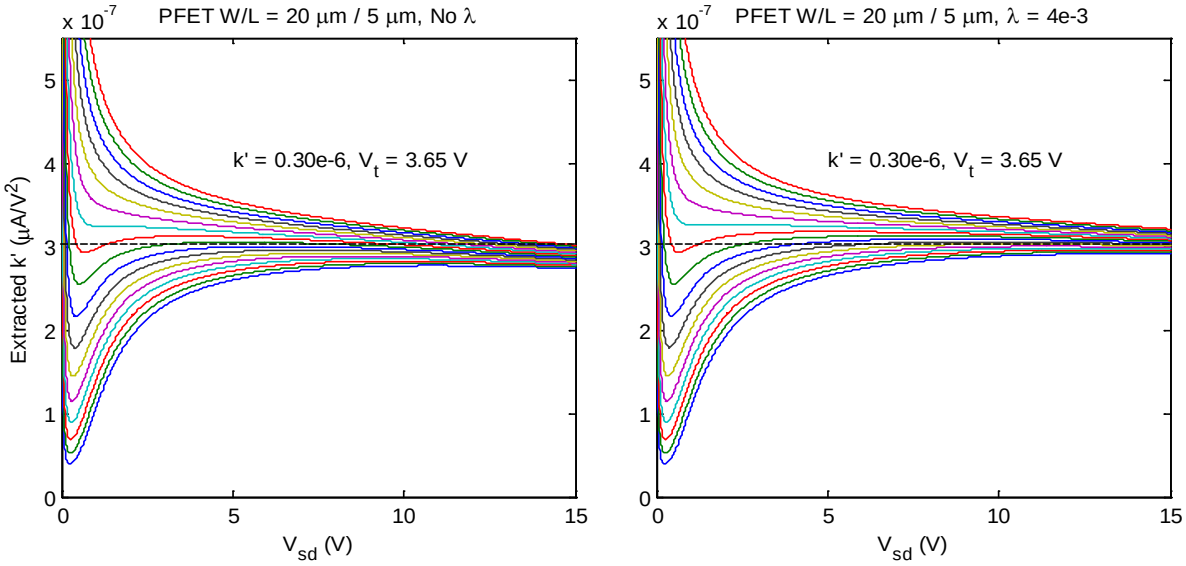


Fig. 3.7. Estimation of V_t and k' for 20 µm / 5 µm PFETs.

TABLE II.
EXTRACTED SHICHMAN-HODGES PARAMETERS FOR HTSIC MOSFETS

Device	Parameter	Value
NFET W/L=20 µm/2 µm	V_t (V)	2.85
	k' (µA/V^2)	1.0x10^{-6}
	λ (V^{-1})	0.013
NFET W/L=20 µm/5 µm	V_t (V)	2.90
	k' (µA/V^2)	0.75x10^{-6}
	λ (V^{-1})	0.006
PFET W/L=20 µm/2 µm	V_t (V)	3.45
	k' (µA/V^2)	0.50x10^{-6}
	λ (V^{-1})	0.012
PFET W/L=20 µm/5 µm	V_t (V)	3.65
	k' (µA/V^2)	0.30x10^{-6}
	λ (V^{-1})	0.004

Beyond estimating the Shichman-Hodges parameters, a general bias point was identified from the test device measurements. The NFET and PFET W/L = 20 μm / 2 μm device curves were examined, and bias currents of 5 μA and 2.5 μA were chosen, respectively. Fig. 3.8 and Fig. 3.9 show the input and output curves, and the selected currents for the devices. This also indicates a sizing ratio of 1:2 for the NFETs and PFETs with L = 2 μm.

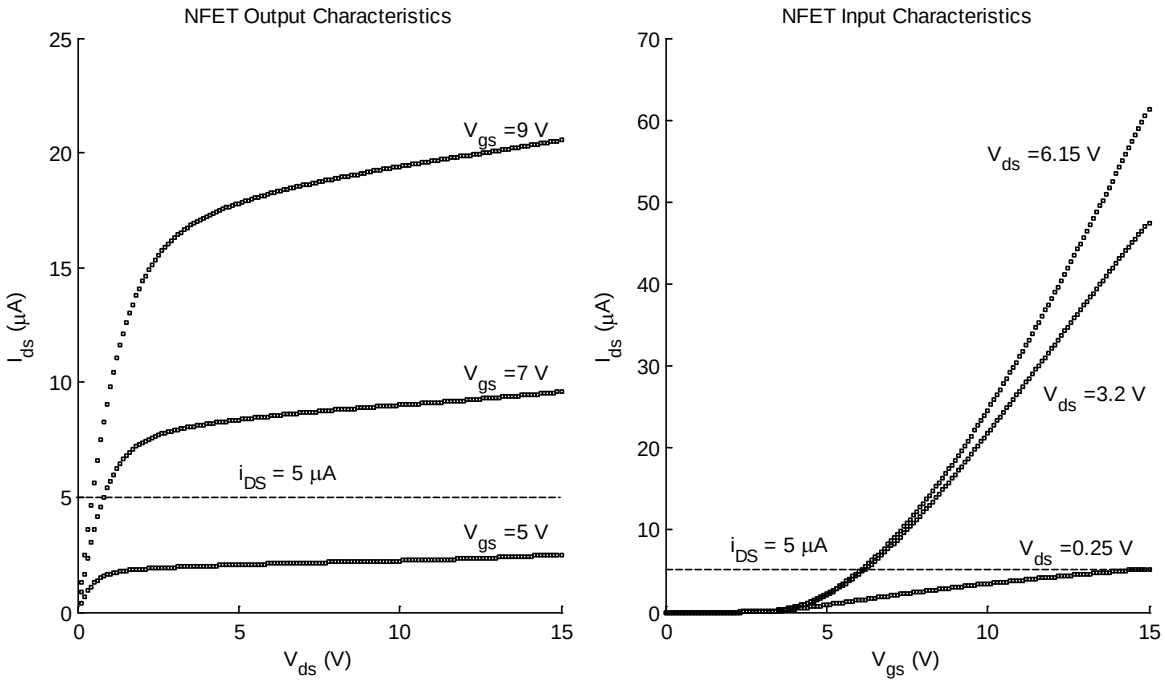


Fig. 3.8. Selection of NFET Bias Current for W/L = 20 μm / 2 μm device.

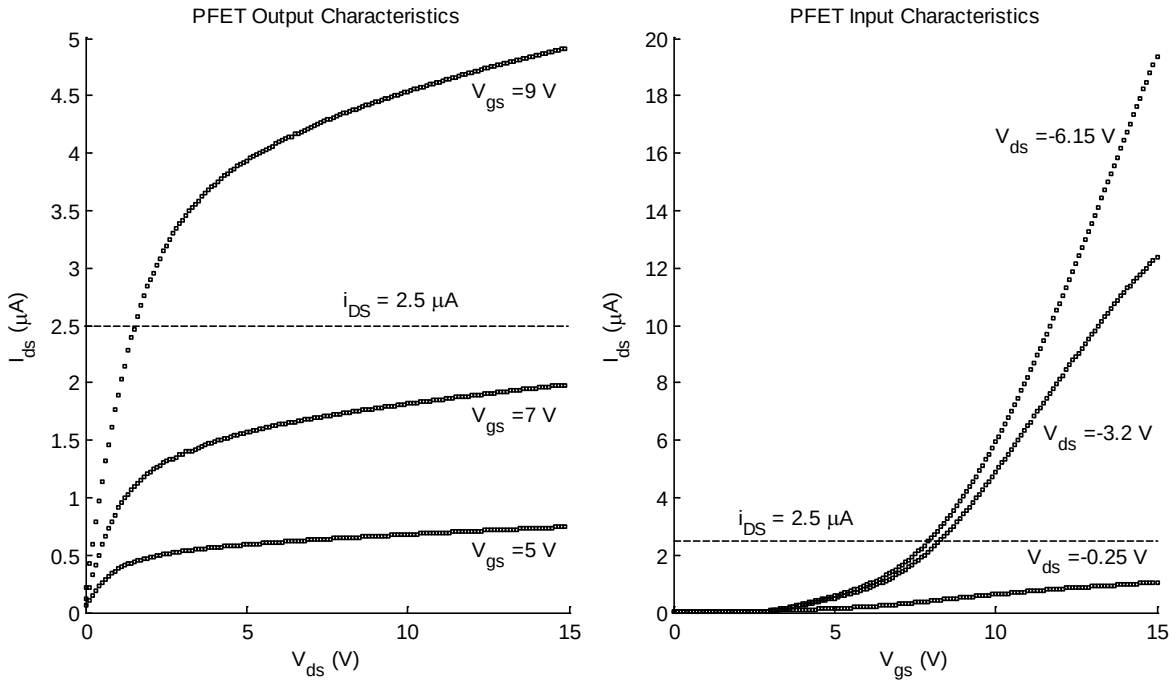


Fig. 3.9. Selection of PFET Bias Current for W/L = 20 µm / 2 µm device.

In Baker's *CMOS: Circuit Design, Layout, and Simulation*, the author recommends choosing v_{DS},*sat* equal to 5% of VDD, which for this process would be 750 mV [40]. Alternately, calculating $v_{DS,sat}$ using Eq. (3.7), yields an approximate value of 707 mV for the chosen current.

$$v_{DS,sat} \approx \sqrt{\frac{i_D}{k'}\frac{L}{W}} \tag{3.7}$$

The resulting standard device operating points, including a set of bias points for W/L = 20 µm / 5 µm devices is shown in Table III. This is analogous to Table 9.1 in Baker's text [40]. Although the self-gain, $g_m r_o$, of the L = 5 µm devices is significantly higher than the L = 2 µm devices, the order of magnitude increase in the gate area to achieve the same bias current causes a significant reduction in the transition frequency, f_T, so the L = 5 µm devices are unsuitable for any applications requiring transient performance.

TABLE III.
HTSIC MOSFET PARAMETERS FOR GENERAL ANALOG DESIGN

Parameter	**NFET 20µm / 2µm**	**PFET 20µm / 2µm**	**NFET 20µm / 5µm**	**PFET 20µm / 5µm**
Bias Current	5 µA			
W/L	20/2	40/2	60/5	160/5
m	1	2	3	8
$V_{DS,sat}$, $V_{SD,sat}$	707 mV	707 mV	745 mV	722 mV
V_{GS},V_{SG}	3.56 V	4.16 V	3.65 V	4.37 V
V_t	2.85 V	2.90 V	3.45 V	3.65 V
k'	1.0 µA/V^2	0.5 µA/V^2	0.75 µA/V^2	0.3 µA/V^2
C'_{ox}	0.86 fF / µm^2			
C_{ox}	34.5 fF	69.0 fF	259 fF	690 fF
C_{gsn},C_{sgp}	23 fF	46.0 fF	173 fF	460 fF
C_{gdn},C_{dgp}	11.5 fF	23.0 fF	86.3 fF	230 fF
g_m	10 µA/V	10 µA/V	9.5 µA/V	9.8 µA/V
r_o	15.4 MΩ	16.7 MΩ	33.3 MΩ	50.0 MΩ
$g_m r_o$	154 V/V	167 V/V	316 V/V	490 V/V
λ	0.013	0.012	0.006	0.004
f_T	69.2 MHz	34.6 MHz	8.73 MHz	3.39 MHz

3.3 An Improved Shichman-Hodges Model for SiC MOSFETs

Although successful design work has been presented with the existing hand-design models, there is still a need for a hand-design model with more fidelity. Current models are

limited to a single bias-point, meaning that they are not very useful for large-signal analysis. The rest of this chapter will be dedicated to improvements in the existing Shichman-Hodges model.

Before formulating an improved model for hand-design using SiC MOSFETs, it is important to explicitly state goals for an optimal hand-design model:

1. A solution should exist for each variable. The equation(s) should have a directly computable equation for each individual terminal voltage or current given all of the other terminal voltages and currents.
2. An expression for the partial derivative with respect to gate-source or drain-source voltage (g_m and r_o) should exist and fulfill criteria number 1.
3. If piecewise-defined functions are necessary (such as in Shichman-Hodges), it should be possible to determine if the correct region of operation was assumed *a posteriori*.

It will be seen that this is quite a strict set of criteria, and fidelity must often be sacrificed to achieve these goals. The first and second goals are necessary to avoid an open-ended "guess and check" approach to circuit design. In hand design, iterative design approaches with more than two or three cycles can become unwieldy, and should be avoided. The 2nd goal is also critical since hand-design work often starts with a desired small-signal specification, and uses the partial derivatives to select terminal voltages and bias currents. On the other hand, the third goal, which does allow for an iterative approach in hand design, is acceptable because the state of operation (triode or saturation) is usually a binary choice, and is always limited to a finite number of possible choices. This limits the maximum number of recalculations that may have to be done during a hand-design procedure.

These goals also stand in contrast to the requirements for models used for computer simulation. Simulation tools implement iterative algorithms which often take several attempts at determining all terminal voltages. Although this may be costly, it is not prohibitive since the computer can perform calculations quickly. Therefore, the first requirement does not apply to computer simulation tools, although model equations which can be solved for any variable will improve simulation speed and convergence.

3.4 Summary of Relevant Short Channel Behaviors for SiC MOSFETs

Although SiC MOSFETs do not exhibit velocity saturation, they do commonly exhibit several other behaviors which are commonly categorized as "short-channel". First and foremost, nearly all device parameters show a dependence on length. Beyond this, SiC devices may exhibit mobility reduction, a saturation voltage different than the overdrive voltage, and a lambda that varies with drain-source voltage.

3.4.1 Mobility Reduction

Mobility reduction is a well-documented and understood phenomenon. The observed mobility of a device may be reduced with increasing gate voltage. The physical explanation is that, with increasing gate voltage, the charge carriers in the channel become more concentrated close to the channel-oxide interface. Surface scattering due to surface roughness becomes more significant, thereby reducing the average carrier velocity and effective mobility [15]. When used in the Shichman-Hodges equations, the effective mobility, μ_{eff}, simply replaces the standard mobility, μ_0, and it is defined as:

$$\mu_{eff} = \frac{\mu_0}{1+\theta(v_{GS}-V_t)} \qquad (3.8)$$

This effect has been described for 6H-SiC MOSFETs [47] in the past. Further, it makes sense that it could be significant in SiC MOSFETs since the coulombic scattering occurs due to SiO_2-SiC interface traps common in SiC semiconductors.

In practice, mobility reduction should be suspected when saturated devices appear to have a power-law dependence on v_{GS}-V_t that is less than square (square-law behavior being a fundamental feature of Shichman-Hodges):

$$i_D \propto (v_{GS} - V_t)^{\alpha}, 1 < \alpha < 2 \qquad (3.9)$$

The mobility reduction coefficient, θ, varies from 0 (having no effect) to a value large enough such that $1+\theta(v_{gs}\text{-}V_t) \approx (v_{gs}\text{-}V_t)$. Although mathematically, these are not equivalent, they will tend to push the equation in the same direction, making the power-law test a good check to see if mobility reduction may be a significant device effect.

Only the NFETs fit prior to the second tapeout benefitted from the inclusion of mobility reduction. Both NFETs and PFETs from the first tapeout, as well as the PFETs from Tapeout 2 were fit with θ values of 0.001 or less, indicating no effect. The NFETs which did benefit from the θ parameter were observed to have the largest interface state trap density as well.

The results of fitting θ for the tapeout 2 NFETs can be seen in Fig. 3.10. Although an improvement is visible from v_{GS} = 7 V and up, at v_{GS} = 5 V the fit without mobility reduction is better. This is likely due to the fact that both fits assume V_t is fixed, when, in reality, it changes significantly when v_{GS} is low. Ultimately, the value of using mobility reduction for this process is low.

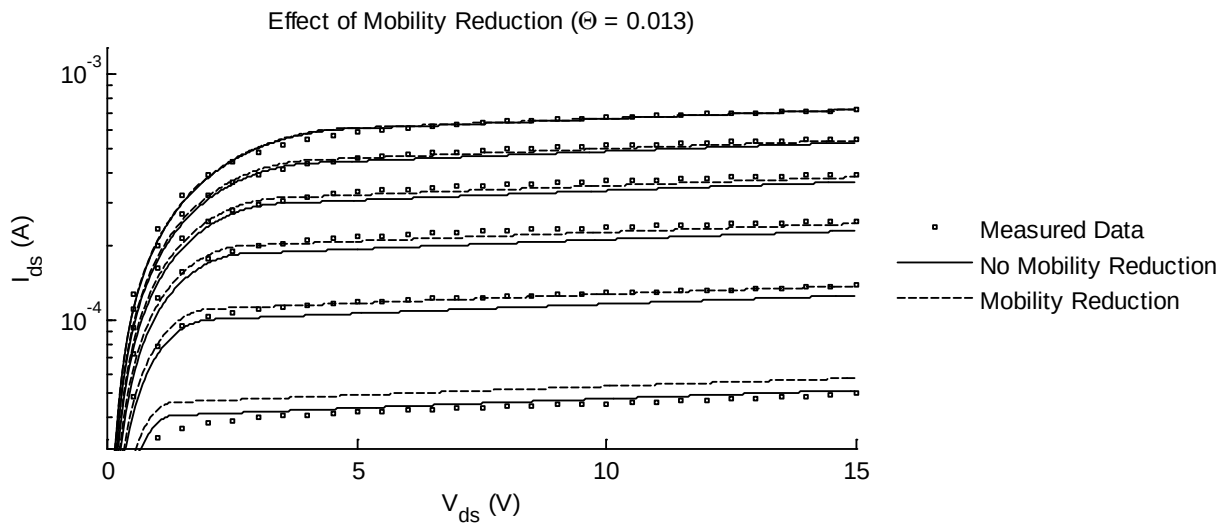


Fig. 3.10. Effect of mobility reduction on curve fitting for NFETs for tapeout 2 with v_{gs}=5, 7, 9, 11, 13, and 15 V. Some improvement in fitting is visible from 7 V and up, but at 5 V, the fit without mobility reduction is better.

3.4.2 Bulk Charge Effect

The onset of saturation at a drain-source voltage less than the overdrive voltage is a common effect in short-channel MOSFETs [48], [49]. It is physically a second order effect of the body effect, and arises due to the fact that the voltage along the length of the device channel is not constant and equal to the source voltage. The body effect can often be avoided by tying the local substrate to the device source to keep V_{BS} equal to 0. Since the channel voltage is not constant, the body effect will actually impact the device behavior despite the body-source tie, and this results in the bulk charge effect. Functionally, the bulk charge effect leads to a reduction in the drain-source voltage where saturation begins, and mathematically, this is represented as:

$$v_{DS,sat} = \frac{v_{GS}-V_t}{A_{bulk}} \qquad (3.10)$$

The bulk-charge effect is derived in the triode region because it requires an integral along the length of the channel from the source to the drain. Attempting to formulate and solve this

integral in a pinched-off channel would be needlessly complex. To obtain the saturation equation incorporating the bulk-charge effect, the triode equation with A_{bulk} and saturation equation with A_{bulk} are set equal to each other, and v_{DS} is replaced with $v_{DS,sat}$. Then, the saturation equation is modified to make the equality correct.

$$i_D = \mu_0 C'_{ox} \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - A_{bulk}\frac{v_{DS}^2}{2}\right], v_{DS} < \frac{v_{GS}-V_t}{A_{bulk}} \qquad (3.11)$$

$$\mu_0 C'_{ox} \frac{W}{L}\left[\frac{(v_{GS}-V_t)^2}{A_{bulk}} - \frac{(v_{GS}-V_t)^2}{2A_{bulk}}\right] = \frac{\mu_0 C'_{ox}}{2}\frac{W}{L}(v_{GS} - V_t)^2\left[1 + \lambda\left(v_{DS,sat} - v_{DS,sat}\right)\right] \qquad (3.12)$$

As can be seen, Eq. (3.12) is incorrect until the right side is divided by A_{bulk}. Leaving the correct saturation and triode equations:

$$i_D = \begin{cases} \frac{\mu_0 C'_{ox}}{2A_{bulk}}\frac{W}{L}[(v_{GS} - V_t)^2(1 + \lambda v_{DS})] & v_{DS} \geq \frac{v_{GS}-V_t}{A_{bulk}} \\ \mu_0 C'_{ox}\frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - A_{bulk}\frac{v_{DS}^2}{2}\right](1 + \lambda v_{DS}) & v_{DS} < \frac{v_{GS}-V_t}{A_{bulk}} \end{cases} \qquad (3.13)$$

The improvement in fitting of SiC MOSFETs by including the bulk charge effect is shown Fig. 3.11. The curve shown is for a v_{GS} of 15 V. At this gate voltage, the traditional Shichman-Hodges equations predict saturation at a much higher voltage than is shown in the data.

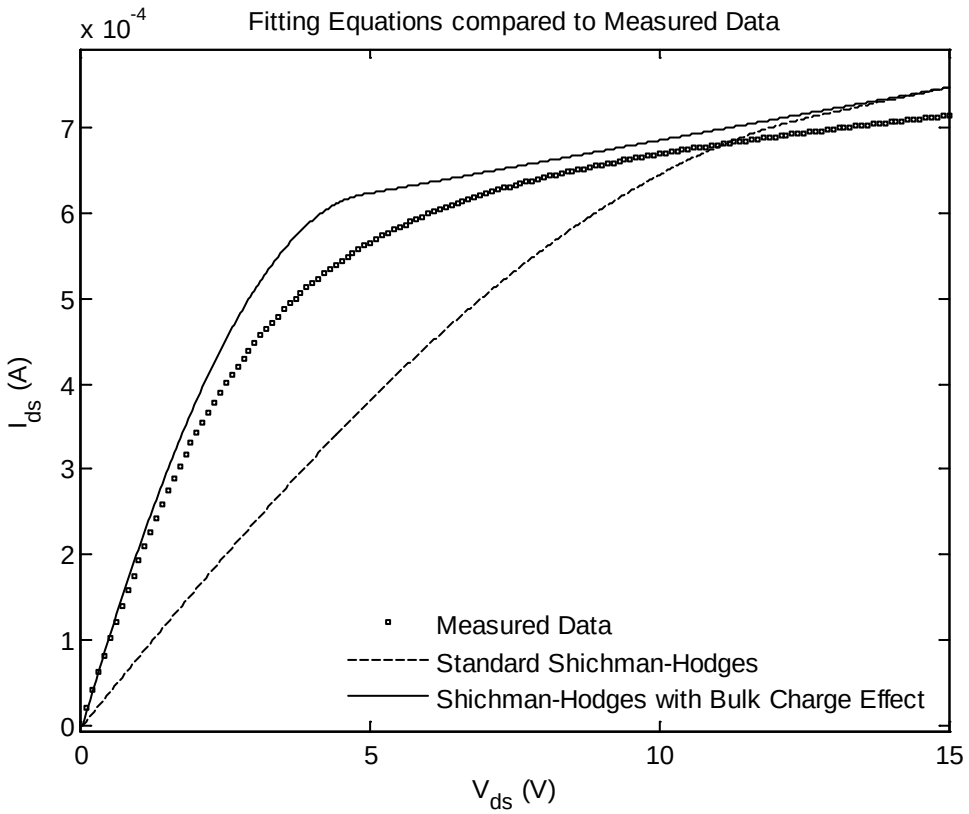


Fig. 3.11. Improvement in device fitting with the addition of the bulk charge effect.

3.4.3 Soft Saturation

Although the addition of the bulk charge effect makes a significant improvement in the accuracy of the equation, the measured devices do not show a clear point of transition between the triode region and the saturation region. This behavior is also seen in short-channel MOSFETs and is modeled in the BSIM3v3 and later models [49]. Although this is a useful feature, it is actually only a side effect of a more important property for simulation models. In these models, a single equation with infinite continuous derivatives is critical for stable simulations. The BSIM3v3 (and later) model equations were formulated with this goal in mind, but the result is a single equation (3.14) which accounts for both triode and saturation behaviors. It does this

through the $v_{DS,eff}$ term, which is nearly equal to v_{DS} at sufficiently small values, nearly equal to $_{VGS}$-V_t at sufficiently large values, and has a smooth transition between the two behaviors. The smoothing parameter, δ, controls how quickly the transition between behaviors occurs. It is important to note that these equations are not the complete model, and do not represent channel modulation and several other important effects.

$$i_D = \mu_0 C'_{ox} \frac{W}{L}\left[(v_{GS} - V_t) * \boldsymbol{v_{DS,eff}} - \frac{A_{bulk}}{2}\boldsymbol{v_{DS,eff}^2}\right] \quad (3.14)$$

$$\boldsymbol{v_{DS,eff}} = \boldsymbol{v_{DS,sat}} - \frac{1}{2}\left[\boldsymbol{v_{DS,sat}} - v_{DS} - \delta + \sqrt{\left(\boldsymbol{v_{DS,sat}} - v_{DS} - \delta\right)^2 + 4\delta\boldsymbol{v_{DS,sat}}}\right] \quad (3.15)$$

$$\boldsymbol{v_{DS,sat}} = \frac{v_{GS} - V_t}{A_{bulk}} \quad (3.16)$$

Several algebraic steps can simplify further analysis of this equation. Going beyond replacing the v_{GS}-V_t term with v_{OV}, it can be written as $A_{bulk}v_{DS,sat}$ and the equation simplified:

$$i_D = A_{bulk}\mu_0 C'_{ox} \frac{W}{L}\left[v_{DS,sat} - \frac{v_{DS,eff}}{2}\right] v_{DS,eff} \quad (3.17)$$

$$\boldsymbol{v_{DS,eff}} = \frac{1}{2}\left[v_{DS} + \delta - v_{DS,sat} + \sqrt{\left(v_{DS,sat} - v_{DS} - \delta\right)^2 + 4\delta v_{DS,sat}}\right] \quad (3.18)$$

Eq. (3.17) is not computationally too complex for hand-design work, but inserting Eq. (3.18) and solving is problematic. Instead of using a single continuous and infinitely differentiable equation as in the BSIM family of models, the method proposed here is to increase the complexity of the channel modulation term only in the saturation equation. The result provides a significant improvement in the accuracy of the model, while requiring only a modest increase in the algebraic complexity.

3.4.4 Nonlinear Channel Modulation

In all variations on the Shichman and Hodges model described up to this point, the channel modulation term was a first-order polynomial, either $1+\lambda v_{DS}$ or $1+\lambda(v_{DS}-v_{DS,sat})$. One of the particularly useful features of the model is that the saturation equation is easily separable into components which depend upon v_{DS} and v_{GS} only, and not a combination of the two. This is particularly important in calculating g_m and r_o. As was shown in the last section, the smoothing between triode and saturation removes this feature. In lieu of this, a modified channel modulation term which is not a first-order polynomial is described here. This approach has the benefit of maintaining the separability in the Shichman-Hodges saturation equation.

In their original work, this term is added to both the triode and saturation equations, which has the benefit of making the first derivative of these equations continuous at the boundary. In most modern texts, the standard channel-length modulation term is $1+\lambda(v_{DS}-v_{DS,sat})$ and is only present in the saturation equation. This approach has the benefit of more correctly modeling the physics, since channel length modulation should not occur before channel pinch-off occurs. Up until this point, the original Shichman-Hodges channel-length modulation formulation has been used to maintain a continuous first derivative, but the new formulation makes that impossible, as will be shown, and the more modern method of only including channel-length modulation in the saturation equation will be used going forward.

The proposed nonlinear channel modulation model adds an exponential coefficient, γ, to the standard model, which will be called the *channel modulation nonlinearity coefficient*. The modulation term then becomes:

$$1 + \lambda(v_{DS} - v_{DS,sat}) \rightarrow 1 + \lambda\left(v_{DS} - v_{DS,sat}\right)^{\gamma} \qquad (3.19)$$

Experimentation showed that using a common term and applying to both triode and saturation equations did not improve fitting results, but applying it only to the saturation region provided a significant improvement in fitting accuracy. The complete saturation equation including nonlinear channel modulation is shown in Eq. (3.20), and the improved fitting results are shown in Fig. 3.20.

$$i_D = \frac{\mu_0 C'_{ox}}{2A_{bulk}} \frac{W}{L} (v_{GS} - V_t)^2 \left[1 + \lambda \left(v_{DS} - \frac{v_{GS}-V_t}{A_{bulk}}\right)^{\gamma}\right] \quad v_{DS} \geq \frac{v_{GS}-V_t}{A_{bulk}} \qquad (3.20)$$

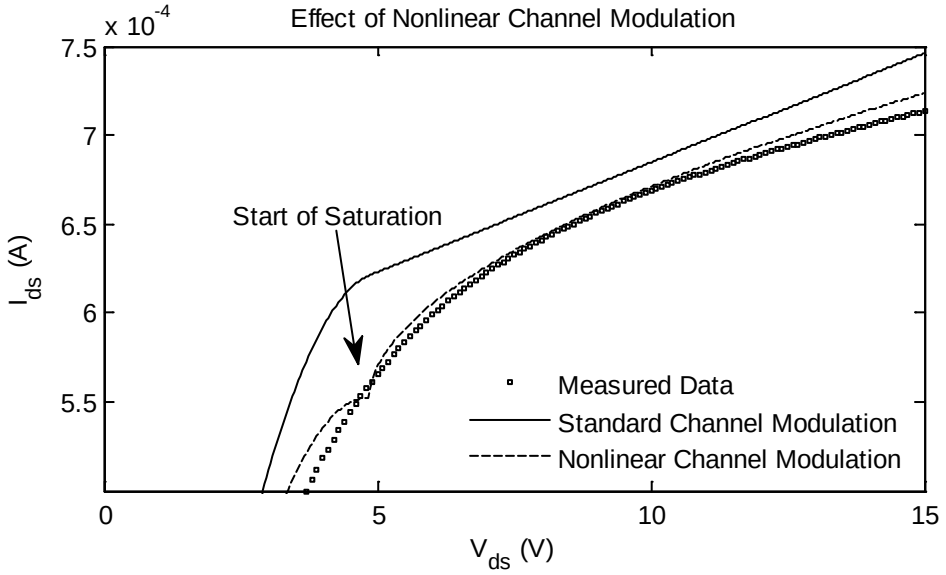


Fig. 3.12. Comparison of nonlinear channel modulation model with linear channel modulation model and measured data from the tapeout 1 NFETs.

A brief inspection of Fig. 3.12 shows that the fitting of the equation is much better across both the saturation and triode regions, but the slope of the saturation region, which determines the device r_o, is still not as precise as might be desired. Close to the saturation/triode transition point, the equation has a larger slope, and therefore reduced output resistance, relative to the

measured data. On the contrary, the standard channel modulation model will significantly over-predict both the output resistance and the output current. So the nonlinear channel modulation model will still provide a significant improvement over the standard model. It must be noted that the nonlinear model leads to a calculated output resistance of infinity in the triode equation. This is a disadvantage relative to the original Shichman-Hodges channel modulation, but is the same as the modern formulation of the linear model.

3.5 Large- and Small-Signal Equations

The resulting large-signal equations, including mobility reduction, body-charge effect, and nonlinear channel modulation are:

$$i_D = \begin{cases} \frac{\mu_{eff} C'_{ox}}{2A_{bulk}} \frac{W}{L} (v_{GS} - V_t)^2 \left[1 + \lambda \left(v_{DS} - v_{DS,sat}\right)^{\gamma}\right] & v_{DS} \geq v_{DS,sat} \\ \mu_{eff} C'_{ox} \frac{W}{L} \left[(v_{GS} - V_t) v_{DS} - A_{bulk} \frac{v_{DS}^2}{2}\right] & v_{DS} < v_{DS,sat} \end{cases} \quad (3.21)$$

$$\mu_{eff} = \frac{\mu_0}{1 + \theta(v_{GS} - V_t)} \quad (3.22)$$

$$v_{DS,sat} = \frac{v_{GS} - V_t}{A_{bulk}} \quad (3.23)$$

The small-signal equation for g_m in saturation has an additional term since μ_{eff} is a function of v_{GS}.

$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \frac{\mu_0 C'_{ox}}{2A_{bulk}} \frac{W}{L} \left[\frac{2(v_{GS} - V_t)}{1 + \theta(v_{GS} - V_t)} - \frac{\theta(v_{GS} - V_t)^2}{\left(1 + \theta(v_{GS} - V_t)\right)^2}\right] \left[1 + \lambda \left(v_{DS} - v_{DS,sat}\right)^{\gamma}\right]$$

(3.24)

Through linearization, the terms v_{GS}, $(v_{DS} - v_{DS,sat})$, and λ are considered to be small relative to other terms, and any terms which contain a product of two small terms are dropped. In this case, the $\lambda(v_{DS} - v_{DS,sat})^{\gamma}$ term is dropped, and the equation can be manipulated to develop a familiar form.

$$g_m \approx \frac{\mu_0 C'_{ox}}{2A_{bulk}} \frac{W}{L} \left[\frac{2(v_{GS}-V_t)+2\theta(v_{GS}-V_t)^2}{\left(1+\theta(v_{GS}-V_t)\right)^2} - \frac{\theta(v_{GS}-V_t)^2}{\left(1+\theta(v_{GS}-V_t)\right)^2} \right] \tag{3.25}$$

$$g_m \approx \frac{\mu_0 C'_{ox}}{2A_{bulk}} \frac{W}{L} \left[\frac{2(v_{GS}-V_t)+\theta(v_{GS}-V_t)^2}{\left(1+\theta(v_{GS}-V_t)\right)^2} \right] \tag{3.26}$$

$$g_m \approx \frac{\mu_0 C'_{ox}}{A_{bulk}} \frac{W}{L} \frac{(v_{GS}-V_t)}{\left(1+\theta(v_{GS}-V_t)\right)^{1/2}} \left[\frac{1+{}^1\!/_2\,\theta(v_{GS}-V_t)}{\left(1+\theta(v_{GS}-V_t)\right)^{3/2}} \right] \tag{3.27}$$

$$g_m \approx \frac{\sqrt{\mu_0}\sqrt{\mu_{eff}} C'_{ox}}{A_{bulk}} \frac{W}{L} (v_{GS} - V_t) \left[\frac{1+{}^1\!/_2\,\theta(v_{GS}-V_t)}{\left(1+\theta(v_{GS}-V_t)\right)^{3/2}} \right] \tag{3.28}$$

$$g_m \approx \sqrt{\frac{2\mu_0 C'_{ox}}{A_{bulk}} \frac{W}{L} i_D} \left[\frac{1+{}^1\!/_2\,\theta(v_{GS}-V_t)}{\left(1+\theta(v_{GS}-V_t)\right)^{3/2}} \right] \tag{3.29}$$

When θ is zero, the additional term on the right side reduces to 1, and the resulting formula is almost identical to the traditional formula for transconductance. The added term A_{bulk} is the only difference. In understanding SiC MOSFETs, it is generally more convenient to define the terms k' and β including the bulk charge effect:

$$k' = \frac{\mu_0 C'_{ox}}{A_{bulk}} \tag{3.30}$$

$$\beta = \frac{\mu_0 C'_{ox}}{A_{bulk}} \frac{W}{L} \tag{3.31}$$

The formulation of the output resistance is slightly more complex. It is useful to define the *excess saturation current*, Δi_D, as the difference between the actual drain current and the drain current when the device is just at saturation ($v_{DS} - V_{DS,sat}$ equal to zero):

$$\Delta i_D = i_D - i_D|^{v_{ds}=V_{ds,sat}} \tag{3.32}$$

$$i_{D,sat} = \frac{\mu_{eff} C_{ox}^{'}}{2A_{bulk}} \frac{W}{L} (v_{GS} - V_t)^2 \tag{3.33}$$

$$\Delta i_D = i_{D,sat}\left[1 + \lambda\left(v_{DS} - V_{DS,sat}\right)^{\gamma}\right] - i_{D,sat} = i_{D,sat}\lambda\left(v_{DS} - V_{DS,sat}\right)^{\gamma} \tag{3.34}$$

$$\Delta i_D = \frac{\mu_{eff} C_{ox}^{'}}{2A_{bulk}} \frac{W}{L} (v_{GS} - V_t)^2 \lambda\left(v_{DS} - V_{DS,sat}\right)^{\gamma} \tag{3.35}$$

$$\Delta i_D \approx i_D \lambda\left(v_{DS} - V_{DS,sat}\right)^{\gamma} \tag{3.36}$$

Where Eq. (3.36) is obtained through linearization. In this case the product of two small terms that is dropped is $\lambda^2(v_{DS} - V_{DS,sat})^{2\gamma}$. The goal of defining Δi_D is that it can be estimated during bias point calculations, and eases the calculation of the device output resistance. The output resistance is:

$$\frac{\partial i_D}{\partial v_{DS}} = \frac{\mu_{eff} C_{ox}^{'}}{2A_{bulk}} \frac{W}{L} (v_{GS} - V_t)^2 \lambda\gamma\left(v_{DS} - V_{DS,sat}\right)^{\gamma-1} \tag{3.37}$$

$$r_o = \frac{\partial v_{DS}}{\partial i_D} = \frac{v_{DS} - V_{DS,sat}}{\frac{\mu_{eff} C_{oxW}^{'}}{2A_{bulk}} \frac{L}{L} (v_{GS} - V_t)^2 \lambda\gamma\left(v_{DS} - V_{DS,sat}\right)^{\gamma}} \tag{3.38}$$

The final step of determining r_o is to combine the definition of the excess saturation current in Eq. (3.36) with Eq. (3.38). The result leaves only γ and i_D in the denominator,

and again has the advantage of reducing to the standard Shichman-Hodges form of r_o when γ is set to 1.

$$r_o = \frac{v_{DS} - v_{DS,sat}}{\Delta i_D \gamma} \approx \frac{1}{i_D \lambda \gamma \left(v_{DS} - v_{DS,sat}\right)^{\gamma - 1}} \qquad (3.39)$$

The final result, shown in Eq. (3.39), provides several ways to calculate the output resistance, depending on which bias point parameters are available. An important note is that each of these equations; large-signal (Eqs. (3.21)-(3.23)), transconductance (Eq. (3.29)) and output resistance (Eq. (3.39)), reduces to the modern standard Shichman-Hodges equations when θ, A_{bulk}, and γ are all set equal to 1. Even more useful is that these effects can be thought of as orthogonal. Each can be utilized as necessary to fit a specific device behavior, without having to commit to either of the others.

3.6 Improved Shichman-Hodges Parameters for HTSiC devices.

The improved model described in the last section was applied to the W = 20 μm, L = 2 μm PFETs and NFETs for both the first and second tapeouts. The model and fitting algorithm was initially developed with data from the tapeout 1 test devices. Once data was available for the tapeout 2 devices, additional development was done on the fitting algorithm. The complete description of the fitting code and algorithm are described more completely in Appendix A, but the simplified version is shown in Fig. 3.13.

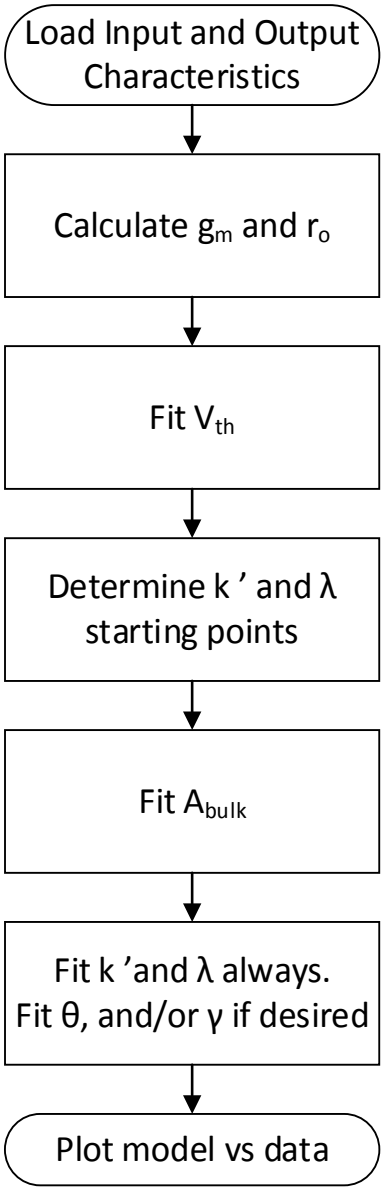


Fig. 3.13 Simplified flowchart of the fitting algorithm.

The two device types had different requirements and challenges. For Tapeout 1, the NFET fitting did not benefit from including mobility reduction, whereas the PFET fitting did not benefit from including the channel modulation nonlinearity coefficient. Only room-temperature data was fit for the Tapeout 1 devices because this was after the first tapeout, and only used to

develop the model and process. The extracted parameters are given in Table IV, and the fits are shown in Fig. 3.14 and Fig. 3.15.

Table IV.
MODIFIED SHICHMAN-HODGES DEVICE PARAMETERS FOR TAPEOUT 1 AT ROOM TEMPERATURE

Parameter	**NFET (W/L = 20 µm / 2 µm)**	**PFET (W/L = 20 µm / 2 µm)**
V_{th} (V)	2.49	5.12
k' ($\mu A/V^2$)	0.91	0.43
λ (V^{-1})	0.095	0.026
A_{bulk}	2.56	1.36
θ (V^{-1})	0 (disabled)	0.05
γ	0.51	1 (disabled)

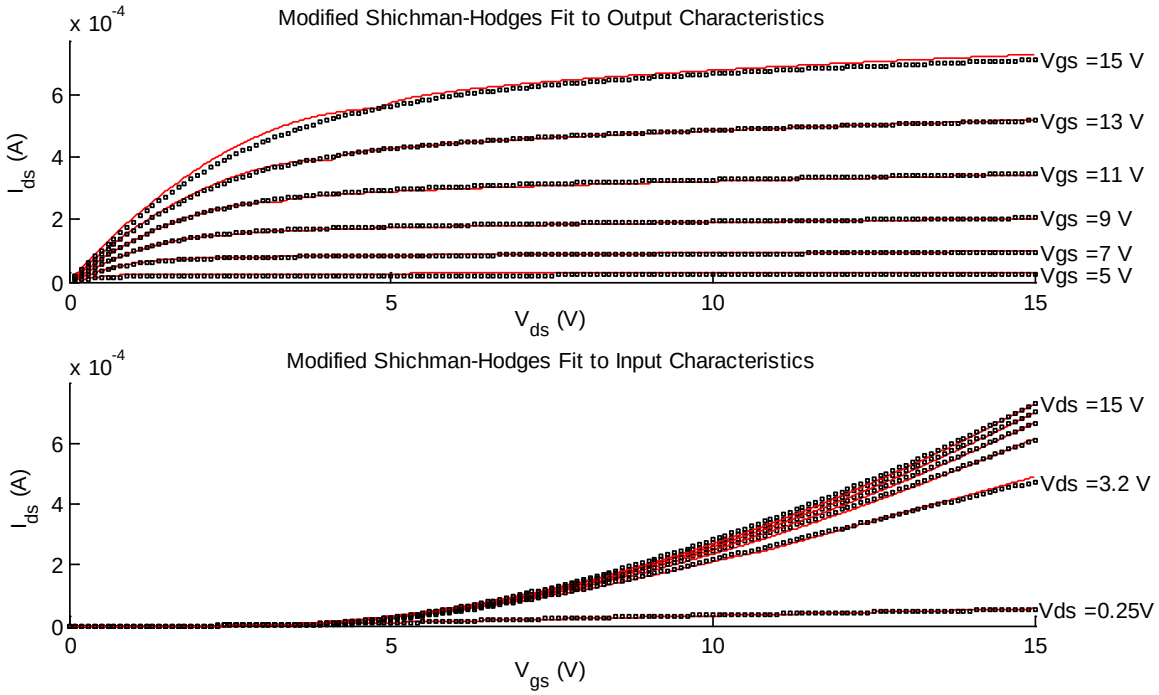


Fig. 3.14. Input and output fits for Tapeout1 NFETs at room temperature.

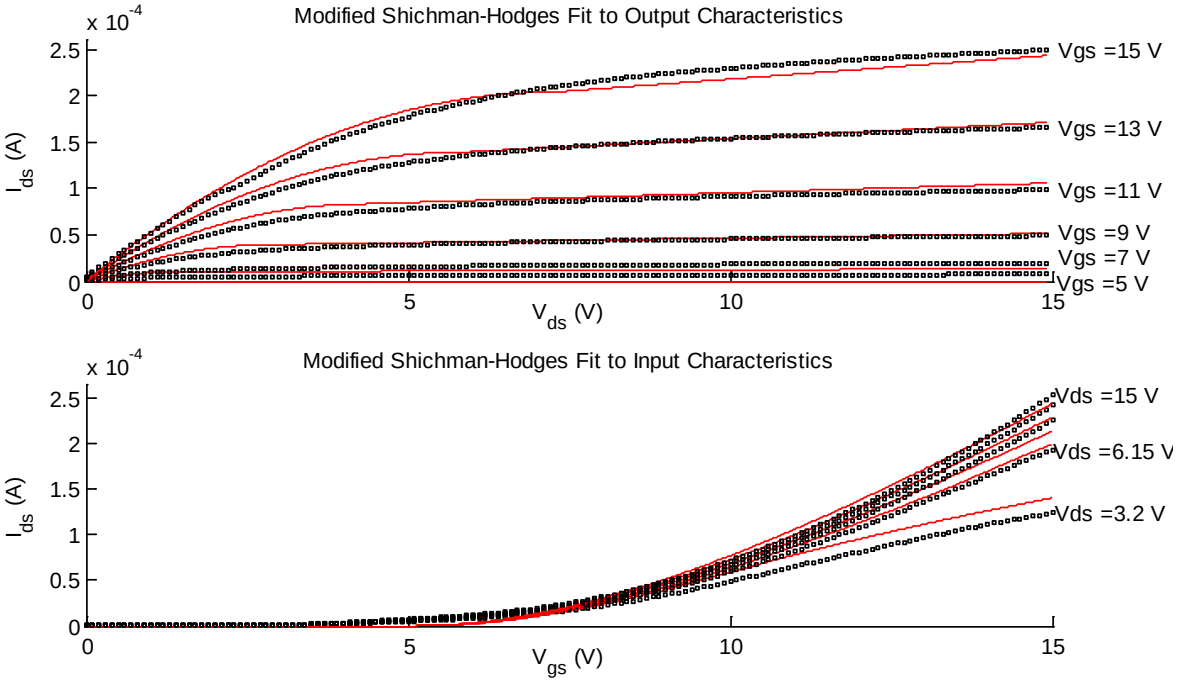


Fig. 3.15. Input and output fits for Tapeout1 PFETs at room temperature. The quality of fit is not as good as the NFETs due to near-threshold leakage of the device.

Although the modified Shichman-Hodges parameters showed great promise in fitting the Tapeout 1 devices, the devices measured for Tapeout 2 demonstrated even more complex behaviors. The body-charge effect was clearly applicable to all devices. For the Tapeout 2 NFETs, mobility reduction was also useful for fitting, but the channel modulation nonlinearity coefficient did not improve fitting results. Fitting results are summarized in Table V, and the fits are shown in Fig. 3.16 and Fig. 3.17.

Table V.
MODIFIED SHICHMAN-HODGES DEVICE PARAMETERS FOR TAPEOUT 2 NFETS WITH W/L = 20 μm / 2 μm ACROSS TEMPERATURE

Parameter	**25 ℃**	**100 ℃**	**200 ℃**	**300 ℃**
V_{th} (V)	1.49	1.39	1.36	1.68
k' ($\mu A/V^2$)	2.08	3.15	2.97	2.42
λ (V^{-1})	0.018	0.017	0.017	0.012
A_{bulk}	2.66	2.51	2.28	2.11
θ (V^{-1})	0.013	0.034	0.028	0.016
γ	1 (disabled)			

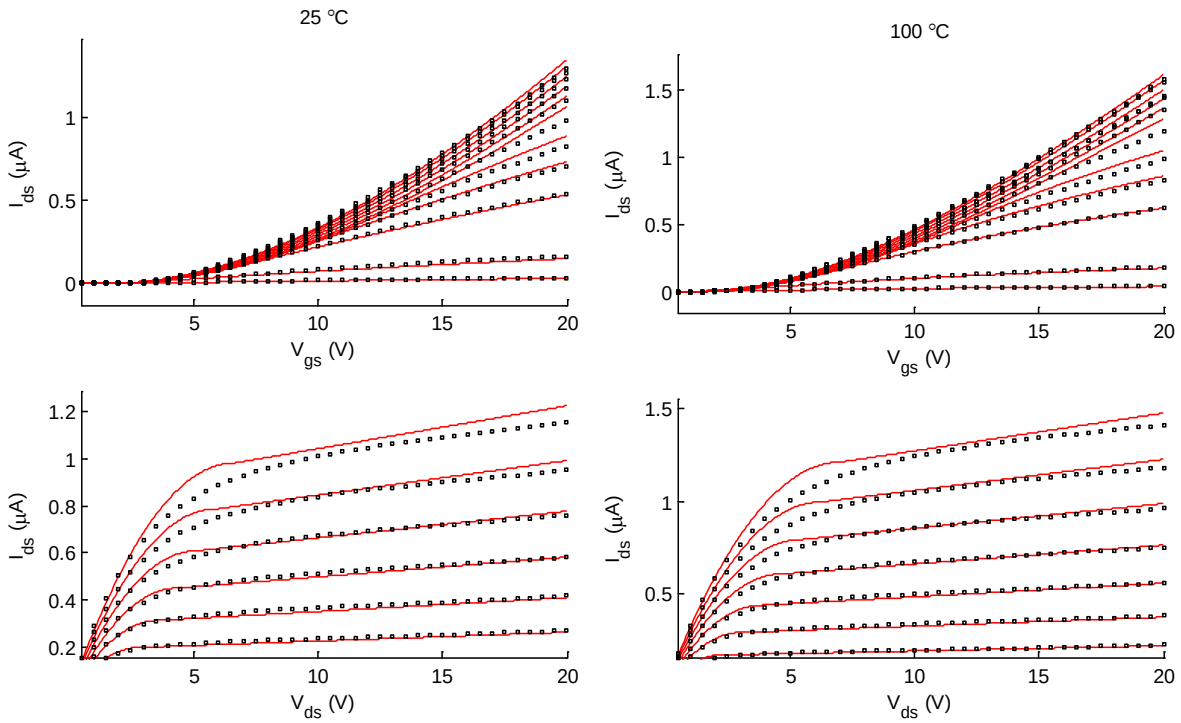


Fig. 3.16. Input and output characteristic fits for Tapeout 2 NFETs with W/L = 20 µm / 2 µm at 25 and 100 °C.

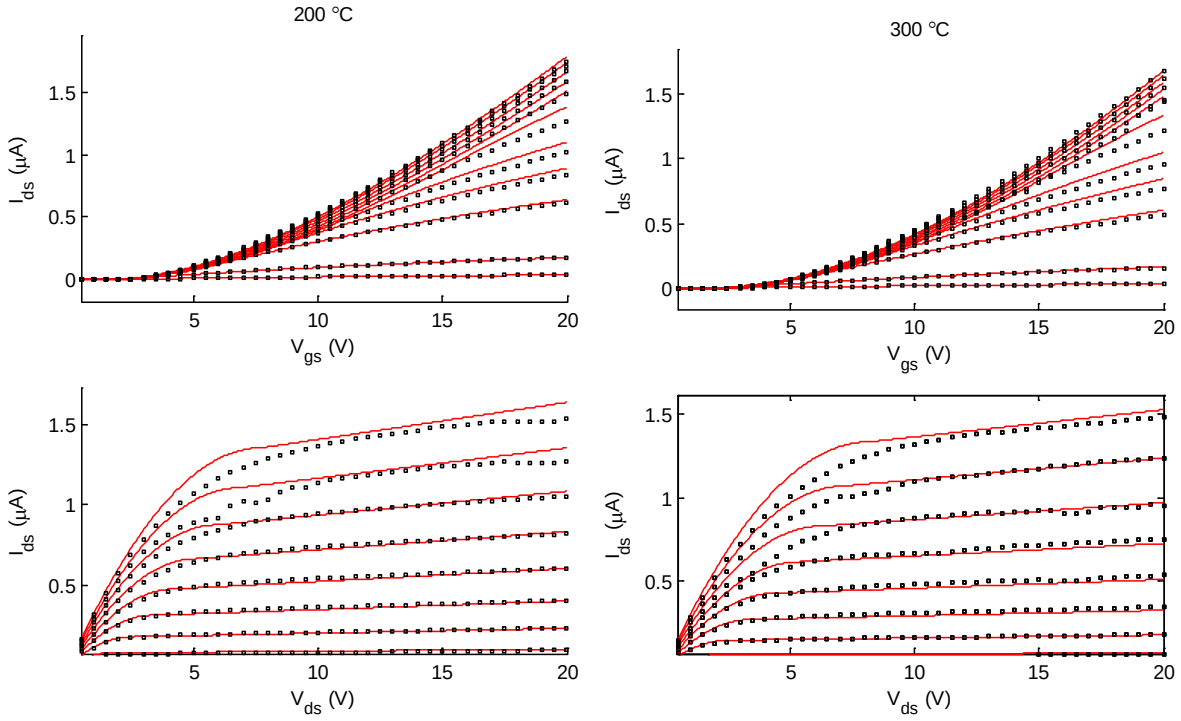


Fig. 3.17. Input and output characteristic fits for Tapeout 2 NFETs with W/L = 20 µm / 2 µm at 200 and 300 °C.

The PFETs for Tapeout 2 were the most difficult to fit with the improved Shichman-Hodges parameters. The algorithm developed to fit threshold voltage did not work for these devices, and including nonlinear channel modulation caused very poor fits (Fig. 3.18). When a constant V_{th} of 7.5 V was assumed, the rest of the fitting algorithm was able to produce much better results across all temperatures, although at 300 ℃ there are still some awkwardly fit regions. Unlike the Tapeout 2 NFETs, mobility reduction was not significant, but nonlinear channel modulation was somewhat useful. This is especially noteworthy since the devices for Tapeout 1 had the opposite relationship between device type and mobility reduction/nonlinear channel modulation. The fitting results are summarized in Table VI.

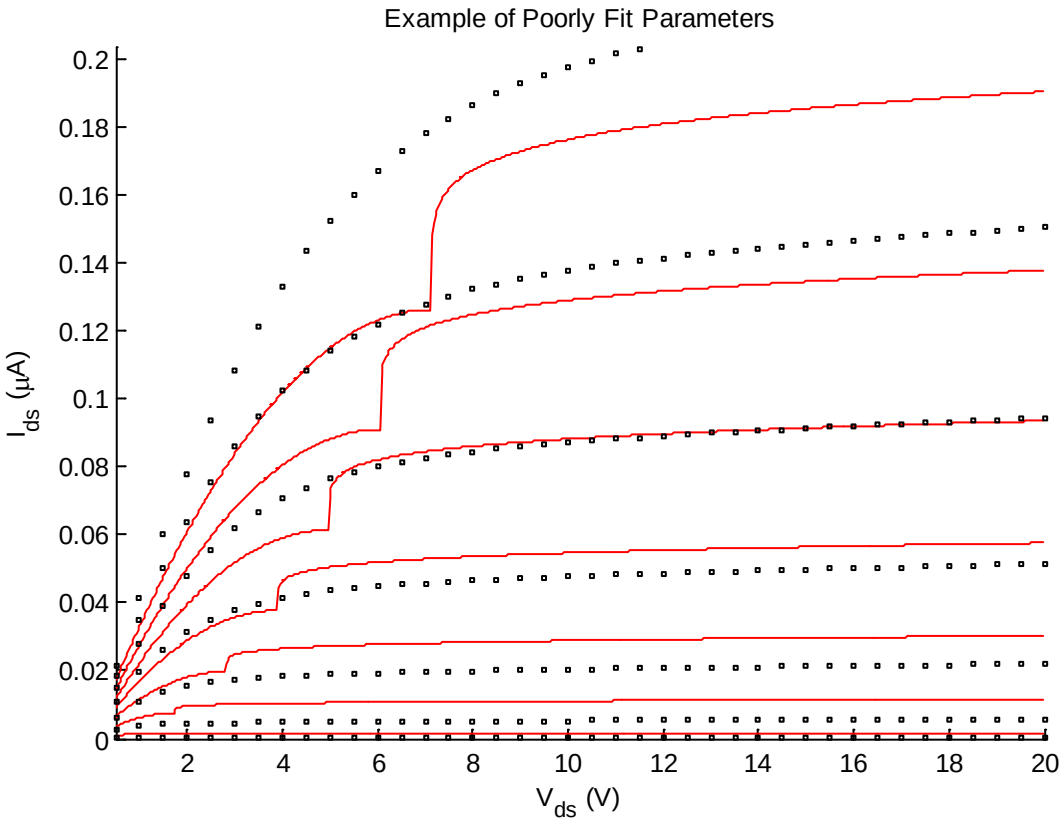


Fig. 3.18. Incorrect selection of threshold voltage causes the fitting algorithm to accentuate γ and generate inappropriate fits.

Table VI.
MODIFIED SHICHMAN-HODGES DEVICE PARAMETERS FOR TAPEOUT 2 PFETS W/L = 20 µm / 2 µm ACROSS TEMPERATURE

Parameter	**25 ℃**	**100 ℃**	**200 ℃**	**300 ℃**
V_{th} (V)	7.5 V			
k' (µA/V^2)	0.45	0.67	0.71	0.41
λ (V^{-1})	0.019	0.019	0.018	0.084
A_{bulk}	1.55	1.66	1.76	2.10
θ (V^{-1})	0 (disabled)			
γ	0.90	0.95	0.93	0.43

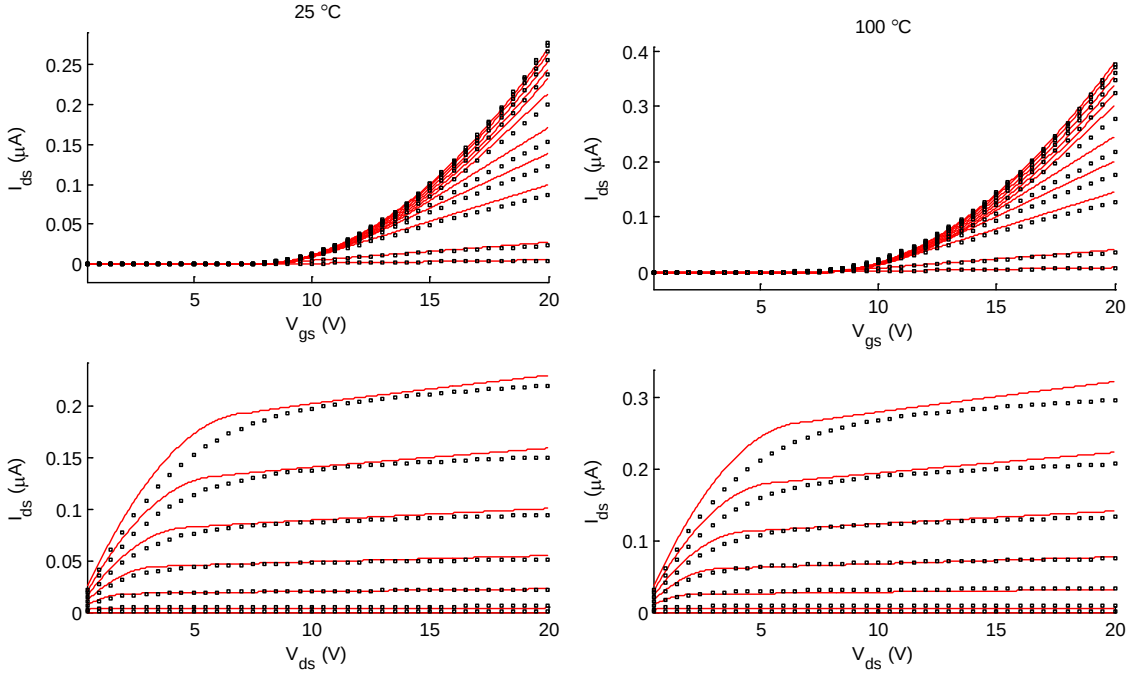


Fig. 3.19. Input and output characteristic fits for Tapeout 2 PFETs with W/L = 20 µm / 2 µm at 25 and 100 ℃.

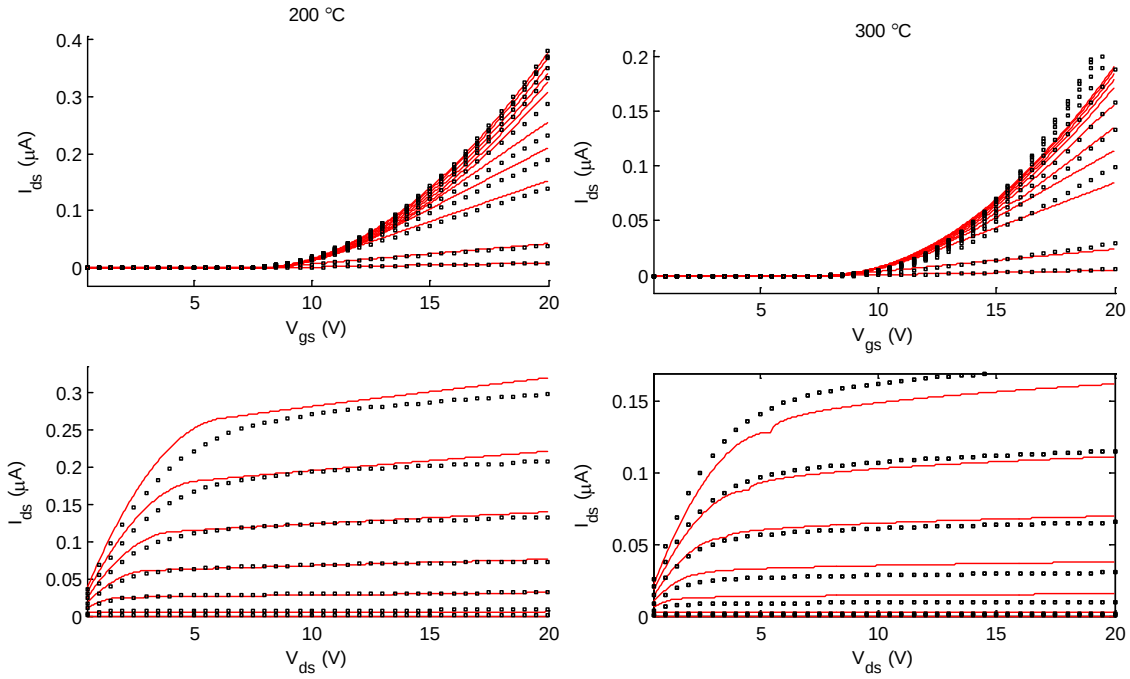


Fig. 3.20. Input and output characteristic fits for Tapeout 2 PFETs with W/L = 20 µm / 2 µm at 200 and 300 °C.

3.7 Design Implications of the Improved Shichman-Hodges Parameters

The features of the improved Shichman-Hodges model are *critical* to effective hand-design efforts in SiC. The example that follows will demonstrate this. More than any other, the addition of A_{bulk} is necessary to identify valid bias points.

Using the traditional Shichman-Hodges model, Baker generally recommends a V_{ov} of 5% of VDD, but a larger amount for high-speed design. Knowing that SiC processes are inherently slow with respect to Si, it is reasonable to select a V_{ov} of 15%, or 2.25 V for a VDD of 15 V. Fig. 3.21 shows a simple difference amplifier used to compare the two models. Table VII shows the Improved Shichman-Hodges parameters fit at 100 °C as well as the traditional Shichman-Hodges parameters fit in a similar manner. The results in Table VII show that with the traditional model and a V_{ov} of 15%, the expected common-mode range is only 0.75 V (5.89 to 6.64 V), or 5% of

VDD! This result would lead the designer to discard this approach out-of-hand, possibly without ever running a simulation.

Using the improved Shichman-Hodges model, which includes A_{bulk}, the common-mode range is predicted to be 4.4 V (from 3.18 to 7.53 V), or nearly 1/3 of VDD. The hand-design equations lead to different PFET multiplicities and bias currents, and the differential gain versus common-mode input voltage for both designs is shown in Fig. 3.22. The calculated common-mode range and gain using the traditional model never crosses the simulated curve, where the improved model provides a much better prediction.

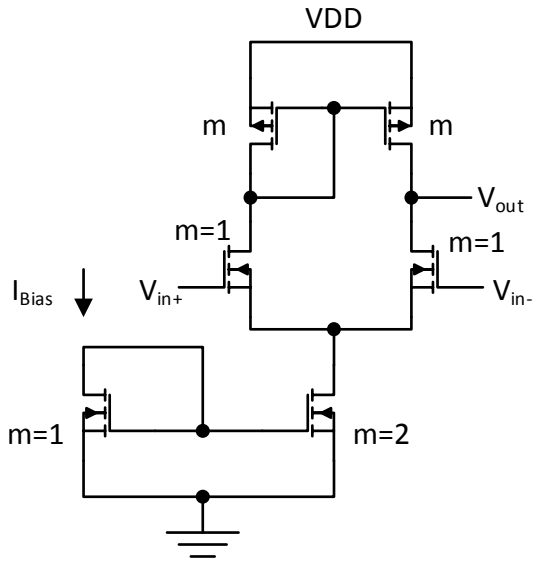


Fig. 3.21. Difference amplifier schematic used to compare the standard and modified Shichman-Hodges models. I_{bias} is stated I_D from the table, and PFET multiplicity, m is given in the table.

Table VII.

COMPARISON OF IMPROVED SHICHMAN-HODGES VS STANDARD SHICHMAN-HODGES PARAMETERS, AND CALCULATED GAIN AND COMMON-MODE RANGE FOR A DIFFERENTIAL AMPLIFIER

	Improved		**Simple**	
	NFET	**PFET**	**NFET**	**PFET**
Vt (V)	1.39	7.5	1.39	7.5
Lambda (V^{-1})	0.017	0.019	0.012	0.006
$k' \frac{W}{L}$ ($\mu A/V^2$)	31.5	6.70	4.40	2.15
Abulk	2.51	1.66	N/A	
θ (V^{-1})	0.034	0		
γ	1	1		
$v_{DS,sat}$ (V)	0.90	1.36	2.25	2.25
v_{GS} (V)	2.29	8.86	3.64	9.75
PFET:NFET k'/A_{bulk}	3.11E+00		2.05E+00	
PFET:NFET Design Ratio	3		2	
Id (μA)	29.5		11.1	
g_m (μA/V)	4.31E-05	1.17E-05	9.90E-06	4.84E-06
r_o (Ω)	1.99E+06	1.72E+06	7.48E+06	1.53E+07
Av (V/V)	39.8		59.5	
CM minimum	3.18		5.89	
CM maximum	7.53		6.64	

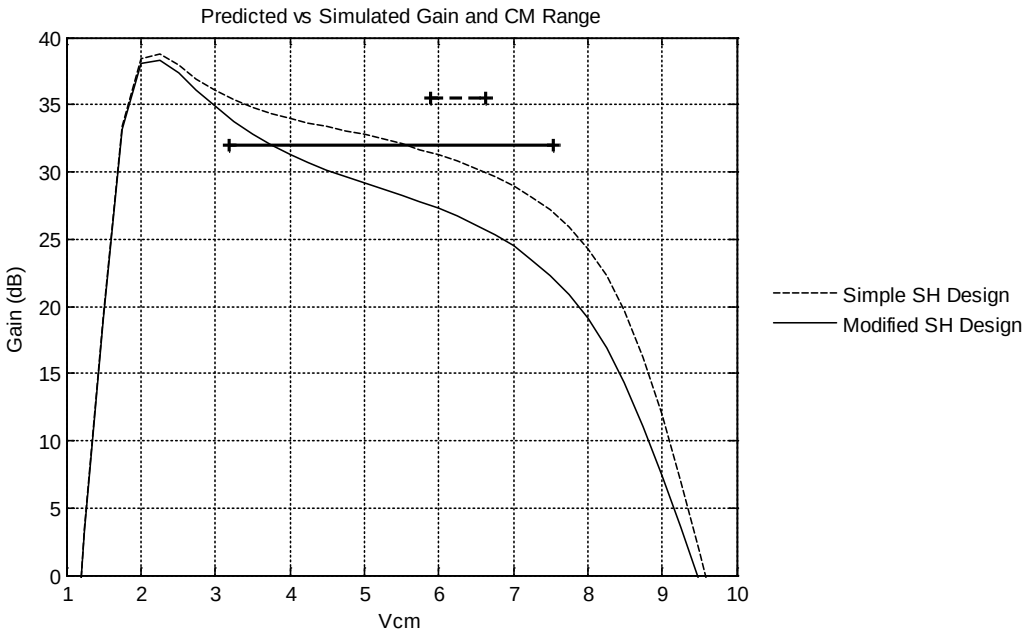


Fig. 3.22. The hand-calculated CM Range and Differential gain (shown with bold lines) is more accurate using the Modified Shichman-Hodges model, but the result provides approximately 4 dB less gain.

CHAPTER 4 – CIRCUIT DESIGN, SIMULATION, AND LAYOUT

4.1 Design Heuristics for SiC CMOS

The design methodology for the first tapeout is based on Baker's CMOS text and focuses on picking an appropriate circuit topology, selecting and using a consistent bias point for analog devices and using device multiplicity to scale currents to the desired values [40]. The bias points selected for this tapeout are those described previously in Section 3.2. Before design of the PLL and its component blocks was begun, several design heuristics for SiC CMOS were articulated. These heuristics were developed from observations of the measured devices and simulation model fits, as well as from previous experience working with the Cree NMOS SiC process [9], [26], [50]. These heuristics helped guide the selection of circuit topologies and generally complement Baker's methods.

- All devices should have source-body ties to avoid backgate effects. This is critical to avoid reducing the already low transconductance. The lack of model fidelity for the NFET backgate effect makes simulations inaccurate as well. For NFETs, this means devices will only share p-wells if they have common source nodes. For PFETs, this means no stacked devices
- Use a fixed device length from the set of available test device lengths. This is a requirement since the simulation device models only offered a few discrete length values. The Shichman-Hodges parameters for device of different lengths were calculated independently. Since device properties show complex length dependence, this improved the accuracy of hand-design work

- Optimize device gain by use of the appropriate device length. From the measured data it was observed that the L=1.2 μm devices had high transconductance but very poor output resistance. The L=5 μm devices had good output resistance but poor transconductance. The L=2 μm devices offered the best compromise of reasonable transconductance and output resistance.
- Design circuits to minimize bias-point sensitivity since global (run-to-run) and local (on-wafer) variation is high.
- Choose the simplest topology that will accomplish the goal. This improves yield by reducing device count.

The device parameters and operating points were determined as described in Section 3.2. For ease of reference, the 20 μm / 2 μm devices from Table III are repeated here:

TABLE VIII.
PARAMETERS FOR TAPEOUT 1 DESIGN USING 20 μm / 2 μm DEVICES

Parameter	**NFET 20μm / 2μm**	**PFET 20μm / 2μm**
Bias Current	5 μA	
W/L	20/2	40/2
m	1	2
$V_{DS,sat}$, $V_{SD,sat}$	707 mV	707 mV
V_{GS},V_{SG}	3.56 V	4.16 V
V_t	2.85 V	2.90 V
k’	1.0 μA/V^2	0.5 μA/V^2
C'_{ox}	0.86 fF / μm^2	
C_{ox}	34.5 fF	69.0 fF

TABLE VIII Cont.

Parameter	NFET 20µm / 2µm	PFET 20µm / 2µm
C_{gsn},C_{sgp}	23 fF	46.0 fF
C_{gdn},C_{dgp}	11.5 fF	23.0 fF
g_m	10 µA/V	10 µA/V
r_o	15.4 MΩ	16.7 MΩ
$g_m r_o$	154 V/V	167 V/V
λ	0.013	0.012
f_T	69.2 MHz	34.6 MHz

4.2 PLL System Topology

The selected PLL system topology is a charge-pump-based design, shown in Fig. 4.1, that is thoroughly described in several sources [10], [31], [40]. The benefit of this topology, beyond the wide body of knowledge, is the interchangeability of different blocks. With this topology, several different VCOs and PFDs can be used to obtain different behaviors and compare the performance.

This topology requires a PFD with a two-wire output consisting of logic signals UP ("increase frequency") or DN ("decrease frequency"). The signals drive a charge pump, which has the ability to both source and sink (or neither) a fixed current on to a control voltage node. A passive RC element connected to this node acts as an integrator to develop the control voltage, and the VCO is connected to this node. The output of the VCO is connected to an input of the PFD, as well as buffered for output.

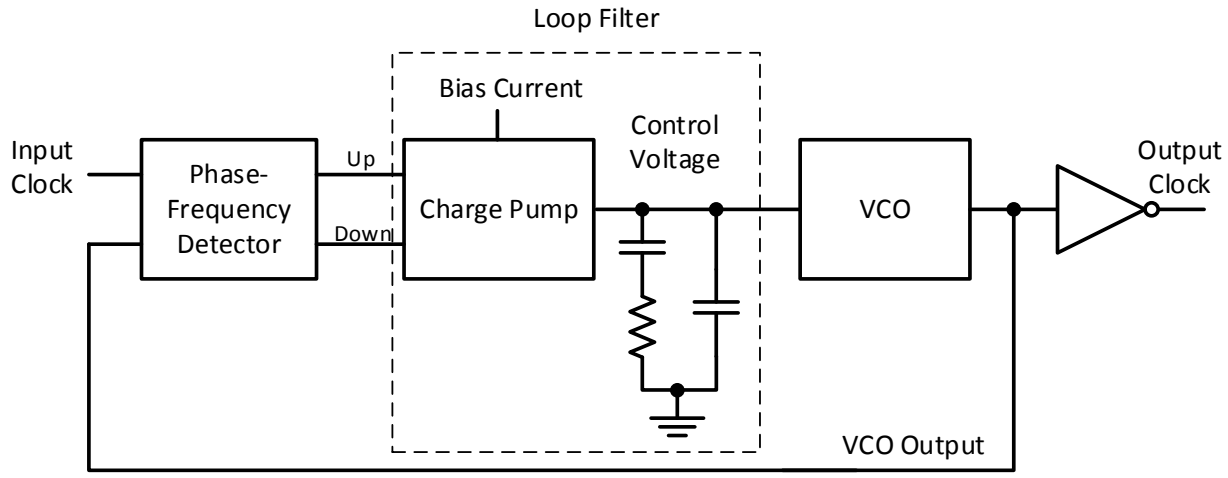


Fig. 4.1. PLL Block Diagram.

4.3 The Phase-Frequency Detector

There are several varieties of the PFD that can be used in this topology. The only requirement is that they have a three-state output. The first, and most popular, is a standard PFD which compares the arrival times of a master input and the feedback VCO output. The PFD instructs the VCO (through the charge pump and filter) to either increase or decrease in frequency in order to time-align the positive-edge transitions of both inputs. Other varieties of PFD, such as the Hogge PFD, are more complex and compare the input signals in a different way. The Hogge PFD, specifically, takes a Non-Return-to-Zero (NRZ) data input and drives the output clock to 90° out of phase with the bit. This circuit is commonly used in serial port hardware to generate a receive clock, and characteristic waveforms are shown in Fig. 4.2.

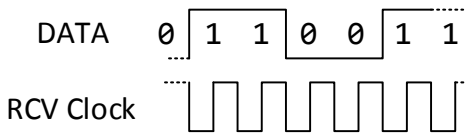


Fig. 4.2. Desired receiver clock for non-return-to-zero (NRZ) serial data.

The PFD is fully digital and a set of Boolean logic gates were designed in order to assemble the PFD hierarchically. The digital gates are all NAND gates (considering that a NAND1 is an inverter), so that the requirement of no stacked PFETs was met. For digital design, the available device models had W = 4 μm or 20 μm, and L = 1.2 μm or 1.5 μm. Based upon observations of the maximum short-circuit current through the two devices, the inverter was built with a PFET/NFET width ratio of 20 μm : 4 μm. The L = 1.5 μm devices were used instead of the L = 1.2 μm device to reduce the risk of low yield. The NFET multiplicity was scaled up for the NAND2 to yield a width ratio of 20 μm : 8 μm, and the NAND3 and NAND4 width ratios were both 20 μm : 12 μm.

The standard PFD schematic is shown in Fig. 4.3, and consists of only NAND gates and inverters. This means it meets the "no stacked PFETs" requirement without modification. An inspection of the schematic reveals it is symmetric with respect to the CLK and DCLK inputs, and there are two $\overline{SR}$ latches inside the circuit. When the CLK input goes high before the DCLK (feedback VCO output) goes high, the UP output is asserted. When the DCLK output then goes high, DN is asserted for a short time while the reset NAND4 is triggered to reset both internal $\overline{SR}$ latches. Since the circuit is symmetric, the same series of events will occur if the DCLK input goes high first (but asserting the DN output instead of the UP output).

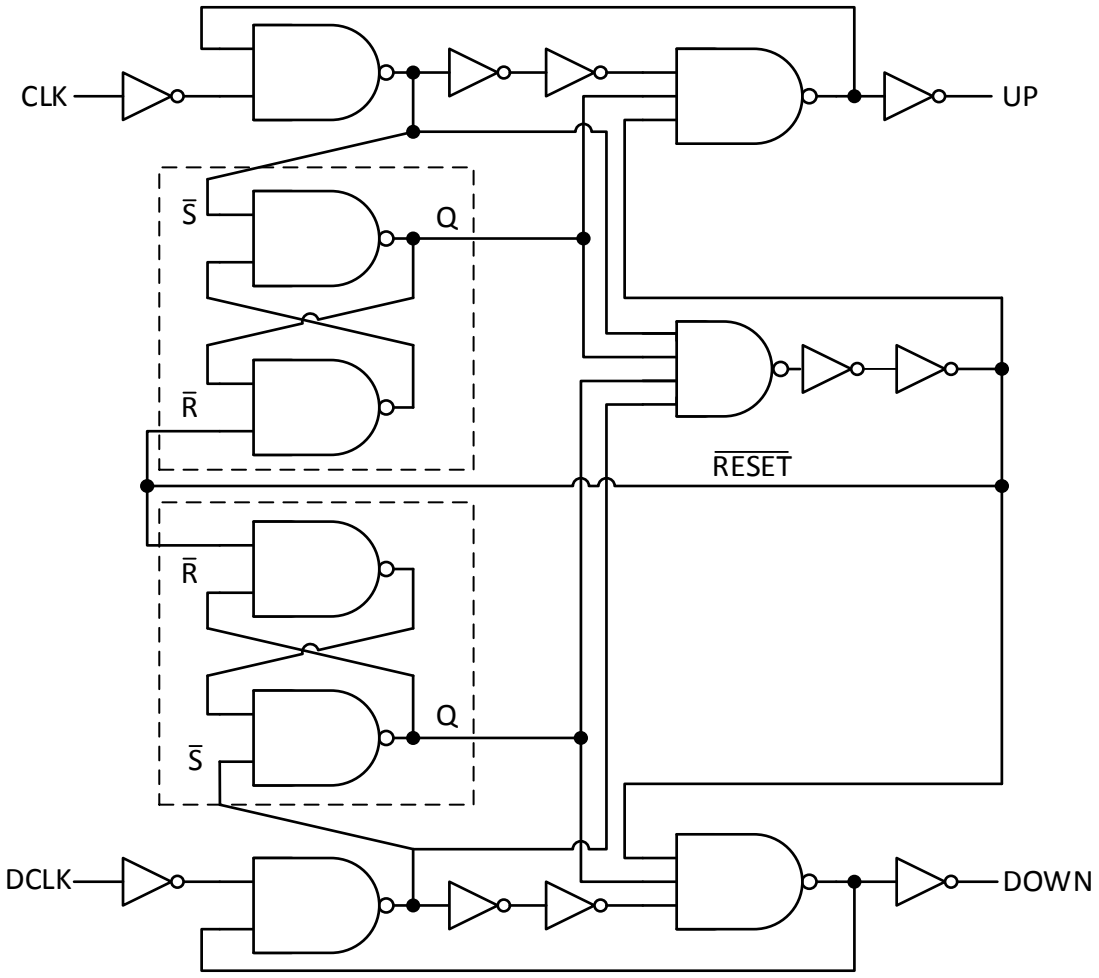


Fig. 4.3. Schematic of the standard PFD showing the internal $\overline{SR}$ NAND latches and the $\overline{RESET}$ signal.

The optimal transfer function of a phase-frequency detector is shown in Fig. 4.4. The -1 to 1 continuum represents the average value of the UP signal minus the average value of the DN signal, so a negative number indicates the PFD is driving the PLL frequency down. The fact that the transfer function is limited to only the first and third quadrants is what distinguishes a phase-*frequency* detector from a phase detector such as an EXOR gate [10].

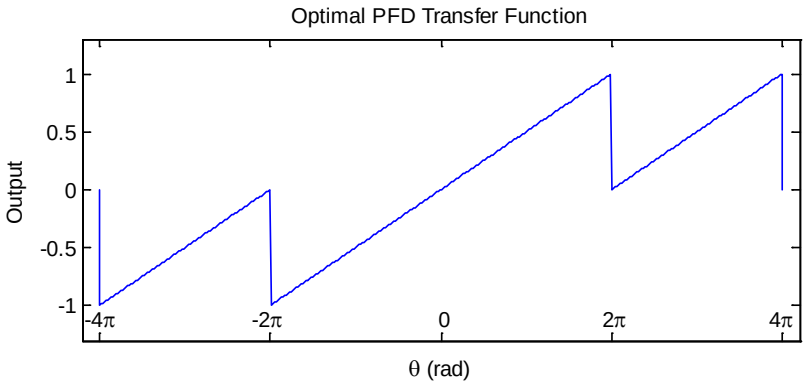


Fig. 4.4. Optimal transfer function for a phase-frequency detector.

The PFD was simulated by varying the phase of two square wave inputs driving the CLK and DCLK inputs. The frequency was stepped from 500 kHz to 10 MHz to determine how the PFD would behave when pushed to a (relatively) high frequency. Fig. 4.5 shows the simulation result when the standard PFD is simulated at 1 MHz, 25 ℃, and typical device models. The transfer function stays in the first and third quadrants as desired. Fig. 4.6 shows results at room temperature and 275 ℃ with typical models, as well as fast and slow models at room temperature. Here, the results show that the PFD transfer function does not stay in the first and third quadrants above 3.68 MHz, except at 275 ℃.

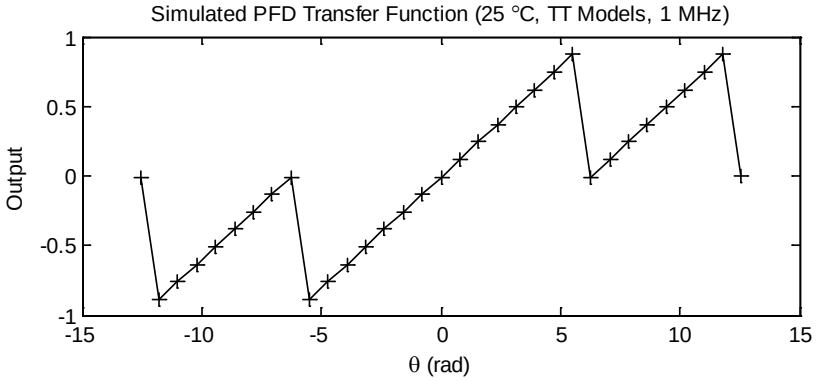


Fig. 4.5. Simulated transfer function of the standard PFD.

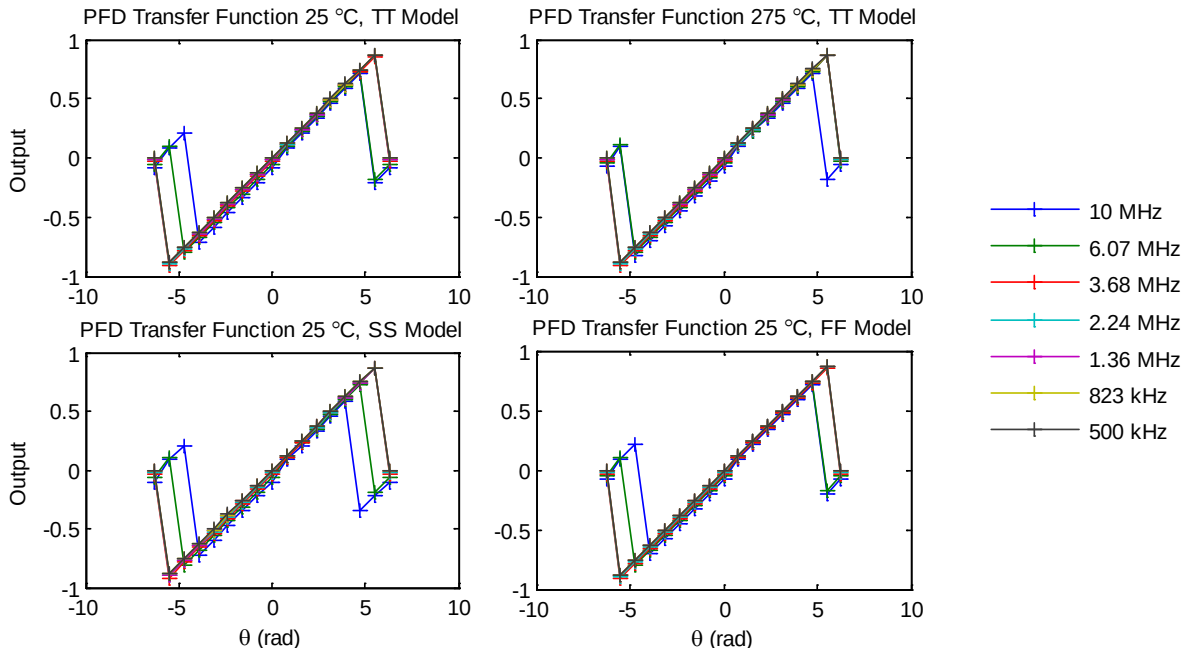


Fig. 4.6. Simulated transfer functions of standard PFD across process corners and at high temperature. Data points are marked for increased clarity.

4.4 Charge Pump and Loop Filter

The charge pump, combined with a simple passive network, forms the Loop Filter as seen in Fig. 4.1. The charge pump is designed to have two logic inputs matching the outputs of the PFD. When one of the logic inputs is asserted, the charge pump drives a fixed current on to the output node. For a VCO with a positive transfer function (increasing the control voltage increases frequency), asserting the UP input of the charge pump causes it to source current from its output, and asserting the DN input causes it to sink. The magnitude of the current being sourced or sunk controls the gain, and the series passive components set the filter pole and zero. Baker recommends the second non-series capacitor be less than 1/10 the value of the capacitor in series with the resistor for additional smoothing without effecting loop stability (since the pole

associated with this smaller capacitor will be significantly above the loop's unity gain frequency).

$$\frac{Control\ Voltage}{Charge\ Pump\ Current} \approx \frac{sCR+1}{sC} \qquad (4.1)$$

The desire not to stack PFETs limited the topologies available for the charge pump. The schematic as designed is shown in Fig. 4.7.

An external bias current sink of 20 μA is used to set the operating point of the circuit, and this current is mirrored to a controlled source leg and a controlled sink leg. In the case of the controlled bias sink, a 1:1 PFET current mirror is connected to a 4:1 NFET current mirror through an NFET on/off device. In the case of the controlled current source, a 1:1 PFET current mirror drives a 1:1 NFET current mirror which then drives a 4:1 PFET current mirror through another NFET on/off device. The 1:1 NFET current mirror was accidently undersized (m=1 instead of m=4), but the conservative bias point allowed this circuit to function well despite the higher bias current per device. The output current is designed to be +/- 5 μA.

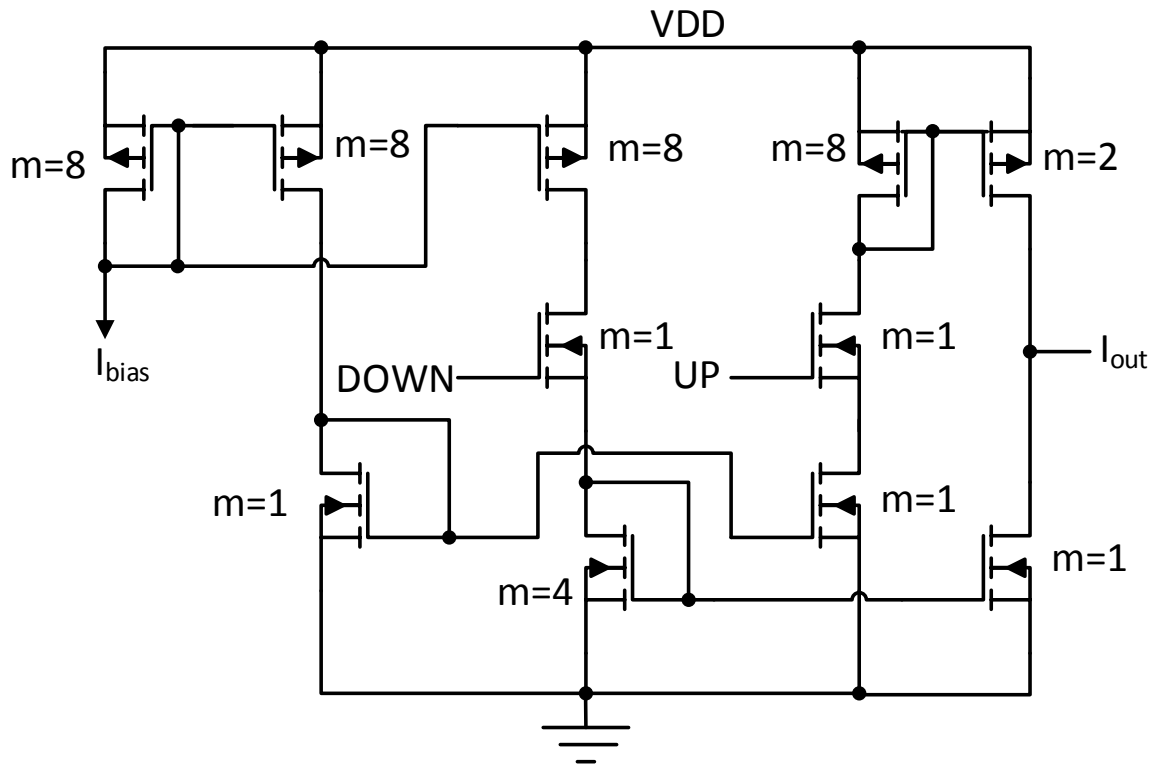


Fig. 4.7. Charge pump schematic showing device multiplicity.

Simulation results showed that the charge pump functioned well across a variety of input voltages and operating frequencies. Fig. 4.8 shows average output current with the output node voltage held at 2.5, 7.5, and 12.5 V. The input duty cycle of the UP and DN inputs was swept from 100% (-1) through 0% DN (0) and from 0% to 100% UP (+1). Although significant nonlinearity is visible at 3.68 MHz and above, the system can still be stable if a conservative overall gain is selected. Fig. 4.9 shows the simulation results at 1 MHz when different model temperatures and corners were used for simulation.

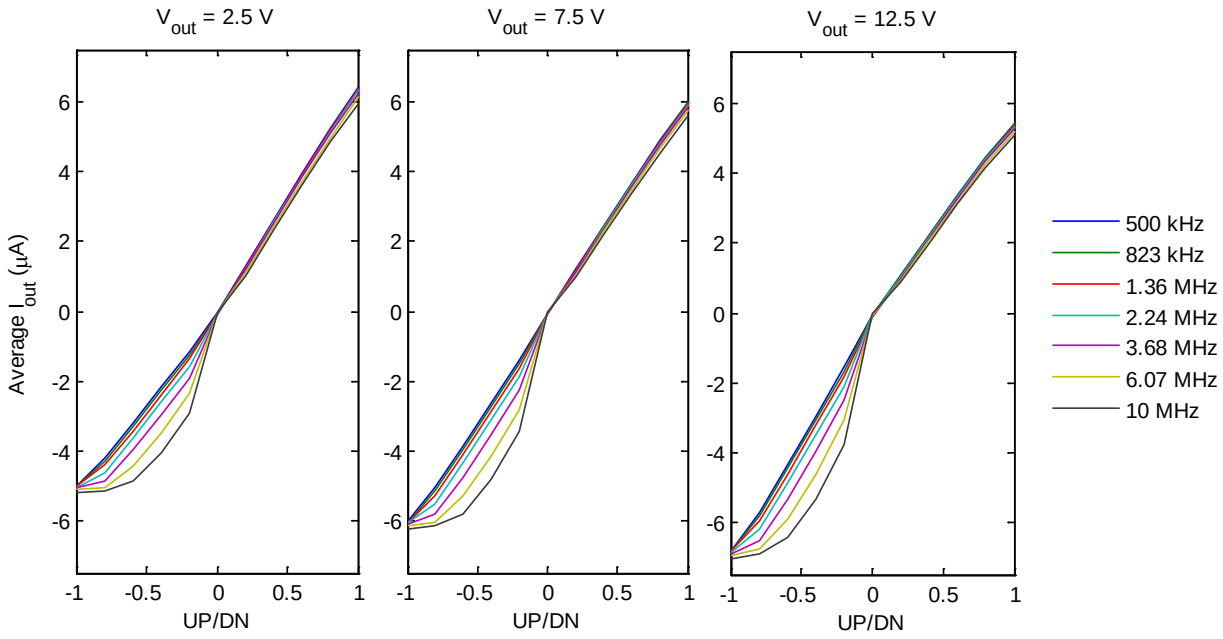


Fig. 4.8. Simulated transfer functions of the charge pump across frequencies and output voltages. Data points are not marked for increased clarity.

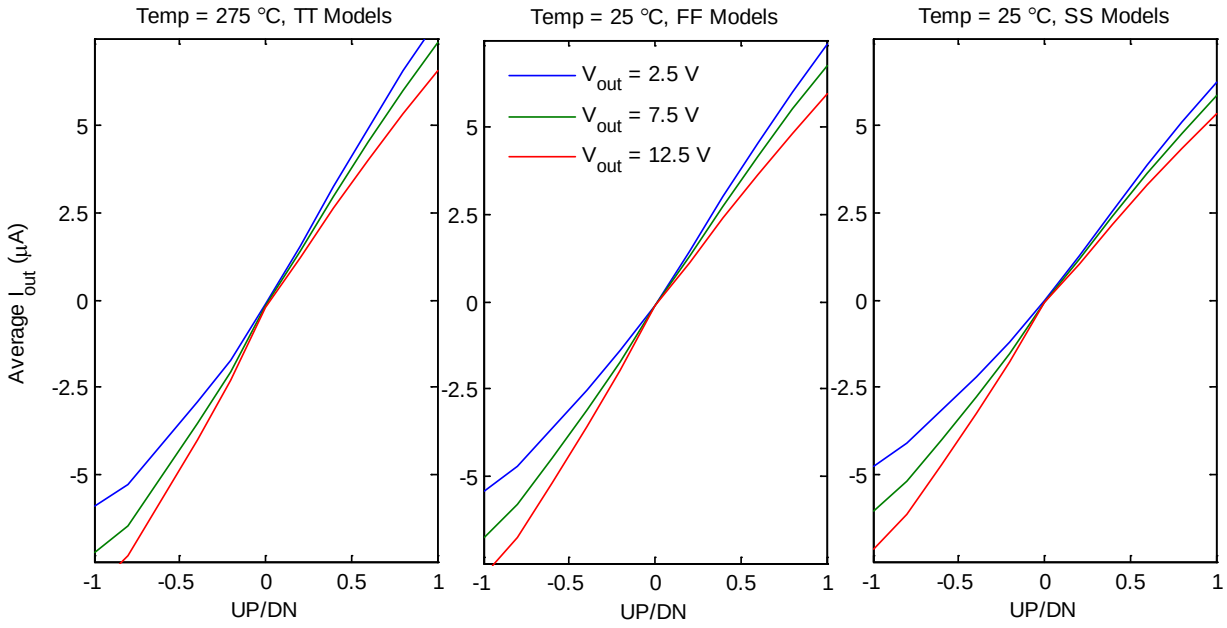


Fig. 4.9. Simulated transfer functions of the charge pump operating at 1 MHz across model corner and temperature at various output voltages. Data points are not marked for clarity.

4.5 Voltage-Controlled Oscillator

The VCO is the most analog component of the PLL. Of the oscillator types discussed in Chapter 2, the resonant-tank oscillator was rejected due to the requirement of an external inductor or crystal, and the relaxation oscillator was rejected due to the higher jitter, particularly since no noise model is available in the HTSiC process at the time of design.

The current-starved inverter, although very simple, is problematic in the HTSiC process. The first issue is that, as shown in Fig. 2.11(c), there is a requirement for a stacked PFET. The second concern is that device variability makes balancing positive-going and negative-going transitions impossible. A differential VCO utilizing the industry-standard Maneatis delay cell (Fig. 2.15) overcomes concerns about balancing transitions, because each transition of the delay cell is the sum of both a positive-going and negative-going waveform. The Maneatis delay cell, however, requires a complex biasing circuit that cannot satisfy the no-stacked PFETs requirement. Additionally, the replica biasing circuit (Fig. 2.17) maintains a constant current, while the actual delay cell current varies from 0 to the biasing circuit value. Since significant aging effects are expected in the HTSiC process, the unequal current in the bias circuit and the VCO delay stages could lead to improper biasing after some time in operation.

A circuit topology was sought that includes the best features of both the current-starved inverter and the differential delay cell. The simple current-source load delay cell, shown in Fig. 4.10, features many of these desirable properties. This circuit has three current sources, which must maintain good matching, but unlike the Maneatis delay cell, the current through these devices will be nearly constant for almost the entire cycle, as will be shown through simulations. Further, MOSFETs used as current sources need only a diode-connected MOSFET of a

proportional width to bias them. The cost of using this cell is a reduced control over the swing of the output nodes with respect to the Maneatis delay cell, and by extension a reduction in PSRR.

Fig. 4.11 shows the simulated voltage at the output nodes and current flowing into the connected capacitor. The slope of the voltage waveform is nearly constant for the duration of the positive and negative transition, showing that the output nodes are slew-rate limited by the current flowing through the capacitor. When the current source load is providing the current flowing in to the capacitor, the current is approximately constant, but when the capacitor is sourcing current, there is a step in the value. This step point occurs when the diff pair common-source node voltage stops rising and starts falling again. This is the moment when the NFET gate-source current suddenly turns on, adding a third current that is summed to make the tail current, and forcing the capacitor current down as a result.

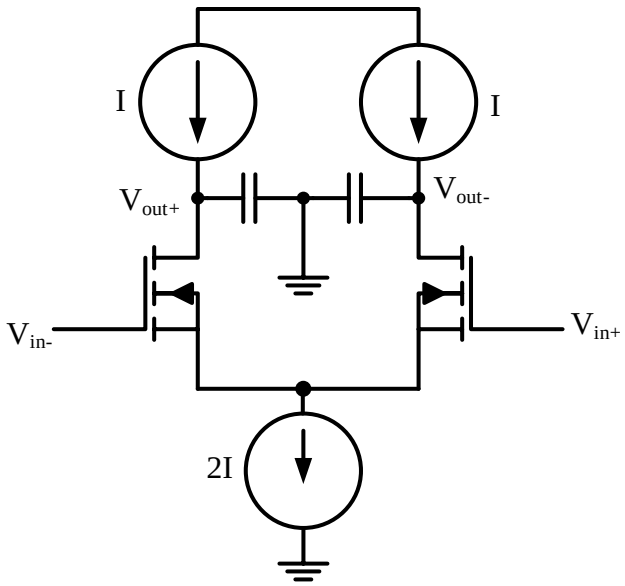


Fig. 4.10. Differential delay cell with current source loads.

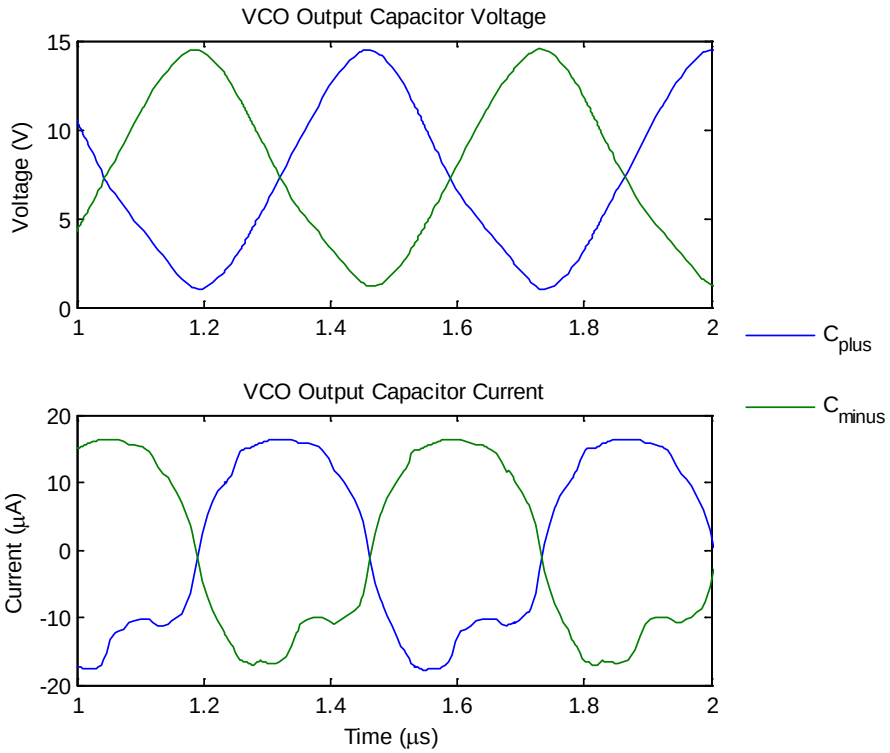


Fig. 4.11. Simulated voltage and current waveforms on the load capacitors of the differential delay stage.

The first-order estimation of the operating frequency of a VCO built from the current-source load delay cell is nearly identical to that of the current-starved inverter VCO. The current into the capacitor is assumed to be +/-I, and the delay for each transition is the time it takes for the capacitors to slew from maximum differential voltage to 0. This delay is half of the total slew time from peak to peak, but is introduced to both a positive and negative going transition during a single cycle, so the total delay is the capacitor slewing time:

$$t_{slew} = \frac{C \cdot VDD}{I_D} \tag{4.2}$$

$$f_{osc} = \frac{1}{N t_{slew}} = \frac{I_D}{N \cdot C \cdot VDD} \tag{4.3}$$

TABLE IX.
COMPARISON OF ESTIMATED AND SIMULATED PARAMETERS FOR THE CURRENT-SOURCE LOAD VOLTAGE CONTROLLED OSCILLATOR

Parameter	Estimated Value	Simulated Value
I	17.5 μA	17.45 μA (average bias current)
C	240 fF	240 fF
V_{swing}	15 V (VSS - VDD)	13.47 V (1.03 V - 14.5 V)
N	3	3
f_{osc}	1.62 MHz	1.86 MHz
oscillator period	0.62 μs	0.54 μs

Table IX shows a comparison of the estimated and simulated oscillation frequency of a 3-stage VCO. The bias current was chosen to be 17.5 μA, and output voltage swing was assumed to be the full VDD of 15 V. The estimated operating frequency was 1.62 MHz. The simulation from Fig. 4.11 shows the output voltage swing is approximately 10% below VDD at 13.47 V and the oscillation frequency is 1.86 MHz. If the simulated output voltage swing of 13.47 V is plugged into Eq. (4.2), the estimated oscillation frequency is 1.80 MHz, an error of only 3%. The load capacitance of each output node was chosen to be 240 fF, approximately seven times the gate capacitance of the next stage's input device, in order to reduce the risk of variation in manufacturing of the transistors.

In addition to the general oscillator behavior just described, it is important to analyze the voltage-control aspect. Eq. (4.3) describes the relationship of oscillator frequency to current, and the derivative gives the current gain:

$$\frac{df_{osc}}{dI_D} = \frac{1}{N \cdot C \cdot VDD} \tag{4.4}$$

By using a simple circuit called a linearized voltage-to-current converter (shown in Fig. 4.12) to generate the current, the oscillator becomes voltage controlled [40]. The MOSFET in this circuit is made very wide, so its V_{GS} is nearly constant, and the slope of the drain current with respect to the control voltage is *1/R*. Eqs. (4.5) through (4.7) include a gain factor *K*, which is the current mirroring ratio between the linearized-voltage-to-current converter and the bias current sources in the delay cell (Fig. 4.10). Combining Eq. (4.4) with Eq. (4.6) gives an approximation of the VCO gain as shown in Eq. (4.7).

$$\frac{1}{K} I_D = I_{converter} \approx \frac{V_{control} - V_{GS}}{R} \tag{4.5}$$

$$\frac{dI_D}{dV_{control}} \approx \frac{K}{R} \tag{4.6}$$

$$\frac{df_{osc}}{dV_{control}} = \frac{K}{R \cdot N \cdot C \cdot VDD} \tag{4.7}$$

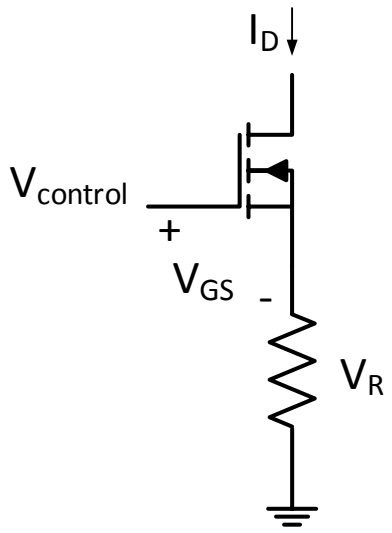


Fig. 4.12. Linearized Voltage-to-Current Converter.

In addition to the three delay cells and a bias generator, a self-biased difference amplifier driving an output inverter is used for the output buffering and conversion from a differential signal to a single-ended one. Fig. 4.13 shows the three different blocks described and Fig. 4.14 shows how the blocks are assembled to form the VCO.

The VCO was designed with three delay cells with a capacitor value of 470 fF, the resistor in the voltage-to-current converter was 36.7 kΩ, and the "wide" device is 10 times wider than other NFETs with the same current. Additionally, the current mirroring ratio was ½. The frequency-to-current gain is expected to be 47.3 kHz/μA and the current-to-voltage gain including the mirroring ratio is expected to be 13.6 μA/V. The total gain of the VCO is expected to be 643 kHz/V.

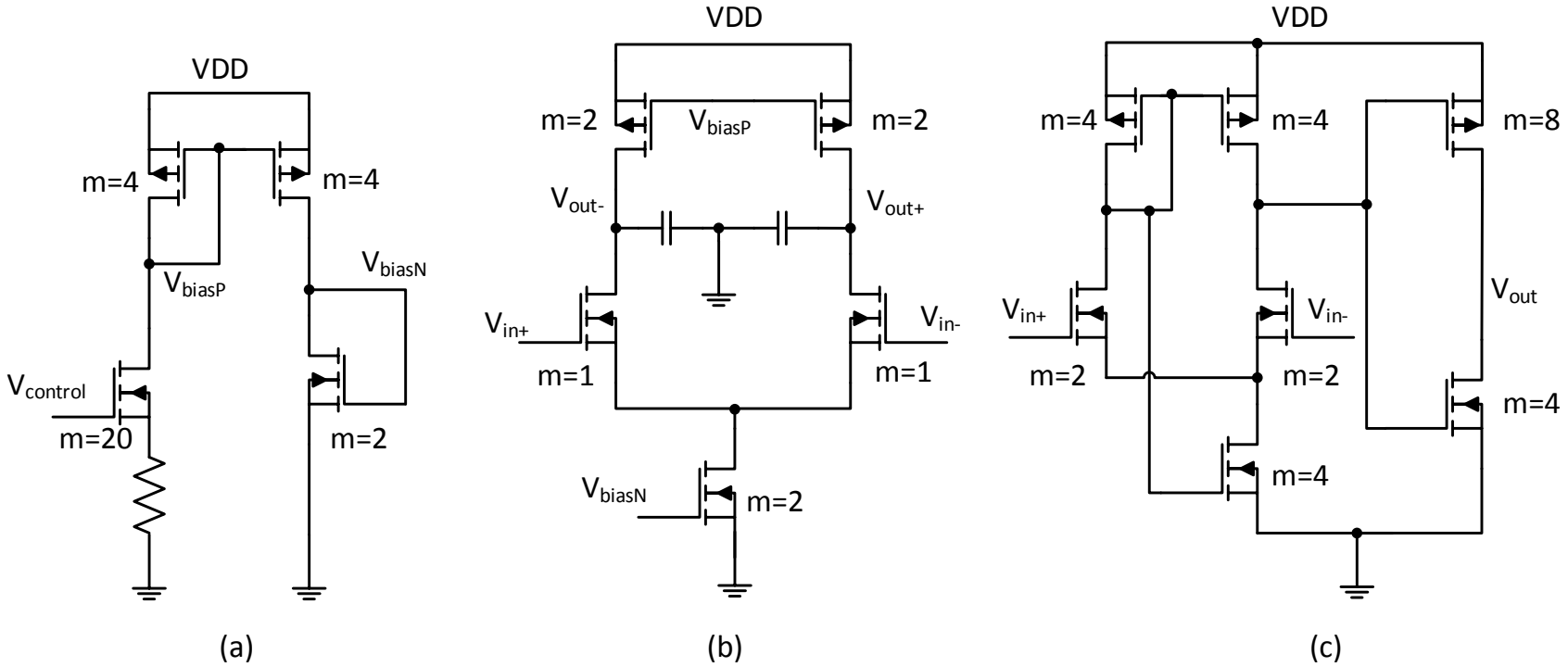


Fig. 4.13. Blocks of the Voltage Controlled Oscillator. (a) Bias generator (b) Differential delay cell (c) Output buffer.

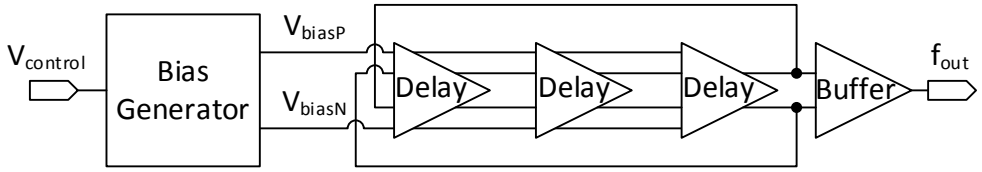


Fig. 4.14. Block-level diagram of the Voltage Controlled Oscillator.

The VCO (with parasitics) was simulated over a range of control voltage inputs, temperatures, and process corners to determine if it would meet the specifications for the PLL. Results showed the VCO had a control voltage input range from ≤ 2 V up to ≥ 10 V. The VCO was capable of approaching or exceeding 5 MHz at elevated temperatures. Fig. 4.15 shows the results of the simulation over temperature. The simulation was a set of transient simulations with the control voltage stepped from 2 to 13 V in 500 mV increments. The overall gain ranges from as high as 400 kHz/V at 25 ℃ up to nearly 700 kHz at 200 ℃. At a control voltage of around 10 V, frequency saturation begins to suppress the gain as shown in Fig. 4.16.

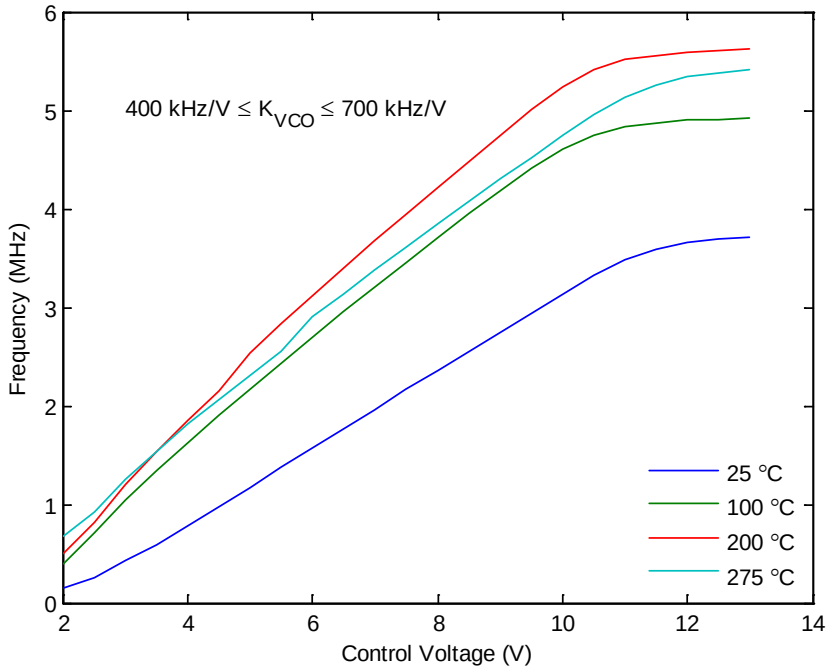


Fig. 4.15. Simulated VCO transfer function across temperature. K_{VCO} is estimated from the smoothed derivative.

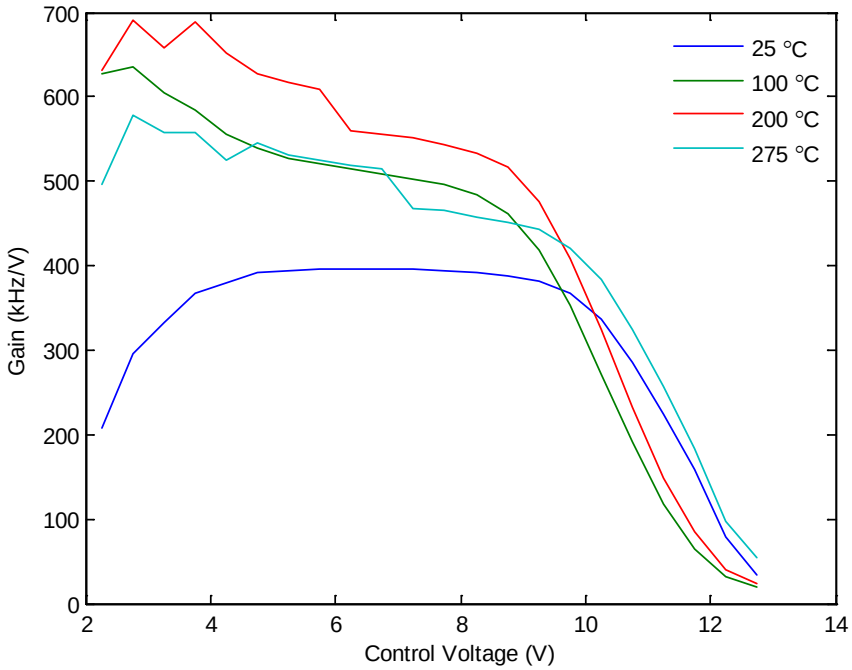


Fig. 4.16. Smoothed simulated VCO gain.

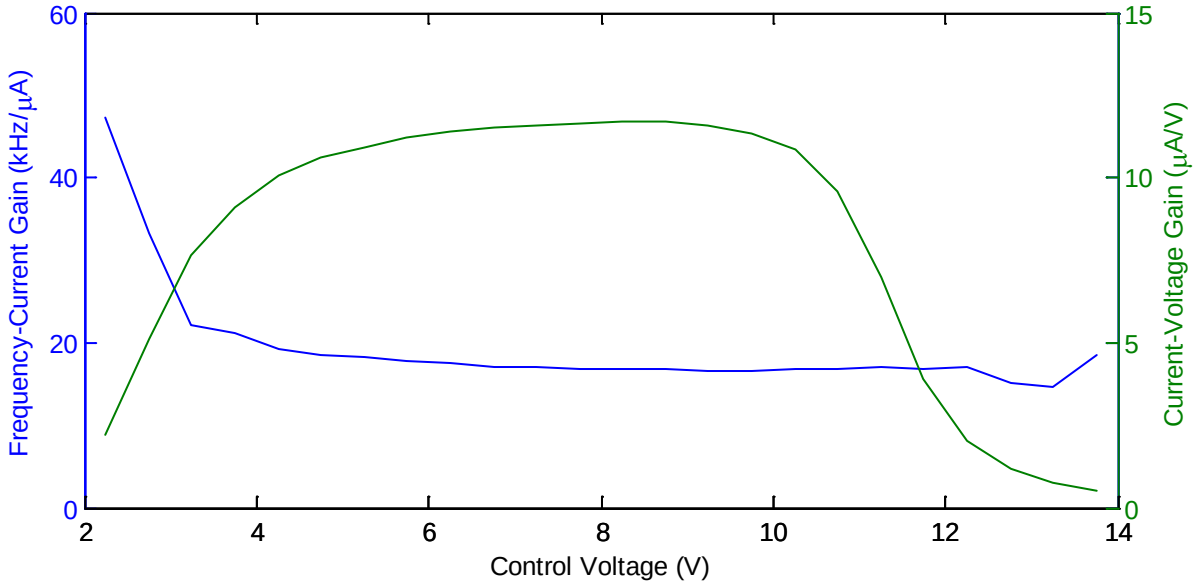


Fig. 4.17. Simulated Gains of the 3 delay cells (left axis) and the bias-generator (right axis).

At 100 ℃ and above, the simulated VCO gain was not too far from the expected value of 643 kHz/V, but at 25 ℃, the gain was only about 62% of the expected value. Additional simulations were run to understand where this discrepancy was originating. The results, shown in Fig. 4.17, indicate that the bias current generator is behaving very much as predicted, with a current output of 10 to 11.7 μA/V over most of its range. The Frequency-Current Gain, on the other hand, was only about half of what was predicted. The simulated current flowing in and out of the capacitor equivalent series resistance (ESR) was observed, and an interesting phenomenon appeared. Contrary to the result shown in Fig. 4.11, the current at 25 ℃ did not have a long period of relatively constant current, but instead spent more time slewing between positive and negative flows. Although the ESR of the capacitor may have some impact on this, it is very likely that this is due to the low number of stages in the loop (3), and the relatively slow device performance. The device performance improves markedly above room temperature, consistent with the observed behavior. It has also been shown that oscillator loops with larger *N* provide output frequencies closer to the theoretical value, and that smaller *N* loops tend to run slower [33].

4.6 System Design and Simulation

With all of the component blocks assembled, the complete VCO could be designed. As previously described, the PFD has a fixed gain target of $1/\pi$ radians^{-1}. The charge pump has a gain of *I*, which in this case is *¼* I_{bias}, and the design was centered at I_{bias} = 20 μA. Finally, the VCO as designed has a gain between 400 and 700 kHz/V. For design of the loop filter components, a K_O of 550 kHz/V was chosen, since higher gains are more difficult to control, and this value aligned well with the 100 ℃ simulation.

The PLL was designed to be both a technology demonstration, as well as a system building block, so there was not a single specification defined for it. Observations of other simulation results, particularly for digital circuits, suggested that they would likely operate between 1 and 2 MHz.. For the PLL, a design-target operating range of 500 kHz – maximum VCO frequency (about 4 MHz at room temperature) was selected to match the 1-2 MHz expected from digital circuits, with a factor of two margin, both above and below.

In [10], the author summarizes the design equations for the PLL with PFD and charge-pump. The loop bandwidth is recommended to be 1/15 to 1/20 of the loop bandwidth so that the assumptions inherent in the design equations are valid. The damping ratio is recommended to be between 0.45 and 2, with lower damping factors providing better jitter performance, and higher damping factors providing better phase tracking [10], [51]. Additional important performance criteria are the lock range, $\Delta\omega_L$, the lock time, T_L, the pull-out range, $\Delta\omega_{PO}$, and the pull-in time, T_P.

The lock range is the region where, after a step in input or output frequency, the PLL can synchronize the output to the input while slipping no more than 1 cycle between them. The lock time is the actual delay between when lock is lost and reacquired inside the lock range. Control-system analysis of the PLL is much simpler inside the lock range, and the operating range is usually aligned with the lock range of the PLL. The pull-out range is the range in which the system is dynamically stable, and oscillations in the output frequency after an input step will be quickly damped. Outside of this range, the system must “pull-in” and the time to do this can be very long with respect to the lock time.

$$\omega_n^2 = \frac{K_P K_O}{C} \qquad (4.4)$$

$$\zeta = \frac{\omega_n RC}{2} \tag{4.5}$$

$$\Delta\omega_L \approx 4\pi\zeta\omega_n \tag{4.6}$$

$$T_L \approx \frac{2\pi}{\omega_n} \tag{4.7}$$

$$\Delta\omega_{PO} \approx 11.55\omega_n(\zeta + 0.5) \tag{4.8}$$

$$T_P = \Delta\omega_0 \frac{C}{K_P K_O \pi} \tag{4.9}$$

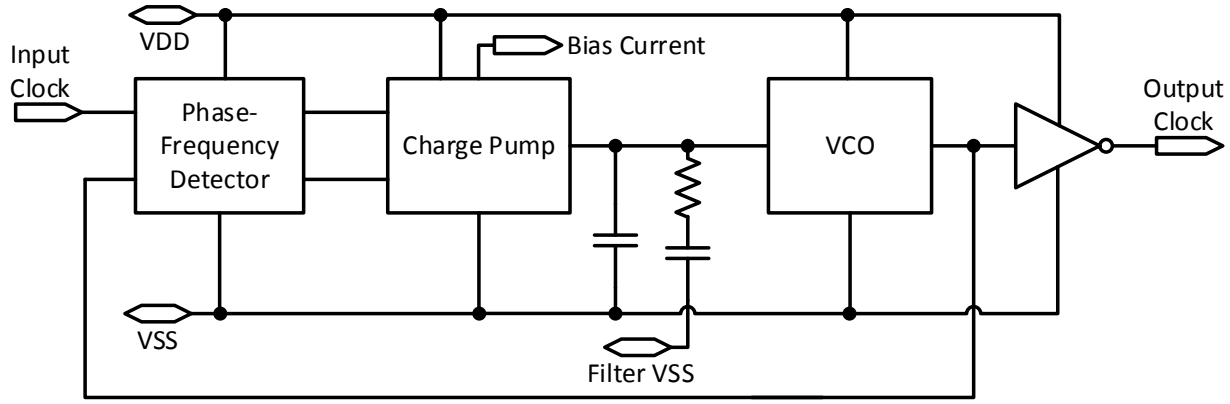


Fig. 4.18. Final system diagram used for layout.

The complete system diagram, shown in Fig. 4.18, shows several important features relating to the system design. In addition to the ability to tune the gain via the charge pump bias current, the separate filter VSS pin meant the system damping could also be modified by inserting an additional series resistance, or natural frequency increased by adding a series capacitance.

When choosing the values for *C* and *R*, the value of *C* required to make the natural frequency less than 1/15 of the minimum tuning frequency was deemed too large for practical implementation (this would have required a 100 pF capacitor). By choosing a value of 54 pF for

C, the area of the capacitor was kept to approximately 40% of the total layout (described in the next section), while maintaining a natural frequency less than 1/10th of the minimum likely frequency of 1 MHz. The value of *R* was chosen to be 41.7 kΩ in order to achieve a damping factor of 0.637. This is heavily weighted towards jitter performance over phase tracking. This choice was made because, without noise models to simulate VCO jitter, the intrinsic loop jitter was minimized to improve the chance of reasonable total jitter. Table X summarizes the design parameters.

TABLE X.
PHASE-LOCKED LOOP DESIGN

PLL Design Parameter	**Symbol**	**Equation**	**Actual Value**
Chosen Values	C	N/A	54 pF
	R		41.7 kΩ
	$K_P \cdot K_D$		5.0 μA
	K_O		3.46 Mrad/V (550 kHz/V)
Natural Frequency	ω_n	$\sqrt{\frac{K_P K_O}{C}}$	566 krad/s (90.0 kHz)
Damping Ratio	ζ	$\frac{\omega_n RC}{2}$	0.637
Lock Range	$\Delta\omega_L$	$\approx 4\pi\zeta\omega_n$	4.53 Mrad/s (721 kHz)
Lock Time	T_L	$\approx \frac{2\pi}{\omega_n}$	11.1 μs
Pull-out Range	$\Delta\omega_P$	$\approx 11.55\omega_n(\zeta + 0.5)$	7.43 Mrad/s (1.18 MHz)
Pull-in Time (Minimum Pull-in Time)	T_P	$\Delta\omega_0 \frac{C}{K_P K_O \pi}$ $(T_P * \Delta\omega_P)$	995 fs * $\Delta\omega_0$ (≥ 7.39 μs)

The complete PLL was simulated several ways. First, a phase-step was simulated to compare against the theoretical lock time. Then a single frequency step, and finally a stair-step frequency input intended to check the PLL's maximum operating range. In all cases, the simulated power supply voltage was ramped from zero, so the PLL had to go through a startup cycle for each simulation. After layout (discussed in the next section), parasitic extraction was performed. All simulations shown in this section are from the parasitic-extracted netlists.

Fig. 4.19 shows the simulated frequency response of the PLL when the input has a +90° phase step introduced. At 25 ℃, the maximum frequency is only 4% higher than input frequency, whereas at 275 ℃, the difference is around 6%. This shows that, at higher temperatures, the PLL loop gain is higher, and the loop should relock more quickly. This finding aligns with the VCO simulations, where the room-temperature gain is significantly lower than the gain at elevated temperature. This can also be observed by the duration of oscillations. At 25 ℃, the VCO gain is lower, so the PLL output frequency rings longer before settling to its final output. The design equations in [10] are based on a 2% settling time criteria. The calculated lock time ranges from 18.7 to 13.7 μs, all somewhat longer than the estimated lock time of 11.1 μs.

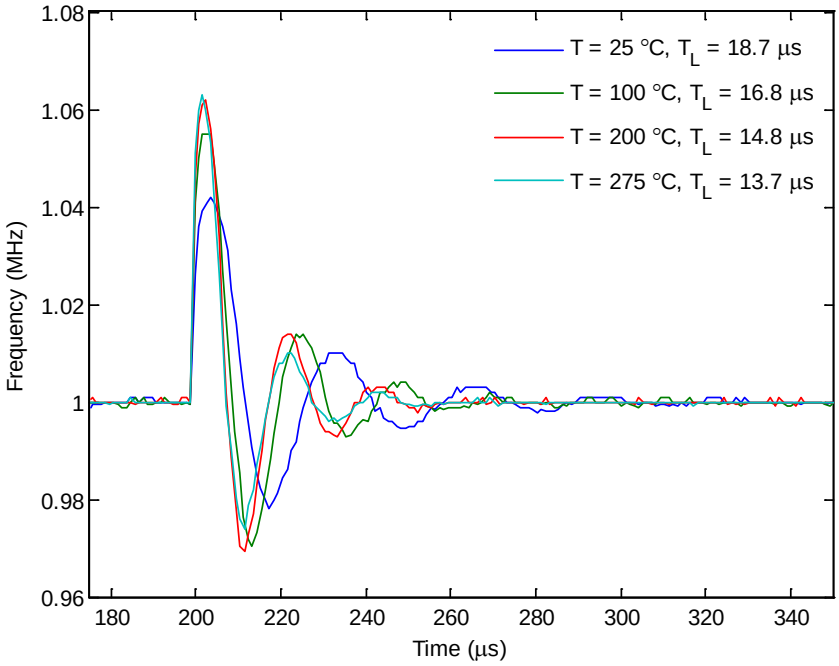


Fig. 4.19. Output Frequency of the PLL when a +90° input phase step is introduced at 200 µs. Lock Time (T_L) is calculated by taking the 2% settling time.

Fig. 4.20, which shows the control voltage during the input phase step, reveals more information about the PLL. There is a very large offset in the DC component of the control voltage at 25 and 100 ℃. This large offset is due to the large change in the NFET threshold voltage and transconductance with temperature. This combined with the relatively small frequency step shown previously, demonstrates how well the PLL design mitigates global changes in device parameters. The high frequency noise visible in the control voltages has minimal effect on the VCO, since it functions a low-pass filter in the phase domain. Reviewing figures 19.35 and 19.75 from Baker, it is also clear that this high frequency noise can show up on the control voltage node, and its presence is not necessarily an indication of a loop filter cutoff frequency that is too high [40].

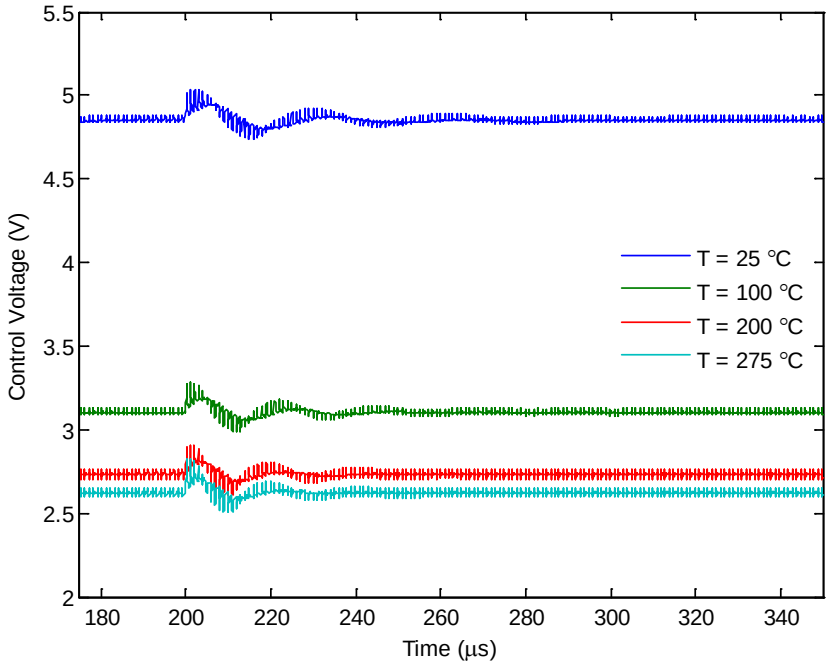


Fig. 4.20. Control voltages during the +90° input phase step.

The input frequency-step simulation results are shown in Fig. 4.21. The input was stepped from 900 kHz to 1.1 MHz, and the output, in each case, shows an overshoot of approximately 50%. In this plot, the rise time is less than half the predicted lock-time, and the settling time is significantly longer than the predicted lock time. This is consistent with the phase-step results shown in Fig. 4.19, and indicates that the damping ratio is lower than the estimated value in Table X.

The stair-step input simulation, shown in Fig. 4.22, demonstrates that the PLL should function at 3.5 MHz at room temperature, and over 4 MHz at 100 ℃ and above.

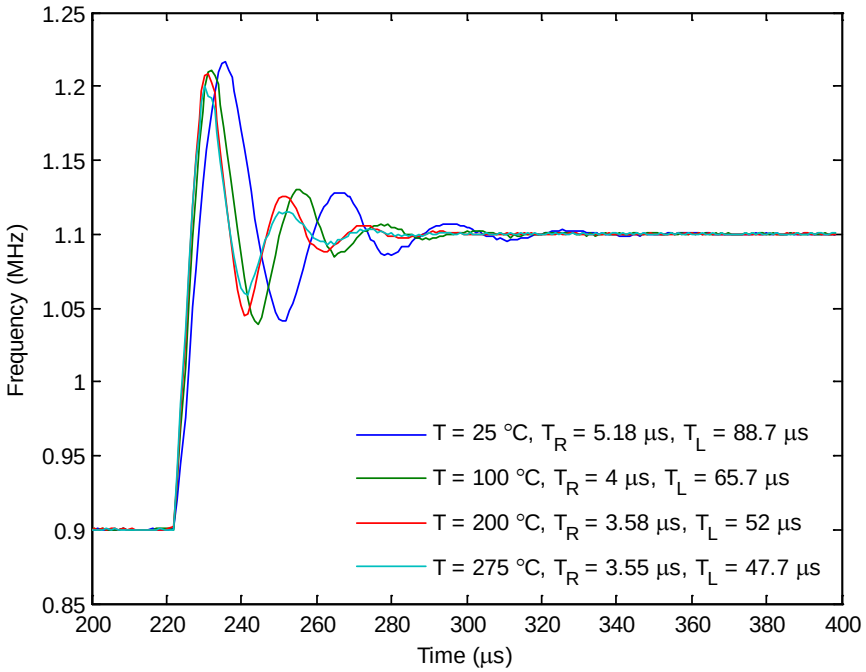


Fig. 4.21. Output response to an input frequency-step from 900 kHz to 1.1 MHz.

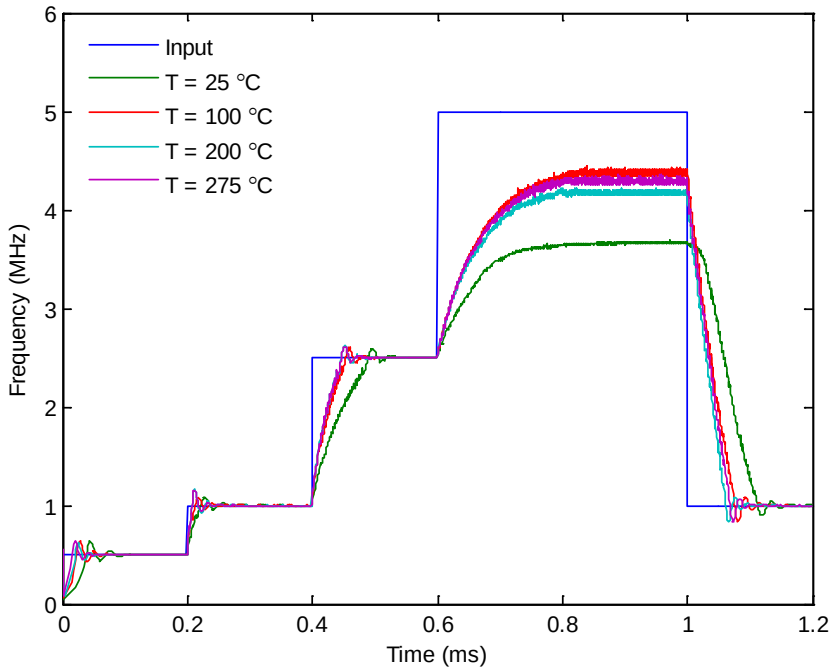


Fig. 4.22. Output response to an input- stair-step to determine maximum operating frequency.

4.7 Circuit Layout

The VCO, PFD, and charge pump were laid out as individual blocks before being combined with the passives to layout the complete PLL. The PFD, shown in Fig. 4.23, was built up from individual gate layouts as well. In this cell VDD and VSS were interleaved so that no breaks in the single metal layer would be necessary on these nets. VSS is in the form of a “U”, open to the right, and connection from outside the cell is made from the left. VDD is “W”-shaped, open to the left, and the output signals use polysilicon jumpers to reach the cell-edge without breaking the VDD metal.

The charge pump and VCO are shown in Fig. 4.24 and Fig. 4.25, respectively. The charge pump and VCO both use linear VDD and VSS busses. In the VCO, the NFET input pairs on the delay cells use dummy transistors on the outside to promote better matching.

Finally, the complete PLL is shown in Fig. 4.26. The passives for the loop filter took up approximately 35-40% of the total layout area, demonstrating the challenge of reducing loop bandwidth through these components.

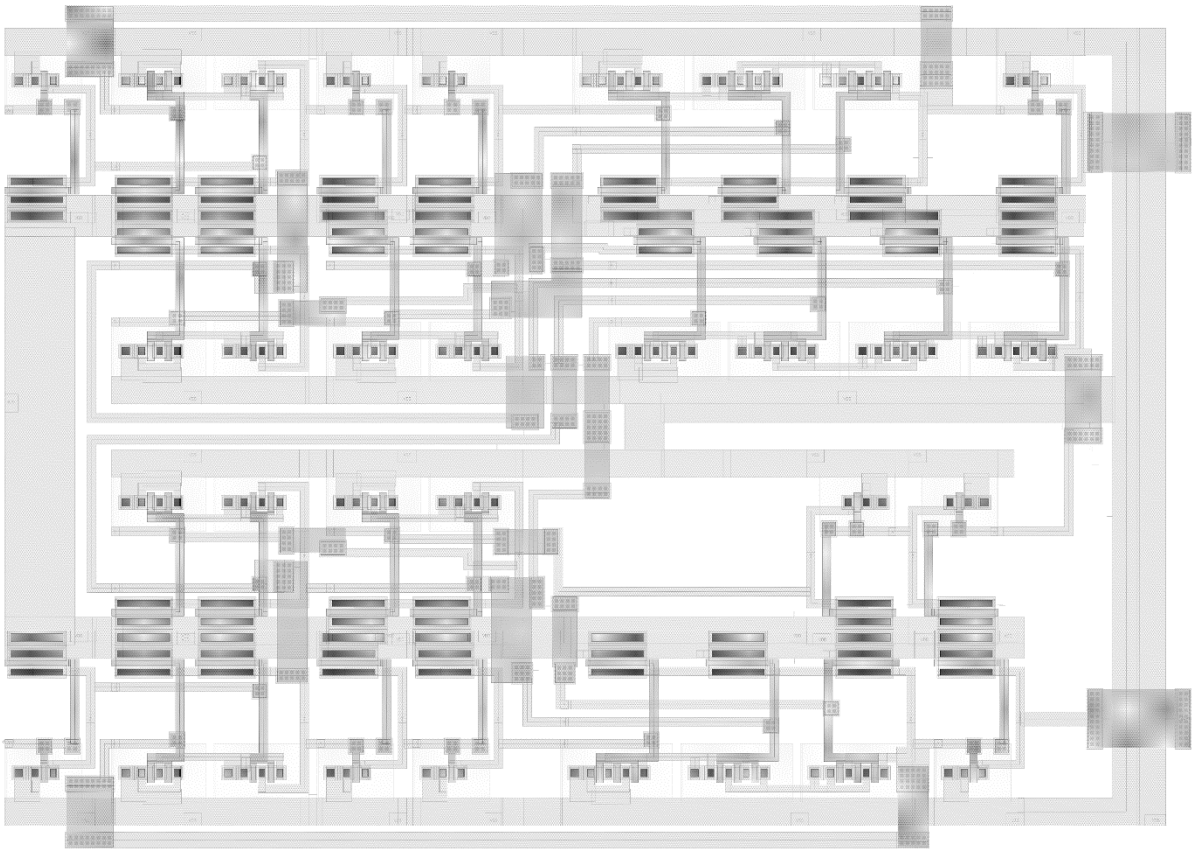


Fig. 4.23. Layout of the Phase Frequency Detector. Input and VSS connection are on the left, while the outputs and VDD connection are on the right.

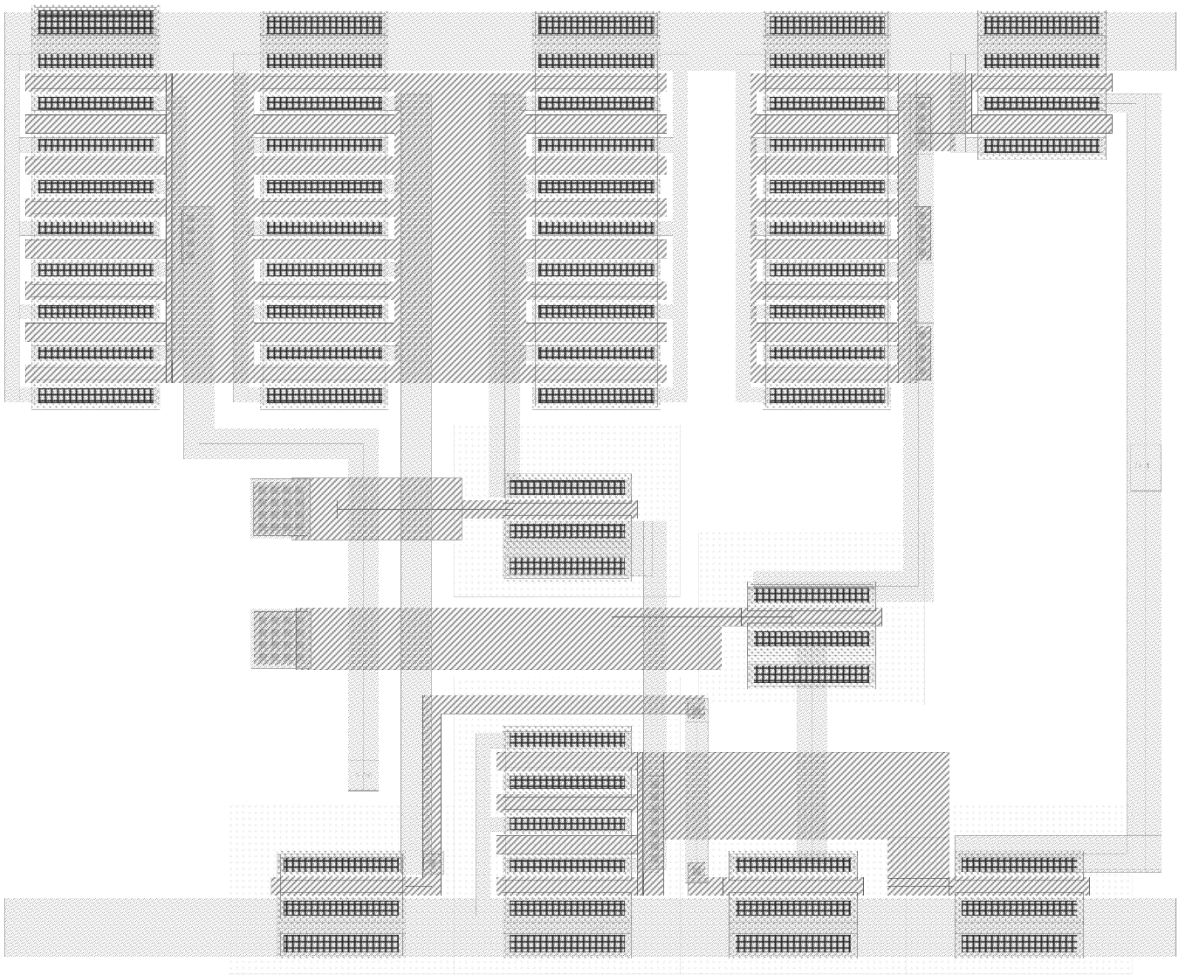


Fig. 4.24. Layout of the Charge Pump. VDD is at the top, VSS is at the bottom, Inputs are on the left, and the output is on the right.

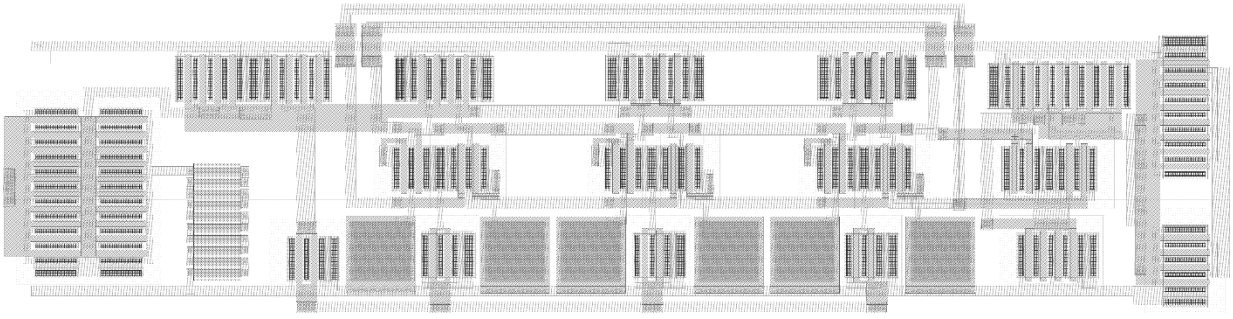


Fig. 4.25. Layout of the VCO. VDD runs along the top and VSS runs along the bottom. The current-mirror load delay cells are in the center. The bias generator and $V_{control}$ input are on the left. The output buffer is on the right.

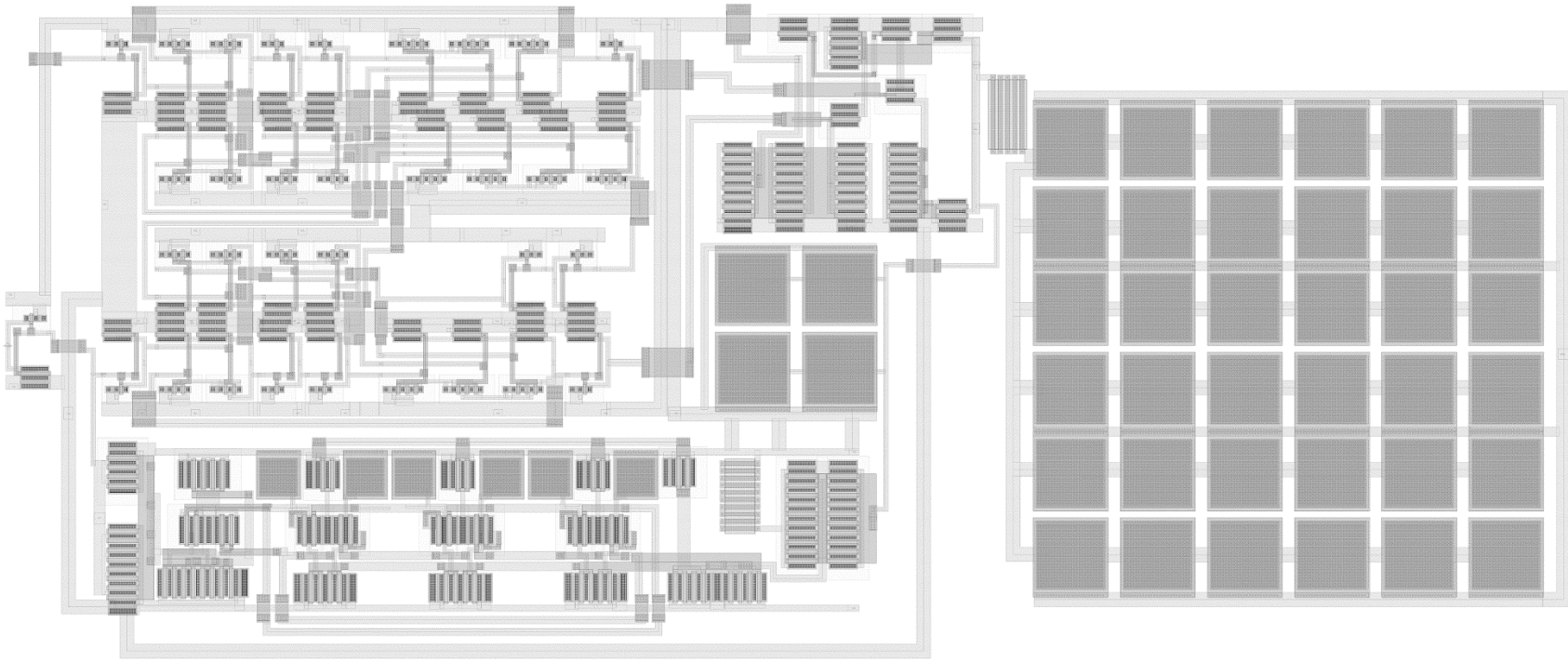


Fig. 4.26. Complete PLL layout. The PFD is on the top left, the charge pump is at top center, and the VCO, rotated 180°, is in the lower left. On the right is the 54 pF capacitor broken into 36 1.5 pF tiled capacitors. The secondary capacitor, consisting of 4 1.5 pF tiled capacitors, is seen in the middle.

CHAPTER 5 – CIRCUIT TESTING

Circuits were fabricated by Raytheon and returned as a lot of five complete wafers. A specific wafer was selected for general testing. The overall circuit yield was tested before the wafer was diced, and after dicing, specific reticles were selected for further investigation. Test devices from this wafer and another wafer were used to formulate new models (described as "post-tapeout 1 models" here). The fabricated PLL is shown in Fig. 5.1.

Fig. 5.2 shows the comparison between post-tapeout 1 models and the models used for design in Chapter 4 (termed "pre-tapeout 1 models"). The NFET input characteristics shows a minimal shift in the threshold voltage, but the PFET input characteristics demonstrate and increase of nearly 3 V in the threshold voltage. The NFET output characteristics show a modest increase in the transconductance, while the PFET output characteristics show a modest decrease. Overall, this large shift in relative device strength is an excellent test case for the PLL topology described in Chapter 4.

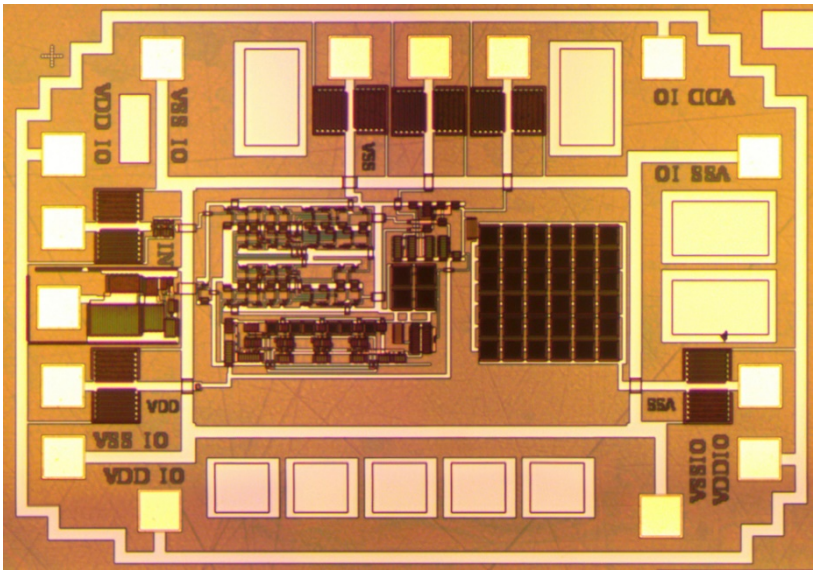


Fig. 5.1. Die micrograph of the fabricated PLL including the pad ring.

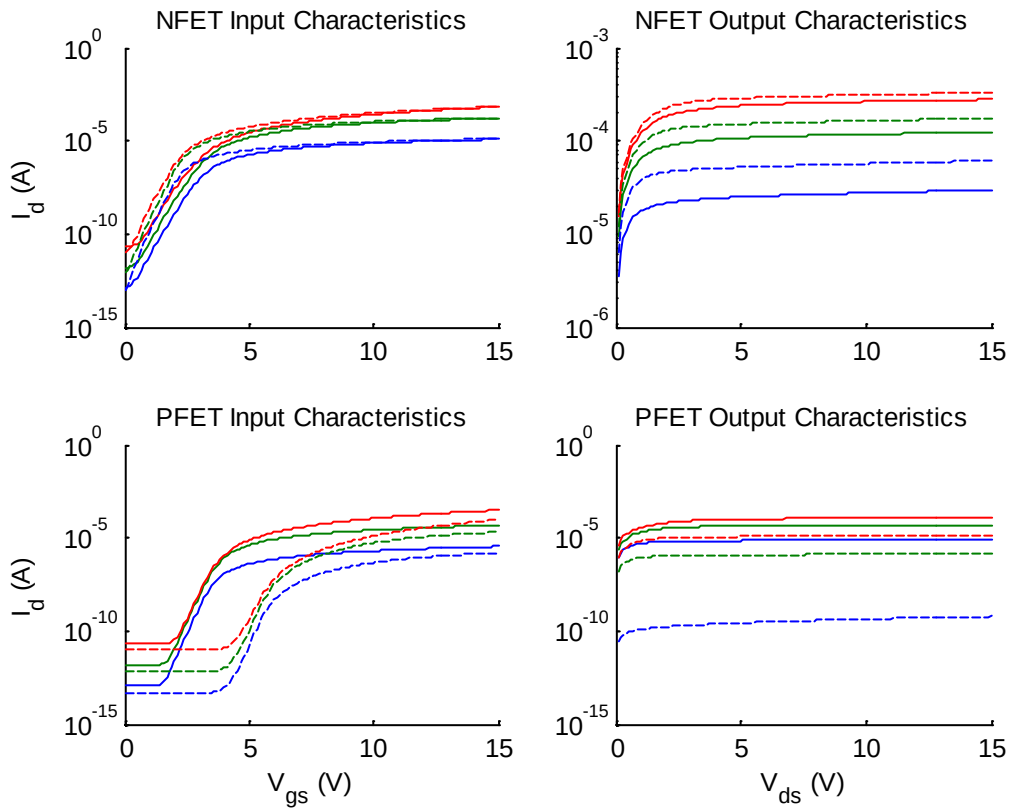


Fig. 5.2. Comparison of input and output characteristics between pre- and post-tapeout 1 models. Solid lines are pre-tapeout 1, and dashed lines are post-tapeout 1.

The results presented in this chapter were obtained from diced reticles on the probe station. In some cases, the wafers were probed with the Picoprobe 12C active voltage probe, but this probe is limited to temperatures of approximately 125 ℃ and below. Fortunately, the pad rings were designed to drive the expected capacitance of the probe station and oscilloscope. In all cases though, the probe lead was run directly to the oscilloscope input, not through the probe station bulkhead, in order to minimize cable length and capacitance.

5.1 VCO Yield Testing at Room Temperature

To gauge the general yield across the wafer, the VCO inside the PLL was checked for basic functionality. This check was performed on the undiced wafer using the probe station. A

control voltage of 5 V was applied, and the output frequency was measured. Table XI shows the output frequency where a signal was present, or an X where the VCO was non-functional. The total yield of the VCO was 14 out of 24 possible, which was considered to be a good outcome based on conversations with the foundry. Further discussions with the foundry led to a new design rule which is expected to significantly increase yield for future runs.

It was also observed that the frequency at the center of the wafer was much higher than the frequency around the outside of the wafer. Observations by the modeling team indicated that the threshold voltage of the NEFTs was lowest towards the center. This means that the VCOs in the center were being driven harder at 5 V input than those on the outside, which accounts for the output frequency trend.

Table XI.
VCO OUTPUT FREQUENCY AT $V_{CONTROL}$ = 5V

	C1	C2	C3	C4
R7		X	X	
R6	240 kHz	X	340 kHz	330 kHz
R5	X	730 kHz	X	600 kHz
R4	530 kHz	780 kHz	840 kHz	X
R3	X	750 kHz	780 kHz	500 kHz
R2	X	X	700 kHz	550 kHz
R1		X	550 kHz	

5.2 Charge Pump DC Testing at Room Temperature

The charge pump transfer function was tested at DC and room temperature to determine the output-voltage range and current matching. This test was done by asserting either the UP or the DN input on the standalone charge pump on the reticle. The output pin was biased using a Keithley 2400 Sourcemeter, and the current read from the bias voltage supply. The charge pump

bias current input was supplied with 20 μA from the other channel of the Sourcemeter. The result is shown in Fig. 5.3.

While acting as a current sink (frequency DN), the charge pump can operate down below 1 V. While acting as a current source (frequency UP), the charge pump can operate up to 14 V. Both of these voltages are beyond the range of the VCO control voltage input. Between 2 and 10 volts, where the VCO control voltage is likely to be effective, the sink mode ranges from 4.7 μA to 5.6 μA, or -6% to +12%. In the sourcing mode, the output ranges from 5.2 μA to 5.7 μA, or +4% to +14%. Overall, these are good results given the simple design of the charge pump and the low output resistance of the devices.

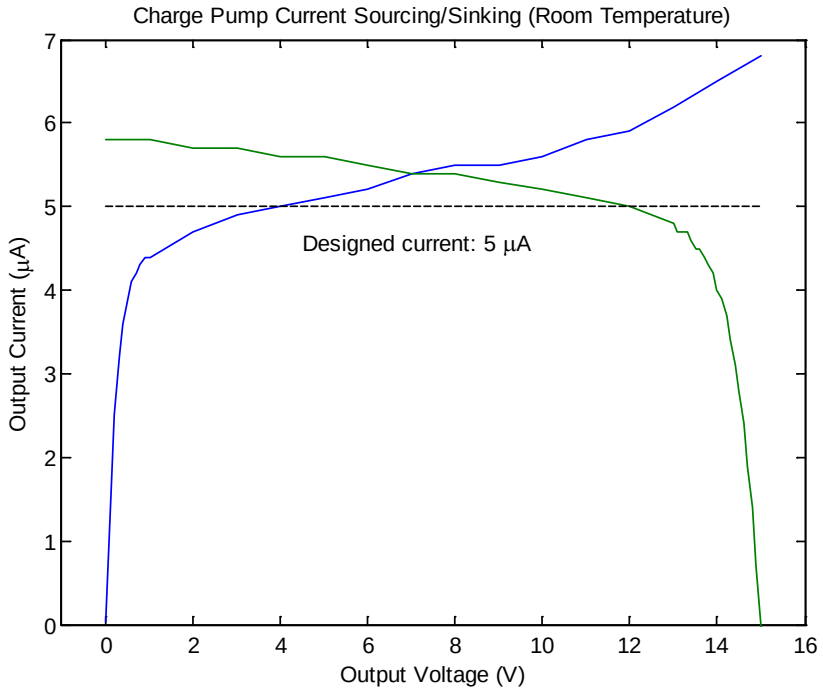


Fig. 5.3. Current drive from the charge pump at DC and room temperature. Blue is the current-sinking mode, and green is the current-sourcing mode.

5.3 Basic Functional Testing of the Phase-Frequency Detector

Very early in the testing phase, the stand-alone phase frequency detector was tested on the probe station at room temperature using active probes. The PFD showed good functionality but some phase offset at 1 MHz. Fig. 5.4 and Fig. 5.5 together demonstrate good functionality, but with a slight phase offset. Fig. 5.4 shows the CLK input to the PFD arriving just slightly before the DCLK input. In this case, the UP output is asserted. In Fig. 5.5, the input phase relationship is reversed, and neither output is asserted. This indicates that the DCLK input path has slightly more delay than the CLK input path, but the phase offset will be trivial compared to the delay introduced by the output buffer.

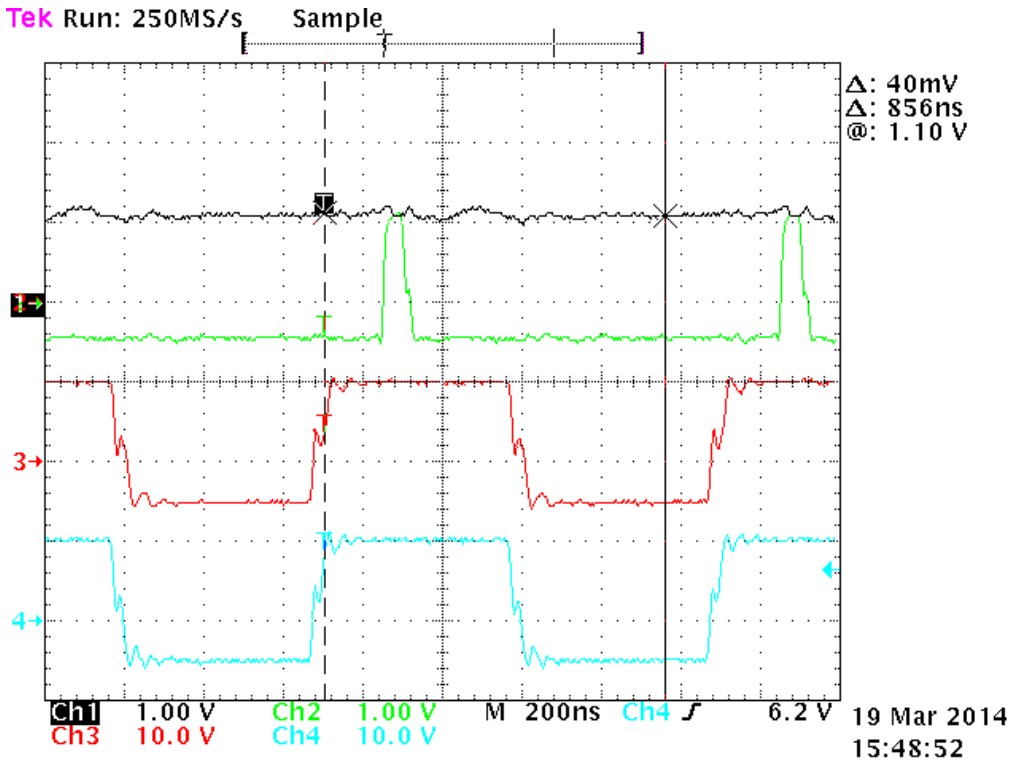


Fig. 5.4. Transient testing of the PFD at 1 MHz. Ch1 (black) is the DOWN output, Ch2 (green) is the UP output, Ch3 (red) is the DCLK input, and Ch4 (blue) is the CLK input. In this case, the CLK input very slightly leads the DCLK input, and after some delay, the UP output is asserted before resetting. Ch1 and Ch2 are measured by 10x active probes, so the voltage scale is actually 10 V/div, and there is a DC offset (DOWN is always logic 0).

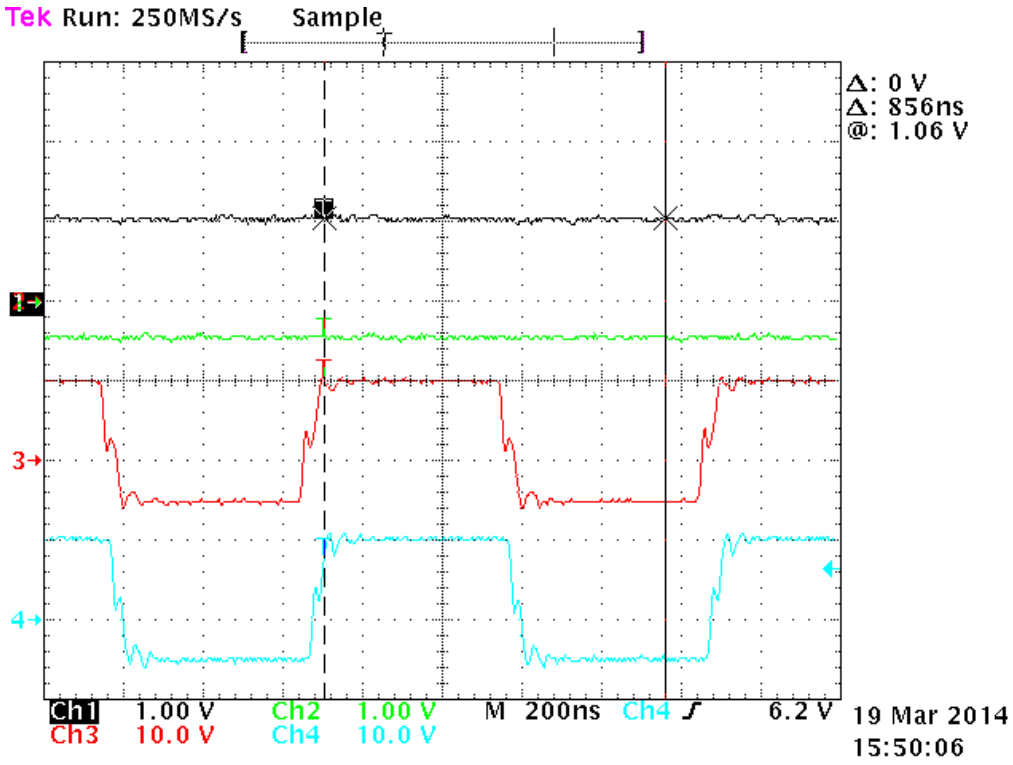


Fig. 5.5. Transient testing of the PFD at 1 MHz. Channel assignments are the same as the previous figure. In this case, the DCLK input very slightly leads the CLK input, and neither output is asserted.

On the other hand, Fig. 5.6 shows the PFD failing to operate normally at 5 MHz. The DCLK input is leading the CLK input, and the DOWN output is correctly asserted at one cycle, but at the next cycle, the output is rapidly oscillating back and forth. This indicates that the operating frequency of the PFD can approach 5 MHz at room temperature. As will be shown in the next sections, this exceeds the capability of the VCO and the system as a whole.

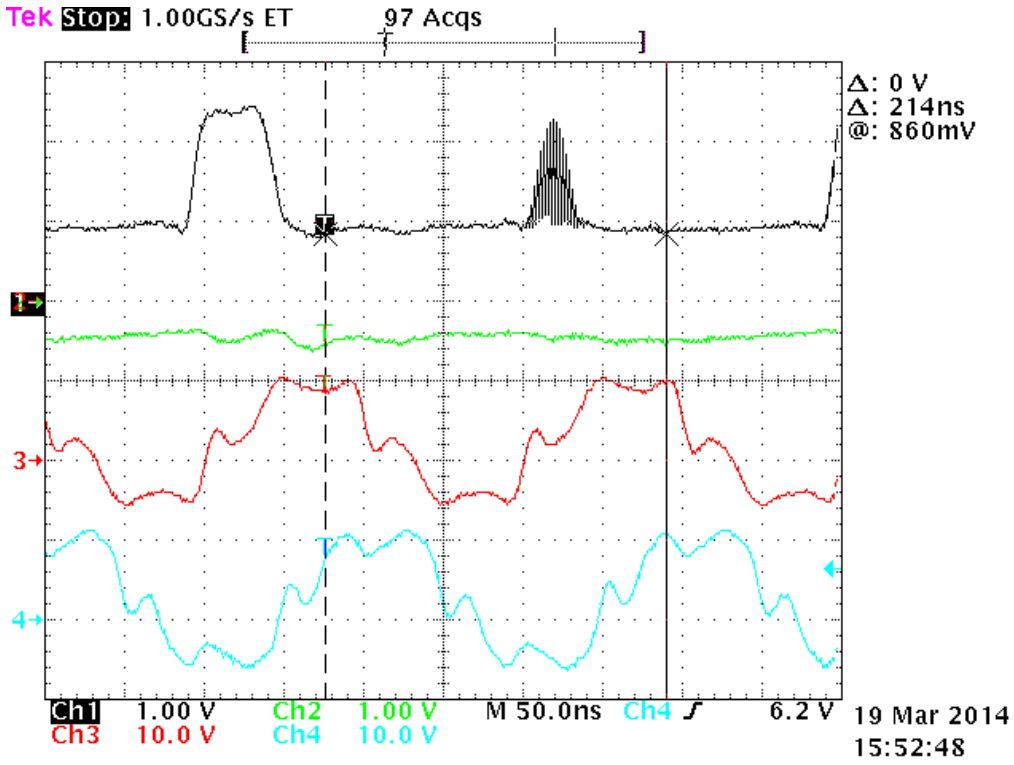


Fig. 5.6. Transient Testing of the PFD at 5 MHz. Channel assignments are the same as the previous figure. In this case, DCLK input leads the CLK input, and the DOWN output is properly being asserted at one time, but is glitching at another time. The poor quality of the input waveforms is due to reflected waveforms from the PFD input (there is no terminating 50-ohm impedance for matching coaxial inputs).

5.4 VCO Simulations and Frequency at Room Temperature

In addition to the room-temperature yield, the maximum operating frequency of the VCO at location C3, R4 was checked. This was the fastest VCO during the wafer yield testing as shown in Table XI. With a control voltage input of 9 V, the VCO was able to achieve slightly greater than 2.5 MHz as shown in Fig. 5.7. The VCO at C3, R2 was only able to run to a maximum frequency of 1.15 MHz. Simulations done with the pre-Tapeout 1 models and models derived from devices on the returned wafers demonstrate the large shift in device parameters. In the pre-tapeout simulations, the frequency saturates when the control voltage reaches 10 V, but in the post-tapeout simulations, the frequency saturates with a control voltage of only 5 V (Fig.

5.8). The gain, shown in Fig. 5.9, is still in the 400-700 kHz/V range, both before and after. This demonstrates the benefit of the VCO topology for a process where device parameters are expected to show large global variation, but small local variation.

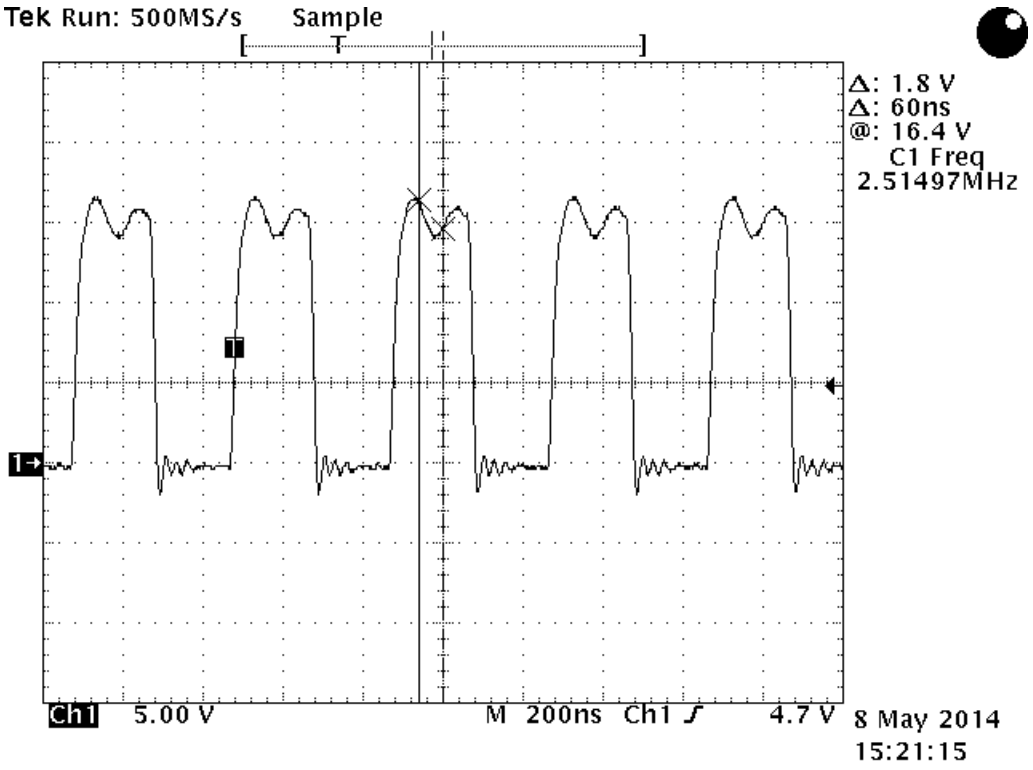


Fig. 5.7. VCO from Reticle C3, R4 operating at a maximum frequency of 2.5 MHz at room temperature.

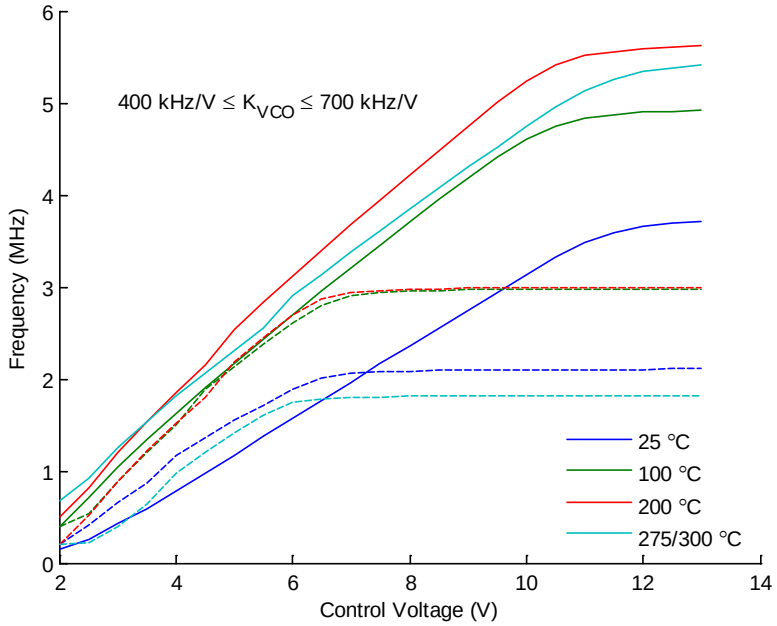


Fig. 5.8. Simulation of the VCO with models before Tapeout 1 (solid lines) and models derived from test devices returned on Tapeout 1 (dashed lines). Although the gain is similar in the controllable region, the large shift in the PFET threshold voltage limits the VCO to an operating frequency of 2-3 MHz.

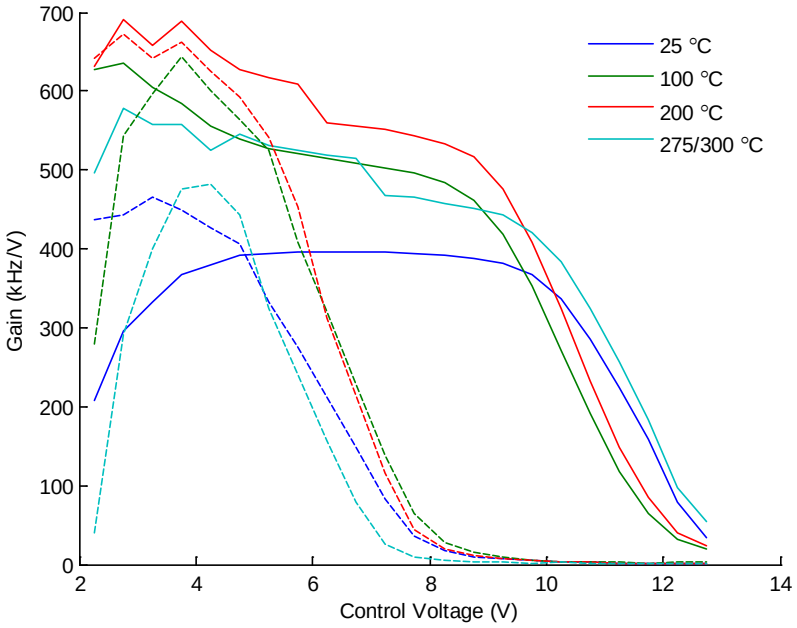


Fig. 5.9. Smoothed simulated gain before (solid) and after (dashed) Tapeout 1. The range of gain is similar, but the operating region is limited to a control voltage of 5 V or less.

5.5 Complete PLL Transient Testing across Temperature

The complete PLL was tested in several ways from 25 to 300 ℃. These tests included frequency step tests to check the transient response, and long duration acquisitions to determine operating range and jitter at different frequencies and temperatures. The PFD + charge pump gain was also estimated to be 5.5 μA from the testing in section 5.2, while the VCO was still estimated to be 550 kHz/V below frequency saturation. Table XII shows a comparison between the estimated PLL parameters and the designed parameters from Table X. Due to the jitter, the 2% settling time standard provided less information about the control loop performance. To overcome this, the lock time was re-estimated for a 5% settling time calculation [52]. All settling times in this chapter use the 5% measurement standard.

TABLE XII.
PHASE-LOCKED LOOP PARAMETER ESTIMATION AFTER MEASUREMENTS

PLL Design Parameter	Symbol	Equation	Intended Value	Designed Value
Chosen Values	C	N/A	54 pF	54 pF
	R		41.7 kΩ	41.7 kΩ
	$K_P \cdot K_D$		5.0 μA	5.5 μA
	K_O		3.46 Mrad/V (550 kHz/V)	3.46 Mrad/V (550 kHz/V)
Natural Frequency	ω_n	$\sqrt{\frac{K_P K_O}{C}}$	566 krad/s (90.0 kHz)	593 krad/s (94.4 kHz)
Damping Ratio	ζ	$\frac{\omega_n RC}{2}$	0.637	0.668
Lock Range	$\Delta\omega_L$	$\approx 4\pi\zeta\omega_n$	4.53 Mrad/s (721 kHz)	4.98 Mrad/s (793 kHz)
Lock Time (5% settling time)	T_L	$\approx \frac{3}{\zeta\omega_n}$	8.32 μs	7.57 μs

TABLE XII Cont.

Pull-out Range	$\Delta\omega_P$	$\approx 11.55\omega_n(\zeta + 0.5)$	7.43 Mrad/s (1.18 MHz)	8.00 Mrad/s (1.27 MHz)
Pull-in Time	T_P	$\Delta\omega_0 \frac{C}{K_P K_O \pi}$	995 fs * $\Delta\omega_0$ (≥ 7.39 μs)	904 fs * $\Delta\omega_0$ (≥ 7.24 μs)

At room temperature, the PLL showed phase-lock across a relatively narrow band of 700 kHz – 1.1MHz. At design time, the goal was 500 kHz – 5 MHz, but this was never achieved. In general, the loop filter bandwidth was higher than desirable at all operating frequencies, and this limited the low frequency operation of the PLL across all temperatures. The minimum stable frequency of 600 kHz (observed 100 ℃) is only 6.35 times the estimated natural frequency of 94.4 kHz.

At the higher operating frequencies, at least two effects came into play. The shift in PFET threshold voltage affected the maximum operating frequency of the VCO, but this maximum frequency was still observed to be around 2-2.5 MHz in simulations and measurements. The PLL was only able to obtain lock up to around 1.1 MHz at room temperature, and higher frequencies with increasing temperature. Fig. 5.10 and Fig. 5.11 show the jitter of the PLL at 25 and 100 ℃, where it was measured to be nearly +/- 1%. At 200 ℃, the jitter begins to exceed 2% as shown in Fig. 5.12. Spontaneous loss of lock was even observed at 1.3 MHz and 200 ℃ (Fig. 5.13). Performance continues to degrade at 300 ℃ (Fig. 5.14), and the PLL even fails to lock at 1.3 MHz (Fig. 5.15).

Two factors could be contributing to a reduction in loop stability at higher temperatures: increased noise or increased gain. The work done on noise in 4H SiC is very limited, however it has been observed that low-frequency and 1/f noise increased with temperature [53]. With higher

loop gain comes a higher natural frequency and a decrease in stability. Despite this, noise must be the primary suspect in the degradation of the PLL behavior at increasing temperature.

There are several reasons for this. First, the gain at 300 ℃ is actually lower than the gain at 25 ℃, so another effect that is proportional to temperature (such as thermal noise) must be a factor. Second, the increased gain observed would tend to destabilize lower frequencies, not higher frequencies, but the greatest loss in jitter performance was observed at higher frequencies, so it is not an increase in the natural frequency leading to a loss of phase locking capability. Although it may seem counter-intuitive that low-frequency and 1/f noise are the likely issue at higher frequencies, this is a characteristic of PLLs. The control loop is able to tightly control the system within its bandwidth, so the output noise of the PLL is attenuated at lower frequencies, but above the loop bandwidth, the system noise sources cannot be attenuated by the loop.

At this time, no noise model for the Raytheon HTSiC FETs exists, as this requires advanced equipment to measure the device noise. The input devices for the VCO were also small, with W/L = 20 μm/2 μm, m=1, and therefore susceptible to noise. The only safe approach would be to increase the device size in the VCO to reduce the overall noise.

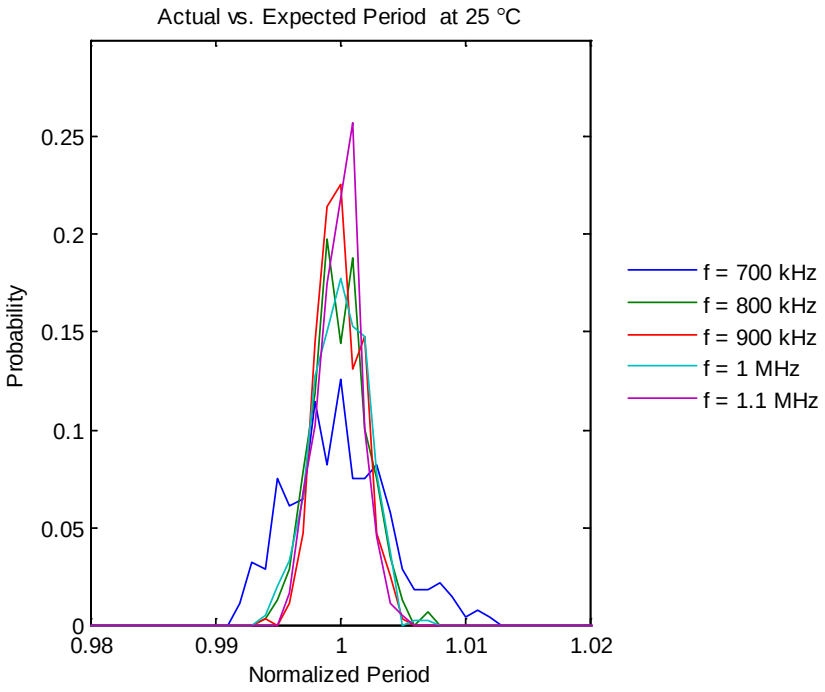


Fig. 5.10. Jitter at 25 ℃.

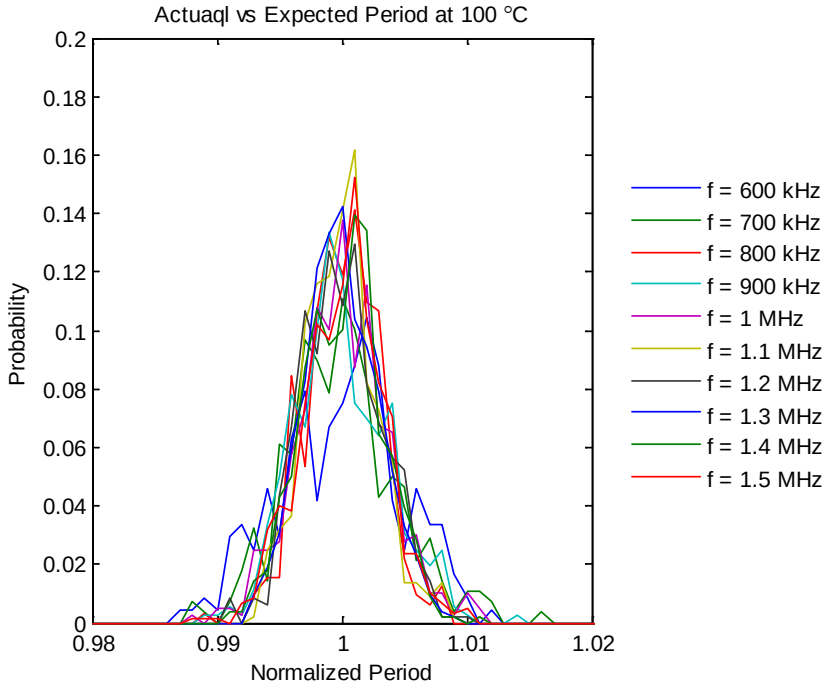


Fig. 5.11. Jitter at 100 ℃.

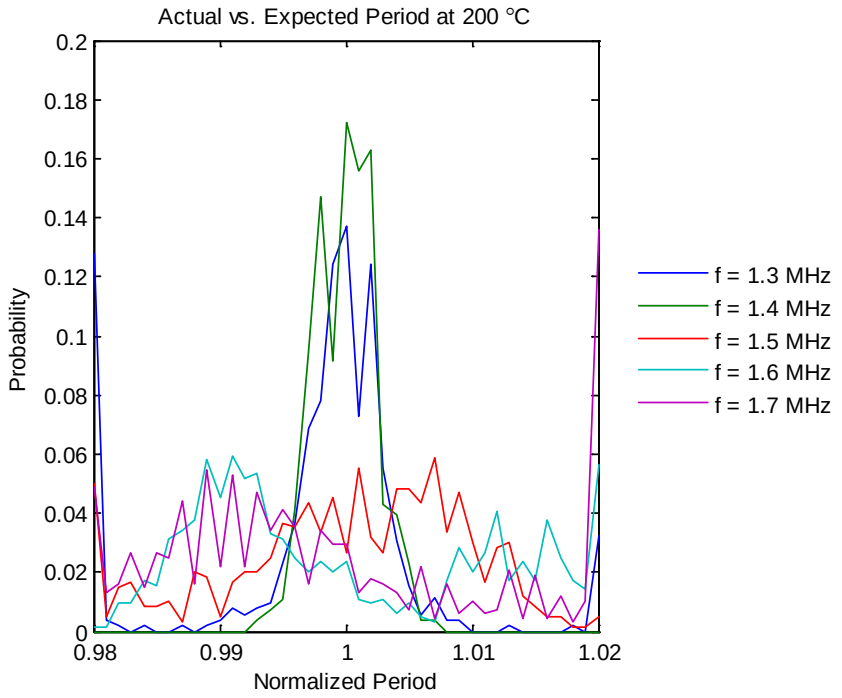


Fig. 5.12. Jitter at 200 ℃.

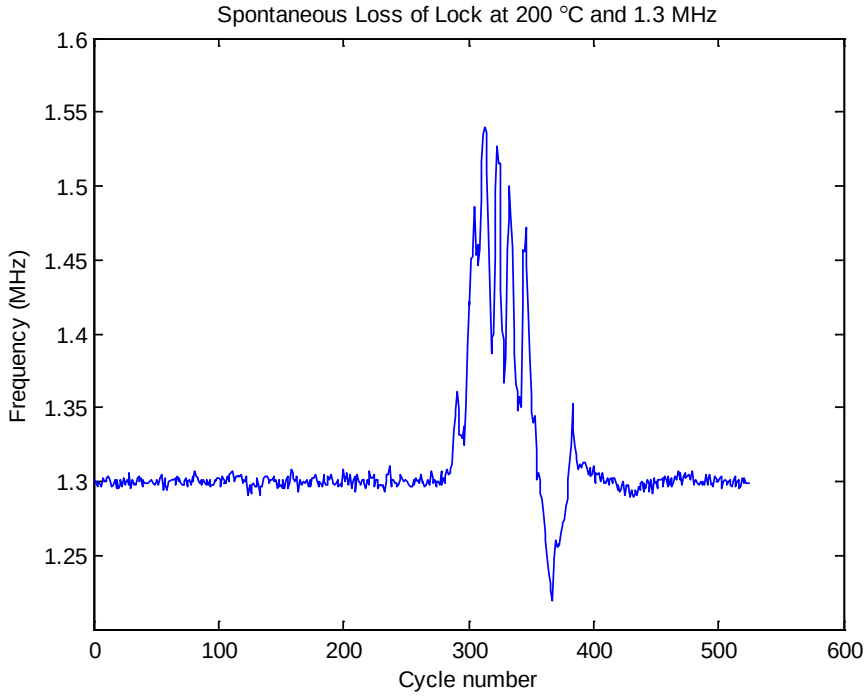


Fig. 5.13. Spontaneous loss of lock at 200 ℃.

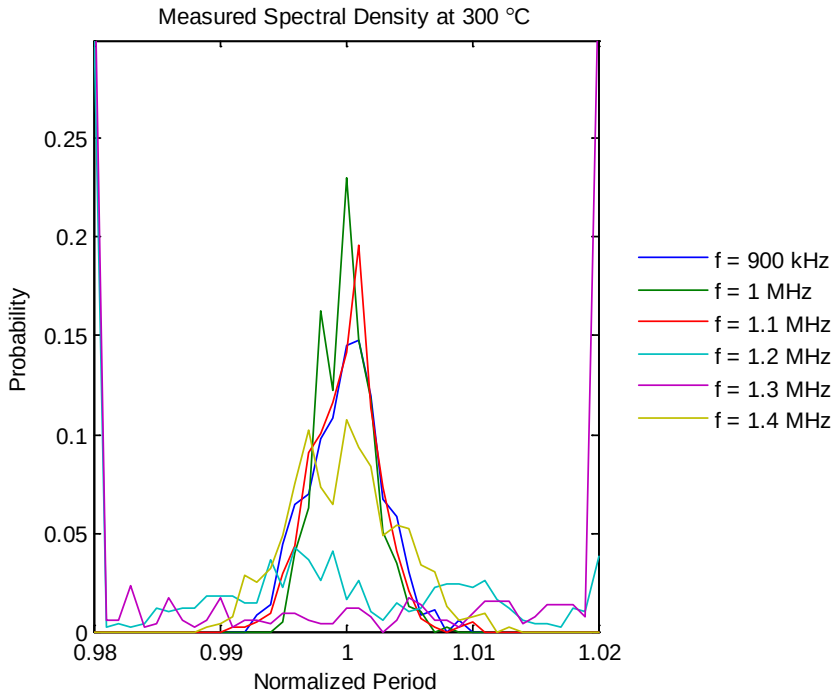


Fig. 5.14. Normalized jitter at 300 ℃.

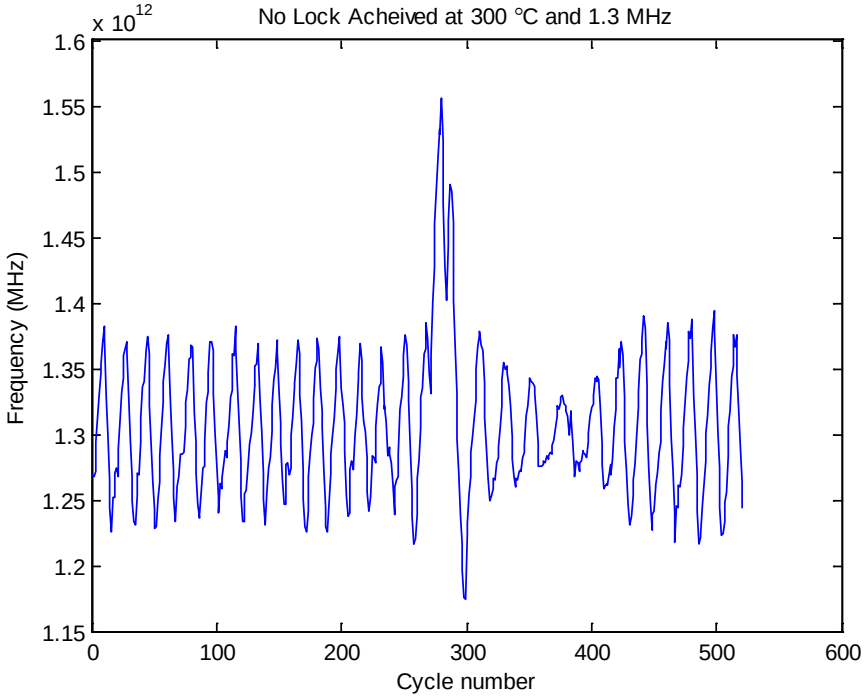


Fig. 5.15. Failure to lock at 300 ℃.

For the frequency step tests, a step size of 200 kHz was used. Fig. 5.16 compares the simulated step response with the pre- and post-tapeout models at 100 ℃. There is only a minimal difference in the behavior of the step response, again demonstrating that the overall PLL topology is very resilient to device parameter shifts. The actual step responses, shown in Fig. 5.17 through Fig. 5.20, show some features very different than the simulated responses.

First is the occurrence of negative-slope periods during the step response rise-time seen in Fig. 5.17 and Fig. 5.18. The theory of operation for the PFD with a charge-pump output is that it will never have these negative-slope regions during the rise-time, but this theory is based on having a perfect 1^{st}-and-3^{rd} quadrant gain plot like that seen in Fig. 4.4. When a JK flip-flop is used as a phase detector, it has a sawtooth transfer function which falls in all four quadrants, and the acquisition of phase-lock shows brief negative-slope regions as the input phase difference rolls over π or $-\pi$ [10]. This suggests that the regions of 2^{nd}-and-4^{th} quadrant operation in Fig. 4.6 are larger than the plot shows, and that this behavior is having a real effect on the PLL. The greater concern is that these negative-slope regions demonstrate that the circuit is slipping cycles, and therefore no longer in lock. Thus, the settling time cannot be compared directly to the hand-design calculations in Table XII.

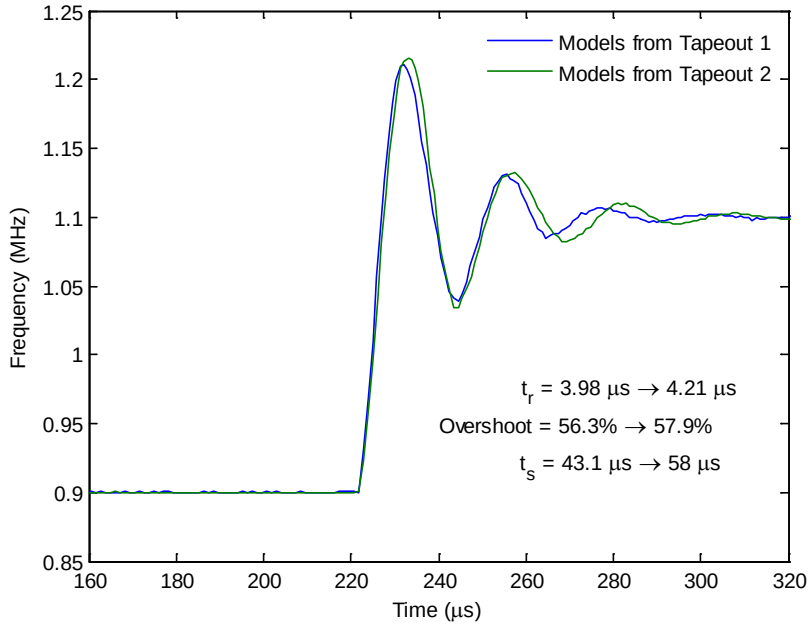


Fig. 5.16. Simulated Step Response at 100 ℃ for the original models, and the BSIM4 models generated from Tapeout 1 devices (Tapeout 2 models).

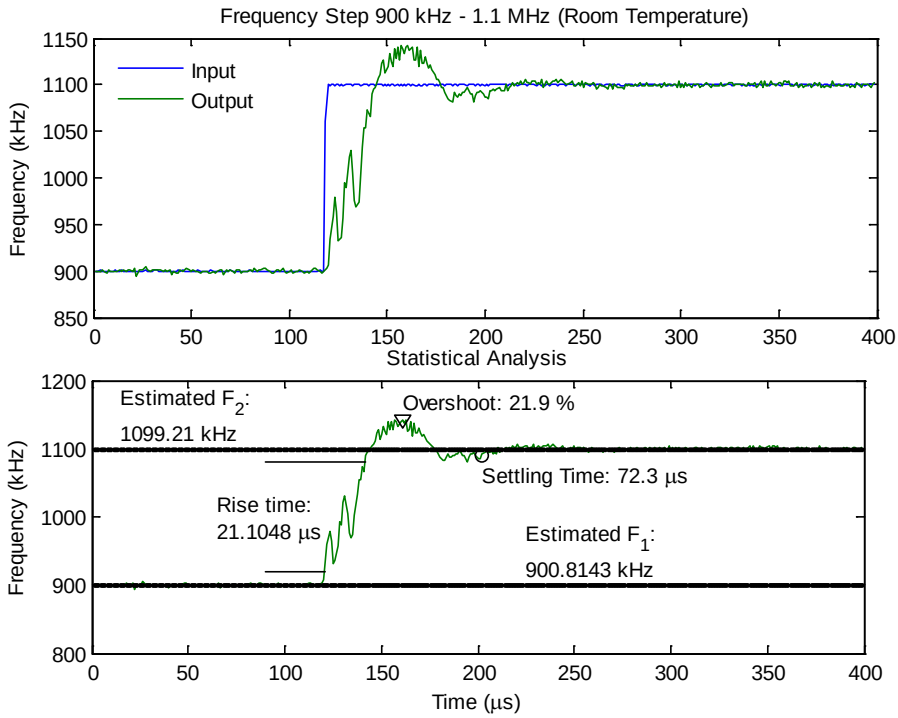


Fig. 5.17. Step Response of the PLL at room-temperature.

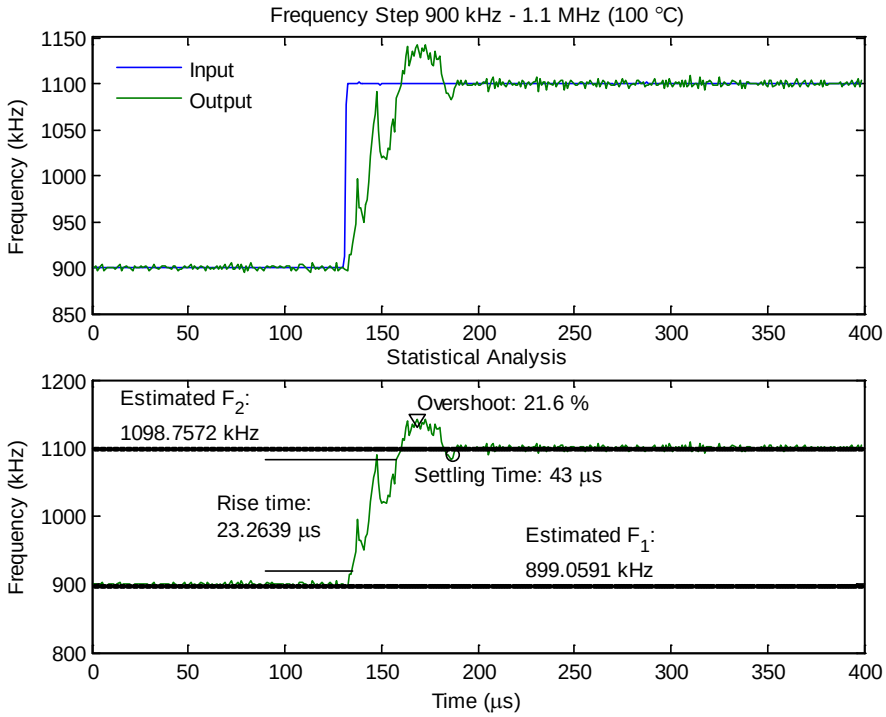


Fig. 5.18. Step Response of the PLL at 100 ℃.

At 200 and 300 ℃, several other phenomena are visible. At these temperatures, the PLL did not lock at 900 kHz, so the test was performed at 1.4-1.6 MHz. At 200 ℃, a spontaneous loss of lock is observed again during the step test as it was during the jitter test. Also at 200 ℃, the overshoot has risen to 50 %, and the rise time has been cut nearly in half with respect to the 25 and 100 ℃ measurements. This demonstrates a performance much closer to the simulated behavior from Fig. 5.16. Finally, at 300 ℃, the PLL is stable at 1.4 MHz, but after the step it oscillates above and below the input frequency for the entire observation period. The period of the frequency oscillation is 49 kHz, roughly half the predicted natural frequency in Table XII, and consistent with the transient behavior shown at 25 and 100 ℃.

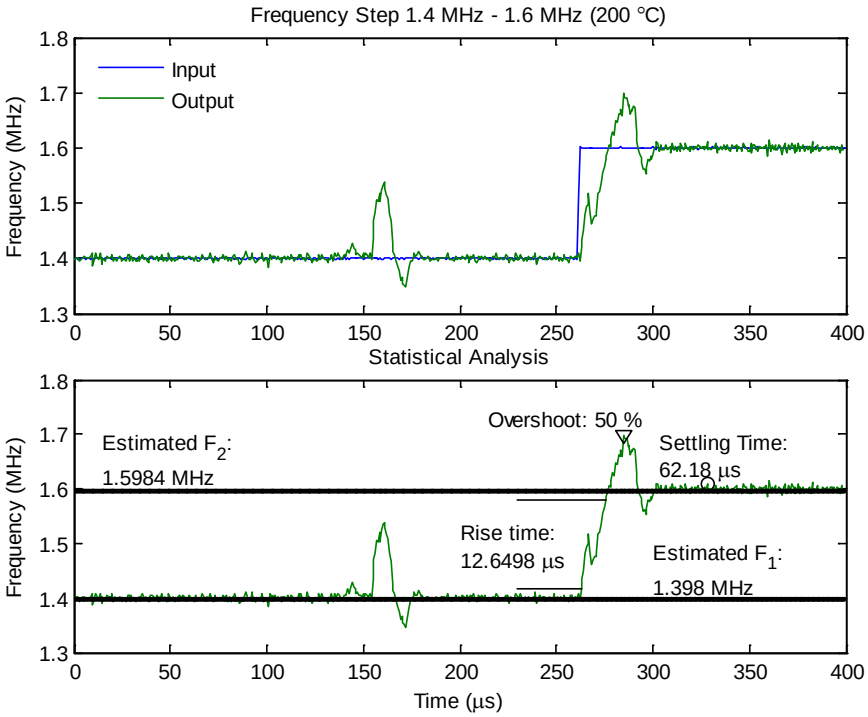


Fig. 5.19. Step Response of the PLL at 200 ℃.

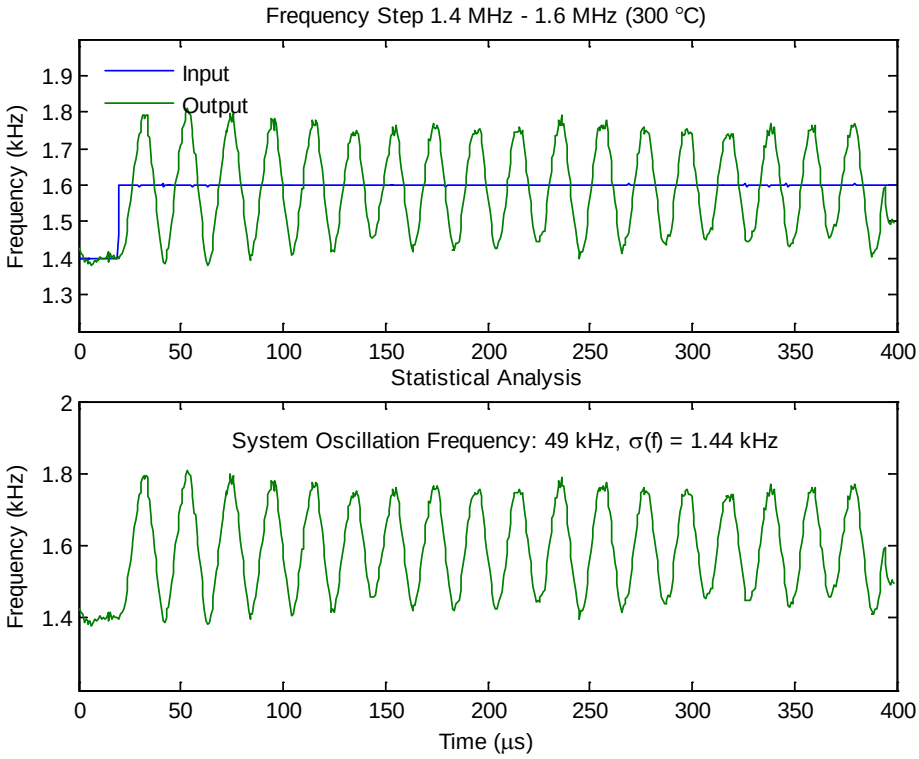


Fig. 5.20. Step Response of the PLL at 300 ℃.

CHAPTER 6 – IMPROVED DESIGN OF A SIC PHASE-LOCKED LOOP

With the experience of the first tapeout, and the observations from testing, an improved design for the PLL was undertaken. The improved design had two specific goals: improve the PLL stability at high temperature, and increase the stable operating range of the PLL. These goals were achieved through several specific steps and additional design work. Several basic tasks were performed in the process of updating the blocks:

1. Rebalance the N- and P-FET ratios based on new device data.
2. Reduce L on all "digital" devices to the 1.2 µm minimum.
3. Maximize common-centroid layout on all devices with m ≥ 4.

The first step was informed by measurements made on the test devices soon after the wafers arrived. It was observed that, at gate-source voltage of -10 V, the 20 µm/2 µm PFET was only sourcing around 12-13 µA, whereas the NFETs were sinking 50 µA at 5 V. To compensate for the large difference in output current, an NFET-PFET sizing ratio of 1:8 was chosen for all "analog" devices. Fig. 6.1 shows the measured output characteristics for the NFET and PFET 20 µm/2 µm device.

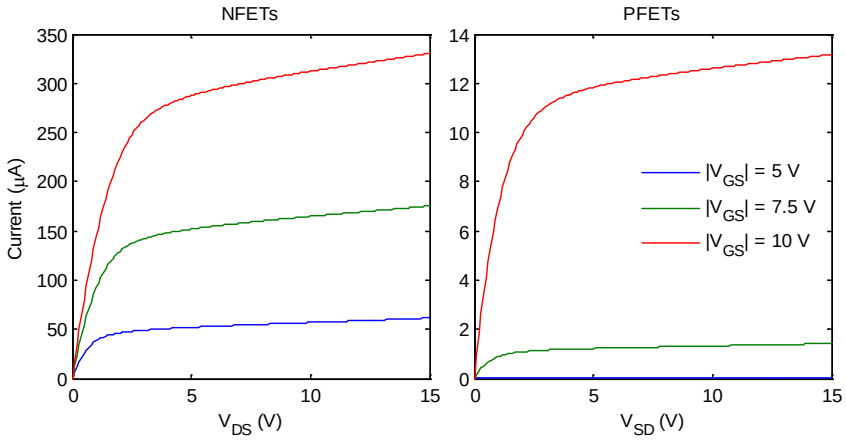


Fig. 6.1. Comparison of Drain current between NFETs and PFETs (W/L = 20 µm/2 µm).

6.1 Modifications to the PFD

The PFD block level schematic was unchanged from Tapeout 1 (Fig. 4.3). Improvements to this circuit were limited to changes inside the logic gates and an improved layout. Originally, this circuit was designed with L = 1.5 μm devices to be conservative, but in the first tapeout, the length 1.2 μm devices had good yield and higher drive strength than the L = 1.5 μm devices, even accounting for the length difference. The digital device lengths were also reduced to 1.2 μm to increase the digital circuits' speed. The NFET-PFET ratios in the gates were also set to 1-to-5 consistent with circuits designed by the digital designers. With shorter devices, the width could also be reduced for equal current drive. The unit NFET device was chosen to have W/L of 4 μm/1.2 μm, and the unit PFET had W/L = 20 μm/1.2 μm, keeping the multiplicity for both devices the same. These changes shrunk the PFD from 425 μm wide by 300 μm tall to 375 μm by 300 μm. With additional space inside the blocks, the signal routing was simpler, and the path lengths into the NAND4 had less disparity between the two symmetric halves of the circuit.

At room temperature, where the devices are slowest, the PFD gain function stays in the first and third quadrant up to around 2 MHz as shown in Fig. 6.2. At 4.7 MHz, the gain no longer stays in the first and third quadrant, but still behaves well enough to function like a JK flip flop PFD in the PLL, as seen in Fig. 6.3. At 10 MHz, the gain no longer resembles a PFD. It can also be seen in Fig. 6.2 that the gain peak in the first quadrant has a larger magnitude than the gain peak in the third quadrant (0.9 vs – 0.63). These results are from the parasitic extracted netlist, and the discrepancy is due to the difference in path lengths between the two symmetric sides of the circuit. The DN output is more affected by parasitics and has a shorter duty cycle than the UP output for the same magnitude of phase offset.

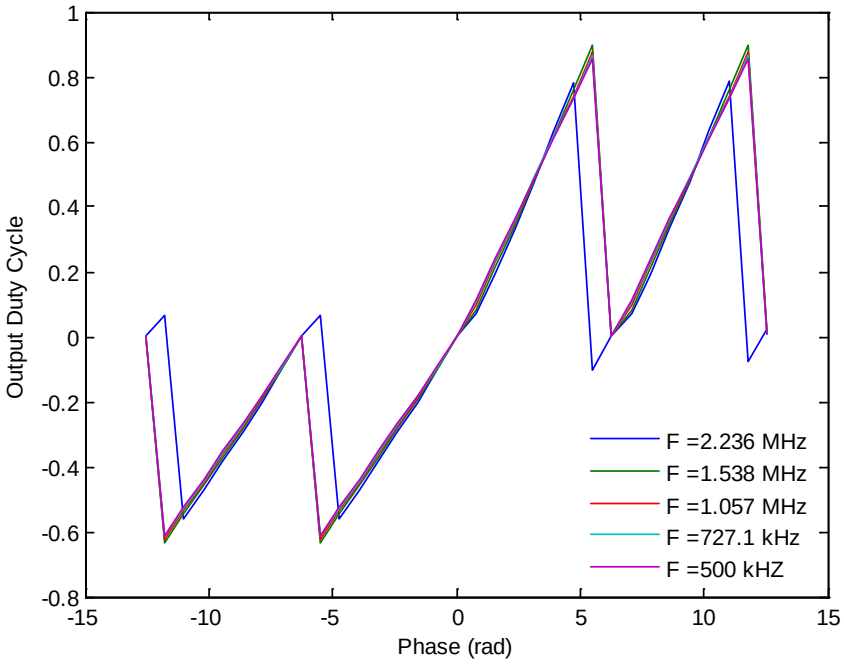


Fig. 6.2. PFD Gain at room temperature up to 2.2 MHz.

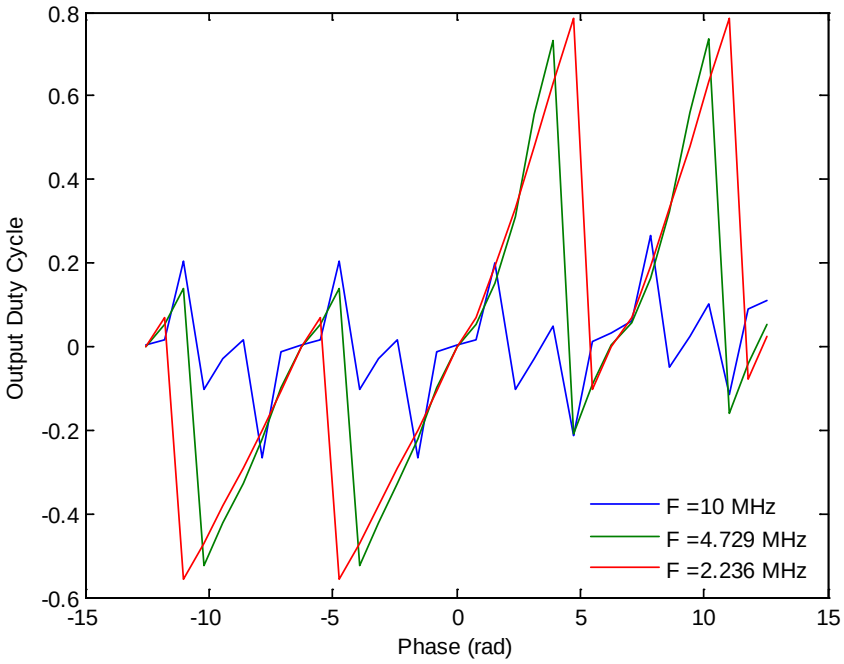


Fig. 6.3. PFD gain at room temperature and 2.2 MHz and above.

6.2 Modifications to the Charge Pump

The modifications to the charge pump were similar in nature to the changes to the PFD. The PFET-NFET ratio was rebalanced to 8-to-1 as mentioned previously. The control devices were reduced to L = 1.2 µm, but given a total width of 40 µm to keep the current density from becoming too high. The modified schematic is shown in Fig. 6.4.

The updated charge pump was simulated at a range of frequencies as shown in Fig. 6.5. At room temperature, the charge pump has a fairly linear transfer function, but at 1.35 MHz and above, the negative portion of the transfer function is compressed into the first 0-50% of the DOWN input duty cycle, and above 50%, the output is saturated.

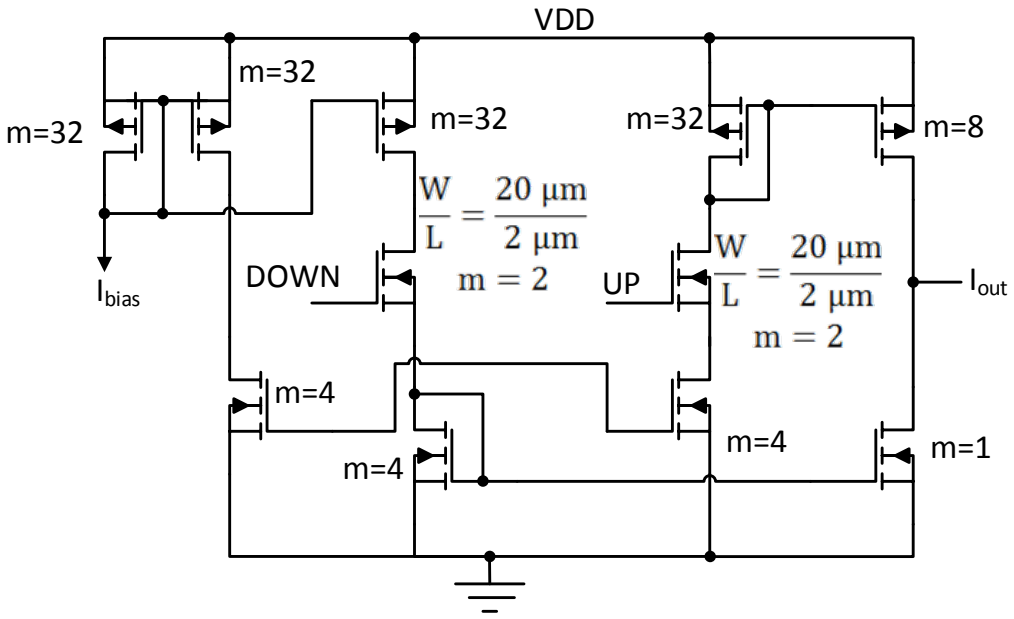


Fig. 6.4. Updated charge pump schematic for tapeout 2.

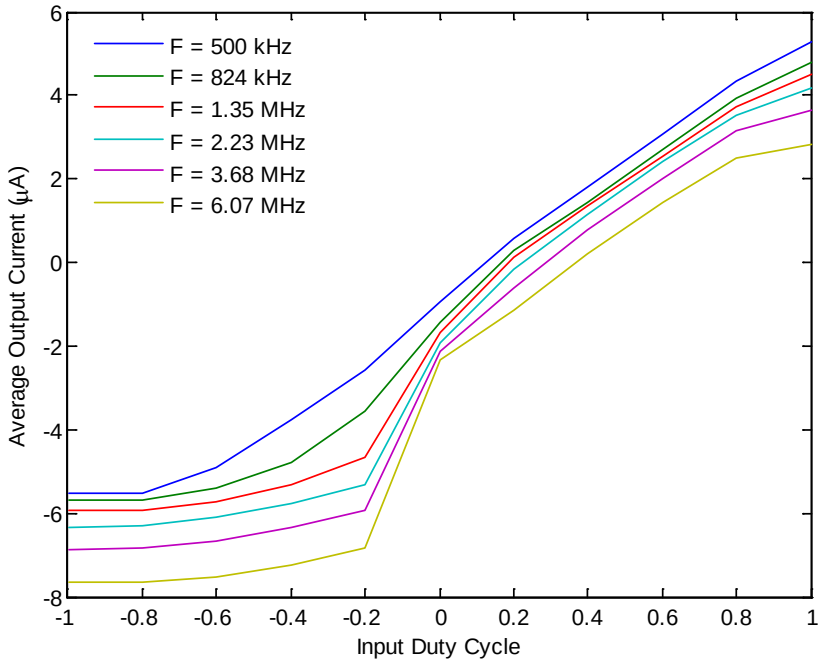


Fig. 6.5. Simulated charge pump transfer function with parasitics for tapeout 2.

6.3 Modifications to the VCO

Several modifications were made to the VCO with the goal making the maximum frequency close to the original design goal, while also reducing the noise. The complete block diagram and block schematics are shown in Fig. 6.6 and Fig. 6.7. First, the number of stages was increased from 3 to 4. This should slightly reduce the gain since the frequency of oscillation is $\propto 1/N$. This should also improve the jitter by a small amount since there are now four noise sources averaged instead of three.

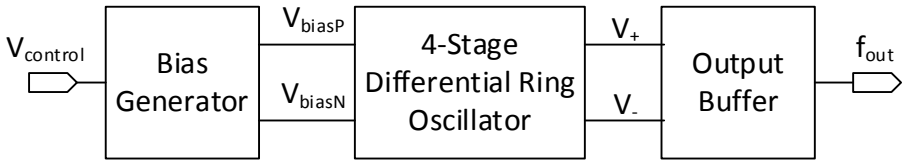


Fig. 6.6. Updated block diagram of the tapeout 2 VCO.

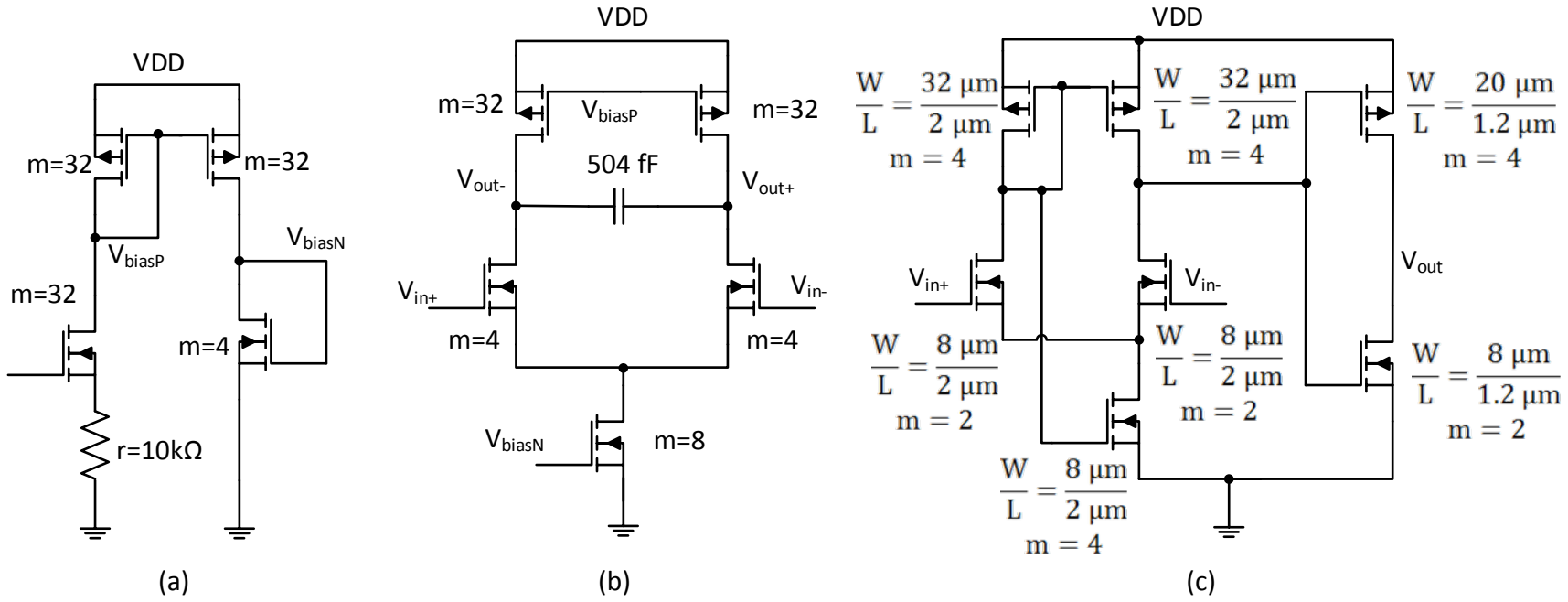


Fig. 6.7. Updated Block Schematics for the VCO for tapeout 2. (a) Bias generator (b) Differential delay stage, and (c) output buffer.

In redesigning the VCO, the most difficult design choice was selecting a new value for the bias resistor. The significant increase in the PFET threshold from the earlier models meant that the active swing of $V_{control}$ would be lower than originally expected in Chapter 4. In order to reach a maximum frequency of 4-5 MHz, the VCO gain would have to be increased. As shown in Chapter 4 and Chapter 5, increasing VCO gain leads to challenges with a loop frequency that is too high. Ultimately, the value of 10 kΩ was chosen during an iterative tuning process and was affected significantly by the maximum area allowed for the primary loop capacitor, which is described later.

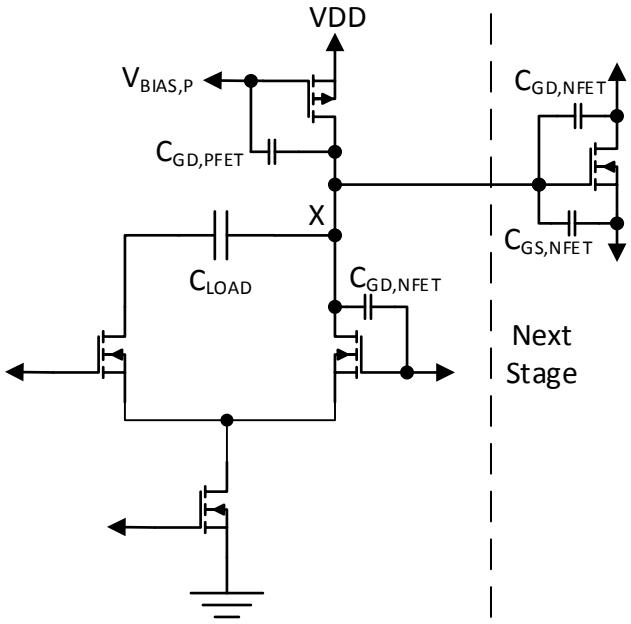


Fig. 6.8. Significant capacitances in the differential delay stage for tapeout 2.

The load capacitor was also changed from two single-ended load capacitors to one differential capacitor. The number of device drains connected to each node also increased significantly from tapeout 1, making the parasitic capacitance a larger factor in the oscillation frequency. Fig. 6.8 shows the load capacitor along with the four primary parasitic capacitances

that affect the oscillation frequency. The gate-drain capacitance of the load PFET is the simplest to analyze, because the device is nearly always in saturation and this capacitor connects to a DC biased node. This capacitance is the overlap capacitance of the PFET which has 32 fingers of width 20μm:

$$C_{PFET} = m * W * C_{OV} = m * W * \frac{1}{2}\mu m * 0.86\frac{fF}{\mu m^2} = 275.2\ fF.$$

The contribution of the two NFET devices is more complex. The gate-drain capacitances of both the current stage's input device as well as the next stage's input device are significant, and both have four fingers of width 20 μm. The largest contributor from the NFETs is the gate-source capacitor of the next-stage input device. All three of these devices are transitioning between off, triode, and saturation, and there are different phase shifts to the voltages on the opposite sides of the capacitors, so a simple estimation of their effective load is not possible like it is with the PFET.

With the intentional capacitor placed between the output nodes, the voltage swing changes from 0 to *VDD* to –*VDD* to +*VDD*, causing an effective doubling of the load capacitance. The PFET capacitor has a swing of only *VDD* so is not doubled.

$$f_{osc} = \frac{K(V_{control} - V_{GS})}{R \cdot N \cdot C \prime \cdot VDD} \qquad (6.1)$$

$$\frac{df_{osc}}{dV_{control}} = \frac{K}{R \cdot N \cdot C \prime \cdot VDD} \qquad (6.2)$$

$$\frac{d\omega}{dV_{control}} = \frac{2\pi K}{R \cdot N \cdot C \prime \cdot VDD} \qquad (6.3)$$

For tapeout 2, the value of the bias resistor was 10 kΩ, C_{LOAD} was 504 fF, four stages were used, and the bias current was not halved as in the previous design. If Eq. (6.3) is used to estimate the VCO gain assuming that *C'* is simply $2*C_{LOAD}$, the expected value is 1.54 MHz/V. If *C'* includes C_{PFET} also, it is approximately 1.28 pF and the gain is expected to be 1.30 MHz/V. The simulated performance of the VCO, shown in Fig. 6.9 and Fig. 6.10, indicates a gain range from 600 kHz/V to 1 MHz/V, suggesting that the contribution of the NFET parasitic capacitances is likely on the order of the contribution of the PFET gate-drain capacitance.

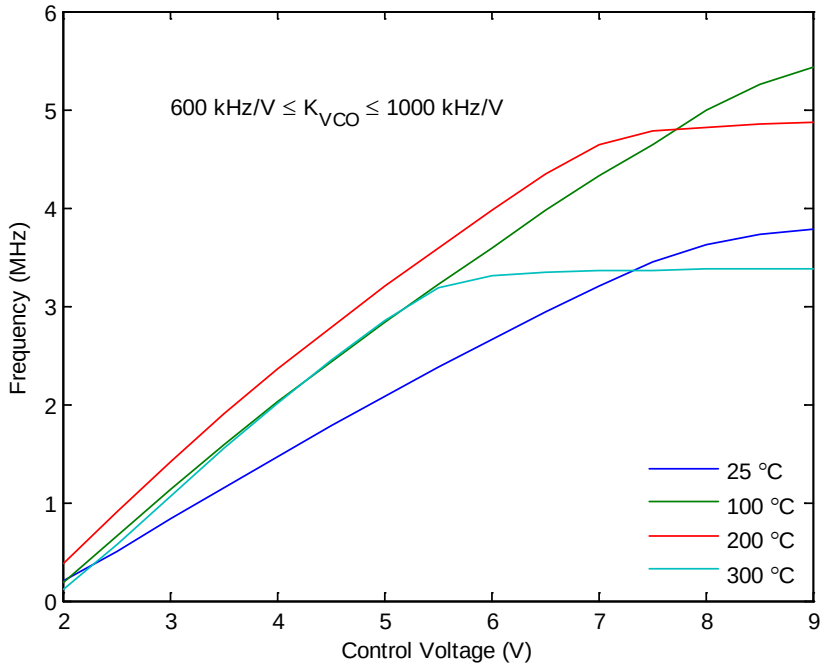


Fig. 6.9. VCO Transfer Function for tapeout 2.

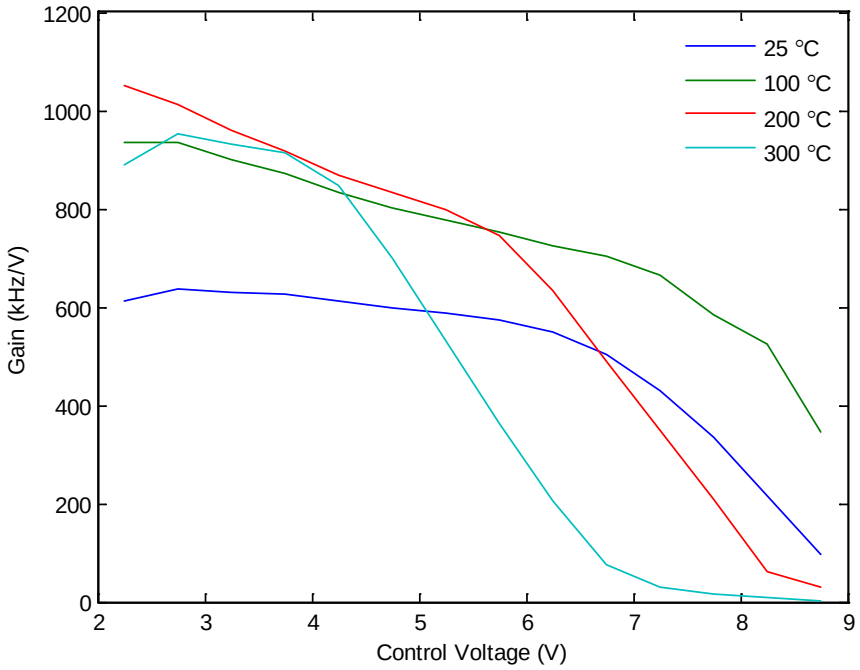


Fig. 6.10. VCO gain vs control voltage for tapeout 2.

6.4 Complete System Design

The PLL design for tapeout 2 was informed by the results observed in Chapter 5. First and foremost, it was desired to make the loop more stable at high temperatures. Since the primary suspect in the high-frequency instability was device noise, all devices in the VCO delay cells were made larger. The input NFETs were made larger by a factor of four, and the load PFETs were made larger by a factor of 16. This means the 1/f noise which is $\propto 1/\text{Area}$, will be reduced by a factor of two or more depending on the contributing sources.

As previously discussed, the VCO gain was made approximately 50% larger. (At 25 ℃ gain went from 400 kHz/V to 600 kHz/V, and at 200 ℃ gain went from 700 kHz/V to 1MHz/V.) In order to compensate for this, and reduce the loop bandwidth further, the primary loop capacitance was increased from 54 pF to 141.75 pF, an increase of 163%. Combining these two

changes, the natural frequency of the loop for Tapeout 2 is estimated to be 75.6% of that designed in tapeout 1.

TABLE XIII.
COMPARISON OF PHASE-LOCKED LOOP DESIGNS FOR TAPEOUT 1 AND TAPEOUT 2

PLL Design Parameter	Symbol	Equation	Tapeout 1	Tapeout 2
Chosen Values	C	N/A	54 pF	142 pF
	R		41.7 kΩ	22.2 kΩ 44.4 kΩ
	$K_P \cdot K_D$		5.5 μA	5.5 μA
	K_O		3.46 Mrad/V (550 kHz/V)	5.18 Mrad/V (714 kHz/V)
Natural Frequency	ω_n	$\sqrt{\frac{K_P K_O}{C}}$	566 krad/s (90.0 kHz)	448 krad/s (71.4 kHz)
Damping Ratio	ζ	$\frac{\omega_n RC}{2}$	0.637	0.707 1.414
Lock Range	$\Delta\omega_L$	$\approx 4\pi\zeta\omega_n$	4.53 Mrad/s (721 kHz)	3.98 Mrad/s (633 kHz) 7.95 Mrad/s (1.27 MHz)
Lock Time	T_L	$\approx \frac{2\pi}{\omega_n}$	11.1 μs	14.0 μs
Pull-out Range	$\Delta\omega_P$	$\approx 11.55\omega_n(\zeta + 0.5)$	7.43 Mrad/s (1.18 MHz)	6.25 Mrad/s (994 KHz) 9.9 Mrad/s (1.58e-06)
Pull-in Time (Minimum Pull-in Time)	T_P	$\Delta\omega_0 \frac{C}{K_P K_O \pi}$ $(T_P * \Delta\omega_P)$	995 fs * $\Delta\omega_0$ (≥ 7.39 μs)	1.58 ps * $\Delta\omega_0$ (≥ 9.88 μs) (≥ 15.6 μs)

The other change to the loop design was to select a different damping ratio. Fischette recommends lower damping ratios for low jitter, and higher damping ratios for improved input phase tracking [51]. The resistance can be selected based on the desired damping ratio:

$$R = \frac{2\zeta}{\omega_n C}.$$

Since the PLL does not have a specific function in mind, damping ratios above and below one were explored, and *R* values of 22.2 kΩ and 44.4 kΩ were investigated, giving estimated damping ratios of 0.707 and 1.414, respectively. Table XIII shows the changes in the design from tapeout 1 to tapeout 2.

Simulations demonstrated that the PLL behavior is still not following theory well. At 25 ℃, the PLL with the lower damping ratio just slips one cycle (losing frequency lock) during the 200 kHz step. This can be seen in Fig. 6.11 where the instantaneous frequency drops for a short period. The frequency step of 200 kHz is 5 times lower than the hand calculations suggest that this circuit should lose lock. If the lock range is calculated assuming K_O of 600 kHz/V, the expected lock range is still nearly 600 kHz, three times the actual step. At 100 ℃, both versions of the loop have enough gain to maintain frequency lock. Fig. 6.12 shows that the smaller damping resistor does show more overshoot and less jitter as expected.

The transient response of the PLL will be driven by the VCO, charge pump, and loop filter. Since the redesign of the PFD will increase its speed, the charge pump transient response is the likely culprit for cycle-slipping at lower frequency steps. (The design equations assume infinite bandwidth for the PFD and charge pump, which is a major assumption in any SiC IC.)

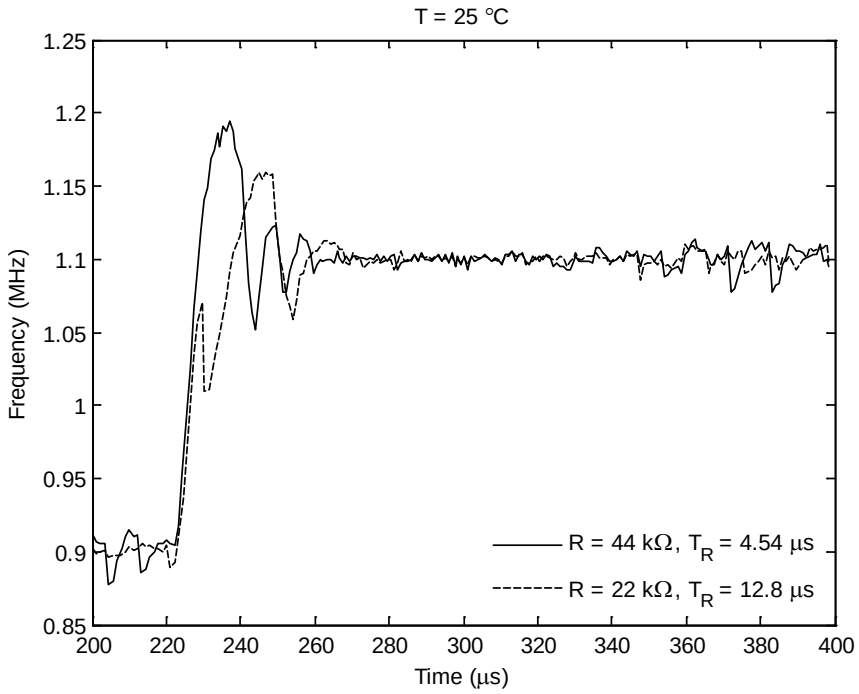


Fig. 6.11. Frequency step at 25 ℃ with two different values of damping resistor.

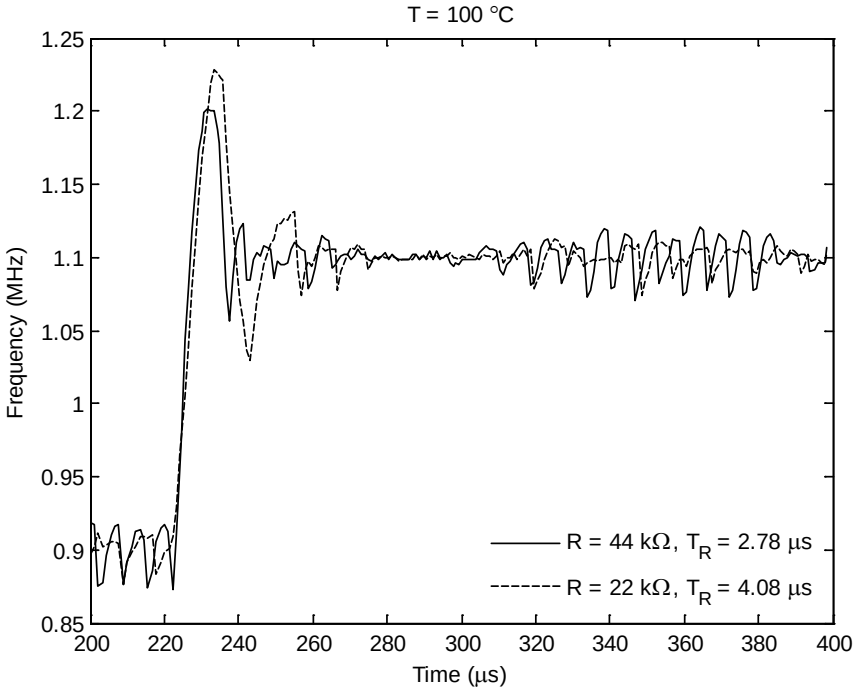


Fig. 6.12. Frequency Step at 100 ℃ with two different values of damping resistor.

Ultimately, it was chosen to go with a larger value of damping resistor in order to attempt to reduce overshoot and cycle slipping at the expense of larger output frequency ripple. The scope of this change was much lower risk than trying to design a new charge-pump topology which improved the speed while still meeting all of the design heuristics. The final layout value for the resistor was 42.2 kΩ (well within the precision of the process). The behavior of the loop at 1 MHz can be seen in Fig. 6.13 and Fig. 6.14. Both figures show an output frequency variation of +2% to -4%, but no cycle slipping is visible, and the total frequency excursion of the phase input step of 90° is only 7%.

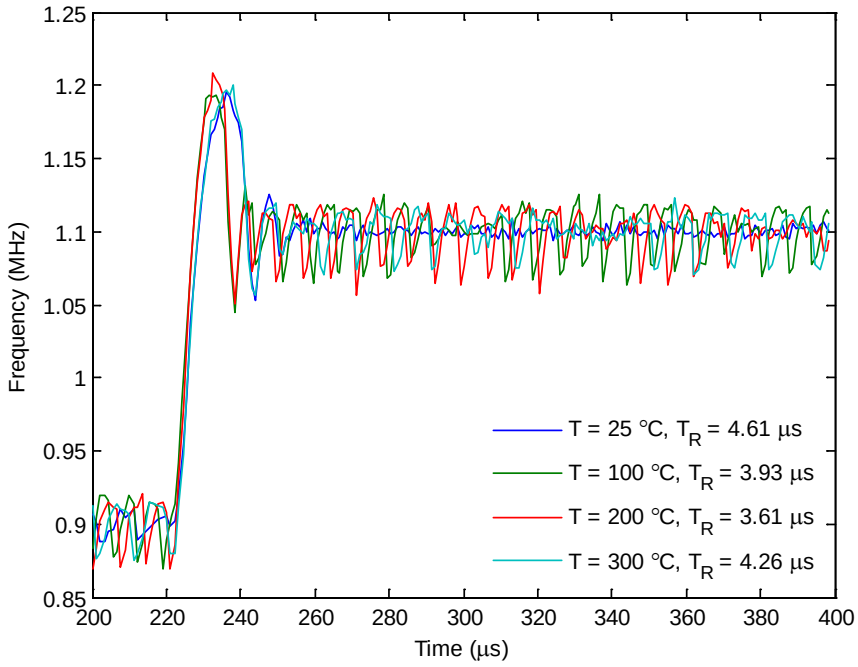


Fig. 6.13. Frequency Step Response of the PLL for Tapeout 2 with an input frequency step from 900 kHz to 1.1 MHz.

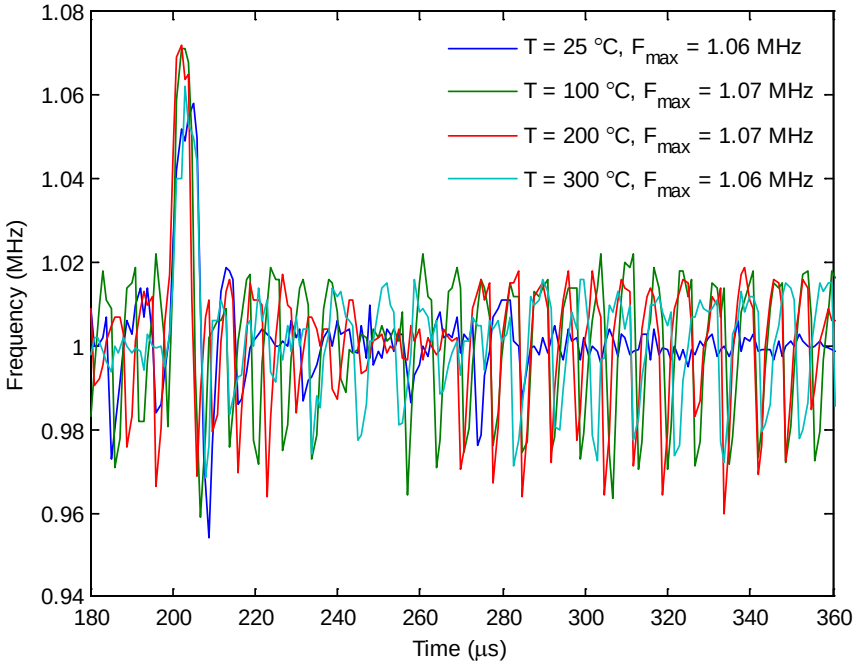


Fig. 6.14. Phase Step Response of the PLL with an input frequency phase step of 90°.

Finally, the frequency step was simulated at 2 MHz (Fig. 6.15). At this frequency, the hand-calculated filter frequency was less than 5% of the operating frequency, suggesting that PLL theory should hold much better. The overshoot was still 50%, and at 300 ℃ there is still cycle slipping during lock. Despite this, the loop filter frequency is low enough relative to the operating frequency that systemic ripple drops well below 1%. This, along with the improvements in expected VCO jitter, indicate that the design is well-suited for operation at this frequency.

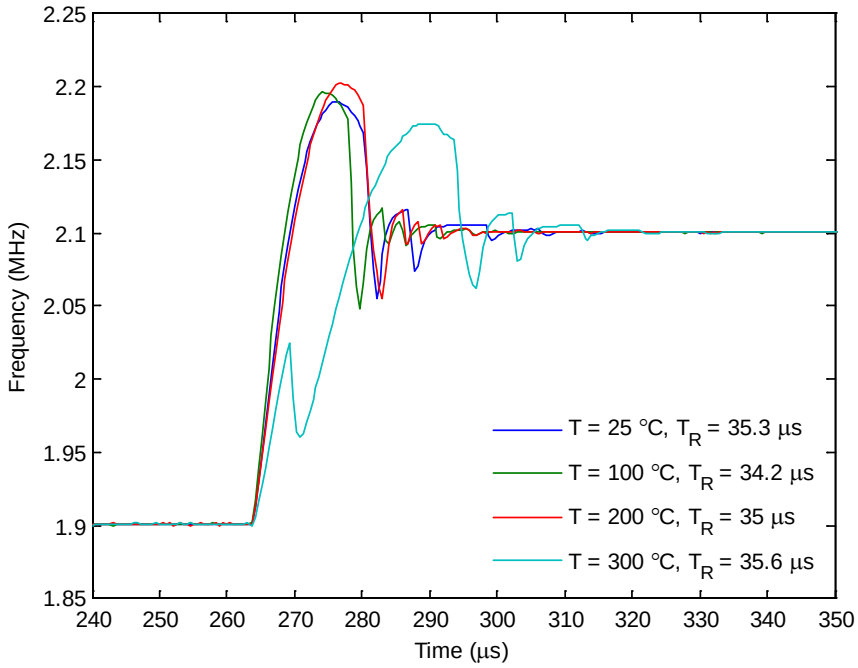


Fig. 6.15. Frequency step response of the PLL for Tapeout 2 with an input frequency step from 1.9 MHz to 2.1 MHz.

6.5 PLL Layout for Tapeout 2

The components of the PLL for Tapeout 2 are shown in Fig. 6.16 through Fig. 6.17. In the case of the PFD, the layout shrunk slightly due to the smaller logic gates. However, in the case of both the charge pump and VCO, the areas grew due to larger device multiplicities. This did provide the opportunity to use common-centroid layout techniques which were not practical during Tapeout 1. The complete PLL layout is shown in Fig. 6.19. The complete circuit is 1175 µm wide by 900 µm tall, of which, approximately 40% is the primary loop capacitor. The VCO has also grown from taking up less than a quarter of the layout to nearly 40% itself. While this is not desirable, it is reasonable since the VCO is the primary analog component in the loop.

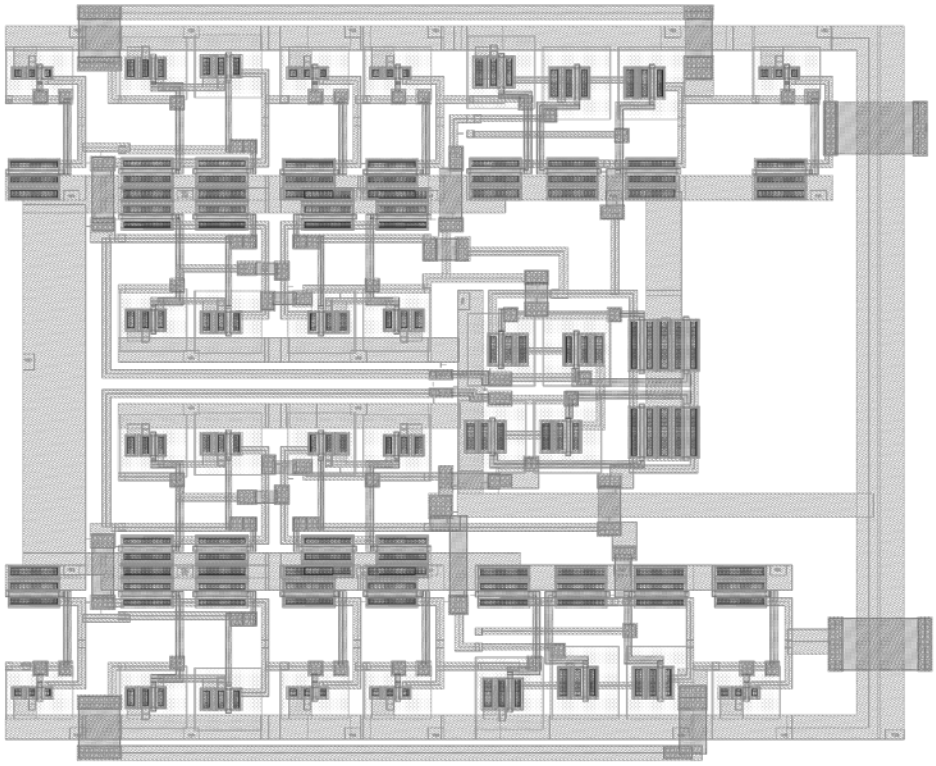


Fig. 6.16. Layout of the PFD for Tapeout 2.

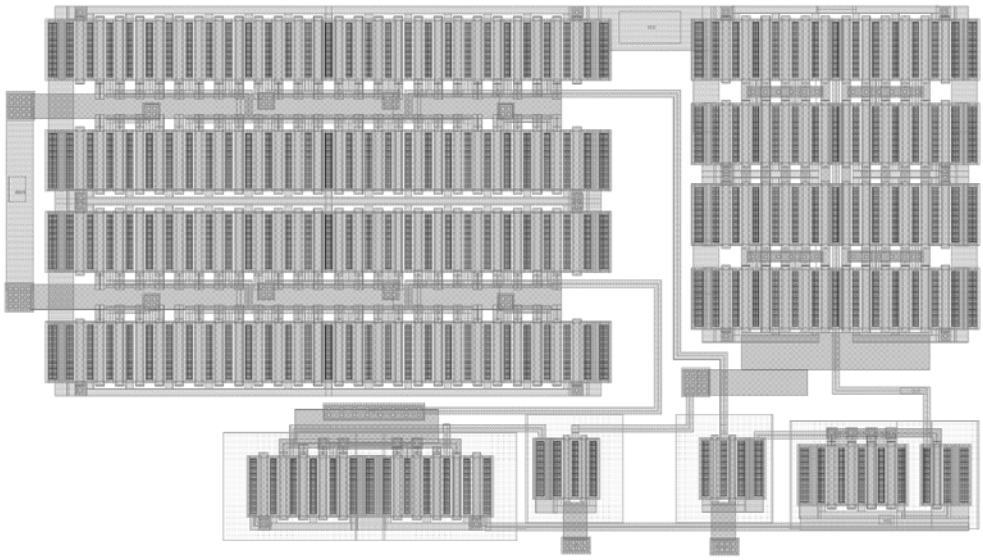


Fig. 6.17. Layout of the Charge Pump for Tapeout 2. Inputs have been relocated to the bottom.

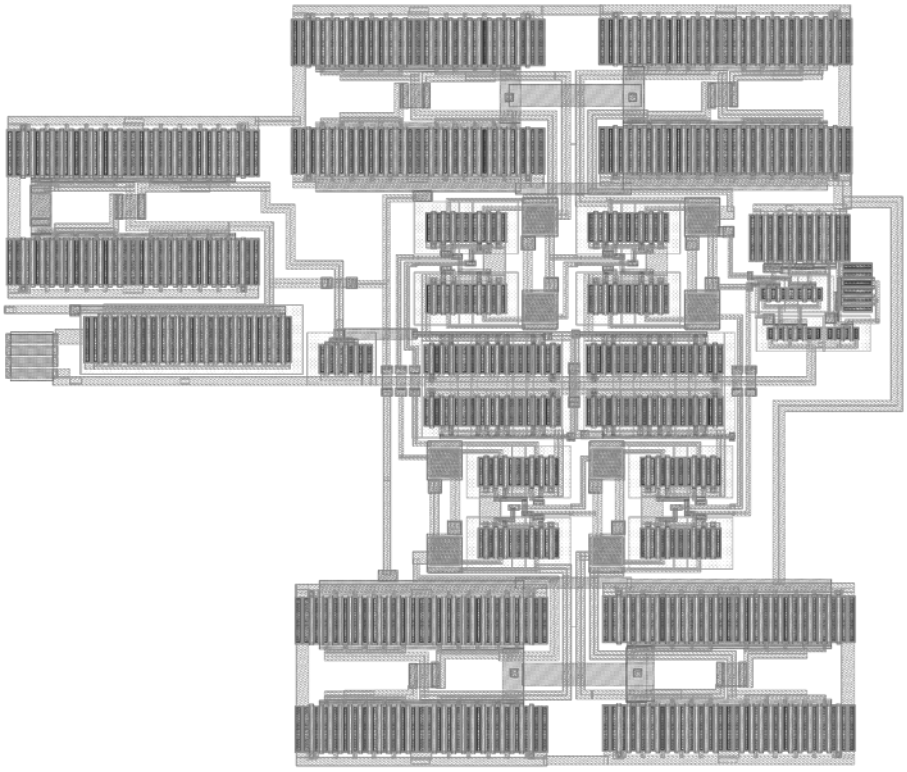


Fig. 6.18. Layout of the VCO for Tapeout 2. The bias generator is on the left, and the output buffer is on the right.

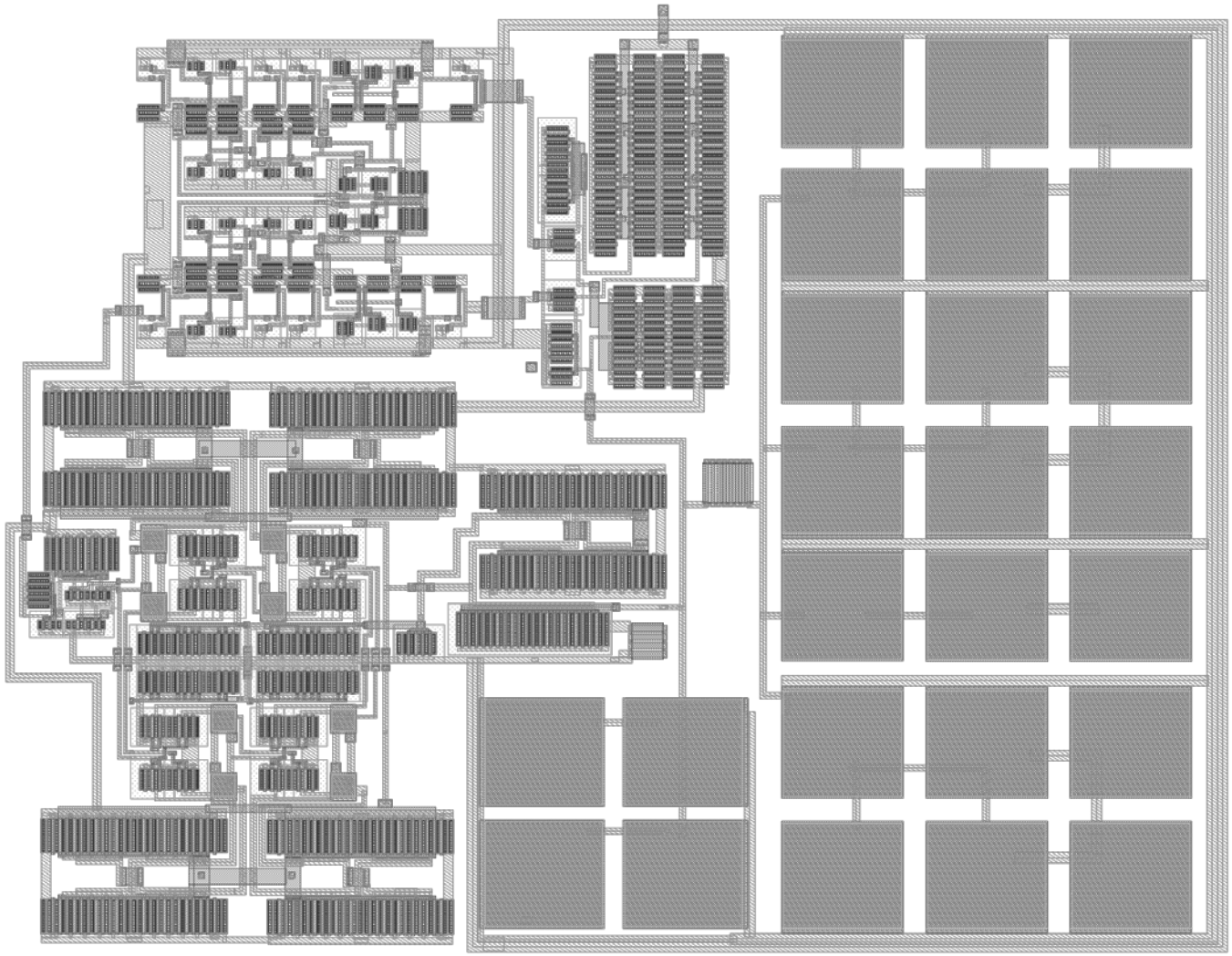


Fig. 6.19. Complete PLL for Tapeout 2. The PFD is on the top left, the Charge Pump is rotated 90° and is in the top middle. The primary loop capacitor is on the right and the VCO is on the lower left.

CHAPTER 7 – CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

In the course of this dissertation, two significant contributions to the state-of-the art were described. First, an improved Shichman-Hodges model for hand design was developed. In this process, the device characteristics of SiC MOSFETs were explored in detail, and several important differences to Si IC processes were highlighted. Effects such as mobility reduction and the body-charge effect will be critical for designers of SiC IC circuits for the foreseeable future. As was shown in the design example, without considering these effects, designers may wrongfully determine that circuits cannot be built which will satisfy basic design targets.

Applying these additional effects during the hand-design stage allows the designer to make intelligent choices about voltages and bias currents to optimize the tradeoff between dynamic range and speed. This is particularly critical since SiC MOSFET's larger gate overlap capacitances and smaller transconductances are currently, and will continue to be, its greatest drawbacks with respect to Si. The great benefits of SiC ICs, such as high operating temperature, radiation robustness, and potential integration with SiC power devices, will not be realized if designers are unwilling to embrace SiC IC processes.

The second contribution to the state of the art was the first phase-locked loop in SiC. At this time, SiC IC processes still feature large wafer-scale device variation, and device parameters are being tuned with each new fabrication run. Overcoming this requires novel topologies which are inherently insensitive to device parameter variation. The current-source load delay cell and charge pump topologies allowed the circuit to function despite the large range of device parameters, and at operating temperature up to 300 ℃.

Although the manufactured circuit did not meet the original design goal of a decade of frequency range, its' behavior did reveal important information about device performance and illuminate areas for further research. Specifically, the PLL's poor locking was likely due to device noise. Steps taken during the improved PLL design should significantly improve the PLL jitter and locking range after Tapeout 2.

This circuit represents a significant step forward in the complexity of mixed-signal circuits that have been successfully demonstrated in SiC IC processes. The approach utilized here, developing topologies that are inherently robust to global device variation, has been shown to be a valuable technique for any IC process which is not yet mature. This approach will also be valuable when devices show global consistency, but are operated over a very wide temperature range, as SiC will be called upon to do as it matures.

7.2 Future Work

In the design of the PLL, several specific steps would be useful. First, the development of a device noise model with appropriate temperature dependence would allow significant improvements in the design of the VCO. Second, additional design revisions on the charge pump could improve the linearity and symmetry of the output characteristics by trying higher risk topologies. Third, a method of tuning the charge pump bias current as a function of VCO frequency would allow adaptive filter bandwidth as proposed by Maneatis [37].

The development of the SiC MOSFET noise model, in particular, will benefit future designers of SiC ICs. The process for measuring device noise is not complicated, but it does require unique measurement equipment. The measurements require a high-precision low-pass filter with a cut-off frequency around 1 Hz for biasing the gate without significant input noise

energy. A low noise current amplifier (such as the SR570 from SRS) is then used to convert the drain current noise into a voltage that traditional device characterization hardware can measure.

The improved Shichman-Hodges model described in Chapter 3 may provide significant benefits in the hand-design of circuits, but until devices are more consistent, it will not predict results accurately. Beyond that, though, it is really only a starting point. A model is only as good as its' fitting algorithm. During the development of this dissertation the algorithm presented in Chapter 3 and the code in Appendix A were developed organically, responding to each new set of device data as it was available. A more complete algorithm might make use of computational methods such as genetic algorithms or particle swarm optimization. The existing fitting algorithm does not take into account the triode region due to the problem of choosing a lower bound for optimizing. Finally, the output resistance reduction term provides a useful function in fitting device behavior, but adds significant complexity to the equation and its usage. It is quite possible that a more graceful construction that produces the same behavior can be derived.

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APPENDIX A – MODIFIED SHICHMAN-HODGES FITTING CODE

The code in this appendix was developed using a variety of Matlab versions, the most recent being version 8.3.0.352 (R2014a). It requires the Curve Fitting Toolbox and the Symbolic Math Toolbox.

```
function [ modSH_fit, gof ] = fitModSH( IdVgs, IdVds, vtFitRange, varargin )
%[ modSH_fit, gof ] = fitModSH( IdVgs, IdVds, vtFitRange, [optional
arguments] )
%   This function takes two input data structures, IdVgs and IdVds, and an
%   array vtFitRange. The structures IdVgs and IdVds must contain two 2-D
%   arays, Id the sweep variable, and 1 vectors, the step variable. The
%   last required argument, VtFitRange, indicates the minimum and maximum
value of
%   Vgs over which to fit a straight line to find Vt.
%
%   The optional arguments include 'quiet' or 'q'. This turns off all
%   plotting for use in other scripts or functions. The other optional
%   argument is 'noWeight', 'linWeight', or 'squareWeight'. This defines
%   how the data is weighted for the final fitting algorithm. 'noWeight' is
%   the default behavior if this argument is not specified.
%
%   Use of the linWeight switch generally provides VERY bad results!
%
%   Specifying '-gamma' turns off the output resistance reduction term, and
%   specifying '-mobility' turns off the mobility reduction term.
%
%   The output is a fit structure and a goodness-of-fit structure.

% check for max Vgs to fit
maxVgs_index = find( strcmpi('maxVgs', varargin)) + 1;
if maxVgs_index > 1
    maxVgs = varargin{maxVgs_index};
else
    maxVgs = Inf;
end

%check for 'quiet' mode
if( any( strcmpi('q',varargin) ) )
    PLOT_ON = false;
elseif( any( strcmpi('quiet',varargin) ) )
    PLOT_ON = false;
else
    PLOT_ON = true;
end
```

```
%check to see if the threshold voltage is predefined
Vt_index = find( strcmpi('Vt', varargin)) + 1;
if Vt_index > 1
    vth = varargin{Vt_index};
    fit_Vt = false;
else
    fit_Vt = true;
end

%Look for Label argument, if it exists, next varargin member is the label
%text
data_label_index = find( strcmpi('label', varargin)) + 1;
if data_label_index >1
    label = strcat( varargin{data_label_index}, ': ');
else
    label = '';
end

%check for weighting mode
if ( any( strcmpi('noWeight',varargin) ) )
    if ( any( strcmpi('linWeight',varargin) ) )
        error('Only one weighting method may be specified!');
    elseif ( any( strcmpi('squareWeight',varargin) ) )
        error('Only one weighting method may be specified!');
    else
        WeightMethod = 0;
    end
elseif ( any( strcmpi('linWeight',varargin) ) )
    if ( any( strcmpi('squareWeight',varargin) ) )
        error('Only one weighting method may be specified!');
    else
        WeightMethod = 1;
    end
else
    WeightMethod=2;
end

%look for effect switches
if ( any( strcmpi('-gamma',varargin) ) )
    noGamma = true;
    disp('Disabling Output Resistance Reduction');
else
    noGamma = false;
end

if ( any( strcmpi('-mobility',varargin) ) )
    noTheta = true;
    disp('Disabling Mobility Reduction');
else
    noTheta = false;
end
```

```
%calculate gm and ro
[gm_Vgs, gm] = diffSmooth( IdVgs.Vgs, IdVgs.Id );
[ro_Vds, ro_inv] = diffSmooth( IdVds.Vds, IdVds.Id(:,:,1) );

%fit Vth using minimum value of Vds over the range specified in vtFitRange
if (fit_Vt)
    vth_fit_options = fitoptions('poly1');
    vth_fit_options.Exclude = excludedata(gm_Vgs(:,1), gm(:,1), 'domain',
vtFitRange); % use only the data inside the fit range
    vth = zeros(1, length(IdVgs.Vds));
    for i = 1:length(IdVgs.Vds)
        vth_fit = fit(gm_Vgs(:,i), gm(:,i), 'poly1',vth_fit_options);
        vth(i) = -vth_fit.p2/vth_fit.p1;
    end
    vth = mean(vth);

    if( PLOT_ON )
        %start setting up main plots
        figure('units','normalized','outerposition',[0 0 1 1]);

        % plot gm data and Vth fit
        subplot(2,2,1);
        hold on
        for i = 1:length(IdVgs.Vds)
            plot(gm_Vgs(:,i), gm(:,i)/max(gm(:,i)),'k.');
        end
        plot(vth,0,'rx','MarkerSize',25);
        hold off
        ylim([ -0.2 1.2 ]);
        title('V_t_h Extraction');
        text(vth+1,0,strcat('V_t_h = ',num2str(vth)));
        ylabel('g_m (normalized)');
        xlabel('V_g_s');
    end
end

%calculate and plot early voltage and lambda fits, and Abulk fits
Va_fit_options = fitoptions('poly1');
Va = zeros(1,length(IdVds.Vgs));

vds_sat = Va;

for k = 1:length(IdVds.Vgs)

    %calculate lambda
    Va_fit_options.Exclude = excludedata( IdVds.Vds(:,k), IdVds.Id(:,k),
'domain', [IdVds.Vgs(k)-vth max(IdVds.Vds(:,k))]); %exclude anything not in
"saturation"
    Va_fit = fit( IdVds.Vds(:,k), IdVds.Id(:,k), 'poly1', Va_fit_options);
    Va(k)=-Va_fit.p2/Va_fit.p1;

    if( PLOT_ON )
        subplot(2,2,[3 4])
        hold on
```

```
        plot(IdVds.Vds(:,k), IdVds.Id(:,k),'k.',[Va(k), IdVds.Vds(:,k)'],[0,
IdVds.Vds(:,k)'*Va_fit.p1+Va_fit.p2], 'r');
        plot(Va(k),0,'rx','MarkerSize',25);
    end

    %Fit ro in triode and saturation to choose Abulk
    Va_fit_options.Exclude = excludedata( ro_Vds(:,k), ro_inv(:,k), 'domain',
[IdVds.Vgs(k)-vth max(ro_Vds(:,k))]); %exclude anything not in "saturation"
    ro_sat_fit = fit( ro_Vds(:,k), ro_inv(:,k), 'poly1', Va_fit_options);



    % calculate Vds,sat from IdVds curves
    Va_fit_options.Exclude = excludedata(  ro_Vds(:,k), ro_inv(:,k),
'domain', [0 (IdVds.Vgs(k)-vth)*0.35 ]); %exclude anything greater than 35%
of "saturation" voltage
    if length( find( Va_fit_options.Exclude < 1 ) ) < 4
        % not enough points to extract a fit for the triode region, skip
        % this step for this value of Vgs
        vds_sat(k) = NaN;
    else
        triode_fit = fit( ro_Vds(:,k), ro_inv(:,k), 'poly1', Va_fit_options);
        vds_sat(k) =  (ro_sat_fit.p2-triode_fit.p2)/(triode_fit.p1-
ro_sat_fit.p1);

        if( PLOT_ON )
            subplot(2,2,2)
            hold on
            plot(ro_Vds(:,k), ro_inv(:,k),'k.',
ro_Vds(:,k),ro_Vds(:,k)'*ro_sat_fit.p1+ro_sat_fit.p2, 'r',
ro_Vds(:,k),ro_Vds(:,k)*triode_fit.p1+triode_fit.p2, 'r')

plot(vds_sat(k),ro_sat_fit.p2+ro_sat_fit.p1*vds_sat(k),'kx','MarkerSize',25);
        end
    end
end
Abulk_array = (IdVds.Vgs-vth)./vds_sat;
%next line strips out any NaNs that might have been picked up it there were
not
%enough points to fit the triode region
Abulk_array = Abulk_array(isfinite(Abulk_array));
Abulk = mean(Abulk_array);
Abulk_std_dev = std(Abulk_array);

lambda_fit = mean(-1./Va);

if (PLOT_ON )
    plottext = {strcat('v_a = [ ', num2str(Va),' ]'),strcat('\lambda \approx
[ ', num2str(lambda_fit),' ]')};
    subplot(2,2,[3 4])
    text(mean(Va),max(IdVds.Id(:,6,1)),plottext);
    title('\lambda extraction');
    xlabel('V_d_s');
    ylabel('I_d_s');
```

```
    hold off;

    subplot(2,2,2)
    plottext = strcat('A_b_u_l_k = ',num2str(Abulk), ' ,\sigma = ',
num2str(Abulk_std_dev));
    text(1,max(ro_inv(:,6,1)),plottext);
    title('A_b_u_l_k extraction');
    ylim([0 1.1*max(max(ro_inv(:,:,1)))]);
    xlabel('V_d_s');
    ylabel('1/r_o');
    hold off;
    set(gcf,'name',strcat(label,'Fits of Vt, Abulk, and Lambda'));
end

% Try fitting theta and k' at Vds,max
if (noTheta)
    fit_func = fittype('k*x^2');
    select_data = find( (IdVgs.Vgs(:,end) - vth) >=0);
    fit_x = IdVgs.Vgs(select_data,end)-vth;
    fit_y = IdVgs.Id(select_data,end,1);
    fit_opts = fitoptions(fit_func);
    fit_opts.StartPoint = [5e-6];
    [first_fit, gof] = fit(fit_x, fit_y, fit_func, fit_opts);
    k_prime = first_fit.k/(1+lambda_fit*IdVgs.Vds(end));
else
    fit_func = fittype('k*x^2/(1+theta*x)');
    select_data = find( (IdVgs.Vgs(:,end) - vth) >=0);
    fit_x = IdVgs.Vgs(select_data,end)-vth;
    fit_y = IdVgs.Id(select_data,end,1);
    fit_opts = fitoptions(fit_func);
    fit_opts.StartPoint = [5e-6, 0.01];
    fit_opts.Lower = [0, 0];
    fit_opts.Upper = [1e-4, 1];
    [first_fit, gof] = fit(fit_x, fit_y, fit_func, fit_opts);
    k_prime = first_fit.k/(1+lambda_fit*IdVgs.Vds(end));
    theta_fit = first_fit.theta;
end

% %build full symbolic equations
% syms('k', 'lambda', 'Ab', 'Vgs', 'Vt', 'Vds', 'Vov','Gamma','theta');
%
% %detect operation region
% on = heaviside(Vgs-Vt);
% mod_triode = heaviside(Vgs-Vt-Ab*Vds);
% mod_sat = heaviside(Ab*Vds-Vgs+Vt)/2;
%
% %mobility reduction
% k_eff = k/(1+theta*(Vgs-Vt));
%
% %output resistance
%
% ro = 1+lambda*(Vds-(Vgs-Vt)/Ab)^Gamma;
%
% %Define the complete Modified Shichman-Hodges Equation
```

```
% Mod_ShichmanHodges = on*k_eff*( mod_sat *ro* (Vgs-Vt)^2 / Ab + mod_triode *
2 *((Vgs-Vt) * Vds - Ab*Vds^2 / 2));

%Create a fitting function. Note that Abulk is integrated into k'

func_string = 'k_prime*(1+lambda*(Vds-(Vgs-Vt)/Abulk)^Gamma)*(Vgs-
Vt)^2/(2*Abulk*(1+theta*(Vgs-Vt)))';
if noGamma & noTheta
    predefined_terms = {'Abulk' 'Vt' 'Gamma' 'theta'};
elseif noGamma
    predefined_terms = {'Abulk' 'Vt' 'Gamma' };
elseif noTheta
    predefined_terms = {'Abulk' 'Vt' 'theta'};
else
    predefined_terms = {'Abulk' 'Vt' };
end

fit_func = fittype(func_string, 'independent', {'Vgs' 'Vds'}, 'problem',
predefined_terms);

fit_opts = fitoptions(fit_func);
vgs_array = repmat(IdVds.Vgs,  size(IdVds.Vds)./size(IdVds.Vgs));
vds_array = repmat(IdVgs.Vds, size(IdVgs.Vgs)./size(IdVgs.Vds));

% reshape the fitting data from output characteristics
[fit_x1, fit_y1, fit_z1] = prepareSurfaceData(vgs_array, IdVds.Vds,
IdVds.Id);

% reshape the fitting data from input characteristics
[fit_x2, fit_y2, fit_z2] = prepareSurfaceData(IdVgs.Vgs, vds_array,
IdVgs.Id);

%concatenate fitting data from input and output curves
fit_x = [fit_x1; fit_x2];
fit_y = [fit_y1; fit_y2];
fit_z = [fit_z1; fit_z2];

fit_opts.Exclude = ( fit_y < (fit_x-vth)/Abulk ) | ( (fit_x-vth) < 0 ) |
(fit_x > maxVgs);

% two options to weight fits to equalize % error
if( WeightMethod == 1 )
    fit_opts.Weights = not(fit_opts.Exclude')./(fit_z.^2);
elseif ( WeightMethod == 2 )
    fit_opts.Weights = not(fit_opts.Exclude')./(fit_z);
    fit_opts.Weights( find( fit_z <= 0) ) =0;
end

%pick starting point Gamma as 1
% Order of startpoint data wrt to coefficients is determined by results of
% coeffnames(fit_func). This is generally in alphabetical order.
% Order: Gamma, k_prime, lambda, theta)
```

```
if noGamma & noTheta
    defined_values = {Abulk vth 1 0};

    fit_opts.StartPoint = [ k_prime*Abulk, lambda_fit/Abulk ];
    fit_opts.Lower = [0, 0];
    fit_opts.Upper = [1, 1];
elseif noGamma
    defined_values = {Abulk vth 1};

    fit_opts.StartPoint = [ k_prime*Abulk, lambda_fit/Abulk, 0];
    fit_opts.Lower = [0, 0, 0];
    fit_opts.Upper = [1, 1, 1];

    %fit_opts.Lower(3) = 0;
    %fit_opts.Upper(3) = 1;

elseif noTheta
    defined_values = {Abulk vth 0};

    fit_opts.StartPoint = [1, k_prime*Abulk, lambda_fit/Abulk ];
    fit_opts.Lower = [0, 0, 0];
    fit_opts.Upper = [1, 1, 1];

else
    defined_values = {Abulk vth};

    fit_opts.StartPoint = [1, k_prime*Abulk, lambda_fit/Abulk, 0];
    fit_opts.Lower = [0, 0, 0, 0];
    fit_opts.Upper = [1, 1, 1, 1];
end

[modSH_fit, gof] = fit([fit_x, fit_y], fit_z, fit_func, fit_opts, 'problem',
defined_values);

if( PLOT_ON )
    plotModSH(IdVgs, IdVds, modSH_fit);

    set(gcf,'name',strcat(label,'Fits to Input and Output
Characterisitics'));
end

end



function [x_out, dydx_out] = diffSmooth(x_in, y_in)
%This function smooths the input then performs an approximate derivative.
%It returns the derivative and the x value corresponding to that
%derivative.
%
% It should only be used with 1- and 2-D arrays
```

```
data_size = size(y_in);

dx = diff(x_in);
y_smooth = zeros(data_size(1), data_size(2));
for k = 1 : data_size(2);
    y_smooth(:,k) = smooth(y_in(:,k));
end
dy = diff(y_smooth);
dydx_out = dy./dx;

x_out = x_in(1:end-1,:) +dx/2;

return


function plotModSH( IdVgs, IdVds, modSH_fit )
% plotModSH( IdVgs, IdVds, modSH_fit] )
%   This function plots the results of the fitModSH function.

%build full symbolic equations
syms('k', 'lambda', 'Ab', 'Vgs', 'Vt', 'Vds', 'Vov','Gamma','theta');

%detect operation region
on = heaviside(Vgs-Vt);
mod_triode = heaviside(Vgs-Vt-Ab*Vds);
mod_sat = heaviside(Ab*Vds-Vgs+Vt);

%mobility reduction
k_eff = k/(1+theta*(Vgs-Vt));

%output resistance
ro = 1+lambda*(Vds-(Vgs-Vt)/Ab)^Gamma;

%Define the complete Modified Shichman-Hodges Equation
Mod_ShichmanHodges = on*k_eff*( mod_sat *ro *(Vgs-Vt)^2 / (2* Ab) +
mod_triode *((Vgs-Vt) * Vds - Ab*Vds^2 / 2));

figure('units','normalized','outerposition',[0 0 1 1]);

inputRange = [min(min(IdVgs.Vgs)), max(max(IdVgs.Vgs))];
outputRange = [min(min(IdVds.Vds)), max(max(IdVds.Vds))];



for i = 1:length(IdVds.Vgs)
    subplot(2,1,1)
    hold on

    h = ezplot(subs(Mod_ShichmanHodges,{k lambda Gamma Vgs Vt Ab theta},
{modSH_fit.k_prime modSH_fit.lambda modSH_fit.Gamma IdVds.Vgs(i) modSH_fit.Vt
modSH_fit.Abulk modSH_fit.theta}), outputRange);
    set(h,'Color', 'red')
    plot(IdVds.Vds(:,i),IdVds.Id(:,i),'ks', 'MarkerSize', 2);
```

```
    top_y_lim = ylim();
    ylim([0 1].*top_y_lim);
    xlim([0 15]);
    text(1.02*outputRange(2), IdVds.Id(end,i,1), strcat('Vgs = ',
num2str(IdVds.Vgs(i))));


end
for i = 1:length(IdVgs.Vds)
    subplot(2, 1, 2)
    hold on
    h = ezplot(subs(Mod_ShichmanHodges,{k lambda Gamma Vds Vt Ab theta},
{modSH_fit.k_prime modSH_fit.lambda modSH_fit.Gamma IdVgs.Vds(i) modSH_fit.Vt
modSH_fit.Abulk modSH_fit.theta}), inputRange);
    set(h,'Color', 'red')
    plot(IdVgs.Vgs(:,i),IdVgs.Id(:,i),'ks', 'MarkerSize', 2);

    bottom_y_lim = ylim();
    ylim([0 1].*bottom_y_lim);
    xlim([0 15]);
    text(1.02*inputRange(2), IdVgs.Id(end,i), strcat('Vds = ',
num2str(IdVgs.Vds(i))));
end

subplot(2,1,1)
title('Modified Shichman-Hodges Fit to Output Characteristics')
xlabel('V_d_s');
ylabel('I_d_s');
hold off;

subplot(2,1,2)
title('Modified Shichman-Hodges Fit to Input Characteristics')
xlabel('V_g_s');
ylabel('I_d_s');
hold off;

set(gcf,'name','Fits to Input and Output Characterisitics');

end
```