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Fabrication of Single Nanowire Device using Electron Beam Lithography

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By

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Abstract

One dimensional nanostructure materials such as nanowires have drawn many interests among the scientific community for a wide range of applications such as field-effect transistors [1], [2], inverters[3], light-emitting diode [1], lasers [4], nanosensors [5], [6], and photodetectors [7]… Comparing with the characterization of nanowire arrays, characterizing a single nanowire will definitely provide a better understanding on new nanowire properties due to simplified behaviors of devices. Although promising theories could be drawn from those results, fabrication of test structure for single nanowire measurements cannot be easily processed using standard microfabrication techniques. Therefore, electron beam lithography integrated with photolithography technique has been used to manipulate the connection; which provides I-V characteristics, of single horizontal nanowire with a specific device. Single Si nanowire characterization could be extended to various materials for further studies.

In addition to single horizontal nanowire device, single vertical nanowire structure has been fabricated. Electron beam lithography technique is mainly used to pattern well-defined nanostructures where single ZnO nanowire is grown. Optical measurement, photoluminescence, is conducted to verify ZnO nanowires.

This thesis also emphasizes on fabrication process to pattern various structures such as lines, rings, and circles with different sizes from 1um to sub 100nm… They could be potential candidate to create nanodisk antenna (rings), fishnet structure (lines), and base to grown single nanowire (circle).

Acknowledgments

I would like to express my deep gratitude and my sincere thanks to my advisor, Dr. Shui-Qing (Fisher) Yu, who always supports and guides me patiently during my research time. He gave me good opportunity to study and work in fabrication area where I could be the best of me. I would like to thank Dr. Vasuran Varadan and Dr. Hammed Naseem to be part of my master committee members.

I am also grateful to my colleague, Liang Huang, for providing me useful suggestions and solutions for fabrication process. He is also a good friend and supporter. I thank Dr. Mourad Benamara from Nano Institute for teaching me to take quality SEM pictures.

Special thanks to Seyed Ghetmiri for the help in measuring photoluminescence, Matthew Young for the help in growing Si nanowires and depositing insulator layer SiO_2, Yusuke Hirono for the help in studying surface roughness using AFM, and Yiyin Zhou for the help in cleaning mask.

I would like to thank my family who always support and colleagues and friends who make my time living in Fayetteville enjoyable. Special thanks to Dongsheng Fang for all the conversations he inspired me.

Dedication

Students of University of Arkansas who have strong interest in fabrication process of single nanowire device could use this thesis as a reference.

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CHAPTER 1: INTRODUCTION

1.1 History of nanotechnology

Although Michael Faraday discovered gold nano-particles in 1857, the first concept of nanoscience and nanotechnology was presented a hundred years later by Richard Feynman, a Nobel laureate. Feynman claimed that "There's plenty of room at bottom" [8] where he discussed the possibility of manipulating materials at atoms scale. Since then, human beings have rapidly developed and operated tools that have the abilities to detect, scan, and fabricate materials down to the nanoscale level. As a result, a new form of carbon C60 or fullerenes, carbon nanotubes (CNT), and quantum dots were discovered in 1985, 1991, and 1993 respectively [9]. In addition, many studies on synthesis materials, fabrication technique, and materials properties have been widely conducted and reached considerable achievements. This opened the era of nanotechnology with promising applications in various fields including bio-medical, electronics, renewable energy, and military defense.

1.2 From nanostructures to one-dimensional nanostructures

Nanostructures are not a new concept. The prefix "Nano" which is derived from Greek means dwarf [10]. In fact, the concept of "nano" is not limited to only its original definition, but transforms in parallel with the extraordinary development of human knowledge. Nanostructures, a particular term with prefix nano, associates with a series of structures having at least one of its dimensions less than 100nm. One of significant difference that differentiates from one type of nanostructures to the others is its physical structures. The first classification suggested by Gleiter in 1995 and later modified by Skorokhod in 2000 divided nanostructures into zero-dimensional

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(0D), one-dimensional (1D), two-dimensional (2D), and three-dimensional (3D) nanostructures [11].

One-dimensional nanostructures such as wires, rods, and tubes can be defined as a group of materials having one dimension surface constrained from 0.1nm to 100nm. Since the late 1980s, 1D nanostructures have attracted much attention because they show enormous potential to be great study models for nano-scopic physics (e.g. electrical / thermal transport, mechanical properties) and better candidates for fabrication at the nanoscale level (e.g. interconnects and functional units in fabricating electronic, optoelectronic and electromechanical devices) [12]. At the moment, 1D nanostructures can be fabricated by using nanolithography techniques such as Electron Beam Lithography (EBL), Focused Ion Beam (FIB), and X-Ray or extreme UV lithography for academic research purposes [12].

Why Single Nanowire?

Nanowires exhibit significantly different thermal, electrical, mechanical and optical properties from their bulk materials thanks to their unique density of electronic states [13]. Thus, mastering the properties of nanowires will lead to promising applications in nanowire field effect transistors, optoelectronics devices, and sensors. Fabricating and characterizing single nanowires is necessary in order to lead to a better understanding of new nanowire material properties because the behaviors of devices are simpler to predict and observe.

1.3 Thesis Outline

The work presented in this thesis will focus on fabricating single horizontal nanowire device using the Electron Beam Lithography (EBL) technique followed by electrical characterizations. Fabrication of single vertical nanowire structures is also another important part

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of this thesis. EBL is used to patterns nanostructures where single vertical nanowire is grown. Before that, one step crucial to preparation is the fabrication of well-defined structures such as rings, circles, and lines followed by metallization and lift off to evaluate the final recipes.

The thesis is mainly composed of six chapters. The first chapter provides the introduction to the thesis. Chapter two gives a theoretical overview on electron beam lithography technique based on the JEOL 5500ZD system and metal semiconductor contact. Chapter three covers step by step of processing works to pattern nanostructures such as holes, rings, and lines. While fabrication and electrical characterization of single horizontal nanowire device will be summarized in chapter 4, single vertical nanowire structures' fabrication and optical measurements will be discussed in chapter 5. In the end is chapter 6 which concludes the thesis.

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CHAPTER 2: THEORY OF ELECTRON BEAM LITHOGRAPHY AND METAL SEMICONDUCTOR CONTACT

2.1 Electron beam lithography

2.1.1 Introduction

Electron beam lithography (EBL) is a direct writing lithographic technique that uses an electron beam to write patterns. Compared with conventional photolithography, there are two advantages in a semiconductor fabrication field. The first trait is the capability to generate pattern without applying photo mask. This saves the fabrication cost of photo mask and offers the freedom to write patterns without relying on a hard layout. The second trait is higher patterning resolution. EBL provides nano-scaled patterning which cannot be realized by conventional photolithography because of diffraction limit.

The following section will mainly focus on concept and writing principle of EBL based on JEOL 5500ZD system, as shown in figure 2.1.

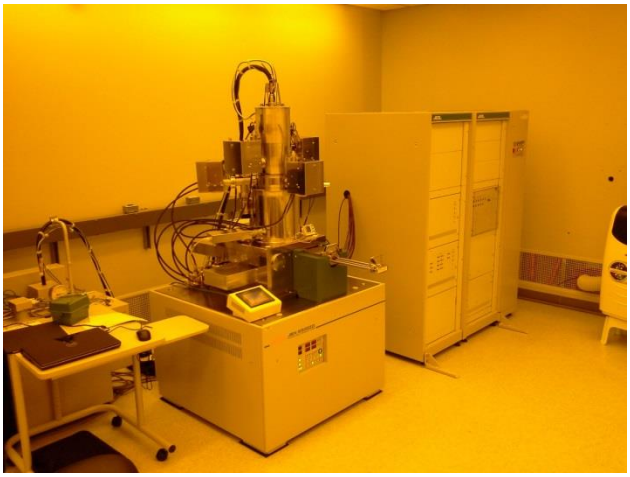

Figure 2.1 EBL JEOL 5500ZD system (Thach Pham, June 2012, HiDEC cleanroom, University of Arkansas)

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2.1.2 Principle of EBL

(a) Formation of beam spot

The source of the electron beam comes from thermal field emission type cathode, i.e. ZrO/W is the emitter [14]. The generated electron beam passes through an electronic optical lenses system that is composed of four main stages where the beam is focused and calibrated before reaching a work piece. The user is able to fully control the beam spot size and its movement.

(b) Patterns generation

A sample coated with e-beam resist is placed on the work piece of the EBL system. The resist can be either positive or negative. The patterns are formed by integrating deflected electron beam with movement of the stage which controls the structure of patterns.

(c) Resist sensitivity

The resist sensitivity or exposure dose (C/cm^2) is defined as the amount of required energy to fully penetrate an e-beam resist layer, which is determined by the resist sensitivity and can be expressed as:

$$Q = \frac{I * T}{S}$$

Where I (A) is the generated beam current from the emitter, S (cm^2) is the pattern writing area, and T (s) is the pattern writing time [14].

Equation 2.1 can be applied to determine resist sensitivity in either case of positive or negative e-beam resist.

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(d) Scanning method

The electron beam lithography system applies vector scanning method which allows the beam to scan only on a writing area defined by the user.

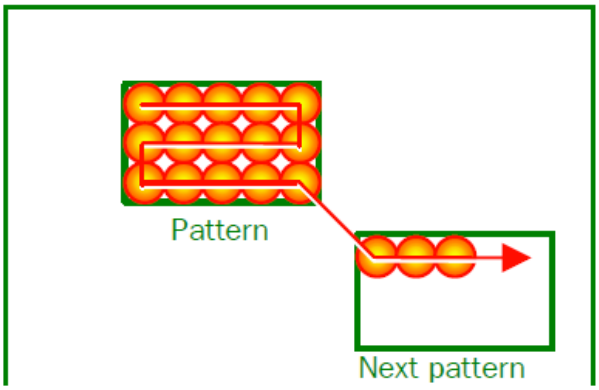

Figure 2.2 Vector scanning method [14]

As mentioned above, there are two key movements that control the carving of patterns on e-beam sensitive resist. In the first step where the stage is immobile during the scanning process, the beam is deflected to scan only in a specific region, called as “field”, as shown in figure 2.2. The field can be divided up to 200,000x200,000 points. The distance between two consecutive points is called as “scanning step”. When the beam finishes scanning the first field, the stage moves by a distance equal to the field size in order to continue writing on the second field, as shown in figure 2.3. The process of scanning one field after another one and moving between consecutive fields until all the patterns are successfully transferred on the entire chip is defined as the step and repeat method. [14]

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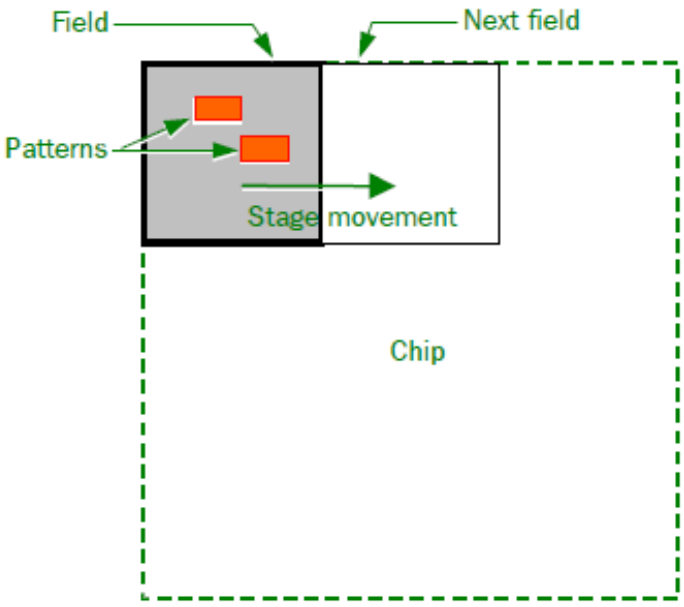

Figure 2.3 Step and repeat method [14]

By modifying different hardware configuration such as objective lens and acceleration voltage, field size, scan step, writing quality, as well as writing speed could be optimized.

Table 2.1 Electron-optical system (EOS) and system configuration

EOS mode	ACC (kV)	Obj. Lens	Max. Field (um)	Min. Scan Step (nm)	Writing result	Writing Speed
1	25	4	2000	10	Rough	High
2	50	4	1000	5	↓	↑
3	25	5	200	1	↓	↑
4	50	5	100	0.5	High	Low

(e) Global marks and chip marks

Global marks and chip marks are special patterns functioning as alignment signals which provide directional information of the substrate to the user, as shown in figure 2.4. The shape of the marks could vary according to a user's purpose. The common shape for both global marks and chip marks that EBL JEOL 5500ZD system is able to detect is a cross.

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In general, at least two global marks and three chip marks are required. Two global marks provide expansion/contraction parameters, rotation and shift of the substrate based on which the system will make corrections. In the case of chip marks, the distortion parameter within the writing field is sent to the system to perform calibration. [14]

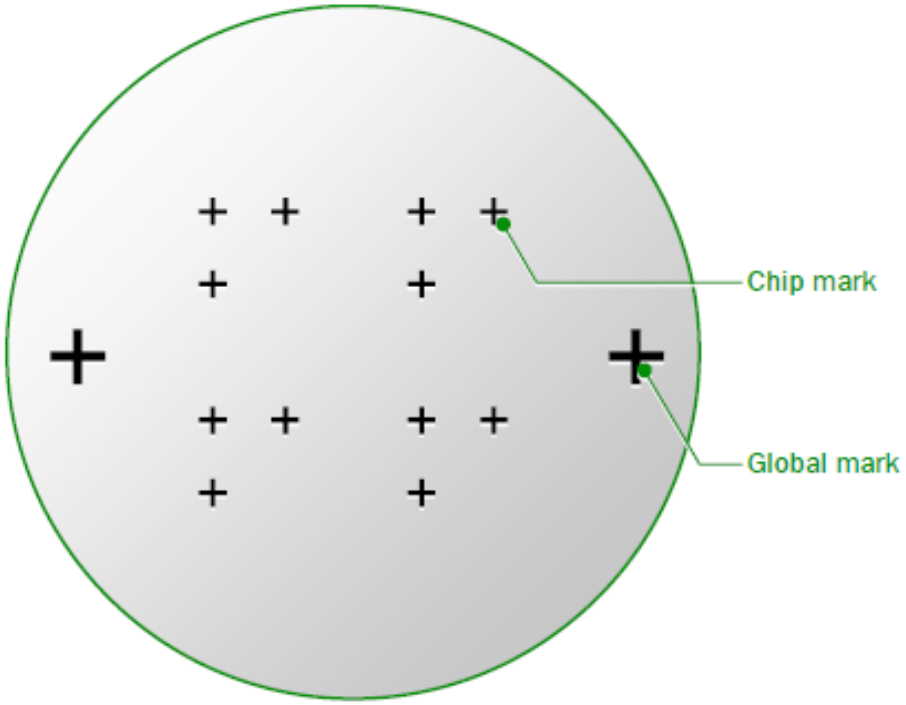

Figure 2.4 Global marks (PQ) and chip marks [14]

2.1.3 System overview

The EBL JEOL 5500ZD system configuration is composed mainly of five components: the main console, control rack, high voltage tank, water chiller, and operation console.

(a) Main console

The main console consists of the electron-optical system (EOS), exposure chamber, manual loader, and base frame, as shown in figure 2.5.

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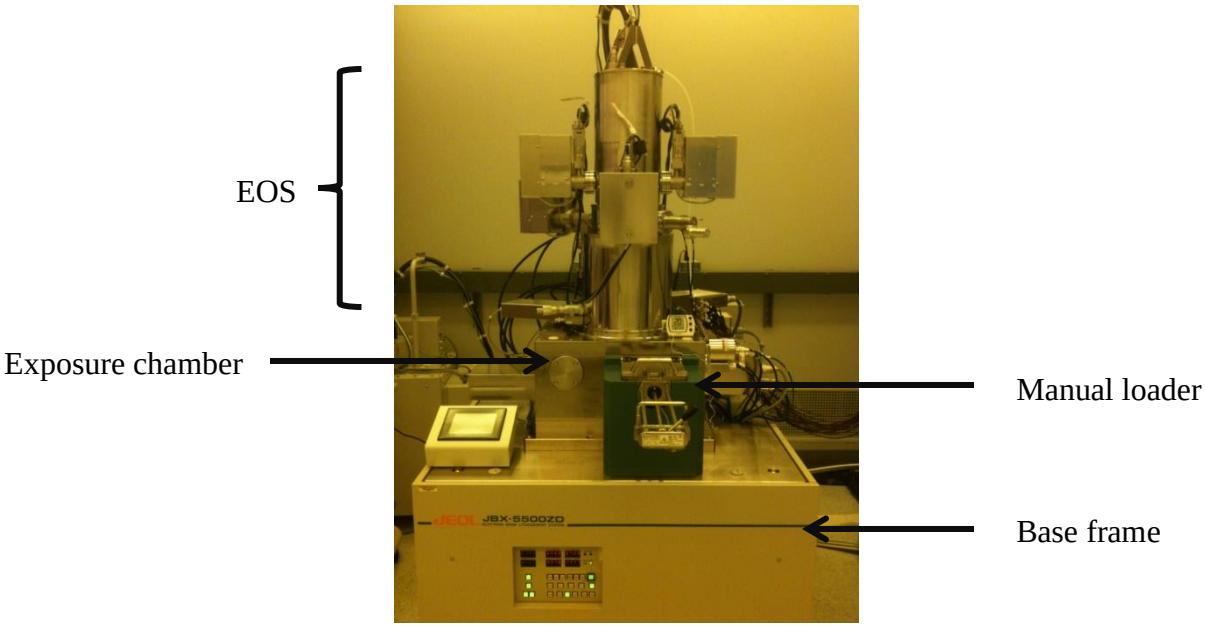

Figure 2.5 EBL main console (Thach Pham, June 2012, HiDEC cleanroom, University of Arkansas)

(b) Operation console

The operation console is the interface between user and equipment. A user can perform 3 main tasks which are pattern design, calibration, and exposure

(c) Control rack

The control rack includes rack A, rack B, and PS box. Rack A controls the lenses and deflectors of EOS, rack B controls the work stage, input and output signals, and PS box controls power.

(d) High voltage tank

The high voltage tank generates the accelerating voltage.

(e) Water chiller

The water chiller keeps the temperature of all equipment stable.

2.1.4 EOS

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Figure 2.6 shows the composition of EOS inside EBL system. Two main parts, the electron source column and a column, form the electron optical system [14].

- The electron source column consists of two parts:
    - Electron source: ZrO/W emitter
    - Alignment coils include two stages deflection coil to correct the axis of incoming electron beam from the electron source. In figure, the tilt correction deflects the beam in such way that the beam is focus at a point located on the aperture (crossover point) while the horizontal tilt deflects the beam to be focus at a point located on the center of 2^{nd} lens.
- The column consists of:
    - Intermediate lenses (2^{nd} and 3^{rd} lenses) reduce the dispersion of beam after passing the crossover point. They also serve as tuning tool for beam current or beam size.
    - Objective lenses (4^{th} and 5^{th} lenses) are two main lenses determining the working condition of e-beam writing such as writing quality, writing time, field size, …
    - A stigmator coil is used as correction tool to tweak the beam spot shape from an ellipse to a perfect circle.
    - Beam blanker can either block the beam by deflecting it out of the objective aperture or let the beam pass through.
    - Deflectors (4^{th} and 5^{th} deflectors) represent the scanning range of the beam. They are prime factors along with acceleration voltage to configure the working condition of EBL machine.

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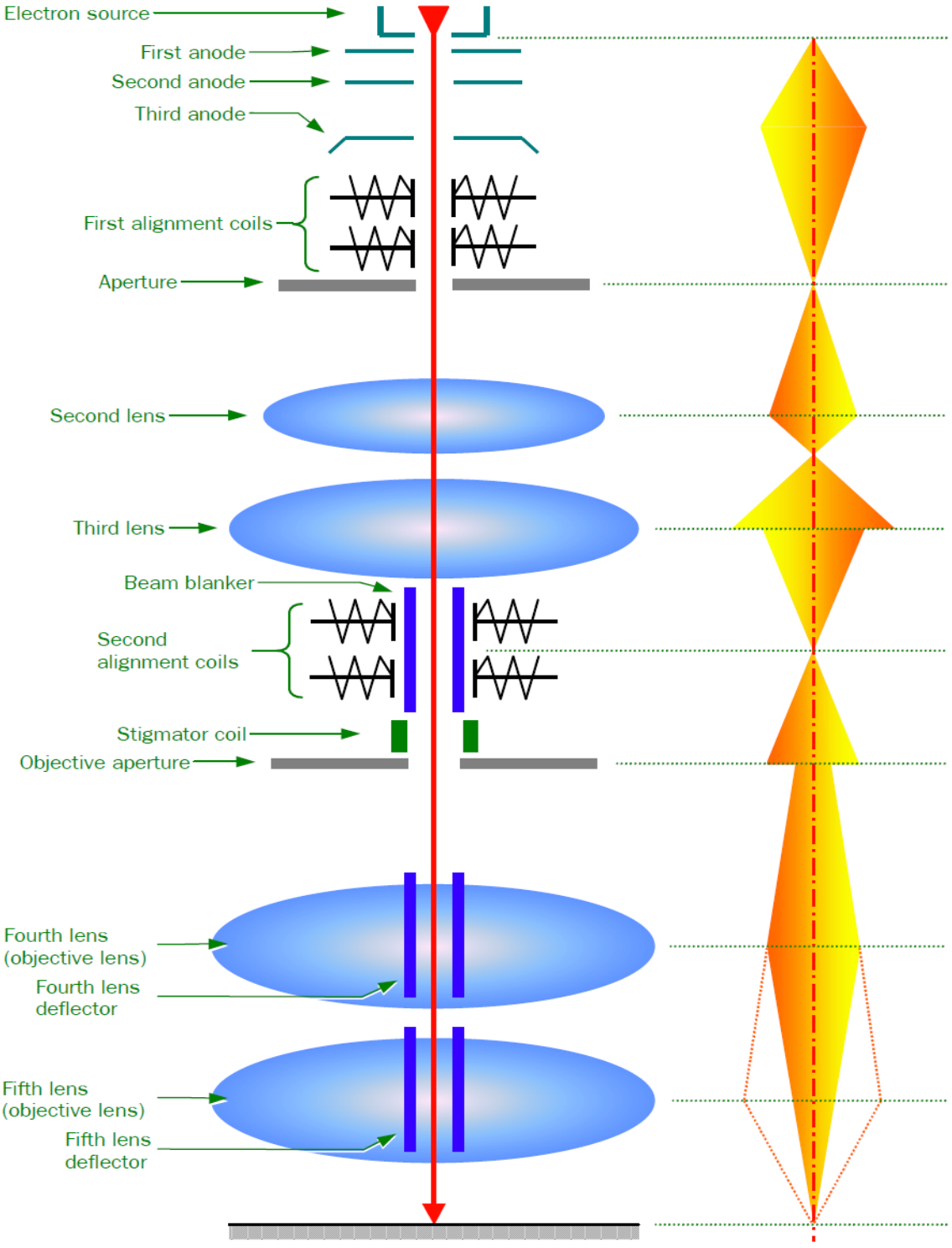

Figure 2.6 Electrons optics system [14]

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2.1.5 Stage driving system

The stage driving system applies the laser beam control (LBC) method to accurately control the position of e-beam as shown in figure 2.7.

The stage moves from one field to another using the step and repeat method. However, there will be an error when the stage moves. The stage is assumed to be located at an arbitrary position called the current location which differs from the specified location defined by the user. The discrepancy between these two locations is the error which can be detected by laser interferometer with a resolution of 0.62nm. The error is sent to a system of signal processor as feedback which helps the system to calibrate the beam. [14]

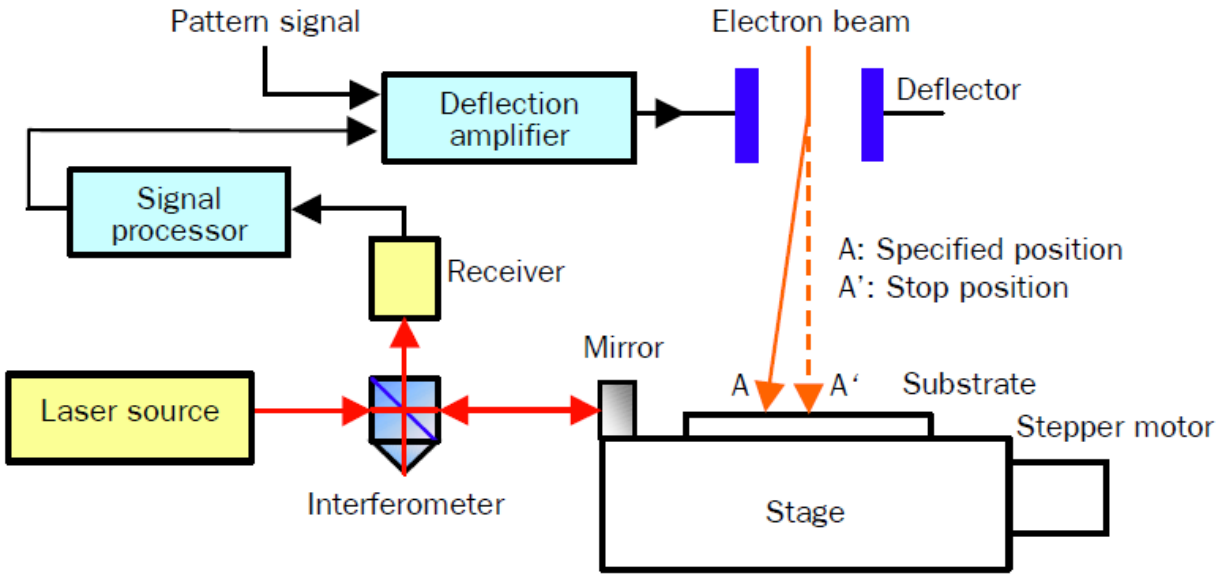

Figure 2.7 Moving stage system [14]

2.1.6 User interface

(a) Main interface: This is the main interface where user performs most of the crucial adjustments such as ammeter, focus, contrast, EOS mode, beam control, and stage movement. In addition, three others main graphic user

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interfaces (GUIs) are integrated with the man interface: pattern designer, calibration, and exposure, as shown in figure 2.8.

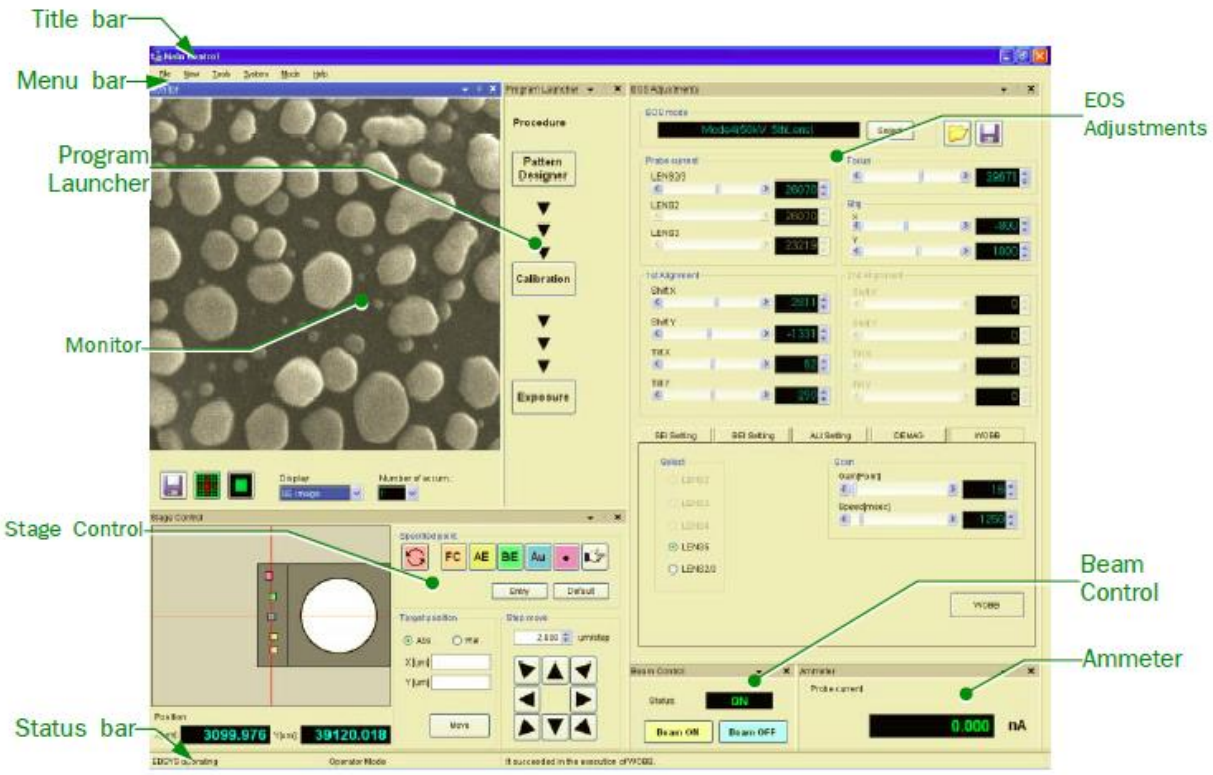

Figure 2.8 Main interface [14]

(b) Pattern designer interface: This is the only GUI in the EBL system allowing user to create pattern file and convert designed pattern to *.v30 file, as shown in figure 2.9. The pattern designer limits the diversity of patterns into certain basic shapes such as lines, circles, rectangles, and rings. The need for manually entered coordinates of each object makes this GUI less competitive with third party design program such as Auto CAD.

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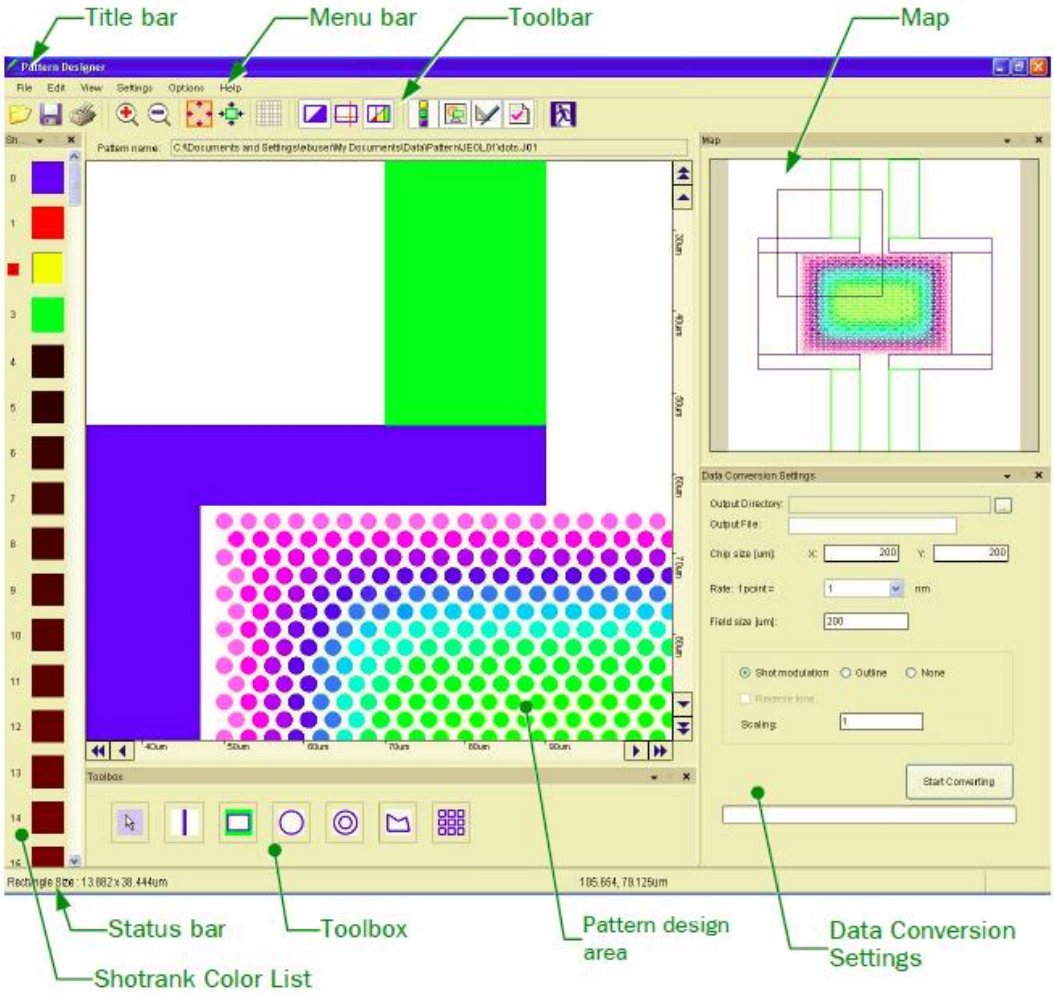

Figure 2.9 Pattern designer interfaces [14]

(c) Calibration interface: In contrast with the pattern designer interface, the calibration GUI is an irreplaceable tool of EBL system as shown in figure 2.10. This offers not only elemental calibration functions such as beam deflection amplitude and deflection distortion but also magnificent alignment capability between two layers with a high level of accuracy.

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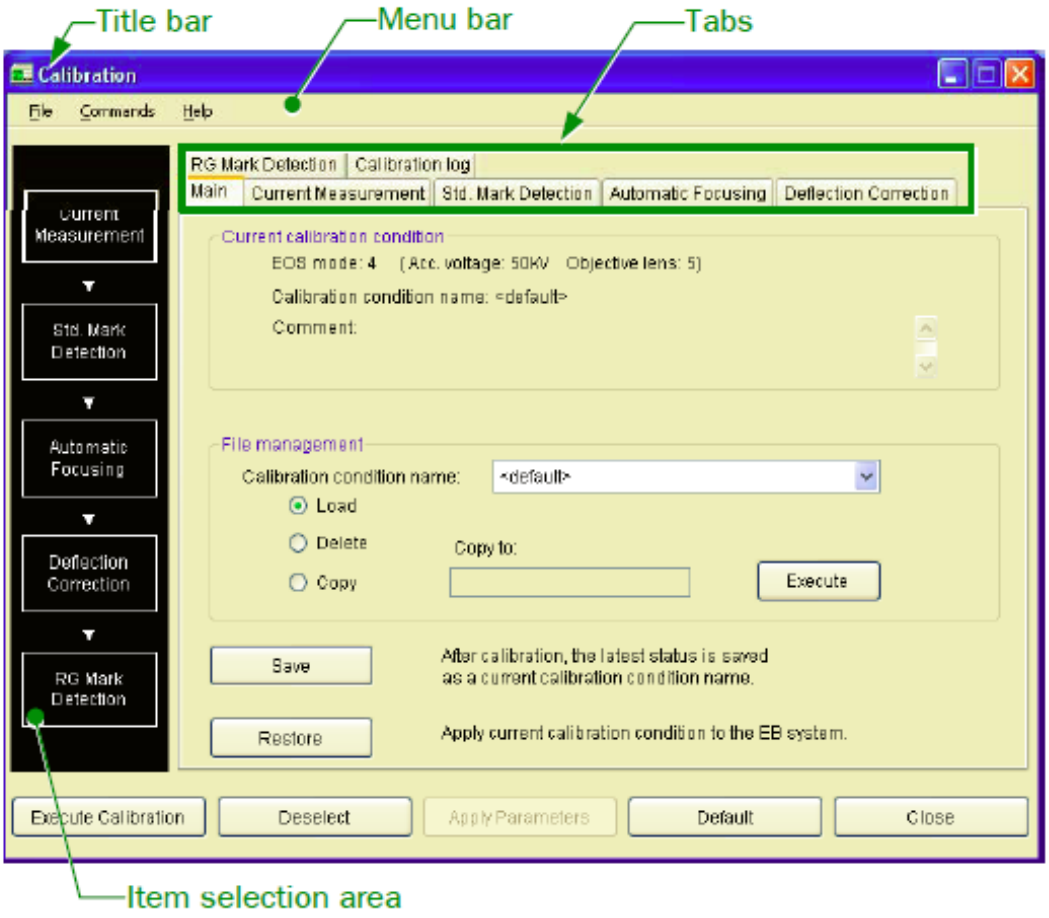

Figure 2.10 Calibration interfaces [14]

(d) Exposure interface: The exposure interface function is to create a layout map where the user defines writing areas to match with the sample position as shown in figure 2.11. In addition, this tool includes exposure dose with shot rank table (discuss in chapter 3).

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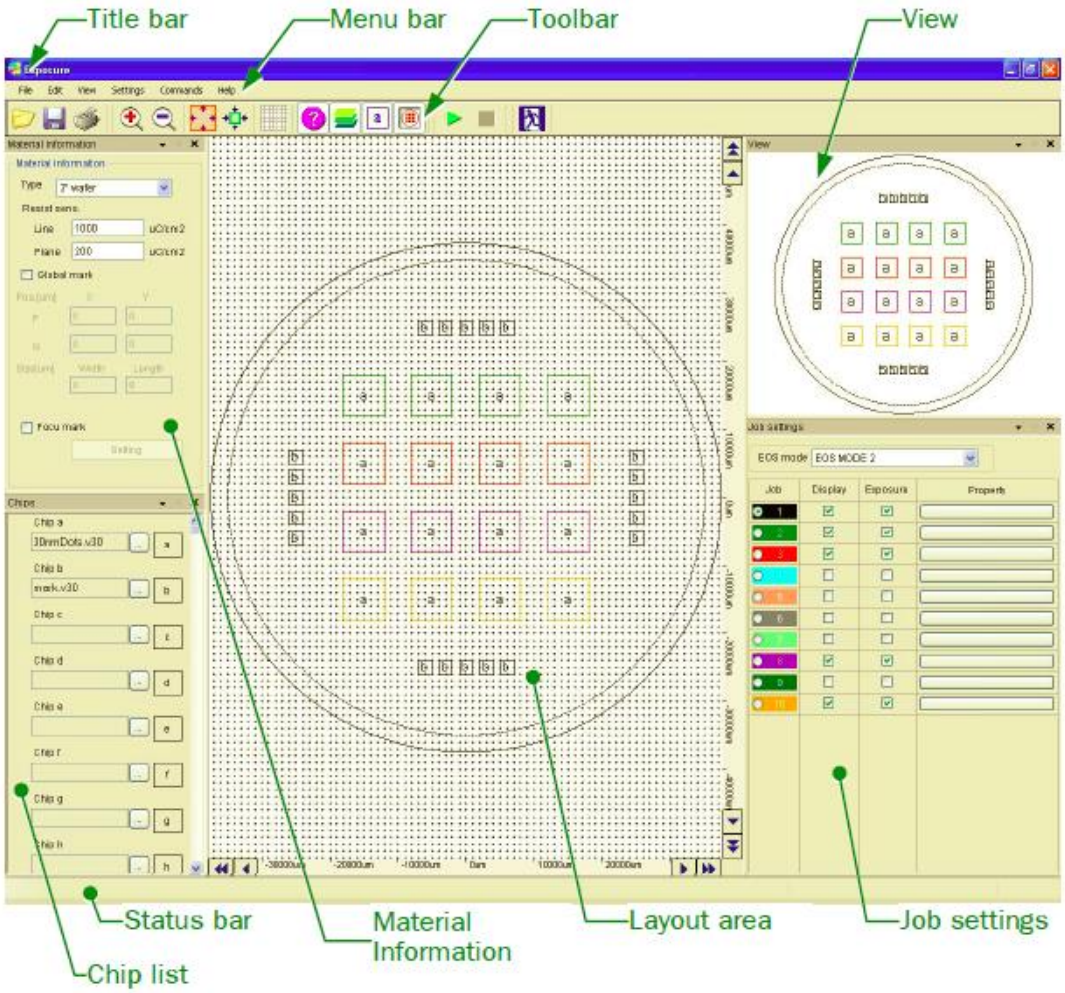

Figure 2.11 Exposure interfaces [14]

2.2 Metal semiconductor contacts

The two-terminal current voltage measurement is one of basic electrical characterization to determine the resistance of a silicon based nanowire. The most critical element in such measurements is having the control over the contact generated when a metal is brought into contact with a semiconductor. In practical, there are two types of metal semiconductor contact: Shottky contact and Ohmic contact.

In the following section, brief theory of two metal semiconductor contacts will be introduced.

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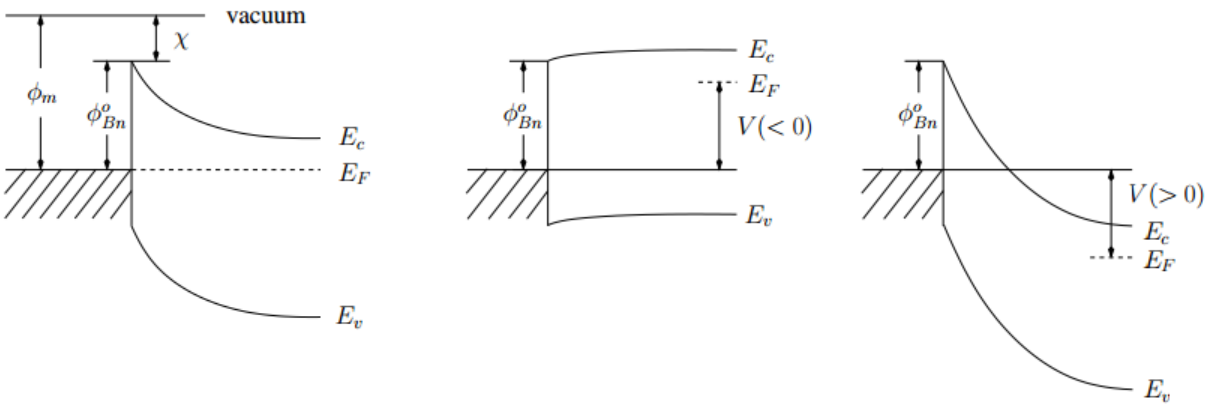
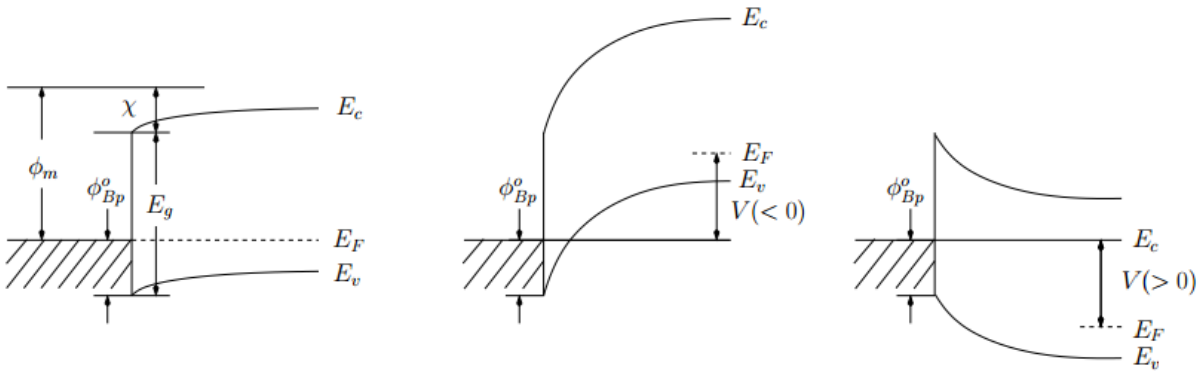
2.2.1 Schottky contact

In this subsection, energy band diagrams become the main tool to analyze and explain phenomena that occurs inside the junction.



Equilibrium Forward bias Reverse bias

Figure 2.12 Band diagram of ideal metal n-type semiconductor contact under equilibrium, forward bias, and reverse bias condition. [15]



Equilibrium Reverse bias Forward bias

Figure 2.13 Band diagram of ideal metal p-type semiconductor contact under equilibrium, forward bias, and reverse bias condition. [15]

Metals and semiconductors have their own Fermi level with distinctive positions with respect to vacuum level. The vacuum level is defined as a level where all existing electrons are free and isolated. All electrons in metal have negative energy compared with those hanging in

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vacuum level. Hence, the required energy to free an average electron located in Fermi level of metal is named as work function. The work function of each metal is different. [15]

The same concept of work function is applied in the case of semiconductors. However, there are no electrons in the Fermi level of a semiconductor and Fermi level depends on doping type. Thus, the concept of work function is replaced by electron affinity. The electron affinity is defined as an amount of energy to liberate an electron located at the bottom of conduction which is irrelevant with doping type. The electron affinity deviates from materials to materials. [15]

When the electric contact is made between metal and semiconductor, a potential barrier will form and prevent the majority of charge carriers (electrons and holes) to cross from one side to another and vice versa assuming that there is no applied voltage. At that stage, the Fermi levels of metal and semiconductor must be realigned under thermal equilibrium condition. The potential barrier height is equal to the initial offset between Fermi levels of two materials in contact. [15]

In the case of an n-type semiconductor, the barrier height can be expressed as:

$$\phi_{Bn} = \phi_m - \chi$$

In the case of a p-type semiconductor, the barrier height can be expressed as:

$$\phi_{Bp} = E_g - (\phi_m - \chi)$$

Where E_g is the band gap of the semiconductor.

There are two effects when voltage is applied to metal semiconductor layer: reverse bias conditions and forward bias condition. They change upon doping type of semiconductor.

When a positive voltage is applied to an n-type semiconductor, the energy level of Schottky barrier is increased, as shown in figure 2.12. This increment further blocks the electron current from metal to semiconductor although there is still a minority of electrons that can

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overcome the energy barrier and define reverse bias current. This reverse bias current is independent with applied voltage. We call this phenomenon the reverse bias condition. In contrast, when a negative voltage is applied to an n-type semiconductor, the energy level of Schottky barrier is decreased. The reduction in potential barrier allows more electrons to flow from semiconductor to metal. The dominant electron flow forms the forward bias current which increases exponentially with applied voltage. This phenomenon is defined as forward bias condition. [15]

In case of a p-type semiconductor, the Schottky barrier is under reverse bias condition when negative voltage is applied and under forward bias condition when positive voltage is applied as shown in figure 2.13. [15]

2.2.2 Ohmic contact

A significant trait to recognize Ohmic contact is its linear I-V curve. The first method to achieve Ohmic contact is to choose metal type which has the work function to be equal or equivalent with the one form semiconductor side. Thus the potential barrier height can be negligible and current flow back and forward between metal and semiconductor is enhanced. Another method is to heavily dope semiconductor material because of the dependency of energy barrier width toward semiconductor doping level. With high levels of doping, the barrier width is severely reduced in both case of p-type or n-type semiconductor. Hence, the current can easily tunnel through the barrier from metal to semiconductor when positive voltage is applied on the heavily doped n-type semiconductor side. When a negative voltage is applied, electrons not only overcome the barrier but also tunnel through it from semiconductor to metal. [15]

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CHAPTER 3: FABRICATION OF METALLIC NANOSTRUCTURES

3.1 Introduction

Metallic nanostructures play as vital part for the fabrication of innovative nanodevices (electronic, optical, sensory, plasmonic …). Numerous scientists recently point out the strong relationship between chemical and physical properties with structural properties of nanostrutures. Thus, one way to tuning nanodevices' functionalities is to engineer geometric parameters of metallic nanostructures such as gratings, circles, rings … This chapter presents the efforts of fabricating several interested metallic nanostructures using Electron Beam Lithography system JEOL 5500ZD as the main tool to archive nanometric resolution.

3.2 Fabrication process

The fabrication process of metallic nanostructures should go through dose calibration step since there are no EBL recipes built up from the beginning. As shown in figure 3.1, this calibration step starts with traveler preparation, structure design with multiple layers of doses, substrate preparation, EBL writing, metal deposition and lift off. Scanning electron microscopy (SEM) pictures will be taken in the end to examine the optimized exposure dose according to that structure's parameters. This particular part could be repeated several times until the level of accuracy of metalized patterns 'parameters meet user's requirements. After completing dose calibration, optimized dose will be applied on the real sample which shares the same fabrication processes listed above with the calibration step except the new structure design containing only the optimized dose. During the whole fabrication process of metallic nanostructures, others calibrations have been made such as electron beam resist spinning thickness, metal deposition thickness, and lift off process.

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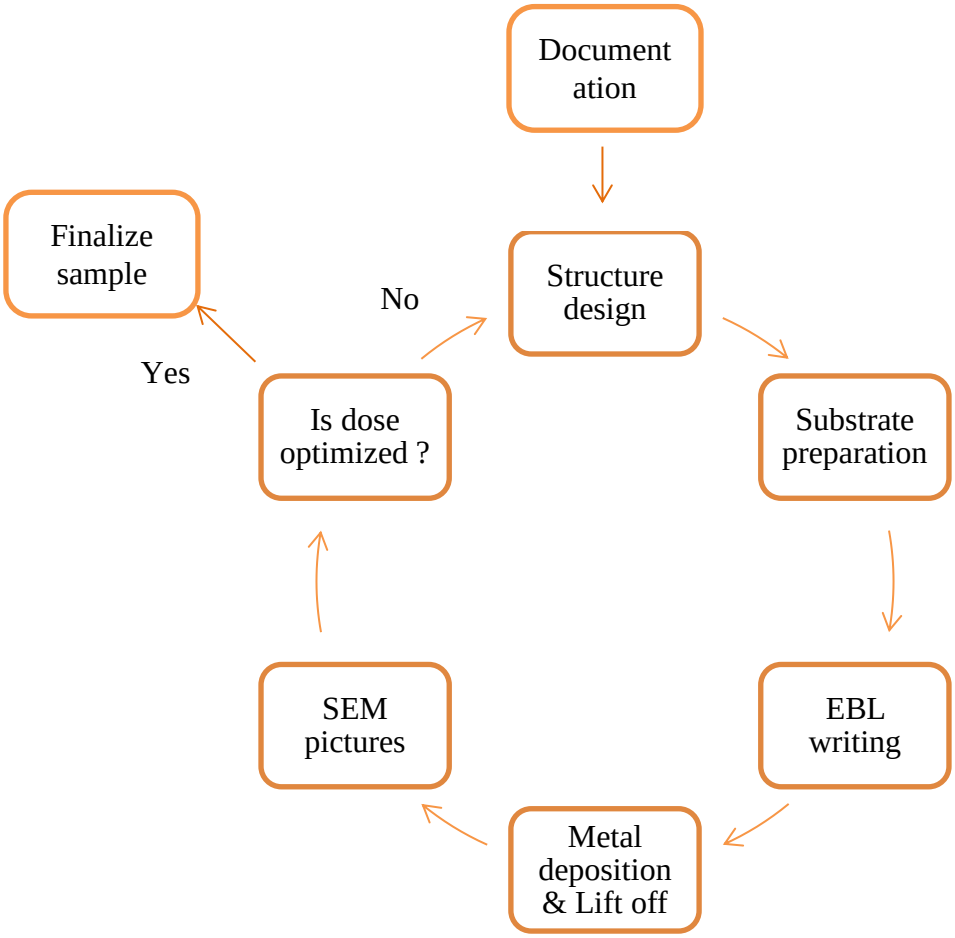

Figure 3.1 Process flow of metallic nanostructures fabrication (Thach Pham, July 2013)

Three particular structures having been studied and fabricated are lines, circles, and rings. Fabrication goals:

- Lines: study ZEP 520A and calibrate line width to 100nm.
- Circles: achieve sub 100nm diameter on c-Si and try fabrication process on different substrates.
- Rings: control inner and outer diameter in such way that |r1-r2| = 100nm and 200nm.

Serving for different potential applications, gratings, circles, and rings are initially fabricated on crystallized silicon substrate while fabrication on glass substrate will be conducted in future.

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Besides, two different e-beam resist has been used during calibration process: poly methyl methacrylate (PMMA) and ZEP 520A. PMMA is heavily used in fabrication process of circles and rings while ZEP 520A is used only for the study of line fabrication.

Following table 3.1 shows a list of equipment used in general fabrication process of metallic nanostructures and time estimation for each step:

Table 3.1 Relevant fabrication tools & machines

Process	Related equipment	Time cost
Traveler preparation	• Microsoft office	
Structure design	• Auto CAD 2012 • Link CAD 7	1 hour / pattern design
Substrate preparation	• Solvent bench • Spinner • Hot plate	1 hour / 4 samples
EBL writing	• EBL system JEOL 5500ZD • Develop bench • Microscope	2-3 hours / sample
Metal deposition	• Thermal evaporator AUTO 306T	3-4 hours / multiple samples
Lift off	• Wet bench • Ultra sonic bath • Microscope	2 days
SEM pictures	• FEI NOVA 200	2 hours / sample

In summary, it will take 4 days to complete one round either for control sample or final sample.

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3.2.1 Traveler preparation

Documentation of each fabrication processes becomes indispensable step not only in industry but also in academic research. Those important documents, travelers, which record critical processing parameters are initially generated based on a general model provided by researchers. Then, after finishing one loop of process, traveleres will be revised and updated until fabrication recipes of that process is optimized. For each particular device, there will be a separated set of traveler.

The discrepancies between traveler and standard operating procedure (SOP) are shown in table 3.2.

Table 3.2 Traveler vs. SOP

Traveler	SOP
Devices based	Equipment based
One time use	Multiple time use
Record critical processing parameters	Contain detailed machine ‘s instructions

3.2.2 Structure design

Structure design is another important preparation step in the fabrication of metallic nanostructures since electron beam lithography is direct writing which does not require a photo mask but a digital plot. The plot, containing the design of nanostructures, could be drawn either from built in program of EBL system called “pattern design” or from third party program such as Auto CAD, a powerful and compatible design tool. Most of design works in my thesis are based on Auto CAD 2012, student version, since it offers drawing flexibility, less time consuming, as well as huge number of exposure dose (EBL “pattern design” only allows 15 layers for each design).

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There are always two types of pattern design for each metallic nanostructure in this step:

- Calibration process pattern design
- Final process pattern design

(a) Calibration process pattern design:

A set of five by five arrays representing 25 distinct exposure doses will be generated to cover 1mm^2 writing area, as shown in figure 3.2a and figure 3.3a. Each similar array contains different structure size ranging from 60nm to 1um and specific dimension marks underneath of those structures, as shown in figure 3.2b and figure 3.3b. In addition, three to five PQ marks, cross marks of 3um width and 300um long are also unevenly distributed at left, right, top and bottom of defined writing area. This enables user to recognize the pattern under microscope after developing, to evaluate lift off process, as well as to comfortably orientate testing sample with SEM camera. Moreover, user has option to modify pitch size in such way that fits to the 1mm^2 writing area.

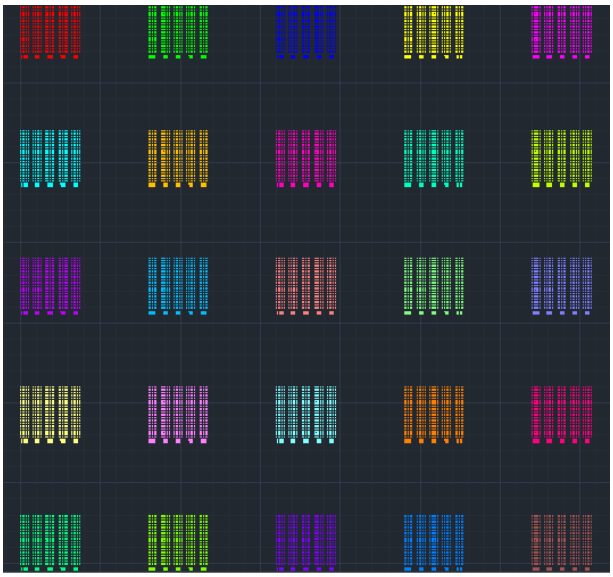

Figure 3.2 (a) CAD design 5x5 arrays of different doses (Thach Pham, December 2012, Auto CAD 2012)

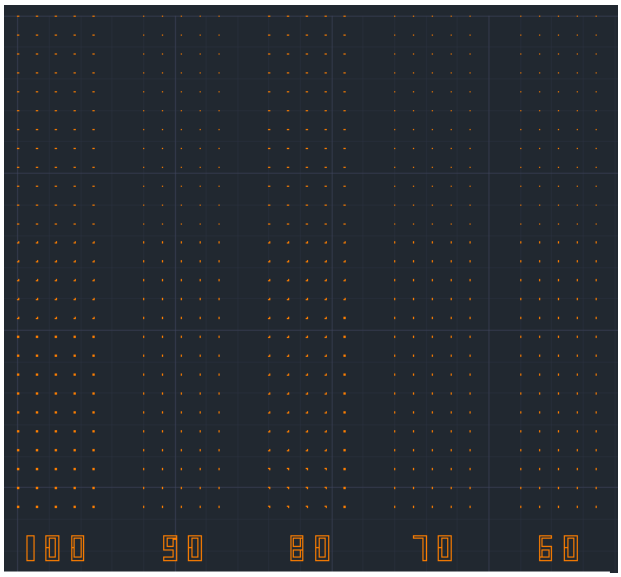

Figure 3.2 (b) Zoom in CAD design 5x5 arrays of different doses (Thach Pham, December 2012, Auto CAD 2012)

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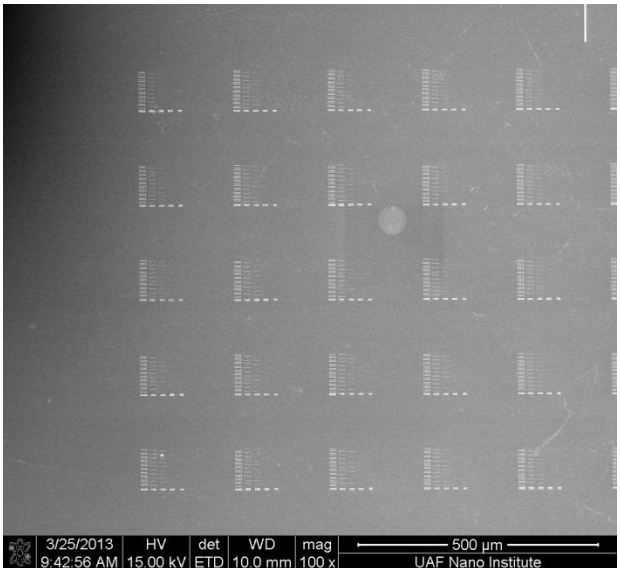

Figure 3.3 (a) SEM pictures of metalized 5x5 arrays design (Thach Pham, March 2013, University of Arkansas)

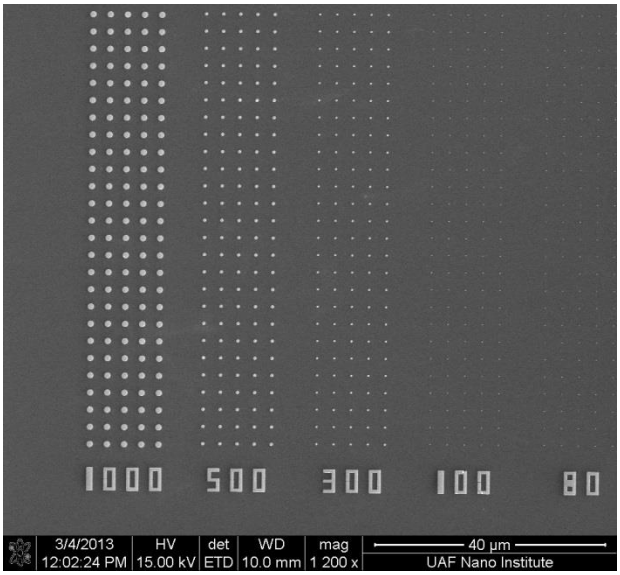

Figure 3.3 (b) Zoom in SEM picture of metalized single array design (Thach Pham, March 2013, University of Arkansas)

(b) Final process pattern design

A large array of structure is formed covering 1mm^2 area instead of 5x5 arrays, as shown in figure 3.4. Exposure dose is optimized from control sample and pitch size is also modified. PQ marks stay the same as those in control sample.

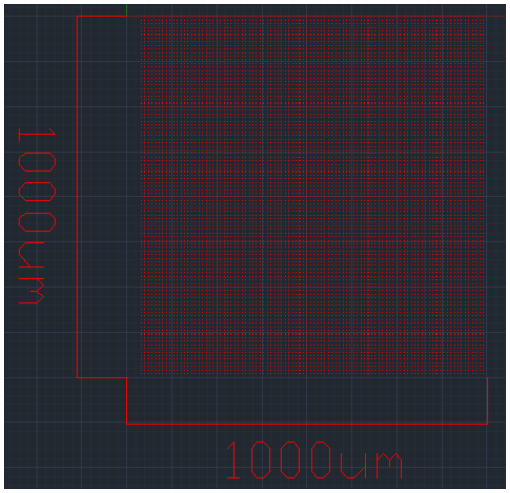

Figure 3.4 CAD design single array covering 1mm^2 area (Thach Pham, December 2012, Auto CAD 2012)

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Although pattern design does not resemble in two processes listed above, it still goes through similar converting process to be translated into input file of EBL JEOL 5500ZD, v30 file as shown in figure 3.5.

- In Auto CAD 2012, save as *.dwg file into *.dxf file.
- In LinkCAD 7, convert *.dxf file into *.gdsii file.
- In Pattern design (EBL system interface), convert *.gdsii file into *.v30 file.

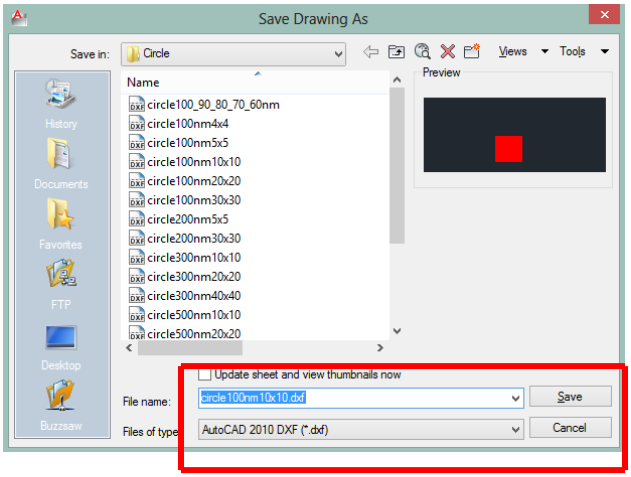

Figure 3.5 (a) Convert dwg file into dxf file in Auto CAD (Thach Pham, July 2013)

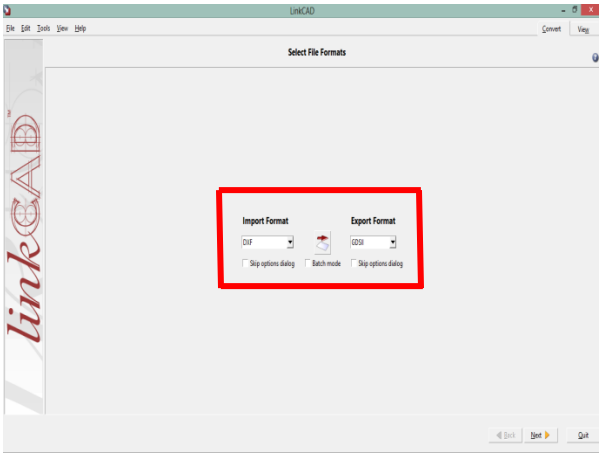

Figure 3.5 (b) Convert dxf file into gdsii file in LinkCAD (Thach Pham, July 2013)

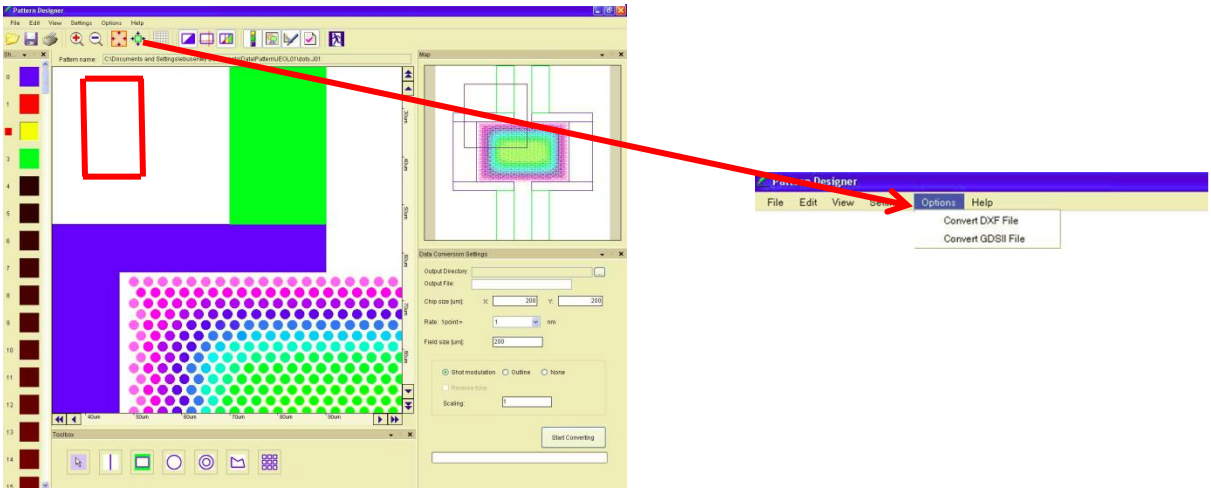

Figure 3.5 (c) Convert gdsii file into v30 file in Pattern Design [14]

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3.2.3 Substrate preparation

In this section, we discuss about required steps to prepare sample before e-beam lithography writing. 1cmx1cm piece c-Si sample goes through cleaning process and coating process.

(a) Cleaning step:

- Clean piece c-Si sample using acetone, methanol, and isopropyl alcohol (IPA) respectively and followed by DI water cleaning. Do not let the surface of sample dry out.
- Dry sample using N_2 gun.
- Dehydrate sample at 90^o C for 5 minutes and let it cool down.
- Check with microscope.

Since c-Si piece sample is diced from high qualify 5" Si wafer, there is no need to apply standard cleaning procedure e.g. RCA cleaning.

(b) Resist coating step:

- Cover spinning plate with blue tape to protect the back of sample and vacuum chuck.
- Spin coat poly methyl methacrylate (PMMA) 495K 2% at 3000 rpm. This gives approximately 60nm of resist thickness.
- Bake coated sample at 180^oC for 2 minutes and let it cool down.

Resist thickness of PMMA 495K (2% and 4%) and ZEP 520A (diluted 1:1, 1:2, 1:4 ratio) is carefully calibrated using both Nanospec (optical measurement) and Dektak profilometer (physical contact) in High Density Electronics Cener (HiDEC)'s cleanroom. Experiment data are collected and presented in table 3.3. The working principle of nanospec (figure 3.6) is

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conducting measurement of reflected light to determine film thickness based on interference effects. Thus, it requires a solid and reliable refractive index value of the coating resist which could be accessed in datasheet provided by chemical company. In the other hand, dektak profilometer (figure 3.7) applies surface contact measurement technique where a tip is dragged across the scratched surface of coated control sample.

Table 3.3 Resist thickness of PMMA and ZEP 520A

E-beam resist	Spin speed	Resist thickness
PMMA 495K 2%	3000 rpm	50-60nm
PMMA 495K 4%	3000 rpm	200nm
ZEP 520A 1:1	3000 rpm	174nm
ZEP 520A 1:2	3000 rpm	114nm
ZEP 520A 1:4	3000 rpm	50nm

Figure 3.6 Nanospec (Thach Pham, July 2013, University of Arkansas)

Figure 3.7 Dektak profilometer (Thach Pham, July 2013, University of Arkansas)

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3.2.4 Electron beam lithography writing

If chapter 2 provides working principle of electron beam lithography JEOL 5500ZD, this section will explore in details important processes and techniques to successfully “write” patterns having final dimensions matching to those in design step.

(a) Sample loading:

- Load sample into cassette.
- Load cassette into chamber 2.
- Pump down chamber 2 until VG2 reaches 4E-3 Pa.
- Open valve connecting 2 chambers and load cassette into chamber 1.
- Pump down system until VG2 reaches 1E-5 Pa and gun valve pops out.

Positioning sample in cassette:

For each EBL exposure, only one sample could be loaded. Coated with e-beam resist, the sample is placed in an appropriate cassette corresponding to sample size. Currently, EBL JEOL 5500ZD supports three main types of cassette: 4” cassette (hold 4” wafer), 2” cassette (hold 2” wafer), and piece cassette (from 1cm x 1cm to 1”x1”) as shown in figure 3.8, figure 3.9, and figure 3.10 respectively.

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Figure 3.8 (a) Front side of 4” cassette (Thach Pham, January 2013, University of Arkansas)

Figure 3.8 (b) Back side of 4” cassette (Thach Pham, January 2013, University of Arkansas)

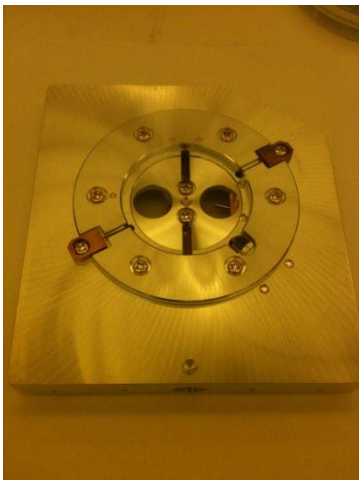

Figure 3.9 (a) Front side of 2” cassette (Thach Pham, January 2013, University of Arkansas)

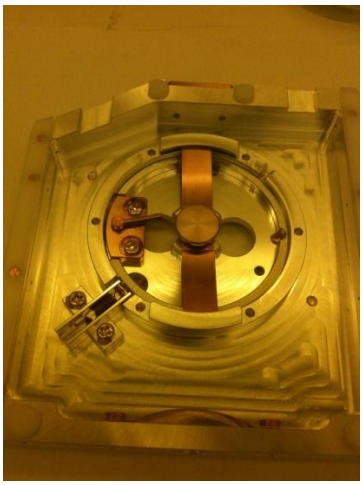

Figure 3.9 (b) Back side of 2” cassette (Thach Pham, January 2013, University of Arkansas)

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Figure 3.10 (a) Front side of piece cassette (Thach Pham, January 2013, University of Arkansas)

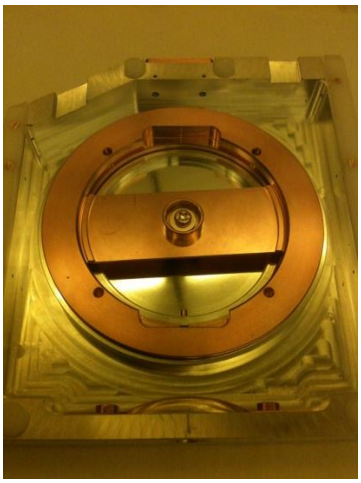

Figure 3.10 (b) Back side of piece cassette (Thach Pham, January 2013, University of Arkansas)

In order to save writing time and materials cost, piece cassette turns out to be the best choice for calibration process of metallic nanostructures fabrication.

The sample could be positioned anywhere along the triangle region as long as user records that position. In case of 1cm x 1cm sample size, because of the sample size and the mismatch between software and sample position (will be discussed in exposure part) it is recommended to place sample in such way that its center is 1cm above from the one of piece cassette, as shown in figure 3.11.

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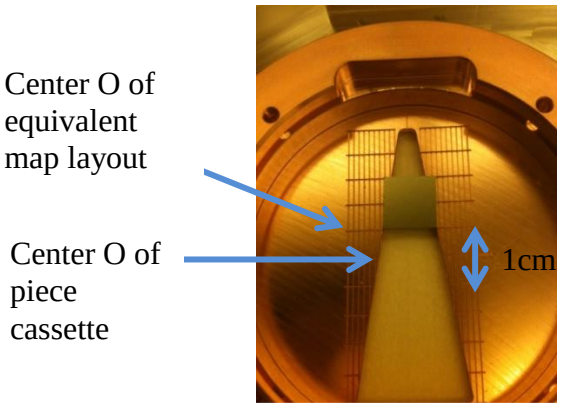

Figure 3.11 (a) Back side of loaded piece cassette, (Thach Pham, January 2013, University of Arkansas)

Figure 3.11 (b) Front side of loaded piece cassette (Thach Pham, January 2013, University of Arkansas)

(b) Calibration

Calibration process in EBL could be either simple or complicated depending on the user's purpose. This section only mentions basic calibration process as shown in figure 3.12 for regular exposure while section on nanowire device will explain advanced techniques in alignment calibration.

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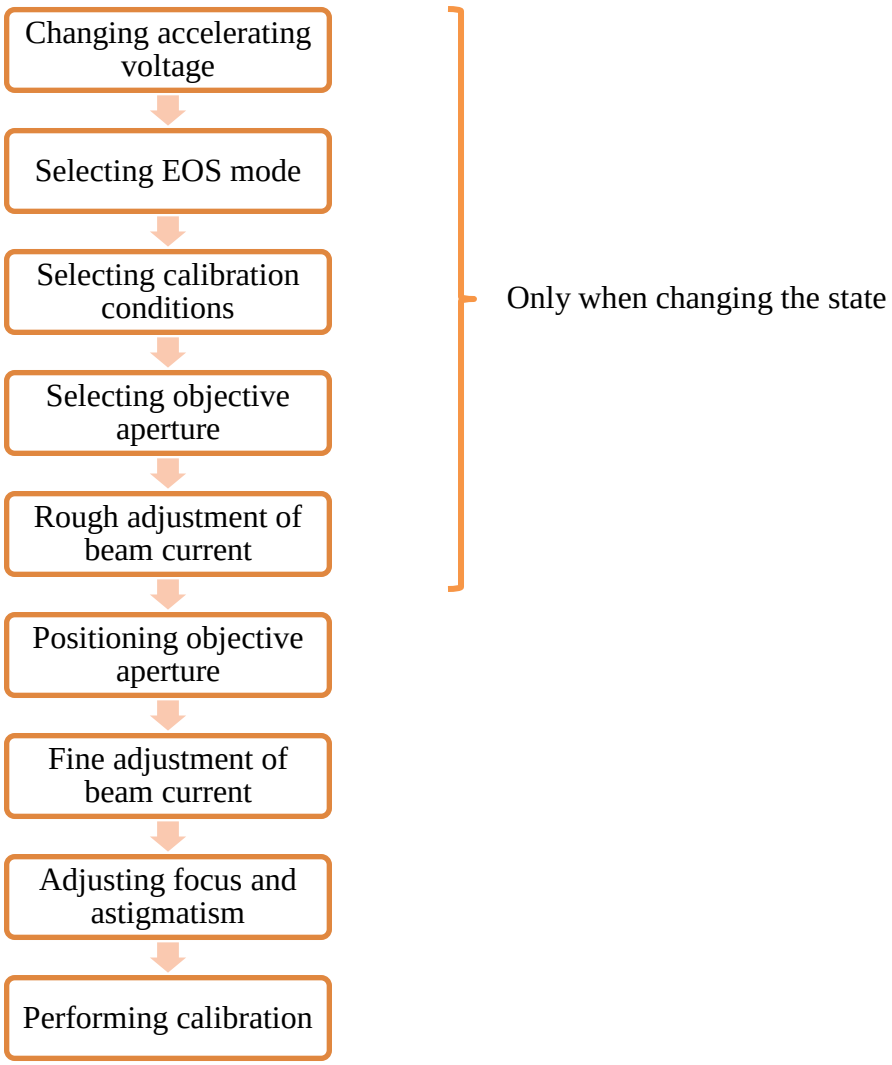

Figure 3.12 Flow of basic adjustment (Thach Pham, July 2013)

The default setting starts with EOS mode 2 where acceleration voltage is set at 50KV. 4th lens and 2nd aperture are also set as default. Although standard beam current starts with 1nA, it could be tuned to smaller beam current which provides smaller beam spot. Figure 3.13 summarizes the relation between current and spot size. Red, green, blue and purple curves represent aperture 1, 2, 3, and 4 respectively. At 1nA 2nd aperture, the beam size is approximately 15nm.

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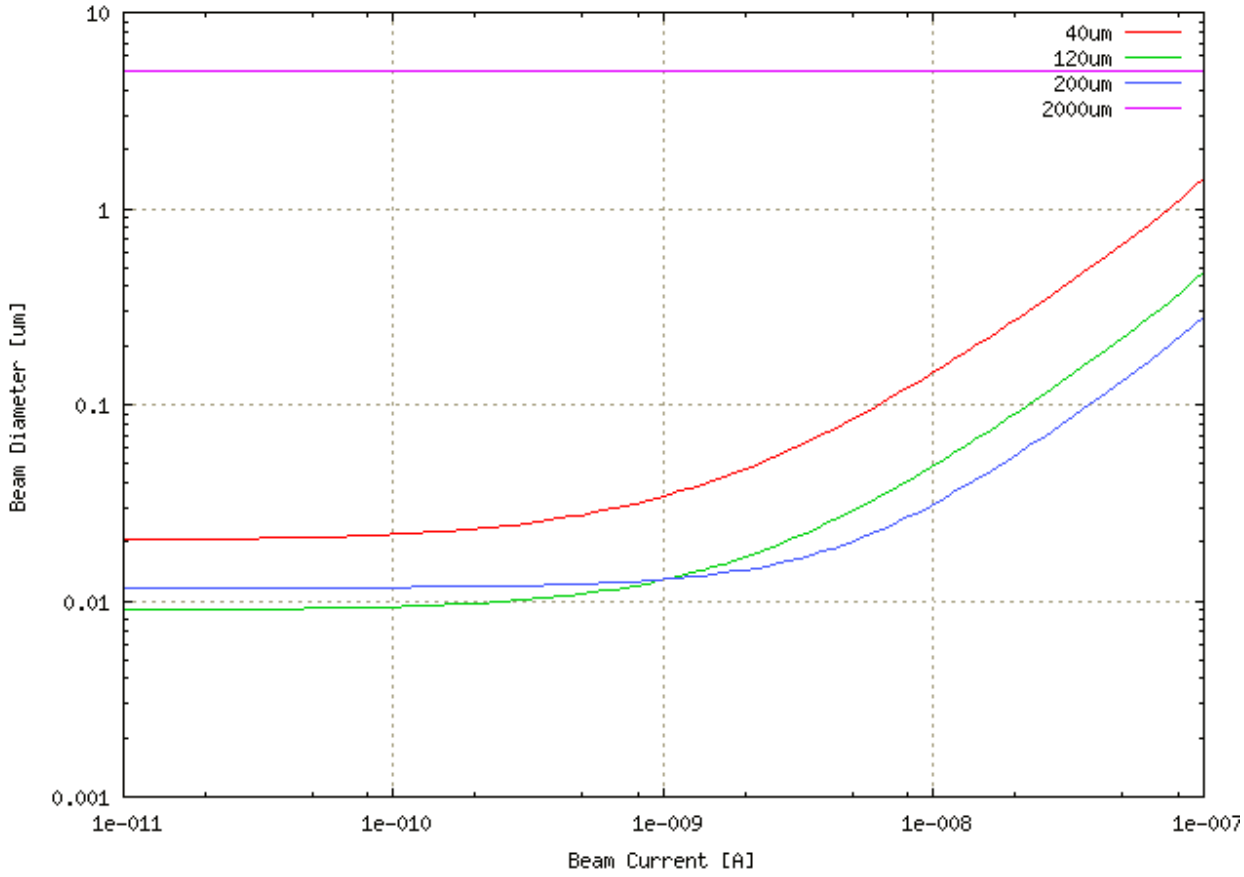

Figure 3.13 Beam current vs. beam diameter [14]

For some particular nanostructures (e.g. line width less than 60nm or circle diameter less than 100nm), EOS mode 4 is preferred since it provides a smaller working range of e-beam spot size. Another factor to be considered when switching between EOS modes is time cost because writing time and beam current are inversely proportional.

(c) Exposure

- Open exposure table and import *.v30 files.
- Choose layout type: piece cassette.
- Select exposure dose.
- Place chips on layout in correct position.
- Edit job property:

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- Scan step 1
- Calibration condition file must match with user's calibration file
- Cycle: each chip
- Calibration mode: deflection

- Save layout file.
- Select exposure.
- When exposure is done, record writing time and stop the beam.
- Move the stage back to its original position before unload sample.

Mismatch of sample position with exposure layout software (piece cassette)

As show in figure 3.11b, the center of piece cassette is marked by a unique dot of the triangle. However, 0 in the exposure software (piece cassette layout) does not represent the center of piece cassette. It is located at 10mm above from the origin 0. Consequently, user must record the coordinates of sample position to avoid any misplacing problem.

Exposure dose plan

JEOL 5500ZD has a very unique dose system. User has to input base dose (line and plane dose) from which he/she is able to expand from a single base dose to multiple doses, named as shot rank table. The number of exposure doses depends on the total number of layers that pattern design carries within. The new dose is calculated as the sum of initial dose and input percentage of that initial dose. It could be either positive percentage or negative one. For instance, base dose is 500 uC/cm^2 and percentage input for 1st layer is 10. The 1st dose will be 550 uC/cm^2 or 1.1 time of 500 uC/cm^2. If the input is -10, the 1st dose will be 450 uC/cm^2. The resolution for choosing 500 uC/cm^2 as the initial dose is 5 uC/cm^2. User has the freedom to input a different number for initial dose. Recommended value for starter is 800 uC/cm^2.

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(d) Develop

- Unload the sample from the cassette
- Prepare 3 separate beakers:
    - Developer IPA:MIBK 3:1
    - IPA
    - DI water
- Develop sample in IPA:MIBK 3:1 for 60 seconds.
- Dip sample in IPA beaker for another 30 seconds
- Rinse with DI water and dry out using N_2 gun
- Evaluate sample pattern under microscope

The develop time is mainly decided based on exposure dose. For each type of resist, there is an optimized dose for a certain parameter of structures. A great amount of time has been spent going back and forth between exposure dose and develop time. The strategy is to keep one variable constant and let the other changes. For instance, develop time is kept at 60s and exposure doses are varied from 400 uC/cm^2 to 1200 uC/cm^2 to fabricate circle of 100nm diameter; e-beam resist is PMMA 495K 2%. After taking SEM pictures, the quasi optimized exposure dose will be found otherwise the process is repeated with a modification of develop time. Recommended starting develop time is 60s.

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ZEP 520A study

For the case of ZEP 520A, developer IPA:MIBK 3:1 is replaced by n-amyl acetate. The develop time of ZEP 520A are influenced by developer's temperature [16]. At colder develop temperature, higher resolution will be archived. However, this process is temporary delayed due to time consuming (need brand new dose plan) and less significance comparing with other fabrication process such as rings and circles. Line structure is used for this type of experiment where line width from 116nm to 65nm has been achieved, as shown in figure 3.14.

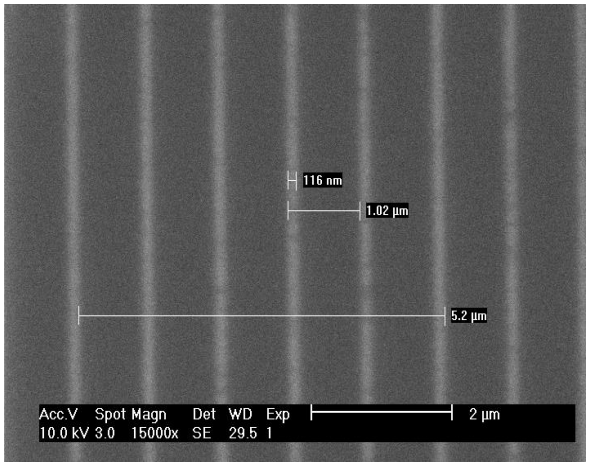

Figure 3.14 (a) Line width of 116nm, pitch size of 1um (Thach Pham, November 2012, University of Arkansas)

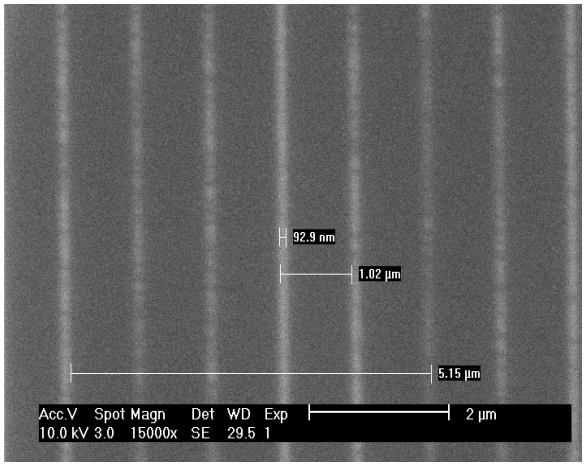

Figure 3.14 (b) Line width of 93nm, pitch size of 1um (Thach Pham, November 2012, University of Arkansas)

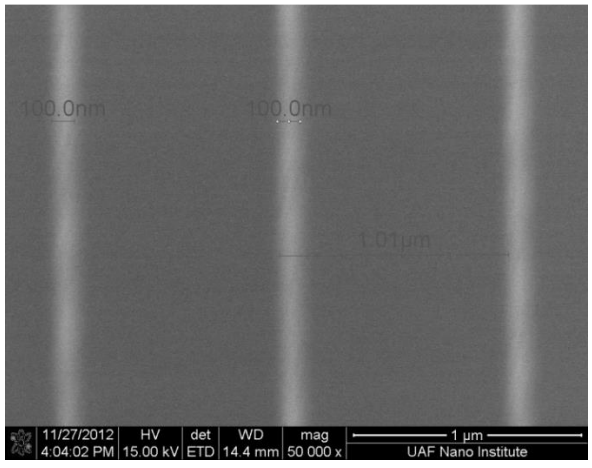

Figure 3.15 (a) Line width of 100nm, pitch size of 1um (Thach Pham, November 2012, University of Arkansas)

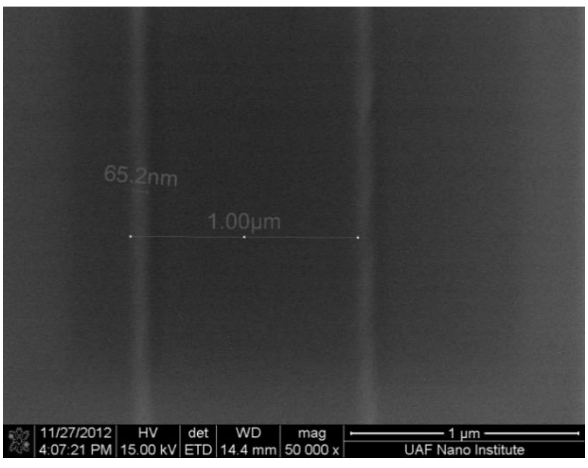

Figure 3.15 (b) Line width of 65nm, pitch size of 1um (Thach Pham, November 2012, University of Arkansas)

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Recipe summary for circle and rings structures

The fabrication of metallic lines is not in a solid state because of discontinuity of ZEP 520A study. As a result, lines recipe using ZEP 520A won't be summarized in this table where only mature recipes are listed in table 3.4.

Table 3.4 Recipe summary to fabricate rings and circles

Pattern description	Substrate	Film description	Dose (uC/cm^2) / Current (nA)	Develop information	Reference sample number
Circle 1000nm	a-Si on c-Si	200nm thick, 4% 495K PMMA, 3000rpm	860 /-1	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_03192013_1
Circle 500nm	a-Si on c-Si	200nm thick, 4% 495K PMMA, 3000rpm	735 /-1	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_03192013_1
Circle 300nm	a-Si on c-Si	200nm thick, 4% 495K PMMA, 3000rpm	735 /-1	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_03192013_1
Circle 1000nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	860 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_03122013_1
Circle 500nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	800 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_03122013_1
Circle	c-Si	60nm thick,	710 /-0.5	3:1 IPA:	T_03122013_1

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300nm		2% 495K PMMA, 3000rpm		MIBK 60sec, IPA rinse 15s	
Circle 200nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	710 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05302013_1
Circle 100nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	620 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05142013_1
Circle 90nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	640 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05142013_1
Circle 80nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	630 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05142013_1
Circle 70nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	670 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05142013_1
Circle 60nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	760 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05142013_1
Ring d1= 500nm d2 = 900nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	510 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05302013_1
Ring d1=	c-Si	60nm thick,	510 /-0.5	3:1 IPA:	T_05302013_1

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300nm d2 = 700nm		2% 495K PMMA, 3000rpm		MIBK 60sec, IPA rinse 15s	
Ring d1= 200nm d2 = 600nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	510 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05302013_1
Ring d1= 100nm d2 = 500nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	510 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05302013_1
Ring d1= 500nm d2 = 700nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	510 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05302013_1
Ring d1= 300nm d2 = 500nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	510 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05302013_1
Ring d1= 200nm d2 = 400nm	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	510 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05302013_1
Ring d1= 100nm d2 = 300nm (not optimized)	c-Si	60nm thick, 2% 495K PMMA, 3000rpm	515 /-0.5	3:1 IPA: MIBK 60sec, IPA rinse 15s	T_05302013_1

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3.2.5 Metal deposition & Lift off

One of main purpose metalizing exposed patterns is to evaluate the recipe used for the entire fabrication process. Edwards AUTO 306T thermal evaporator (figure 3.16) is mainly used to archive this goal. Follow the metal deposition process is lift off which dissolves the unexposed e-beam resist and simultaneously removes the metal layer sitting on top of those areas. In the end, only exposed areas are metalized and the sample is ready for taking SEM pictures.

(a) Metal deposition:

- Load one/multiple sample on sample holder disc with kapton tape
- Place/replace Cr rod and fill new Au pallets on boat
- Pump down chamber for 2-3 hours until it reaches approximately 8E-6 mTorr
- Start depositing metal at rate of 1-2 A/s to obtain 5nm Cr and 30 nm Au

Figure 3.16 Thermal evaporator Edward 306T (Thach Pham, July 2013, University of Arkansas)

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(b) Lift off:

- Prepare beaker/beakers containing remover PG, a dedicated solvent stripper for PMMA
- Heat up to $70^{o}C$
- Place one sample for each beaker
- Wait 30 minutes
- Bubble sample surface in order to remove most of unnecessary metalized parts.
- Replace new solvent, cover beakers and monitor samples for a least 2 days. Fill up solvent again if it evaporates.
- Bubble sample surface and leave beakers in ultrasonic bath for 5 minutes
- Rinse samples with IPA to stop the reaction of remover PG
- Rinse samples with DI water and dry out using N_2 gun
- Examine sample under microscope. Look for PQ marks

This lift off process has been carefully calibrated for many times and reaches a solid state at the moment. Besides, remover PG could also be replaced by acetone for some applications.

Metal thickness and roughness study

The metal thickness and the film quality (roughness) are two priority concerns in this step. Many users have totally ignored thickness measurement step after depositing metal layers and always believe in machine tool. As consequence, high resolution SEM picture and atomic force microscopy (AFM) are used to conduct the study of metal thickness and roughness.

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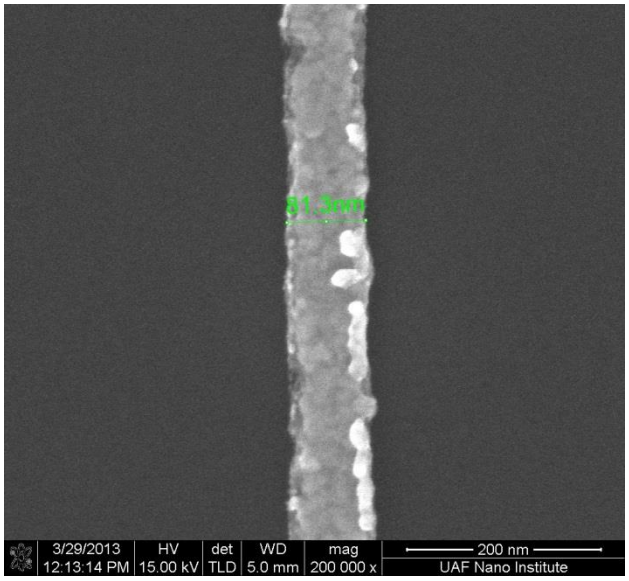

Figure 3.17 (a) SEM picture of metalized line with high roughness (Thach Pham, March 2013, University of Arkansas)

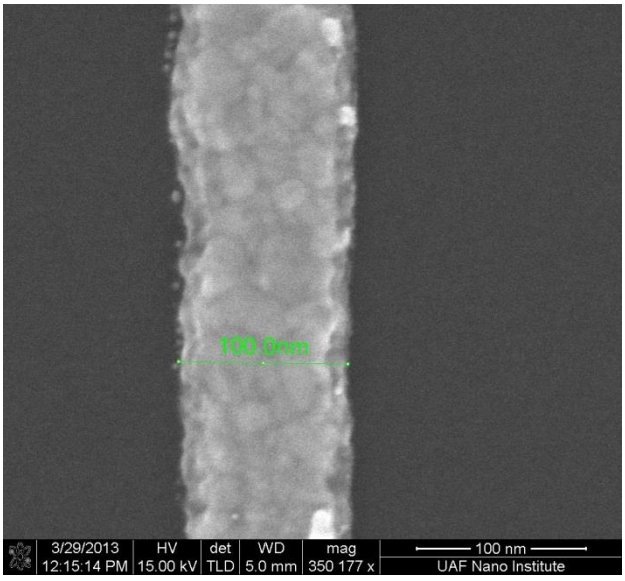

Figure 3.17 (b) SEM picture of metalized line with high roughness (Thach Pham, March 2013, University of Arkansas)

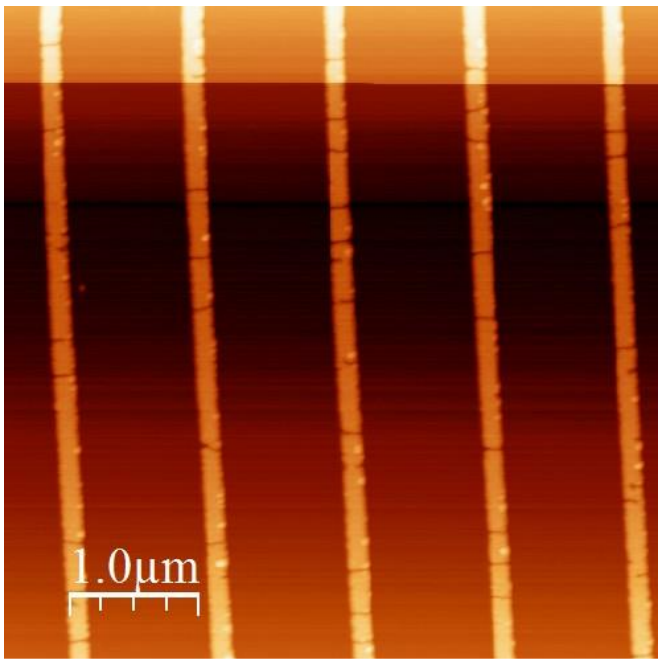

Figure 3.18 (a) AFM surface geometry of multiple lines (Thach Pham, March 2013, University of Arkansas)

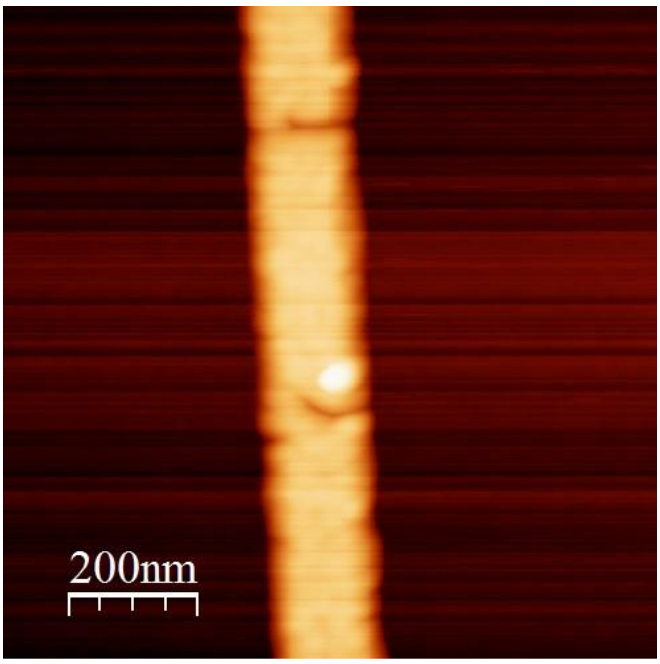

Figure 3.18 (b) AFM surface geometry of single line (Thach Pham, March 2013, University of Arkansas)

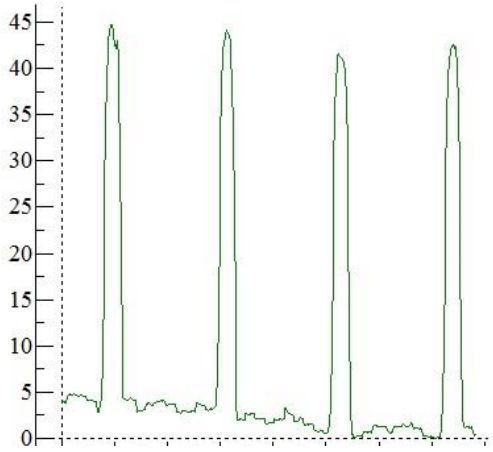

Figure 3.19 (a) AFM data, metal thickness of multiple lines (Thach Pham, March 2013, University of Arkansas)

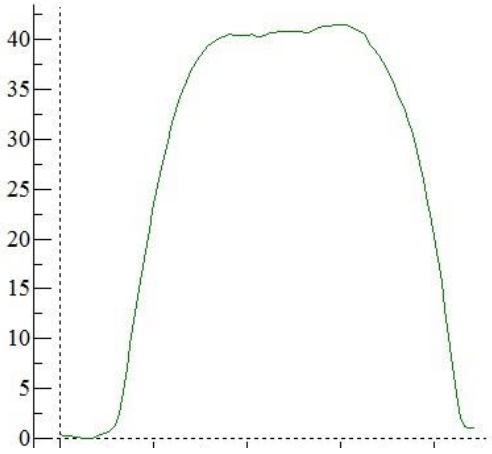

Figure 3.19 (b) AFM data, metal thickness of single line (Thach Pham, March 2013, University of Arkansas)

From figure 3.17, figure 3.18, and figure 3.19 a thicker layer of Cr/Au has been deposited (approximately 40nm instead of 30nm) and possesses high roughness. The temporary solution for the metal deposition using thermal evaporator is to lower the deposition rate from 1-2 A/s to 1-2 A/5s or much slower. However, this will raise the temperature inside the chamber. Thus, e-beam resist will melt down and make lift off process much harder. A better solution is to use electron beam evaporator to deposit metal layer since it works in atomic scale.

Lift off problem: rings structure

As shown in figure 3.21, most of metallic rings could not be lift off using 5nm Cr / 30nm Au. Possible reason is that e-beam resist is thin while deposited metal layer might too thick to lift off. From AFM thickness measurement results, depositing 5nm Cr / 30nm Au yields approximately 40-55nm of metal layer, which approaches resist thickness. In addition, heat generated during the metalized process could melt resist's top surface and edges. Consequently, developer barely reaches to open area of e-beam resist and metal layer attaching to the resist remains on unwanted sites, as shown in figure 3.20.

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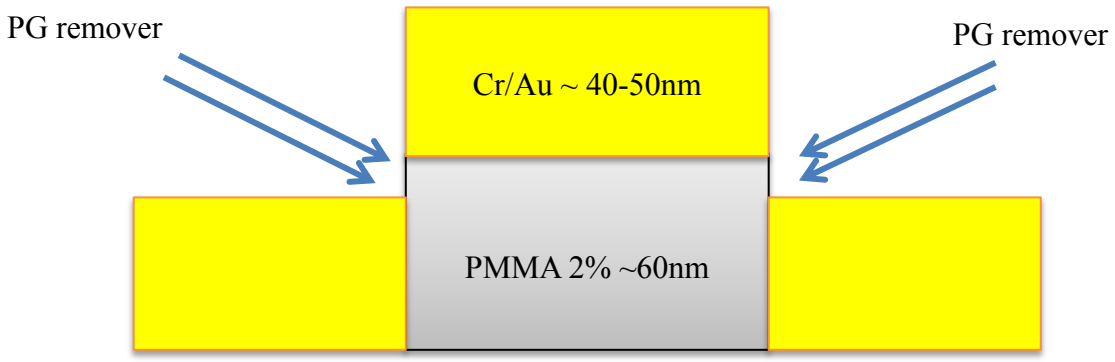

Figure 3.20 Thick layer of metal prevents PG remover to attack e-beam resist (Thach Pham, July 2013)

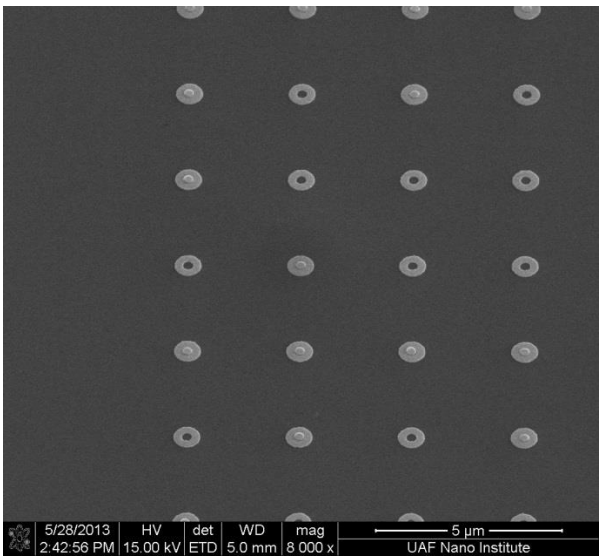

Figure 3.21 (a) SEM picture of ring structure where lift off fails (Thach Pham, May 2013, University of Arkansas)

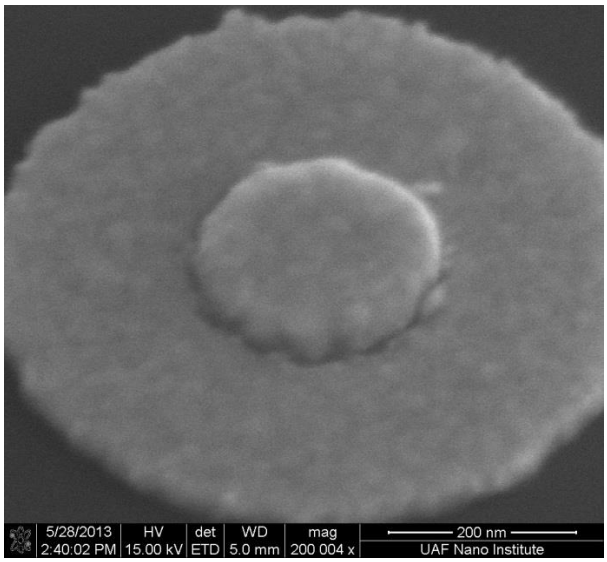

Figure 3.21 (b) Zoom in SEM picture of ring structure where lift off fails (Thach Pham, May 2013, University of Arkansas)

One reasonable solution is to either increase resist thickness or reduce metal layer. Since dose plan's status is in solid phase using PMMA 2%, Cr and Au layer has been reduced to 2nm Cr/ 10-15nm Au. As a result, lift off is a success.

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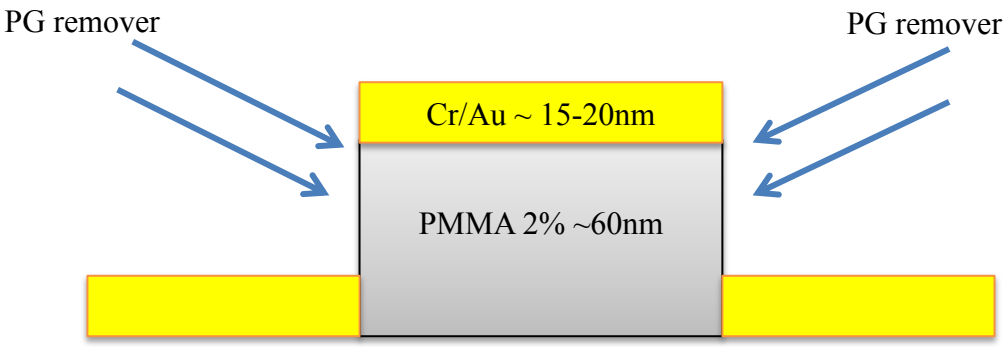

Figure 3.22 Reduce metal layer for rings structure (Thach Pham, July 2013)

3.3 SEM pictures of metallic nanostructures

In brief, a considerable amount of nanostructures having various geometrical dimensions from 1um to 60nm has been successfully fabricated using e-beam lithography system although fabrication processes encounter several technical problems. Lines width goes down to 90nm (ZEP 520A); circles diameter reaches 1um, 500nm, 300nm, 100nm, 90nm, 80nm, 70nmn, 60nm (PMMA); rings' inner diameter goes down to 70nm while outer diameter goes down to 300nm.

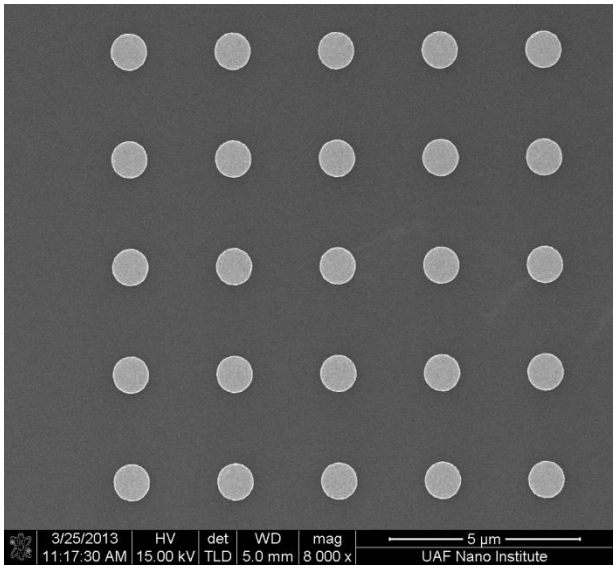

Figure 3.23 (a) SEM picture of circles having diameter of 1um (Thach Pham, March 2013, University of Arkansas)

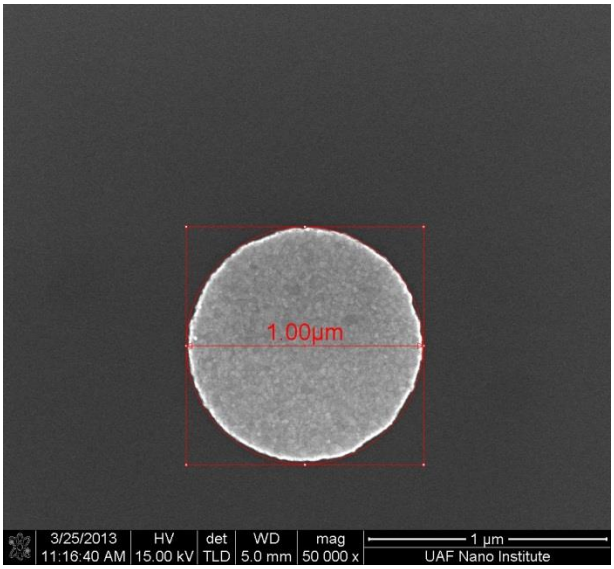

Figure 3.23 (b) Zoom in SEM picture of 1um circle structure (Thach Pham, March 2013, University of Arkansas)

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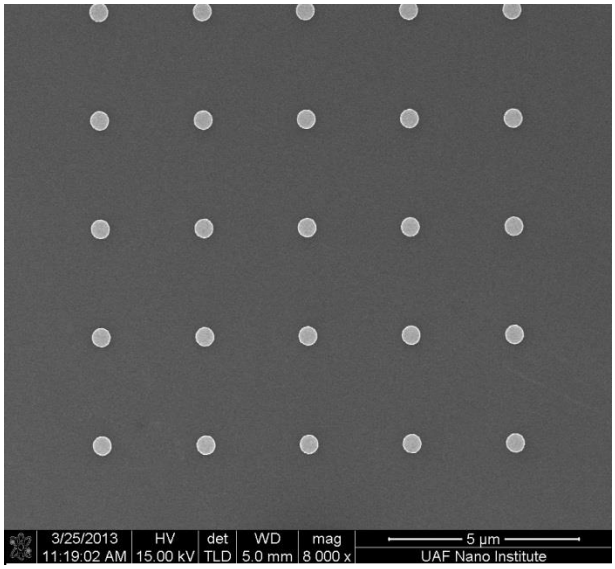

Figure 3.24 (a) SEM picture of circles having diameter of 500nm (Thach Pham, March 2013, University of Arkansas)

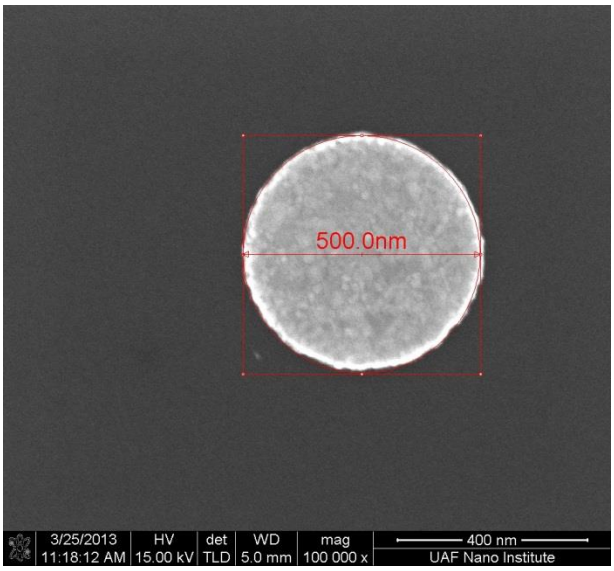

Figure 3.24 (b) Zoom in SEM picture of 500nm circle structure (Thach Pham, March 2013, University of Arkansas)

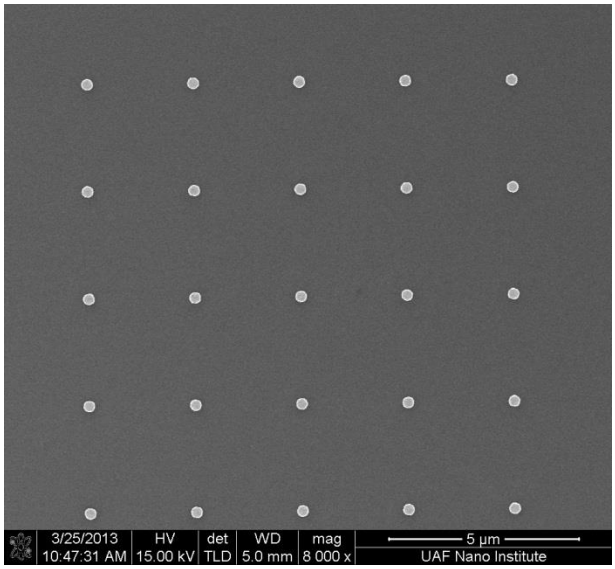

Figure 3.25 (a) SEM picture of circles having diameter of 300nm (Thach Pham, March 2013, University of Arkansas)

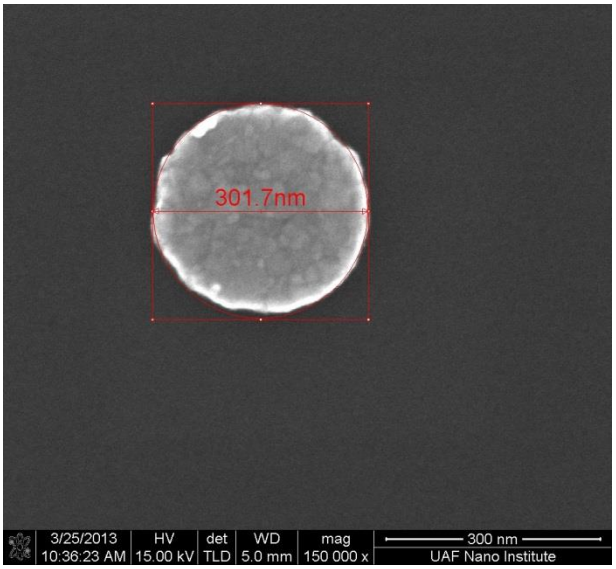

Figure 3.25 (b) Zoom in SEM picture of 300nm circle structure (Thach Pham, March 2013, University of Arkansas)

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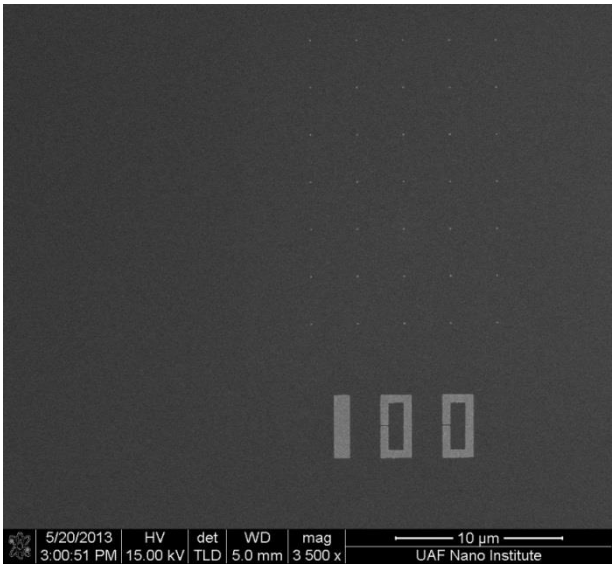

Figure 3.26 (a) SEM picture of circles having diameter of 100nm (Thach Pham, May 2013, University of Arkansas)

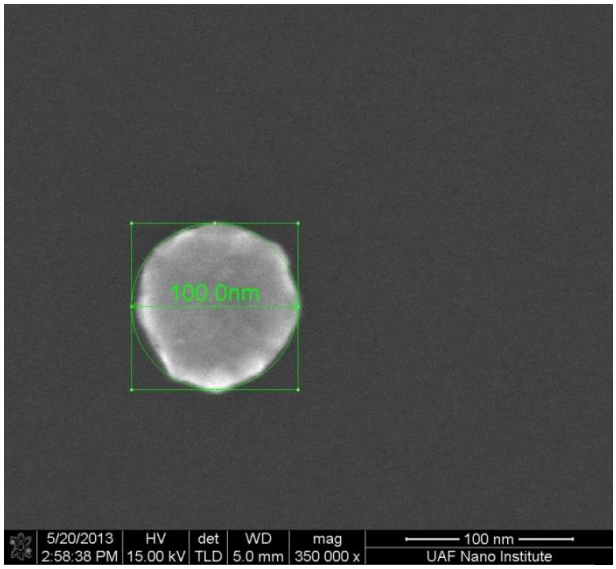

Figure 3.26 (b) Zoom in SEM picture of 100nm circle structure (Thach Pham, May 2013, University of Arkansas)

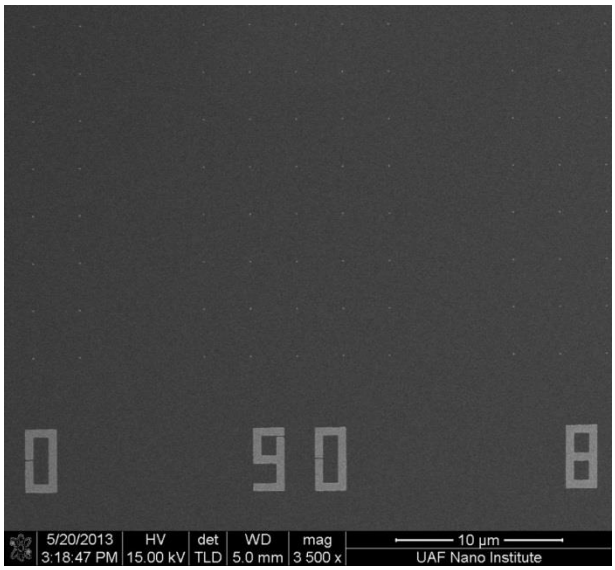

Figure 3.27 (a) SEM picture of circles having diameter of 90nm (Thach Pham, May 2013, University of Arkansas)

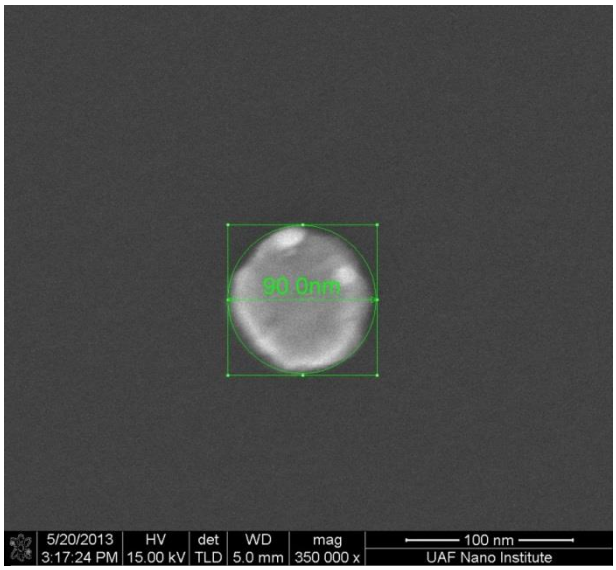

Figure 3.27 (b) Zoom in SEM picture of 90nm circle structure (Thach Pham, May 2013, University of Arkansas)

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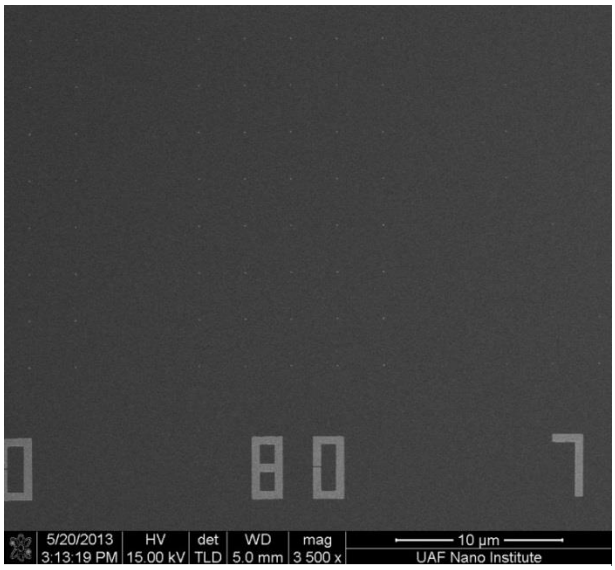

Figure 3.28 (a) SEM picture of circles having diameter of 80nm (Thach Pham, May 2013, University of Arkansas)

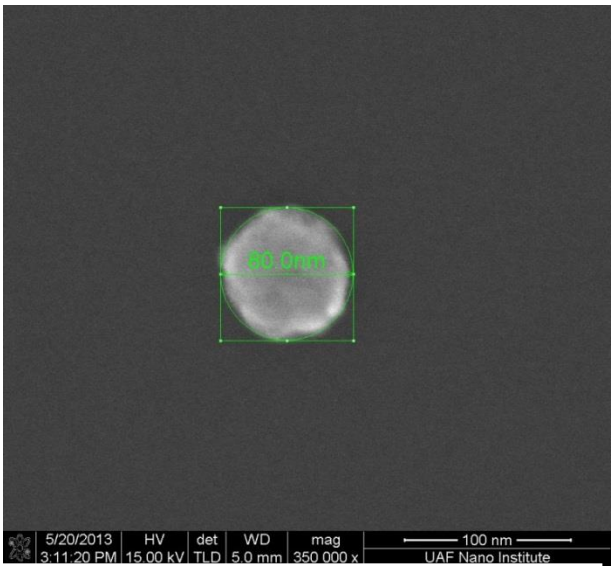

Figure 3.28 (b) Zoom in SEM picture of 80nm circle structure (Thach Pham, May 2013, University of Arkansas)

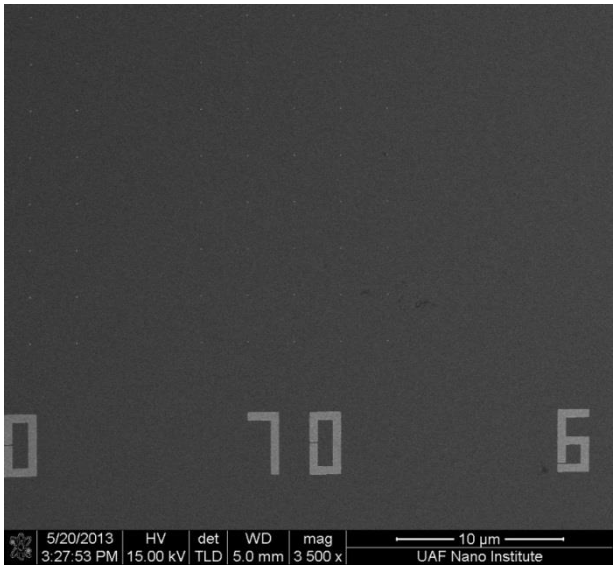

Figure 3.29 (a) SEM picture of circles having diameter of 300nm (Thach Pham, May 2013, University of Arkansas)

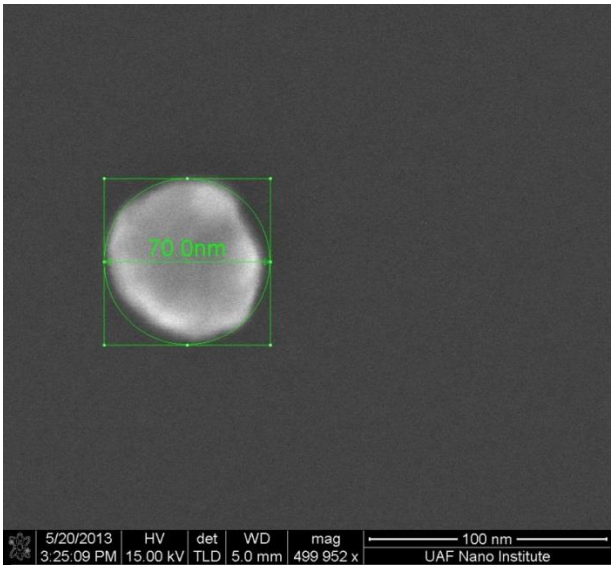

Figure 3.29 (b) Zoom in SEM picture of 300nm circle structure (Thach Pham, May 2013, University of Arkansas)

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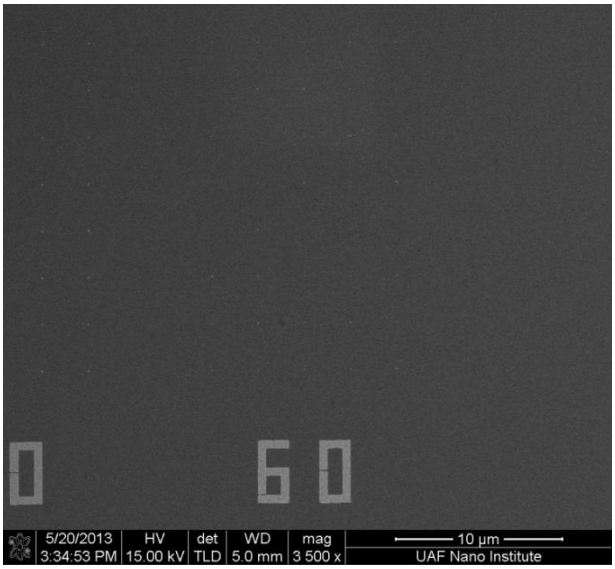

Figure 3.30 (a) SEM picture of circles having diameter of 60nm (Thach Pham, May 2013, University of Arkansas)

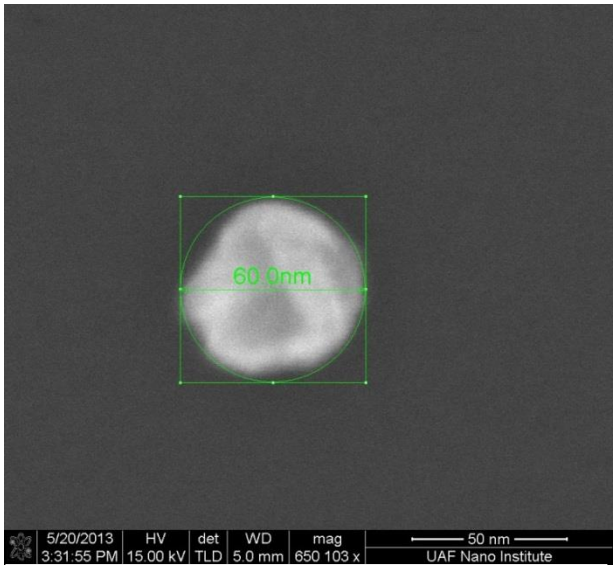

Figure 3.30 (b) Zoom in SEM picture of 60nm circle structure (Thach Pham, May 2013, University of Arkansas)

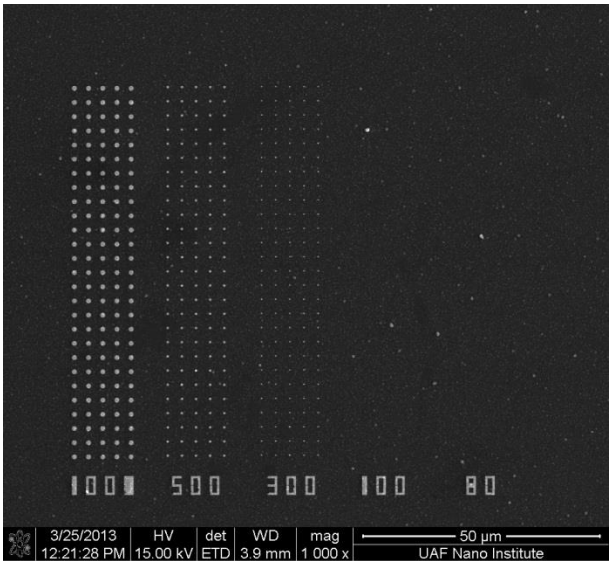

Figure 3.31 (a) SEM picture of testing layout on a-Si substrate (Thach Pham, March 2013, University of Arkansas)

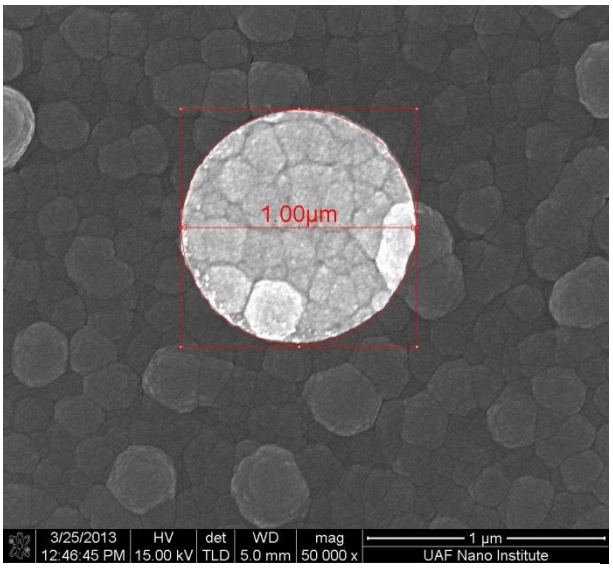

Figure 3.31 (b) Zoom in SEM picture of 1um circle structure on a-Si substrate (Thach Pham, March 2013, University of Arkansas)

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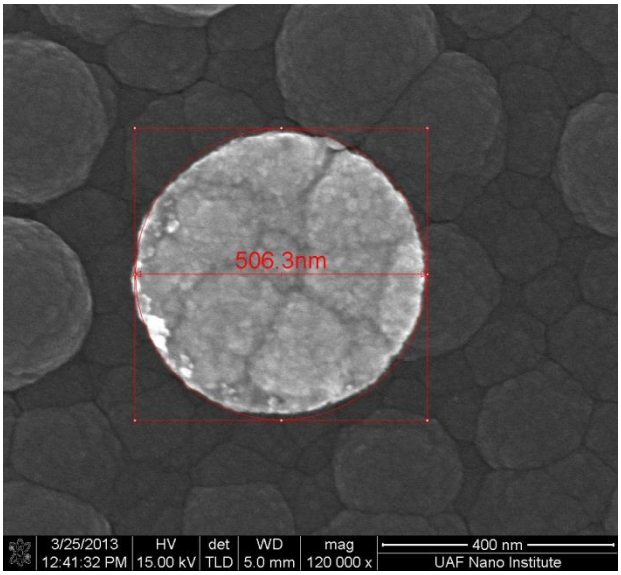

Figure 3.32 (a) Zoom in SEM picture of 500nm circle structure on a-Si substrate (Thach Pham, March 2013, University of Arkansas)

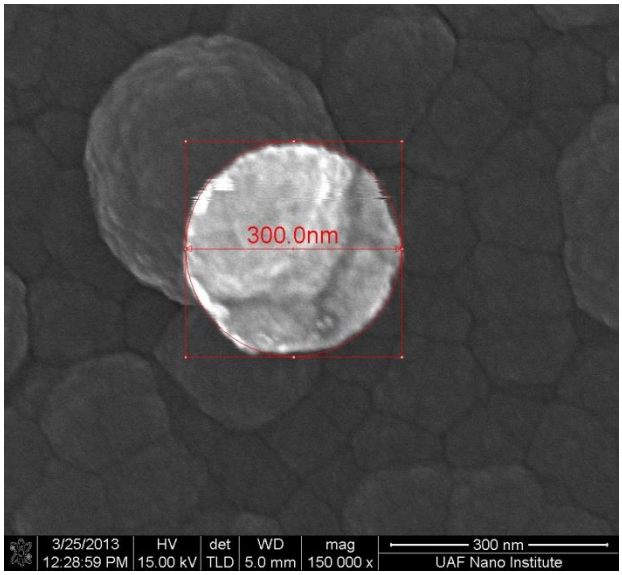

Figure 3.32 (b) Zoom in SEM picture of 300nm circle structure on a-Si substrate (Thach Pham, March 2013, University of Arkansas)

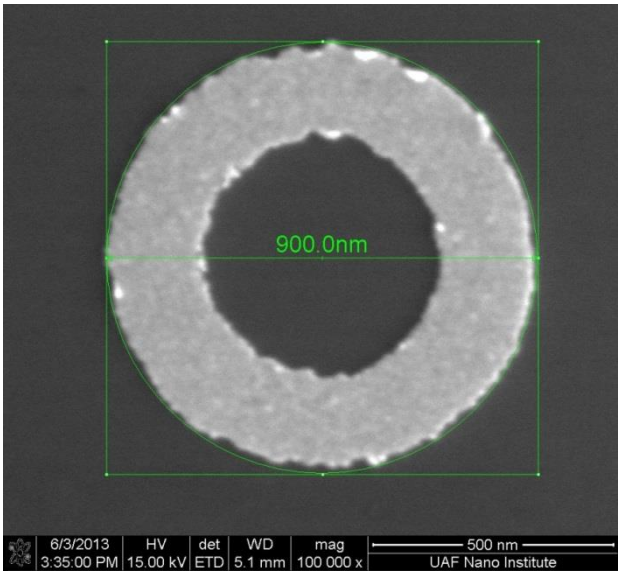

Figure 3.33 (a) Zoom in SEM picture of ring structure, outer diameter 900nm (Thach Pham, March 2013, University of Arkansas)

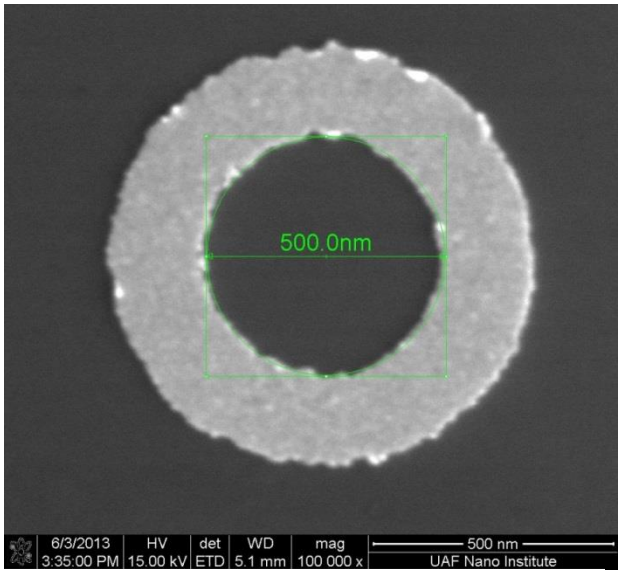

Figure 3.33 (b) Zoom in SEM picture of ring structure, inner diameter 500nm (Thach Pham, March 2013, University of Arkansas)

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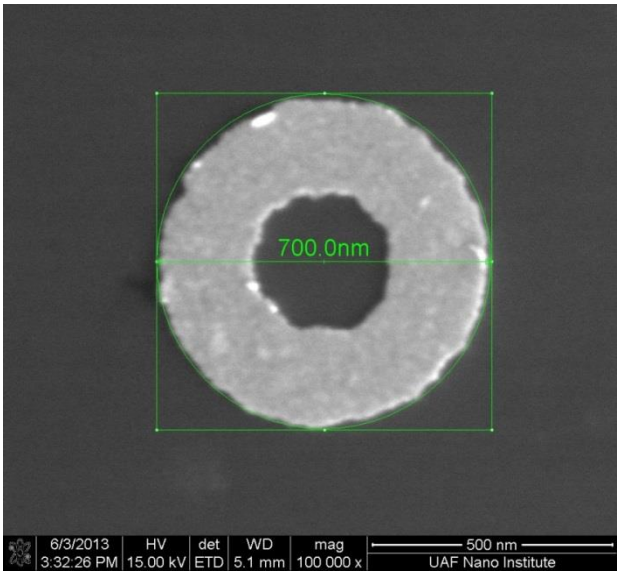

Figure 3.34 (a) Zoom in SEM picture of ring structure, outer diameter 700nm (Thach Pham, June 2013, University of Arkansas)

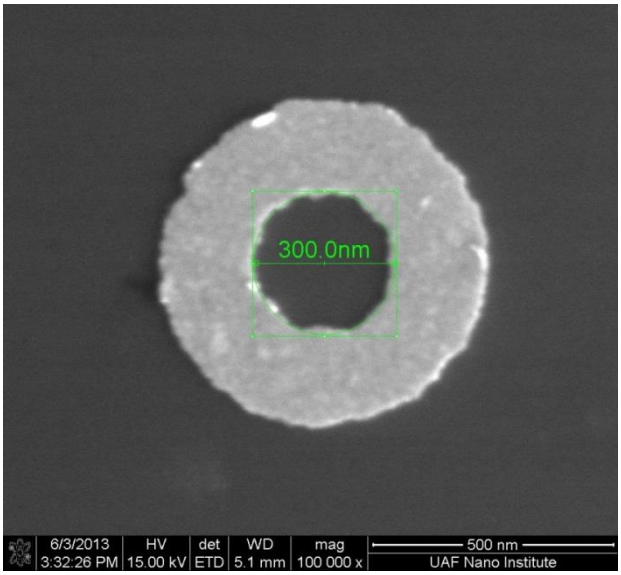

Figure 3.34 (b) Zoom in SEM picture of ring structure, inner diameter 300nm (Thach Pham, June 2013, University of Arkansas)

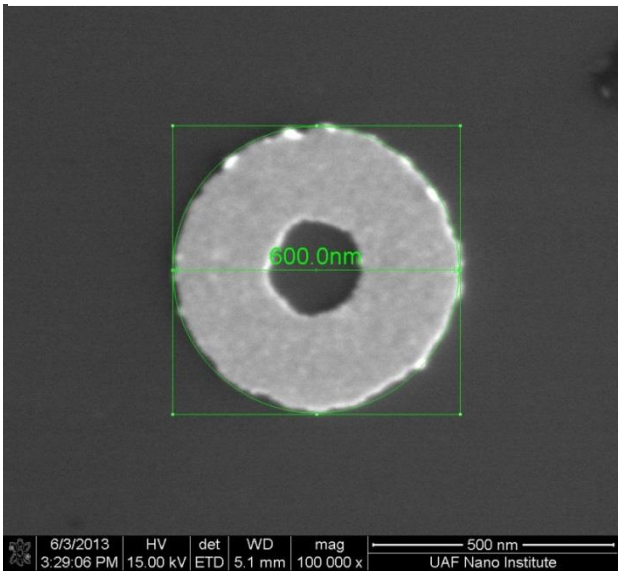

Figure 3.35 (a) Zoom in SEM picture of ring structure, outer diameter 600nm (Thach Pham, June 2013, University of Arkansas)

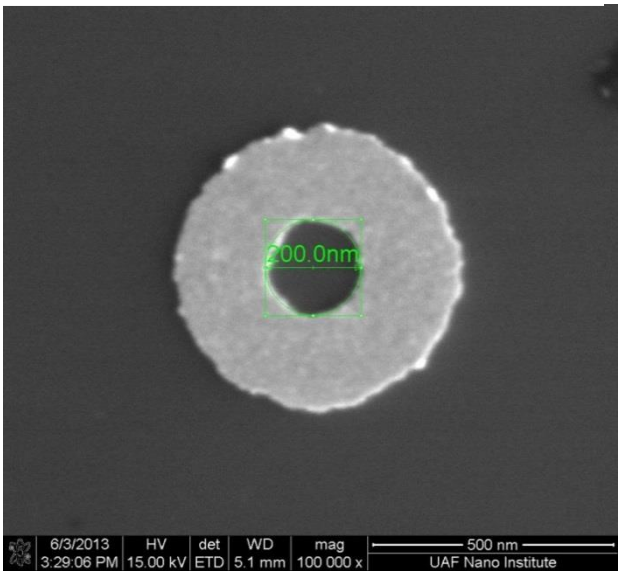

Figure 3.35 (b) Zoom in SEM picture of ring structure, inner diameter 200nm (Thach Pham, June 2013, University of Arkansas)

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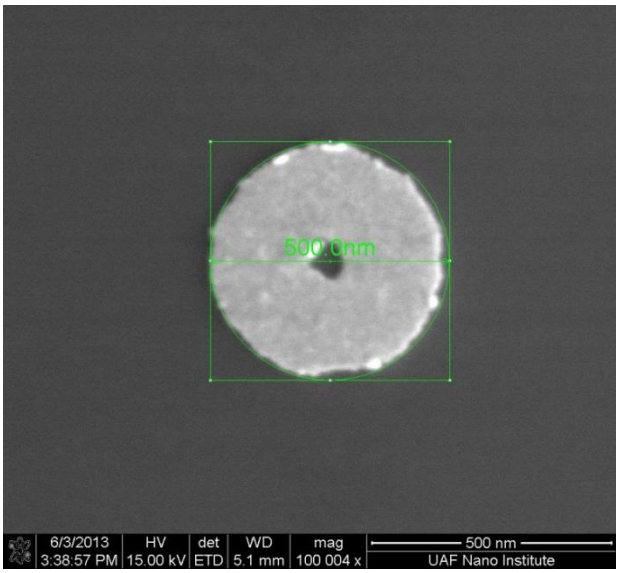

Figure 3.36 (a) Zoom in SEM picture of ring structure, outer diameter 500nm (Thach Pham, June 2013, University of Arkansas)

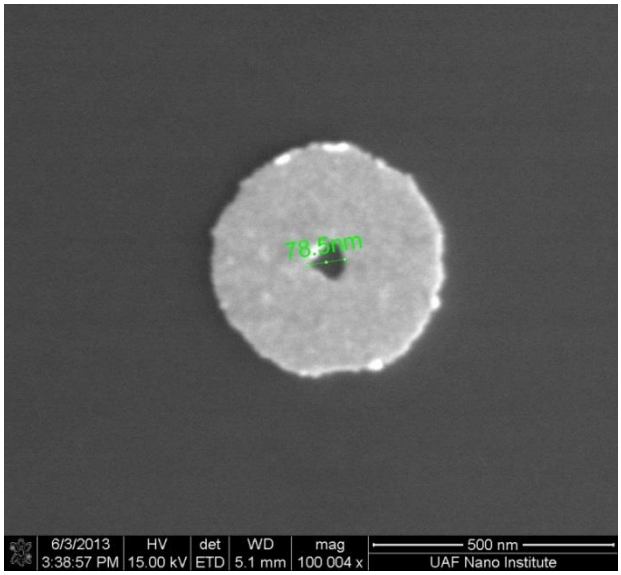

Figure 3.36 (b) Zoom in SEM picture of ring structure, inner diameter 78nm (Thach Pham, June 2013, University of Arkansas)

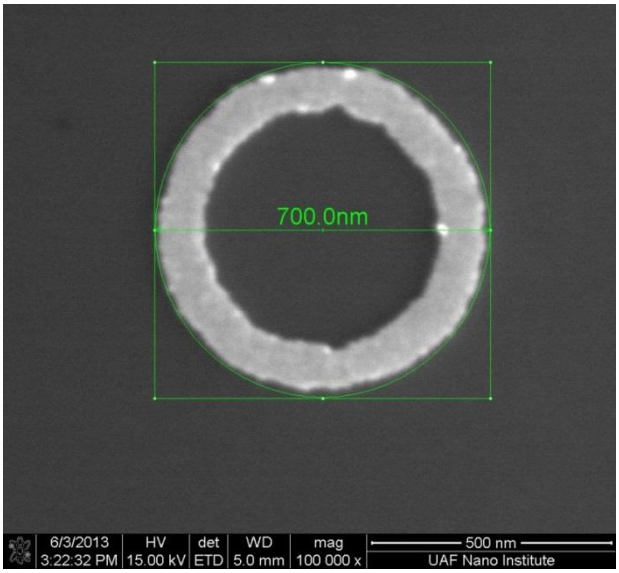

Figure 3.37 (a) Zoom in SEM picture of ring structure, outer diameter 700nm (Thach Pham, June 2013, University of Arkansas)

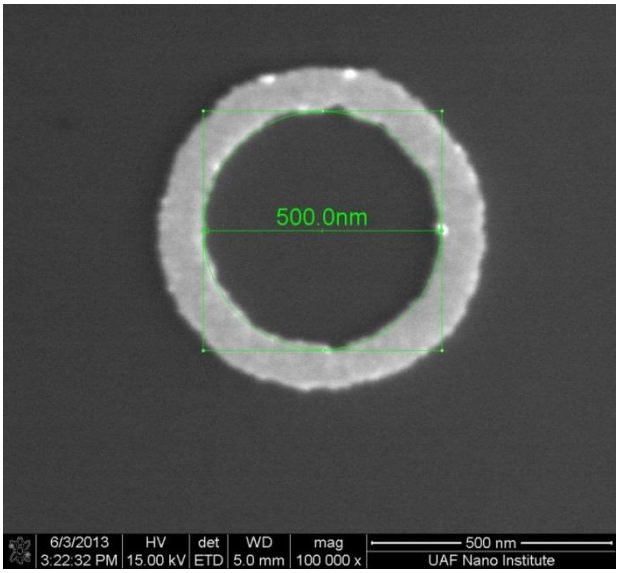

Figure 3.37 (b) Zoom in SEM picture of ring structure, inner diameter 500nm (Thach Pham, June 2013, University of Arkansas)

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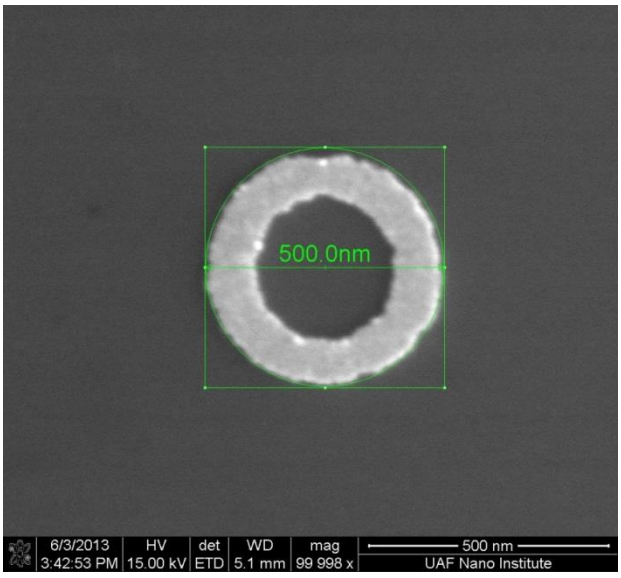

Figure 3.38 (a) Zoom in SEM picture of ring structure, outer diameter 500nm (Thach Pham, June 2013, University of Arkansas)

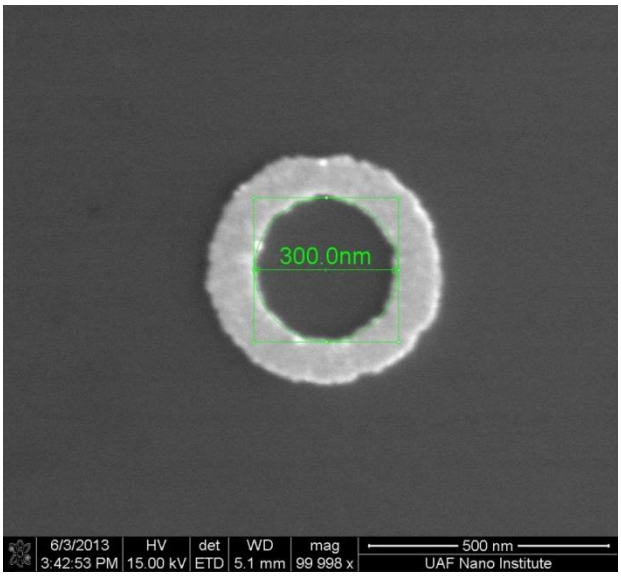

Figure 3.38 (b) Zoom in SEM picture of ring structure, inner diameter 300nm (Thach Pham, June 2013, University of Arkansas)

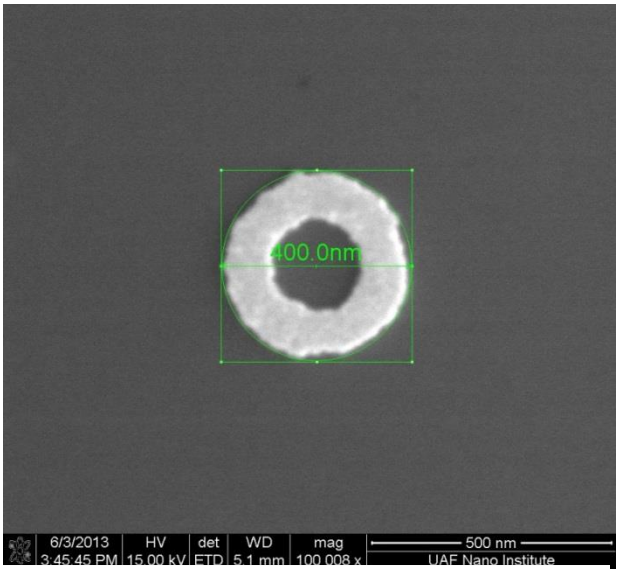

Figure 3.39 (a) Zoom in SEM picture of ring structure, outer diameter 400nm (Thach Pham, June 2013, University of Arkansas)

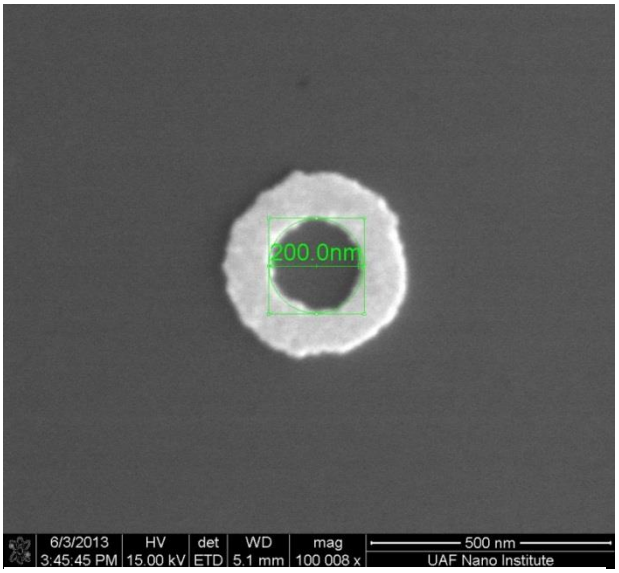

Figure 3.39 (b) Zoom in SEM picture of ring structure, inner diameter 200nm (Thach Pham, June 2013, University of Arkansas)

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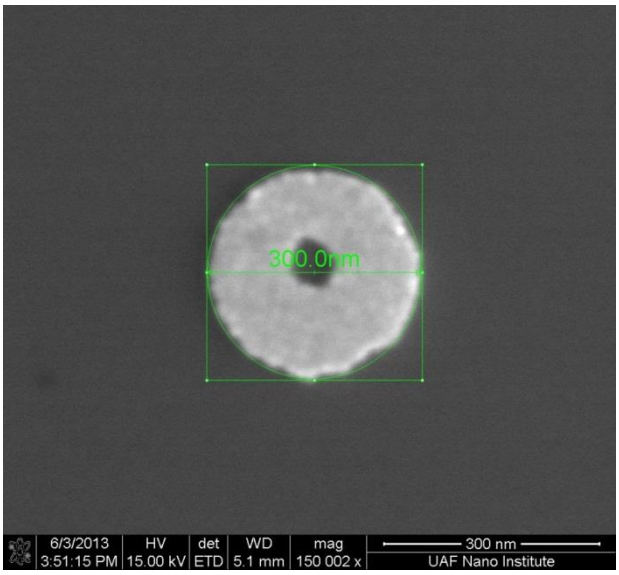

Figure 3.40 (a) Zoom in SEM picture of ring structure, outer diameter 300nm (Thach Pham, June 2013, University of Arkansas)

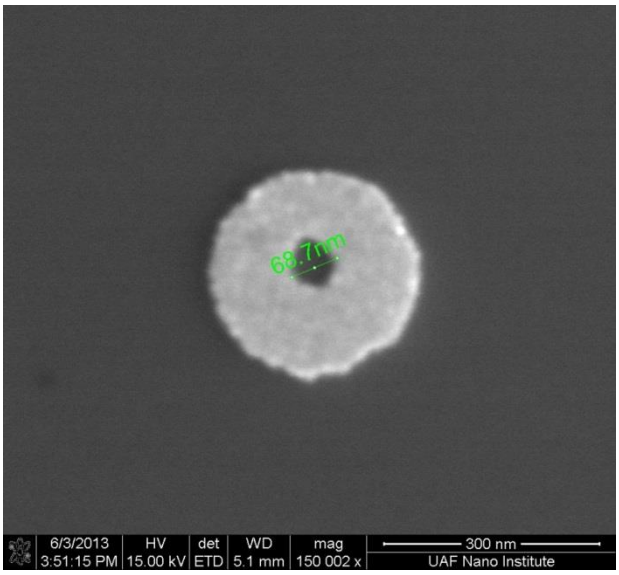

Figure 3.40 (b) Zoom in SEM picture of ring structure, inner diameter 69nm (Thach Pham, June 2013, University of Arkansas)

In future, switching EOS mode of EBL system to higher mode will break down current achievement of lines, rings, and cirles' critical dimension listed above. In addition, fabrication process of those metallic nanostructures could be implanted on devices and be transferred to glass substrate instead of c-Si substrate for optical measurement purposes.

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CHAPTER 4: FABRICATION AND CHARACTERIZATION OF HORIZONTAL SINGLE Si NANOWIRES DEVICE

4.1 Introduction

Although fabrication of single nanowire devices is not a new concept in academic researches, it still has significant impact on the study of single nanowire characteristics. Electron beam lithography (EBL) is especially integrated into the photolithography process in order to provide control over the connections position and geometric structure. In addition, horizontal single nanowire devices offer a solid platform where further electrical studies on various types of nanowires could be conducted.

The fabrication goal is to create metallic bridges connecting a single nanowire (Si) with global electrodes where external devices are used to conduct electrical measurement, as shown in figure 4.1. Global electrodes are patterned using photolithography while metallic bridges are written by electron beam lithography.

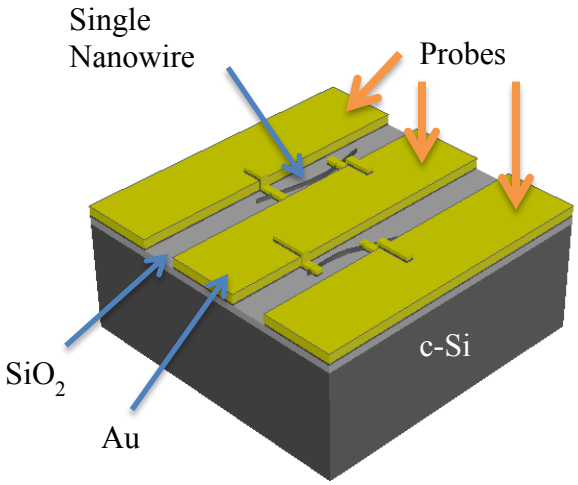

Figure 4.1 3D module of single horizontal nanowires device (Thach Pham, July 2013)

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4.2 Fabrication process of horizontal single Si nanowires device

The fabrication process of a horizontal single Si nanowire device goes through similar processing steps as the one of metallic nanostructures such as traveler preparation, platform preparation, EBL writing, metal deposition, lift off, and SEM pictures, as shown in figure 4.2. However, for this specific type of device which requires photolithography and e-beam lithography techniques, advanced processes (e.g. mask design, nanowires deposition & location, bridge design, and EBL alignment) have been added to have a precise control on the metal bridge connecting single nanowire with global electrodes.

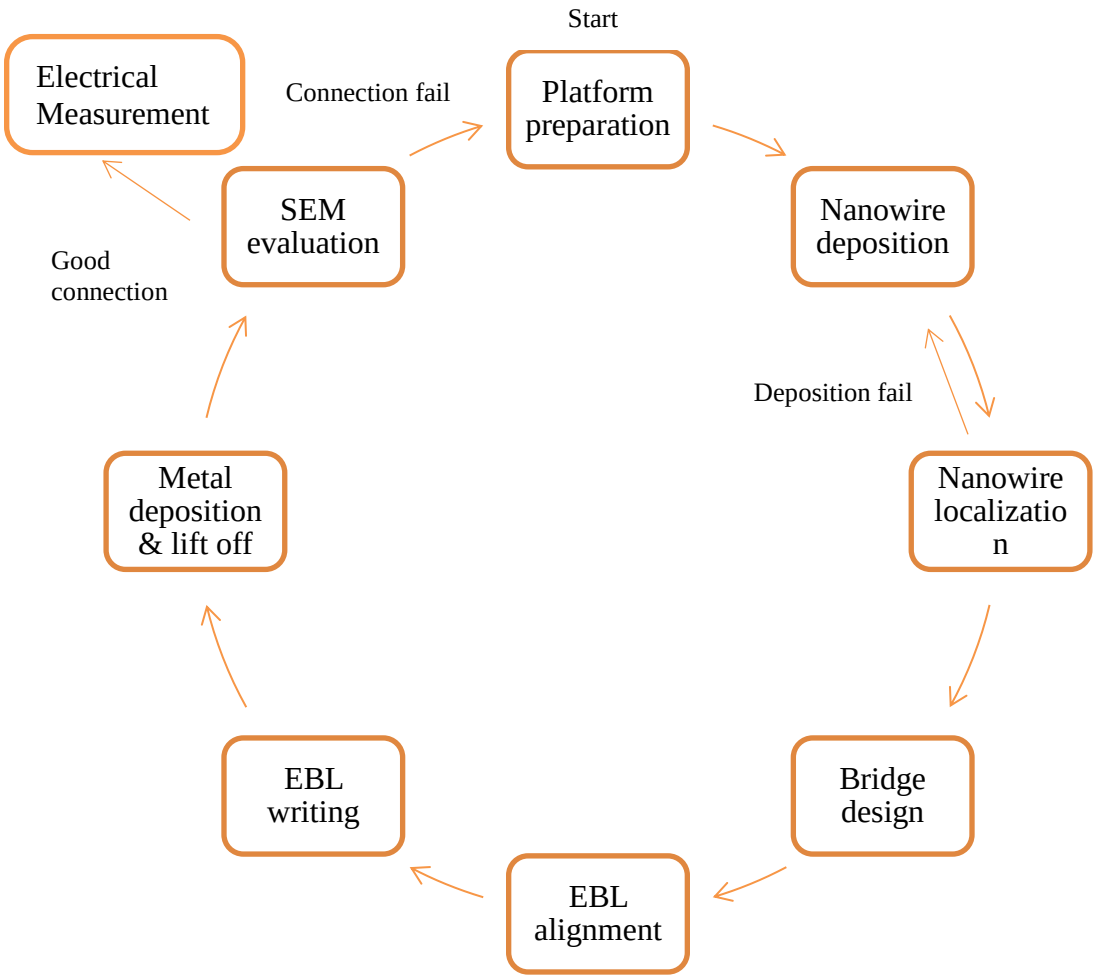

Figure 4.2 Flow of main fabrication processes (Thach Pham, July 2013)

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Table 4.1 shows a list of equipment used in fabrication process of horizontal single Si nanowire device and spending time for each process.

Table 4.1 Fabrication tools and machines

Process	Related equipment & tools	Time cost
Traveler preparation	• Microsoft office	
Mask design	• Auto CAD 2012	
Platform preparation	• Solvent bench • Spinner • Hot plate • Mask aligner Kark Suss MJB3 • Thermal evaporator AUTO 306T • Ultrasonic path • Microscope	1 day / 4 samples
Nanowire deposition	• Pipet • Microscope	2-3 hours / sample
Nanowire location	• FEI NOVA 200	2-3 hours/ sample
Bridge design	• Auto CAD 2012 • LinkCAD 7	1 day / sample
EBL alignment	• EBL system JEOL 5500ZD	4 hours / sample
EBL writing	• EBL system JEOL 5500ZD	2-3 hours / sample

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	• Develop bench • Microscope	
Metal deposition	• Thermal evaporator AUTO 306T	3-4 hours / multiple samples
Lift off	• Wet bench • Ultra sonic bath • Microscope	2 days
SEM pictures	• FEI NOVA 200	2 hours / sample

In brief, it will take 7 working days to fabricate one device assuming that nanowires alignment and EBL alignment are perfectly performed. In reality, the EBL alignment will take a large amount of time since it varies for each substrate.

4.2.1 Processing flow

Horizontal single Si nanowire structure:

- Substrate: SiO_2 coated c-Si piece sample
- Platform: 10nm Cr, 200nm Au
- Nanowire: Si
- Bridge: 5cm Cr, 50 nm Au

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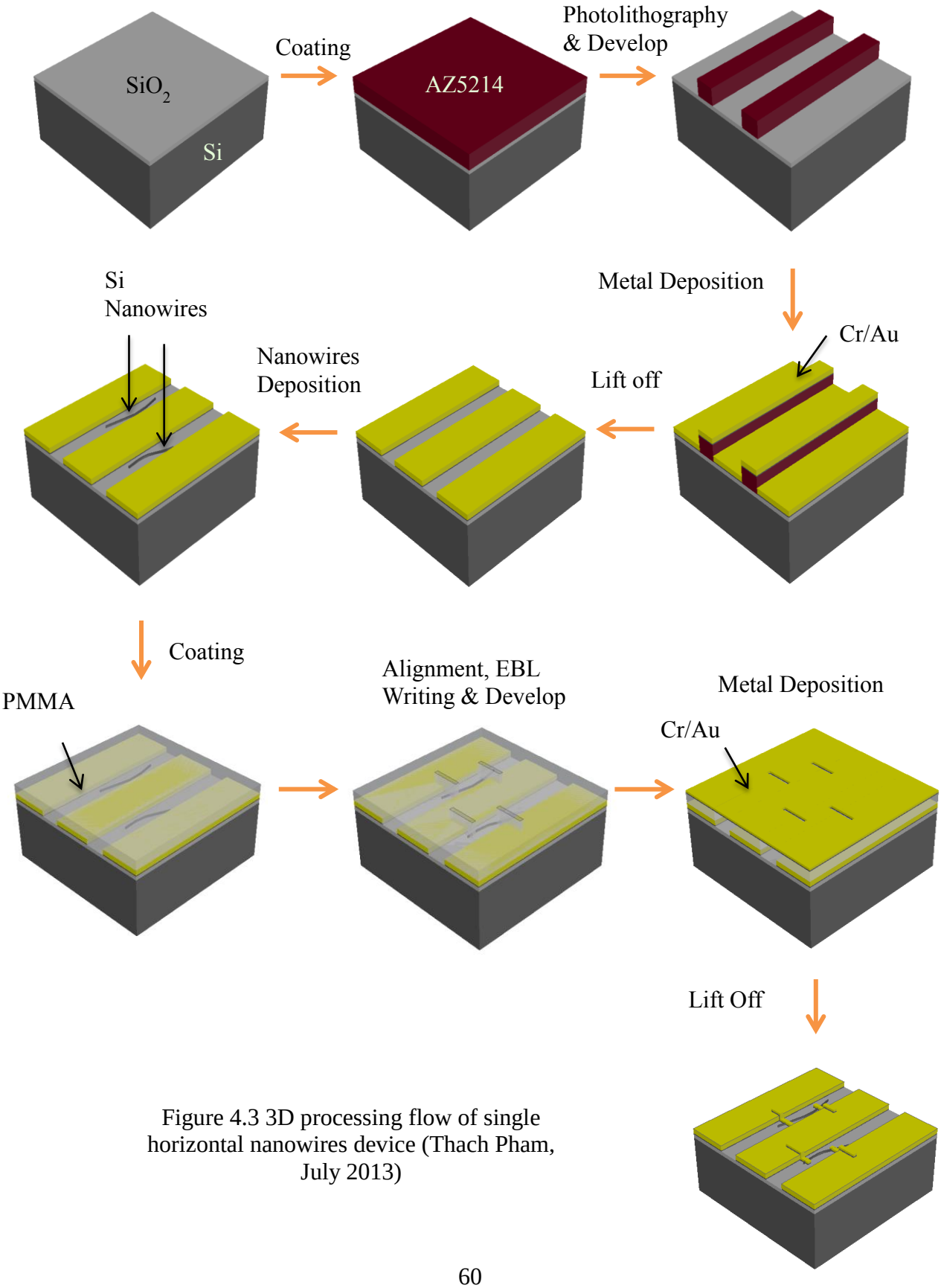

Figure 4.3 3D processing flow of single horizontal nanowires device (Thach Pham, July 2013)

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4.2.2 Mask design

From the beginning, in order to conduct electrical measurement of a single nanowire, a photo mask has been used to form a special platform where metallic global electrodes are systematically distributed. However, the first mask contains several elements preventing the nanowires deposition process, nanowires localization process, as well as electrical characterization. As shown in figure 4.4, the distance between the horizontal global electrodes located on both the left and right sides is too dense for multiple single nanowires to be placed. The current gap between small electrodes is 10um while the one between a small electrode and big electrode is 15um. Consequently, the probability of having four connections forming form a single nanowire to global electrodes is very small. It also limits the user's freedom in designing metal bridges. In addition, the areas that has similar square shape have insufficient dimensions for a good connection to be made with metal pin. The smallest square is approximately 80x80um while the largest one is approximately 100x100um. Because of listed parameters, pin adjustment under a microscope will damage the metal surface of the platform and peel off the metal layer after one or two attempts.

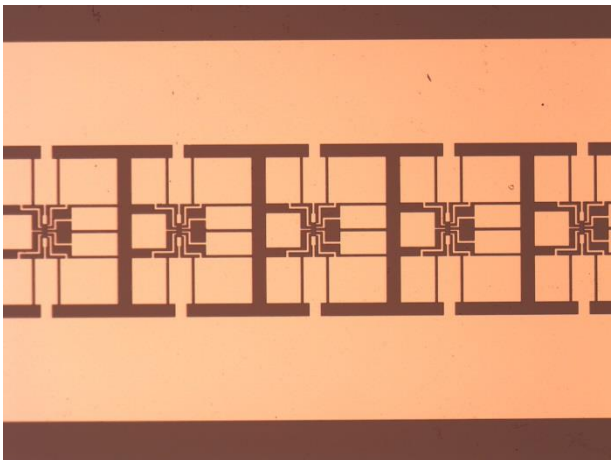

Figure 4.4 (a) An array of metalized platform (Thach Pham, January 2013, University of Arkansas)

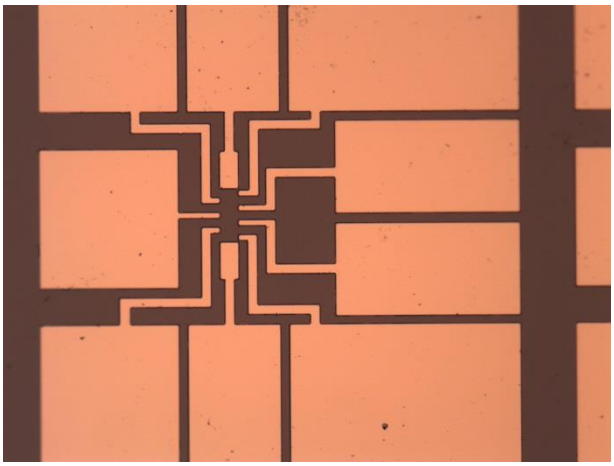

Figure 4.4 (b) Single metalized platform (Thach Pham, January 2013, University of Arkansas)

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Based on experiences obtained from fabrication processes using 1st mask, 2nd mask composing 2 designs for single nanowire device and 2 designs of other device has been designed using Auto CAD 2012. Final product, 4”x4”x0.09” mask chrome coated quartz with minimum feature size of 3um, is delivered by HTA photo mask company in January 2013.

(a) First design

First design is composed of 4x3 blocks covering one fourth area of the mask. Each block, designed for specific 1cmx1cm sample piece, is divided into arrays of 3x4 platforms. As shown in figure 4.5a, four global PQ marks, composed of only cross marks (3umx300um), are placed at four corners to define the boundary of main features and play an important role in alignment testing. The main platform covering an area of 700umx700um is bounded by 4 local PQ marks or chip marks which enhance alignment accuracy, as shown in figure 4.5b. However, due to a lack of deep understanding on chip mark alignment by the JEOL 5500ZD, this function is not applicable for this fabrication process. Details about alignment will be discussed later.

Compared with the first platform design, all metal blocks parameters are carefully extended in such way that facilitate measurement probes’ placement. By increasing the block area with the smallest size of 125umx200um and largest size of 200umx200um, measurement probes are allowed to scratch metal surface several times before the placement is optimized. The distance between small global electrodes is increased to 15um instead of 10um while the one between the small electrode and large electrode is extended from 15um to 20um and 20-25um to 40um. Another improvement is the numeration of platform so user has control on documentation and evaluation under SEM.

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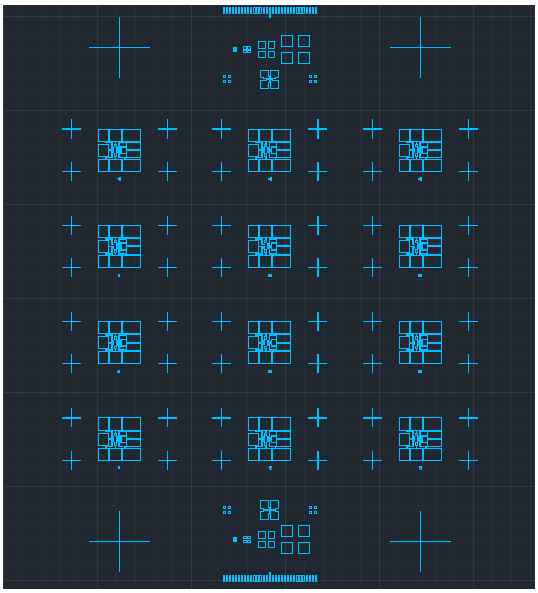

Figure 4.5 (a) CAD file of 1st design (Thach Pham, December 2012, University of Arkansas)

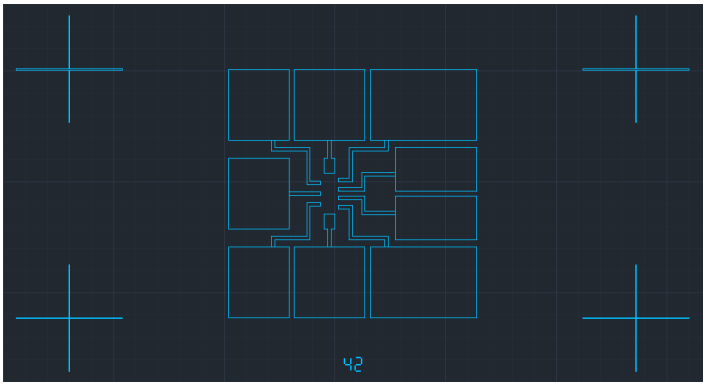

Figure 4.5 (b) Zoom in of single platform in CAD (Thach Pham, December 2012, University of Arkansas)

(b) Second design

Second design is composed of 4x3 blocks covering one fourth area of the mask. Also served for photolithography purpose on 1cmx1cm sample piece, each block in figure 4.6a is formed from 3x3 arrays of platforms. In general, the 2nd design resembles the 1st design in the way it is structured which is platform numeration, PQ marks position and its purpose. One difference which stands out is the area of platform which is approximately 950umx1250um. If the 1st design aims to place all single nanowires around the center of platform which simplify bridge design, the 2nd design is an open space for single nanowire to be placed. Since the deposition of a single nanowire could not be handled with a certain level of accuracy and reliability, 2nd design allows a single nanowire to flow anywhere on four corners and along the center of its platform, as shown in figure 4.6b. With a minimum distance of 30um between electrodes, 2nd design enables the “freedom” space for bridge design and also assures four connections from a single nanowire

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to global electrodes if that single nanowire has good quality. In addition, the area of metal blocks ranges from 165umx125um to 250umx200um.

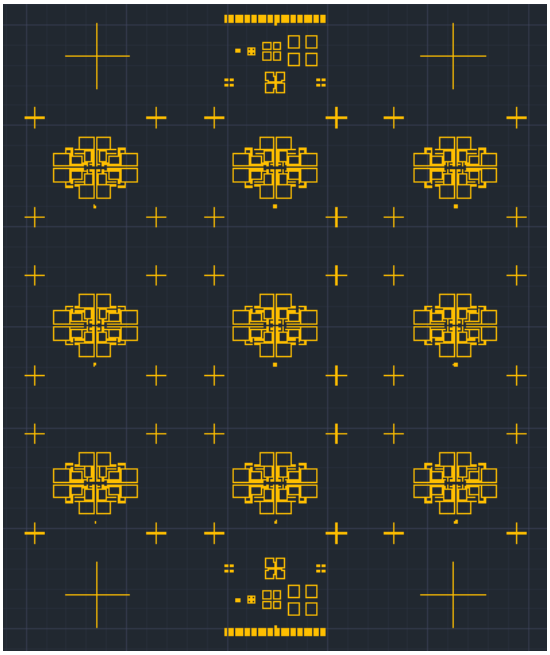

Figure 4.6 (a) CAD file of 2nd design (Thach Pham, December 2012, University of Arkansas)

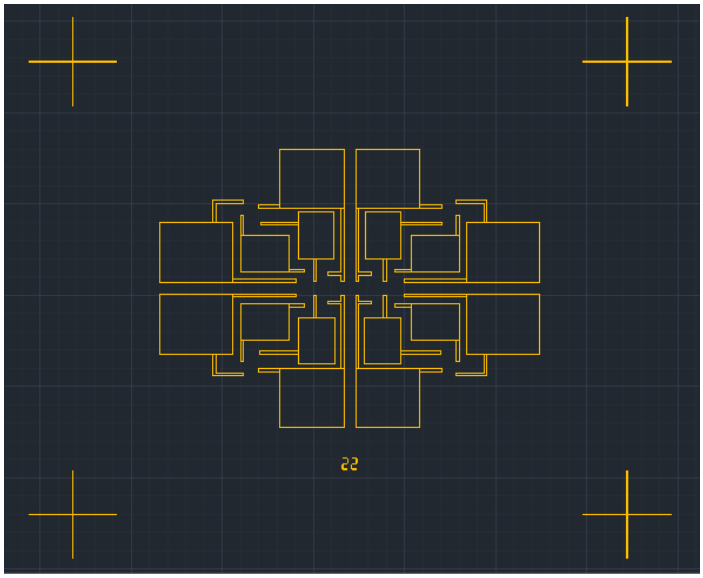

Figure 4.6 (b) Zoom in of single platform in CAD (Thach Pham, December 2012, University of Arkansas)

4.2.3 Platform preparation

In addition to the cleaning process of piece sample, this section will include the photolithography technique and metallization process to complete the platform preparation process. At least four samples are fabricated at the same time. Mask cleaning will also be discussed since a dirty photo mask could disrupt the entire fabrication process.

(a) Sample cleaning

- Clean SiO_2 coated Si piece sample using acetone, methanol, and isopropyl alcohol (IPA) respectively and followed by DI water cleaning. Do not let the surface of sample dry out.
- Dry sample using N_2 gun.

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- Dehydrate sample at 90^{o} C for 5 minutes and let it cool down.
- Check with microscope.

(b) Photolithography – image reverse process

As presented in chapter 2, a negative photo resist (AZ 5214E) is required for the image reverse process.

- Cover the spinning plate with blue tape to protect back side of testing sample and vacuum chuck
- Spin coat AZ 5214E at 3000 rpm using recipe 30. Resist thickness is approximately 2um
- Soft bake coated sample at 95^{o}C for 1 minutes and let it cool down
- Expose the sample using photo mask "Metal a-Si nanowire",
- Bake exposed sample at 105^{o}C for 2 minutes and 30 seconds and let it cool down
- Flood expose the sample again (without mask)
- Develop the sample in AZ MIF 300 developer for 70 seconds
- Rinse with DI waters for 30 seconds and dry out using N_2
- Evaluate pattern under microscope

Listed above is the basic recipe for the image reverse process. However, parameters such as exposure time for 1^{st} and 2^{nd} exposure and develop time are tweaked every time the process is repeated since they depend on many elements such as light intensity and resist thickness. The method commonly used to improve image reverse recipe is to keep develop time constant while changing exposure time and vice versa. Proposal develop time is 45 seconds.

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Exposure time calculation:

$$t = \frac{energy}{light\ intensity} = \frac{resist\ thickness * constant}{light\ intensity}$$

For 1st exposure, initial constant value is 25.6.

For 2nd exposure, initial constant value is 67.7.

Light intensity could be obtained from a log sheet. The constant value changes upon developer. Figure 4.7a and 4.7b show successful photolithography process using new photo mask.

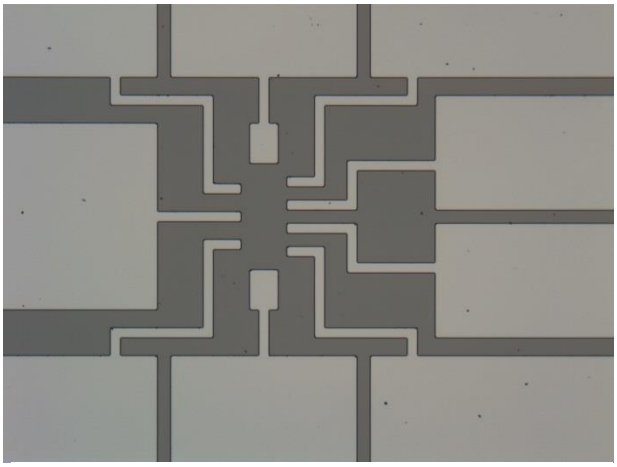

Figure 4.7 (a) 1st design structure after develop, (Thach Pham, January 2013, University of Arkansas)

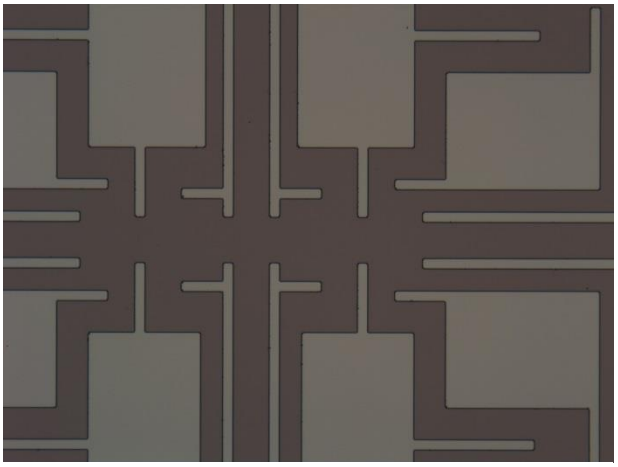

Figure 4.7 (b) 2nd design structure after develop (Thach Pham, January 2013, University of Arkansas)

(c) Metal deposition & lift off

Metal deposition:

- Load one/multiple sample on sample holder disc with kapton tape
- Place/replace Cr rod and fill new Au pallets on boat
- Pump down chamber for 2-3 hours until it reaches approximately 8E-6 mTorr

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- Start depositing metal at rate of 1-2 A/s to obtain 10nm Cr and 200 nm Au

Lift off

- Prepare beaker/beakers containing remover PG, a dedicated solvent stripper for PMMA
- Heat up to 70^{o}C
- Place one sample for each beaker
- Wait 30 minutes
- Bubble sample surface in order to remove most of unnecessary metalized parts.
- Replace new solvent, cover beakers and monitor samples for a least 2 days. Fill up solvent again if it evaporates.
- Bubble sample surface and leave beakers in ultrasonic bath for 5 minutes
- Rinse samples with IPA to stop the reaction of remover PG
- Rinse samples with DI water and dry out using N_2 gun
- Examine sample under microscope

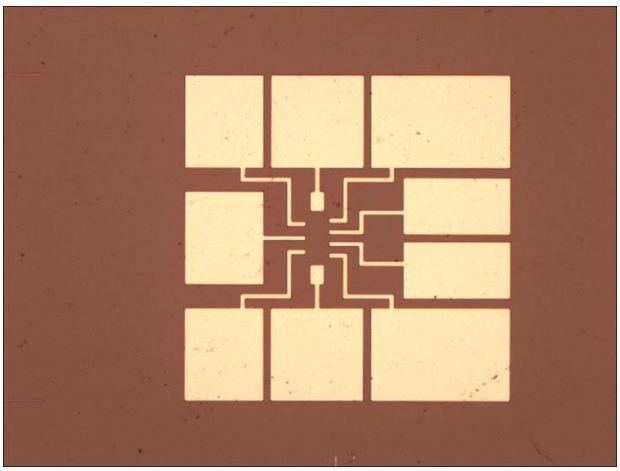

Figure 4.8 (a) 1st design structure after lift off (Thach Pham, January 2013, University of Arkansas)

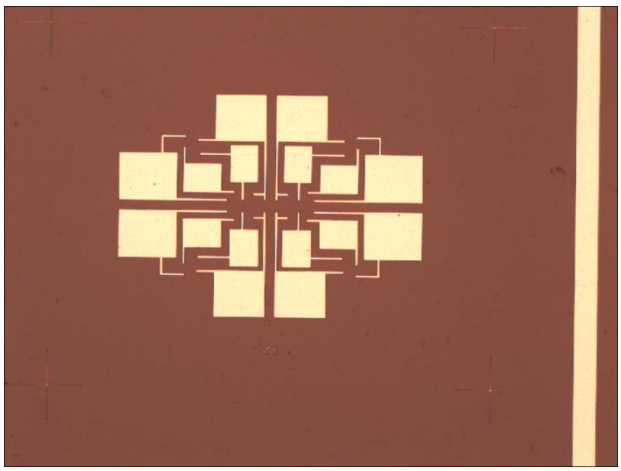

Figure 4.8 (b) 2nd design structure after lift off (Thach Pham, January 2013, University of Arkansas)

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(d) Mask cleaning

Keeping the mask clean after each sample's exposure by photolithography is an important step to preserve the photo mask so that it could be used multiple times with the same quality. This step is usually ignored by user and causes serious problems such as deformation in features size at specific locations. User will lose control not only on the develop recipe but also on further processes which requires accurate and stable features size.

During the fabrication process of horizontal single nanowire, the 2^{nd} photo mask is affected by photoresist residue and causes uniformity of exposed patterns, as shown in figure 4.9a. Several tries to clean the photo mask using available remover , such as acetone, PRS 1000 remover and PG remover, have been attempted but none of them have succeed.

The last attempt to clean the mask using photoresist asher LFE Asher APE110 is a success, as shown in figure 4.9b. Normally, this tool is configured with oxygen to remove patterned photoresist on silicon wafers. However, this method leaves a question on etching effect on photo mask if it is heavily used. Further study should be made to make sure this method is stable and does not damage the photo mask.

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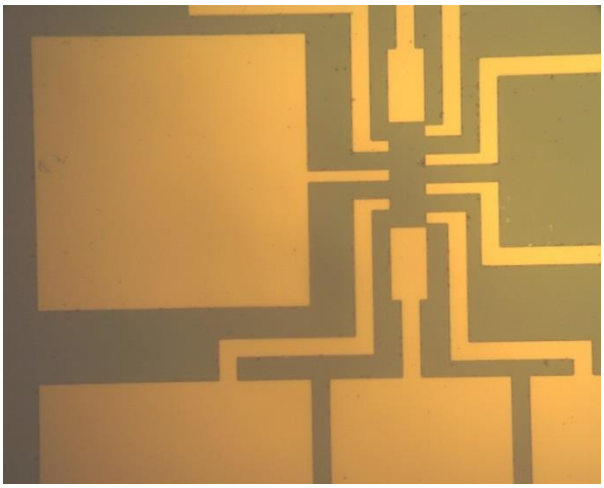

Figure 4.9 (a) Mask before cleaning (Thach Pham, January 2013, University of Arkansas)

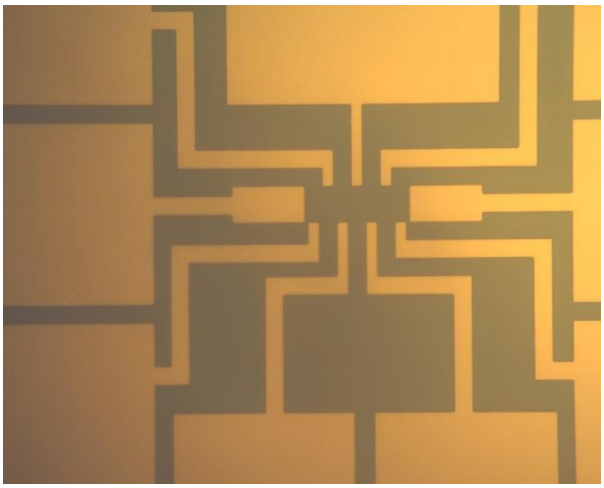

Figure 4.9 (b) Mask after cleaning (Thach Pham, January 2013, University of Arkansas)

4.2.4 Nanowires deposition & localization

(a) Nanowires deposition

After the metallic platform is formed on top of SiO_2 coated c-Si piece sample, Si nanowires will be deposited. The single Si nanowire, which is growth using plasma enhanced chemical vapor deposition method by Matthew Young, is a composite of amorphous Si and crystalline Si. The a-Si layer is the shell while the c-Si layer is the core. The nanowire diameter is approximately 400nm. At the moment there is no reliable control on the position where nanowires are dropped.

- Clean and dry the tube which is used to store nanowires solution
- Fill the tube with 1ml of DI water
- Tilt the nanowires sample and scratch its surface so that most of nanowires fall into the tube
- Use VWR dancer to mix nanowires solution for 10 minutes
- Use pipet to transfer one drop of nanowires solution on the center of platform

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- Place testing sample on hot plate of 90^{o}C for 10-20 seconds
- Cool down the testing sample
- Examine the distribution of nanowires under microscope
- If nanowires are too dense, add an appropriate amount of DI water into the tube. Repeat the whole process to reevaluate the density of the solution
- Repeat the transfer process until several single nanowires are well distributed on each platform

How to define good nanowires position:

Good position is defined as an area having enough space for four metallic bridges to connect from a single nanowire to global electrodes. Evaluating nanowires positions also depends on what type of platform design being used. 1st platform design requires good single nanowires to be placed near the center of the platform where connection to global electrodes are feasible. On the other hand, 2nd platform design allows nanowires to spread out all at four corner of platform and along the center of the platform. Figure 4.10a and 4.10b show potential nanowires positions that could be used for four probes connections (orange circles) and 2 probes connections (blue circles).

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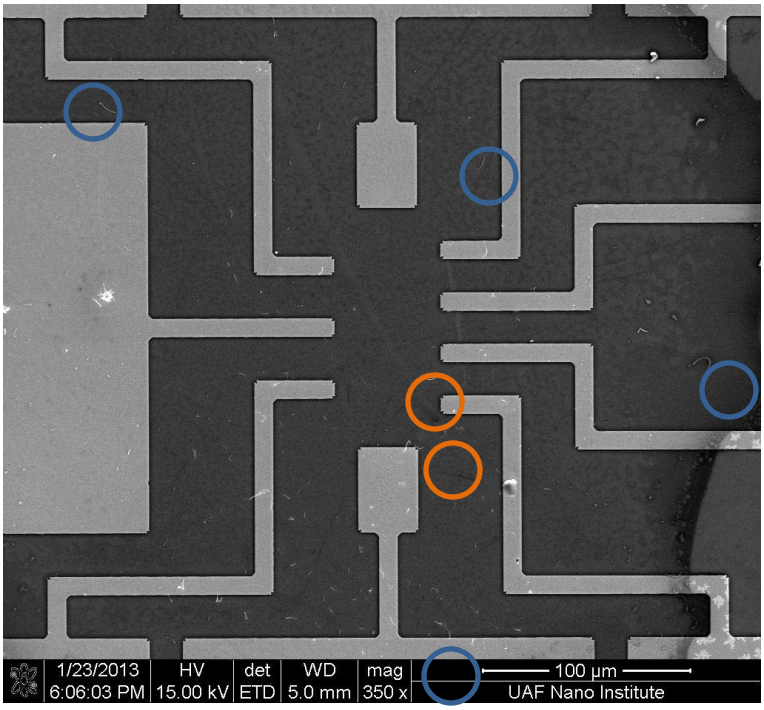

Figure 4.10 (a) Good nanowires position on 1st design platform (Thach Pham, January 2013, University of Arkansas)

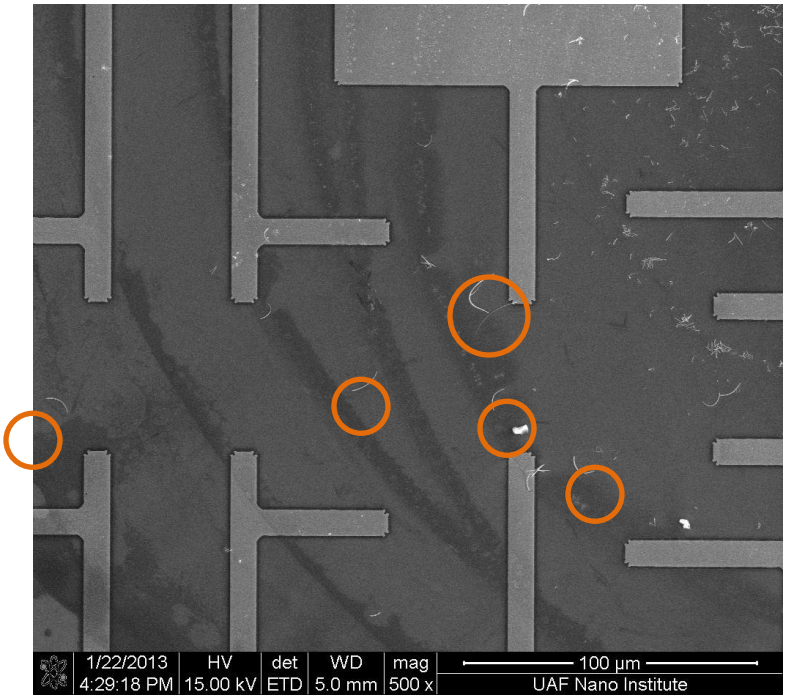

Figure 4.10 (b) Good nanowires position on 2nd design platform (Thach Pham, January 2013, University of Arkansas)

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(b) Nanowires localization

The ultimate goal of nanowires localization is to record nanowires position after the deposition process. The more accurate it is, the simpler bridge design and alignment process using EBL JEOL 5500ZD is. Thus, in order to archive this goal, scanning electron microscopy (SEM) FEI NOVA 200 is extensively used. Each single nanowire will be located and recorded at a different level of magnification so that its position could be easily recognized by user. High quality pictures are imported to Auto CAD 2012 for bridge design.

4.2.5 Bridge design

Since metallic bridges are patterned based on nanowires position which deviates from case to case, EBL is preferred over photolithography. Thus, it requires a digital mask which collects patterns parameters and its mapping related to each single nanowire. Auto CAD 2012 is once again a useful tool to design "random" bridges by integrating high quality SEM pictures of single nanowires with platform design built inside Auto CAD (mask design).

- Load mask design "Metal a-Si Nanowire"
- Delete all patterns except for mask design 1. If user is working with mask design 2, delete all patterns except for mask design 2.
- Delete all patterns of mask design 1 except 1^{st} block of platform which is the one closest to the origin 0. There are in total 12 platforms for 1^{st} design and 9 platforms for 2^{nd} design.
- Import SEM picture of single nanowire. Auto CAD will ask for scaling factor since SEM picture and platform design are scaled differently. Scaling factor deviates from case to case. It is important to have SEM pictures of single

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nanowires taken at the same magnification level so that scaling factor‘s calibration is simplified.

- Use scaling factor 128.7 in the case of 1000x magnification. Scaling factor is found by minimizing the gap between the upper bound and lower bound until a value satisfies the equation. Since electrodes dimensions patterned by photolithography are known (mask design), they could be used to compare with those after initial scaling. First pick any reasonable value such as 100 and compare that dimension with the real one. If the testing dimension is larger, reduce input value and vice versa. Repeat until the tolerance between testing dimension value and truth value is minimized.
- Continue to import SEM picture of good positioned nanowires
- Use polyline to design bridges as shown in figure 4.11. Golden rule is that all blocks must be closed polygons.
- Bridge width is 500nm. The distance between each bridge should be kept consistent within nanowire. It varies from 1um to 3um.

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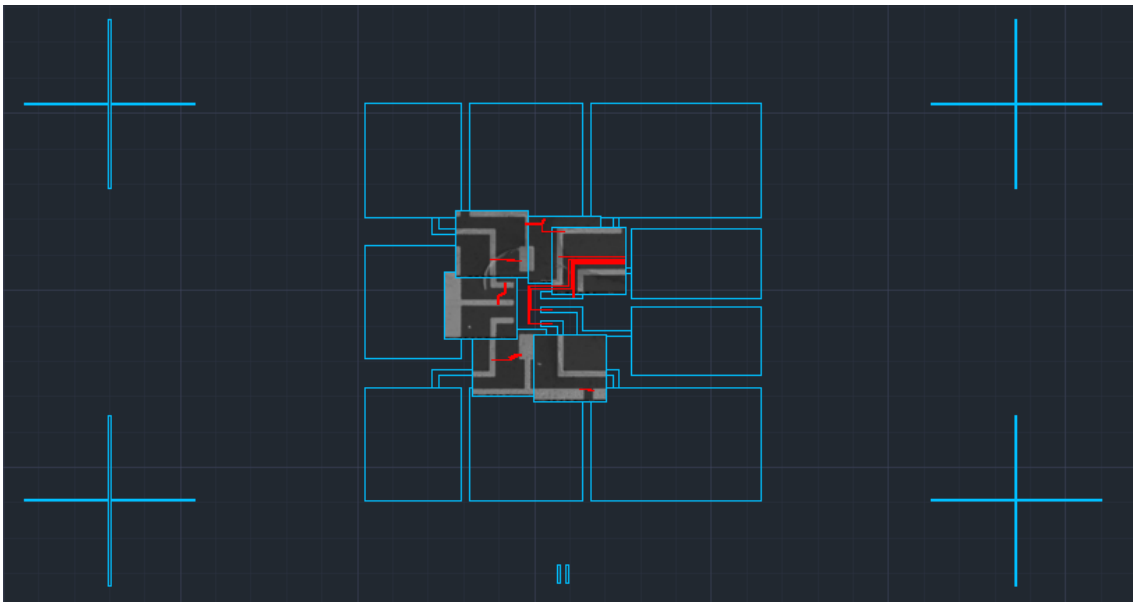

Figure 4.11 (a) Bridge design in CAD platform (Thach Pham, February 2013, University of Arkansas)

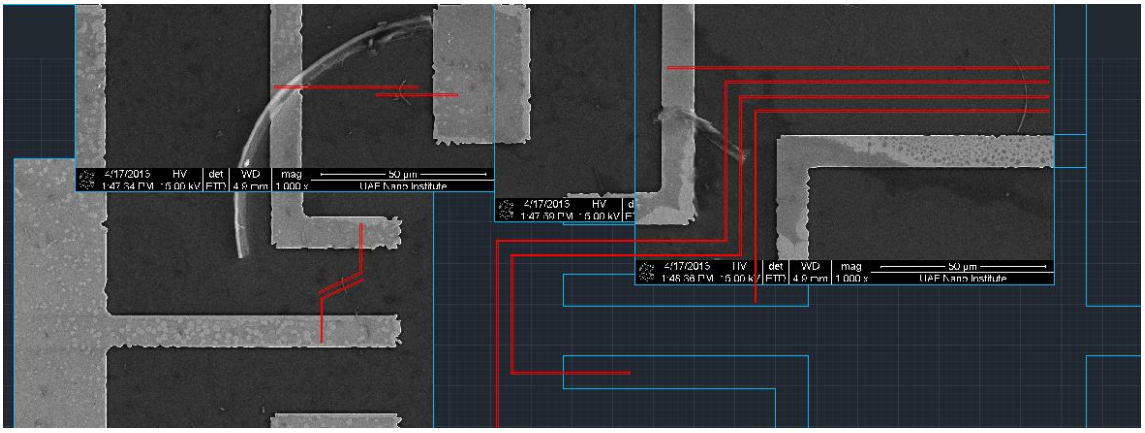

Figure 4.11 (b) Zoom in bridge design in CAD (Thach Pham, February 2013, University of Arkansas)

- Save bridge design file with another name.
- Delete all imported SEM pictures.
- Draw four rectangles 700umx3um (one at top, one at bottom, one at left, and one at right) to define the boundary of main patterns. The outer edge of each rectangle

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has the same coordination with the chip mark on the same side as shown in figure 4.12.

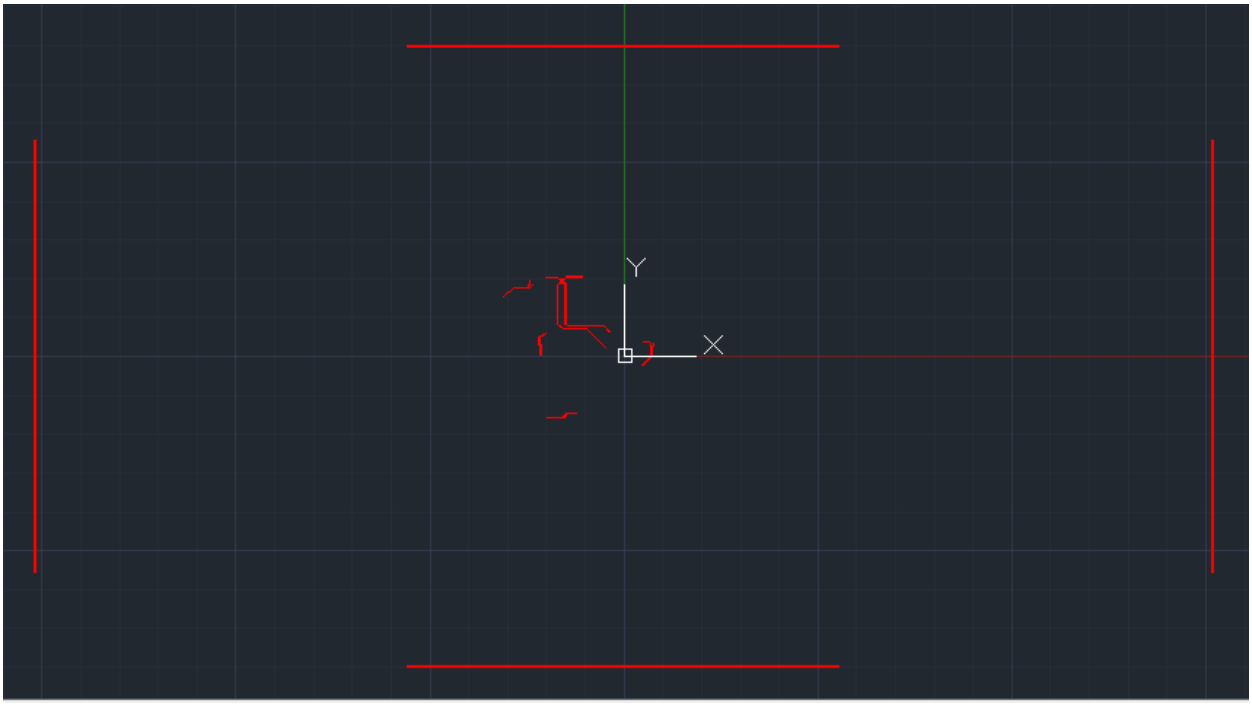

Figure 4.12 Final plot of bridge design (Thach Pham, February 2013, University of Arkansas)

- Keep one platform at a time and delete all others platform patterns. The only patterns left are four rectangles and a system of bridges as shown in figure 4.12. In the end, twelve bridge design files and nine bridge design files are generated from mask design 1 and mask design 2.
- Save *.dwg file as *.dxf and go through conversion process stated in chapter 3.

4.2.6 EBL alignment & writing

Although chapter 3 presents basic principles to successfully write patterns using EBL, it is insufficient to fabricate horizontal single nanowire devices because metallic bridges connecting single nanowire with global electrodes are placed randomly according to nanowires

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position on the platform. In order to transfer the designed patterned to a desired location, alignment with a high level of accuracy between bridges and platform is needed. This section will mainly discuss alignment technique in EBL JEOL 5500ZD system.

(a) EBL alignment

EBL alignment or photolithography alignment is just the rearrangement of two consecutive layers so that features on later layer are placed at defined position on 1st layer. However, EBL alignment is more flexible than photolithography since it does not require any photo mask, rather it employs an editable digital layout.

The EBL alignment process starts with a control sample (1cmx1cm piece) patterned with metallic platform of either mask design 1 or mask design 2. There is not a photoresist coated on control sample.

- Load control sample inside EBL system and pump down until VG2 reaches 1E-5 Pa
- Choose working condition of EBL system. Working condition must be consistent during alignment and exposure.
    - EOS mode 2
    - Aperture 2
    - 4th lens
    - Accelerating voltage 50kV
    - Current -1nA
- Adjust lens focus and astigmatism

`

- From the calibration table, choose Registration (RG) mark detection tab. Choose global mark detection settings.
- Fill or select the following options for the first time of each calibration:
    - Measurement mode : semi auto
    - Material size: 2
    - P point mark position: x, y = 0
    - Q point mark position: any number except 0
    - Auto update
    - P mark offset position: x, y = 0
- Record the real position of the 2” wafer origin. Name it Xo and Yo
- Open SEM built in EBL system and move to one of four corners of the control sample. Record its value for reference.
- Open SEM and move to one of four global PQ marks. Record the coordinates of its center as accurate as possible. Name it X1 and Y1.
- Open SEM and move to the opposite corner of previous global PQ mark. Record the coordinates of its center as accurate as possible. Name it X2 and Y2. If the quality of that PQ mark is not good, move to one other two PQ marks.
- Open RG mark detection tab and fill the following options
    - P point mark position: x = Xo – X1, y = Yo – Y1. Positive or negative value depends on the relative position of chosen mark with the origin. Top left corner: $x < 0$, $y > 0$; top right corner: $x > 0$, $y > 0$; bottom left corner: $x < 0$, $y < 0$; bottom right corner: $x > 0$, $y < 0$.

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- Q point mark position: x = Xo – X2, y = Yo – Y2. Positive or negative value depends on the relative position of chosen mark with the origin. Top left corner: x < 0, y > 0; top right corner: x > 0, y > 0; bottom left corner: x < 0, y < 0; bottom right corner: x > 0, y < 0.
- P mark offset position: x, y = 0. Keep x, y = 0 for each stage movement.

- On left panel, only select RG mark detection. The green color shows that it is selected. Press "execute calibration" button.
- EBL system will automatically move the stage to a new P and Q where the system will detect P and Q marks. If no error panel pops out and the calibrating graphs shows a good peak, those positions are tested properly. To increase alignment accuracy, always check the P mark offset position. If its coordinates are less than 0.1, input parameters are optimized otherwise modify x and y value of P and Q until the condition is met.
- Unload control sample
- Spin coat with e-beam resist using PMMA 4% 495K, recipe 30 (200nm)
- Bake at 180^{o}C for 2 minutes
- Load control sample inside EBL system and pump down until VG2 reaches 1E-5 Pa
- Apply same working condition as stated above
- Record origin position and compare with measured values. Update the offset to every coordinates of P and Q if there is offset (rarely happen).
- Record selected corner coordinates and calculate the offset
- Open RG mark detection tab and fill the following options

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- P point mark position: x’ = x + |offset|, y’ = y + |offset|. Offset sign depends on the relative position of P mark 1st load and P mark 2nd load.
- Q point mark position: x’ = x + |offset|, y’ = y + |offset|. Offset sign depends on the relative position of P mark 1st load and P mark 2nd load.
- P mark offset position: x, y = 0. Keep x, y = 0 for each stage movement

- On left panel, only select RG mark detection. Green color shows that it is selected. Press “execute calibration” button.
- If no error panel pops out and calibrating graphs shows good peak, those positions are tested properly. Always keep P mark offset position less than 0.1 to have high level of alignment accuracy.

After 1st control sample without coating any e-beam resist is tested, user must have the following critical coordinates recorded:

- Corner of control sample. Each time the control sample is loaded or unloaded, its relative position with the origin changes, so does the relative position of PQ marks. If the coordinates of selected corner of control sample are recorded, the difference between two loading times becomes the curing factor for the offset.
- Origin of 2” layout
- P and Q marks (2 out of 4)

After 2nd test on control sample, user must have P and Q marks coordinates.

(b) EBL writing

Comparing with EBL writing process in metallic nanostructures chapter, EBL writing for horizontal single Si nanowires mainly focuses on map layout so that 2nd layer of patterns are

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matched to selected position on 1st layer patterned by photolithography. Calibration setting is the same as the one in EBL alignment.

- Load testing sample inside EBL system and pump down until VG2 reaches 1E-5 Pa
- Choose working condition of EBL system:
    - EOS mode 2
    - Aperture 2
    - 4th lens
    - Accelerating voltage 50kV
    - Current -1nA
- Adjust lens focus and astigmatism. Execute calibration
- Convert *.dwg files to *.v30. On the process of converting patterns files from *.gdsii to *.v30, the EBL system will provide boundary parameters of specific pattern design which is previous controlled by user in Auto CAD bridge design section.
- Open exposure table and import *.v30 files
- The mismatch position discussed in chapter 3 will not be a problem in this step since the P and Q coordinates are obtained through alignment. This already defines the boundary for the placement of chips.
- Choose exposure dose of 500uC/cm^2 for line and plane dose. This is a reasonable exposure dose for features size greater than 500nm.
- Select global mark box and fill in with P and Q coordinates measured in alignment step. Size: length = 150 um and width = 3um

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- P and Q marks position will appear on the layout.
- Select the chip corresponding to its platform (defined in bridge design) and place around that area.
- Further calculation is needed to match bridges pattern chip with platform. From pattern design in Auto CAD 2012, the distance between global P or Q mark to the center of the box that bounds bridges design inside is known. The real coordinates of pattern file is equal to the sum of P or Q mark coordinates and the distance obtained from Auto CAD 2012.
- Right click on selected chip and edit its coordination.
- Repeat the process until all chips are correctly placed on the layout.
- Edit job property:
    - Scan step 1
    - Calibration condition file must match with user's calibration file
    - Cycle: each chip
    - Calibration mode: deflection
- Save layout file
- Select exposure
- When exposure is done, record writing time and stop beam current.
- Move the stage back to its original position before unload sample.
- Develop sample in MIBK:IPA 1:3 for 60s.
- Rinse carefully in IPA for another 15s before dry out by N_2. Nanowires could be removed easily if sample is not handled with care.
- Check the existence of nanowires as well as exposed patterns.

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4.2.7 Metal deposition & lift off

The metal deposition and lift off processes on an exposed patterns sample should be taken with extremely care since nanowires could be removed easily by strong physical interactions. This implies that remover PG needed to be replaced and ultrasonic bath is removed.

(a) Metal depostion

- Load one/multiple sample on sample holder disc with kapton tape
- Place/replace Cr rod and fill new Au pallets on boat
- Pump down chamber for 2-3 hours until it reaches approximately 8E-6 mTorr
- Start depositing metal at rate of 1-2 A/s to obtain 2nm Cr and 50 nm Au

(b) Lift off

- Prepare beaker containing acetone
- Place sample inside beaker
- Wait 30 minutes
- Lightly bubble sample surface in order to remove most of unnecessary metalized parts.
- Replace new solvent, cover beakers and monitor samples for a least 2 days. Fill up solvent again if it evaporates.
- Bubble sample surface.
- Rinse samples with IPA and let sample dry out naturally.
- Examine sample under microscope.

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4.3 SEM pictures of single horizontal Si nanowires device

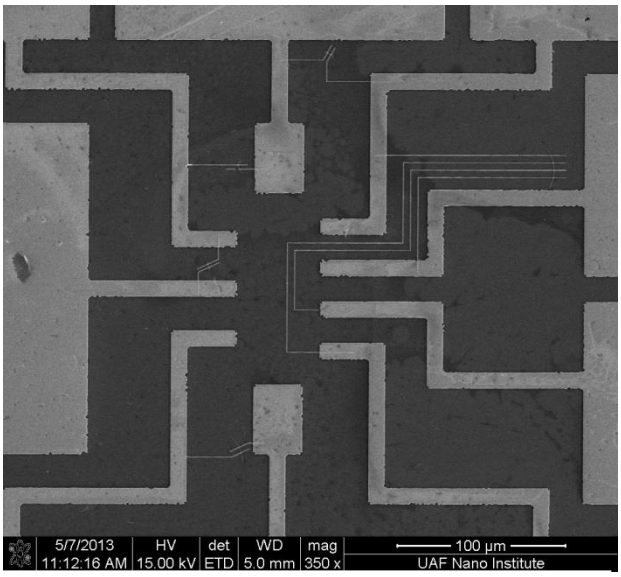

Figure 4.13 Map layout of platform 11 (Thach Pham, May 2013, University of Arkansas)

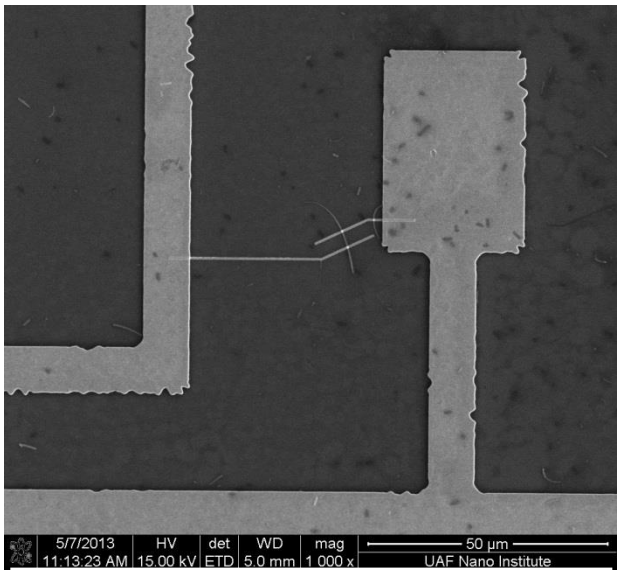

Figure 4.14 Two connections structure, platform 11 (Thach Pham, May 2013, University of Arkansas)

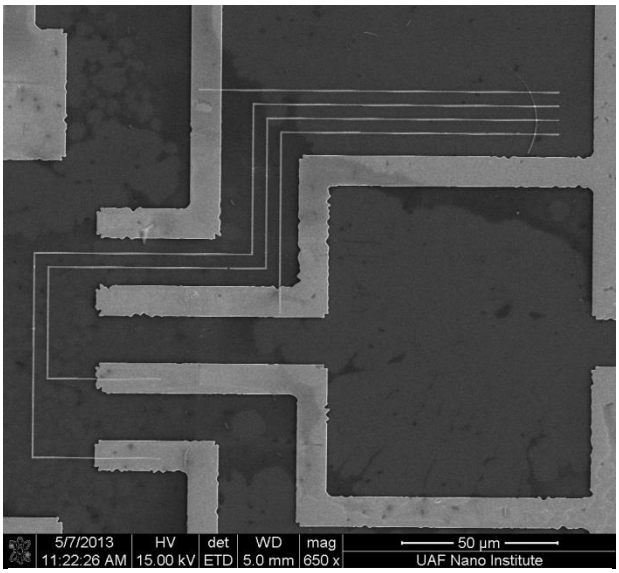

Figure 4.15 (a) Four connections structure, platform 11 (Thach Pham, May 2013, University of Arkansas)

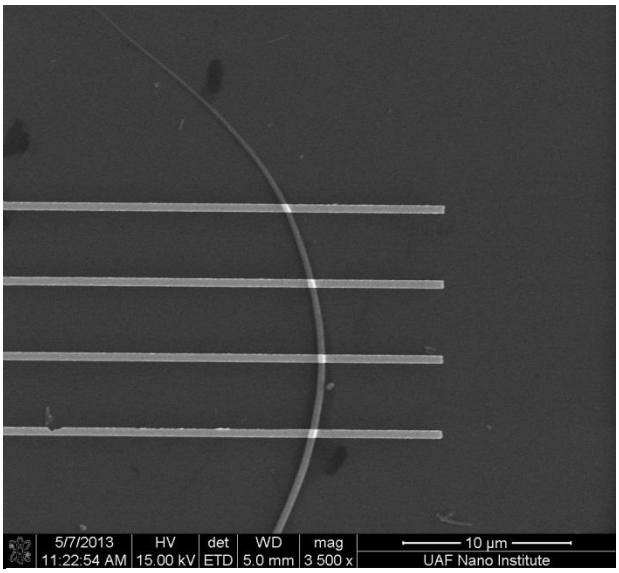

Figure 4.15 (b) Zoom in four connections structure, platform 11 (Thach Pham, May 2013, University of Arkansas)

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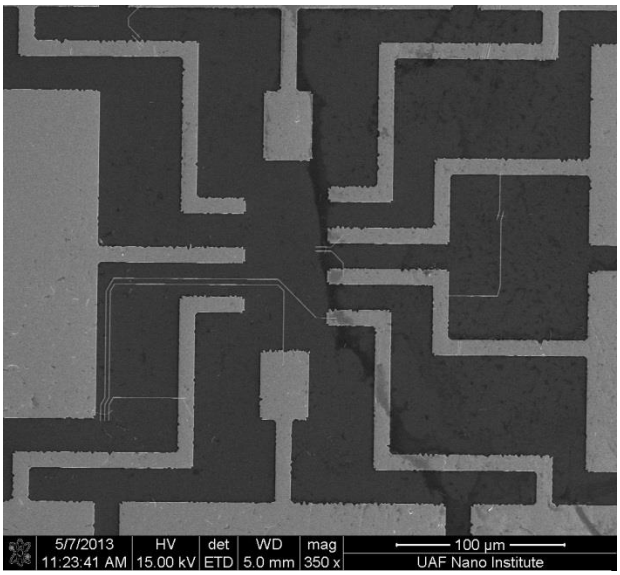

Fig 4.16 Map layout of platform 13 (Thach Pham, May 2013, University of Arkansas)

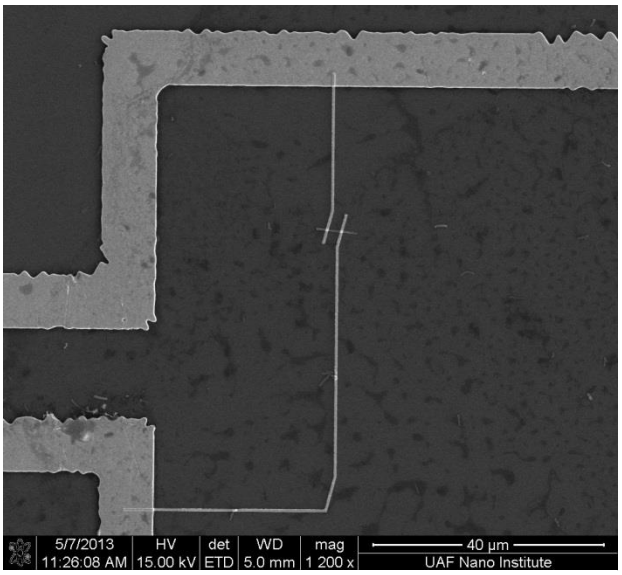

Fig 4.17 Two connections structure, platform 13 (Thach Pham, May 2013, University of Arkansas)

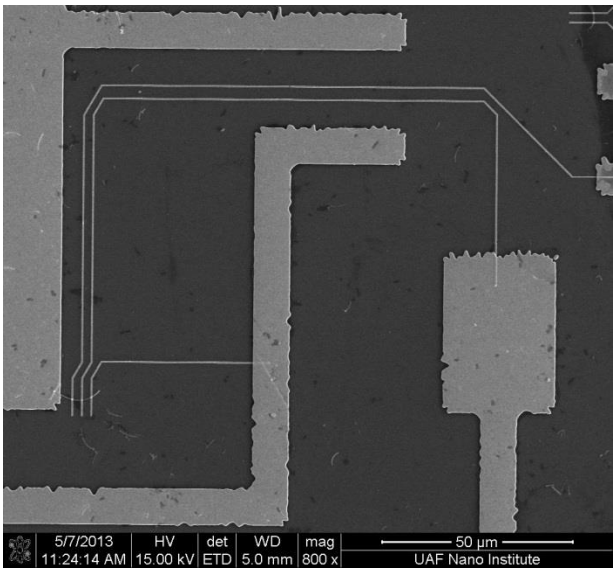

Fig 4.18 (a) Four connections structure, platform 13 (Thach Pham, May 2013, University of Arkansas)

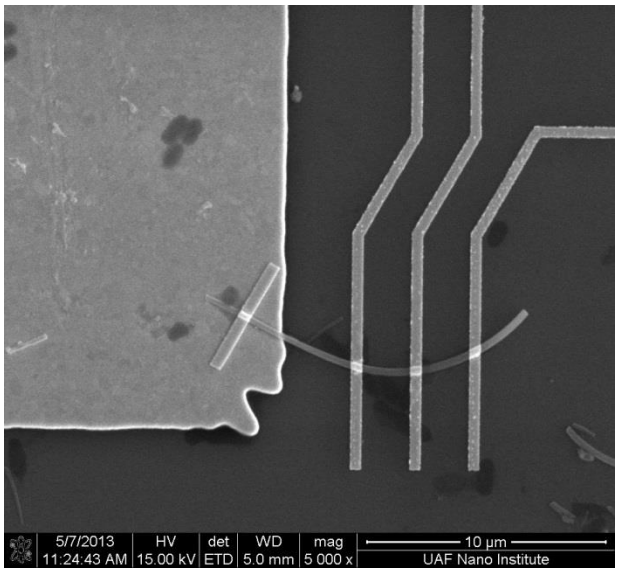

Fig 4.18 (b) Zoom in four connections structure, platform 13 (Thach Pham, May 2013, University of Arkansas)

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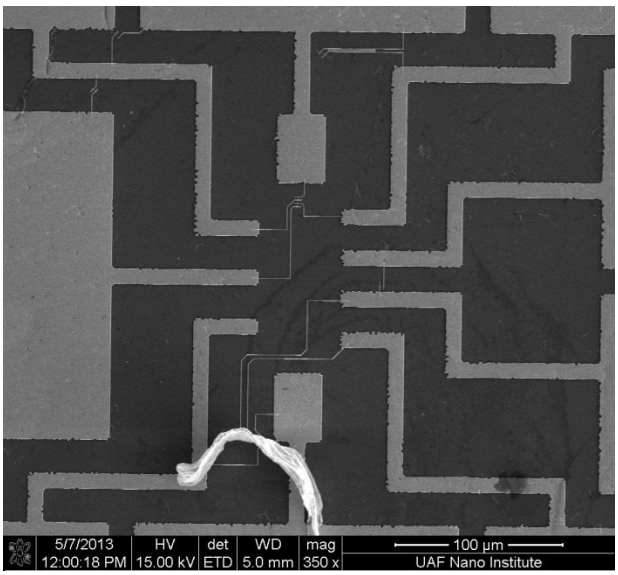

Fig 4.19 Map layout of platform 32 (Thach Pham, May 2013, University of Arkansas)

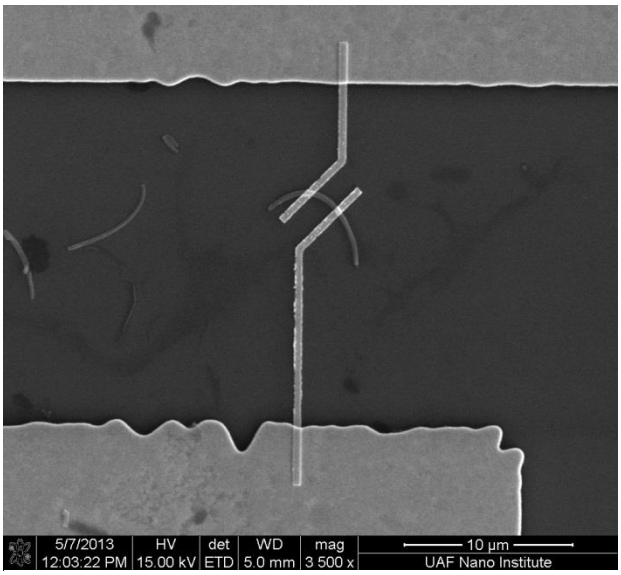

Fig 4.20 Two connections structure, platform 32 (Thach Pham, May 2013, University of Arkansas)

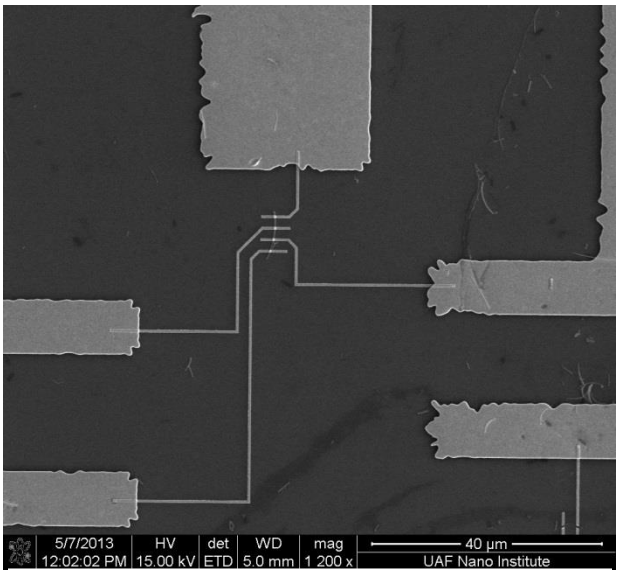

Fig 4.21 (a) Four connections structure, platform 32 (Thach Pham, May 2013, University of Arkansas)

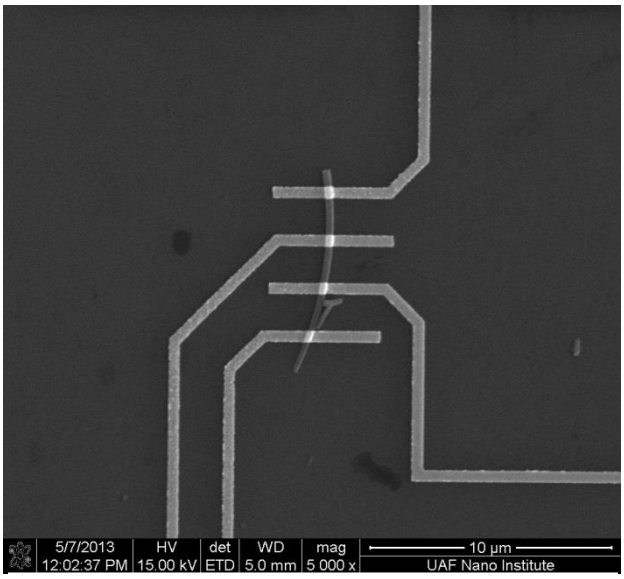

Fig 4.21 (b) Zoom in four connections structure, platform 32 (Thach Pham, May 2013, University of Arkansas)

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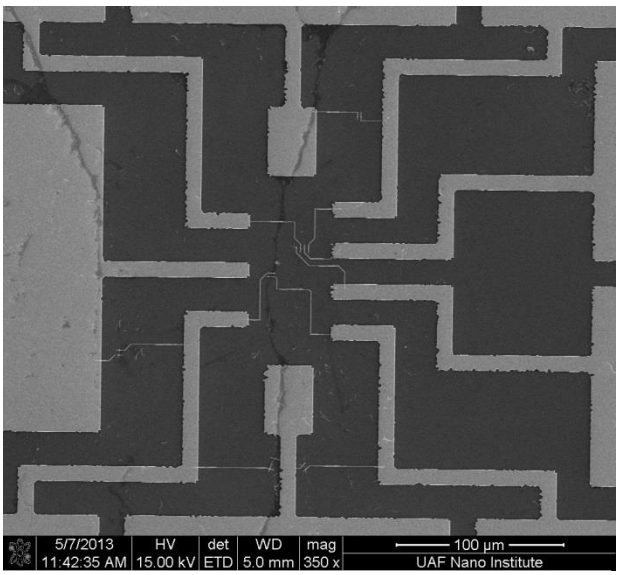

Fig 4.22 Map layout of platform 41 (Thach Pham, May 2013, University of Arkansas)

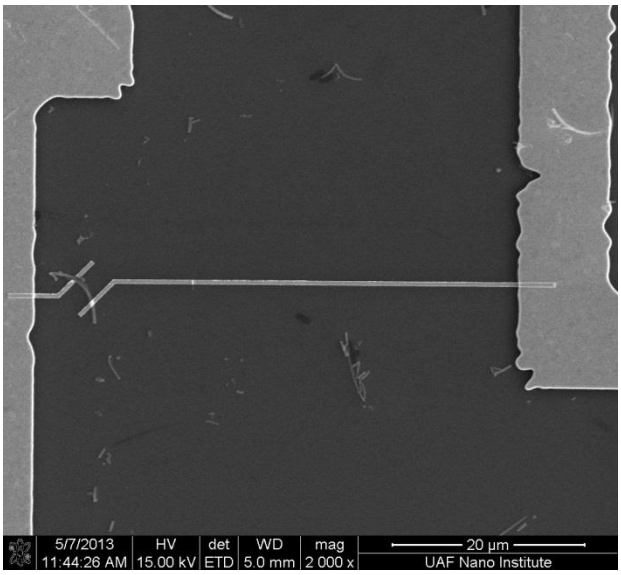

Fig 4.23 Two connections structure, platform 41 (Thach Pham, May 2013, University of Arkansas)

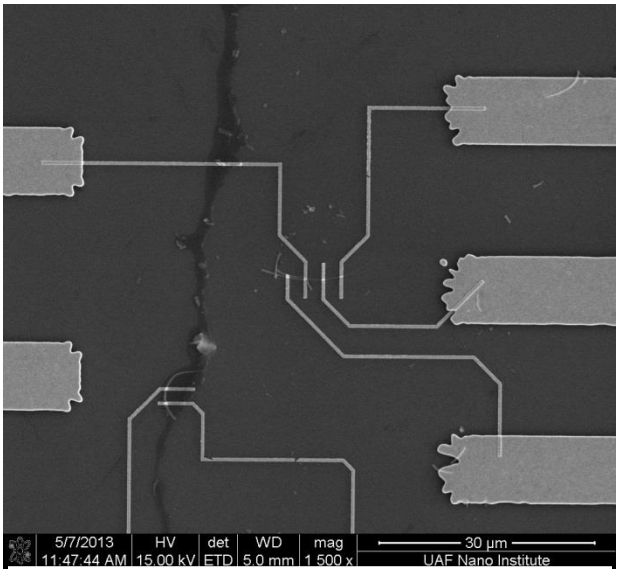

Fig 4.24 (a) Four connections structure, platform 41 (Thach Pham, May 2013, University of Arkansas)

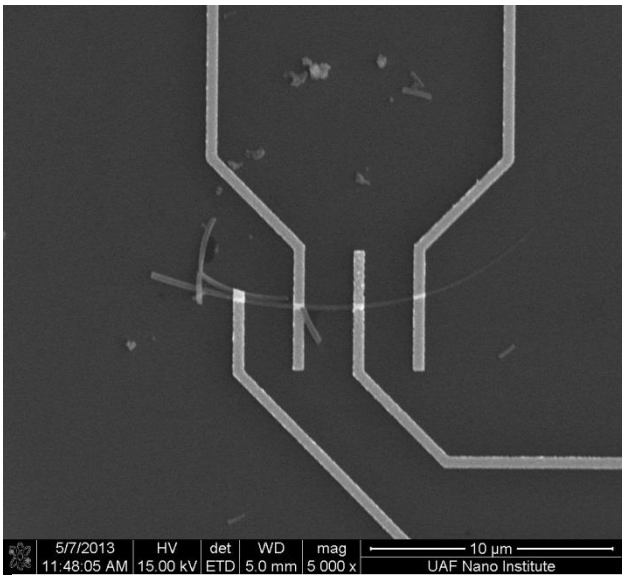

Fig 4.24 (b) Zoom in four connections structure, platform 41 (Thach Pham, May 2013, University of Arkansas)

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4.4 Current-voltage measurement of single horizontal Si nanowires device

4.4.1 Measurement setup

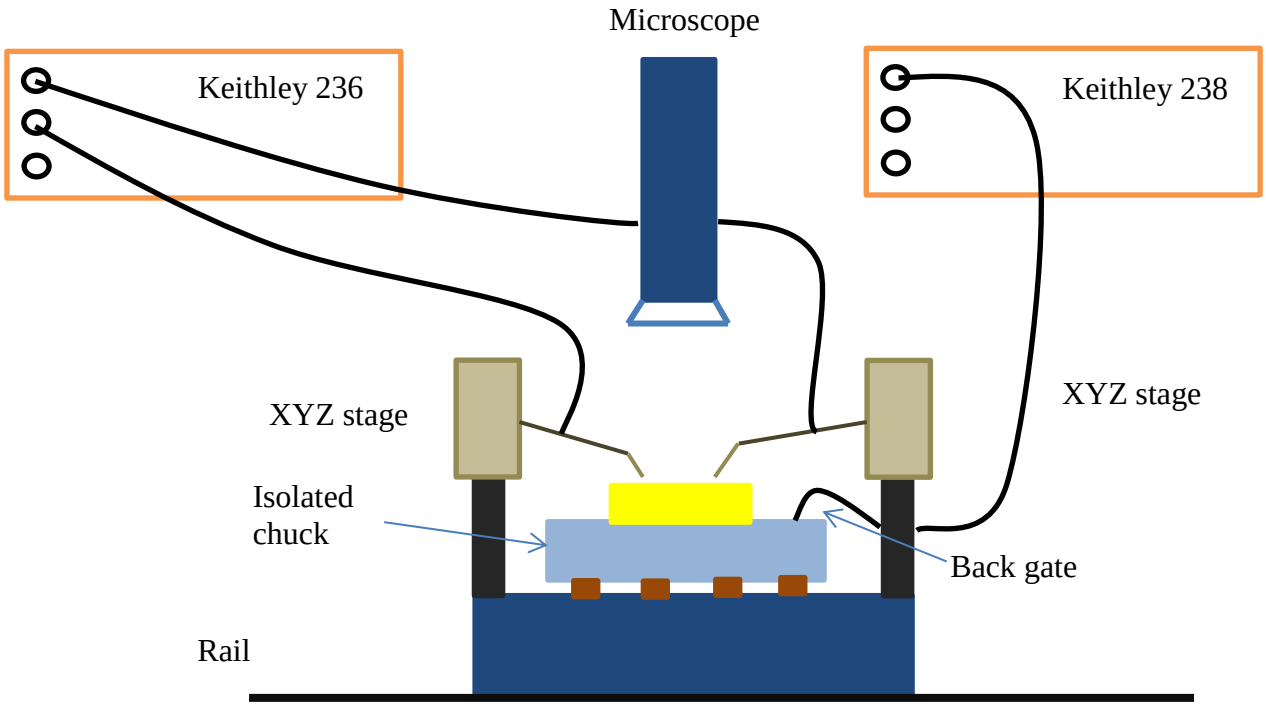

Fig 4.25 The instruments setup for I-V measurement (Thach Pham, July 2013)

The current voltage measurement general is mainly composed of two source measurement units (SMU) Keithley 236 and Keithley 238, a probe station mounted on a rail, one sun simulator, and a microscope, as shown in figure 4.25. The probe station has a sample holder which is isolated from the ground and is connected to a temperature control system. Two 3D stages, placed on the probe station, control the movement of the needles. Keithley 236 and Keithley 238 have a current resolution of 100fA. They are both connected to a trigger control and share a common ground. Measurement connection and data interpretation is controlled by ICS program.

For the photoconductivity measurement, the probe is placed in contact with two metal pads which form two terminals contacts with the nanowire. The two terminals are connected to

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Keithley 236 through guarded-coaxial cables. The rail is used to transfer the probe station to the one sun simulator station.

For the I-V measurement with the effect of back gate voltage biasing, the setup is initially set with two point probe. Keithley 238 is used as the gate voltage source. It is connected to the back side of the substrate.

4.4.2 Measurement results and discussions

(a) Photoconductivity measurement

The photoresponse of the single horizontal Si nanowires device has been conducted using two terminals measurement. The voltage source is swept from -100V to 100V. I-V curve of 15 singles nanowires are obtained under both dark condition and light (one sun simulator) condition.

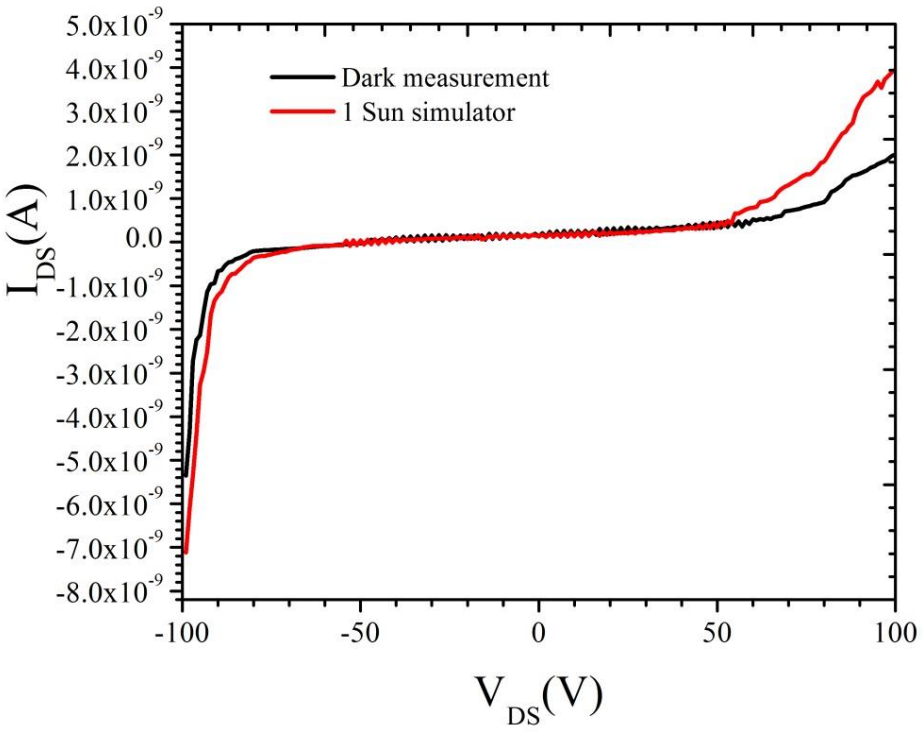

Fig 4.26 The photoresponse of single Si nanowire (Thach Pham, June 2013, University of Arkansas)

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Figure 4.26 shows that there is current amplification under the one sun light. The amplification factor varies among devices. The current enhancement is clearly observed at 50V where the current value of nanowire device under light illumination exhibits two times greater than the one under dark environment. The I-V curve also implies that the amorphous Si layer at the outer shell of the nanowire has very low number of carrier concentration. It is in good agreement with the theory of growth nanowire using Au as the catalyst in the plasma enhanced chemical vapor deposition (PECVD). The a-Si layer acts as intrinsic layer or very lightly doped, approximately $10^{14}cm^{-3}$.

The non-linear curve shows that the metal electrodes did not make ohmic contact to the Si nanowire, yet they form a Schottky barrier. The barrier height forming by Au and the shell of nanowire, amorphous silicon, could be estimated approximately 1.2eV from the difference between the work function of Au (~5.1eV) and the electron affinity of amorphous silicon (~3.9eV), as shown in figure 4.27.

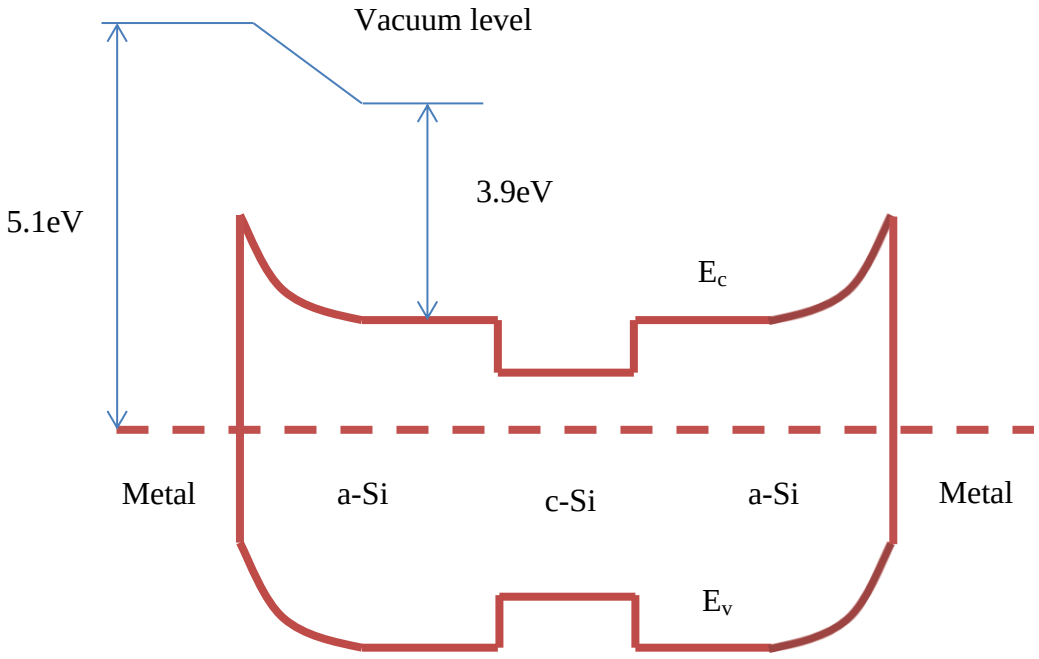

Fig 4.27 Band gap diagram at two terminals (Thach Pham, June 2013, University of Arkansas)

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From the figure 4.26, the turn on voltage of the metal-semiconductor junction is not observable. The nanowire is connected to two metal pads which lead to the formation of two Shottky barriers. One of the two terminals is selected as the reference ground. Therefore, when a positive voltage is applied to the terminals, one is forward bias while the other one is reverse bias and vice versa in case of negative applied voltage. The measured current is the sum up of two current curve of each terminal. Due to the symmetry, the portion of each I-V curve in the turn on region cancels each other. Consequently, only the breakdown voltage regions on both forward bias and reversed bias are left, as shown in figure. On the reverse bias side, the breakdown phenomenon occurs approximately at -85V while it is 55V on the forward bias side.

There is a higher probability that the avalanche breakdown dominates the breakdown phenomenon. Under reverse bias condition, the depletion width is reduced, but not as effective as high doping levels. The a-Si in the device is lightly doped. Therefore, the tunneling breakdown might occur at the junction, but has low impact comparing to the avalanche breakdown. Another fact confirming the nanowire is intrinsic is the triggering condition of the avalanche breakdown. The phenomenon depends on the concentration of the semiconductor. If the material is highly doped, the built in electric field is high enough that requires less external voltage to trigger the breakdown [15]. As shown in figure 4.26, it requires -85V to achieve breakdown condition. Consequently, the a-Si layer is intrinsic or lightly doped.

Furthermore, a low current is observed in the range of -80V to 50V. By applying reverse bias voltage, the barrier height is increased to $q(V_{bi} + V_a)$ in the depletion region of the semiconductor. At the same time, it will prevent the electrons from the semiconductor to move through the contact. The reverse bias current is formed only by a minority of electrons that could

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travel from the metal to the semiconductor side under the thermionic effect. A current value ranging from 10^{-11}A to $3x10^{-10}$ A was reported as the reverse bias current.

(b) Gate dependent current versus bias voltage measurement

V_G dependent I-V characteristic of the composite Si nanowires were measured. The gate voltage is biased at 0V, 10V, 20V, 30V, 40V, and 50V respectively.

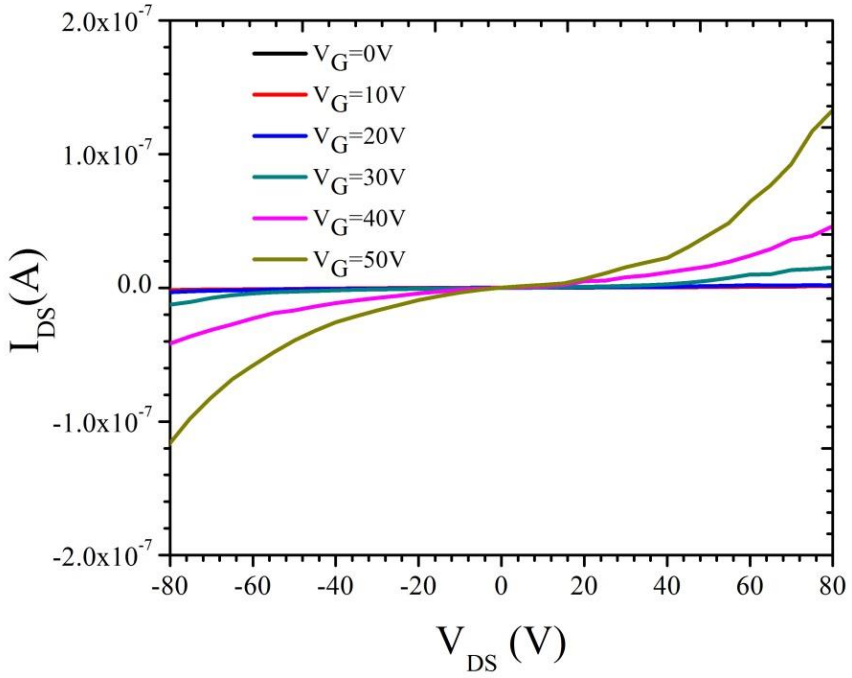

Fig 4.28 I_D-V_{DS} characteristic curves as a function of V_G of 0V, 10V, 20V, 20V, 30V, 40V, and 50V (Thach Pham, June 2013, University of Arkansas)

The I-V characteristic of the single silicon nanowire is nonlinear, as shown in figure 4.28. The nonlinearity could be explained in the same manner as the previous section. As the gate voltage changes from 0V to 50V with 10V of increment, the measured current rapidly increases from 10^{-9}A to 10^{-7}A. The gate voltage which is applied on the back side of the substrate forms an electric field. The electric field attracts more electrons and forms an inversion layer at the bottom side of the nanowire. The inversion layer could be considered as n type semiconductor and is a

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conductive channel between drain and source. Therefore, the conductivity of the nanowire is enhanced. It is also implied that the nanowire is lightly n-type [17]. In fact, the I_{DS} is significantly triggered at V_G = 30V, which could be considered as the threshold voltage of the device. However, the true value of the threshold voltage cannot be obtained when the Schottky barrier exists. A high gate voltage value is due to the thick of the oxide layer SiO_2 (250nm), which is 50 times thicker than the state of art of field effect transistor.

The carrier mobility μ could be calculated from the transconductance g_m.

$$\mu = \frac{g_m L^2}{C V_{DS}} \text{ [18]}$$

Where L is the length of the nanowire and C is the capacitance of the nanowire.

The transconductance can be extracted from the dI_{DS}/dV_G. The capacitance is given by:

$$C = 2\pi\epsilon_o\epsilon \frac{L}{\ln(\frac{2t_{ox}}{r})} \text{ [19]}$$

Where t_{ox} is the thickness of SiO_2 and r is the radius of the nanowire

The transconductance and carrier mobility of this nanowire are estimated approximately at 66.2 pS (V_{DS} = 25V) and $36x10^{-6}$ $cm^2V^{-1}s^{-1}$. The silicon nanowire mobility is extremely low. A further study of carrier mobility as a function of nanowire diameter will expand the influence of nanowire physical parameter to the nanowire characteristics. Another possibility could cause low conductivity of the nanowire is its crystalline structure. It could contain defects that reduce the number of conductance channel [13].

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Table 4.2 List of nanowire types, metal contacts, and the I-V behaviors

Nanowires type	Metal contacts	I-V behavior	Note	References
Intrinsic c-Si	50nm Al / 150nm Au	Non linear		[17]
P-doped Si	50nm Al / 150nm Au	Non linear		[17]
Heavily P-doped Si	50nm Al / 150nm Au	Linear		[17]
B-doped Si	50nm Al / 150nm Au	Linear		[17]
Heavily B-doped Si	50nm Al / 150nm Au	Linear		[17]
B-doped Si	50nm Ti / 50nm Au	Linear	With annealing	[2]
c-Si	300nm Al	Linear		[20]

The I-V behavior of single Si nanowire that is studied by others researchers is summarized in table 4.2. The linear behavior at the junction is observed in most of the cases where Si nanowire is heavily doped or the Si/Ti interface is thermally treated. Aluminum is also a candidate to form the ohmic contact. In case of our device, the sample could either be annealed or fabricated with Al.

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CHAPTER 5: FABRICATION AND CHARACTERIZATION OF VERTICAL SINGLE NANOWIRES STRUCTURE

5.1 Introduction

In addition to electrical characterization of a single nanowire, optical measurement is considered a supplement to enhance the study of single nanowire. By integrating the electron beam lithography method, this chapter describes substantial processes to create a platform where optical characterization and single nanowires growth could be conducted.

The essential step is to pattern an array of circles on top of a piece Si sample coated with a thin layer of Au. Patterned circles play as the base where ZnO nanowires are grown vertically using electrochemical method. The growth of single ZnO nanowire is based on the diameter of the circle which is controlled by EBL. Finally, photoluminescence will be conducted as the main optical characterization.

5.2 Fabrication process of vertical single nanowires structure

Compared with the fabrication process of horizontal single nanowires devices, the fabrication process of a vertical single nanowires structure is simpler and could be divided into two main steps which are platform preparation and nanowires growth. Platform preparation is composed of substrate preparation (substrate metallization and substrate coating), EBL platform design, as well as EBL writing as shown in figure 5.1. Nanowires growth part is done by Dr. Jingbiao Cui at University of Arkansas at Little Rock and will not be discussed.

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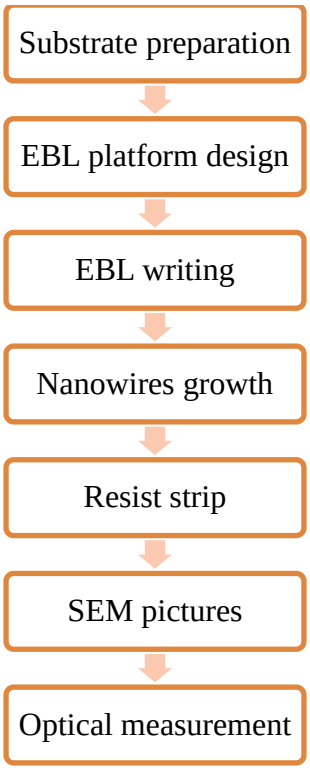

Fig 5.1 Flow of critical fabrication processes (Thach Pham, July 2013)

Following table 5.1 represents a list of equipment used in fabrication process of vertical single nanowires structure and spending time for each process.

Table 5.1 Equipment and tools reserved for fabrication process of single vertical nanowires

Process	Related equipment & tools	Time cost
Traveler preparation	• Microsoft office	
Platform preparation	• Develop bench • Spinner • Hot plate • Thermal evaporator AUTO 306T	1 day / 4 samples

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	• Microscope	
Platform design	• Auto CAD 2012 • LinkCAD 7	1 hour / design
EBL writing	• EBL system JEOL 5500ZD • Develop bench • Microscope	2-3 hours / sample
Resist strip	• Wet bench • Microscope	1 hour / sample
SEM pictures	• FEI NOVA 200	2 hours / sample

In general, it will take two days to prepare the platform. However, nanowires growth will take two weeks to finish due to transport time back and forth between the University of Arkansas, Fayetteville and UALR. Another day is needed to strip the resist before taking SEM pictures for evaluation.

5.2.1 Processing flow

Horizontal single Si nanowire structure:

- Substrate: 5nm Cr / 200nm Au coated c-Si piece sample
- E-beam resist: 50-60nm PMMA 2%
- Nanowire: ZnO

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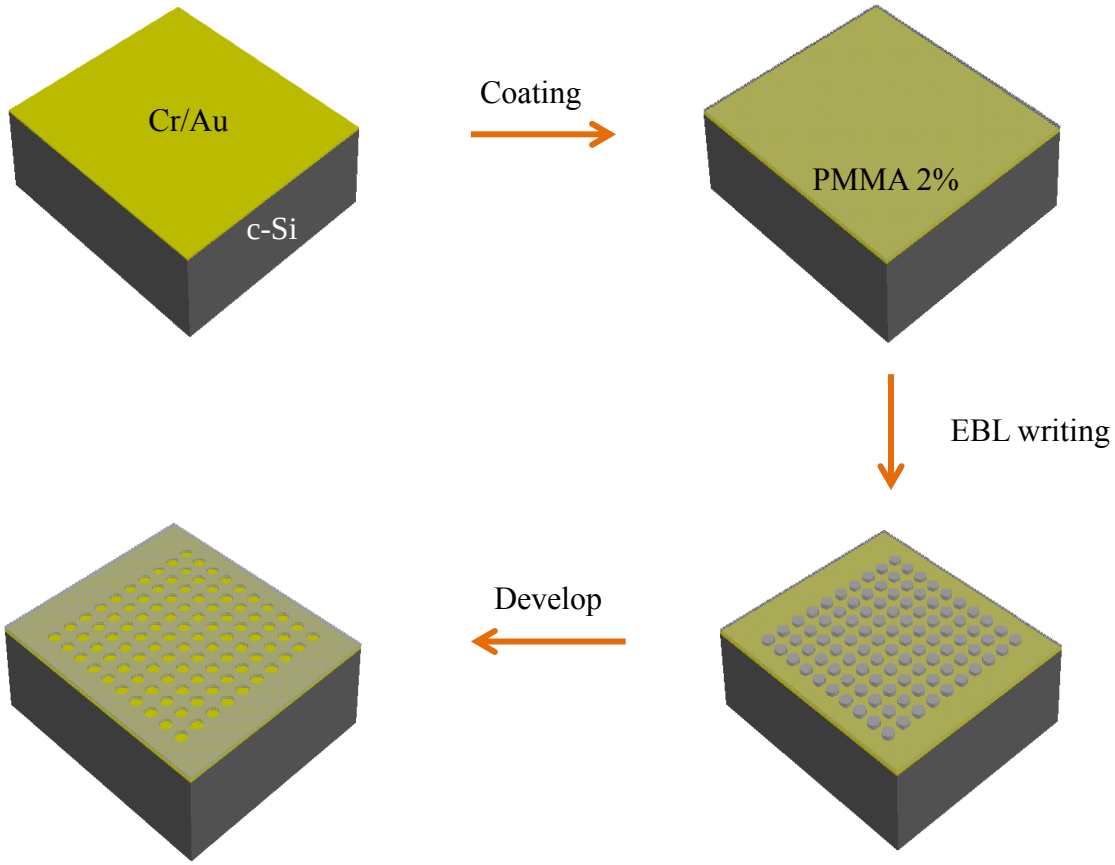

Fig 5.2 3D processing flow of single vertical nanowire structure (Thach Pham, July 2013)

5.2.2 Platform preparation

(a) Substrate metallization

A thin layer of metal, 5nm Cr and 200nm Au, is first deposited on 5" c-Si wafer using thermal evaporation Edward 306T. Gold is chosen as the main platform material from which ZnO nanowires are growth by UALR.

- Pre-clean 5" Si wafer by solvent cleaning process: acetone, methanol, and IPA since processing 5" wafer has high quality and cleanness.
- Load 5" wafer sample on sample holder disc.

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- Place/replace Cr rod and fill new Au pallets on boat
- Pump down chamber for 2-3 hours until it reaches approximately 8E-6 mTorr
- Start depositing metal at rate of 1-2 A/s to obtain 5nm Cr and 200 nm Au

Second, metalized wafer is cut into multiple pieces of rectangle shapes 0.5cmx1.5cm using diamond scriber. A larger size (any size greater than 0.7cmx1.5cm) may cause uneven resist coating.

(b) Substrate coating

After collecting piece samples from earlier step, selected samples go through a solvent cleaning process using acetone, methanol, and IPA followed by e-beam resist coating. In order to achieve feature size less than 100nm, PMMA 495K 2% should be used rather than PMMA 495K 4%. At 3000 rpm, PMMA 495K 2% gives 50-60nm of thickness while PMMA 495K 4% gives 180nm of thickness.

- Cover spinning plate with blue tape to protect the back of sample and vacuum chuck.
- Spin coat poly methyl methacrylate (PMMA) 495K 2% at 3000 rpm. This gives approximately 60nm of resist thickness.
- Bake coated sample at 180^{o}C for 2 minutes and let it cool down.

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(c) Platform design

A platform composed of equidistant nanostructures (in a circle shape) is patterned by EBL to create separated bases where a single ZnO nanowire is grown vertically in each hole. In order to evaluate geometric parameters and to characterize optical properties of single vertical ZnO nanowires, two areas of distinct pitch size are recommended. The circle diameter is also crucial since it affects the structure of nanowires which could be single or multiple nanowires. Consequently, two designs are needed to complete this fabrication process: one dedicated for calibration purpose and another one used for nanowires growth and characterization purposes.

1st design (refer chapter 3 for details): The structure of this design is simply 25 arrays of circles with different diameter size ranging from 60nm to 1um. Each array is represented by a unique layer which is equivalent to 1 exposure dose (25 layers in total). Pitch size variation is not substantial.

2nd design: As the optimized dose has been found from the 1st design, the structure of 2nd design is composed of arrays of circles (single layer) covering an area of $1mm^2$. The selection of circle diameter is decided based upon one crucial criterion that secures the successful rate of growing a single vertical nanowire. After the 1st test batch, single vertical nanowires are found on circles of 100nm diameter. In addition, 5umx5um pitch size is selected for SEM while 30umx30um pitch size is dedicated for PL measurement.

All design files are saved as *.dwg format in Auto CAD 12. They will go through converting process from *.dwg format to *.v30 format to be used in EBL JEOL 5500ZD system. Refer chapter 3 for more details of this step.

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(d) EBL writing

The EBL writing process for the fabrication of single vertical nanowires resembles the one of metallic nanostructures in chapter 3. Calibration and exposure will be two crucial processes.

While calibration process is consistent for most of fabrication processes, exposure deviates from case to case.

Important settings for 1st design:

- Working condition of EBL system:
  - EOS mode 2
  - Aperture 2
  - 4th lens
  - Accelerating voltage 50kV
  - Current -0.5nA
- Exposure dose:
  - Initial dose: 500uC/cm^2
  - Short rank: -20% to 100%

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- Map layout:

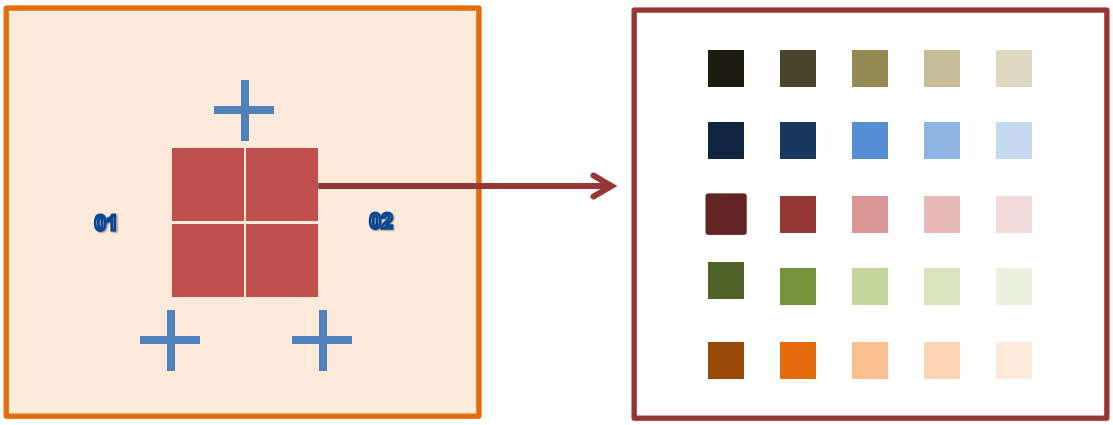

Fig 5.3 Map layout of 1st design (Thach Pham, July 2013)

  - Figure 5.3 shows a map layout of the 1st design. Each identical red square which represents a range of exposure dose includes 25 blocks arrays of circles. The structure of each block is composed of circles having diameter that varies systematically from 60nm to 100nm with 10nm of increment and from 100nm to 1um with 100nm of increment.
  - The color of each small square represents for different dose usage.
  - 3 global PQ marks defined the boundary of main patterned features.

Important settings for 2nd design:

- Working condition of EBL system:
  - EOS mode 2
  - Aperture 2
  - 4th lens
  - Accelerating voltage 50kV
  - Current -0.5nA
- Exposure dose:

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- Optimized dose for circle of 100nm: 620uC/cm^2
- Optimized dose for circle of 200nm: 710uC/cm^2

- Map layout:

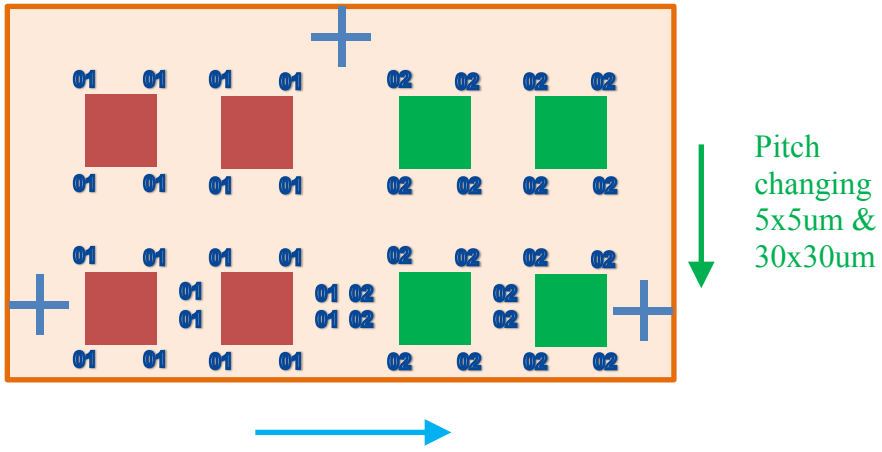

Fig 5.4 Map layout of 2nd design (Thach Pham, July 2013)

- Figure 5.4 shows map layout of 2nd design. Each square represents 200x200 circles (5umx5um pitch size) and 30x30 circles (30x30um pitch size) of same diameter.
- The red square represents 100nm circles (01 at four corners) while the green square represent 200nm circles (02 at four corners).
- The pitch size stays the same 5x5um for 1st array and switch to 30x30um for 2nd array.
- Four top structures are dedicated for SEM evaluation.
- Four bottom structures are dedicated for optical measurement (PL). Pitch size is 30umx30um so that optical characteristic of single nanowire could be easily observed without interference of consecutive nanowires.

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- Three global PQ marks defined the boundary of main patterned features.

5.2.3 ZnO nanowires growth

The growth of single vertical ZnO nanowires is done by Dr. Cui from UALR. This is a collaboration work between two universities, one provides platform patterned by EBL while the other one takes charge of growing ZnO nanowires using electrochemical method. The method of growth will not be discussed in this thesis.

5.2.4 Resist strip

In order to conduct optical measurement with high levels of accuracy, the e-beam resist that was not exposed during the EBL writing process must be removed completely. First attempt has been made by slowly drop remover PG which is pre-heated at 70^{o}C on tilted sample surface. Any strong physical contact with sample surface will damage nanowires structure. The sample with vertical ZnO nanowires is air dried naturally.

SEM pictures show that remover PG is too strong since it not only remove e-beam resist but also etches down ZnO nanowires. Although the 2^{nd} attempt has not been conducted, acetone stored at room temperature is suggested to strip the e-beam resist completely without modifying nanowires physical condition.

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5.3 SEM pictures of single ZnO nanowire

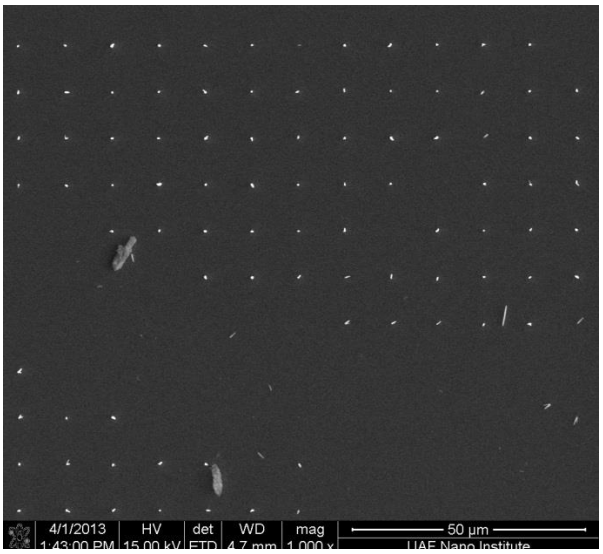

Fig 5.5 Field of ZnO nanowires, top view (Thach Pham, April 2013, University of Arkansas)

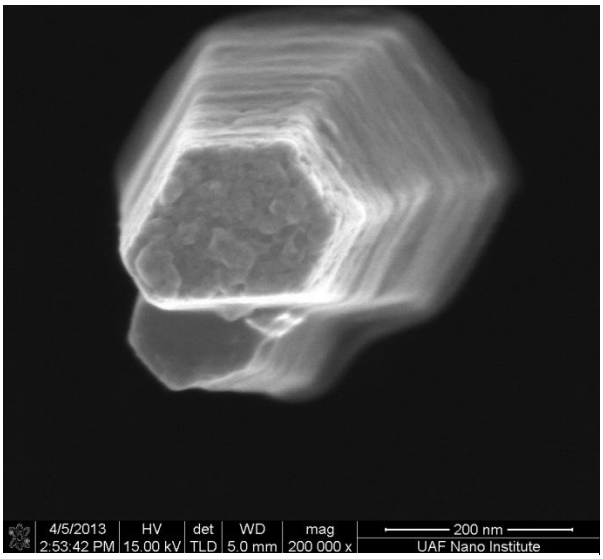

Fig 5.6 Two ZnO nanowires grown on same base (Thach Pham, April 2013, University of Arkansas)

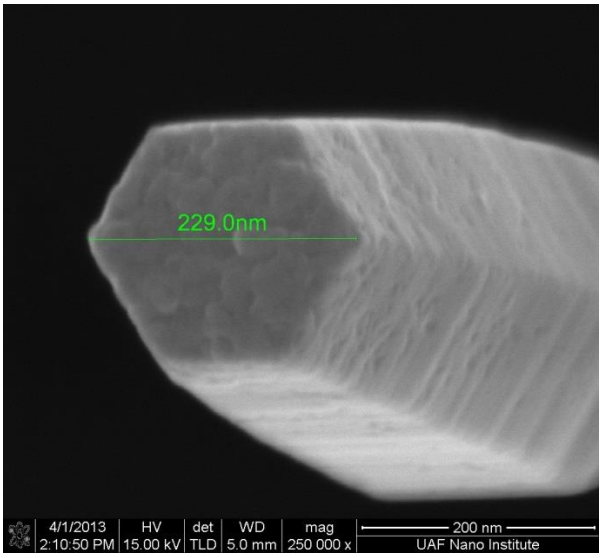

Fig 5.7 Single ZnO nanowire with top diameter of 229nm, top view (Thach Pham, April 2013, University of Arkansas)

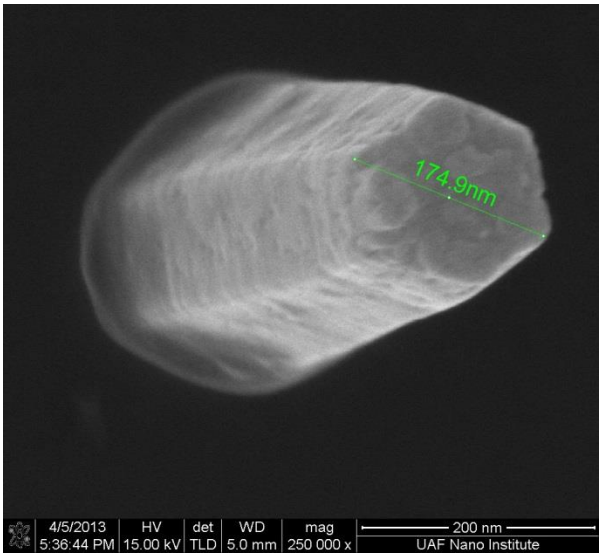

Fig 5.8 Single ZnO nanowire with top diameter of 175nm, top view (Thach Pham, April 2013, University of Arkansas)

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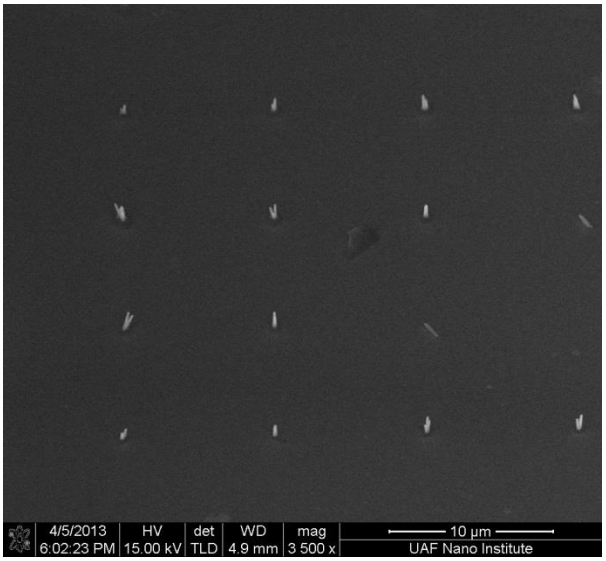

Fig 5.9 Field of ZnO nanowires after resist removal, 45^{o} tilted (Thach Pham, April 2013, University of Arkansas)

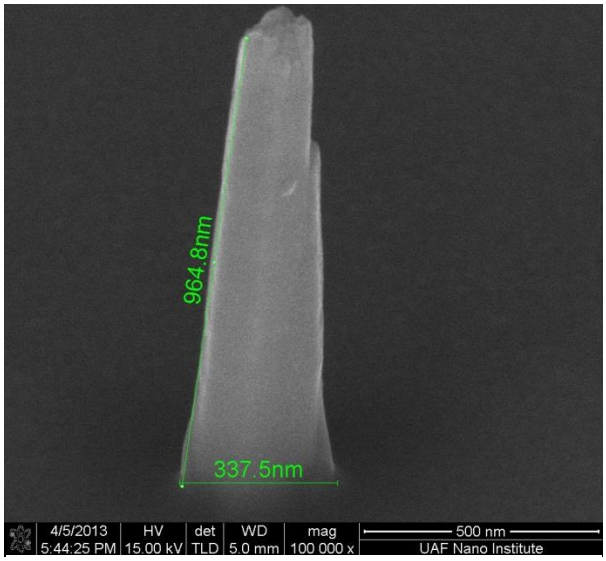

Fig 5.10 Single ZnO nanowire with 965nm length after resist removal, 45^{o} tilted (Thach Pham, April 2013, University of Arkansas)

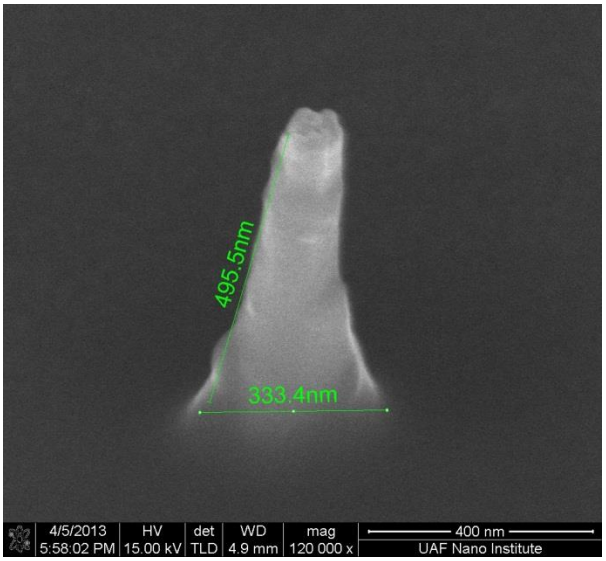

Fig 5.11 Single ZnO nanowire with 495nm length after resist removal, 45^{o} tilted (Thach Pham, April 2013, University of Arkansas)

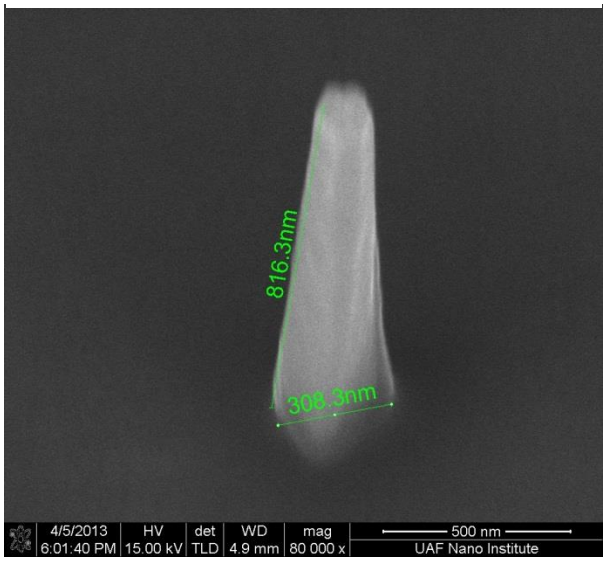

Fig 5.12 Single ZnO nanowire with 816nm length after resist removal, 45^{o} tilted (Thach Pham, April 2013, University of Arkansas)

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5.4 Photoluminescence measurement of single ZnO nanowire

Photoluminescence (PL) measurement is a common method to optically investigate material properties. An optical source having an energy level greater than the typical band gap value of the measuring material is used to excite the sample. As a consequence, electron-hole pairs are generated and later participate in various recombination mechanisms. Only radiative recombination, a dominant mechanism at room temperature, produces emitted light which provides the picture of material band gap [21].

A simple self-built PL setup which is mainly composed of a green laser source (wavelength of 355nm) and a photodetector having a working range from 200nm to 800nm is used to obtain the photo-response of single ZnO nanowire. Five different positions of single ZnO nanowire are arbitrary selected as shown in figure 5.13. The detector is kept at low temperature (approximately 80 ^{o}F) in order to reduce the thermal noise.

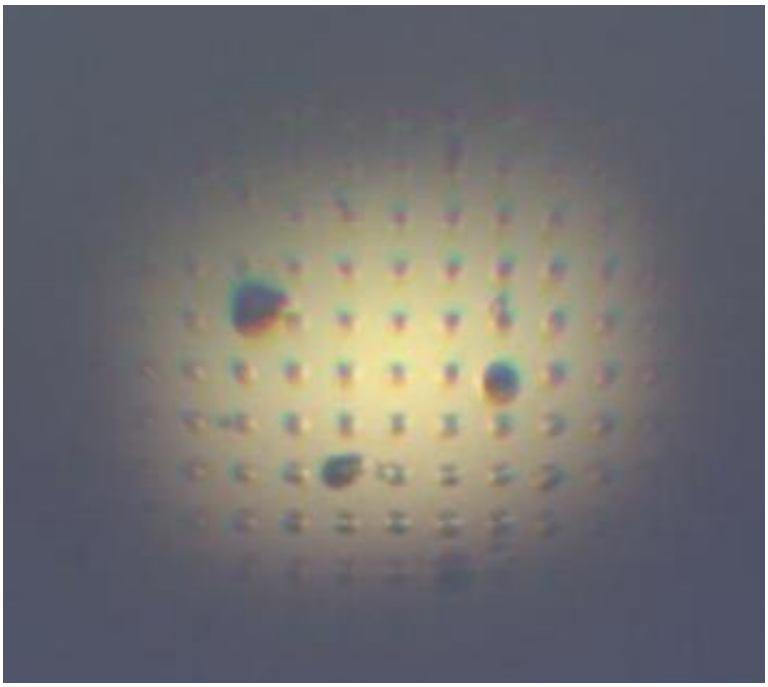

Fig 5.13 Camera picture of single ZnO nanowires (Thach Pham, May 2013, University of Arkansas)

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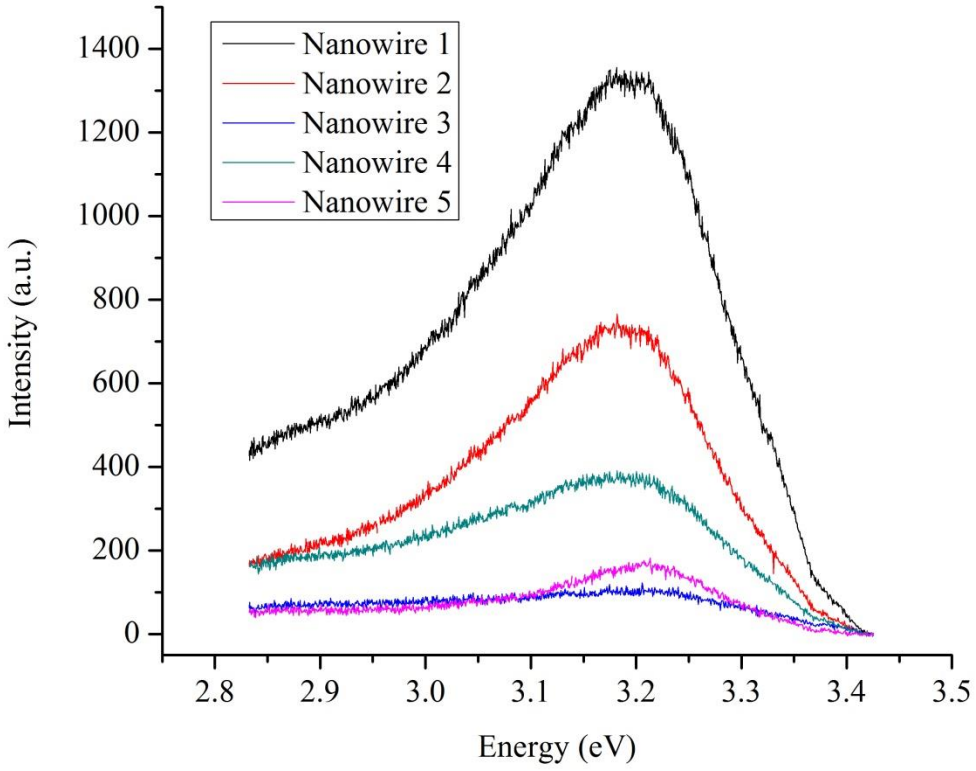

Fig 5.14 Photo-response of single ZnO nanowire sample at room temperature (Thach Pham, May 2013, University of Arkansas)

Figure 5.14 provides the spectrum of five different measuring spots on the single ZnO nanowire sample. The measured band gap is approximately 3.22eV (~387nm) which is comparable with conventional PL measurement of ZnO [22], [23]. The dominant concern is the weak spectrum obtained from the single ZnO nanowires. This is possibly caused by the etching effect of the remover chemical (remover PG) during the resist removal process where single nanowire height is reduced. A less reactive resist remover could solve the problem. Another modification in order to reduce the discrepancies of spectrum intensity is to increase the pitch size between adjacent single ZnO nanowires from 20um to 30um. This will eliminate the photo-

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response of multiple single ZnO nanowires at one location since the laser spot size is approximately 20um.

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CHAPTER 6: CONCLUSION

First, the JEOL 5500ZD is extensively used to fabricate the metallic nanostructures such as rings circles, and lines on various photoresists. Lines with a width of 90nm were fabricated on the ZEP 520A. Circles structures were successfully demonstrated on PMMA with a diameter of 1um, 500nm, 300nm, 100nm, 90nm, 80nm, 70nmn, 60nm (PMMA). Rings' inner diameter is down to 70nm while outer diameter could reach to 300nm. The next target is to fabricate nanostructures at smaller size while consistent improve the shape of the features.

Second, horizontal single Si nanowire device is fabricated by integrating the EBL technique with conventional photolithography. The contacts were made between Au and the composite Si nanowire (a-Si/c-Si) and form a Schottky contact. The two point probe I-V measurement were conducted to evaluate the performance of the device with incident light and with a gate voltage applied at the back gate. The measured I-V characteristic predicts that the Si nanowire is lightly n-doped and has low conductivity. The breakdown phenomena were observed at high voltage (-85V and 55V). A transconductance of 66.2 pS (V_{DS} = 25V) and a carrier mobility of $36x10^{-6}$ $cm^2V^{-1}s^{-1}$ were reported. The lightly doped nanowire in combination with Schottky barrier prevents the field effect transistor characteristic. There are several suggestions for this problem. Either annealing the sample or change the contact metal from Au to Al will reduce the barrier height and could form an ohmic contact, which is more desirable for FET device. For future studies, the mobility as a function of diameter and the temperature dependent I-V characteristic should be conducted. In addition, the presented Si nanowire can be replaced by other materials such as ZnO or grapheme.

Third, nano-scale cirlces were carefully calibrated and fabricated to create the platform where single ZnO nanowires are grown vertically. Single ZnO nanowires are found on circles

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having a diameter of 100nm. Photoluminescence were conducted to verify the ZnO nanowire band gap (~3.2eV).

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