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High Temperature LTCC based SiC Double-sided Cooling Power Electronic Module

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Abstract

This objective of this dissertation research is to investigate a module packaging technology for high temperature double-sided cooling power electronic module application. A high-temperature wire-bondless low-temperature co-fired ceramic (LTCC) based double-sided cooling power electronic module was designed, simulated and fabricated. In this module, the conventional copper base plate is removed to reduce the thermal resistance between the device junctions to the heat sink and to improve the reliability of the module by eliminating the large area solder joint between the power substrate and the copper base plate. A low-temperature co-fired ceramic (LTCC) substrate with cavities and vias is used as the dielectric material between the top and bottom substrates and it also serves as the die frame. A nano silver attach material is used to enable the high-temperature operation.

Thermal and thermo-mechanical simulations were performed to evaluate the advantages of the LTCC double-sided power module structure and compared to other reported module structures and its wire-bonded counterpart. The junction-to-case thermal resistance for the power module without a copper base plate is 0.029^{o}C/W, which is smaller than that of the power module with a copper base plate. Thermo-mechanical simulation reveals that double-sided cooling power modules generate higher thermal stresses when compared to that of the single-sided cooling power modules which indicates the trade-off between the junction temperature and the thermo-mechanical stress.

Electrical and thermal characterizations were performed to test the functionality of the fabricated module using a 1200V rated voltage blocking capability. The forward and reverse characteristics of the SiC power MOSFET and SiC diode module were tested to 200°C and they demonstrated the functionality of the power module. The junction-to-ambient thermal resistance of the

proposed module is shown to reduce by 11% compared to the wire-bonded equivalent which shows an improvement of the thermal performance of the double-sided cooling structure. Finally, the reliability of the several power substrates was evaluated based on the thermal stress and fatigue life simulation of the bonding layer to determine the mechanical weakest spots of the power module. Thermal cycling experiments were also conducted to validate the simulation results.

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Nomenclature

k Thermal conductivity, W/m·K

Q Power loss, W

R_{th} Thermal resistance, °C/W

T Temperature, °C

V Voltage, V

ν Poisson's ratio

σ Stress, MPa

E Yong's modulus, GPa

τ Shear stress

W Strain energy, W

u Strain energy density, W/mm^3

Acronyms

AC Alternating Current

CTE Coefficient of Thermal Expansion

DBC Direct Bonded Copper

DBA Direct Bonded Aluminum

DC Direct Current

GaN Gallium Nitride

HTCC High Temperature Co-fired Ceramic

IMC Intermetallic Compound

I-V Current-Voltage

LTCC Low Temperature Co-fired Ceramic

LTJT Low Temperature Joining Technology

MOSFET Metal oxide semiconductor field effect transistor

PBGA Power Ball Grid Array

POL Power Overlay

PAI Polyamide imide

RoHS Restriction of Hazardous Substances Directive

SiC Silicon Carbide

SIPOS Semi-insulating polycrystalline silicon

SAM Scanning Acoustic Microscope

SEM Scanning Electronic Microscope

TIM Thermal Interface Material

TDR Time Domain Reflectometry

TAMI Tomographic Acoustic Micro Imaging

TSP Temperature Sensitive Parameter

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Chapter 1. Introduction

1.1 Background and Motivation

Application of new devices and new technologies along with the rapidly growing power electronics market has pushed the power density of power electronic industry toward another higher level. Power electronic modules are of great importance in power electronic systems. The packaging technologies used in these power modules largely influence the electrical, thermal and mechanical properties of the resulting modules. One of the biggest challenges for the power packaging is the thermal management of the module. The power dissipation of semiconductor devices is increasing rapidly as speed and device density increases. On the one hand, keeping a low die temperature plays an important role in maintaining good device performance and improves the fatigue life of the power module. For example, every 10℃ lower transistor temperature gives 1-3% performance improvement, depending on its construction [1]. Arrhenius equation indicates that decreasing every 10℃ reduces failure rate by a factor of 2 within -20℃ to 140℃ of die temperature [2]. Leakage current of the power devices contributed 1% of dissipated power for CMOS circuit which is exponentially related to the device temperature increases and could be orders of magnitude greater at higher temperatures [3]. On the other hand, for some harsh environment applications such as automobiles and aircrafts, high temperature operation becomes increasingly important because it reduces the cost and size of the cooling equipment without a reduction in lifetime [4]. The emergence of silicon carbide (SiC) and gallium nitride (GaN) devices physically allow much higher device temperatures compared to Si devices. However, the packaging technologies for such high temperature operation power modules are inadequate in terms of die attachment, die interconnection, substrate, and cooling assembly. So designing a power module that can extract the heat dissipated by the semiconductor devices as

much as possible while is also able to work under high temperature would be very promising for future power electronics application.

For traditional wire-bonded power modules, the cooling of the module is normally through the bottom side to protect the bond wires on its top side. The heat flux flows through the direct bonded copper (DBC) or other substrate, passes through the thick copper base plate and then goes to the heat sink or cold plate. The interface material between two metals inside the module is solder which has a relatively larger thermal resistance. Soldering is a fast and cheap way to attach power semiconductor die to the substrate. The solder pastes or solder preforms made of tin (Sn) and lead (Pb) were widely used in industry. However, due to the requirements by RoHs, this type of solder will be replaced by a Pb-free solution. Also, soldering technology is not suitable for high temperature application or multi-step manufacturing due to the limitation of the reflow temperature of solders available today. Solder layer inside the power modules is the region that is easy to suffer from fatigue failure under temperature cycling.

The thermal interface material (TIM) for the power module attached to heat sink such as thermal paste or thermal grease normally contributes to the major part of the thermal resistance from power devices to heat sink, which is approximately 50% or more. The reason is that the base plate never contact with the heat sink fully across the entire surface, which occurs when two materials with different coefficients of thermal expansion (CTEs) are joined by soldering or screwing. Even pre-bending may compensate for the deformation to some extent, however, bending also changes when temperature changes. So a pre-bend base plate can only help to increase the contact area at one temperature point and the poorly conducting thermal paste are used to fill the gap between the base plate and heat sink. Wire-bonding is a popular method to realize die interconnection to the input and output pins or lead frame. The traditional aluminum

wire-bonds are widely used historically and provide a fast and cheap way to realize the electrical connection for the package. But wire count and thickness is limited and detaching wire is impossible. Copper wire bonding is the new interconnect technology due to the fact that copper has a much lower electrical and thermal resistance than aluminum. However, the compatibility of the metals used for the wire and bonding pad is of major concern for wire bonding. For example, the intermetallic compound (IMC) grown at the interface will create a brittle bond. Diffusion of one metal to another in a wire bond is called Kirkendall effect, which creates voids at the interface, and further weakens the bond strength and increases the bond resistance. One of the most popular metal combinations in industry, gold wire (Au) and aluminum (Al) bond pad is prone to this failure, especially at elevated temperatures. Large diameter Au and Pt wire bonding is available for high temperature applications with substrate heating.

1.2 Objectives of the Study

The primary goal of this dissertation research is to develop a novel wire-bondless double-sided cooling power module using a 3-D planar packaging technology capable of a working temperature up to 200℃. The module is designed, simulated, fabricated, and characterized. The reliability of the module structure was simulated and initial reliability assessment of the module was performed.

1.3 Outlines of the Dissertation

The outline of this dissertation is as follows. In Chapter 2, a survey of existing packaging technologies for double-sided cooling power module will be presented, which include the traditional wire-bonded module, press pack and flip chip power module, etc. In Chapter 3, the proposed high-temperature low temperature co-fired ceramic (LTCC) based double-sided cooling power module is introduced. The material selections for the substrate, gap sealing and

interface bonding are carefully investigated. The module parasitic inductance based on the layout design is simulated and compared with the wire-bonded counterpart. Chapter 4 presents the thermal performance simulation theory and models used to predict the maximum junction temperature and temperature distribution of the power modules. Several double-sided cooling power modules are investigated and 3D models are constructed to simulate the thermal performance under the same operation conditions and the results are compared to the proposed double-sided cooling module. Chapter 5 concentrates on the thermo-mechanical analysis for the LTCC double-sided cooling module. Finite element simulations are also used in this chapter to identify the maximum thermal mechanical stress inside the module. Chapter 6 illustrates the fabrication process for the proposed module. The process includes DBC and LTCC substrate preparation, dry film and patterning, nano silver paste stencil printing, passivation of the die top surface, sealing material application, and final assembly. Electrical and thermal evaluations of the proposed double-sided cooling power module are described in Chapter 7. In Chapter 8, thermal cycling experiment was conducted to evaluate the reliability of the power module and die bonding quality. Finally, the contributions of this dissertation research and recommended future work are given in Chapter 9.

Chapter 2. Literature Review

2.1 Introduction

This chapter introduces the current status of packaging technologies for double-sided cooling power module. The directFET™, flip chip solder ball and solder bump technology, press pack technology, GE power overlay technology and embedded power technology will be discussed.

2.2 Existing Packaging Technologies for Double-sided Cooling Applications

2.2.1 DirectFET™ Technology

DirectFET™ developed by International Rectifier is the first commercialized double-sided cooling module [5].

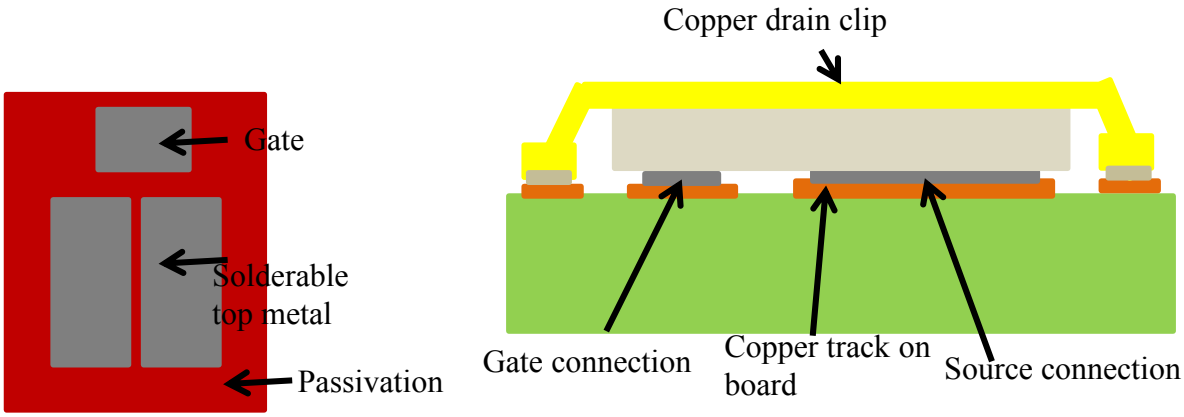


Fig. 2.1 DirectFET™ module architecture and forced air with additional cooling fins [5]

Fig. 2.1 shows the passivation system in conjunction with a MOSFET die with solderable top metal contacts. The passivation layer separates the source and gate pads on the top of the die and acts as a solder mask to protect the gate and sources from being shorted. A copper clip is then soldered directly to the MOSFET drain region and brings it into contact with the lead frame. The large surface contact reduces the conduction losses and improves the thermal dissipation. Since the only material between the junction of the die to the printed circuit board is the copper strap and solder alloy is used to bond them to the board, the thermal resistance between the junction to

the board is significantly reduced. Due to the planar structure of the top side of the packaging, extra heat sink could be used on top of the copper strap to facilitate the top side cooling.

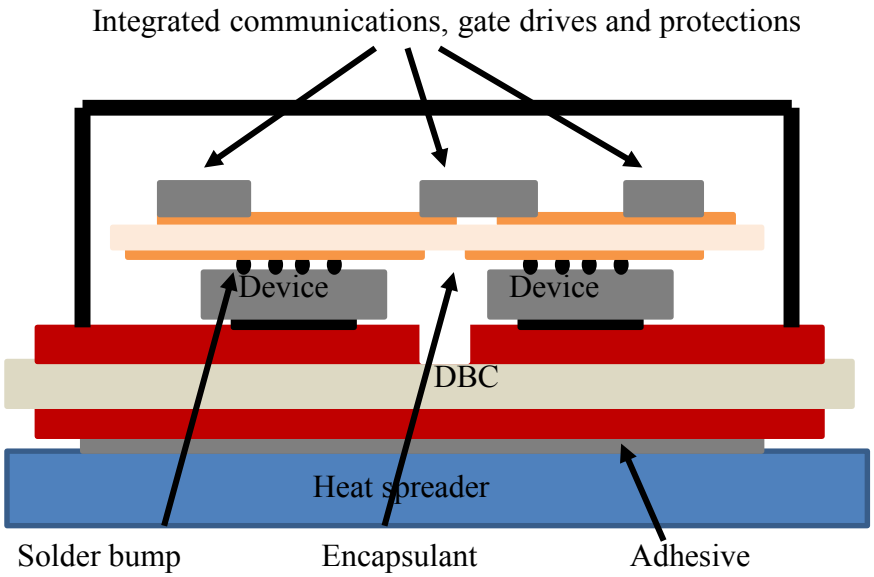
2.2.2 Flip Chip Solder Ball Interconnection Technology

In [6], a Power Ball Grid Array (PBGA) module is introduced. In the PBGA structure, the power semiconductors are soldered between two pieces of DBCs. While the bottom side of the collector was soldered to the bottom DBC through large area contact, the top gate and emitters region were contacted to the top DBC by a large number of solder bumps to improve the high current carrying capability as shown in Fig. 2.2 (a). The bumps on the top surface have a diameter between 200 to 250 μm. With a die size of 4.5 mm×7 mm, there are around 90 to 170 bumps on the die top surface. The module was reported to have a higher process efficiency, a reduced drain-source resistance, a lower parasitic inductance and a better thermal dissipation, and lower heating of the leads due to the large area solder connection. In [7], the flip chip double-sided cooling module was sandwiched between microchannel heat sink to further decrease the thermal resistance of the package. The resulting module is a very compact structure with a good thermal performance.

Flip chip on flex is a high density low profile power stage structure shown in Fig. 2.2 (b) [8][9]. In this structure, the power devices with solder balls are soldered onto the top side flexible substrate, which is made of a polyimide film bonded to copper. The bottom sides of the devices are soldered to the DBC substrate with appropriate patterns to realize the electrical connection and form the thermal path as well as to improve the mechanical strength of the package. Underfill was used as an adhesion material as well as a stress distribution material to enhance the ruggedness and reliability of the module. The gate drivers and other integrated communications are mounted on top of the flex board to achieve an integrated module. This packaging style

eliminated the bonding wires and allowed for the higher frequency operation with reduced size and cost. The double-sided cooling could be enabled by rearranging the structure.

(a)



(b)

Fig. 2.2 (a) IGBT with solder balls on chip and (b) Flip chip on flex power stage structure [10]

In order to reduce the thermal stress in the solder bump caused by the CTE mismatch, the influence of different shapes of the solder bumps were investigated. In [11], a stacked assembly with substrate-chip-bump-chip-substrate was made using latest generation of Infineon Technologies® 70 µm thin IGBTs and diodes as shown in Fig.2.3. The simulation results reveal that the thickest AlN based DBC substrate offers the best thermal performance while the thinnest Si_3N_4 based DBC substrate generates the lowest thermal stress in the solder critical point. The

effect of bump shapes has the least influence on the thermal performance.

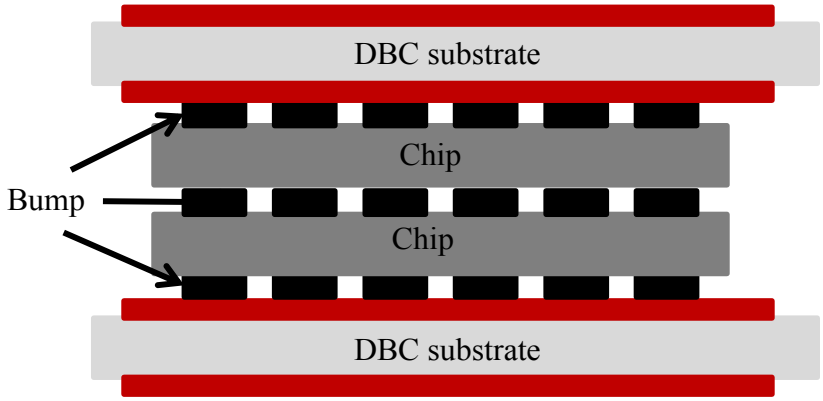


Fig. 2.3 A stacked assembly of substrate-chip-bump-chip-substrate for the bi-directional switch cross section view [11]

2.2.3 Press Pack Technology

Press pack is another wire bondless interconnect technology originally developed by Fuji, Toshiba and ABB [12] [13]. In press pack packaging, external applied pressure was used to contact the die to eliminate the bond wires. Thus, the thermal stress caused by the temperature variation and parasitic inductance generated by the bond wires is absent. Individual press-pins were used to connect the die gate and source metal pad to the external terminals via a planar distribution board with carefully designed series impedance to the die to ensure a homogeneous switching. Press pack structure allows for easy series and parallel configurations to increase voltage and current capabilities, and it has a better overall performance but high cost. A 4.5kV 2000A press pack IGBT module was presented in [14]. In order to eliminate the damage on the delicate die top surface when installing modules into the coolers, individual spring unit was used to contact the chip as shown in Fig 2.4. By accurately controlling the spring constant tolerance and travel distance, the internal force of each spring unit can be controlled well and press homogeneity will not cause the damage of the die. Under the short circuit situation in HVDC

application, the failed modules should be still carrying the load current. A metal plate made of Ag or Al shown in Fig. 2.4 was used to contact the silicon chip. The high energy during short circuit could melt the metal and form a stable alloy on top surface of the chip and allows for the current flow through it.

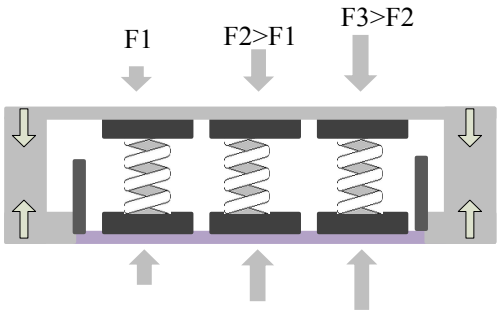


Fig. 2.4 IGBT chips with individual spring unit [14]

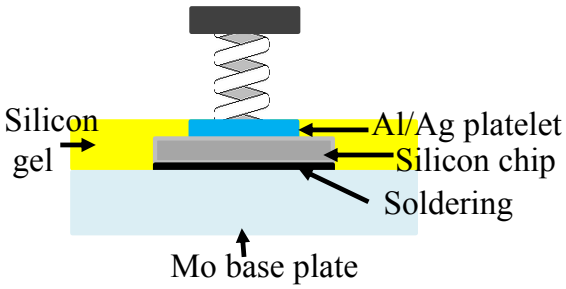


Fig. 2.5 Cross section of press pack chip contact layers [14]

2.2.4 Metal Post Interconnected Parallel Plate Structure (MPIPPS)

Metal-Post Interconnected Parallel Plate Structure (MPIPPS) is a planar packaging technology originally developed by CPES (Center for Power Electronic System) in 1999 [15][16]. This structure uses a thick copper post with low DC resistance instead of bond wire to connect the top die metal pad to the top DBC substrate. The power devices IGBT and diode are soldered on the top copper layer of patterned bottom DBC substrate followed by the soldering of the copper posts on top of the device metal pads. When soldering the copper posts on the power device metal pads, the copper posts with dimension of 1 mm length x 1 mm width x 2.5 mm thickness

are first carefully positioned onto a sticky tape, and then flip over and stack onto the solderable metal pads of the power device followed by the reflowing in an oven in a nitrogen atmosphere. These copper posts have different sizes and heights to compensate for the size and thickness of the different power devices used. The top DBC is patterned to contact the top side of the copper post and to make the electrical connection. The MPIPPS structure provides the potential for double-sided cooling, and the ability of removing heat from the parallel plates by flowing a dielectric fluid between the plates.

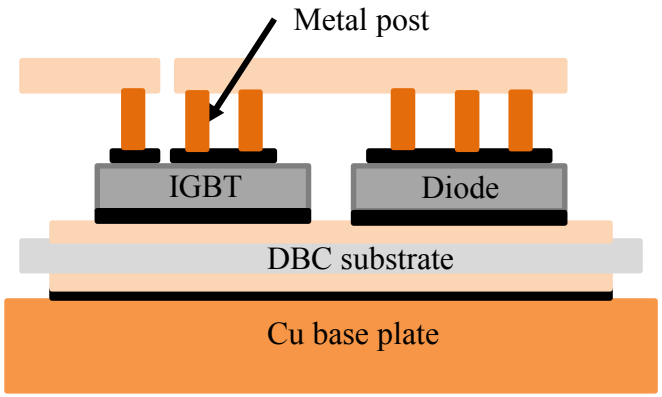


Fig. 2.6 Metal post bonding concept for power module assembly [15]

2.2.5 Power Overlay Technology

Power Over-Lay (POL) developed by GE is a high density packaging technology with low parasitic, low weight and smaller size [17][18][19]. Fig. 2.8 shows the cross section of the POL structure. The design of POL eliminates the bond wires, and uses a metallization layer through holes to realize the interconnection of the device pad. As a result, the interconnection length, and parasitic are reduced dramatically compared to the wire bonded structure. Another advantage of removing bond wires and using chip on flex feature is the capability of employing double-sided cooling method and reducing the thermal resistance from the junction to the ambient.

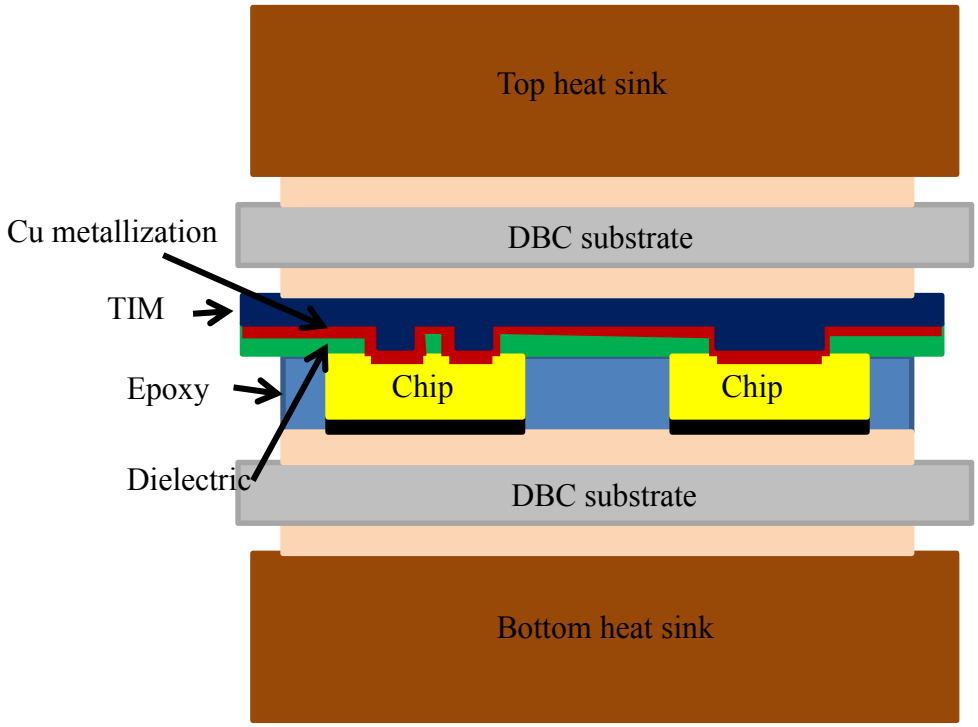


Fig. 2.7 Cross section of GE Power Overlay structure [17]

Several 50 μm thick polyimide films with low modulus and low CTE are laminated to form a 200 mm diameter carrier layer with a working area with a diameter of 150 to 170 mm. A partially cured B-stage bond layer such as acrylic or epoxy resin with a 12 μm thickness is attached to the carrier layer. The power devices top side is mounted to this partially cured B-staged bond layer with vias of diameters between 20 mils to 50 mils formed by mechanical punching or lazer machining. These power devices are attached face down onto the adhesive layer with the metal pad of the chips aligned with each via on the bottom side.

The adhesive is then cured in the oven with required temperature, vacuum and pressure to achieve the bonding of the power chips with dielectric sheet. In order to remove the resin that has been squeezed into the vias during adhesive curing process, RIE or sputter cleaning of the glue and the thin aluminum oxide layer from the metallization of the devices is used. After cleaning, a seed metal layer Ti and Cu for adhesion and conduction is sputtered over the surface of the

device top through vias. Subsequent copper plating would deposit 50 μm to 150 μm metal to improve the current handling capability. The seed layer functions not only as an adhesive layer to strengthen the bonding with the plating copper but also as a barrier to stop the metal diffusion to the polymer. Subsequently, the blanket copper layer is patterned using photoresist to form the desired interconnect structures. In order to attach the control circuit and/or their I/O pad, other solderable metal such as Ni: Au or Ni: Ag is electro-less plated over the patterned copper layer. The next step is the cutting of the half packaged devices from the carrier frame mechanically or by laser and attached to a high performance substrate such as DBA or DBC. An underfill material is then dispensed to wrap around the power chips in order to release the thermal stress and protect the power chips from electrical breakdown under working conditions. Due to the usage of the underfill, the operation temperature of the POL is limited to be below 150℃.

2.2.6 Embedded Power Technology

Embedded Power is another interconnect strategy that used metal deposition method to conduct the current and heat flux [20]. Different from POL which uses the polyimide films as the die top bonding layer, the embedded power uses screen printable material applied on the top surface of the device as the dielectric material to separate the gate and source pad and to further improve the voltage blocking capability. A smooth solid layer Enthone® DSR-3241 liquid photoimageable solder mask was used to improve the adhesion between the printed material and the metal material used in the following step. Physical vapor deposition (PVD) or sputtering is used to deposit a thin layer of titanium and copper on the top side of the device and liquid photoimageable solder mask. Copper electroplating is then used to further increase the thickness of the metal layer to enhance the current carrying capability. After electroplating, a dry film process was used to make the connection pattern and etch the unnecessary metal layer to form

the I/O pads. The assembly is attached to the bottom patterned DBC substrate using a solder paste. In order to insulate the top layer from the top cooling equipment, another layer of liquid photoimageable solder mask was employed and the electrical isolation was realized.

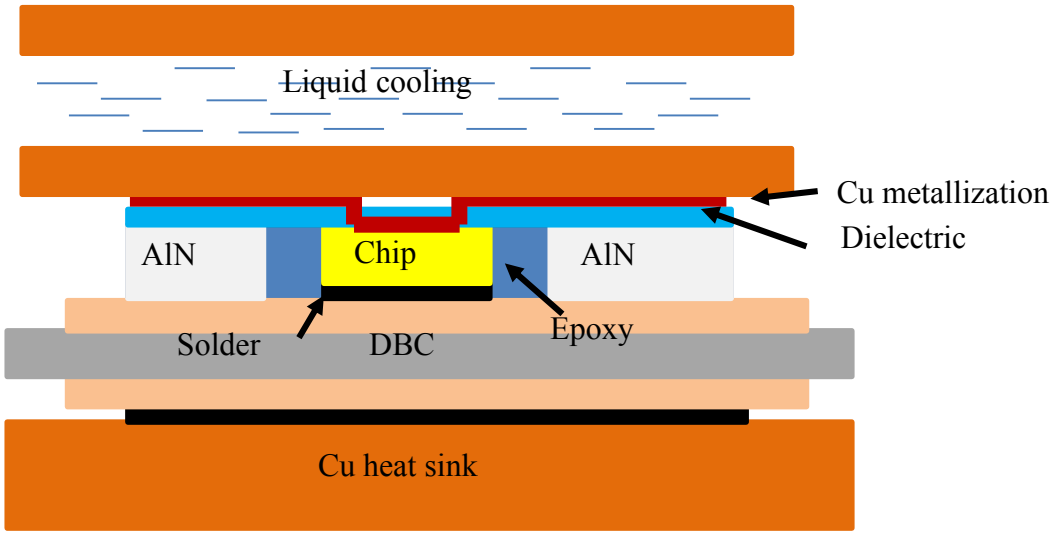


Fig. 2.8 Embedded power structure cross section view [20]

2.3 Summary

The double-sided cooling is the trend for the power electronics packaging, with the potential ability to improve thermal performance, reduce parasitics of the power electronic modules. The current existing double-sided cooling module technologies of directFET®, flip chip on flex, power overlay and embedded power are reviewed. In flip chip and power overlay structure, the underfill limits the operation temperature to be below 150°C. The polyimide and epoxy in embedded power packaging are the materials that are not appropriate for high temperature application.

Chapter 3. Proposed LTCC based Double-sided Cooling Power Module

3.1 Introduction

The schematic cross section view of the LTCC double-sided cooling module structure is presented in Fig.3.1. The low temperature co-fired ceramic (LTCC) layer is used as the dielectric material between the bottom and top DBC substrates. The LTCC is a high temperature dielectric material, and furthermore, cavities and thermal and electrical vias can be easily formed. A die bonding material is used to attach the bare dies to the DBC substrate. The base plate is removed from the module structure to reduce thermal stress induced by the bimetallic effect and the thermal resistance between junction and ambient. The double-sided DBC structure provides a mechanical balanced structure to enable double-sided cooling capability for a better thermal performance. Figure 3.2 shows the exploded view of the LTCC based double-sided cooling module.

One of the biggest challenges for this LTCC based double-sided cooling power module is to choose the proper materials for high temperature application. For the die attachment material, high temperature solder alloys or micro/nano silver paste, and transient liquid phase bond are the

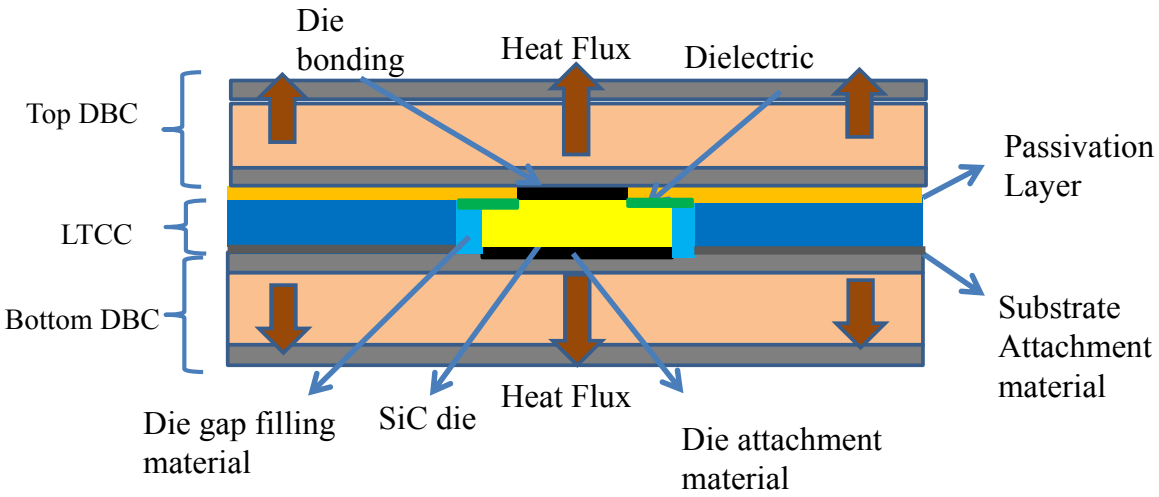


Fig. 3.1 Proposed LTCC based double-sided cooling module cross section

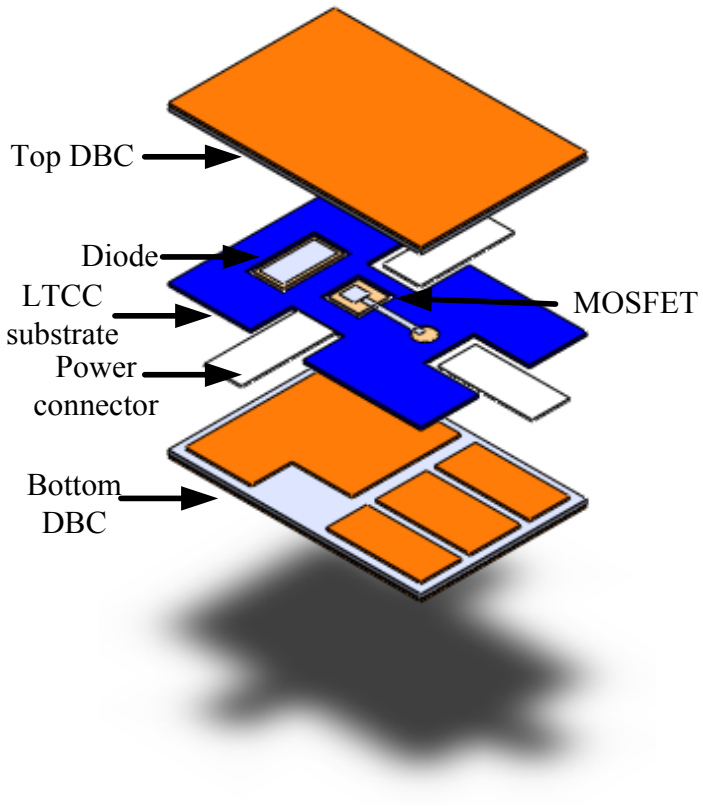


Fig. 3.2 Exploded view of the LTCC based double-sided cooling module

potential candidates. Compared to the solder alloys, micro/nano silver die attach has high thermal and electrical conductivities and can operate up to 961℃ after sintering. The lower Young's modulus of nano silver die bonding with a porosity structure reduces the thermal stress compared to the solder alloy and pure silver material. Due to the small size of the nano silver particles, its sintering pressure is reduced compared to micro sized nano silver particles. For the substrate material, high thermal conductivity and high temperature operation materials such Al_2O_3 or AlN DBC are good candidates. An adhesive layer is used to bond the LTCC substrate with the bottom DBC substrate to improve the integration and robustness of the entire assembly. A high temperature operation is also required for this material. High temperature material with a CTE similar to the power devices and substrate are required to fill the gaps between the bare die and LTCC substrate to protect the die from voltage breakdown. A high dielectric strength

passivation layer was applied to the top DBC bottom surface except the regions where the metal pads of the power devices are attached. This passivation layer fills the air gaps between the top DBC and the die edge region and ensures there is no electrical breakdown in the package. Before the assembly of the top DBC substrate, the power connectors are attached to either the top or the bottom DBC substrate in such a way that the power connectors are protruded out parallel to the DBC substrate and the electrical connections are realized by the conductor pattern on the DBC substrate. The final module has a reduced size and weight, and an improved electrical and thermal performance compared to the traditional wire-bonded counterpart.

3.1.1 Challenges for High Temperature Double-sided Cooling Power Modules

The requirement of the proposed high temperature double-sided cooling module with planar packaging brings several challenges of the module design and packaging technologies. First of all, the elimination of the bond wires and the usage of the direct die bonding reduce the die spacing between the highest and lowest voltage potential. As a result, the electrical field distribution inside the dielectric material will be redistributed and the maximum electrical field intensity will be increased which may lower the breakdown voltage of the double-sided cooling power module. Secondly, the high temperature operation may cause the premature failure of some of the packaging materials such as solder alloy, dielectric material and encapsulant material. The available materials and packaging technologies for high temperature operation are limited. Thirdly, the thermal stress caused by the mismatch of CTE of different materials inside the module is extremely large under high temperature environment and double-sided DBC structure. The reliability of the power module is affected by the high stress induced inside the package, especially under passive thermal cycles. As such, the selection of appropriate packaging materials and designing of the proper packaging fabrication process to package the selected

components are of great importance to a successful high temperature double-sided cooling power electronics module.

3.2 Material Selections

3.2.1 Semiconductor Devices

Semiconductor devices with smaller structure and more precise process control as well as more complex technologies are reaching the physical limits of silicon in power electronics industry. In recent years, wide band-gap materials such as silicon carbide (SiC) and gallium nitride (GaN) are attracting great attention in the power electronics field. Compared to silicon, these wide band gap devices display many attractive material properties due to the higher energetic gap between valence and conduction bands. Table 3.1 lists the key material properties for these semiconductors [21]. Compared to the Si devices, the power semiconductors made from SiC or GaN have low losses, high breakdown voltages, higher power densities, higher operating temperatures, and higher switching frequencies over conventional Si devices.

Table 3.1 Key material properties of Si, SiC and GaN [21]

Parameters	Sign	Unit	silicon	Silicon carbide	Gallium Nitride
Band gap energy	E_g	eV	1.12	3.26	3.39
Intrinsic density	n_i	cm^{-3}	1.4e-10	8.2e-9	1.9e-10
Breakdown field intensity	E_c	MV/cm	0.23	2.2	3.3
Electron mobility	μ_n	cm^2/Vs	1400	950	1500
Drift velocity	v_{sat}	cm/s	10e7	2.7e7	2.5e7
Dielectric constant	ε_r	-	11.8	9.7	9.0
Heat conductivity	λ	W/cm·K	1.5	3.8	1.3

3.2.2 Interface Bonding Methods

3.2.2.1 Soldering

Soldering is the bonding process to attach two metal material through melting of metals or metal alloy. When heating the solder material up to its reflow temperature, the atoms inside the solder diffuse into the metal surface and a thin layer of bonding interface alloy will be created. In order to achieve void free bonding, the surface of all bonding components involved should be cleaned and be free from oxide. Apply vacuum as soon as the solder is liquefied is an effective way to stop the void from forming inside the solder layer. Nowadays, programmable vacuum chamber is available to reflow solder material and achieve a high quality void free bonding layer. Most of the solder pastes contain flux agents, which will be activated and clean the surface and protect the surface from re-oxidation when they are warmed up. However, the drawback of all solder flux residues and flux condensates is the cost of cleaning and rework efforts.

Due to the regulations of Restriction of Hazardous Substances Directive (RoHS) of the European Union, the high lead solders are being eliminated from the market. The knowledge for using SnAg and SnAgCu solder for the die attachment in DBC substrate such as soldering process and equipment is well established in the industry recently. However, the limitations of the soldering process such as the joint degradations, high temperature restriction prevent it from some high power density applications.

3.2.2.2 Diffusion Sintering

Diffuse sintering is a process that is superior than soldering in terms of thermal and electrical performance as well as its long term reliability. Typical processing temperature for nano silver paste sintering is between 200℃ and 275℃ with pressure various from 1 to 5 MPa [22]. Due to the high volume percentage of organic contents, sintering process usually takes a long time and the thickness of the bonding layer shrinks after the sintering process. The major advantage of sintered nano silver paste is its high resistance to temperature cycling compared to solder,

especially at high temperatures [23]. Table 3.2 shows the comparison of some material properties of SnAg solder and sintered nano silver paste. Besides the electrical and thermal material properties, homologous temperature is another important parameter to demonstrate the material property at elevated operation temperature. Materials are not weakened by temperature when this value is below 40%, and between 40% to 60%, materials are susceptible to mechanical stress. When this value is larger than 60%, the material strength decreases considerably and the material is not suitable for the application. From Table 3.2, SnAg solder is obviously not an appropriate material for 200 ℃ applications. The sintered nano silver paste is the bonding material of choice up to 350°C. Nano silver attach is adopted in this work since it has been used in the industry [24].

Table 3.2 Comparison of SnAg solder and sintered nano silver paste

Property	Solder alloy Sn96.5Ag3.5	Sintered nano silver paste
Melting point (°C)	221	961
Heat conductivity (W/m·K)	70	240
Electrical conductivity (MS/m)	8	41
Typical thickness (μm)	90	20
Thermal expansion coefficient (ppm/°C)	28	19
Homologous temperature at 200°C	95.7%	38.3%

3.2.2.3 Diffusion Bonding

Diffusion bonding is also called eutectic soldering or transient liquid phase bonding (TLPB). It is a thicker high melting temperature metal layers. The resulting homogeneous joint alloy has a higher melting temperature than the previous metal alloys [25]. During the TLPB process, the medium temperature solder alloy is put between thick metal alloys first and then is heated up to its melting point. The liquid phase alloy is then diffused into the thick metal layer on both sides and the intermetallic phases with high melting points are formed during processing. As an example in a CuSn system, Cu_3Sn with a melting point of 676℃ and Cu_6Sn_5 with a melting point

of 415℃ are formed. Due to its high melting point of the intermetallic die attach layer, the reliability of such system is improved compared to solder attach, which is proven for operation temperature up to 170℃ [26]. Table 3.3 lists the key material properties for state-of-the-art die attach methods.

Table 3.3 State of the art die attach methods

Parameters	Thermal conductivity (W/m·K)	CTE(ppm/°C)	Processing temperature (°C)	Melting point (°C)
Tin-lead solder	28	28	220	183
Lead free solder	-20	20	265	224
TLPB	-	-	-	~400 for Cu/Sn
Sintered micro silver paste	250	19	250	961
Sintered nano silver paste	290	19	275	961

3.2.3 LTCC Interconnect Substrate

LTCC is a low temperature co-fired ceramic technology for multilayer circuits using multiple green tapes. These green tapes are provided by different commercial suppliers with slightly different material parameters, such as dielectric constant k, the permittivity ε, CTE, insertion loss, etc. The major green tape suppliers are Dupont, Heraeus, Ferro, ESL, and CeramTec [27]. Unlike HTCC (High Temperature Co-fired Ceramic) technology, LTCC has a much lower firing temperature at about 850℃ which is almost half of the HTCC firing temperature. This makes it possible for LTCC to use low resistivity conductors such as gold, silver and copper, and alloys instead of using high melting temperature metals such as tungsten and molybdenum.

The fabrication process of LTCC is similar to that of HTCC and all of the different layers are processed in parallel, resulting in a reduced cost and effective yield because each process is independent to the previous process step [28]. The process includes tape blanking, via punching,

via filling, conductor printing, stacking, lamination, scribing, burnout, co-firing, and singulation [29]. Compared to other organic materials for electronic packaging, LTCC has a higher reliability. It is easy to achieve different thicknesses by laminating different numbers of green tapes together, and cavities are easy to make inside the substrate. Furthermore, some passive elements like capacitors, inductors and resistors can be easily created in the substrate. The CTE of LTCC matches with SiC devices well, and the operation temperature is much higher than the normal application.

3.2.4 Sealing Material

Nusil R-2187 is a high temperature silicone with a low curing temperature. It can work at 314°C continuously after cured at 70°C for two hours in the oven. Common defects such as delamination, wraping and bowing can be avoided when curing at low temperature when the bonded materials have different CTEs. Table 3.4 lists the physical properties of R-2187. As can be seen, this material has a high tensile and tear strength. Meanwhile, due to its high flexibility, it can absorb stress during temperature cycling process. They can work with maintained electrical and mechanical properties from -200°C to 314°C. This adhesive has a mix ratio of 10:1 (part A: part B) and they are easily dispensed and de-air. Another sealing material used is the Resbond 920 material which is a white paste based on Al_2O_3. This adhesive is electrically resistant and thermally conductive and is formulated with different binders which have various properties. These special binders maintain their high electrical resistance and dielectric strength up to 3000°F. Resbond 920 can be used to seal light bulb fixtures, bond high temperature resistors and some other instrumentation etc [30]. Table 3.5 lists the physical properties of Resbond 920 [31]. Resbond 920 has a similar CTE to SiC and AlN which will induce a smaller thermal stress at high temperature. Additionally, it provides a dielectric strength of 10.6kV/mm, which is high

enough for medium or low voltage applications. The application process for Resbond 920 includes mixing it with water at a ratio of 100:14 by weight. Then paste mixture can be applied into the sealing gap between the chip and the LTCC substrate. It is then cured at 120°C for 2 hours in oven.

3.2.5 Substrate Material

The substrate serves as an insulation layer to isolate the circuit part from the outside layer and provides the path for the heat to dissipate from the power devices to the heat sink or the ambient.

Table 3.4 Physical properties of Nusil R-2187

Material properties	value
Viscosity	23,000 cP (23,000 mPas)
Specific Gravity	1.12
Tensile Strength	790 psi (5.4 MPa)
Elongation	175%
Tear Strength	50 ppi (8.8 kN/m)
Maximum operation temperature	314°C

Table 3.5 Physical properties of Resbond 920 [31]

Continuous Use Temp. (°F)	3000
Base	Al_2O_3
Form	Paste
Compressive Strength (psi)	4500
Flexural Strength (psi)	450
Thermal Expansion ($x10^{-6}$/°C)	4.5
Thermal conductivity (W/m·K)	26
Dielectric Strength (kV/mm)	10.6

Often times, the surface flatness is an important parameter for a good substrate since the need of coating thin films, attaching dies and bonding wires. Direct bonded copper (DBC) is a widely used substrate in power electronic packaging. It has two layers of high purity copper that are directly bonded onto an aluminum nitride (AlN) or aluminum oxide (Al_2O_3) ceramic base. By

the combination of different thicknesses of copper and ceramic and ceramic type, the CTE of the DBC can be adjusted in order to match the CTE of the system. Al_2O_3 is a cheap and common ceramic material for the DBC. However, the thermal conductivity and CTE mismatch with SiC devices makes it not the best option for the power electronic modules. AlN DBC is a promising substrate material since it has a high thermal conductivity and a similar CTE with SiC die and its mechanical properties are adequate for the high power applications [32].

Direct bonded aluminum (DBA) is another type of substrate for electronic packaging and has been developed for high temperature applications. Compared to the DBC substrate, DBA has a remarkably higher temperature cycling capability, which leads to a significant improvement in reliability, especially in harsh environment [33]. The drawback of this substrate is that the surface roughness will be increased after the high temperature operation or cycling as well as its high cost in the market [34]. Si_3N_4 is a new substrate material for the power electronic packaging and is known for its high reliability. Its thermal conductivity is on the average level, however, its CTE matches well with SiC devices and it has a very high mechanical fractural toughness. It has 850 MPa of flexural strength and 5 MPa$\sqrt{m}$ of fracture toughness, compared to Al_2O_3 with 274 MPa of flexural strength and 3.3 MPa$\sqrt{m}$ of fracture toughness, and AlN with 400 MPa of flextural strength and 2.7MPa$\sqrt{m}$ of fracture toughness [35]. Kyocera's active metal brazing (AMB) technology is based on Si_3N_4 and uses silver-copper-titanium metallization system to actively braze Si_3N_4 ceramic to copper, which yield a much stronger substrate than the conventional Al_2O_3 or AlN DBC substrate [36]. Table 3.6 lists the CTE, thermal conductivity and modules of elasticity of common substrate materials.

Table 3.6 CTE, thermal conductivity and modules of elasticity of common substrate material

Material	CTE (ppm/°C)	Thermal conductivity (W/m·K)	Modulus of Elasticity (GPa)
Copper	17	400	1170
Al_2O_3	7	26	370
AlN	4.5	170	330
BeO	7	270	345
Al	23.1	208	70
Si_3N_4	3.3	30	304
SiC	4	120	420
Resbond 920	4.5	26	70

3.2.6 Passivation Material

The traditional passivation material used for the semiconductor device surface passivation include oxide deposited layer covered with glass, inorganic dielectric such as SIPOS (Semi-insulating polycrystalline silicon) or organic dielectric such as nitride, silicon rubber, polyamide as well as polyimide etc. [37]. These polymer materials have several advantages for the passivation application. Normally, they are inert, pinhole free, good adhesion with metals, composites, plastics, elastomers, and ceramics. Parylene HT is a high temperature parylene polymer that achieves a thermal capability up to 400°C [38]. Besides the important material properties shared with traditional Parylene such as excellent gap filling capability and uniform pinhole free coverage, Parylene HT has a lower dielectric constant, higher thermal stability at higher temperature and low moisture absorption. However, the application process of Parylene HT requires a special coating system and availability of the coating equipment and process control limits its wide application. Polyamide imide (PAI) is well known for its low thermal expansion coefficient, high heat resistant and better process ability and relative low curing temperature [39]. It has been widely used as an inter-dielectric material and electrical insulator in large scale integrated circuit industry due to its high dielectric strength reported between

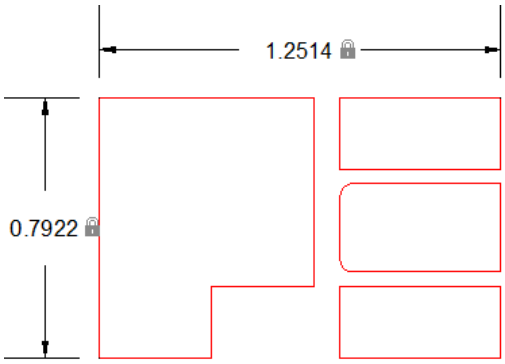
100kV/mm to 280kV/mm and its wide operation temperature between -200°C and 260°C [40].

3.3 Parasitic Inductance Consideration of the LTCC based Double-sided Cooling Module

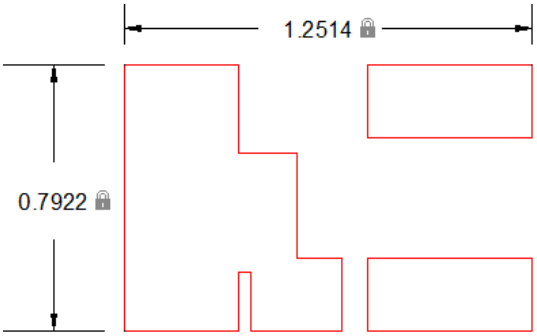
Interconnection parasitic inductance has detrimental impacts on power device switching characteristics. When there is current flowing through the circuit, parasitic inductance can store energy. When the device is switching off, the stored energy is released and voltage spike occurs which leads to the voltage overshoot and energy loss and even the breakdown of the dielectrics [41]. The spike voltage is a function of inductance and the rate of current change di/dt. With continuously increasing switching frequency of the power electronics, di/dt becomes larger at higher frequencies [42]. In order to reduce the voltage spike, improve the switching characteristics and long-term reliability, the parasitics of the packaged modules should be reduced to their minimum.

3.3.1 Layout Design

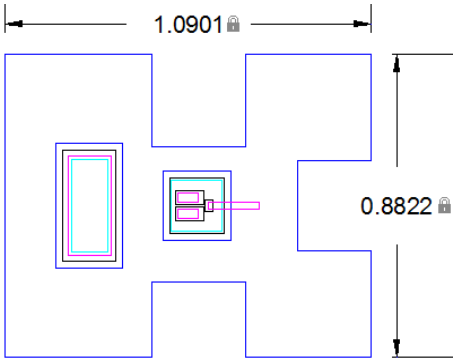
The layout design of the module is used to realize the electrical and physical connections for the module assembly. The detailed dimensions for both the top and bottom DBC layers and LTCC substrate are required and must be carefully considered from the system level. Fig. 3.3 shows the layout design of the LTCC based double-sided cooling module. The major components for this module include an Al_2O_3 DBC with Ag plating, a LTCC substrate with cavities and vias, power semiconductor devices and materials used for bonding and passivation. In order to minimize the parasitic inductance and improve the thermal performance of the package, the top and bottom sides of the DBC are in direct contact with the power devices metal pads. The total foot print of the layout for a single switching position of a SiC MOSFET and its anti-parallel diode is 1.25 "╳0.79".



(a) Bottom DBC layout



(a) Top DBC layout



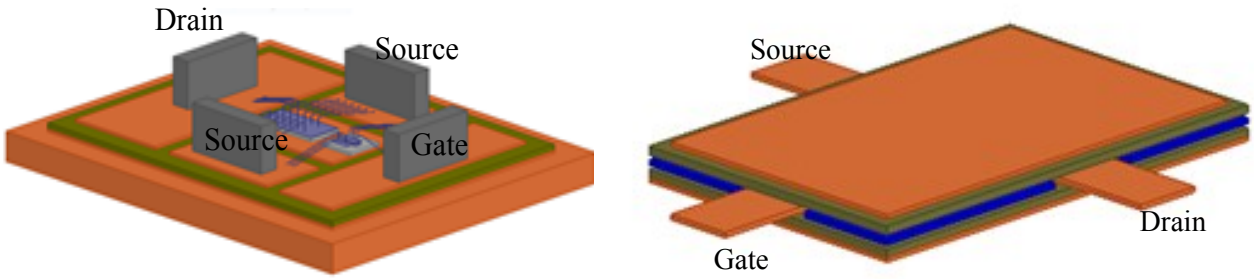
(C) LTCC and devices position layout (unit: inch)

Fig. 3.3 Layout design

3.3.2 Parasitic Inductance Simulation

In order to investigate the parasitic inductance induced by the module packaging, a Q3D 11 extractor was used to simulate the parasitic inductance between the terminals of the conductive paths for both the LTCC based wire-bondless module and wire-bonded module. Fig. 3.4 shows

the simulation models for the wire-bonded and wire-bondless modules.



(a) (b)

Fig. 3.4 Q3D model for parasitic inductance simulation (a) wire-bonded (b) wire-bondless model

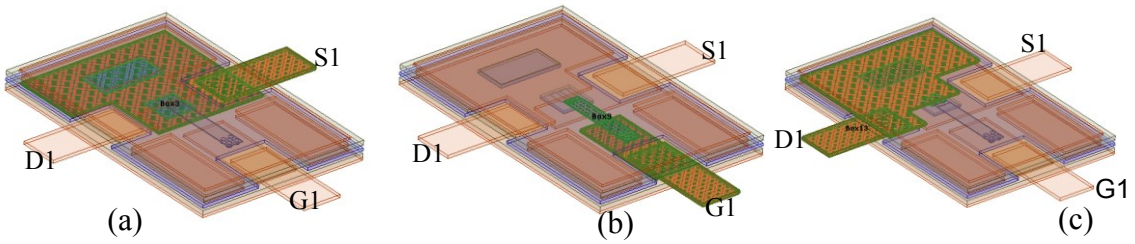


Fig. 3.5 Three nets assigned for the parasitic inductance simulation for wire-bondless model (a) source path (b) gate path (c) drain path

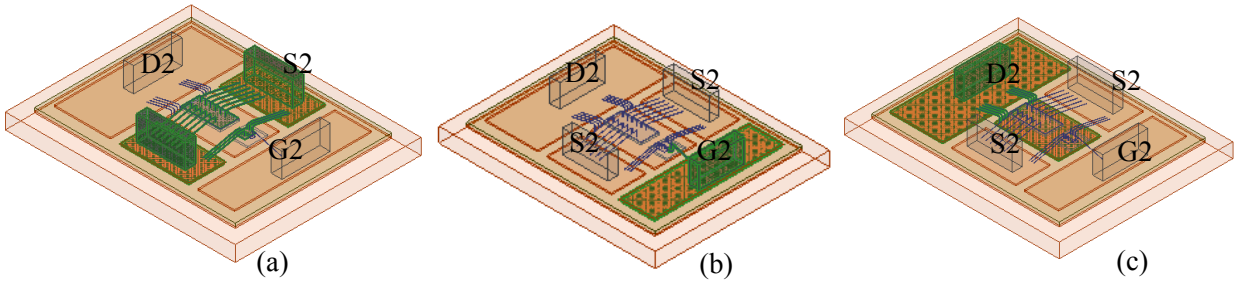


Fig. 3.6 Three nets assigned for the parasitic inductance simulation for wire-bondless model (a) source path (b) gate path (c) drain path

Figs.3.5 and 3.6 show the nets for wire-bondless module and wire-bonded modules, respectively. Fig. 3.5 (a) shows the path from the power connector end to the DBC copper trace and then to

MOSFET source and diode anode. Fig. 3.5(b) shows the gate power connector end through vias and DBC trace to the gate metal pad of the MOSFET, and Fig. 3.5 (c) shows the source power connector end through bottom DBC copper trace to the drain of the MOSFET and cathode of the diode. Fig. 3.6 shows the three nets for the wire-bonded module. Fig. 3.6 (a) shows the path of two source power connector ends to the source of MOSFET and anode of the diode. Fig. 3.6 (b) shows the gate power connector end through bond wire to the gate metal pad of the MOSFET, and Fig. 3.6 (c) shows the drain power connector to the cathode of the diode and drain metal pad of MOSFET.

Table 3.7 Inductance matrix for the wire-bondless module (DC RL) unit=nH

Terminal	D1	G1	S1
D1	0.952	-0.29	0.189
G1	-0.29	7.266	0.41
S1	0.189	0.41	1.541

Table 3.8 Inductance matrix for the wire-bondless module (AC RL, Freq=1GHz) unit=nH

Terminal	D1	G1	S1
D1	0.368	-0.098	0.002
G1	-0.098	3.285	0.106
S1	0.002	0.106	0.53

Table 3.9 Inductance matrix for the wire-bonded module (DC RL) unit=nH

Terminal	D2	G2	S2
D2	1.679	0.127	-0.161
G2	0.127	9.281	0.295
S2	-0.161	0.295	3.752

Table 3.10 Inductance matrix for the wire-bonded module (AC RL Freq = 1GHz) unit=nH

Terminal	D2	G2	S2
D2	1.28	0.237	-0.225
G2	0.237	7.138	-0.065
S2	-0.225	-0.065	2.491

The parasitic inductance results from the Q3D extractor analysis on the wire-bonded module are listed in Table 3.7 and 3.8 for DC and AC circuits, respectively. Table 3.9 and 3.10 are the DC and AC results for the wire-bondless module. The diagonal elements from Tables 3.7 to 3.10 are self-inductances, and the non-diagonal elements are mutual inductances between two different conductor paths. From these results, all the self-inductances are larger than the mutual inductances in each model. In both DC and AC, the self-inductances of the conductive path for wire-bondless module are smaller than those of the wire-bonded module. The self-inductance is nearly a constant value in terms of frequency. The total self-inductances for the wire-bondless module are 8.62nH and 4.17nH for DC and AC, respectively. Values for the wire-bonded module are 14.01nH and 10.90nH for DC and AC cases. The AC self-inductance is lower than DC self-inductance due to that the skin effect reduces the magnetic fields as well as the corresponding stored inductive energy inside the conductors. The total self-inductance of the wire-bondless module is considerably smaller than the package with wire bond technology.

3.3.3 Parasitic Inductance Measurement

In order to validate the simulation results of parasitic inductance for the power modules, a time domain reflectometry (TDR) was used to measure the parasitic inductances of the wire-bonded module. The TDR method involves propagation of a high frequency step signal (incident signal) through the conductive path and capturing its reflected signal. The absolute parasitic values can be computed by comparing the differential inductance waveforms. Since this method can only measure the parasitic inductance in a conductive path, the parasitic inductance between the two source power connectors was measured to compare the result to the simulated value.

Fig. 3.7 shows the wire-bonded module for the parasitic inductance measurement. Fig. 3.8 shows the measurement result of 5.64nH after calibration. Compared to the simulated value of 6.04nH,

the error between the simulation result and the measurement result is about 6%.

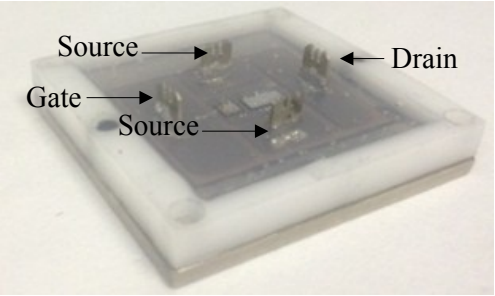


Fig. 3.7 Wire-bonded equivalent for parasitic inductance measurement (photo by author)

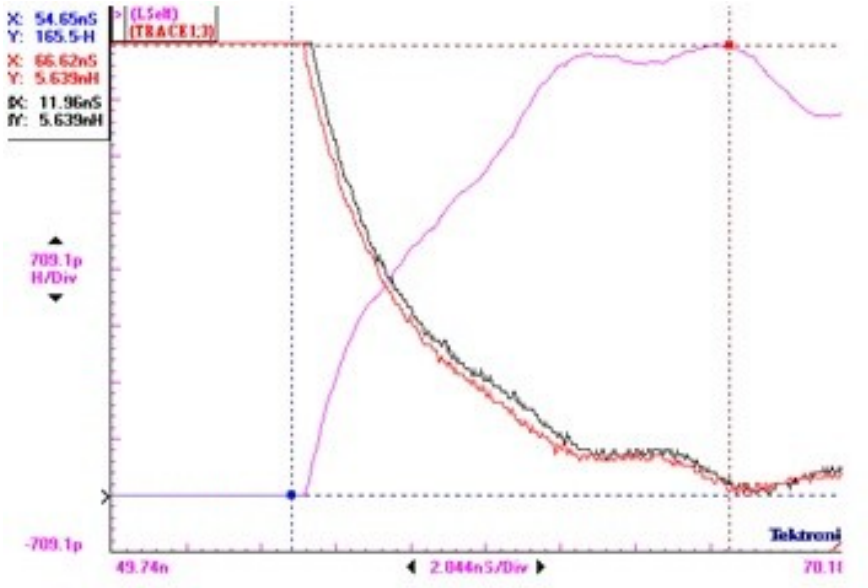


Fig. 3.8 Measurement of parasitic inductance between two source connectors

3.4 Summary

In this chapter, a high temperature LTCC based double-sided cooling power module with planar packaging was proposed and introduced. The different materials for the module application, such as substrate materials, sealing materials and die bonding materials, were discussed. In order to achieve a low thermal stress generated by the temperature variations, the base plate was removed from the structure. Parasitic inductances of the proposed double-sided cooling module and traditional wire-bonded module were extracted using Q3D extractor version 11.0. The parasitic

inductances for the wire-bondless module are 9.76nH and 4.18nH for DC and AC, respectively, compared to 14.71nH and 10.9nH, respectively, for the wire-bonded module. A TDR measurement was used to validate the Q3D simulated parasitic inductance values.

Chapter 4. Analysis of Thermal Performance of the LTCC based Double-sided Cooling Module

4.1 Introduction

Thermal simulation is of great importance at the early stage of the power module design since it can help to compare different designs, address design issues comprehensively and quickly, and optimize the design without the high cost of developing physical prototypes. It also allows the engineer to fully understand the thermal performance of the power module and the thermal dynamics of the heating and cooling processes as well as to design a good thermal management system.

For the traditional power electronic modules, bond wires are used to realize the electrical connections, the potting compound is then applied to seal the top side of the module to protect module components from environmental factors. Heat is usually dissipated from the chip through the wire bonds and solder layer to the substrate and the base plate, then to the heat sink or cold plate and finally to the ambient air or the cooling medium. A very limited amount of heat is also conducted through the poorly conductive potting compound to the top side of the package. However, the double sided cooling module has a more complicated heat transfer behavior than the traditional wire bonded module due to its spatially distributed thermal resistance and capacitance. Therefore, a good simulation tool is required to analyze the thermal performance of the multi-layer planar packaging power module.

Steady state and transient state thermal simulations of the power modules can be conducted using 1D, 2D or 3D models. 1D and 2D models can quickly build the physical layers of the components and generate the results. However, they suffer from the poor accuracy because heat spreading in different directions are not considered. The thermal model described by 3D finite

element method provides three dimensional meshes, which allows the consideration of the heat dissipation in both vertical and horizontal directions and is highly accurate. Softwares used for thermal simulation include Solideworks, Ansys, Icepack, ProE, Matlab, etc. In this chapter, Solidworks steady-state thermal simulation platform was used to predict the thermal performance of the modules. They are also used to evaluate the thermal behaviors of several planar packaging power modules for comparison purposes.

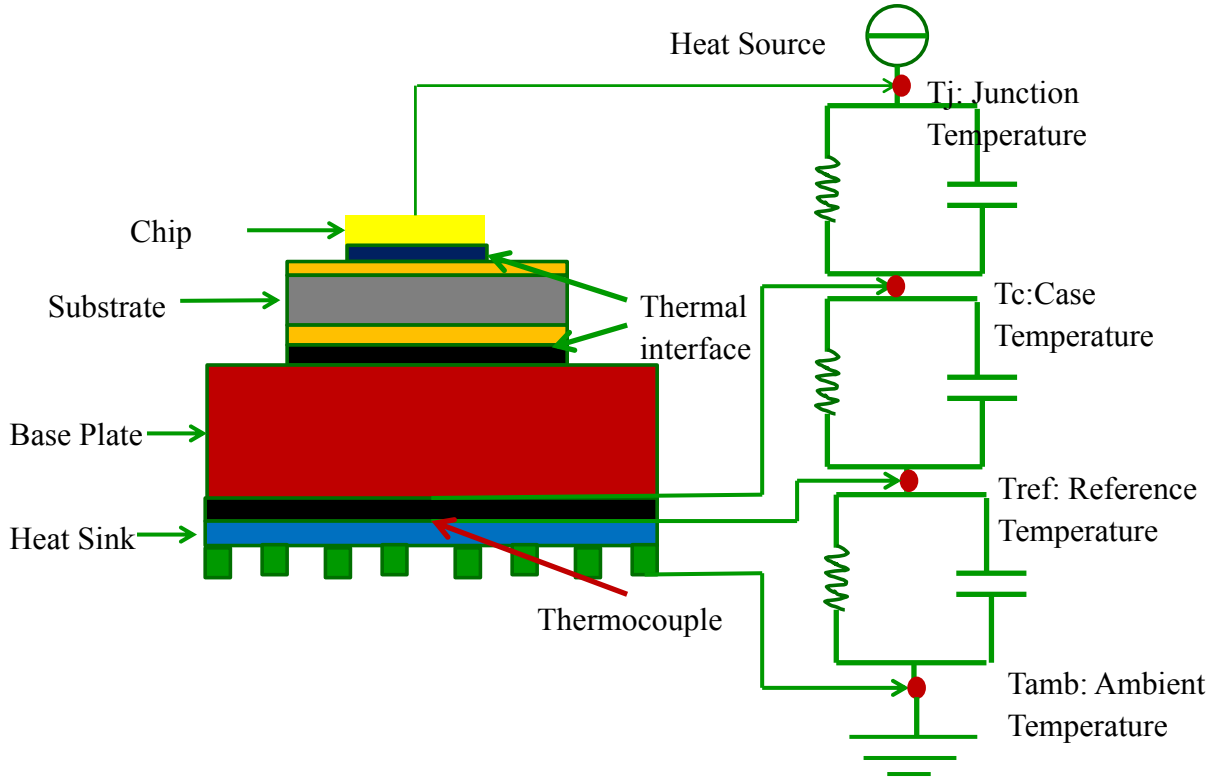


Fig. 4.1 Chip temperature hierarchy for modules with base plate

In order to conduct the power losses optimally through the connection layers to the heat sink, one of the focuses of the packaging design is to reduce the thermal resistance and thermal impedance of the power modules. Thermal impedance is defined as follows:

$$Z_{th}(t) = \frac{T_1(t) - T_2(t)}{P} \qquad (4.1)$$

where $Z_{th}(t)$ is the thermal impedance of the power module, $T_1(t)$ is the transient temperature at

the first spot and $T_2(t)$ is the transient temperature at the second spot, and P is the total heat losses generated.

In a practical power module, thermal resistance depends on the choice of temperature detection points as shown in Fig. 4.1. The total thermal resistance is calculated as:

$$R_{th\,(j-c)} + R_{th(c-s)} + R_{th(s-a)} = R_{th(j-a)} \qquad (4.2)$$

where $R_{th(j-c)}$ is the junction to case thermal resistance, $R_{th\,(c-s)}$ is the case to heat sink thermal resistance, and $R_{th\,(s-a)}$ is the heat sink to ambient thermal resistance.

4.2 Thermal Model for LTCC based Double-sided Cooling Power Module

Finite element models were developed with the help of the student-version Solidworks. The Sparse solver allows for the conductive, convective and radiate analysis of the thermal dissipation. Conduction is an internal energy exchange between one body in perfect contact with another body or from one part of a body to another part due to a temperature gradient. Conduction heat transfer is defined by Fourier's law and can be expressed as [43]:

$$q = -K_{nn}\frac{\partial T}{\partial n} \qquad (4.3)$$

where q is the flow rate per unit area in direction n, K_{nn} is the thermal conductivity in the direction n, T is the temperature, and $\frac{\partial T}{\partial n}$ is the thermal gradient in the direction n. The negative sign indicates that heat flows in the opposite direction of the thermal gradient.

Convection is heat transfer by mass motion of a fluid in the solid-fluid interface. Convection heat transfer is defined by Newton's law of cooling and can be expressed as [43]:

$$q = h\,(T_s - T_b) \qquad (4.4)$$

where q stands for the heat flow rate per unit area between surface and fluid, h is the convection film coefficient, T_s is the surface temperature, and T_b is bulk fluid temperature. Convection is typically applied as a surface boundary condition while convection coefficient and bulk

temperature are user inputs.

Radiation is heat transfer by the emission of electromagnetic waves and is derived from the Stefan-Boltzmann's law as [43]:

$$Q = \sigma \varepsilon A_i F_{ij} (T_i^4 - T_j^4) \quad (4.5)$$

where Q is heat flow rate from surface i to surface j, σ is Stefan-Boltzmann constant, ε is emissivity, A_i is area surface i, F_{ij} is form factor from surface i to surface j, T_i is the absolute temperature of surface i and T_j is the absolute temperature of surface j.

Thermal solid elements use high order node configuration, element degree of freedom is temperature, and temperature distribution within element is calculated from element shape functions. The finite element models include 2D triangular and rectangular shell elements, 3D tetrahedron, and pyramid as well as prism elements.

Heat generation in the power chips was assumed to be uniformly distributed inside the chips. The main heat paths inside the proposed double-sided cooling module were from the heat sources to both sides of the DBC substrate and to the heat sink. Heat was then transferred to ambient air through convection, or take away by the liquid cooling mediums inside the cold plate. Other path included from the high temperature side of the DBC to the lower temperature side.

4.3 Comparison of the Double-sided Cooling Module Designs

In order to present an overview over several double-sided cooling power electronics packaging solutions, finite element simulation was employed to assess their thermal performance regarding temperature distribution in the assemblies. In this work, simulations only consider the simplified case of a single diode packaged in different double-sided cooling module designs. From these simulations, the steady-state hot spot of the power chip is derived and compared. The double-sided cooling modules simulated were Embedded Power Stage by CPES [20][44] shown in

Fig.2.9, Power-Ball-Grid-Array Technology by Siemens shown in Fig.4.2 [6], Power Overlay by GE shown in Fig.2.8 [19], and the LTCC based double-sided DBC power module shown in Fig.3.1.

In all simulations, the power device was assumed to be a SiC diode with the size of 0.314"x0.314"x0.020" (thickness), the top metal pad size is 0.24"x0.24" The internal heat generation of the power chip is 160 W with an equivalent thermal coefficient of 3000 $W/m^2 \cdot ℃$. The material properties used in the simulations are shown in Table 4.1.

Table 4.2 summarizes the thermal simulation results for the six cases. As can be seen, the original embedded power module has the highest junction temperature of 119.2°C. This is due to the isolation layer applied between the top liquid cooling system and the die top surface. The isolation layer has a very low thermal conductivity which hinders the heat from dissipating efficiently from the top side. If this isolation layer is removed from the structure, the junction temperature is reduced by 41.6°C. Based on the original embedded power structure, if the top side liquid cooling system is replaced with DBC to contact with deposited copper trace, the junction temperature is reduced by 25°C. This is due to that the DBC layer improves the heat spreading on the top side, which results in a lower junction temperature. Furthermore, if the top

Table 4.1 Thermal conductivity of the material system for the thermal simulation

Material	Thermal conductivity (W/m·K)
Copper	400
AlN	150
LTCC	3.3
Nano silver paste	290
Gap filler	2.16
SiC	120
Solder	50

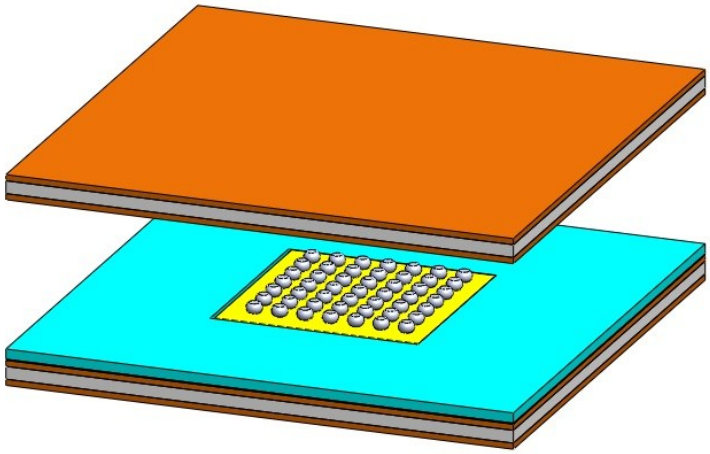


Fig. 4.2 PBGA package [6]

Table 4.2 Thermal simulation results comparison

Model	Maximum temperature (°C)	Minimum temperature (°C)	Mean temperature (°C)	Thermal resistance (°C/W)
EP	119.2	36.8	77.94	0.589
EP w/o top isolation layer	77.6	32.4	54.56	0.329
EP with double-sided DBC in direct contact with top copper trace	93.9	50.5	72.04	0.43
EP with double-sided DBC in direct contact with device metal pads	67.8	40.1	53.58	0.268
PBGA	75.2	35.4	55.05	0.314
LTCC based double-sided cooling module	64.3	41.9	52.75	0.246

DBC layer is directly in contact with the top device metal pads, the junction temperature is reduced by 51°C, which is about half of the original junction temperature. The LTCC based double-sided cooling module has the lowest maximum junction temperature of 64.3°C, and the mean temperature of 52.74°C as well as the smallest thermal resistance of 0.246 °C/W. The direct metal pad contact and the usage of the nano silver paste as die bonding material contribute to the lower thermal resistance of the power module. The PBGA structure has a middle level of

the thermal performance. This is because the usage of solder balls reduces the contact region compared to the direct large area solder contact.

4.4 Steady-State Thermal Simulation of the Double-sided Cooling Module and Its Single-sided Cooling Counterpart

For comparison purposes, steady-state thermal simulations were performed on both the LTCC double-sided cooling module and its single-sided cooling wire-bonded counterpart. Utilizing an axisymmetric approximation, the model consists of the DBC – SiC chip and LTCC – DBC stack, with 12/25/12 mils Cu-AlN-Cu DBCs, and 50 μm sintered Ag joints. The SiC MOSFET dimensions are $4.08\text{mm} \times 4.08\text{mm}$, and those for the SBD diodes are $4.02\text{mm} \times 8.03\text{mm}$. Solidworks steady-state thermal simulation platform was used to model the temperature distribution for both models. In the simulation, three scenarios were investigated, and the power dissipation for the MOSFET and diode were assumed to be 20W and 5W, 50W and 50W, and 100W and 100W, respectively. Assume the top surface of the power chips are fully contacted with the top side DBC in the double-sided cooling module model. The heat dissipation method is assumed to be purely convection. In the double-sided cooling module, the heat flow direction includes both downward and upward paths. For the wire-bonded module, the heat can only dissipate from the bottom side of the module. The heat removing efficiency varies from 100 $\text{W/m}^2\cdot\text{K}$ to 15,000 $\text{W/m}^2\cdot\text{K}$ in each interface between the module and outside heat sink or cold plate to model the air cooling to liquid cooling. Fig.4.3 shows the temperature distribution for the double-sided cooling module. Figs.4.5 and 4.6 show the Solidworks rendering of single-sided cooling wire-bonded counterpart and the thermal simulation result for temperature distribution. For the double-sided cooling module, assume both the entire top and bottom chip surfaces are fully attached to the cooling equipment. From these results, given the same heating and cooling

situations, the maximum temperatures of both models are located in the center of the SiC MOSFET due to the high heat generation of the device and the smaller size of the SiC MOSFET than that of the SiC diode .

Fig. 4.6 shows the comparison of junction temperature for the double-sided cooling and single-sided cooling modules for a power dissipation of 200W as a function of heat transfer coefficient.

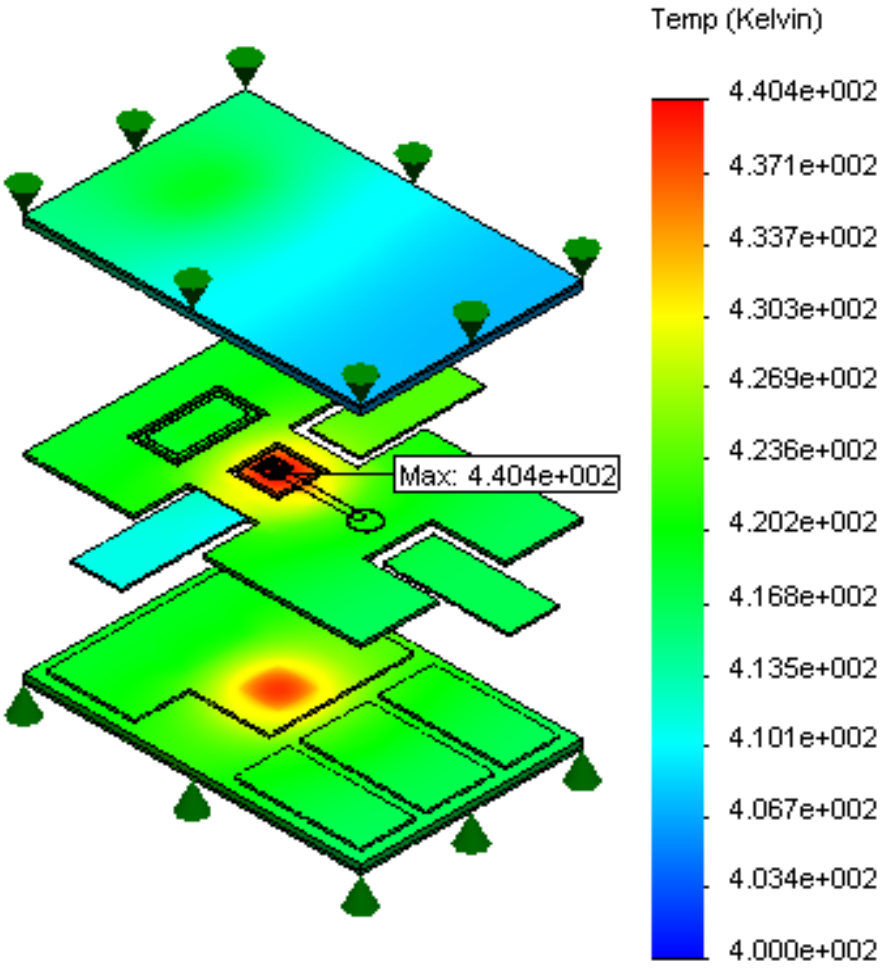


Fig. 4.3 Temperature distribution of the LTCC double-sided cooling module

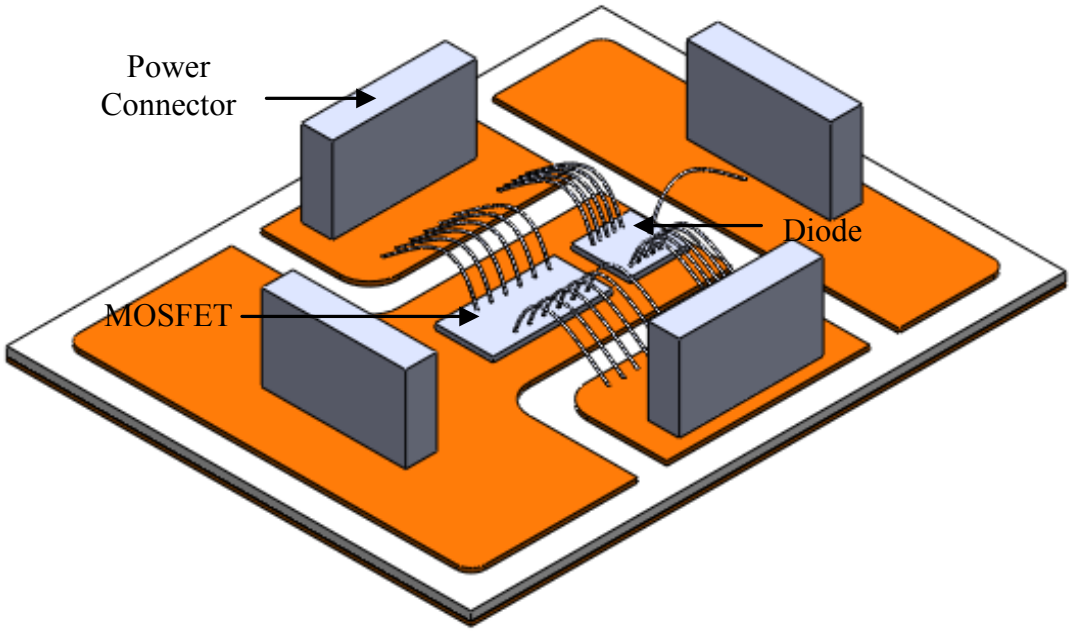


Fig. 4.4 Solidworks rendering of Wire-bonded counterpart

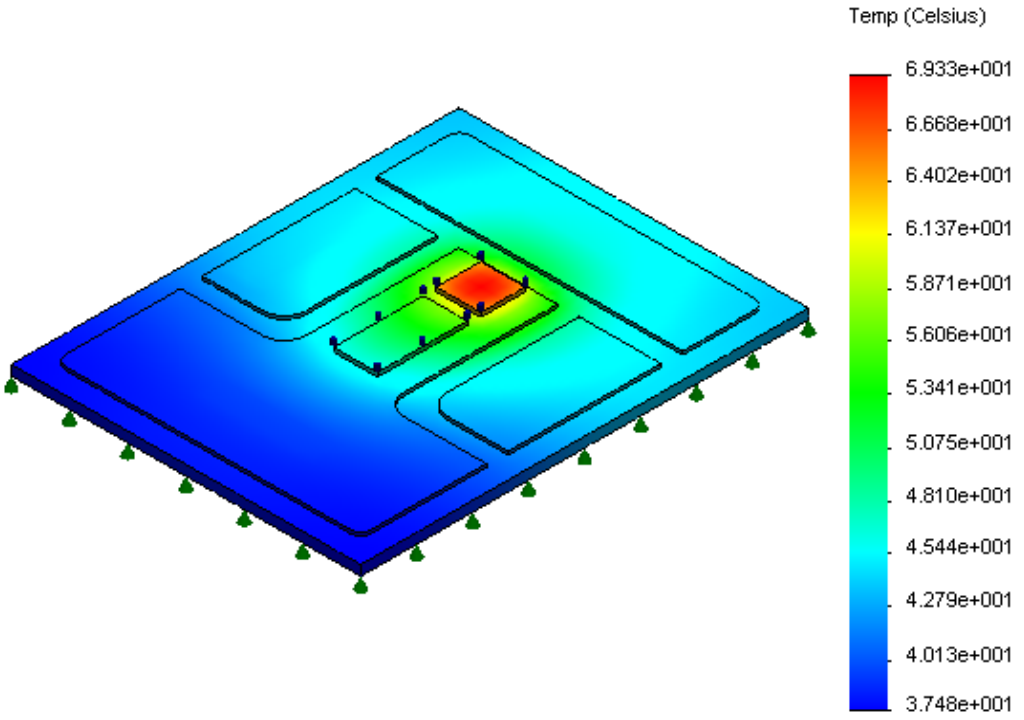


Fig. 4.5 Temperature distribution of the wire-bonded counterpart

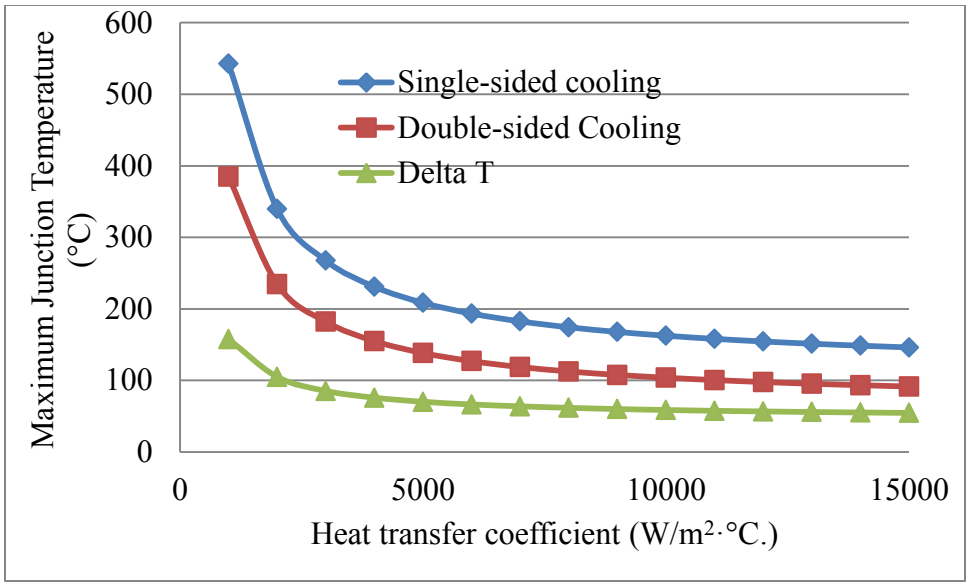


Fig. 4.6 Junction temperature comparison of double-sided cooling and single-sided cooling modules for a power dissipation of 200 W

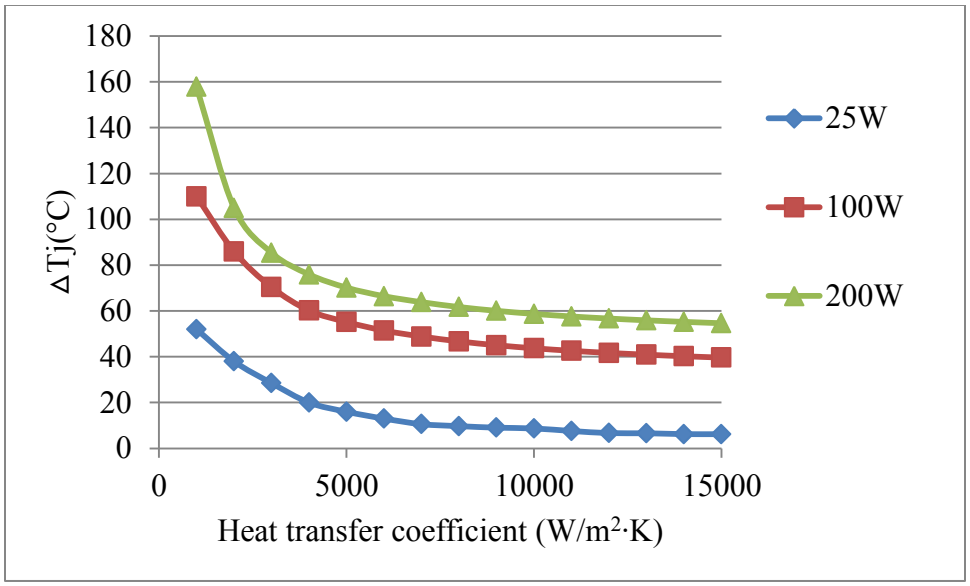


Fig. 4.7 Comparison of junction temperature difference for different power dissipations

As can be seen, the double-sided cooling module has lower junction temperatures than that of the single-sided cooling module for the same heat transfer coefficient. Fig. 4.7 shows that with a higher power dissipation, the maximum junction temperature difference between the single-sided

cooling module and double-sided cooling module is larger at the low power dissipations. As shown, the change in the junction temperature of the double-sided cooling module is much larger at low convection heat transfer coefficients.

4.5 Summary

This chapter introduces the finite element model for thermal performance simulation based on Solidworks. Several planar packaging structures were simulated and temperature distributions were compared for a power dissipation of 160W. Simulation results show that the proposed double-sided cooling structure has the lowest junction to ambient thermal resistance of 0.246°C/W. The thermal performances of the power modules with and without a base plate were also compared. Steady-state thermal simulations of the proposed LTCC based double-sided cooling module and its wire-bonded equivalent were also conducted. The overall temperature of the double-sided cooling module is lower than that of its wire-bonded counterpart. The thermal performance of double-sided cooling modules offers significant advantages for many high power density power electronic systems.

Chapter 5. Thermo-mechanical Analysis of the Proposed LTCC Double-sided Cooling Module

5.1 Introduction

Power modules usually consist of several components with various materials that have different coefficients of thermal expansion (CTEs). When current flows through power devices, Joule heating is generated and a temperature gradient in the module is developed. The stress resulting from the CTE mismatch between different materials plays an important role in manufacturing and the system in operation. Furthermore, it also affects the functionality and long-term reliability of the module. During the fabrication process, the power chips and the other parts of the module will be heated up and cooled down for several times, and residual stresses will be introduced to the final module assembly at room temperature. These stresses cause detrimental damage to the power chips, substrates and other parts of the module if they are not properly managed. For example, crackery of power chips, ceramic substrate, bonding wire and potting compound may be the result of an over stress in the power module. This chapter investigates the thermo-mechanical stresses caused by the temperature changes of the power module based on finite element simulation.

5.2 Thermo-mechanical Model for the Simulation

Table 5.1 shows the material system in a power module. For high temperature applications, thermo-mechanical stresses caused by the CTE mismatch would be even more severe. Residual stress caused by the fabrication process is also important if practical experiment is performed. Solder reflow temperature or room temperature for a non-underfilled package was mostly chosen as the stress-free temperature. When choosing the reflow temperature as the stress-free temperature, after the module cool down and dwell at room temperature for at least 4 days, the

hysteresis loop is similar to the case where room temperature was chosen as the stress free temperature [45]. Therefore, room temperature was used as the stress-free temperature in the simulations.

Table 5.1 Material properties of the components inside a power module

Material name	CTE (ppm/°C)	Yong's modules (GPa)	Thermal conductivity (W/m·K)	Poisson's ratio
SiC chip	4	420	120	0.14
copper	17	117	400	0.34
AlN	4.5	330	170	0.24
Sealing material	4.5	70	2.16	0.26
Nano silver paste	19	9	290	0.37
SAC405	20	40	50	0.37
LTCC	5.8	120	3.3	0.17

All parts in the model except the bonding layer material were modeled as elastic materials. Nano silver die attach and solder were modeled using the Anand's visco-plasticity model because rate dependent plasticity (creep) occurs in the sintered nano silver paste and solder over time [46, 47]. Anand's visco-plasticity model considers the material physical behaviors sensitive to strain rate, temperature, history of strain rate and hardening and softening [48]. In Anand's model, inelastic deformation is referred to all irreversible deformation and it incorporates a single internal variable, namely deformation resistance, to represent the isotropic resistance to inelastic flow of the material [48]. The following functional formulations represent Anand's model with the flow equation and three evolution equations [49]:

Flow equation [49]

$$\dot{\varepsilon_p} = A[\sinh(\xi\dot{\sigma}/s)]^{1/m}\exp(\frac{-Q}{RT}) \quad (6)$$

Evolution equations [49]

$$\dot{s} = \{h_0(B)^a \frac{B}{|B|}\}\dot{\varepsilon_P} \quad (7)$$

$$B = 1 - \frac{s}{\hat{s}} \quad (8)$$

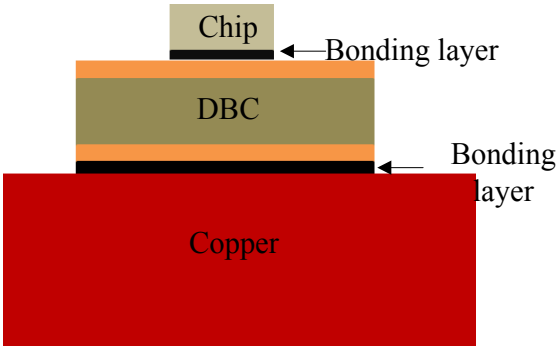
$$s^* = \hat{s}[\frac{\dot{\varepsilon_p}}{A}\exp(\frac{Q}{RT})]^n \quad (9)$$

The parameters along with their meanings are shown in Table 5.2.

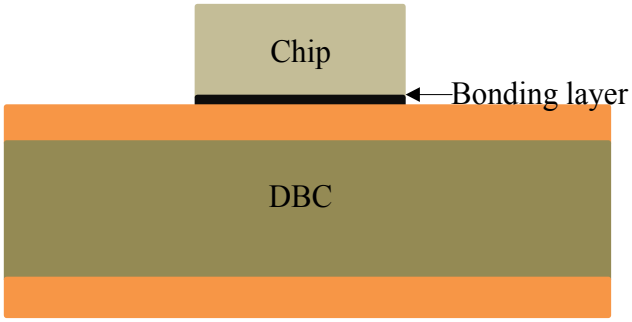
Table 5.2 The parameters for Anand's model for the bonding layer [50] [51]

Constant	Parameter	Nano silver paste	SAC405	Definition
C1	S_0 (MPa)	2.77	20	Initial value of deformation resistance
C2	Q/R (1/Kelvin)	5709	10561	Activation energy/Boltzmann's constant
C3	A (1/sec)	9.81	325	Pre-exponential factor
C4	ξ (dimensionless)	11	10	Multiplier of stress
C5	m (dimensionless)	0.657	0.32	Strain rate sensitivity of stress
C6	ho(MPa)	15800	8E5	Hardening or softening constant
C7	S (MPa)	67.4	42	Coeff. Of deformation resistance saturation value
C8	n (dimensionless)	0.003	0.02	Strain rate sensitivity of saturation (deformation resistance) value
C9	a(dimensionless)	1	2.57	Strain rate sensitivity of hardening

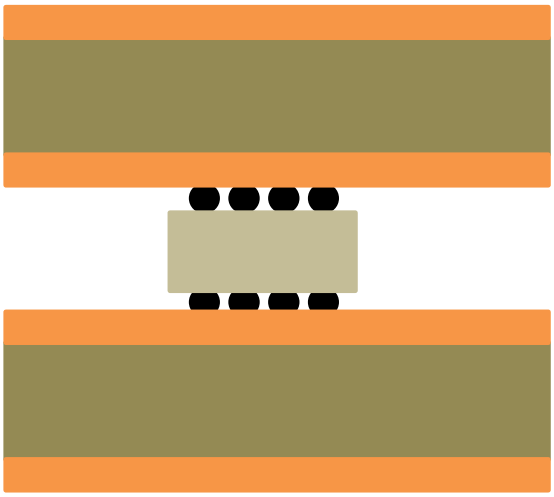
In order to optimize the structure and achieve the lowest stress in the package, several different cases were investigated. In the first case, a SiC chip was bonded to the DBC substrate using a solder preform as shown in Fig. 5.1 (a). In case 2, a copper base plate was added to the structure based on case 1 using a large area solder shown in Fig. 5.1 (b). In case three, a solder layer was replaced by solder balls as shown in Fig. 5.1 (c). Case 4 shows a double-sided DBC structure with a solder layer as shown in Fig. 5.1 (d). Based on case 4, case 5 adds the LTCC substrate and gap filling material into the structure and represents the proposed double-sided cooling structure



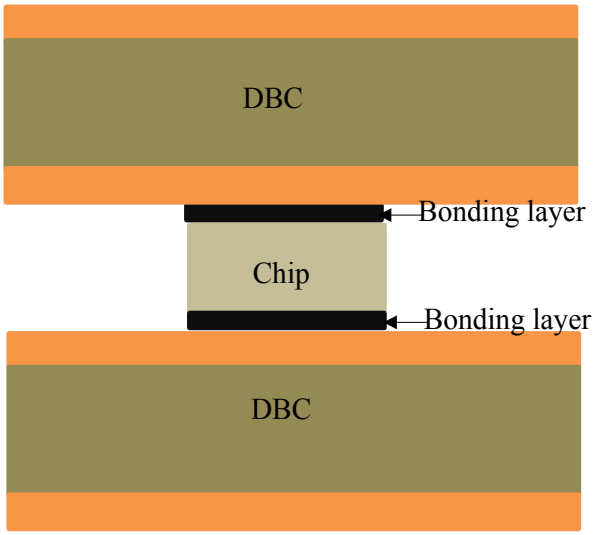
(a) Simulation case 1: packaging with base plate



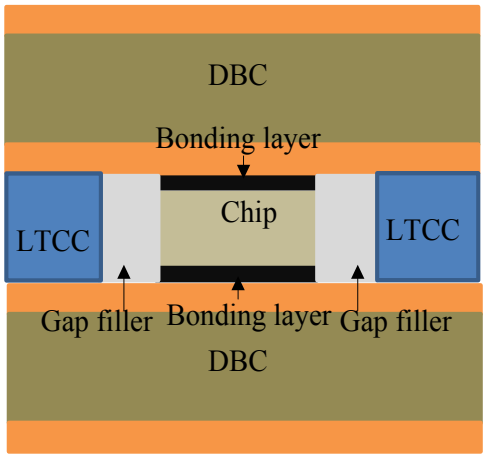
(b) Simulation case 2: packaging without base plate



(c) Simulation case 3: Solder ball attachment



(d) Simulation case 4: Double-sided DBC attachment



(e) Simulation case 5: Double-sided DBC attachment with chip supporting structure

Fig. 5.1 Comparison of thermo-mechanical stress for different structures

as shown in Fig. 5.1 (d). In each case, the chip was assumed to be a diode with the size of 0.314"x0.314"x0.020". The DBC stack used in the simulation has a footprint of 1"x1". The thicknesses for the AlN substrate and copper are 0.025" and 0.012", respectively. Assume the heat sink is an aluminum chunk. The bonding layer thickness was assumed to be 2 mils in all cases.

5.3 Simulation Set Up

The thermo-mechanical stress simulations were conducted using the Workbench steady state thermal and static structural platform of Ansys software. The temperature of the structure was increased from room temperature (25°C) to the steady state temperature assuming the internal heat generation of the power device is 208W and a heat transfer coefficient of 3000W/m^2·K for the heat sink. This temperature distribution is used as the input for the thermo-mechanical stress simulation to obtain the stress and strain distributions in the structure as shown in Fig. 5.2. Due to the symmetry structure for each case and the non-linear material properties of the solder, a quarter region model for single-sided DBC structure as shown in Fig. 5.3 is used to speed up the simulation process. Fig. 5.4 shows the boundary conditions for the simulation cases 1 and 2. Due to the symmetrical structure in the XZ and YZ plane, the center surface in each module was set to be frictionless support of all the points in the plane of ZY, X direction was constrained, and Y direction was constrained for all the points in the plane of XZ, the bottom center point was fully constrained for both rotation and translation. For cases 3, 4 and 5 as shown in Figs. 5.2 (c), (d), (e), it is symmetrical in the XY plane, YZ plane and XZ plane. The boundary conditions include the frictionless support of center surface in the XY plane, YZ plane and XZ plane. As such, only 1/8 region of the model was simulated for the double-sided DBC structure.

ANSYS sub-modeling technology was used to obtain a more accurate simulation result in the stress and strain concentrated areas to reduce simulation time. Sub-modeling utilizes a global model to represent the entire structure and a coarse mesh was used to calculate the results first.

The global loads were transferred to local deformation and the global model simulation results were applied as boundary conditions in the localized sub-models of the bonding layer. Fig. 5.5 shows a global module with a coarse mesh for case 2 in (a) and a fine mesh with only in solder layer (b).

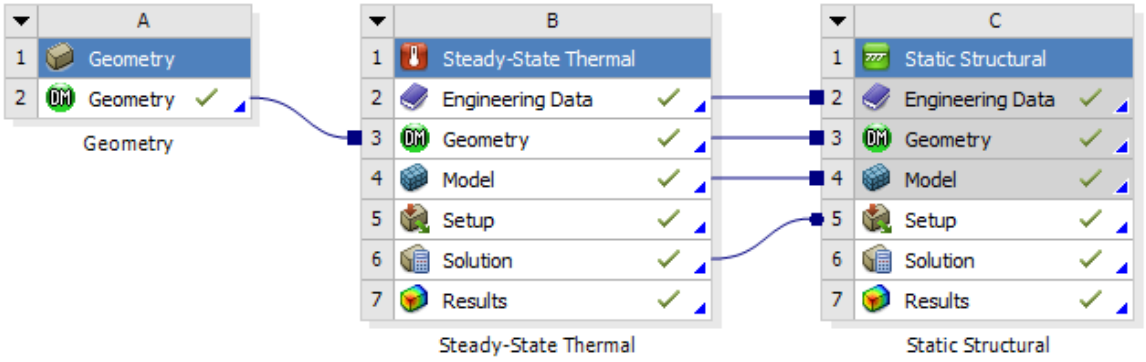


Fig. 5.2 Thermo-mechanical stress simulation process flow

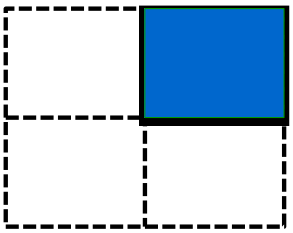
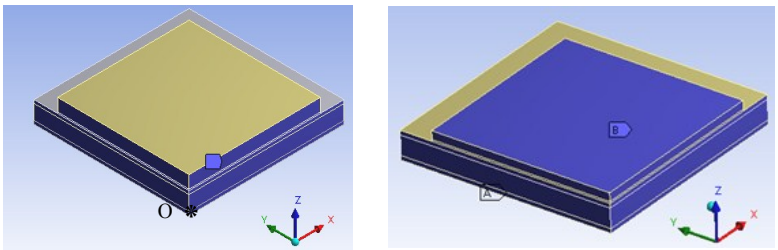
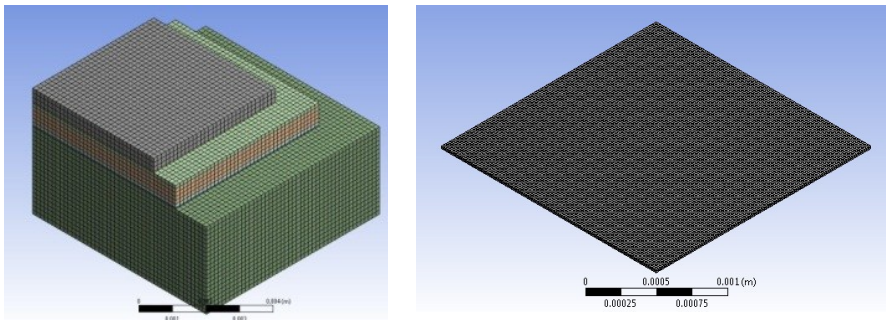


Fig. 5.3 Quarter region for thermo-mechanical simulation



Cases 1 and 2 Cases 3, 4 and 5

Fig. 5.4 Boundary conditions for thermo-mechanical simulation



(a) (b)

Fig. 5.5 (a) global model with coarse mesh and (b) sub-model with fine mesh in solder layer

5.4 Simulation Results Comparison and Discussion

Table 5.3 shows the simulation results for both the base plate module and module without a base plate. The same geometry and power dissipation were applied. In the table, △L is the maximum deformation, and F_{VM} is the maximum Von-Mises stress in the body. These results are discussed in the following sections.

Table 5.3 Thermo-mechanical simulation result comparison

Model	Layer	SiC	Die bonding layer	DBC	DBC to base plate Bonding layer	Base plate
Case 1	T_{jmax} (°C)	167.58	166.79	166.48	161.42	161.18
	ΔL(um)	17.2	17.5	18.1	23.1	27.0
	ε_{total}(1e-4m/m)	1.89	164.5	25.6	1179.8	6.9
	F_{VM} (MPa)	75.6	24.3	300.3	39.8	80.8
Case 2	T_{jmax} (°C)	164.75	163.97	163.67	/	/
	ΔL(um)	14.5	14.8	16.5	/	/
	ε_{total}(1e-4m/m)	1.83	112.7	24.8	/	/
	F_{VM}(MPa)	73.4	20.8	290.9	/	/
Case 3	T_{jmax} (°C)	119.79	117.91	96.343	/	/
	ΔL(um)	3.56	3.58	5.41	/	/
	ε_{total}(1e-4m/m)	1.12	27.5	15.58	/	/
	F_{VM}(MPa)	44.8	26.5	208.9	/	/
Case 4	T_{jmax} (°C)	94.958	94.752	94.6	/	/
	ΔL(um)	3.45	4.47	5.59	/	/
	ε_{total}(1e-4m/m)	3.94	208.5	12.85	/	/
	F_{VM}(MPa)	157.9	34.7	209.5	/	/
Case 5	T_{jmax} (°C)	94.957	94.751	94.6	/	/
	ΔL(um)	3.82	3.92	5.18	/	/
	ε_{total}(1e-4m/m)	2.97	23.5	12.5	/	/
	F_{VM}(MPa)	118.9	8.77	318.2	/	/

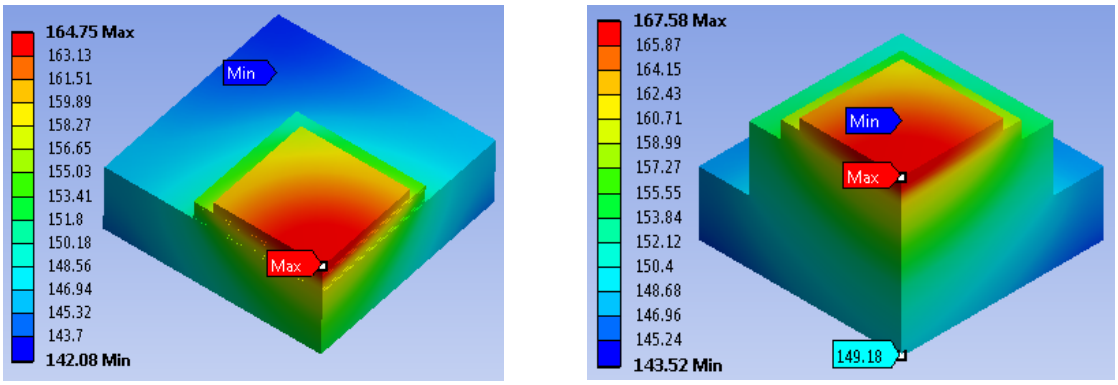
5.4.1 Base Blate Versus No Base Plate

Traditional wire bonded power modules normally used a copper base plate as the heat spreader and the DBC substrate was attached to the base plate using a large area solder. Such modules are

mechanically more robust during transport and assembly. However, the thick base plate increases the weight of the module assembly, and reduces its temperature cycling capability since the large area solder layer attached to base plate is susceptible to temperature cycling failure. The chip to heat sink thermal resistance is usually higher due to a thicker layer of thermal paste caused by the base plate bending.

Modules without a base plate usually use the heat sink to help spread the heat. Such modules usually have lower thermal resistances due to the reduced layers and thinner thermal paste layer. Due to the removal of solder layer in base plate, thermal cycling capability is largely improved. A lower temperature gradient can also be achieved which means the smaller thermal stress in the package under working condition. The disadvantage with this structure is that there is no heat storage due to the removal of the copper base plate which functions as a thermal capacitance.

Fig. 5.6 shows the imported temperature distribution of power module with and without a copper base plate, respectively. In both cases, the maximum junction temperature is located in the center point of SiC chip top surface, Fig. 5.7 gives the comparison of the maximum temperature in each layer. It shows the junction temperature for the model with a base plate is167.6°C, which is 3°C higher than the one that does not a have base plate.



(a) (b)

Fig. 5.6 Temperature distribution for power module (a) without and (b) with a base plate

Table 5.4 shows the simulation results of different temperatures in each module. Tmax represents the maximum junction temperature; Tc is the case temperature at the bottom surface of the power module in the chip center. From the results, power module without a base plate has a lower global temperature distribution than the power module with a base plate, and the junction to case thermal resistance of the power module without a base plate is 0.059°C/K, this value is smaller than 0.088°C/K – the thermal resistance of the power module with base plate. This is due to the high thermal conductivity of AlN that helps dissipating the heat from the power device to the heat sink. In the meantime, the removal of the thick base plate reduces the thermal path for the heat flow, which results in a better thermal performance and a lower thermal resistance between the junction and case.

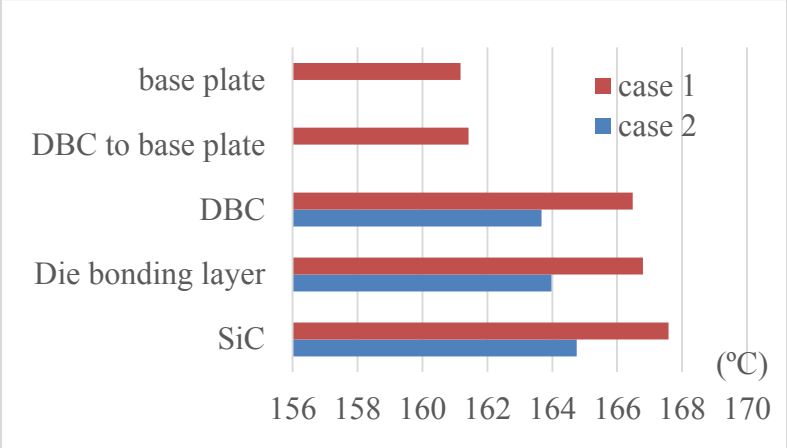
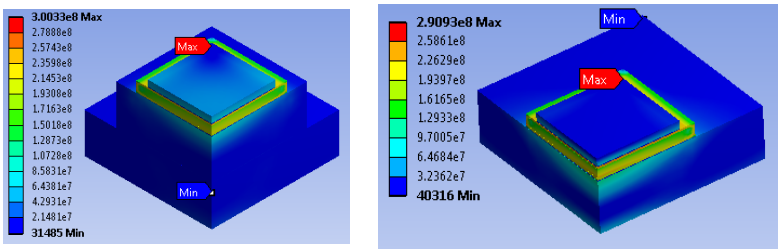


Fig. 5.7 Temperature comparison of case 1 and case 2

Table 5.4 Comparison of construction and temperature measurement for power module with and without base plate

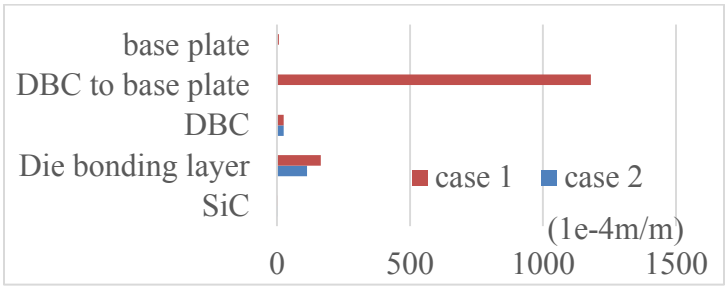
Results	W/base plate		W/O base plate	
	Tmax (°C)	Tmax - Tc(°C)	Tmax(°C)	Tmax - Tc(°C)
SiC	167.6	18.42	164.8	12.31
Substrate	166.5	17.32	163.7	11.21
Base plate	161.2	12.02	-	-
Rth (°C/K)	0.088		0.059	

As shown in Fig. 5.8 and Fig. 5.9, due to the absence of the base plate and the large solder between the DBC substrate and the copper base plate, the maximum deformation and total strain in each layer for case 2 is smaller than those in case 1. The base plate module has an extreme thermal mismatch between the substrate and base plate, which resulting in a larger total strain in the bonding layer between the substrate and base plate due to the ductile material properties of solder. Thermo-mechanical stress on each layer in the base plate module is larger than that of the non-base plate module shown in Fig. 5.10.

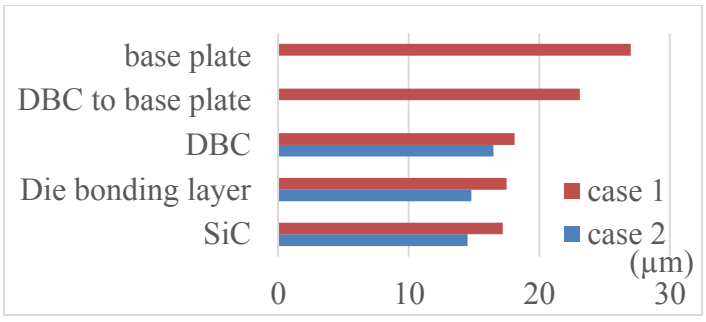


(a) (b)

Fig. 5.8 Von-Mises stress distribution for (a) base plate and (b) non-base plate module (Unit: Pa)



(a)



(b)

Fig. 5.9 Total strain (a) and deformation (b) comparison of case 1 and case 2

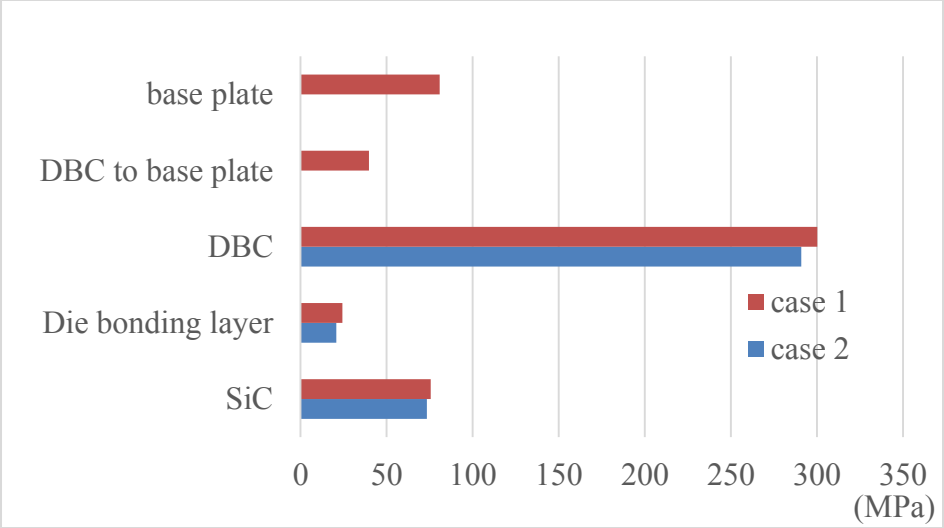


Fig. 5.10 Comparison of maximum thermal stress of case 1 and case 2

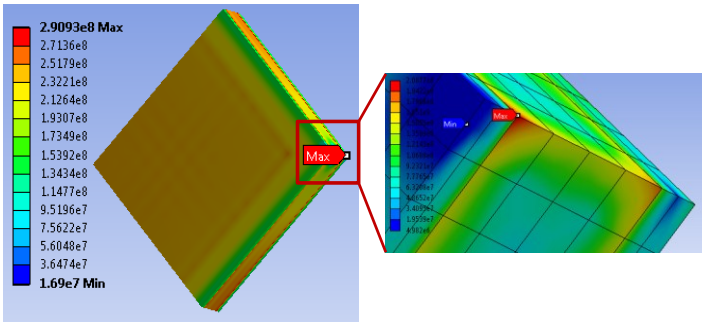
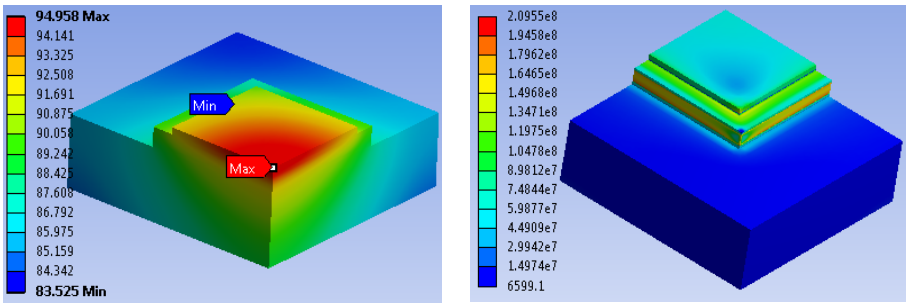


Fig. 5.11 Von-Mises distribution in DBC substrate

In all cases, the maximum stress occurs between the DBC ceramic layer and copper layer. This is because of the large CTE mismatch and large contact area between the copper and ceramic as well as the high Young's modulus of the ceramic layer. Fig. 5.11 shows the detailed stress distribution in DBC substrate. From this figure, the maximum stress of 290MPa is located at the corner of the top ceramic that contacts with the copper layer. However, in the practical module, this is not necessarily the case, since the actual DBC manufacturing process subjects the copper alloy to various annealing, hardening and dispersion strengthening process, and the material properties of the DBC is different from the pure copper and ceramic which is used in the simulation.

5.4.2 Single-sided Cooling Versus Double-sided Cooling

Fig. 5.12 shows the temperature and Von-Mises distributions for the double-sided cooling module. The maximum junction temperature of the double-sided cooling module is 94.96°C, which is 72.65°C lower than that of the single-sided DBC module with single-sided cooling. Fig. 5.13 shows the deformation for the quartered double-sided cooling structure. As can be seen, the edge region of each layer has a larger deformation, similar to single-sided cooling structure. The maximum temperature in each layer of both cases is compared in Fig. 5.14. As can be seen, the temperature of each layer for the double-sided cooling module is about half of that in the single-sided cooling model. This is because the top side metal pads have a smaller size compared to the average of the bottom side of the device. Consequently, the heat dissipated from the bottom side is larger than that from the top side.



(a) Unit: °C (b) Unit: Pa

Fig. 5.12 Temperature distribution (a) and Von-Mises distribution (b) for double-sided DBC module

Due to the lower temperature generated in the double-sided DBC model, the total deformation of each layer is smaller than that of the single-sided cooling model as shown in 5.15 (a). The bonding layer has a larger strain than the SiC and DBC due to the ductile material properties of the solder and large plastic strain occurs at the highest temperature. This large strain helps to release the stress, which results in a lower stress in the solder layer than that in SiC die and DBC.

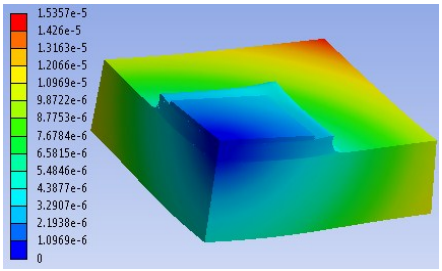


Fig. 5.13 Total deformation distribution for double-sided DBC model (unit: m)

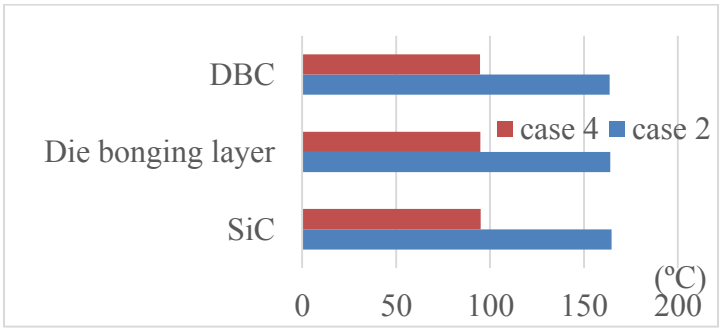
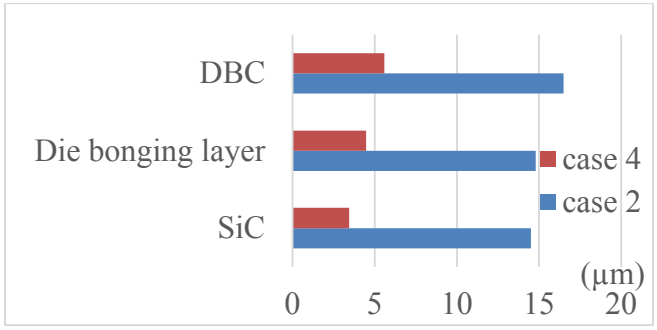
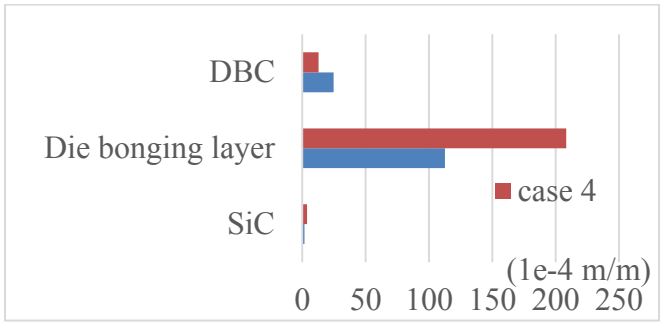


Fig. 5.14 Temperature comparison of case 2 and case 4



(a)



(b)

Fig. 5.15 Comparison of total deformation (a) and total strain (b) of case 2 and case 4

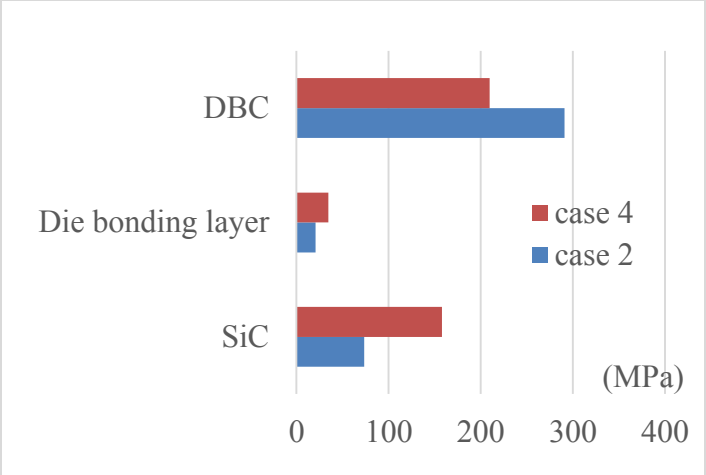


Fig. 5.16 Comparison of Von-Mises stress of case 2 and case 4

The SiC die has a higher stress in the double-sided cooling model than that of the single-sided cooling model as shown in Fig. 5.16. This is due to the symmetrical structure of the double-sided cooling model, and the frictionless support of the middle surface of device during the temperature excusion process. Both the top and bottom sides of the DBC substrate will pull the die during the temperature increase process which makes the SiC device more stressful.

5.4.3 Solder Ball Versus Direct Solder Attachment

For the double-sided DBC attachment with double-sided cooling, when solder balls were used to bond the power chips instead of using nano silver paste, the maximum junction temperature of the power chip increased from 95°C to 119.8°C as shown in Figs 5.17 and 5.18. This is due to the limited contact areas of the solder balls rather than large area direct bonding with devices.

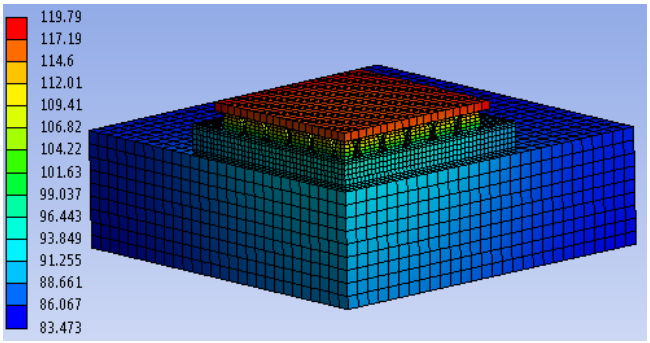


Fig. 5.17 Temperature distribution for double-sided DBC structure with solder ball (unit:°C)

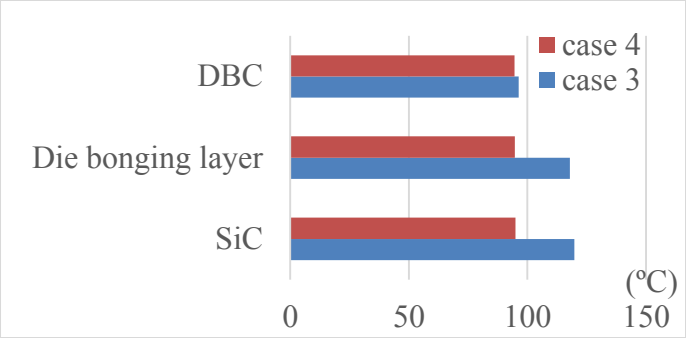


Fig. 5.18 Temperature comparison of case 4 and case 3

Figs. 5.19 and 5.20 show the total deformation and thermal stress distribution for the solder ball model. As expected, the maximum deformation (17.3 μm) is located at the corner of the base plate, and the maximum thermal stress occurs in the center region of the model, which indicates that the DBC substrate along with the solder balls introduce relative large thermal stresses. Figs. 5.21 and 5.22 show the detailed views of solder ball deformation and thermal stress. As shown, the maximum stress of 26.5MPa of the solder ball attachment is located in the corner solder joints. This is due to the thermal expansion coefficient mismatch of the solder ball substrate and the interposer. The deformation of the solder ball in the edge region (3.58μm) is larger than that in the center region (0.09 μm), which causes the largest stress and strain in the outmost solder joint.

Figs. 5.22 and 5.23 compare the maximum deformation, total strain and thermal stress in each layer for case 3 and case 4. From these two figures, the die bonding layer shows a smaller deformation, total strain and equivalent stress in case 3 than that in case 4. This is because the solder balls are separated from each other. As such, the influence of the center solder balls on the outside solder balls is minimum. Since the total dimension and volume of each solder ball is small, the maximum deformation and thermal stress for the most vulnerable spot of the outside solder ball is smaller compared to the large area solder contact. While the maximum deformation

of the SiC die and DBC substrate is similar in case 3 and case 4, the thermal stress generated in

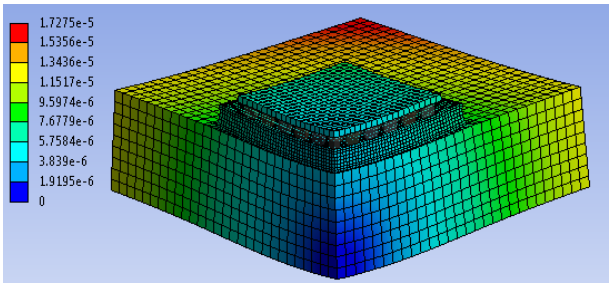


Fig. 5.19 Total deformation distribution in solder ball model (unit:m)

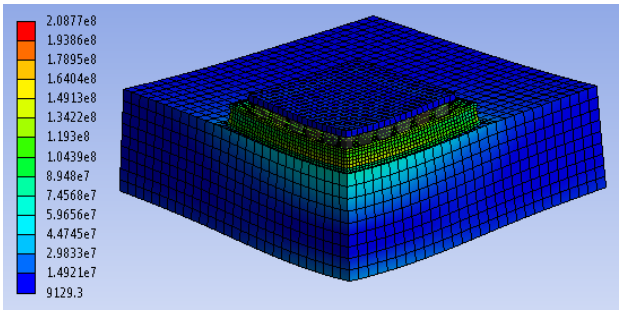


Fig. 5.20 Equivalent stress distribution in solder ball model (unit: Pa)

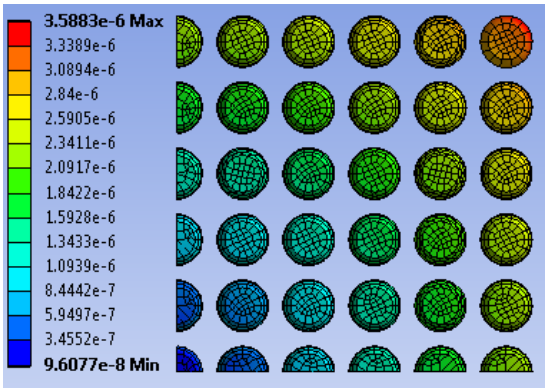
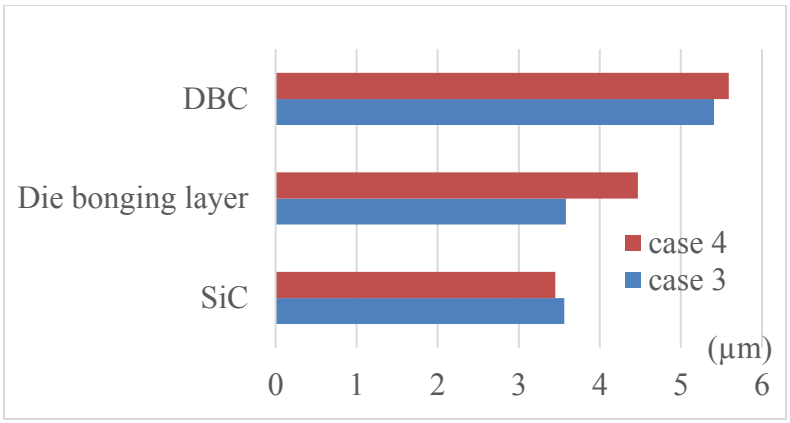
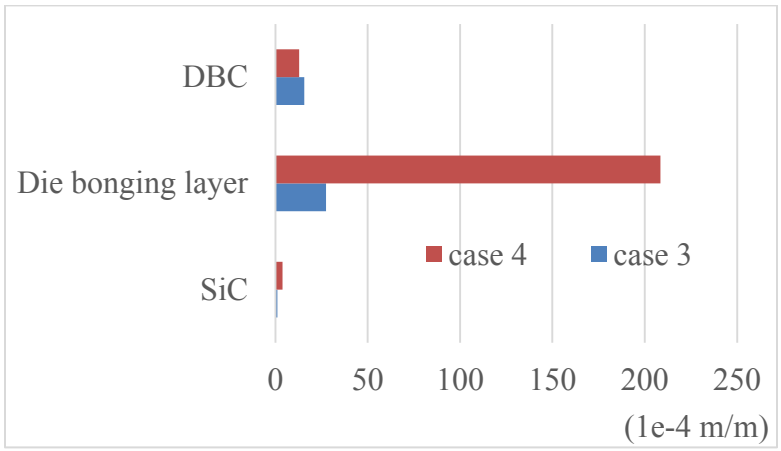


Fig. 5.21 Total deformation of solder balls (unit: m)

the SiC die in case 3 is much smaller than that in case 4. This is because the contact area of solder balls with device are much smaller than that of the solder preform and the contact regions are distributed uniformly with some spaces between different contacts. As such, the device has more freedom to flex during temperature variation and the thermal stress is not concentrated as in the case for the large solder preform contact.



(a)



(b)

Fig. 5.22 Deformation (a) and total strain (b) comparison of case 3 and case 4

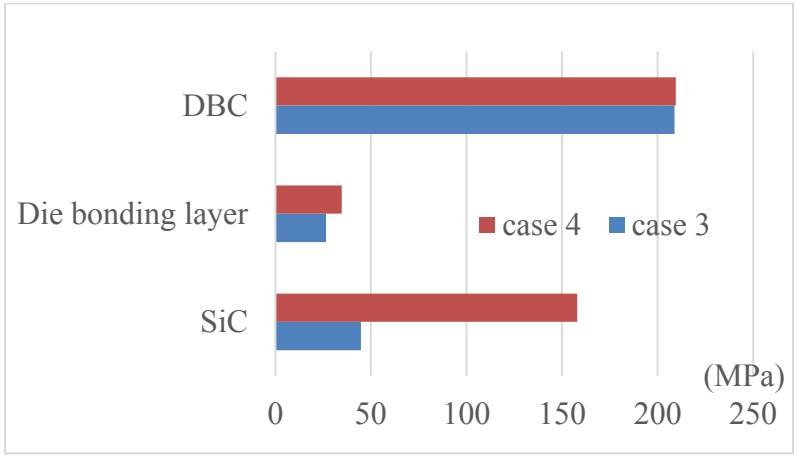


Fig. 5.23 Thermal stress comparison of case 3 and case 4

5.4.4 Packaged Die Versus Unpackaged Die

Case 4 and case 5 compare the difference of an unpackaged die with only DBC attachment and packaged die with LTCC die carrier and dielectric material filling the gap between die and LTCC substrate. Fig. 5.26 shows the maximum temperature of each layer in case 4 and case 5. As shown, the addition of the die carrier and dielectric material did not affect the temperature distribution very much inside the package. The reason is that the heat spreads at a 45° angle corresponding to a truncated pyramid [52] on the top and bottom of the device. The dielectric material and LTCC substrate is out of the heat dissipation path which contributes nothing to the heat spreading. Fig. 5.27 shows that the total deformation of the three layers in case 4 and case 5 are similar to each other. However, the thermal stress in the SiC and bonding layer shown in Fig. 5.28 is much smaller in case 5 than those in case 4. This is due to the fact that the CTEs of the dielectric material and LTCC substrate are similar to that of the SiC die. When the package is going through the temperature variation process, the center layer in the packaged structure will expand and shrink more uniformly than the non-packaged structure, which helps to release the stress in the bonding layer and the die. The stress reduction in the die and bonding layer increases the thermal stress in the DBC substrate.

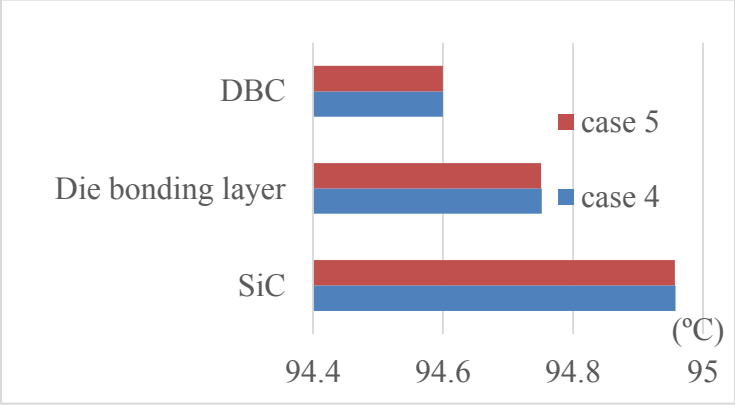
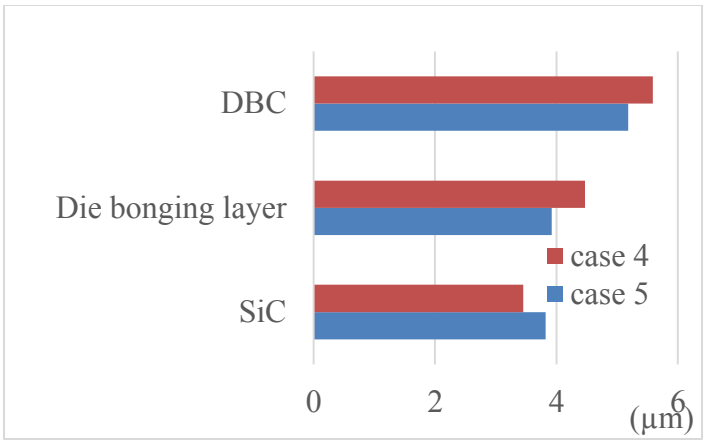
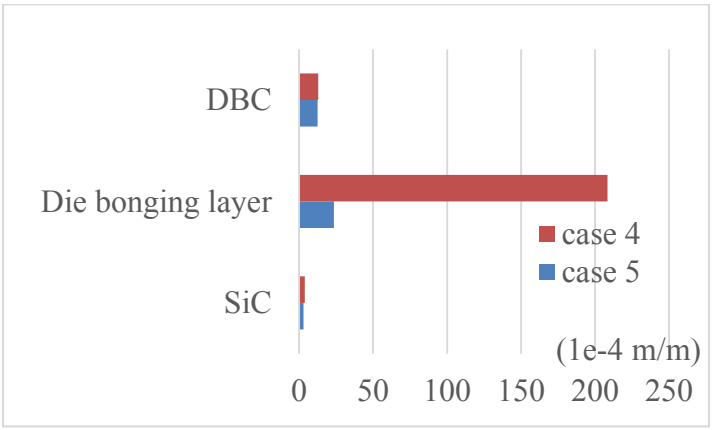


Fig. 5.24 Junction temperature comparison of case 4 and case 5



(a)



(b)

Fig. 5.25 Maximum total deformation (a) and total strain (b) of case 4 and case 5

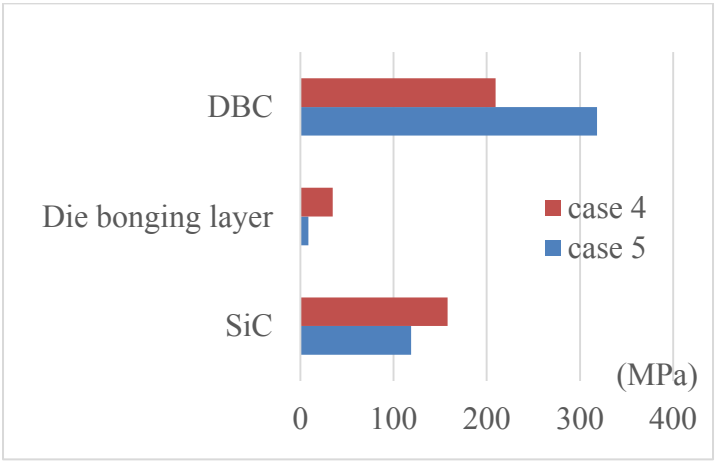


Fig. 5.26 Maximum thermal stress comparison of case 4 and case 5

5.5 Summary

This chapter introduces thermo-mechanical performance for the power module. Five different die packaging structures were simulated and compared. Anand visco-plastic model was adapted for the die bonding layer in the simulation using inserted script. In the simulation, the distribution of the package temperature was calculated at 208W power dissipation. This temperature distribution was then imported to the static structure calculation to generate the thermal stress in each packaging layer. Simulation results show that the thermal stress of single-sided DBC without a base plate is lower in each layer than the one that has a base plate. The reason is that the removal of the base plate not only reduces the thermal resistance in the thermal path but also eliminates the use of a large area solder beneath the substrate. Compared to the single-sided cooling structure, double-sided cooling module lowers the junction temperature by cooling the device from both the top and bottom sides. With solder ball die attachment, the junction temperature reduced from 165°C to 120°C. The solder preform attachment further reduces junction temperature to 95°C. However, the challenges brought by the double-sided DBC structure is the higher thermal stress generated in the semiconductor devices. The maximum thermal stress generated in the die when using double-sided DBC structure is 157.9MPa compared to the 75.6MPa for the single sided cooling module. A dielectric material and LTCC substrate help to relieve the thermal stress to 118.9MPa.

Chapter 6. Fabrication of the Module

6.1 Introduction

After the simulation of the LTCC based double-sided cooling module, a prototype module was fabricated. The fabrication and assembly processes are described in this chapter.

6.2 DBC Substrate Preparation Process

The direct-bonded-copper substrate from Curamik® is made of 25 mils of Al_2O_3 ceramic sandwiched between two pieces of 12 mils copper plates. The surface is plated with 0.1 to 0.3 μm of Ag to ensure a good bonding between the DBC and SiC devices for nano silver joints. In order to selectively pattern and etch the DBC substrate, a dry film photoresist process was used along with a chemical etching process.

The dry film lamination process starts with adhering a composite structure of photopolymer and polyester film to DBC substrate. Before the process, the DBC substrate was heated on top of a hot plate to 100°C for 30 seconds to promote the adhesion of the film to the DBC substrate. A Kepro® bench-top laminator as shown in Fig. 6.1 (a) was used to apply the thin layer of photoresist and polyester coversheets. After the film was applied, a dry film photo mask representing the copper trace layout of the DBC substrates was overlaid on top of the DBC substrate and exposed with an UV light for 2 minutes. The sample was then immersed in a developing solution of 1% sodium carbonate for about 2 minutes to develop the metal pattern. After this step, the DBC substrate was put on a transfer belt in a chemical etching machine to etch away the copper layer as shown in Fig. 6.1 (b). Before the etching, the $FeCl_3$ solution in the chemical etching machine has to be heated to 125°F to enhance the etching process. The transfer speed for the 12-mil copper layer is 2.0 mils per min at this temperature. Since the dry film resist is a negative resist, the metal under the dark region in the mask will be etched away. After

etching, the samples were cleaned with DI water and IPA. The next step is dicing the DBC substrate into individual pieces. A micro dicing saw from Micro Automation shown in Fig. 6.2 was used. The individual diced DBC substrate is shown in Fig. 6.3. The cutting model for the rectangular DBC is 30 and the forward cutting speed was 60 mils/min with a spindle speed of 20,000 rpm.

(a) (b)

Fig. 6.1 Kepro bench-top laminator (a) and chemicut machine for etching (b) (photo by author)

Fig. 6.2 Micro dicing saw (photo by author)

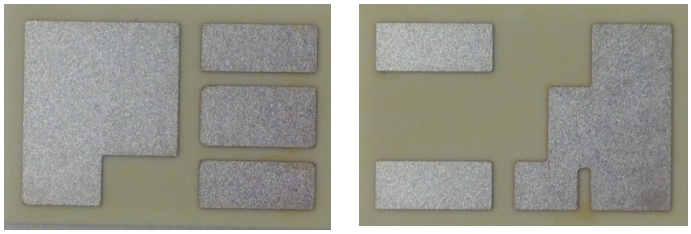


Fig. 6.3 Diced DBC pieces (photo by author)

6.3 LTCC Substrate Preparation Process

The fabrication of the LTCC substrate starts with preconditioning of the fresh green tapes in an oven at 80°C for 20 minutes. Dupont 951 LTCC green tapes with a thickness of 10 mils were used. After the preconditioning of the green tapes, a punch machine (model APS-8718 from Pacific Trinetics Corporation) was used to create the cavities and vias according to the mask shown in Fig. 6.4. The pin sizes for punching cavities and vias are 94 mils and 20 mils, respectively. When punching the green tapes, it is preferred to rotate the single tape 90° to compensate for the different shrinkages in the X and Y directions. Fig. 6.5 shows the single green tape after the cavities and vias have been punched.

The next step is vias filling. There are two ways to fill in vias, either conventional screen printer or an extrusion via filler. Both method needs a via filling mask. In this case, vias were filled manually by using a soft polymer squeegee and Dopunt 6141 paste was used as the via filling material. Before proceeding to the next step, green tapes were put in the LTCC oven to dry the vias at 80°C for 5 minutes to ensure that the vias stay its original shape and not be scratched by the tapes. There are two ways of laminating the green tapes traditionally. A uniaxial lamination uses a hot plate at 70°C and the tapes are placed in between the hot plate and a pressure of 200 bar is applied for 10 minutes. The disadvantage of this method is that it requires a 180° rotation in the middle of the press for half of the time and may cause high shrinkage. Our samples were made using the isostatic lamination method. In this method, the stacked tapes are vacuum sealed in 4 aluminum foil bags and pressed in hot water at a temperature of 70°C with a pressure of 3000 pai. The total cycle time is about 10 minutes. Fig. 6.6 shows the PTC isostatic laminator system.

The laminated tapes are then ready to be diced on top of a hot plate. The temperatures of the hot

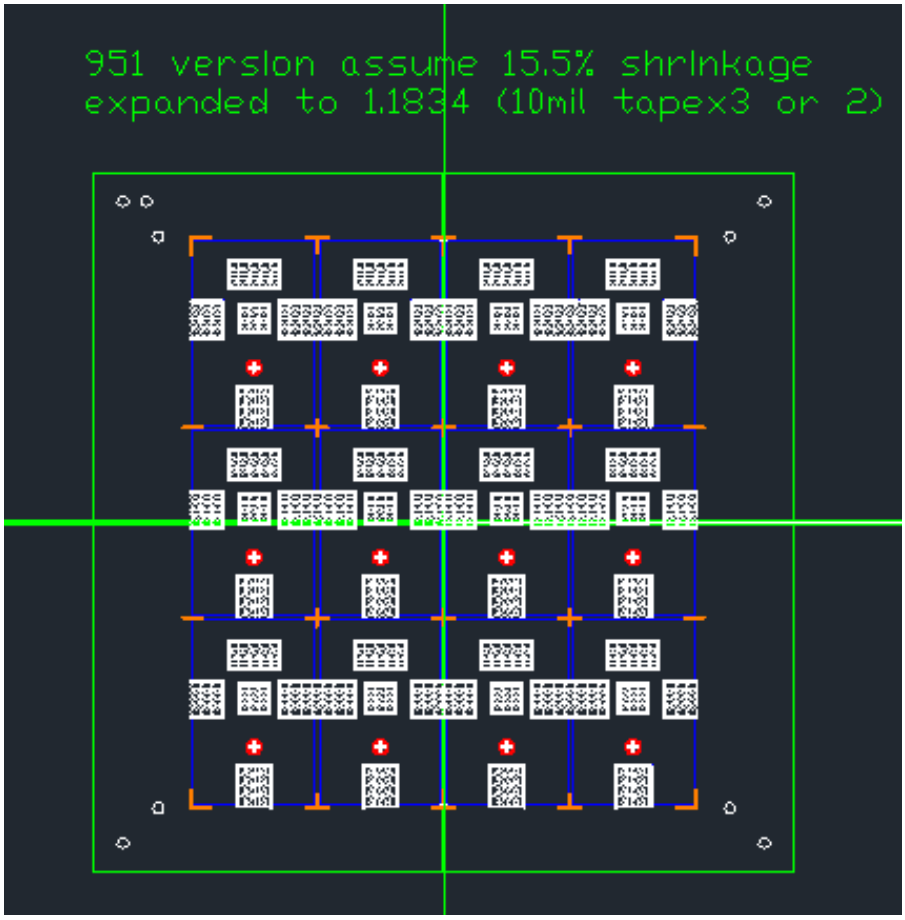


Fig. 6.4 LTCC substrate punch mask design

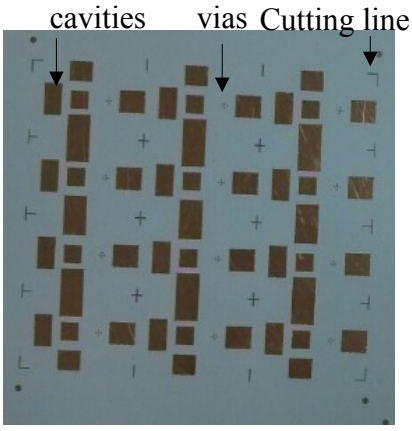


Fig. 6.5 Green tape after punch cavities (photo by author)

plate and the blade were set to be 70°C. Next, the samples are ready to be co-fired in a high temperature oven. The detailed firing profile is given in Appendix A. A typical firing profile has

Fig. 6.6 Isostatic laminator system from PTC (photo by author)

a slow rising temperature up to 350°C with a dwell time of about 1 to 2 hours, when the organic or binders burnout takes place. Then, increase the temperature to 850°C - 875°C and dwell for 10 to 15 minutes. The entire firing cycling lasts for about 4 hours. It takes another 4 hours for the samples to cool down slowly to reduce the thermal stress. Fig. 6.7 shows the samples after co-firing in the oven.

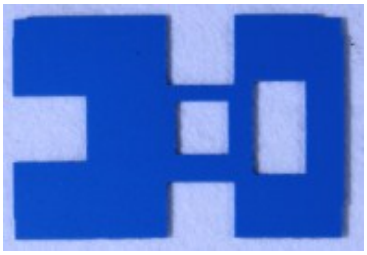


Fig. 6.7 LTCC parts after firing in the oven (photo by author)

Dupont 6277 co-firable conductor paste is screen printed on the green tape with a conventional thick film screen printer. The screen has a 12"x12" frame size. It is made from a 325 mesh count stainless steel with a wire diameter of 0.0009". Its mesh angle is 45° and the emulsion thickness is 0.0005". After printing one side of the substrate, the substrate needs to be post fired in the

oven using the post firing profile given in Appendix A. The other side of the substrate is screen printed with the conductive paste and post fired again. The total time for post firing both sides is about 26 hours. The substrate after post firing of the conductive paste is shown in Fig. 6.8.

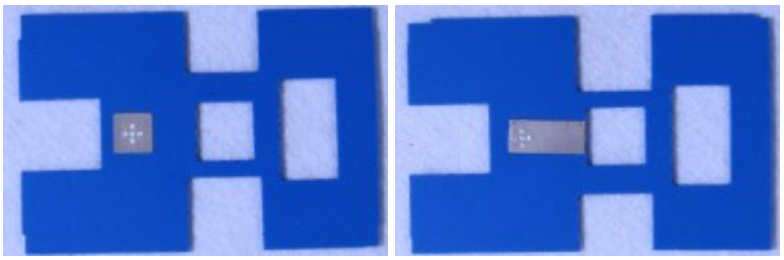


Fig. 6.8 LTCC substrate after post firing of the conductive paste (photo by author)

6.4 Die Top Surface Preparation

The power devices for this application are power MOSFETs and SBD diodes from Cree Power, Inc. In these devices, the pads for the drain of the MOSFETs and the cathode of the diodes are metallized with Ag. However, the source and the anode of the devices are metallized with Al since these devices are originally designed for Al wire-bonding. In this application, since nano silver paste is chosen as the die bonding material, the top sides of both devices have to be metalized with silver. A metallized scheme of Cr/Ni/Ag was evaporated in an Auto 306D evaporator as shown in Fig. 6.9. This process needs to be performed before any further fabrication due to the rapid formation of oxide layer of Al at elevated temperature, and the difficulty to remove this oxide layer, which inhibits a good adhesion with the deposited metal layers [53]. The devices were first cleaned with acetone and isopropyl alcohol (IPA). They were then attached to the chamber top where the thin film metals will deposit. Table 6.11 lists the parameters for depositing the three metal layers. A LTCC fixture as shown in Fig. 6.10 acts as a shadow mask to ensure that the metal was deposited onto the top electrodes. Figs. 6.11 and 6.12 show the die surface before and after depositing the metal layers, respectively.

Fig. 6.9 306D evaporator and metal pellets inside boat (photo by author)

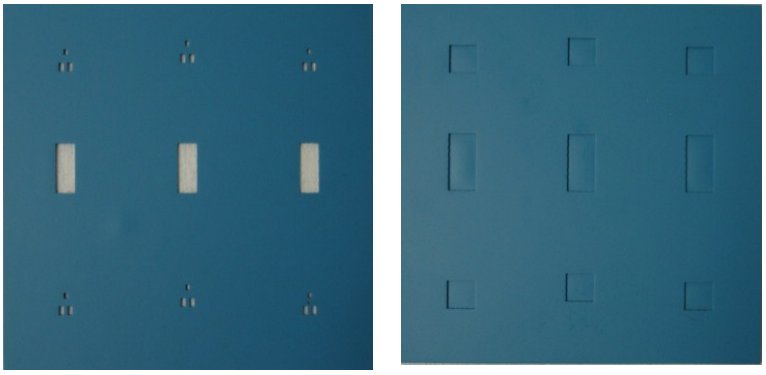


Fig. 6.10 LTCC jig for the die surface preparation (photo by author)

(a) (b)

Fig. 6.11 Original power diode (a) and MOSFET (b) (photo by author)

(a) (b)

Fig. 6.12 Die top surface after depositing thin film metal layers for (a) diode (b) MOSFET (photo by author)

Table 6.1 Parameters for evaporating metal layers on top surface of bare die

Metal	Density(g/cm^3)	Thickness (nm)	Current (A)	Pressure (MB)	Boat type
Cr	7.2	40	1.8	1.6e-6	-
Ni	8.9	100	3.2	1.0e-5	W
Ag	10.5	700	2.0	4.6e-6	Ta

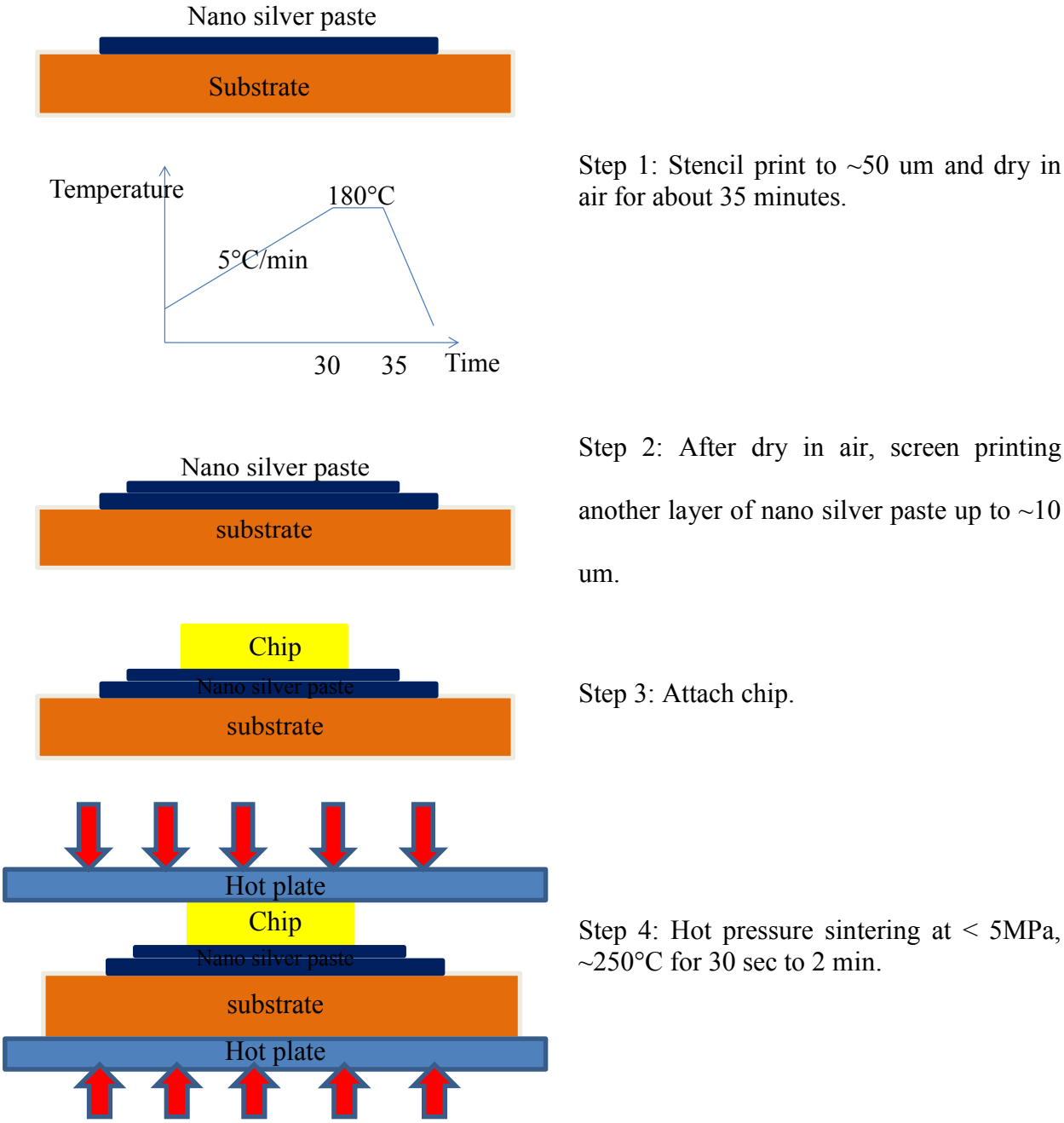
6.5 Interlayer Bonding Process

Before the bonding process, the DBC and LTCC substrates were cleaned using 10% HCl and IPA, respectively. Nano silver paste was stencil printed to bond the dies and the LTCC substrate to the bottom of the DBC substrate.

Fig. 6.13 shows the process for the nano silver paste application. Due to the large bonding area of the SiC diode, the first stencil printed nano silver paste with a thickness of 50 μm was dried from room temperature to 180°C with a ramp up rate of 5°C/min. The soaking time at 180°C was 5 minutes. After this step, another thin layer of nano silver paste was screen printed on top of the first nano silver paste layer with a thickness up to 10 μm. Power devices were put on top of the nano silver paste. The stencil and screen used are shown in Fig. 6.14. A soft polymer blade was used to dispense the nano silver paste and then stencil printing the thin layer as shown in Fig. 6.15. Before the attachment of the LTCC substrate onto the bottom side of the DBC substrate, a high temperature silicone R-2187 was dispensed using a syringe onto the bottom DBC away from the conducting paths. This material is needed to enhance the adhesion between the LTCC and the bottom DBC substrate because of its large elongation property. It also reduces the thermal stress during the temperature cycling process.

After each component is assembled, the assembly was put on top of a hot plate for sintering. A 5Kg weight was placed on top of the assembly with a PTFE sheet in between to distribute the force uniformly on the power devices. The hot plate temperature was first set to 80°C to cure the

silicone and then increased up to 255°C to sinter the nano silver paste in a fume hood as shown in Fig. 6.16. Fig. 6.17 shows the nano silver paste applied on the DBC substrate and the attachment of the power devices and LTCC to the bottom DBC substrate.



Step 1: Stencil print to ~50 um and dry in air for about 35 minutes.

Step 2: After dry in air, screen printing another layer of nano silver paste up to ~10 um.

Step 3: Attach chip.

Step 4: Hot pressure sintering at < 5MPa, ~250°C for 30 sec to 2 min.

Fig. 6.13 Application process for nano silver paste

Fig. 6.14 Stencil (left) and screen (right) used for applying nano silver paste (photo by author)

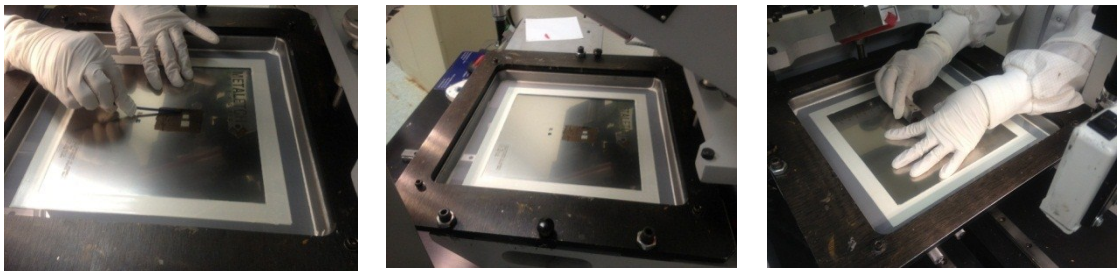


Fig. 6.15 Stencil printing first layer of nano silver paste on DBC substrate (photo by author)

Fig. 6.16 Sintering of nano silver paste on top of a hot plate (photo by author)

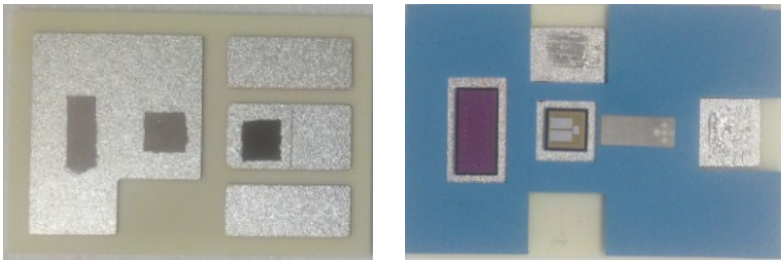


Fig. 6.17 After applying nano silver paste (left) and attach devices and LTCC (photo by author)

6.6 Adhesive Sealing Process

In order to avoid electrical breakdown of the power devices under high voltage operation, an adhesive sealing material was used to fill in the gaps between the power devices and the LTCC substrate. As introduced in Chapter 3, a high temperature silicone R-2187 and a Resbond® 920 pastes are both good candidates for this application. In comparison, Resbond® 920 has a very high operation temperature of about 1000 °C. Before using the Resbond material, it needs to be mixed with water at a ratio of 10:1 in a mixing machine for at least 2 minutes. A small needle was used to apply the mixed sealing material to the gap between the LTCC substrate and the power devices. Fig. 6.18 shows half of the module assembly after this process step.

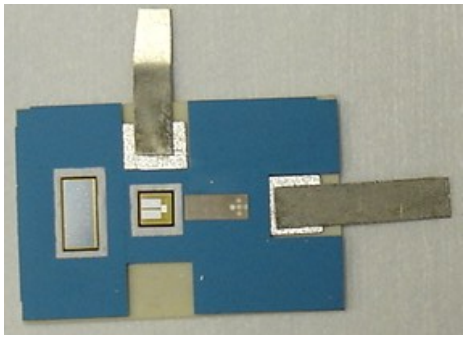
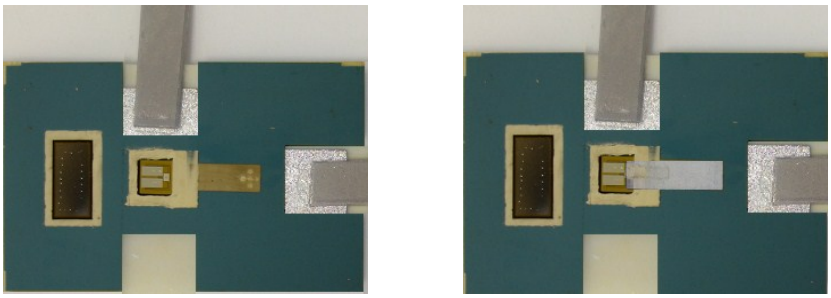


Fig. 6.18After applying adhesive filling material (photo by author)

6.7 Gate formation and top DBC substrate attach

Top side dielectric material is required to improve the flatness of the top surface for the gate thin film metal deposition. The dielectric material used was EPO-TEK®TV1003 from Epoxy Technology, Inc. The advantage of this material is the high temperature operation capability. It can work at 400°C intermittently and its continuous working temperature is 300°C. The dielectric material was screen printed and cured in the oven at 150°C for an hour and 275°C for another hour. Thin film metals Cr/Ni/Ag are deposited on top of the cured dielectric material

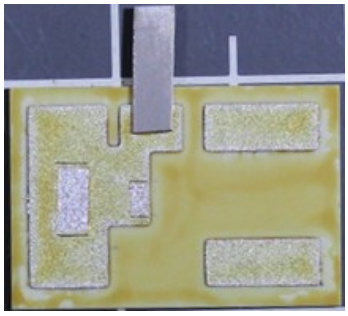
using the same evaporation process described earlier. In order to enhance the adhesion strength of the metals, a thin layer of nano silver paste was screen printed on top of the deposited thin film metal layer and sintered in the open air. Fig. 6.19 shows the half-finished module assembly after gate formation.



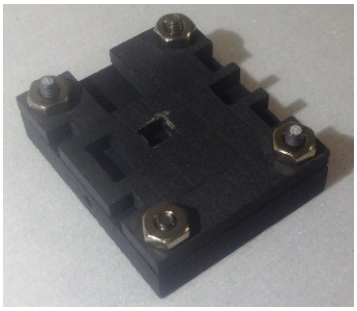
(a) (b)

Fig. 6.19 Half-finished module assembly after (a) dielectric screen printing (b) gate formation (photo by author)

In order to avoid the gate and source electrodes from shorting due to the small gap distance of 0.1mm distance, a thin layer of silicone elastomer R-2187 was applied on top of the gate region using a syringe. The silicone was then cured in an oven at 70°C for 2 hours. The last step is to attach the top DBC lid to the bottom DBC substrate. In order to improve the voltage handling capability, a layer of polyamide imide (PAI) was spin coated on the bottom surface of the top DBC substrate to form a 10 μm thick passivation layer with the aid of a Kapton tape. The material is then cured in an oven at 200°C for an hour. A sample after passivation application is shown in Fig. 6.20 (a). The yellow surface indicated the presence of this PAI passivation layer. Nano silver paste was used again and stencil printed on top of the MOSFET source and diode anode regions. A graphite fixture shown in Fig. 6.20 (b) was used to aid the alignment of the top and bottom substrate attachment as well as to ensure a flat surface during sintering of the nano silver paste.



(a)



(b)

Fig. 6.20 (a) Passivated top DBC lid and (b) fixture for attach bottom and top substrate (photo by author)

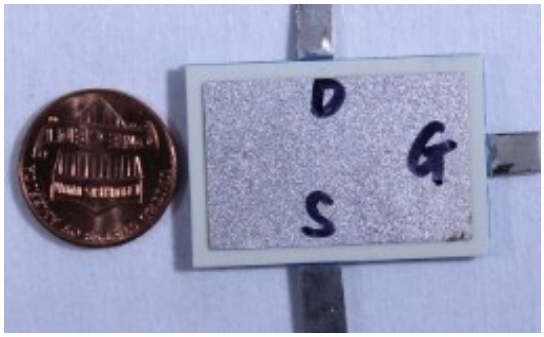


Fig. 6.21 Final module assembly (photo by author)

The last step is to attach the top DBC substrate to the bottom half-finished assembly. The top DBC substrate was attached following the drying and sintering profile of the nano silver paste described in section 6.5. The final module assembly is shown in Fig. 6.21.

6.8 Summary

This chapter describes the fabrication process of the double-sided cooling module. A SiC MOSFET and a SiC diode were packaged in the module. The LTCC substrate was used as the dielectric material and die carrier. A high temperature material Resbond 920 was used to fill in the gap between the power devices and the LTCC die frame to ensure a high voltage operation capability. Gate formation includes the deposition of the thin film metals and the nano silver paste conductor formation. High temperature and high dielectric strength material was spin

coated on top of the DBC substrate to avoid the electrical breakdown. A nano silver paste was applied to attach the power devices to the DBC substrate to eliminate the use of bond wires and to ensure the high temperature operation for the power module.

Chapter 7. Characterization of the module

7.1 Introduction

After the fabrication of the double-sided cooling power module, electrical and thermal performance characterization were performed and described in this chapter. The electrical testing shows the forward and reverse characteristics of the power module to demonstrate its proper device functionality. The high voltage blocking test demonstrates the packaging capability for high voltage operation condition. The steady state thermal resistance measurement is also employed to show the increase thermal performance of the double-sided cooling module compared to the traditional wire-bonded module.

7.2 Electrical test

7.2.1 I-V Curve Characterization

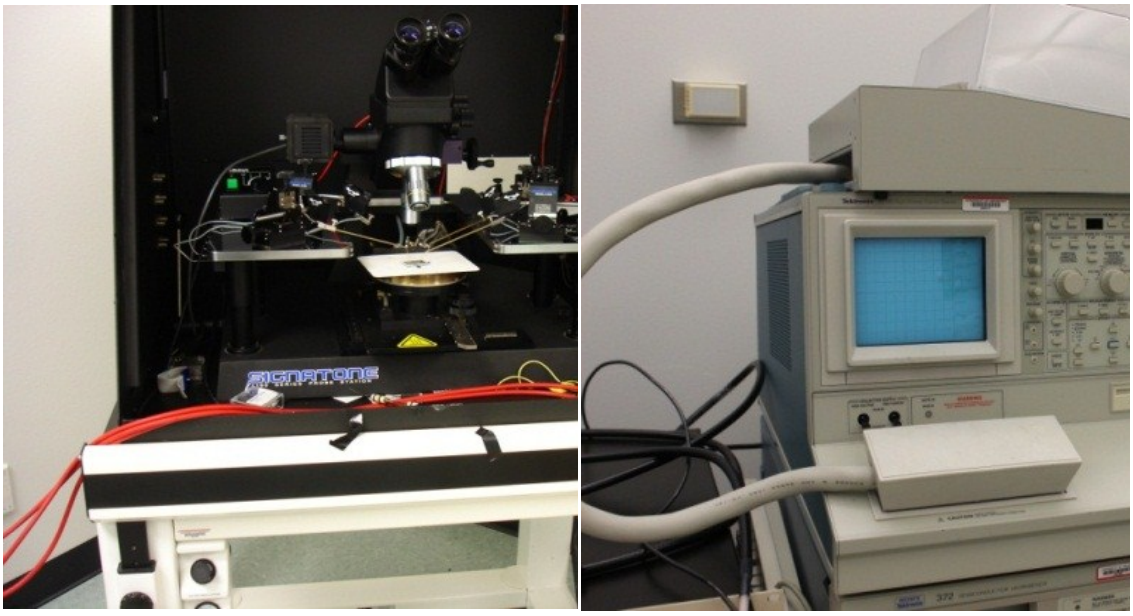
A Tektronix 371B power curve tracer was used to characterize the forward and reverse voltage-current relationships of the power module. In order to reduce the influence of the path resistance caused by the wires and ohmic contact, a four wire Kelvin configuration was used to obtain the I-V curves at different temperatures. By using a Kelvin configuration, the voltage drop across the wires will be excluded from the overall voltage drop across the device under test, which improves the measurement accuracy. The module was heated on top of a hot plate and a thermalcouple was used to monitor the temperature close to the device. The test set up is shown in Fig. 7.1. Fig. 7.2 (a) shows the transfer characteristics for the SiC MOSFET with an anti-parallel SiC SBD diode at a gate-to-source voltage of 10 volts, and Fig. 7.2 (b) shows the I-V curve of the power module. The measurements were performed from room temperature to 200 °C. As can be seen from Fig.7.2 (a), the drain current increases as the temperature increases. For a Vgs of 10V, the drain current is about 16A at room temperature, whereas it increases to

33A at 200°C. For the power MOSFET, the drain current in the linear region can be described by the relationship:

$$i_D = k_n' \frac{W}{L} \left[\left(V_{gs} - V_{to} - \frac{V_{ds}}{2} \right) V_{ds} \right] \qquad (7.1)$$

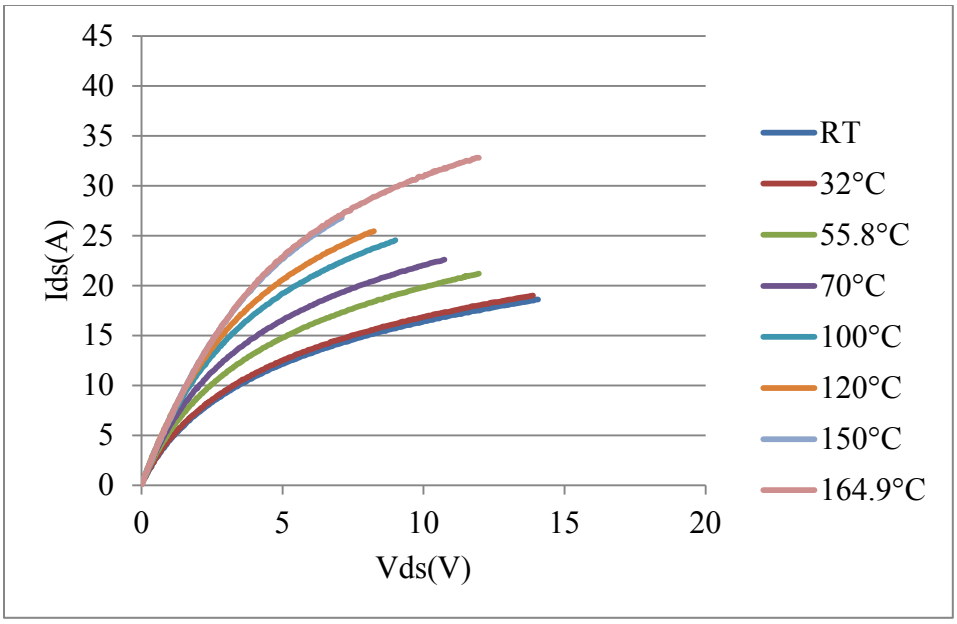
where i_D is the drain current, k_n' is the process transconductance parameter of the MOSFET with the dimension of A/V^2, W is the width of the transistor, L is the length of the transistor, Vgs is the gate/source voltage, V_{to} is the cut-in voltage of the MOSFET, and V_{ds} is the drain-to-source voltage.

Both V_{to} and k_n' are the temperature sensitive parameters in (7.1). Normally, V_{to} and k_n' decreases as the temperature increases. However, in this SiC MOSFET, the effect of V_{to} decrease dominates the transistor characteristics, which gives rise to a corresponding increase in the drain current as temperature increases as shown in Fig. 7.1 (a).

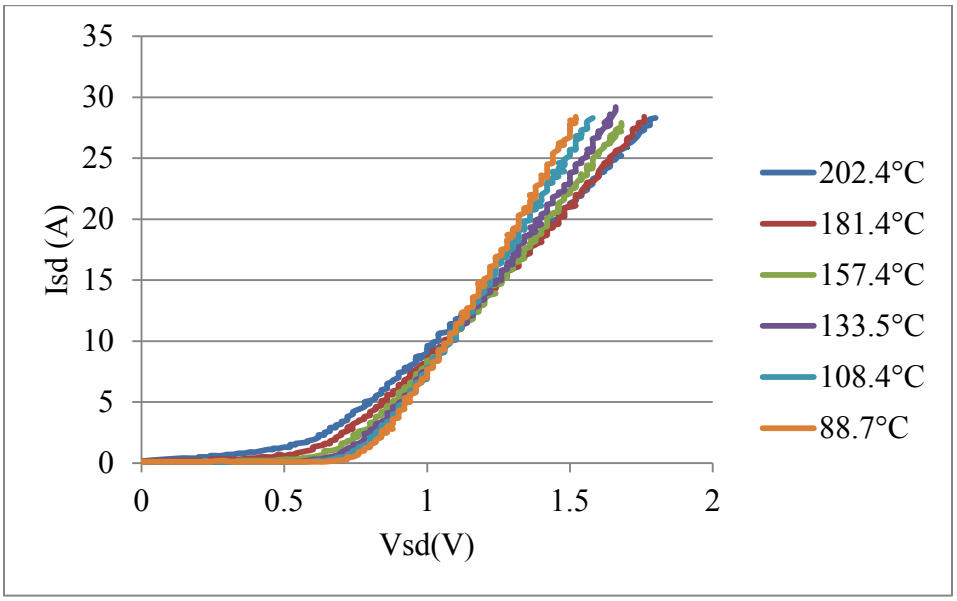


(a) (b)

Fig. 7.1 371B I-V curve characterization set up (a) probe station (b) 371B curve tracer (photo by author)



(a)



(b)

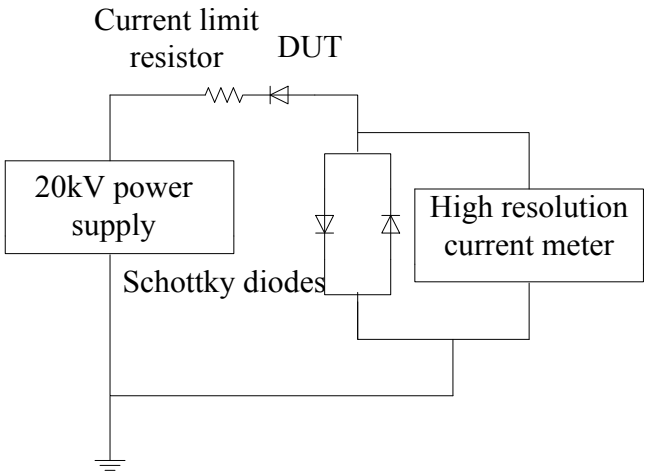
Fig. 7.2 I-V Curve for (a) MOSFET and (b) freewheeling diode at different temperature ratings

As can be seen from Fig. 7.2 (b), the reverse voltage changes as the temperature changes as is essentially the forward voltage characteristic of the SiC SBD diode. As shown, the cut-in voltage for the SiC Schottky barrier diode (SBD) is about 0.79 volts at room temperature. At

202°C, the cut-in voltage decreases to 0.3V. At room temperature, the voltage drop across the SBD is 1.4V for a current of 25A. However, the voltage drop across the SBD increases to 1.67V for a current of 25A at 202°C. This increase in voltage drop is due to the increase of resistivity or decrease of conductivity of the SiC semiconductor as temperature increases.

7.2.3 Leakage Current of the Power Module

The high voltage leakage current measurement for the power module was conducted using the test circuit shown in Fig. 7.3 (a). Fig. 7.3 (b) shows the test set up. The power supply used is the Glassman High Voltage Inc. FL series 1500 W regulated high voltage DC power supply with a resolution of 100 volts. The current limit was set to 2mA. The current limit resistor consists of three 47 kΩ resistors with a power rating of 7W each. A Keithley 2602 high resolution current meter was used to monitor the leakage current through the device. Two clamping Schottky diodes were used to protect the multimeter from any voltage spike. Figs. 7.4 (a) and (b) show the leakage current at different temperature ratings. For the temperature lower than 150°C which is the rating of the device operation temperature, the leakage current is smaller. When the temperature increases to more than 150°C, the leakage current increases dramatically as shown in Fig. 7.4 (b). The reverse leakage current consists of three sources: the body leakage current through junction, the leakage current through the interfacial passivation of the die, and the leakage current through the package [37]. At elevated temperatures, the component of interfacial passivation current will increase dramatically which contributes the major part of the total leakage current [54]. This can be obviously seen from Fig. 7.4 (b), the leakage current at 195°C with a reverse voltage drop of 500 volts is about 1.8mA which is more than 100 times of the leakage current at around 40°C with 1.2kV voltage drop (10 μA).

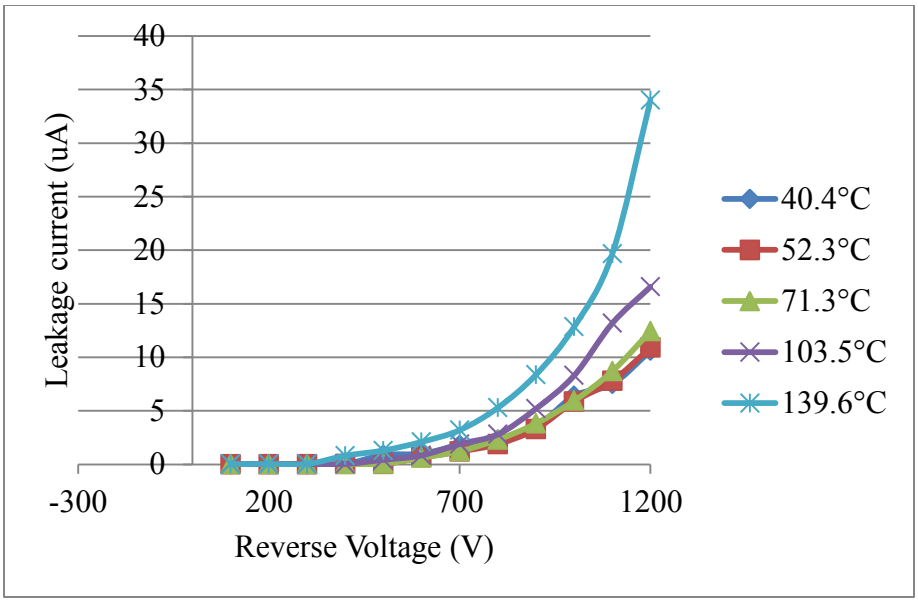


(a)

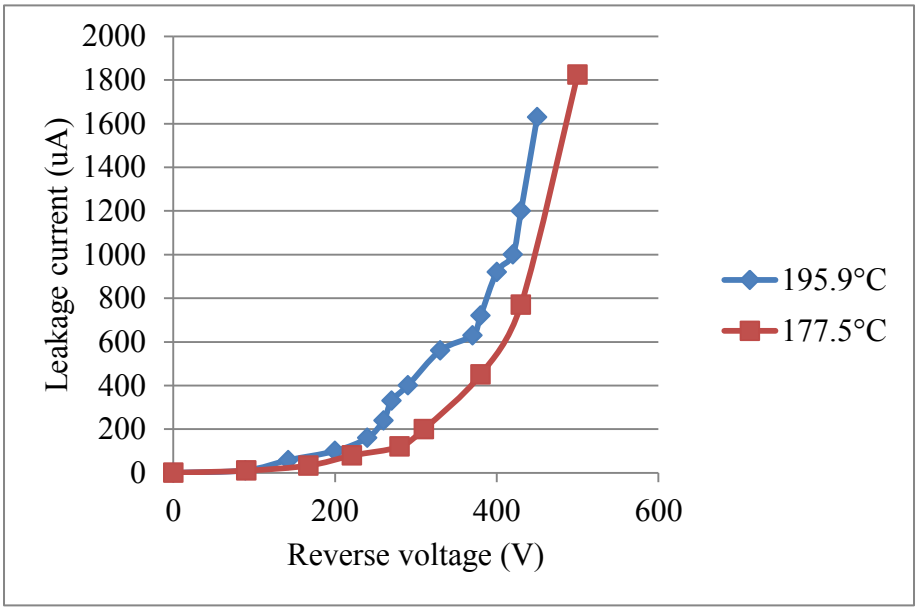
(b)

Fig. 7.3 Leakage current measurement circuit (a) and testing set up (b) (photo by author)

In order to investigate the package influence to the leakage current, an alumina dummy device was made and packaged as shown in Fig. 7.5 to measure the leakage current caused by the package. The measurement used the same set up for the power module leakage current measurement and the measured result is shown in Fig. 7.5. As can be seen, the leakage current for the package at room temperature and at 200°C increases almost linearly with the increasing of the voltage when R-2187 is used as dielectric. At room temperature, the leakage current reaches about 5nA at 1.2kV, and this value is about 16nA at 200°C.



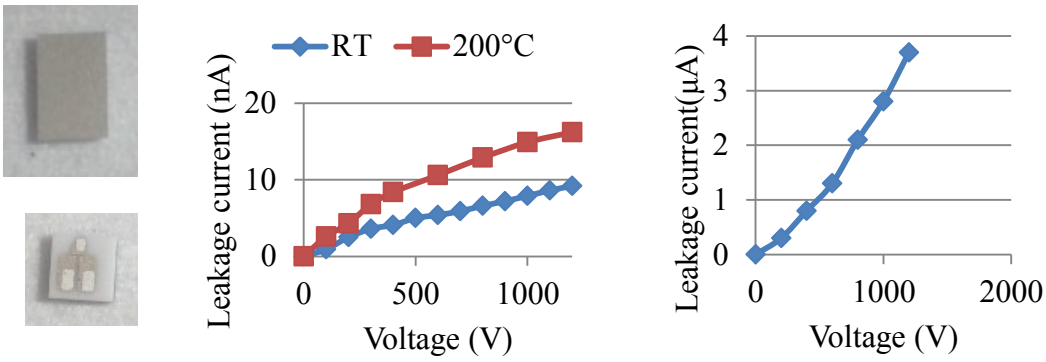
(a)



(b)

Fig. 7.4 Leakage current measurement at different temperature ratings

When Resbond 920 is sued as the dielectric, the leakage current at 200 °C linearly increases from 0 to about 3.7μA. Compared to the power module leakage current, the leakage current caused by the package is negligible.

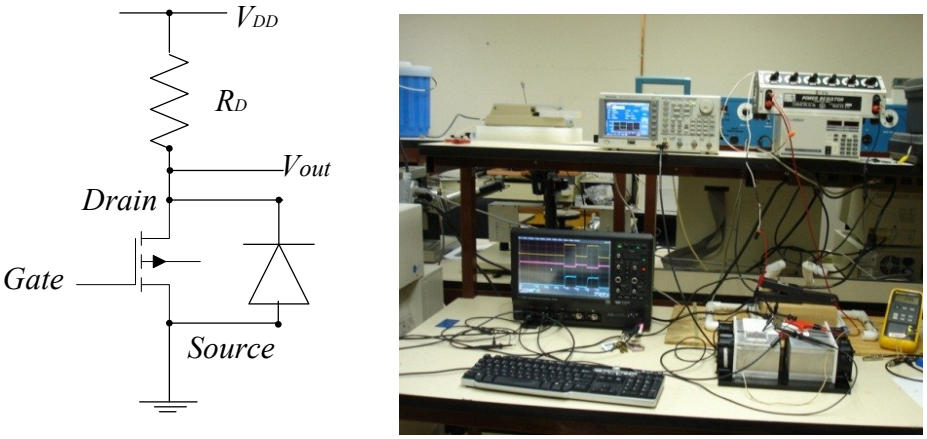


(a) (b)

Fig. 7.5 Leakage current measurement using dummy devices with (a) R-2187 (b) Resbond920 as dielectric material

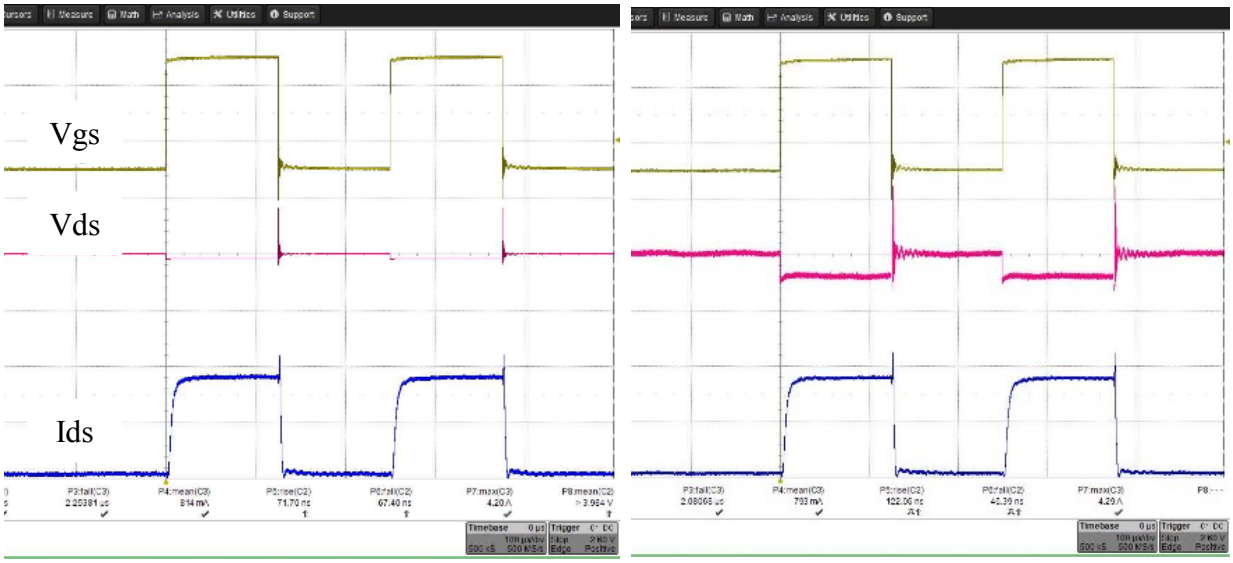
7.2.4 Switching Test

A switching test was performed using the circuit shown in Fig. 7.6. The power supply is a LAMBDA LLS8018. It has a 0 to 18 V output and a current output of 24 A. A Tektronix AFG 3022B function generator was used to generate a voltage pulse for the gate to turn on and turn off the device. The switching waveforms were captured using an HDO4104 oscilloscope from Teledyne Lecroy Inc. A power resistor decade box acted as the drain resistor for the circuit. Fig. 7.7 shows the switching waveforms of the power module. The gate signal is 10 volts with a 50% duty cycle. Each cycle is 0.25 μs. Voltage spikes are obviously seen due to the parasitic inductances. The applied drain voltage is 5V and the drain current is about 4.2A. The rise and fall times for the wire bonded module are 8.3 μs and 2.1 μs, respectively. The voltage spike is 80 volts to 90 volts. For the wire-bondless double-sided cooling module, the rise and fall times are 8.2 μs and 2.2 μs, respectively. The generated voltage spike is 40 volts to 50 volts which is about half of the wire-bonded module, indicating that the parasitic inductance is smaller for the wire-bondless double-sided cooling module.



(a) (b)

Fig. 7.6 Switching test circuit (a) and set up (b) (photo by author)



(a) (b)

Fig. 7.7 Switching waveforms for (a) wire-bondless and (b) wire-bonding module

7.3 Steady State Thermal Resistance Measurement

The thermal resistance measurement of power module is based on the temperature sensitive parameter calibration as shown in Fig. 8.8. The silicon carbide diode has a unique relationship between the on-state voltage drop across the P-N junction and the temperature as shown in equation (7.2) [55]:

$$V_d = \frac{kT}{q} ln(\frac{I_d}{I_s}) \quad (7.2)$$

where, Vd is the voltage across P-N junction (V), Id is the direct current through P-N junction (A), Is is the saturation current (A), K is the Boltzman constant, T is the local temperature (K), and q is charge (c).

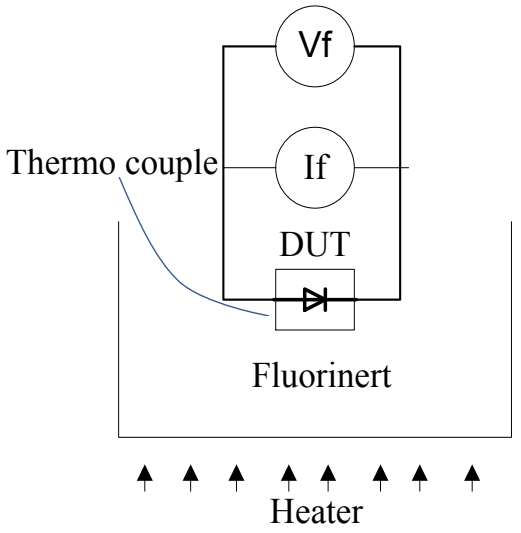


Fig. 7.8 Temperature sensitive parameter (TSP) calibration schematic

During the calibration experiment, the temperature of the fluorinert was first increased to 100°C and the heating of the bath was stopped. Then a 20mA sense current was applied and the forward voltage drop across the junction was measured at the temperature reduced by 5 °C each time. A sample calibration curve for the device is shown in Fig. 7.9.

From Fig. 7.9, the relationship between the junction temperature and the voltage can be expressed by the following equation:

$$V_d = m \cdot T_j + V_0 \quad (7.3)$$

where, Tj is the junction temperature (°C), m is the slope of the curve (V/°C), Vd is the voltage across the P-N junction (V), and V_0 is the voltage of the source coordinate (V).

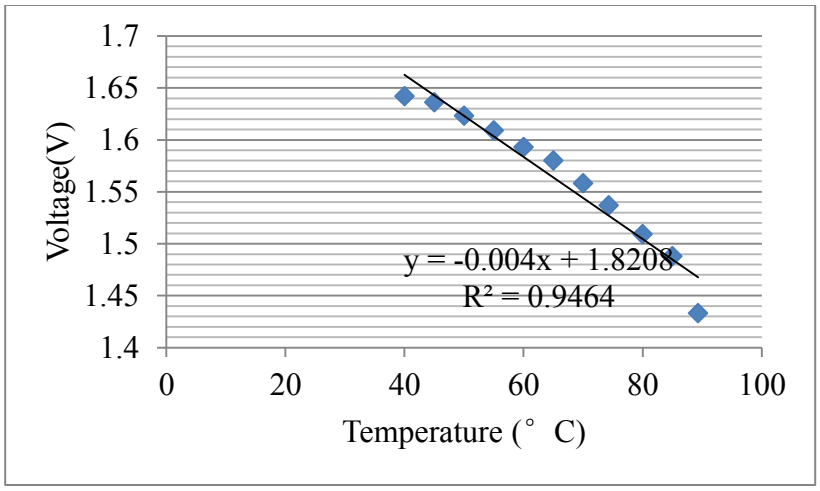
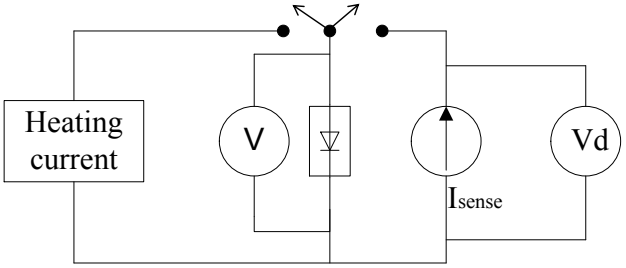


Fig. 7.9 Calibration results of TSP

After the calibration of the temperature sensitive parameter (TSP), thermal resistance of the power module can be measured using the circuit shown in Fig. 7.10. This circuit consists of two configurations. First, the SiC diode is connected to a high current source, which results in an increase of the junction temperature and a temperature gradient will be built up. The second circuit configuration rapidly disconnects the power source and a TSP calibration current is applied to the diode. Thus, the junction temperature can be calculated through the TSP curve. The thermal resistances for the double-sided and single-sided cooling modules are shown in Table 7.1. The measured junction-to-ambient thermal resistance of the double-sided cooling module is 5.48°C/W, which is about 11% lower than that of the wire-bonded counterpart.

Table 7.1 Thermal resistance testing results

TVs	Power (V)	Vj (V)	Tj (°C)	Tamb(°C)	Rth (°C/W)
Double-sided cooling module	19.8	1.286	133.7	25	5.48
Single-sided cooling module	19.8	1.236	146.2	25	6.12



(a) (b)

Fig. 7.10 Thermal resistance measurement circuit schematic (a) and testing set up (b) (photo by author)

7.4 Summary

In this chapter, the forward and reverse characteristics of the power modules were measured up to 200°C. The high voltage testing was conducted up to 1.2 kV which is the rated voltage for the power devices. The I-V curve and high voltage blocking test demonstrate the functionality of the power module up to its allowable operation temperature. Steady state thermal resistance of the power module was measured using a temperature sensitive parameter calibration method. The measured junction-to-ambient thermal resistance of the double-sided cooling module is 5.48 °C/W, which is about 11% lower than that of the wire-bonded module.

Chapter 8. Reliability Assessment of the Power Modules

8.1 Introduction

For power modules, reliability means the extent to which a power module can be expected to perform its intended function under the allowable operation conditions [56]. Reliability is an important quality feature for the power modules due to the fact that the power modules are highly utilized electrically and thermally under actual operation conditions. Premature failures may cause dangers, direct and consequential damage or even high cost to the systems. The minimum requirements of a reliability test are standardized in order to aid the comparison of different products. These tests normally include high temperature reverse bias test (HTRB), high temperature gate bias test (HTGB), high humidity high temperature reverse bias test (THB), high and low temperature storage test (HTS, LTS), temperature cycling test (TC), power cycling test (PC), and vibration test. Conventional power modules have thick copper base plate, which bring a number of disadvantages with regard to reliability. The base plate is normally attached to the heat sink by way of screwing the corners along the outer edges. However, the difference of CTE between the copper base plate and the DBC substrate causes a bending of the base plate during temperature cycles, which means that the base plate may not fully contact with the heat sink across the entire surface due to the base plate bending [24]. This bi-metal effect occurs when two different materials with different CTEs are joined together by soldering. It cannot be fully compensated by the pre-bending of the base plate due to that the solder interface between the substrate and the base plate is a visco-plastic system and the stresses are relieved over time due to plastic deformation [46]. In actual applications, power modules suffer from not only significant temperature fluctuations caused by the power losses of the devices but also passive thermal cycling caused by the ambient temperature change such as the heat sink or coolant

temperature change. For traditional modules, the primary factors affecting the reliability of the power module are the lifetime of the bonding area between aluminum wire and the power devices metal pads, and the life time of the solder layer [57]. The difference of the CTE of substrate and heat spreader generates a significant amount of thermal stress on the bonding layer. Furthermore, the non-uniform attachment, the introducing of the voids and the intermetallics attribute to varying mechanical stresses within the solder, continue to delaminate or/and crack. This begins at the point where the stress is the greatest, normally at the corner of the soldered areas as shown in Chapter 5. Over time, the crack or delamination will keep increasing and eventually lead to the failure of the connection and the power module. This chapter investigated the fatigue life of the bonding layer based on finite element simulation and laboratory investigation.

8.2 Simulation of the Fatigue Life Prediction

Failure of solder joints is a complex phenomenon which involving different mechanics such as grain and phase coarsening, grain boundary sliding, matrix creep, mirco-voids formation and linking, and so on [58]. The criterion used to predict the fatigue lifetime of the solder joints is either based on mechanical cracks or electrical failure. For the failure mechanisms that are related to the crack of the solder joints usually use life prediction models of Manson-Coffin model or analogous model are normally used [59]. The former is based on the creep strains accumulated in one thermal cycle and the fatigue ductility exponent based on the mean temperature and calculated thermal frequency. The latter model calculates the visco-plastic strain energy density release in each cycle and based on that, the crack initiation and crack growth rate are calculated. The final characteristic life is then calculated using the previous parameters. By measuring the actual crack rate using the solder, Rober Darveaux proposed four correlation

parameters K1 to K4 to predict the solder fatigue life [60]. The equations are as follows [60]:

$$\text{Crack initiation: } N_0 = K_1(\Delta W_{age})^{K_2} \tag{9.1}$$

$$\text{Crack growth rate: } \frac{dl}{dN} = K_3(\Delta W_{avg})^{K_4} \tag{9.2}$$

$$\text{Characteristic fatigue life: } N = N_0 + \frac{l}{dl/dN} \tag{9.3}$$

$$\text{Failure free life: } N_{ff} = N/2 \tag{9.4}$$

where K1 through K4 are material parameters, and ι is the characteristic dimension of the selected volumetric region of the solder interface. Normally, this dimension is obtained when the crack propagation has led to a 20% decrease of solder joint surface area [47]. ΔW_{avg} is the strain energy density or plastic work per cycle.

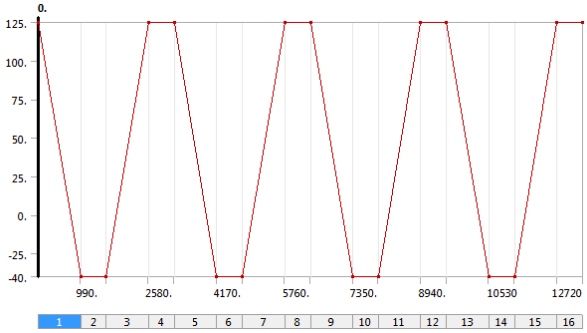


Fig. 8.1 Temperature profile for the thermal cycling

Darveaux volumetric average energy model was used to predict the bonding layer fatigue life based on different bonding materials and different structures of the package under the thermal cycling loading. The advantage of this model over the strain based model is that it considers the fatigue life a function of both stress and strain. The thermal cycling profile is from JEDEC. The temperature ranges from -40°C to 125°C as shown in Fig. 8.1. Four thermal cycles are normally used in the literatures for thermal cycling simulation. The ramp up and ramp down rates are 10°C/min, and the highest and lowest temperature soaking times are both 10 min. Assume all the bodies inside a model were uniformly heat up and cool down. Table 8.1 lists the Darveauxx K1

to K4 crack growth correlation constants.

Table 8.1 Darveaux K1 to K4 crack growth correlation constants [60]

Constant	Value
K1	22400 cycles/psi
K2	-1.52
K3	5.86e-7 in/cycle/psi
K4	0.98

8.3 Simulation Results and Discussion

8.3.1 Stress and strain analysis for the model

The solder or nano silver joint reliability in a package is of great interest. In all figures, the top side of solder layer is the surface that bonded with the SiC die, while the bottom side is the surface that bonded with the DBC as shown in Fig. 8.2.

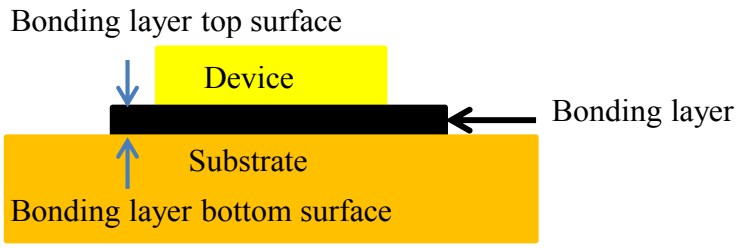


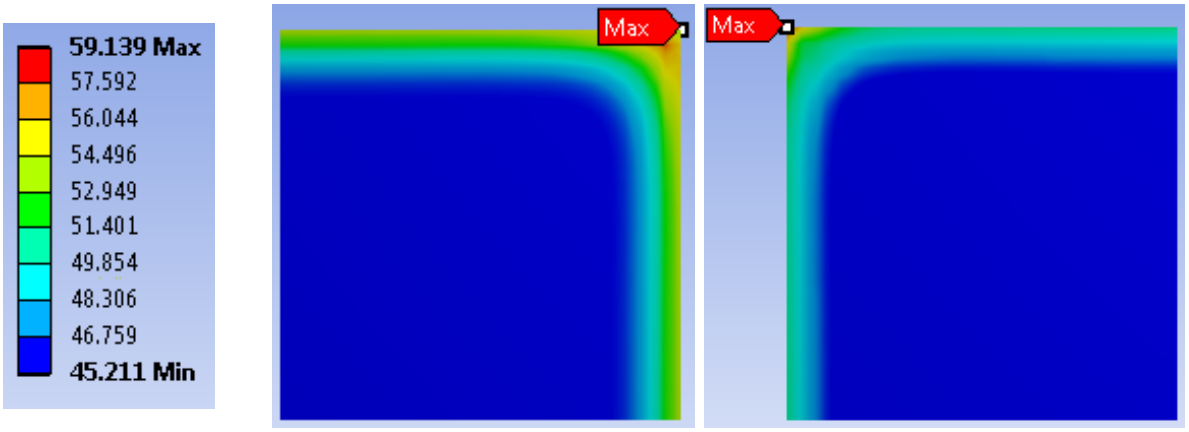
Fig. 8.2 Cross section of different layers for the simulation model

Figs. 8.3 and 8.4 show the equivalent Von-Mises stress distribution within the top and bottom surface of the solder layer at the end of low temperature dwells in the last thermal cycle for a single-sided DBC and a double-sided DBC model, respectively. Figs. 8.6 and 8.7 show the equivalent elastic and plastic strain for the single-sided DBC model, while Figs. 8.8and 8.9 show the equivalent elastic and plastic strain for the double-sided DBC model. It can be seen that the maximum Von-Mises stress, plastic and elastic strain were at the corner of the bonding layer in general. This means the most vulnerable point is located at the corner region of the bonding, which is the first place to fail in the thermal cycling test. From Figs. 8.3 and 8.4, it can be seen

the Von-Mises stress distribution on top and bottom sides of the solder layer is different, and the stresses are higher in the top surface of the solder layer. This is attributed to the CTE mismatch between the SiC device and solder is different from that between the DBC and solder. The maximum values were found on the interface of bonding layer where the power devices reside due to the maximum thermal expansion mismatch within the bonding layer. The double-sided cooling DBC model generates a maximum equivalent stress of 66.75MPa at the lowest temperature of the fourth cycle, compared to 59.14 MPa for the single-sided DBC model. The higher stress in the double-sided cooling module is attributed to the symmetrical structure of the double-sided cooling model, the middle surface of the die is constraint in the horizontal direction, the bonding layer is no longer free to bend, which causes a larger stress on the bonding layer.

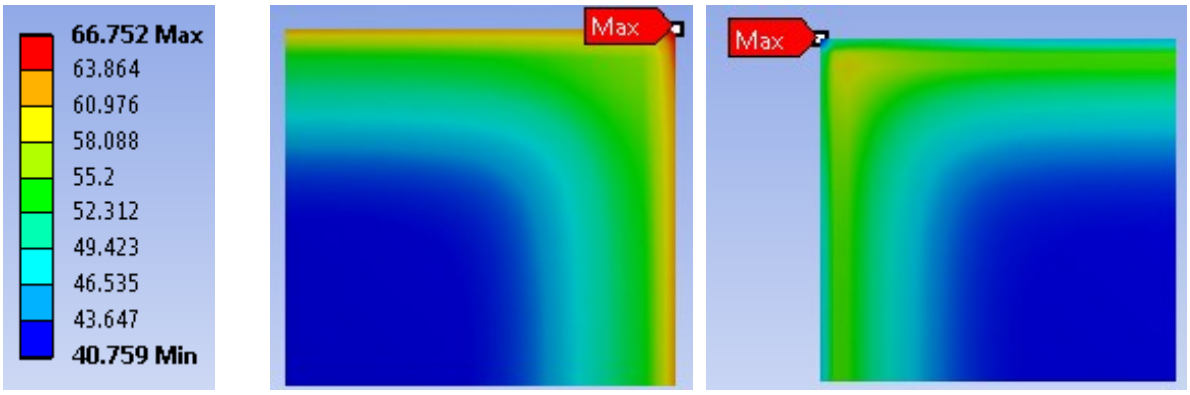
Fig. 8.5 shows the time history of the normalized temperature load, the maximum and minimum Von-Mises stress for the bonding layer. In this thermal fatigue simulation, the first temperature cycle ramps from 125°C to -40°C, and the thermal stress are developed during the cooling period of temperature cycle, primary due to the CTE mismatch between the solder and contacted materials. Stress relaxation at the lowest temperature manifests over 90% of the dwell time and is accompanied by viscoplastic deformation due to the high stress occurred during the dwell time at -40°C. Stress decrease maintains during the temperature increase period. Diffusion creep effect dominates at the highest temperature dwell time. It can be seen that the higher stress occurs at lower temperatures while the smaller stress occurs at the higher temperatures.

During the temperature cycling, a small stress change occurred at the end of the low temperature dwell for the minimum stress spot at the center region of the bonding layer. It is likely that the bonding material in the center region could not release the large stress quickly due to the material property.



(a) (b)

Fig. 8.3 Equivalent Von-Mises stress distribution for the single-sided DBC module (a) solder layer top surface (b) solder layer bottom surface (Unit: Pa)



(a) (b)

Fig. 8.4 Equivalent Von-Mises stress distribution for the double-sided DBC module (a) solder layer top surface (b) solder layer bottom surface (Unit: Pa)

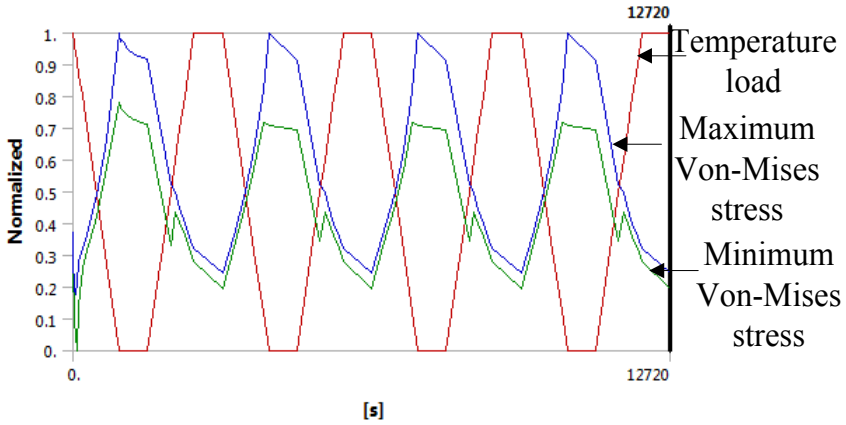
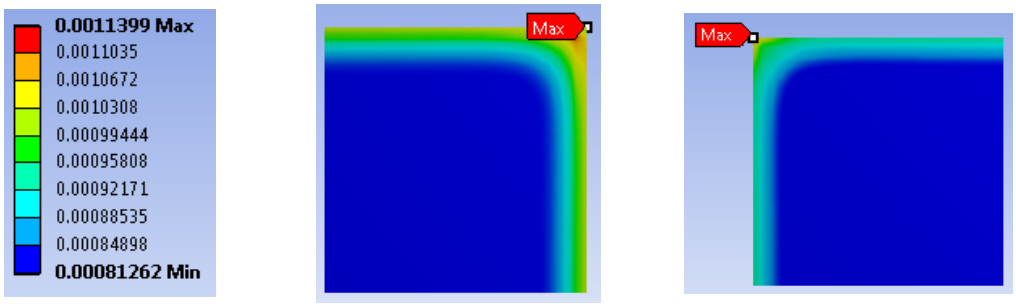


Fig. 8.5 Time history of temperature load and Von-Mises stress

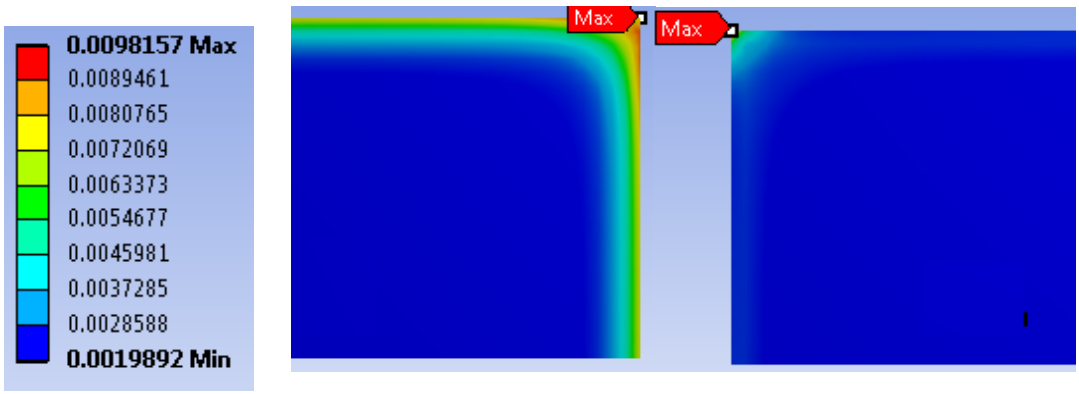
When the solder layer suffers from these stresses, it will undergo deformation. If the stress is below the yield point, the deformation of solder lattice is small and the stress and strain, and the relationship is linear. This process is reversible and the strain resulting is called the equivalent elastic strain as shown in Figs. 8.6 and 8.7 for single-sided and double-sided cooling modules, respectively. When the stress is beyond its yield point, the solder undergoes a permanent deformation along with the plastic strain. Figs. 8.8 and 8.9 show the plastic strain distribution for the single-sided and double-sided cooling modules, respectively. Unlike elastic strain, plastic strain is irreversible, and it is caused by the motion of crystal defects in the solder material due to high loads caused by the large temperature changes. From Figs. 8.5 to 8.8, for both single-sided and double-sided cooling modules, the elastic strain of single-sided cooling module is 0.0011 m/m and 0.0012 m/m, which is much smaller than plastic strain, 0.0098 m/m and 0.031 m/m for single-sided and double-sided cooling modules, respectively.

Both the elastic and plastic deformations for the double-sided cooling module are larger than those of the single-sided cooling module. This is caused by the larger stress induced inside the double-sided cooling module than that inside the single-sided cooling module. These figures also show that the plastic deformation dominates the major part of the total deformation during the temperature cycling process, which can also be seen from the normalized value in Fig. 8.10.



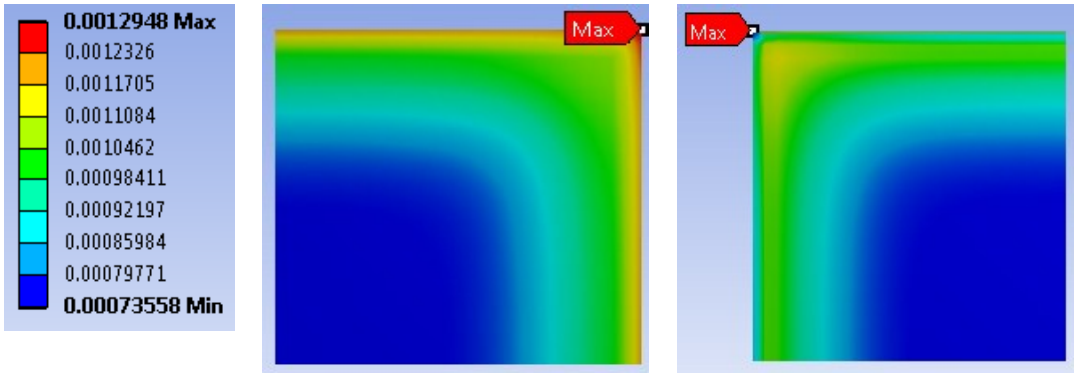
(a) (b)

Fig. 8.6 Equivalent elastic strain distribution for the single-sided DBC module (a) solder layer top surface (b) solder layer bottom surface (m/m)



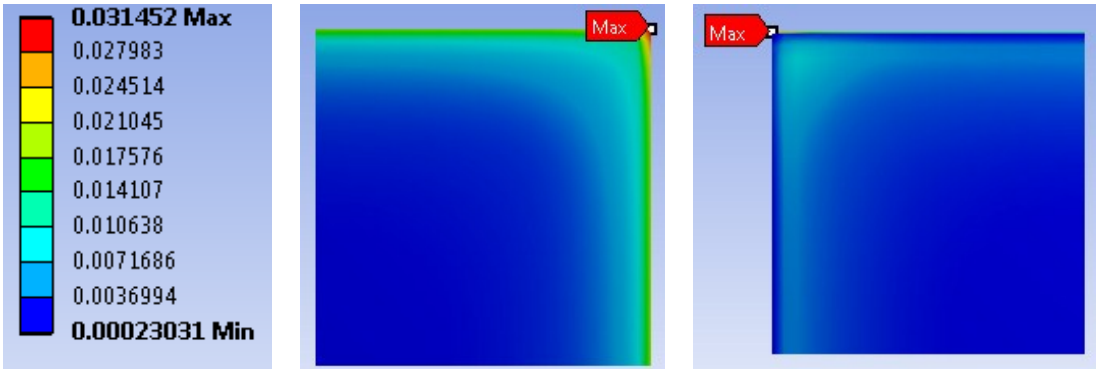
(a) (b)

Fig. 8.7 Equivalent plastic strain distribution for the single-sided DBC module (Unit: m/m)



(a) (b)

Fig. 8.8 Equivalent elastic strain distribution for the double-sided DBC module (Unit: m/m)



(a) (b)

Fig. 8.9 Equivalent plastic strain distribution for the double-sided DBC module (m/m)

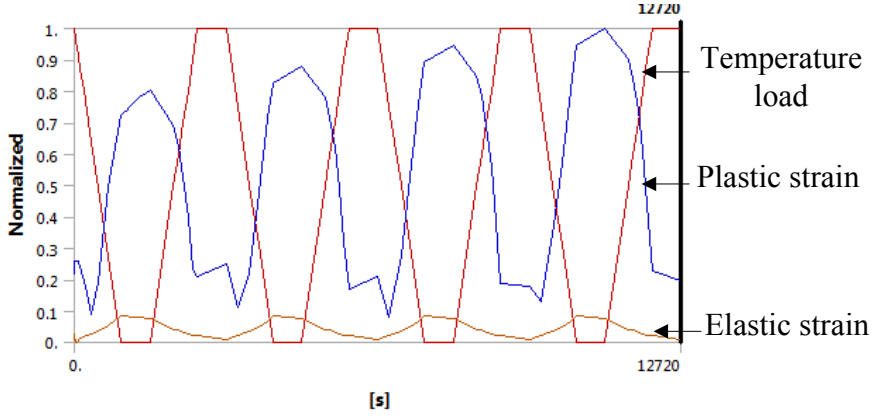


Fig. 8.10 Time history of temperature load, plastic and elastic strain for solder layer

Figs. 8.11 and 8.12 show the stress-strain hysteresis loop in the solder layer for single-sided and double-sided cooling modules, respectively. A strain hardening process can be clearly seen as temperature cycles. This can be explained in Fig. 8.13. When temperature reduces, the stress and strain increases linearly until they reach the yield point A of the solder. After this, the solder undergoes a plastic deformation until point B where the unloading of the solder starts, and a permanent deformation occurs which is represented by OD. The strain from DC is the reversible elastic deformation. During the plastic deformation, an increasing stress is required to produce an additional plastic deformation. This is because the solder material dislocation chains pile up as the plastic deformation increases, which lead to the increase of plastic flow stress, as such a continued increasing stress is required to maintain the increased dislocation beyond the yield point [61]. In Figs. 8.11 and 8.12, stresses and equivalent strain of the solder layer increase when the temperature reduces from 125°C to -40°C (path a-b). During b to c, there is stress relaxation with accumulated strain. This is due to the increasing dislocation, diffusion of vacancies, and sliding of grains past each other [62]. On the one hand, creep allows the stress to be relaxed and minimizes the stress concentration points in solder. However, creep causes large deformation which leads to microstructure degradation in the solder material. When the

temperature subsequently increased from -40°C to 125°C, the Von-Mises stress reduces as indicated by the path c-d. Finally, path d to e shows that due to high temperature creep during the dwell time, the stress relaxes at the end of a temperature cycle. It can also be seen that at each end of temperature cycles, there is a fluctuation along the hysteresis curve. This is probably caused by the residual stresses and strains available at the beginning of the next temperature cycle. Figs. 8.11 and 8.12 also show that the stress for the double-sided cooling module reaches a higher value (73.4MPa) than that of the single-sided cooling module (64.67MPa) during the temperature cycling processes.

This is similar to the previous discussion about the Von-Mises stress. The area of the hysteresis loop represents the inelastic energy in each cycle. The dissipated energy per cycle for the double-sided cooling module is larger than that of the single-sided cooling module due to the higher stress in the double-sided cooling module. This energy decreases the ductility of the solder, thus causes it to fail.

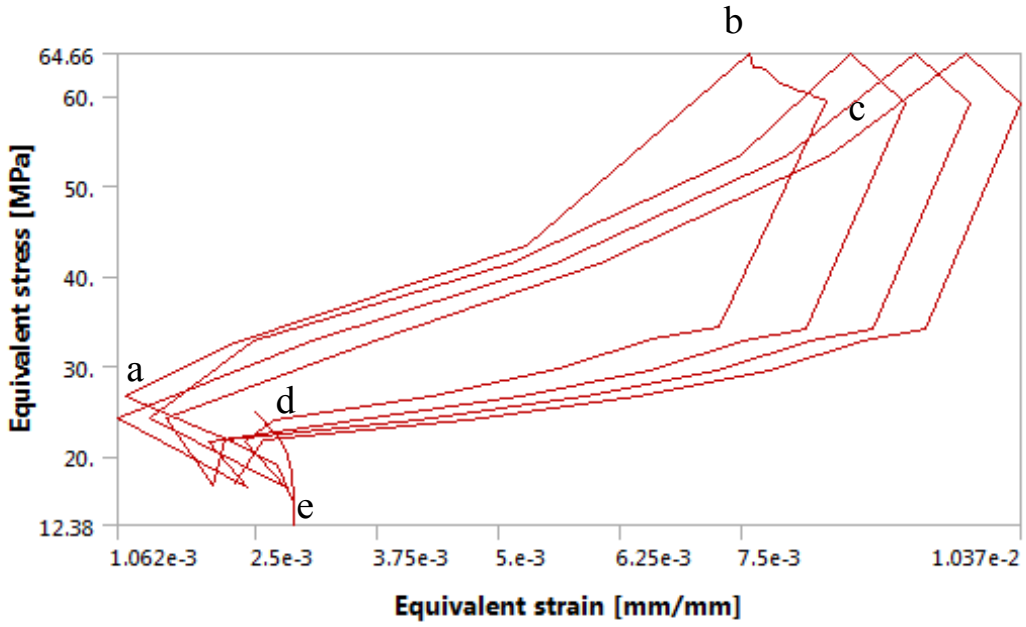


Fig. 8.11 Stress-strain hysteresis loop for single-sided cooling module

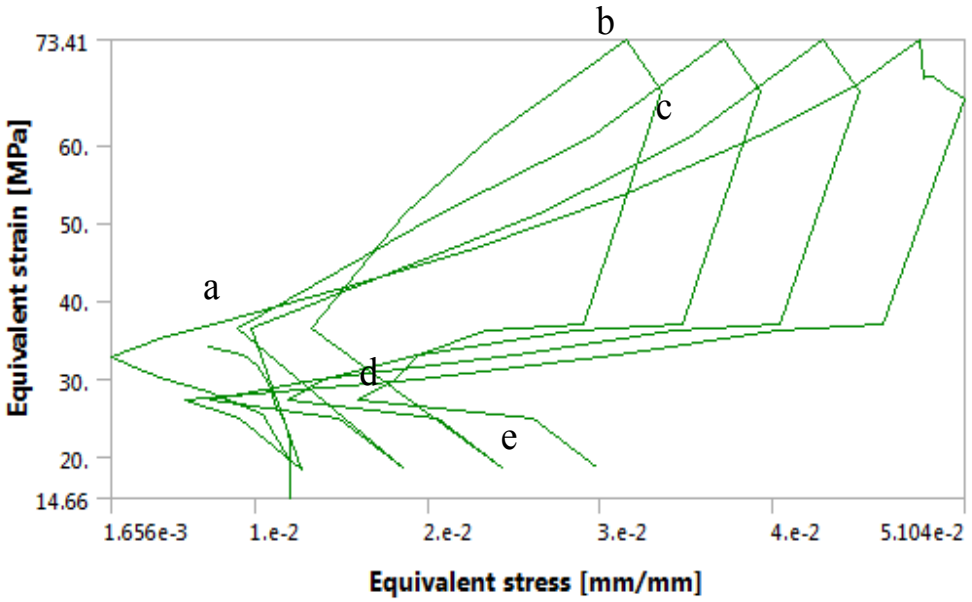


Fig. 8.12 Stress-strain hysteresis loop for double-sided cooling module

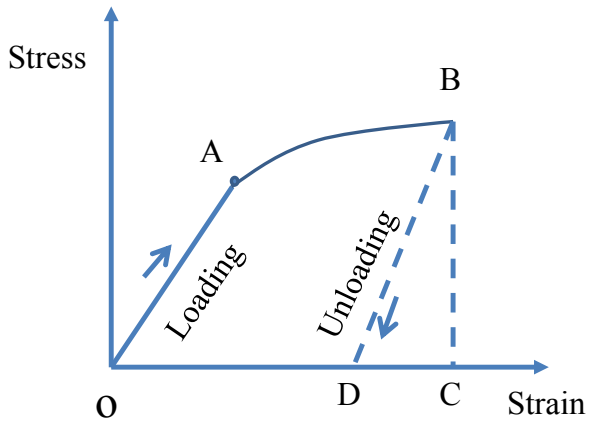


Fig. 8.13 The loading and unloading process for the solder

8.3.2 Fatigue Life Prediction

The fatigue life for the bonding layer prediction was calculated based on volume-averaged visco-plastic strain energy density accumulated per cycle using Robert Darveaux method, which is described in equations (8.1) through (8.4). The thickness of the entire bonding layer, 2 mils, was used to calculate the visco-plastic strain energy density for precise fatigue

cycles. The plastic work distribution and evolution during the temperature loading history for both single-sided DBC module and double-sided DBC module are shown from Figs. 8.14 to 8.17. As can be seen, the maximum plastic work at the end of the low temperature dwell within the last thermal cycle for both models is located at the corner region. From Figs. 8.15 and 8.17, the plastic work is an accumulated process and eventually leads to the failure of the bonding joints. The delta plastic work ($\triangle u$) in each cycle can be calculated from the plastic work curve as shown in Figs. 8.15 and 8.17. This value is coincident with the value of the surface area of the hysteresis loop in each cycle discussed previously, which represents the inelastic work done on the solder. Fig. 8.18 shows the simulation convergence process, and the total simulation time for a single model is about 3.5 hours due to the non-linear material properties used in the simulation. In the simulation, iterative solver instead of direct solver was used to save the memory. The simulation results are listed in Table 8.18. The simulated single-sided cooling module with a base plate yielded a predicted failure free life of 927 cycles for the large area solder between the DBC substrate and the copper base plate. With the base plate remove, the fatigue failure free life increases to 1583 cycles for the solder that bonded the SiC device to the DBC substrate. Compare to the module without a copper base plate, the module with a base plate is prone to failure under thermal cycling. Simulation of the double-sided DBC module yielded a predicted failure free life of 1335 cycles for the solder joints, which is 248 cycles less than that for the single-sided DBC module without a base plate. Clearly, the double-sided DBC module has a higher stress in the solder layer than that of the single-sided DBC module under thermal cycling. When nano silver paste is used as the bonding material instead of the SAC 405 solder alloy, the predicted failure free life for the double-sided DBC module without a base plate is 1465 cycles, which shows the improvement of reliability by using the nano silver joints. Compared to the

single-sided cooling model with large area solder attachment, nano silver joint compensate the reliability loss caused by the double-sided DBC structure, the free life of the double-sided cooling model increased by 538 cycles compared to the large area solder attached single-sided cooling model.

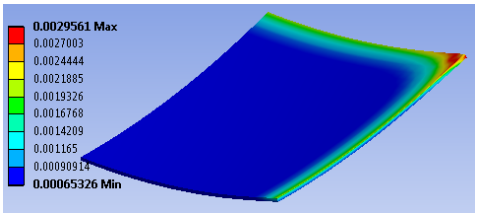


Fig. 8.14 Plastic work distribution for the single-sided DBC module (Unit: J)

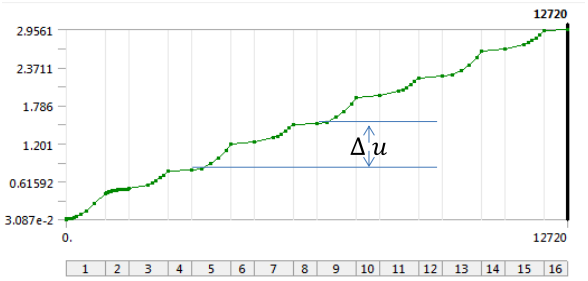


Fig. 8.15 Time history of plastic work for the single-sided DBC module

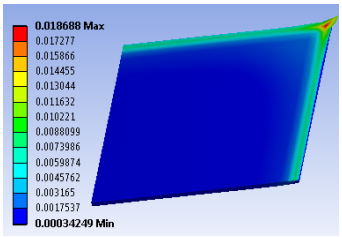


Fig. 8.16 Plastic work distribution for the double-sided DBC module (Unit: J)

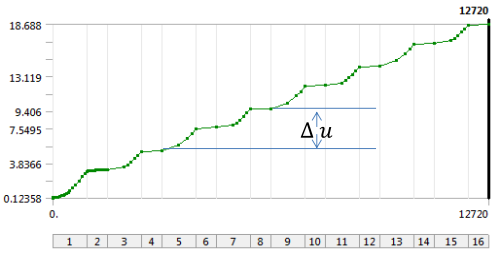


Fig. 8.17 Time history of plastic work for the double-sided DBC module

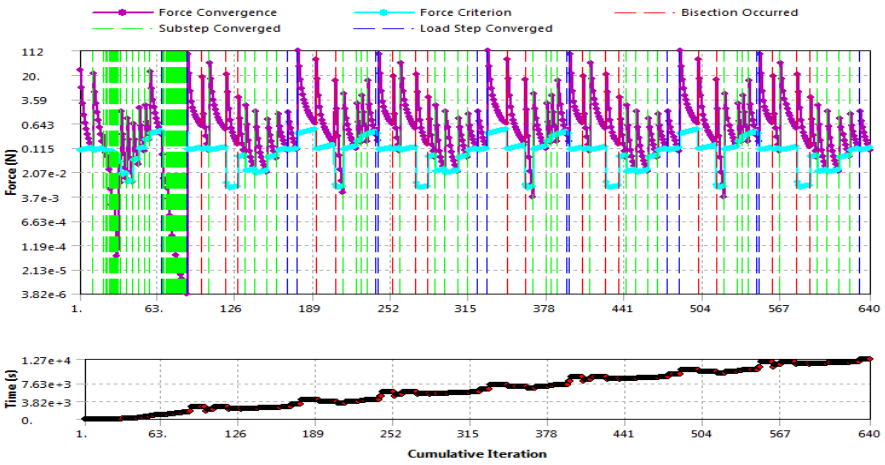


Fig. 8.18 Convergence process and the timing of the simulation for fatigue life prediction

Table 8.2 Simulation results of fatigue life prediction of different packaging structures

Life prediction items	Single-sided Cooling with SAC405 solder bonding with base plate (large area solder bond with base plate)	Single-sided Cooling with SAC405 solder bonding W/O base plate (solder bond with device)	Double-sided Cooling with solder bonding W/O base plate (solder bond with device)	Double-sided cooling with nano silver paste W/O base plate (Ag bond with device)
Delta plastic work in the first cycle (PSI)	46.86	16.13	25.44	20.6
Delta plastic work in the second cycle (PSI)	66.18	26.8	38.72	31.7
Delta plastic work in the third cycle (PSI)	54.51	24.81	34.95	27.78
Crack initiation (cycles)	51	169	98	101
Crack growth rate (mm/cycles)	7.46E-4	4.135E-4	4.826E-4	4.382E-4
Smallest characteristic dimension (mm)	1.346	1.24	1.24	1.24
Crack propogation (cycles)	1802	2998	2569	2829
Characteristic life (cycles)	1853	3167	2670	2930
Failure free life (cycles)	927	1583	1335	1465

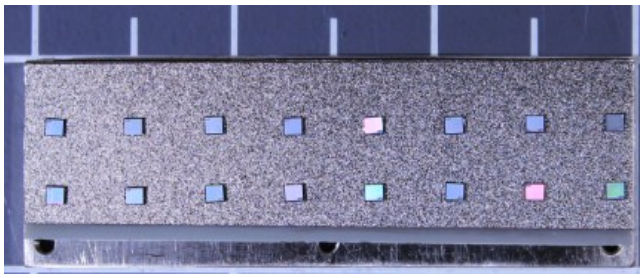
8.4 Thermal Cycling Tests

8.4.1 Experiment Preparation

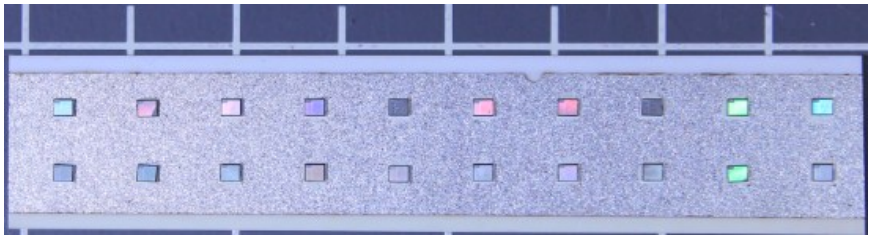
To investigate the influence of thermal cycling on die bonding, three sets of devices were bonded onto the DBC substrate using solder and nano silver die attachment. The devices used were the mechanical version of the JFET SJEC120R100 from SemiSouth. In the first set of the sample, lead free solder preform SAC405 was used to solder the SiC devices to the AlN DBC substrate as well as the DBC to the copper substrate as shown in Fig. 8.19 (a). The second set of samples was prepared using the nano silver paste and dies were attached to the Al_2O_3 DBC with Ni/Ag coating on top of the copper layer as shown in Fig. 8.19 (b).The sintering pressure used for the power devices are 1.15MPa for the single layer sintering. The third sets of the devices was also attached to the Al_2O_3 DBC substrate using nano silver paste, however, the sintering pressure was increased to 2.73MPa. The AlN DBC substrate has 12mils copper plates on both sides of the 25mils thick AlN ceramic, while the Al_2O_3 DBC substrate has 8mils of copper plates on both sides of the 12mils thick ceramic. Aluminum and graphite fixtures were made to fix the positions of the devices as shown in Fig. 8.20 (a). A 76 mils diameter and a quarter inch deep hole was drilled in the bottom of the Al fixture to place the thermocouple in to monitor the soldering or sintering temperature. When bonding the power devices using the nano silver paste, PTFE dices as shown in Fig. 8.20 (b) were placed on top of the devices to ensure a uniformly distributed force on top of the devices as well as to protect the surface of these devices.

Three double-sided cooling power modules were fabricated and thermal cycling was performed in a temperature cycling oven along with the die attach samples. Before the experiment, all modules were characterized for their forward and reverse I-V characteristics. Fig. 8.21 shows the three samples for the thermal cycling test. The JEDEC22A-104D standard was adopted for the

temperature cycling tests. The test set up is shown in Fig. 8.22. Liquid nitrogen was used as the cooling medium.

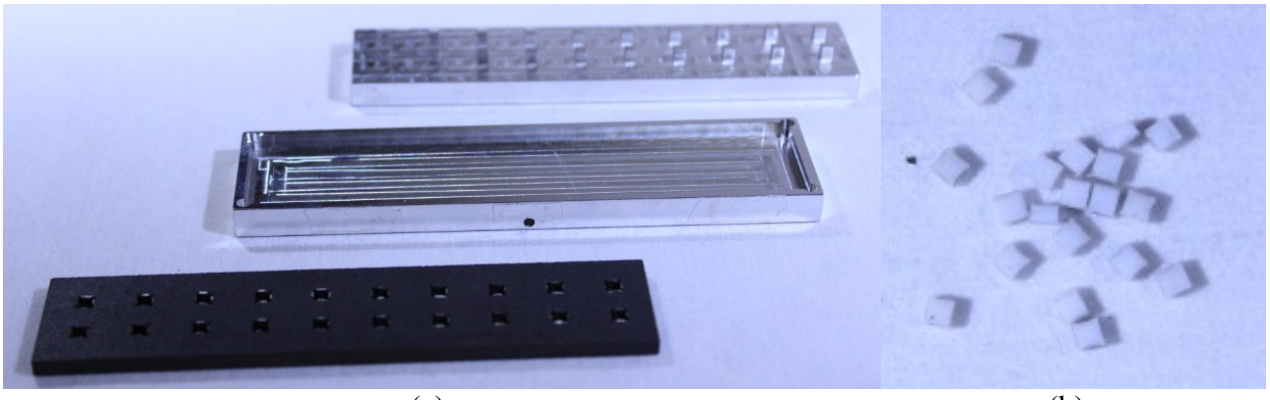


(a)



(b)

Fig. 8.19 Thermal cycling samples (a) Solder attachment (b) nano silver paste attachment (photo by author)



(a) (b)

Fig. 8.20 Fixture used to sinter nano silver paste (a) Aluminum and graphite fixture (b) PTFE dice (photo by author)

Fig. 8.21 Power modules for thermal cycling experiment (photo by author)

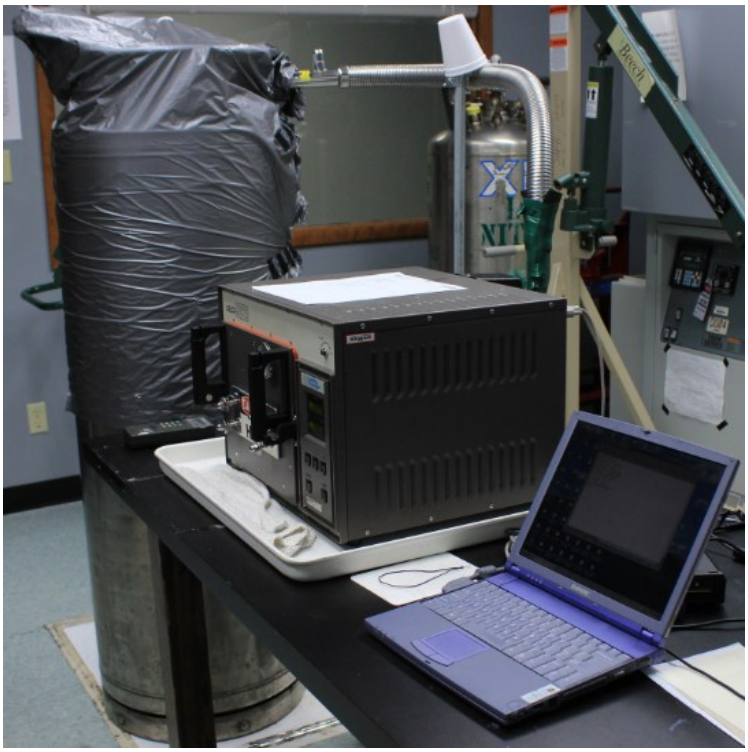


Fig. 8.22 Thermal cycling experiment set up (photo by author)

The samples were taken out from the oven for evaluation after completing certain amount of cycles. Both destructive and nondestructive tests were performed to check the bonding quality. The nondestructive test was performed using a scanning acoustic microscope (SAM) from Sonix as shown in Fig. 8.23. For the SAM inspection, a 75 MHz transducer and C-scan mode were used to check the voids, cracks and delamination of the interested layer. TAMI (Tomographic Acoustic Micro Imaging) region was employed to allow the focus of all depth and the images of different layers obtained all at once [63]. Front surface follower is enabled during scanning.

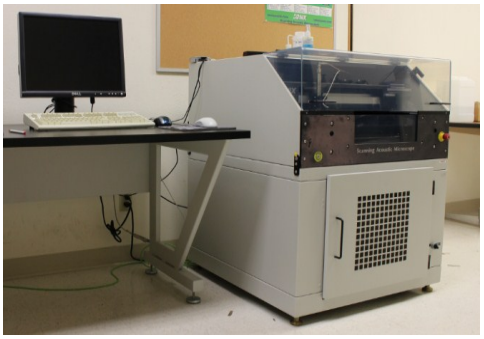


Fig. 8.23 Scanning acoustic microscope (photo by author)

Fig. 8.24 shows a typical C-scan of the SAM. The first peak is the front surface of the SiC device since the signal from the top surface metal pad of the device is the first reflected signal and it is very strong. The second peak is the SiC device itself since this is the second material in the scanned layers. The third peak is the die back metallization and the forth peak is the bonding layer which is the layer of interest. TAMI region should include the interested layer and the value of the " data gate" must be set smaller enough to obtain the image of this layer.

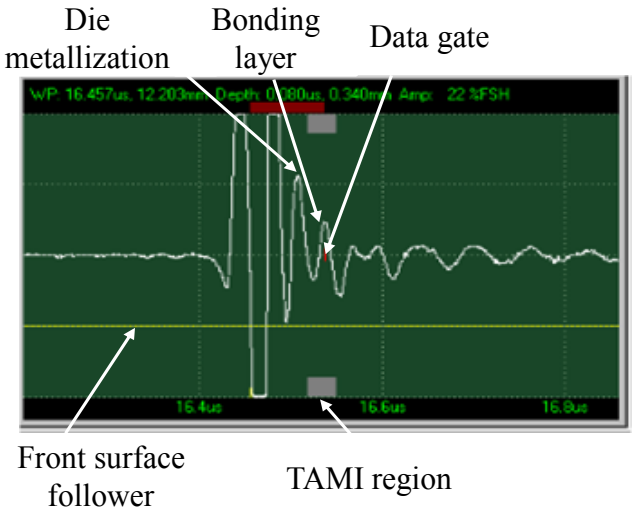
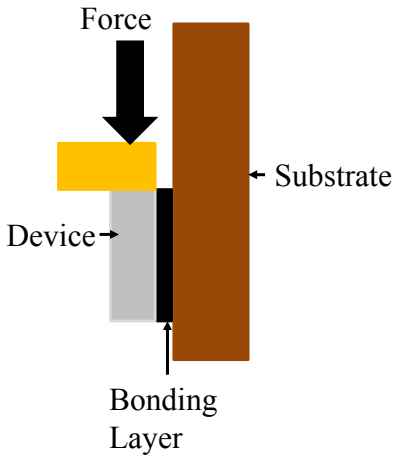


Fig. 8.24 SAM scan of die bonding sample

A shear tester from Quad Group was used to shear the die from the substrate. The shear speed was set to be medium. Fig. 8.25 shows the shear tester and a schematic of the die shearing process.



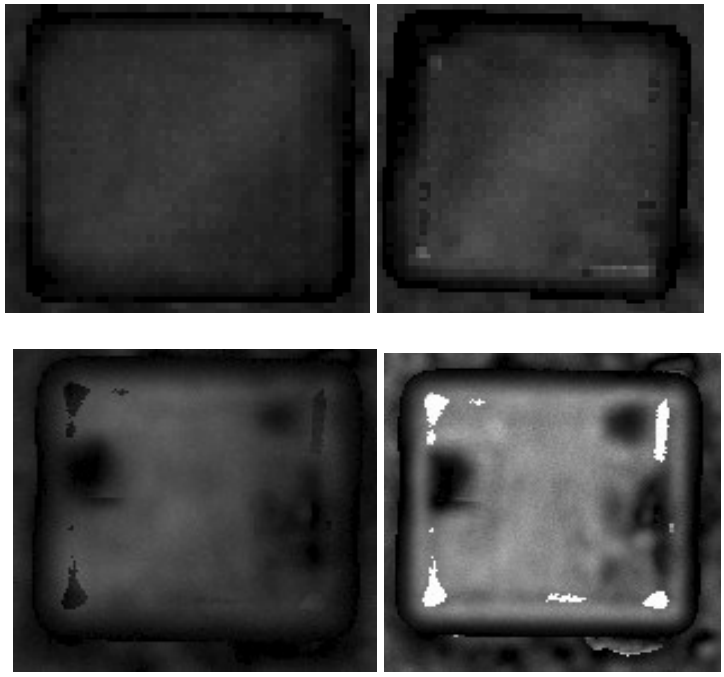
(a) (b)

Fig. 8.25 (a) Shear tester, and (b) die shear off illustration (photo by author)

8.4.2 Thermal Cycling Results and Discussion

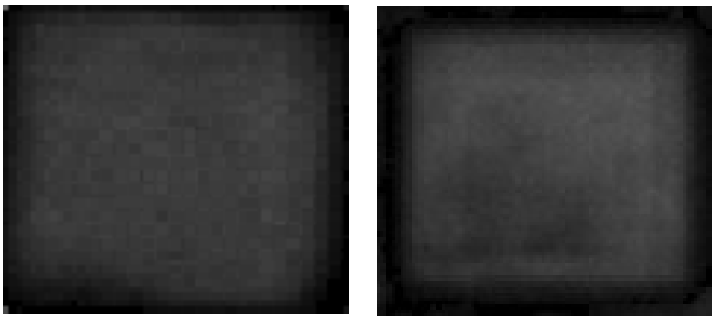
8.4.2.1 Solder and Nano Silver Joints for the SiC Devices

Figs. 8.26 and 8.27 show the SAM images of the thermal cycled solder joints and nano silver joints, respectively. It can be seen that both the solder and nano silver die bonding layers are intact up to 343 cycles. However, Fig. 8.26 the top image shows some tilt in the solder bonding layer. This is most likely due to the solder reflow process. The solder preform melted and the back flow from one side was much stronger than from the other side due to the uneven size of the solder preform. As such, the device was lifted unequally which lead to the tilt of the device after soldering. Another important factor for reliability is the voids inside the solder layer as shown in the bottom layer images of Fig. 8.26. Voids reduce the thermal and electrical conductivity of the solder layer and are often the site where cracks initiate, which reduces the lifetime of the power module. Compared to the solder joints, nano silver joints are more smooth and flat since a high pressure was applied uniformly on top of the device during sintering.



(a) (b)

Fig. 8.26 The SAM images of the solder joints after (a) 0 cycle (b) 343 cycles (photo by author)



(a) (b)

Fig. 8.27 SAM images of the nano silver joints after (a) 0 cycle (b) 343 cycles (photo by author)

Figs. 8.28 to 8.30 show the die bonding strength for three bonding sample sets. As can be seen, the solder (sample set 1) and nano silver joints (sample set 3) have a similar average initial die bonding strength of about 35MPa. The maximum solder bonding strength is slightly higher than 40MPa for the SAC405 sample. The die bonding strength for sample set 2, which is the nano silver joint with a low sintering pressure, has a relative lower die bonding strength. After 343 cycles, the die bonding strength for both sample set 1 and sample set 3 did not change much.

However, for sample set 2, the die bonding strength degrades faster as the number of temperature cycles increases. Its average bonding strength reduces to less than 10MPa after 343 cycles. From the result, the sintering pressure has a great influence on the die bonding strength for the nano silver die joints.

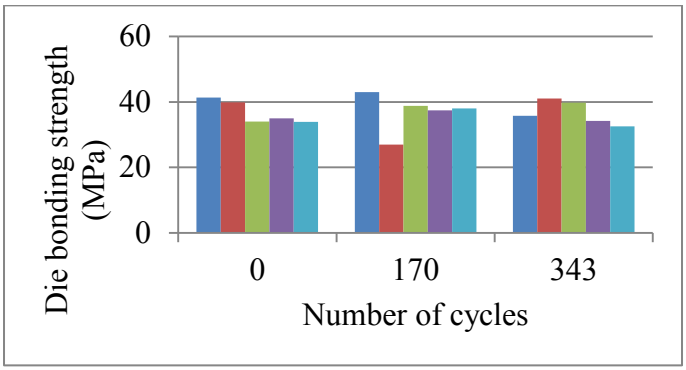


Fig. 8.28 Change of die bonding strength using solder attachment (sample set 1)

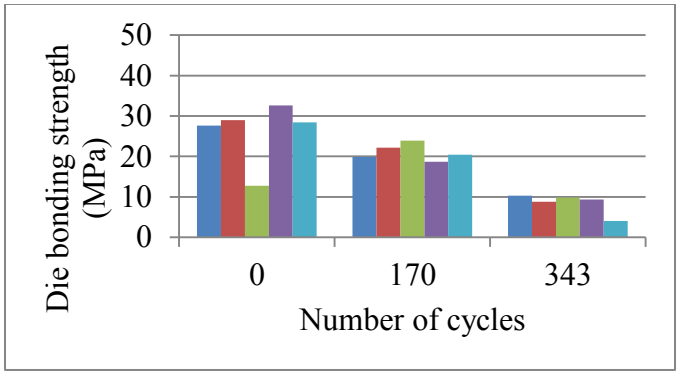


Fig. 8.29 Change of the die bonding strength using nano silver paste (sample set 2)

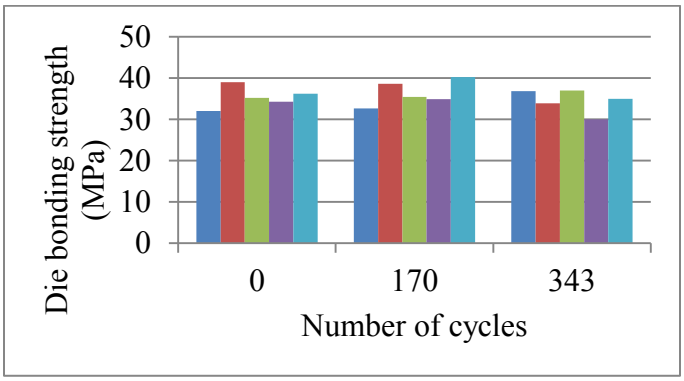


Fig. 8.30 Change of the die bonding strength using nano silver paste (sample set 3)

Fig. 8.31 shows the SEM images of the sintered nano silver and SAC405 solder joints. As can be seen, nano silver joints have a porosity structure. This porous structure is expected to reduce the Young's modules of the sintered nano silver to about 9GPa compared to that of pure silver (83GPa), which helps to improve its joint reliability. This porosity structure reduces the thermal and electrical conductivity of the sintered nano silver joint to some level. However, compared to the solder joints, sintered nano silver joints still have a higher thermal and electrical conductivity. This is because the metallic bonds of silver have a large number of free-floating electrons, which make it easy for phonon and electrons to jump from place to place [64]. From the die bonding thermal cycling experiment, nano silver joints have a similar bonding strength when compared to that of the SAC405 joints below 343 cycles.

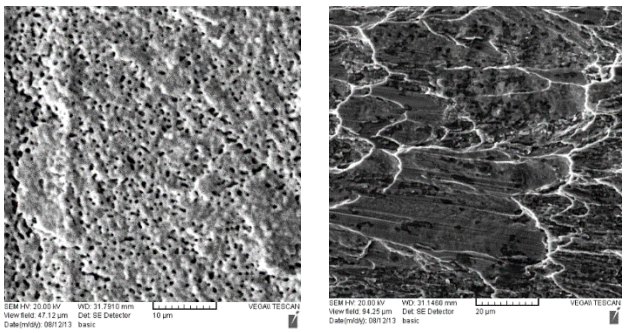


Fig. 8.31 SEM images of nano silver bonding (a) and solder bonding (b) (photo by author)

8.4.2.2 Double-sided cooling power module

Table 8.3 summarizes the temperature cycling results. In the table, a "✓" sign for the gate-source indicates that there is no gate-to-source shorting. A "✓" sign for the forward and reverse indicates that an I-V curve can be obtained, while an "x" means that the I-V curve cannot be measured, assuming that the tested module does not have a gate-to-source shorting failure. After 43 thermal cycles, module 3 did not yield both the forward and reverse I-V characteristics. The reverse characteristics of both the modules 4 and 5 could be measured. However, their forward characteristics could not be measured. Table 8.4 summarizes the possible failure modes for the

power modules. The results indicate that, the major possible failure mode for the module is the failure of the device joints. Fig. 8.32 shows the reverse I-V curve for the diode at the beginning of the temperature cycling and after 85 thermal cycles. It can be seen that the resistance of the reverse I-V characteristic increases dramatically after 85 thermal cycles for the power module. Since the SBD diode is directly attached to the bottom and top DBC substrates, the major reason for such a big increase in resistance is the increase in its contact resistance. Both the SiC MOSFET and SBD diode used in this work have Ag drain and cathode metal pads. From the thermal cycling experiment for the silver joints, the commercial devices with Ag metal pads were shown to have a good bonding joint using the nano silver die attach. However, the source and gate pads on the MOSFET and the anode of the SiC SBD diode used in this work originally have aluminum pads as they were designed for aluminum wire bonding. In order to use the nano silver die attach, a thin layer of Cr/Ni/Ag was evaporated onto these aluminum pads. It is possible that the adhesion of this metal layer onto the partially oxidized aluminum pads is one possible cause for the degradation of the joints. Another possible reason may be due to the weakening of the nano silver joints from the top DBC substrate to the source pads of the SiC MOSFET and the anode of the SBD diode by the residues left from cleaning the PAI polymer. From the thermo-mechanical simulation results, the double-sided DBC structure generates a much larger thermal stress during the temperature cycling process. It is also possible that the power devices were damaged by the thermo-stress during temperature cycling. In this module, the gate connection method was designed to obtain a good alignment with the source to avoid a gate-to-source short during the attachment of the top DBC substrate. However, it introduces several new sources of potential failure. The gate path includes a thin film metal layer of Cr/Ni/Ag, an LTCC ink and vias, as well as the nano silver joint to the gate power connector. It

is very likely that during the temperature cycling process, one or more of these interfaces were broken which might lead to the failure of gate connection. One way to mitigate the gate connection failure is to directly attach the gate to the top DBC substrate to reduce the number of interfaces in the gate connection path. Fig. 8.33 shows a modified layout for directly attaching the gate and source of the SiC MOSFET to the both the top and bottom DBC substrates. Fig. 8.34 (a) and (b) show the semi-completed power module assembly with the top side metal pads of the power devices attached using two different dielectric materials, R-2187 and FP-4526. This "bottom-up" fabrication method reduces the number of fabrication steps and should improve the thermal performance by directly attaching both the source and gate pads of the SiC MOSFET to the top DBC substrate. However, the disadvantage of this design is that a PAI or other high dielectric strength material is required before attaching the device source and gate regions. A well-designed alignment jig is necessary to avoid the gate/source shorting and electrical breakdown in the guard ring region. Another disadvantage is the large thermal stress caused by both the top and bottom DBC substrates being rigidly bonded with the SiC power devices.

Table 8.3 Power module characterization after 43 and 85 thermal cycles

Power module samples	cycles	Gate-Source	Forward (Drain to Source)	Reverse (Source to drain)
3	43 cycles	✓	x	x
4		✓	x	✓
5		✓	x	✓
3	85 cycles	✓	x	x
4		✓	x	✓
5		✓	x	✓

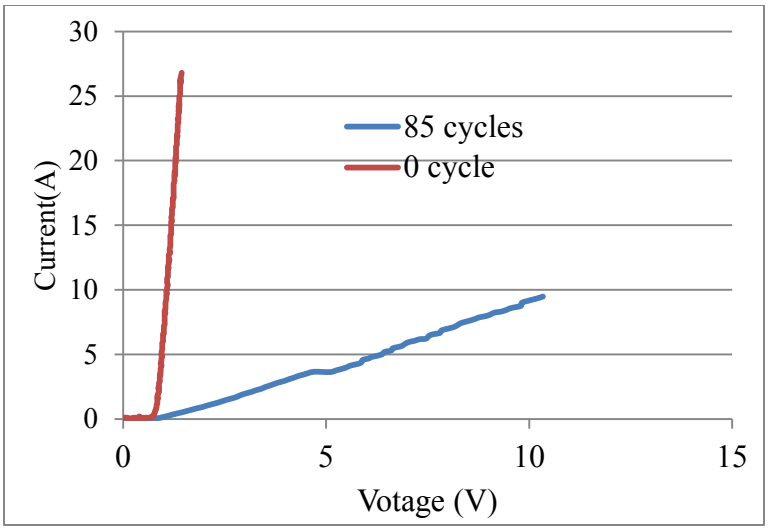
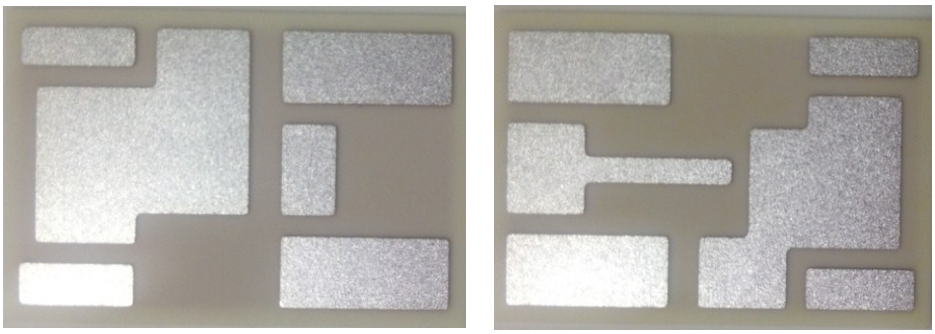


Fig. 8.32 I-V curve for the reverse diode at 0 and 85 thermal cycles

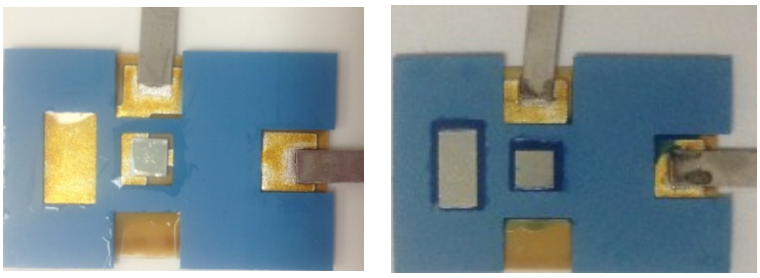
Table 8.4 Possible failure modes for the power modules

Power module possible failure models	Module 3	Module 4	Module 5
Gate contact broken	✓	✓	✓
Source disconnect	✓	✓	✓
Drain disconnect	✓	✓	✓
Big thermal stress cause crack of device	✓	x	x
Anode disconnect	✓	x	x
Cathod disconnect	✓	x	x



(a) (b)

Fig. 8.33 DBC substrate for the bottom-up design (photo by author)



(a) (b)

Fig. 8.34 Semi-completed module assembly with (a) R-2187, and (b) FP-4526 dielectric (photo by author)

8.5 Summary

This chapter investigates the reliability issue based on the thermal cycling experiments. It reveals that the quality of nano silver joints is greatly influenced by the sintering process parameters. A higher pressure applied during the sintering process yields a higher bond strength. For low numbers of thermal cycles, lead free solder has a similar bond strength compared to those of the sintered nano silver joints. However, nano sivler bonds are smoother and void free. Thermal cycling of the fabricated double-sided cooling power modules revealed some reliability issues attributed to thermal stresses of their multiple joints. This is possibly due to poor joints as the result of aluminum interconnection on these power devices. High thermal stress may also contribute to the failure of the power module. A modified bottom-up design was proposed and compared to the original design.

Chapter 9. Conclusions

9.1 Contributions of This Dissertation Research

A novel double-sided cooling power electronic module was designed, analyzed, simulated, and fabricated. The salient feature of this power module is the use of a LTCC die frame and a dielectric material between the top and bottom DBC substrates to relieve the thermal stress of the rigid conventional double-sided power modules. Finite element simulations were performed to investigate the thermal and thermo-mechanical performance of the double-sided cooling module and these results were compared to existing double-sided and single-sided power modules. Compare to the single-sided cooling module, the double-sided cooling modules induce a larger thermal stress due to the symmetrical structure of the double-sided cooling module and their different material layers are constraint to move in the horizontal direction instead of the ability to bend in the vertical direction as in a single-sided module. Simulation results show that the LTCC die frame and dielectric layer reduces the thermal stress of the SiC devices by about 25%. The module was successfully fabricated using a packaging material system for operation to 200^{o}C. A polyamide imide passivation layer on the top DBC was proven to improve the breakdown voltage of the module. The functionality of the module was demonstrated by the current-voltage and reverse blocking characteristics of the SiC MOSFET and SiC SBD configuration. This module exhibits a smaller parasitic inductance as evident from its lower switching spikes in its switching waveforms. A junction-to-ambient thermal resistance of 5.48°C/W was obtained for this module, which is about 11% smaller than that of a comparable single-sided wire-bonded module. Even though the double-sided cooling LTCC module failed the thermal cycle test at relatively low number of thermal cycles, this dissertation research has demonstrated the promises of the double-sided cooling LTCC module as a viable double-sided

cooling structure for future power electronic modules.

9.2 Recommended Future Research

From the simulation results shown in Chapter 5, the double-sided cooling module induces a larger thermo-mechanical stress compared to its single-sided counterpart. Structures for the double-sided cooling design should be improved and new packaging materials should be developed to reduce the thermal stress to improve their thermal cycling capability. A flexible substrate to realize the top side contact for the power semiconductor devices can be used to improve its reliability.

The nano silver die attach is a promising die bonding method due to its high thermal and electrical conductivity as well as a higher reliability compared to the solder attach material. However, its bond quality is highly dependent on its sintering process. It is recommended that a hot press with an accurately controlled temperature and pressure to be developed for the nano silver sintering process to improve the silver joint quality. Other bonding technique such as the transient liquid phase bonding should be investigated.

For practical application in the power electronic systems, an appropriate cooling system for the high temperature double-sided cooling module should be designed and investigated. The module to cooling system attachment material and attachment method should also be investigated.

Finally, an option for silver pad metallization scheme for SiC power semiconductor devices should be available from the commercial vendors for the nano silver attachment method.

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Appendix

A. LTCC substrate preparation process

Greentape: two sheets of Dupont 951PX (10mil thick before shrink)

Via paste: Dupont 6141

Post fired conductor: dupont 6277

1. Precondition tape: place them in the oven at 80 °C for 20 min.

2. Punch two tapes.

3. Fill the vias using the 6141 paste

4. Place them in the LTCC oven to dry the vias (at 80 °C for 5 min).

5. Laminate two tapes together:

Pressure: 3000 PSI

Temperature: 70 °C for 10 min

6. Dice the parts.

8. Place them in the oven (951 co-fire profile, the total time is about 13 hours)

Ramp to 350°C (rate 6°C/min)

Soak at 350 °C for 1hour

Ramp to 450°C (rate 3.3 °C/ min)

Ramp to 875°C (rate 5°C/min)

Soak at 875 °C for 15 min

Ramp to 500 °C (rate 6 °C/min)

Ramp to 300 °C (rate 6 °C/min)

End (shut down, cool down)

9. Print using the conductor paste 6277

10. Place them in the oven (post fire profile, the total time is about 13 hours)

Ramp to 200 °C (rate 50 °C/min)

Ramp to 600 °C (rate 20 °C/ min)

Ramp to 850 °C (rate 15 °C/min)

Soak at 850 °C for 15 min

End (shut down, cool down)

B. PVD operation process

1. Pre-check: check the water open and crystal light on

2. Power up:

- verify power on, press START, wait until Turbo start appears
- Vent: press “VENT”, disconnect rotary work holder power cable
- Remove lid cables, unscrew ground wire, check if door opens then press “SEAL”
- Remove lid and remove shield
- Identify sources and boats
- Load source

3. Set density

- Set the current layer
- Press DATA and up/down keys to change the density

4. Pump down

- Close the door and press CYCLE
- Display will read ROUGH, PUMPDOWN, FINE PUMPING
- When ROUGHING FAILURES appears, press RESET then CYCLE
- Wait until pressure drops to ~1e-5MB

5. Metal deposition

- Set LAYER
- Set termination to be desired thickness
- Press RUN to reset monitor thickness to be 0
- Push in RESET and switch to LT
- Increase current by 0.25A each 5 seconds until current reach 1 to 2 mA and stop, wait until the pressure drops to around 1e-5MB then remove the shutter

6. Shutdown

- Set CC dial to 0 and close shutter at the same time
- Switch LT to 0 and push in TRIP
- Rotate plate to the next metal

7. Remove sample

- Allow source to cool for ~10 min under vacuum
- Press VENT and disconnect rotary work holder power cable
- Unscrew ground wire and check if door opens and then press SEAL
- Tilt lid back to break seal and remove boat and rods
- Remove sample from the sample holder
- Place lid on chamber and insure power receptacle faces to the back
- Connect rotary work holder power cable and screw in ground wire
- Close door and press CYCLE
- When ROUGHING FAILURE appears, press RESET then CYCLE
- When pressure reach ~1e-4MB, press SEAL
- Press STOP and display will read TURBO STOP then STANDBY

C. Fatigue life prediction script

```
!   Manual UNIT system in Workbench:  Metric (mm, Pa)
! Assumes use of (in, MPa) units
! units of K1 is in Cycles/PSI
  k1 = ARG1
! K2 is unitless exponent
  k2 = ARG2
! K3 is in in/cycles/psi
  k3 = ARG3
! K3 is unitless exponent
  k4 = ARG4
  ufactor = ARG5
  cycles=ARG6
  cycletime = ARG7
! Converts diameter units to inches
  diameter = 1.24
!    Loop through number of cycles (4)
*do,AR98,1,cycles
!    x is from 1 to 3
    my_test_AR98=AR98
    set,,,,,cycletime*AR98
    cmsel,s,SOLDER
!    Get accumulated plastic work (nl,plwk) and volume (volu)
          etable,erase
          etable,vsetable,nl,plwk
          etable,volu,volu
!    Multiply accumulated plastic work by volume
          smult,pwtable,volu,vsetable
          ssum
          *get,s_volu%AR98%,ssum,,item,volu
          *get,s_plwk%AR98%,ssum,,item,pwtable
!         convert to PSI units
```

```
        s_wavg%AR98%=s_plwk%AR98%/s_volu%AR98%*ufactor
*enddo
my_solder_wdiff_2_1=s_wavg2-s_wavg1
my_solder_wdiff_3_2=s_wavg3-s_wavg2
my_solder_wdiff_4_3=s_wavg4-s_wavg3
my_n0_solder=k1*my_solder_wdiff_4_3**k2
dadnprop=k3*my_solder_wdiff_4_3**k4
my_nprop_solder=diameter/dadnprop
*status
```

D. Sub-modeling script

```
LSNUM=0
*if,lsnum,eq,0,then
/COPY,COARSE,RST,..\..\,COARSE,RST   ! COPY THE RESULT FILE FROM THE
COARSE MESH
/COPY,COARSE,DB,..\..\,COARSE,DB      ! COPY THE DATABASE FILE FROM THE
COARSE MESH
FINISH
/PREP7
CMSEL,S,CUT_BOUNDARY
NWRITE,CUT_NODES,DAT          ! WRITE THE NODES AT THE CUT_BOUNDARY TO
A FILE
ALLSEL,ALL
SAVE,FINE,DB                  ! SAVE THE DATABASE OF THE SUB-MODEL
FINISH
/POST1
RESUME,COARSE,DB              ! OPEN THE COARSE MESH DATABASE
FILE,COARSE,RST
*GET,1cNUM,ACTIVE,0,SET,NSET     !GET NUMBER OF LOAD STEPS
*DO,i,1,1cNUM
  set,i
  allset
  CBDOF,CUT_NODES,DAT,,CUT_BOUN%i%,CBDO        ! ACTIVATES CUT
BOUNDARY INTERPOLATION
*enddo
FINISH
*endif
lsnum=lsnum+1
/PREP7
RESUME,FINE,DB              ! RESUME THE SUBMODEL
/INPUT,CUT_BOUN,CBDO ! CUT BOUNDARY CONDITIONS TRANSFERRED TO
SUBMODEL
```