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Investigation of a GaN-Based Power Supply Topology Utilizing Solid State Transformer for Low Power Applications

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Investigation of a GaN-Based Power Supply Topology Utilizing Solid State Transformer for Low Power Applications

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by

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ABSTRACT

Gallium nitride (GaN) power devices exhibit a much lower gate capacitance for a similar on-resistance than its silicon counterparts, making it highly desirable for high-frequency operation in switching converters, which leads to their significant benefits on power density, cost, and system volume. High-density switching converters are being realized with GaN power devices due to their high switching speeds that reduce the size of energy-storage circuit components. The purpose of this dissertation research is to investigate a new isolated GaN AC/DC switching converter based on solid-state transformer configuration with a totem-pole power factor corrector (PFC) front-end, a half-bridge series-resonant converter (SRC) for power conversion, and a current-doubler rectifier (CDR) at its output. A new equivalent circuit model for the converter is constructed consisting of a loss-free resistor model for the PFC rectifier with first harmonic approximation model for the SRC and the CDR. Then, state-space analysis is performed to derive the converter transfer function in order to design the controllers to yield sufficient phase margins.

The converter offers the advantages of voltage regulation feature of the solid-state transformer, low harmonics and close-to-unity power factor of the PFC rectifier, soft-switching of the half-bridge SRC, reduced size of the high-frequency transformer, and smaller leakage inductance of the CDR which is used for low-voltage high-current applications as the CDR draws half of the load current in the transformer secondary side yielding less copper losses. A high-frequency nanocrystalline toroid transformer, based on a modified equation to determine its leakage inductance, is designed and fabricated to satisfy the performance specifications of the converter. A meticulously planned gate driving strategy together with a Kelvin-source return circuitry is used to mitigate Miller effects, minimize gate ringing, and minimize the parasitics of the pull-down and pull-up loops of the converter. A new programming method that combines

MATLAB Simulink embedded coder with code composer studio for the TMS320F28335 digital signal processor (DSP) controller is developed and demonstrated. Finally, the GaN-based AC/DC converter is experimentally verified for a 120Vac to 48Vdc/60Vdc conversion operating at 100 kHz for various loadings.

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IEEE published conference papers:

- A. M. Elrajoubi, K. George and S. S. Ang, "Design and analysis of a new GaN-based AC/DC topology for battery charging application," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 2018, pp. 2959-2964.

- A. M. Elrajoubi and S. S. Ang, "Design and evaluation of a high-current gate driver circuit for six paralleled 1.2kV 36A SiC MOSFETs," 2018 IEEE Power and Energy Conference at Illinois (PECI), Champaign, IL, USA, 2018, pp. 1-8.

- A. M. Elrajoubi, K. George and S. S. Ang, "Investigation of a new GaN AC/DC topology for battery charging application," *2018 IEEE Texas Power and Energy Conference (TPEC)*, College Station, TX, USA, 2018, pp. 1-6.

- A. Elrajoubi, S. S. Ang and A. Abushaiba, "TMS320F28335 DSP programming using MATLAB Simulink embedded coder: Techniques and advancements," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-7.

CHAPTER 1

INTRODUCTION

1.1 GaN Based Converters' Features

Gallium Nitride (GaN) technology offers higher performance converters with faster switching speed due to reduced switching losses, and so reducing heat sink requirement. Very high efficiency is achievable using GaN technology due to very low on resistance, superior fast switching ability, and zero reverse recovery losses. GaN devices can realize high current capability up to 100's Amperes. It is proven that GaN systems offer extreme benefits to switching power supply designs. Totem-pole power factor correction (TP-PFC) circuit can be improved for closed-loop control, and obtaining higher efficiency AC/DC converters topology. So, an efficient power supply converter can be developed using GaN devices for low and medium power applications. In this research, a low-power battery charging application is proposed for the investigated GaN converter topology which is designed for 120 Vac to 48Vdc/60Vdc conversion, operating at 100 kHz in the 1.3–1.5 kW range. Figure 1.1 shows the advantageous of GaN properties compared to silicon and gallium arsenide (GaAs) [1-1].

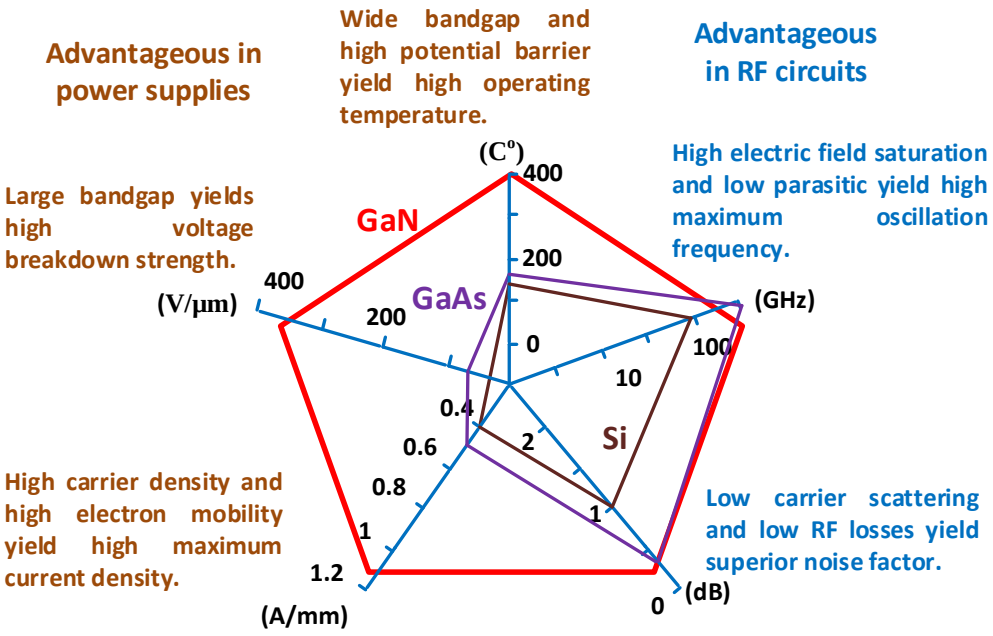

Figure 1.1. The Advantageous of GaN properties compared to Si and GaAs [1-1].

Totem-pole bridgeless PFC rectifier is now emerging using 600 V GaN devices as a preferred front end rectifier for low power applications. Since the GaN reverse recovery charge is much less than that of Si MOSFET, hard switching operation is still appropriate. GaN high-electron-mobility-transistor (HEMT) high-frequency capability and significant system advantages have been shown to dramatically reduce the volume of the boost inductor and the electromagnetic interference (EMI) filter. The switching frequency can be above 1 MHz for the totem-pole PFC rectifier, and verified solutions were addressed for significant high frequency issues [1-2]. An efficient power supply converter can be developed using GaN devices for low and medium power applications. High efficiency converters are achievable using GaN technology, superior fast switching ability, and zero reverse recovery losses. GaN device characteristics are especially suitable for hard switched diode bridgeless applications, such as PV inverters, and related totem pole PFCs applications [1-2, 1-3, 1-4]. The cascode GaN HEMT is very suitable for high-frequency operation as zero-voltage switching (ZVS) turn on has been achieved [1-5].

GaN technology is significant for several reasons:

1) GaN devices have high energy gap and so yield significantly higher electric field for GaN over Si or SiC. Therefore it allows less channel length of a GaN device which results in smaller on resistance and conduction loss [1-4].
2) Low input and output capacitances reduce switching losses in hard-switched converters and allows higher switching frequency in hard-switched and soft-switched converters.
3) Near-zero reverse recovery charge losses in hard-switched, half-bridge converters enables new topologies such as totem-pole PFC.
4) Greatly reduced switching loss reduces transition period and allows faster switching speeds while reducing or eliminating heat sink.
5) It is an ideal solution for applications requiring high frequency, high-efficiency operation in a small form factor [1-3].

6) Recently the highest current rating for 650 V GaN HEMTs has exceeds 90 A [1-4].
7) GaN HEMTs has been applied to many traditional power converters topologies, and higher efficiency with high power density was demonstrated. A 600 V, 10 kW E-Mode GaN based three phase inverter with targeted power density of 17 kW/L was built and under test [1-4].

The depletion mode (D-Mode) GaN devices are used since the cascode structure can yield positive gate-to-source threshold voltage of 2.1 V [1-4]. The switching losses and sizes of switching power supplies can be reduced by 50% through low on-resistance and high frequency capability of the GaN HEMTs. Hard switching losses occur at both turn-on and turn-off periods of the power switching devices. The total power loss (P_{LOSS}) for Si device is the sum of the following losses multiplied by the switching frequency.

$$P_{LOSS} = f\,x\,(E_{OFF} + E_{RR} + E_{OSS} + E_G + E_{ON}) \tag{1.1}$$

where, E_{OFF} = Turn-off switching energy loss.

E_{RR} = Diode recovery energy loss.

E_{OSS} = Output charge energy loss.

E_G = Gate charge energy loss.

E_{ON} = Turn-On switching energy loss.

The use of enhancement GaN HEMTs reduces switching losses and increases switching frequency to yield smaller size and improve the performance. GaN HEMTs have near-zero reverse recovery charge (Q_{RR}) due to their absence of the minority carriers. The output capacitance (C_{OSS}) and its associated charge (Q_{OSS}) is also smaller because GaN HEMTs are physically smaller than MOSFETs of comparable $R_{DS(ON)}$. Both V_{GS} and Q_G are low for GaN HEMTs, as such E_G is negligible. GaN HEMT can yield 2.5 ns rise time for a hard-switched

device. This switching speed is much faster than that of the silicon power MOSFETs. Soft-switching transitions of less than 5 ns are achievable, as parasitic capacitances and inductances are no longer ignored in the GaN HEMT based switching converters [1-3, 1-5].

1.2 Solid-State Transformer Functionalities

Solid-State Transformer (SST) is a key component with promising features. SST has reduced weight and size and can be utilized for niche applications, with additional voltage regulation and voltage disturbance rejection functionality. It allows bidirectional power flow control, and SST is very convenient for many applications since better automation and control algorithm can be developed. Also, SST will help gaining more advantages for power quality, storage management, and power flow control in addition to the reduction of volume and weight compared to the traditional transformer [1-6, 1-7]. Therefore, utilizing the advantages of SST operation and functionalities to develop a GaN-based power supply topology for low power applications will be investigated. SST demonstrated good structure as it enables superior controllability. Figure 1.2 shows the basic structure of the solid-state transformer topologies. It has been concluded that dual active bridge (DAB) converter with PWM control offers extended ZVS range and improved efficiency at light load [1-8]. Four topologies for SST were investigated in [1-9] by considering cost, number of semiconductor devices, efficiency, and specifications.

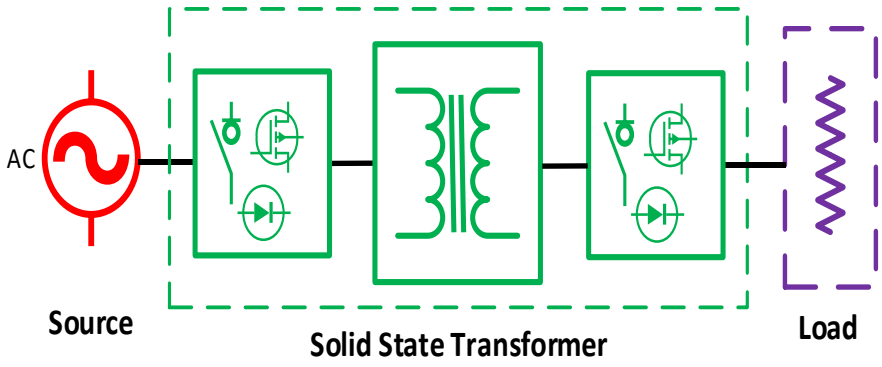

Figure 1.2. Solid State Transformer structure [1-6].

The advantages and disadvantages of the selected SST topologies (full or half bridges DAB, Boost Based topology) for emerging distribution system applications were highlighted and compared. The main advantages and promising features of SST are [1-6, 1-7, 1-8]:

- Voltage regulation and voltage disturbance rejection.
- It allows bidirectional power flow control.
- Easier for voltage and frequency adaption.
- Possible reactive power compensation.
- Reduced weight and size potentially.
- Fault current limiting.
- Overall power quality improvement.
- Power factor correction.

The proposed and designed GaN AC/DC topology in this dissertation will be operated to achieve these aforementioned SST features and functionality advantages for low power applications. The basic objective is to pursue an intelligent power electronic transformer to develop the GaN AC/DC converter which achieves SST control features.

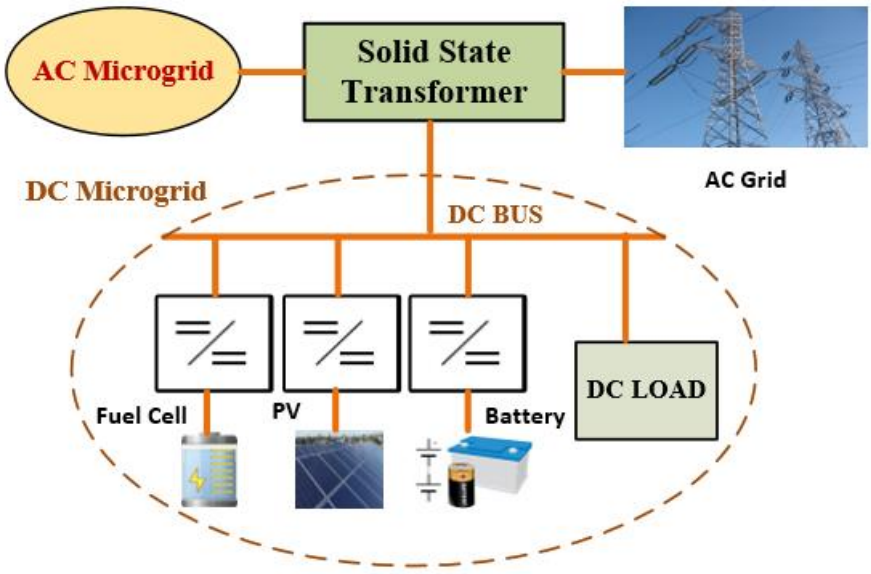

Figure 1.3. SST power management for DC microgrid [1-10].

It is stated and presented in some literatures that the core part of the SST is the isolated DC/DC converter which is operated at a medium or high frequency. Figure 1.3 demonstrates the structure of SST which was adopted in [1-10] as an interface between the distribution grid, AC loads, and DC loads. Therefore SST allows not only AC to AC conversion, but also AC to DC conversions to interact between different grids.

1.3 Dissertation Motivation

With the current advancement in wide bandgap power semiconductors, power conversion with high-frequency (HF) link has been found very convenient for many applications, and it gives an opportunity to improve power density and efficiency as well as reducing the weight, volume, and cost. GaN technology is significant as GaN HEMT devices have smaller ON resistances and thus smaller conduction losses. Also, near-zero reverse recovery charge losses in hard-switched converters makes totem-pole PFCs feasible [1-2, 1-4]. A 1 MHz bridgeless totem-pole PFC rectifier has been designed in [1-2] using the low-loss 600 V GaN device, which provides a great front-end converter for low power applications. Bridgeless totem-pole PFC has shown several advantages like higher efficiency, less parts count, and bidirectional power flow operation [1-11].

On the other hand, the current doubler rectifier (CDR) reduces RMS current on the transformer secondary (half of the load current, so less copper losses) and the output voltage ripple is reduced. Therefore it is widely used for high current, low voltage applications. Also, CDR yields smaller leakage inductance to obtain ZVS condition [1-12, 1-13], it has bi-directional energy control capability, and offers better thermal performance (good heat dissipation); also, CDR transient response performance is improved [1-14]. Reference [1-15] designed an optimized telecom phase shift full-bridge DC–DC converter with CDR for 400 V_{dc} input voltage, while the proposed topology in this dissertation utilizes the 120 V_{ac} line input and half

bridge series resonant converter (SRC), which is easier to control and yields half of the voltage to the transformer primary side. Most importantly, converter losses in series resonant converters are significantly reduced because of zero-voltage- and zero-current-switching operation of all switching devices compared to hard-switching full-bridge and half-bridge topologies, which increases the overall efficiency of this proposed topology. The combination of the reduced SRC losses with the alleviation of losses in the transformer secondary winding, due to the CDR, makes the proposed topology an attractive high-efficiency AC/DC low power converter.

The main target is to develop a power supply converter utilizing SST functionalities for few kilowatts application by using GaN switches and fully utilize their high temperature, high frequency, and low loss characteristics. It is recommended to continue the research on this particular idea in order to solve some issues related to the complex control of these topologies and to achieve the objective of high efficiency and small size with acceptable cost switching converters. The proposed converter will enhance and maintain power quality supply for low power application as well as produce a power supply topology with higher reliability and minimum cost spent in manufacturing it. The proposed GaN power converter shown in Figure 1.4 yields a close-to-unity power factor, low harmonic content (<5%), and high efficiency power supply for 120Vac to 48Vdc/60Vdc conversion, operating at 100 kHz in the 1.3–1.5 kW range.

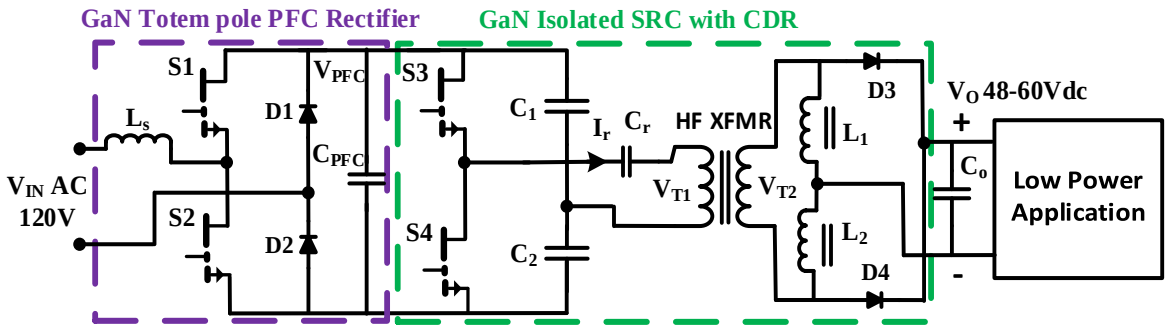

Figure 1.4. The proposed GaN AC/DC converter topology.

This converter topology includes a totem-pole power-factor-correction (TP-PFC), a half bridge series resonant converter (SRC), and a current doubler rectifier (CDR) at the secondary of the high frequency transformer. The equivalent averaged model for the proposed and investigated topology, state space equations, and transfer function are presented in this dissertation. Analysis, simulation, and experimental prototype are conducted to demonstrate the feasibility of the proposed power supply topology for low power application. MATLAB/Simulink is used for simulation and controller design and to analyze the stability of the proposed switching converter system.

1.4 Dissertation Objectives

The main objectives for this dissertation research are:

- Investigate, simulate, propose and design a new GaN-based power supply topology utilizing solid-state transformer for low power applications, particularly by combining the advantages of PFC and SRC with CDR utilizing the superior switching characteristics of GaN devices and the reduced size and cost of HF transformer.
- Analyze and synthesize the operation of the proposed GaN topology to yield higher efficiency converter due to zero-voltage- and zero-current-switching operation of all switching devices, GaN performance, and CDR advantages.
- Design the controller algorithm to achieve close to unity power factor, low harmonic contents, and high efficiency power supply for $120V_{ac}$ to $48V_{dc}/60V_{dc}$ conversion, operating at 100 kHz in the 1.3–1.5 kW range. Then implement the control algorithm with TMS320F28335 digital signal processor (DSP).
- Design, fabricate and experimentally investigate a scaled down 4-layer printed circuit board (PCB) prototype to demonstrate the feasibility of the designed GaN AC/DC converter topology and its operation.

1.5 Dissertation Organization

The literature review for the operation and topologies of solid-state transformer, resonant converters soft-switching, and GaN gate drivers design considerations will be covered in Chapter 2. Chapter 3 is about the theoretical operation concepts, modeling and simulation of the proposed GaN AC/DC topology. High-frequency transformer design is documented in Chapter 4. Then TMS320F28335 DSP programming and controller algorithm design are covered in Chapter 5. Experimental prototype results for the investigated GaN converter topology are presented in Chapter 6 with all PCB design and fabrication steps. Finally, the research conclusions and recommendations for future work are explained in Chapter 7.

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CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

The theoretical fundamentals and concepts of solid-state transformer (SST) operation and topologies are described in this chapter. The resonant converters soft switching, and gallium nitride (GaN) gate drivers design considerations are also described. It is believed that energy crisis could be avoided by improving the necessary infrastructure for renewable energy sources and storage devices. Currently, there are many researches conducted to develop various technologies for the electric distribution system using power electronics as a key technology. It is expected to experience many developments in the near future for solid-state transformer (SST) market because of its advantages. SST can operate using medium and high frequency and its physical size and weight already have been reduced significantly. Using advanced semiconductor devices in addition to the essential diodes and transistors, SSTs become very flexible. So they should be fast switching and manipulate low, medium and high power levels. Also, they can exchange different forms of electric power by changing the voltage and the frequency. Therefore, they connect the power grid to the wind turbines and solar panels using DC and AC power converters. In addition, they utilize some control equipment to communicate with utility operators and consumers. The distributed power generation and smart grid applications are very promising technologies for solid-state transformers. SST size and weight reduction can be accomplished, while the efficiency of the entire electric power system can be improved. Moreover, the characteristic of being a solid-state device is very convenient for smart grid applications as better automation and control are possible [2-1].

In the low and medium voltage power distribution network, power quality (PQ) was affected by the fundamental reasons of PQ issues and the presence of renewable energy sources. There

are many products which improved the power quality are serving the sensitive loads. Power electronics (PE) conversion technique is the main base for these important products [2-2]. Power quality solutions have been developed using power electronics systems such as uninterruptible power supply systems and active filters. These improvements are due to the significant decrease in cost, high reliability, and high-frequency switching semiconductors with low losses. Medium-voltage (MV) power distribution systems which were in the last few years dominated by electromechanical and electromagnetic technology are depending significantly on power electronics conversion techniques. Also, SST which is a high-frequency switched transformer and has extended functionality, as such, it is more economical to replace the typical power frequency distribution transformer. This PE transformer can operate on both AC MV input (single or three phase) or DC MV input. In addition it can enable balancing the loads and result in low harmonic distortions [2-2].

Power electronics transformer with high frequency is a “niche product” [2-2], and has higher functionality to serve the future power distribution systems. However, the costs and power losses are still challenges for the wide usage of SST. A medium-voltage distribution grid has been described in [2-2] which contains some DC subsystems and distributed resources, such as wind energy and fuel cell. More importantly the usage of power electronic converters to connect varies forms of electricity. More than fifteen years ago several preferred topologies of SSTs were discussed to replace the typical power frequency distribution transformer. Semiconductor switches with higher blocking capability, lower on state losses, higher switching speed and with smart integrated gate drivers are now available in the market [2-2]. However, SSTs were not popular due to unavailability of high-voltage high-frequency switching power semiconductor devices.

Electricity is generated by power generation plants, then it is transferred to the transmission lines and eventually to the distribution grids to feed the loads. In all these stages, the

transformer is an essential part to step up/down the voltage to the desired usage values. Traditional power transformer has achieved high efficiency, but its size and weight are still relatively high and could be improved. Power electronic developments are presenting a very suitable technology to serve the electric power system. High-power and high-frequency converters have been involved in the power transmission and distribution system, especially in the applications related to the utilization of renewable power energy resources. SST was introduced in 1970 and was called the electronic transformer [2-3], while the concept of solid-state transformers or electronic transformers was firstly introduced in 1950 [2-4]. It was defined as an intelligent universal transformer since it is controlled by advanced intelligent controllers and can provide different forms of DC and AC voltages. Power switching devices have been developed to be used in power electronics applications to achieve higher efficiency. The basic structure of solid-state transformer is shown in Figure 2.1. It is clear that SST is containing power electronics converters working as rectifiers and inverters, and in between these there is a high-frequency (tens to hundreds of kHz) transformer to step the voltage up/down. SST is considered as a promising component with great advantages to improve the future electric grid and be a key part especially to help connecting to the new DC microgrid architecture.

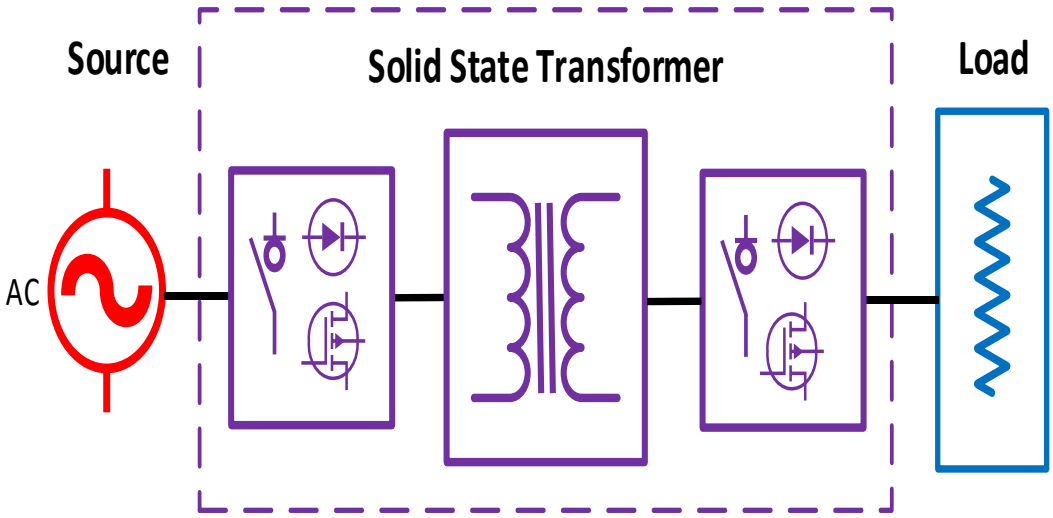

Figure 2.1. Solid State Transformer configuration [2-3].

So basically SST is a power electronic converter connected to function as a transformer which is going to replace the traditional power transformer, hence, the volume and weight are significantly decreased. Moreover, SST can provide extra benefits to the distribution network by offering useful functions such as power flow control, protection monitoring, power factor correction, and voltage sag compensation [2-3]. Future electric power distribution systems highly depend on more penetration of power electronic converters, so all efforts to understand, analyze and control the subsystems interactions are significantly valuable. Nowadays there are significant improvements because of the advancements of power electronic converters in electrical power systems. These improvements are clear and very important parts for autonomous power systems, and smart grid components [2-5].

2.2 Solid State Transformer Operation and Functionalities

Figure 2.2 shows the functional configuration of SST which is described as a power electronic converter that does much more than only voltage change (step up/down) task. SST is an important smart device for the electric distribution and delivery system to connect these different parties and transform the electric energy from one another through either AC or DC form [2-6]. It is not easy to implement this basic idea for SST, especially to obtain high efficiency and utilize additional benefits from the SST to the network. Efforts should be made to overcome the challenges for power electronic circuits to work properly in high-voltage and high-power applications. The design must be effective to ensure the reduction in size and weight since SST has extra elements like (control circuits, power devices, and heat sinks). There are many researches conducted to improve the design of SST, but still there is no standard could be followed. So it is important to review the literature and the outcomes of the previous works in order to help design SST for distribution networks considering its volume and efficiency [2-3].

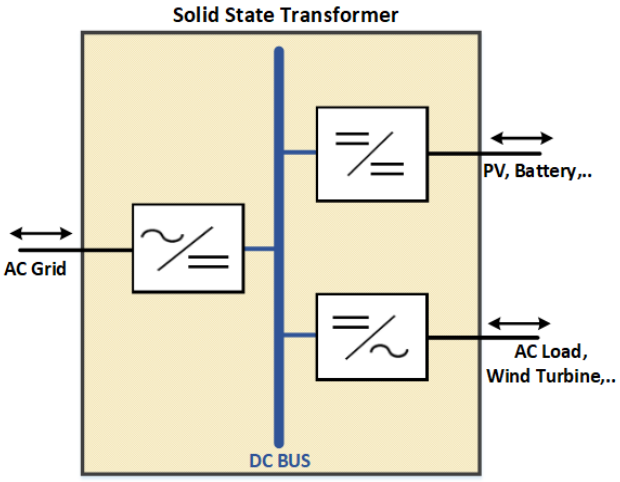

Figure 2.2. SST functional configuration [2-6].

The efficiency of the traditional transformer is already high and it is difficult for power electronic converter to achieve a 97% efficiency. However, a lower efficiency can be compromised to achieve the other functions from SST. Currently, the highest efficiency of SSTs in distribution grid is between 96% and 98%, according to the power ratings [2-3]. By reducing the size and weight of the transformer, the costs of their transportation and the required space will be much less, then both the manufacturers and the customers would gain economic benefits. Special and appropriate design considering the thermal and insulation aspects is really valuable and challenging to obtain a small size high-voltage SST.

The future renewable electric energy delivery and management (FREEDM) system using distributed renewable energy resources (DRERs) and distributed energy storage devices (DESDs) is shown and explained in [2-6]. DRERs include wind, solar, hydro, and fuel cells, while DESDs means the equipment like batteries, hydrogen storage, and hybrid electric vehicles. SST is a fundamental and important element to achieve the suitable operation of this proposed FREEDM system.

Table 2.1 compares four different SST structures: universal and flexible power management (UNIFLEX), Electric Power Research Institute (EPRI), General Electric Global Research

(GE), and FREEDM [2-3]. Si power devices and multilevel converter topologies are used in UNIFLEX, EPRI, and FREEDM in the high-voltage rectifiers for their SSTs, to achieve VAR compensation and voltage sag compensation capabilities. The highest SST efficiency is that of GE because of the customized SiC MOSFET line frequency commutation in the high-voltage rectifier [2-3].

2.3 Solid State Transformer Components and Topologies

High-voltage and high-frequency power devices are necessary for SST to be inserted into the distribution system which operate in voltages from 2.3 kV to 35 kV. Because of the switching loss limitations, silicon power devices (IGBT, IGCT, and ETO) are not able to operate at high switching frequencies. So the practical switching frequency is usually less than 1 kHz, which is not convenient for SST to obtain significant reduction in size and weight. One of the possible solutions for high-voltage is to series connect low voltage power devices. For future high-voltage applications, wide band gap materials (like 4H-silicon carbide) will be adopted. SiC material can operate at high temperature since it has a larger energy band gap.

Table 2.1. Comparison between four different SST designs [2-3].

SST Functionality	**UNIFLEX**	**EPRI**	**GE**	**FREEDM**
Eliminates oil	No	Yes	Yes	Yes
VAR compensation	Yes	Yes	No	Yes
Voltage sag compensation	Yes	Yes	No	Yes
Voltage regulation	Yes	Yes	Yes	Yes
Harmonic isolation	Yes	Yes	Yes	Yes
Common DC link	No	Yes	Yes	Yes
Energy storage option	Yes	Yes	Yes	Yes
Fault isolation	Yes	Yes	Yes	Yes
Bidirectional power flow	Yes	No	Yes	Yes
Control complexity	Complex	Average	Easy	Complex
Efficiency	Average	Average	High	Average

Also, the larger breakdown electric field enable SiC devices to switch at higher voltage, higher current, and higher frequencies. These features are suitable for SST applications. High voltage SiC devices have been investigated and it was found that 10 kV SiC MOSFETs are the best option for applications with higher than 20 kHz. However, IGBTs can operate for higher current than MOSFET at lower frequencies. For compact SST SiC MOSFETs are preferred for voltages less than 10 kV, rather than SiC IGBT, SiC GTO, and SiC ETO because of their switching speed [2-3].

SST replaces the 50/60 Hz transformer with a high-frequency transformer as the main circuit component in SST. There are several challenges needed to be investigated carefully to obtain the desired requirements for SST operation. First, to achieve high saturation flux density and less losses in the transformer, the magnetic material should be critically selected. Secondly, the efficiency at high frequencies is affected by the transformer winding method, so it should be studied sufficiently. Also, high-voltage and high-power applications must consider the thermal breakdown issue when designing the SST. Finally, for small SST size and when oil is eliminated the insulation requirement for SST is very difficult for high voltage applications. Many magnetic materials may be considered like: ferrite, nanocrystalline, silicon steel, and amorphous. Optimization must be done to evaluate these magnetic materials by considering cost, permeability, losses, and saturation flux density. In general nanocrystalline core is the best option to satisfy the efficiency and power density requirement as well. Recent studies mentioned that the efficiency can be improved up to 99.99% for different core types. Solenoidal and coaxial windings are the two main structures of transformers. Solenoidal structure is more popular and preferred because of its advantages in more flexible design, lower cost, and easier manufacture. In SST it is much more difficult to design the thermal and insulation aspects since it is desired to have less space and oil-free operation [2-3].

Figure 2.3 shows four different configurations for SST. Type A is a one stage converter that contains the high-frequency isolation transformer. Type B and Type C are both two-stage conversion topologies but they contain different DC voltage levels. Type D has a rectifier to produce HVDC, then there is a high-frequency isolation transformer to give LVDC, and finally, the inverter to provide the LVAC output. Type D is the most used topology for SST field application [2-3]. The future distribution grid requires an intelligent controller to provide the electric energy to the loads and fulfill the stability requirement. SST can present an essential element since it uses power electronic converters to integrate all those renewable sources with storage devices. The idea of energy router is mentioned in [2-6] and it is mainly built on SST and how it enables the plug-and-play of renewable resources, distributed storages, and loads. A 15 kV SiC MOSFET single phase SST circuit topology in which there are three voltage levels (7.2 kV AC, 120/240 V AC, and 400 V DC) is depicted in [2-6]. Figure 2.4 shows the three stages SST structure. This contains PWM rectifier, dual active bridge (DAB) DC/DC converter, and PWM inverter. As can be noticed the isolation in DAB is through a high-frequency transformer.

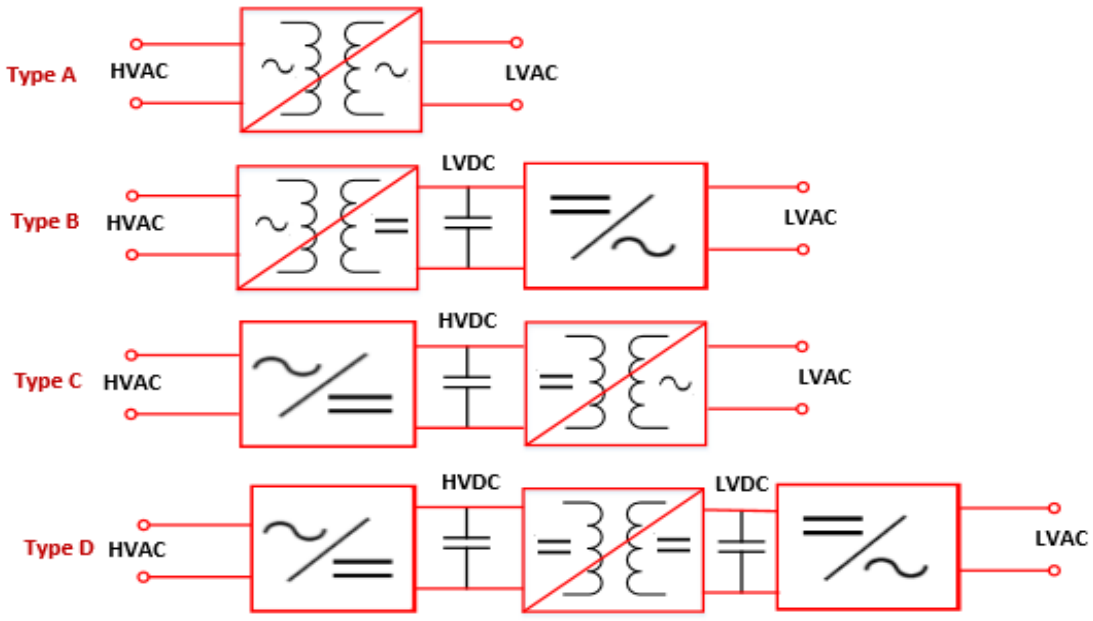

Figure 2.3. Topology classification of SST [2-3].

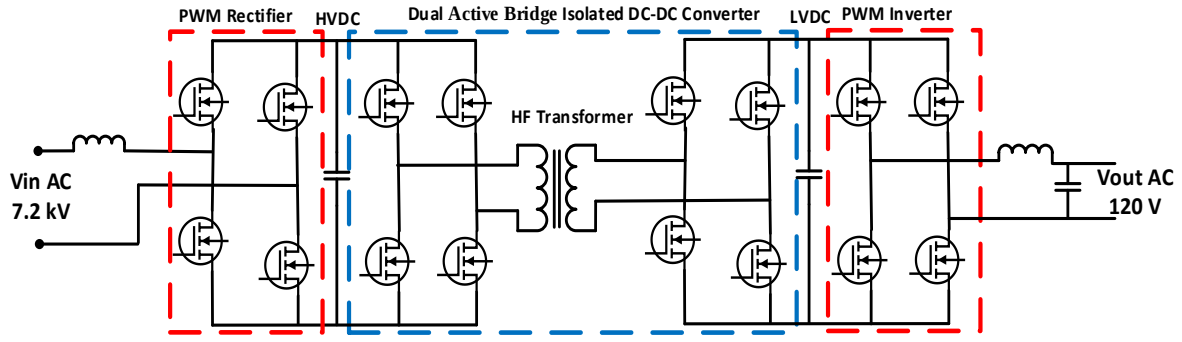

Figure 2.4. Three stages SST configuration [2-7].

This topology is providing HVDC, LVDC, and transforming from 7.2 kV AC to 120/240 V AC. This feature has enabled the SST superior controllability. It has been concluded in [2-7] that DAB converter with PWM control has extended ZVS range to improve its efficiency at very light load [2-7]. Figure 2.5 shows the basic topology of a single-phase SST which presents the values of the voltages at all stages, while figure 2.6 presents its average model [2-8].

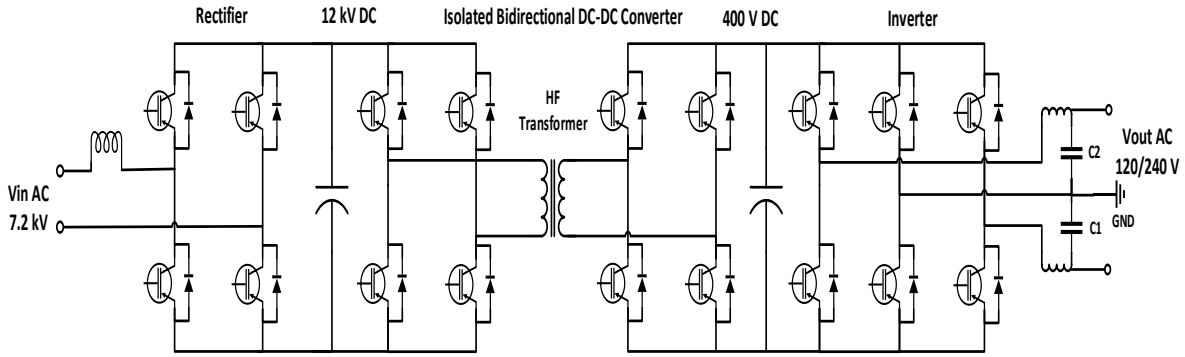

Figure 2.5. Gen-I SST single phase topology [2-8].

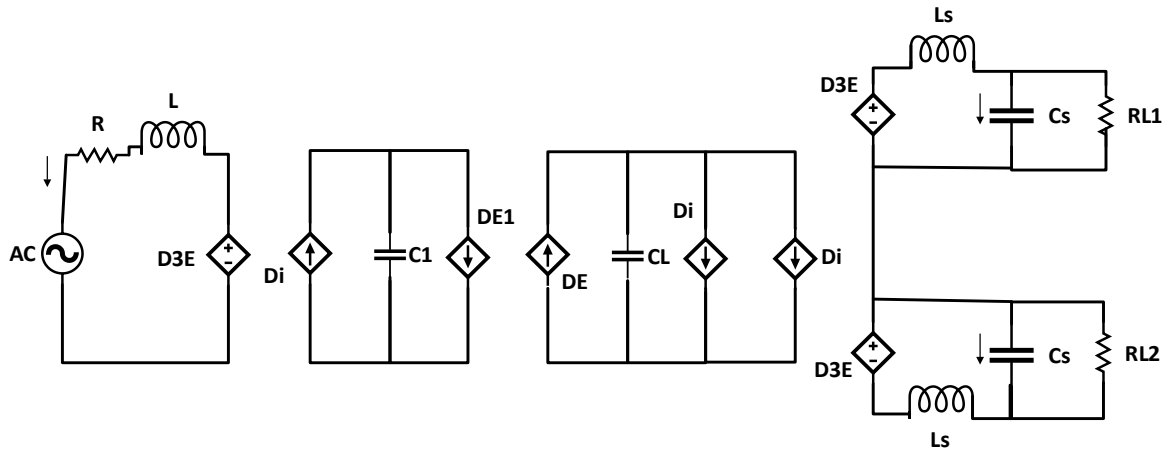

Figure 2.6. Single phase Gen-I SST average model [2-8].

2.4 Solid State Transformer Applications and Emerging Research Directions

Figure 2.7 shows the desired future distribution network by adopting SSTs instead of the 60 Hz transformer and the necessary converters for renewable energy resources and traction system. Obviously, SST can operate as an isolated AC/DC topology with power electronics converters operating at high frequency. Figure 2.8 presents the concept of using SST for reactive power compensation and harmonics filtering [2-5]. The SST plays a significant role for traction systems and it can effectively replace the low-frequency transformer and some power electronics converters since it is able to regulate the voltage as presented in [2-10].

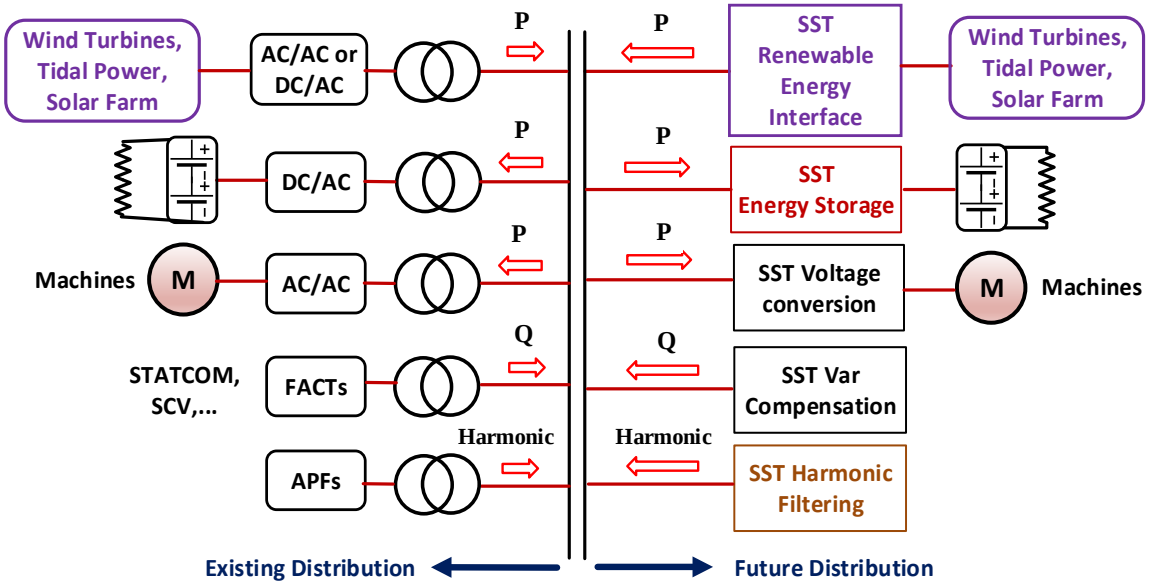

Figure 2.7. Future distribution network utilizing SSTs [2-3, 2-9].

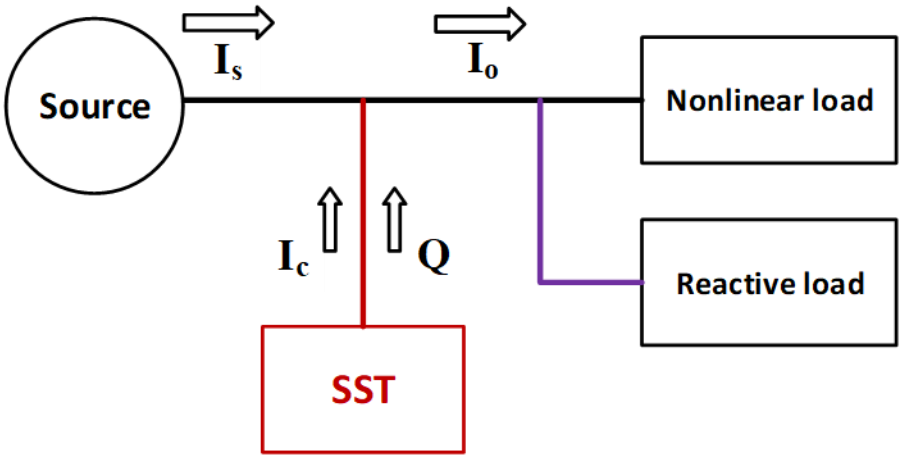

Figure 2.8. SST compensates reactive power and filters harmonics [2-9].

It is recommended to continue the research in order to solve some issues related to the complex control of SST topologies and to achieve the objectives of high-efficiency and small size with acceptable cost. For future work, the stability issues need more investigations, and it is recommended to gain more experience in future distribution systems utilizing SST. Power electronics technology is entering the electric power grid especially for the penetration of renewable energy resources. In addition SST is promising to function like an energy router to integrate smart grid applications [2-3].

The microgrid concept has been studied recently, and by adopting power electronic technology it can be proposed to replace the bulky and uncontrollable networks and solve some power quality issues [2-10]. As can be seen from Figure 2.7 and explained in [2-9], the SST can interface both the DC and AC grids in the distribution network. An interleaved configuration topology has been suggested in [2-4] for high-voltage applications to reduce the number of SiC MOSFETS and their switching losses.

The TMS312F28335 digital signal processor (DSP) is used for the experimental prototype. Experimental and simulation results showed the feasibility of proper SST operation for the proposed system [2-4]. Figure 2.9 shows the diagram to adopt SST in a DC Microgrid [2-11]. This proposed system concerns the DC load and DC renewable energy sources (PV, fuel cell, and battery) with the advantages of SST to operate the system. It is confirmed that SST has many useful features and it can work bi-directionally. When the microgrid provides more power than the loads' demand, the extra power will be re-distributed to the utility grid, and vice versa. The battery can take in or give the energy according to its state of charge (SOC) while the PV and fuel cell are only alternative sources [2-11]. SST can be utilized as a smart plug-and-play interface to exchange the electricity among different subsystems, so it is the key enabling technology for the distribution system and smart grid.

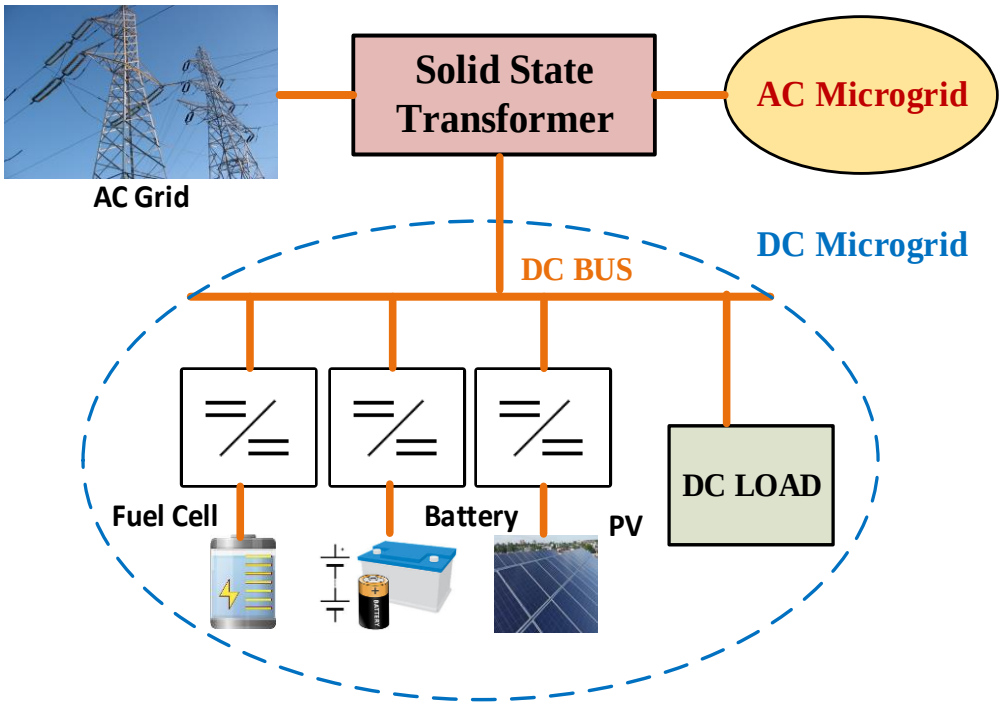

Figure 2.9. SST for DC Microgrid [2-10].

FREEDM system diagram has been described in [2-6, 2-9, 2-12] and it shows the fundamental concept for using SST to provide 120V AC and 400V DC from the 12 kV AC bus. Intelligent energy management (IEM) is performing energy flow control using SST and distributed grid intelligence (DGI) unit. So IEM will fulfill the bidirectional power flow and distributed power management. The local loads are supplied initially from DRER and DESD, and if the demand is more than the supply then SST will draw the needed electricity from the grid. Also, when the loads are less than the supply SST will send the extra power to the grid [2-12]. SST technology needs an efficient high-voltage and high-frequency transformer. FREEDM research center has compared and reviewed the theoretical concepts for the magnetic core materials, and winding layout options. They reported the test results for the 6.7 kVA high voltage high-frequency transformer prototype [2-8]. SST is established and implemented in [2-13] for the smart grid to improve the system performance and integrate the alternative energy sources and storage devices. So eventually mitigate the energy crisis by developing an efficient electric network infrastructure for controlling the entire system.

2.5 Resonant Conversion Concepts and Soft Switching Operation

Zero-voltage-switching and zero-current-switching topologies are designed to gain higher efficiency power conversion by minimizing switching losses for the switches. That is typically obtained by utilizing the resonant operating condition for the switching frequency. Resonant converters are different from typical PWM converters as they include resonant L-C networks and their voltage and current sinusoidal waveforms are depending on each subinterval switching period conditions. By changing the switching frequency, the magnitudes of the resonant tank current and voltage can be controlled as desired for the topology under consideration [2-14]. The resonant switch concepts are not discussed in this chapter, which are thoroughly explained in the literature for several resonant converters. In these resonant switch topologies the PWM converter has switch network contains resonant elements, therefore they result in a resonant switch network with the properties of the original PWM converter. Common quasi-square wave methods for soft switching converters achieves zero voltage switching without having high voltage stress on the transistor [2-14].

The main feature of the resonant converters is minimizing the switching loss by the mechanism of turning on and off transitions at the zero crossing of the waveforms. This phenomena has been widely implemented in switching converters to let the transistors switching transitions coincide the zero crossing of the voltage and current waveforms. Typically for a full-bridge topology, zero-voltage-switching (ZVS) occur when it operates below resonance, while zero-current-switching (ZCS) occur at above resonance operation. These are because the circuit causes the transistor current become zero before it turns off, likewise it causes the voltage across the transistor to be zero before the turn-on transition is done. In addition, diodes reverse-recovery charge losses are mitigated by ZVS, whereas ZCS is applied to eliminate current tailing and stray inductances switching losses. ZVS is preferred when diode reverse-recovery losses and semiconductor output capacitors are causing major switching losses [2-14].

Considering the efficiency and losses in any switching converter is an important step during the equivalent circuit operation analysis. Many references described the sinusoidal approximation to investigate and analyze the operation of resonant converters. Sinusoidal approximation approach is very useful to have great insight for many properties of the resonant converters such as the output characteristics, load current dependence, and zero-voltage and zero-current-switching transitions. It is accurate for large Q factor and close to resonant switching frequency operation [2-14].

Zero-voltage-switching has been discussed and analyzed in [2-15] for an isolated forward converter with current doubler rectifier (CDR) on the secondary side of the high frequency transformer. CDR has been utilized for high-current low-voltage applications due to the smaller current in the transformer secondary windings, and CDR can maintain ZVS with its reduced leakage inductance [2-15]. Soft switching has been achieved for the analyzed topology by adjusting the desired leakage inductance of the CDR topology to meet the resonant frequency condition.

2.6 GaN Gate Drivers Design Considerations

Gate driver circuitry is designed to provide the required voltage and current levels to drive a transistor in a safe and an efficient way. At the same time it protects the digital signal processor (DSP) from voltage spikes or any noise as well as operates to minimize conduction and switching losses. The gate capacitance is charged as fast as possible to minimize the switching time, hence, a driver IC with sufficient current capability should be used. Also the stray inductances in drive circuits have to be eliminated or minimized to avoid the presence of unwanted oscillation during device turn-off. This is typically employed using a four terminals (Kelvin) connection to have the transistor source connected separately to the gate driver terminals. Meanwhile, the length of all unshielded terminals should be minimized to reduce the

over-voltages at turn-off transients. Therefore, the layouts of gate drivers and power electronic converter printed circuit boards are crucial to mitigate the effects of parasitic inductances and reduce switching noises to obtain satisfactory operation [2-16, 2-17].

Bootstrap capacitance effect for high speed non isolated gate driver circuitry is addressed in [2-18] for driving the top switch of a half-bridge converter, or for driving two MOSFETs in a synchronous buck converter. The voltage level of the gate pulse is shifted to switch on the upper switch by using a bootstrap bias circuit comprising of a bootstrap capacitor, diode, and resistor. The bootstrap capacitor is charging when the bottom switch is ON and it is discharging to turn the top-switch off. Bootstrap circuits use a single pulse width modulation (PWM) input signal to drive both the low-side and high-side switches through the charge storage bootstrap capacitor, resistor and diode [2-16, 2-18]. However, in this dissertation, gate driver isolation is obtained by utilizing separated power supply for each opto-coupler and gate driver IC of any of the GaN transistors. Silicon Labs half-bridge isolated gate drivers for E mode GaN FETs (SI8273) are used to drive both the top and bottom switches of the proposed AC/DC converter. The SI8273 isolated gate driver has several features such as high dv/dt immunity, low propagation delay, and high DC bus voltage level (1500 V) [2-19].

A quasi-Kelvin source connection is employed for the GaN transistors and their gate drivers' return loops to eliminate the deleterious effects of common source inductances. It is called quasi-Kelvin because the GaN HEMTs used in this research work have only three terminals. As such, a small amount of source parasitic inductance is present within the package. Also minimizing the layout parasitics for the prototype is taken into account for the 4 layer printed-circuit-board (PCB). Designing an appropriate layout is extremely critical for GaN converters to minimize the noise and avoid any false switching for the GaN transistors, which is a high priority. It has been recommended in [2-20] for driving GaN switches to minimize noise coupling, mitigate gate ringing or oscillations, and control Miller effects by optimizing the 4

layer PCB layout. Therefore, 4 layer PCB has been designed for the converter described in Chapter 6. It is essential to apply quasi-Kelvin connections for the driver return loops, and minimize the pull-down and pull-up loops by locating the components (gate resistances, capacitors, and diodes) as close as possible to minimize the parasitics. Also, isolating and preventing gate, drain, and control traces from overlapping among each others are performed [2-20]. The converter utilizes gate resistors of 10 Ω for $R_{G(ON)}$, and 1 Ω for $R_{G(OFF)}$ with low forward voltage Schottky diode as depicted in Figure 2.10. Gate-to-source spike clamping diodes are employed in the gate drivers circuitry.

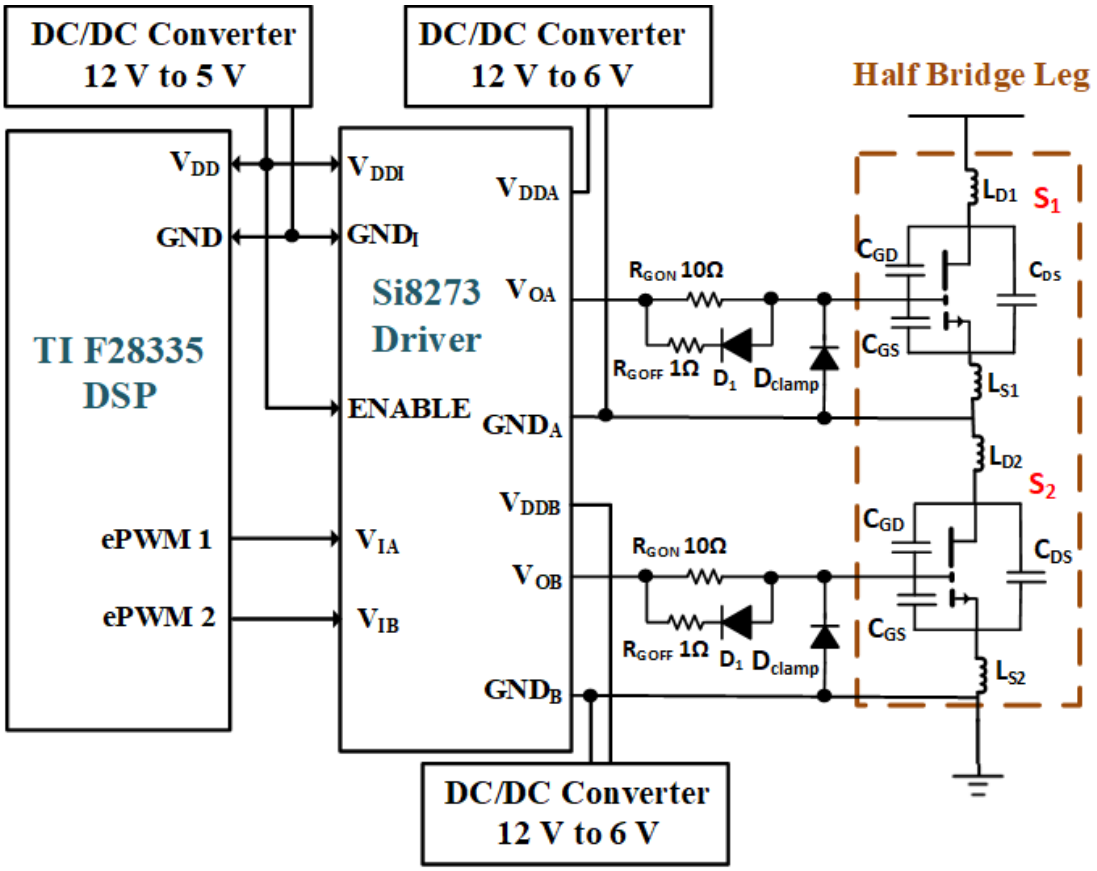

Figure 2.10. The gate driver for the GaN half-bridge structure.

2.7 Conclusion

SST is considered one of the most significant enabling technologies for future electric systems especially to the distribution system. This chapter presents an overview of SST previous researches and to provide useful information to review this technology and its main features.

Also, it presents several application topics of SST in the future smart electrical system. In addition, interfacing SST with some renewable energy sources is addressed. The literature for SST has been reviewed and summarized to provide the fundamental background and concepts. Different topologies have been applied to operate SST for different applications and different voltage levels. Several selected SST topologies have been reviewed and evaluated for the desired functionalities. SST offers extra benefits to the distribution grid by enabling significant function such as power flow control, power factor correction, voltage sag compensation, and significant reduction in volume and weight. Moreover, resonant conversion concepts and soft switching operation for solid state converters have been briefly addressed. Finally, GaN gate drivers design considerations for the proposed converter are highlighted and described.

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CHAPTER 3

SIMULATION AND MODELING OF THE PROPOSED GaN TOPOLOGY

3.1 Introduction

Solid-state transformer (SST) had been intensely investigated and reported because of its desired advantages, so SSTs are becoming more popular in many important applications. On the other hand, wide bandgap power semiconductors have several advancements recently. The opportunity to improve efficiency and power density in addition to weight, volume, and cost reduction is higher for power converters with high-frequency links [3-1][3-2]. An efficient power supply converter can be designed using GaN devices for low and medium power applications. Very high efficiency can be achieved using GaN technology due to their superior fast switching ability and zero-reverse-recovery losses. GaN technology characteristics are promising for several efficient power conversion applications, such as PV inverters, and hard switched diode bridgeless totem pole PFCs topologies [3-3][3-4]. GaN devices have smaller ON resistances which yield less conduction losses to improve converters efficiency [3-4]. Totem-pole power factor corrections (PFCs) are utilized to have near-zero reverse-recovery charge losses in half-bridge hard-switched converters. Power electronics converters with high efficiency and high power density are desired for future power supplies. So, it is beneficial to develop a new compact higher efficiency GaN AC/DC converter topology utilizing the advantages of SST for low power applications.

In this Chapter, the proposed GaN-based AC/DC power supply converter for low power applications is simulated and modeled. It has been simulated in MATLAB/Simulink in order to study its operation and control perspectives. The complete topology state-space equations, transfer function, controller design, and equivalent circuit model have been addressed and derived. An equivalent model is derived to determine the main steady-state characteristics of

the investigated AC/DC converter. The proposed converter topology is designed for 120Vac to 48Vdc/60Vdc conversion, operating at 100 kHz in the 1.3–1.5 kW range. A totem-pole power-factor-correction (TP-PFC) active front-end yields close-to-unity power factor (~0.98), and higher efficiency with reduced harmonic content. This converter combines the advantages of GaN TP-PFC and high-frequency (HF) series resonant converter (SRC) with current doubler rectifier (CDR) utilizing the superior switching characteristics of GaN devices and the reduced size and cost of HF transformer. Therefore, the proposed converter has many of the operating functionalities and features of the SST configuration reviewed in [3-5]. The SRC promotes reduced switching losses by having zero-voltage- and zero-current-switching operation for switching devices. Also, current doubler rectifier (CDR) is utilized in the secondary-side of the HF transformer for high-current, low-voltage applications due to several advantages, such as reduced copper losses as the transformer secondary winding conducts half of the load root-mean-square (RMS) current. In addition, CDR yields zero-voltage-switching (ZVS) condition due to its smaller leakage inductance [3-6][3-7]. The proposed converter topology has been investigated, simulated and modeled to achieve several attractive features for high-efficiency low power application due to GaN technology merits, reduced losses in SRC, and CDR mitigation of losses in the transformer secondary winding [3-8].

3.2 Proposed GaN AC/DC Power Supply Converter

Figure 3.1 shows the proposed 100 kHz 1.3-1.5 kW 120V/60 V GaN based AC/DC converter structure. As shown, it comprises a TP-PFC, a half-bridge series resonant converter (SRC), and a current doubler rectifier (CDR) at the secondary of the high-frequency transformer. This topology is converting 120V AC supply to a 48Vdc/60Vdc output for low power applications. The secondary side CDR consists of two diodes instead of transistors as this is easier and has been previously developed in some literature.

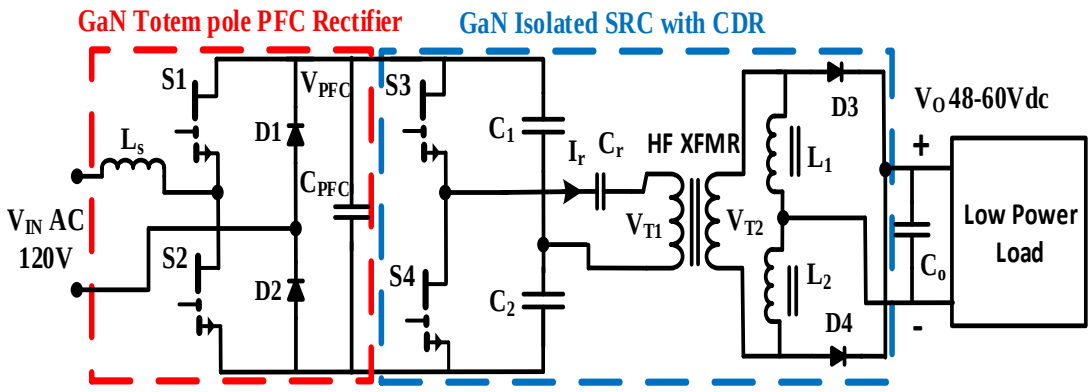


Figure 3.1. The proposed GaN AC/DC converter topology.

The CDR is widely used for high-current low-voltage applications since it has half of the load current, as such, the transformer copper losses are reduced, while the output voltage ripple is reduced. Also the CDR has a smaller leakage inductance to obtain ZVS condition [3-6]. The CDR topology can achieve ZVS for a wide load range to improve its efficiency. It has a bi-directional energy control capability when transistors are used instead of the diodes (D_3 and D_4), and CDR obtains good heat dissipation [3-9]. However, for the converter in this dissertation, CDR has two diodes (D_3 and D_4) which is easier for reducing the gate driver's circuitry. Figure 3.2 shows the main theoretical waveforms of the proposed converter topology. The top switches (S_1 and S_3) are turned on simultaneously, and likewise for the two bottom switches (S_2 and S_4). This sequence yields less voltage spikes at the PFC DC link and for the output voltage as the top switches (S_1 and S_3) provide a path for the current to flow from the boost inductor to the resonant capacitor. Both PFC and SRC switches are turned on alternatively to avoid the shoot-through for the two half-bridges. The CDR inductors current depends on the load current being supplied. The duty cycles of the switches S_1, S_2, S_3, and S_4 change the transformer primary current waveform and peak value as well as regulate the output voltage of the converter. The transformer primary-side current is shown and the CDR inductors currents are also depicted in Figure 3.2. The CDR inductor current flows through only one diode (D_3 or D_4) at each half-cycle interval.

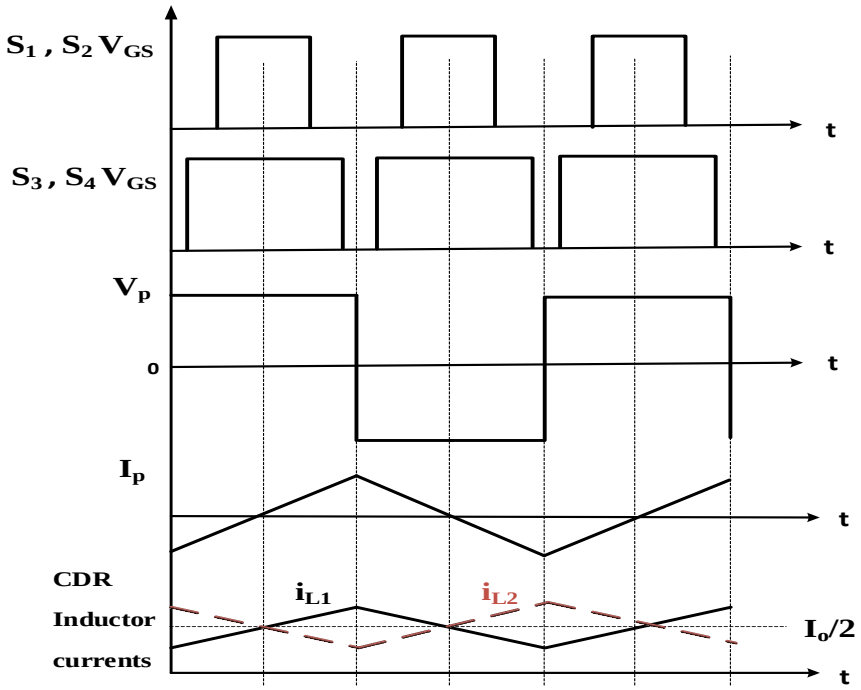


Figure 3.2. Key theoretical waveforms of the proposed converter.

As can be noticed L_1 and L_2 currents are identical with 180° phase shift, so they cause partial current ripple cancellation of the CDR output current.

3.3 Converter Design Calculations

It is essential to calculate the converter voltages and currents when designing any power supply converter to have reasonable safety margin for the component ratings. In addition, considering the efficiency and losses in the switching converter is a significant step for the equivalent circuit analysis. Using GaN high-electron-mobility-transistor (HEMT) devices in the PFC front end without a traditional full-bridge rectifier reduces losses in the proposed converter especially for high switching frequency. Moreover, conduction losses in the transformer secondary winding are reduced by using a current-doubler rectifier [3-8]. Simulation of the circuit topology shown in Figure 3.1 was performed after determining the main component values as shown in Table 3.1. The secondary-side of the high-frequency transformer is connected to the current doubler rectifier to step-down the voltage and obtain a higher output current. The main components

values were calculated for the designed converter as below. The PFC inductor value is given by:

$$L_s = \frac{\sqrt{2}\, V_{in-rms}\, D}{f_{sw}\, i_{ripple}} \tag{3.1}$$

where,

$$D = 1 - \frac{\sqrt{2}\, V_{in-rms}}{V_{o\_pfc}} \;,\; V_{o\_pfc} = \frac{\sqrt{2}\, V_{in-rms}}{Modulation\ index\ (M)} \;,\; i_{ripple} = 10\%\, \sqrt{2}\, \frac{P_{load}/\eta}{V_{in-rms}}.$$

So, D = 1 – M.

where, M is the power-factor-correction (PFC) modulation index, C_1 and C_2 are equal large capacitors for the half-bridge inverter. The DC blocking capacitor (C_b) is estimated as:

$$C_b = \frac{I_p\, T_{on\,max}}{\Delta V} \tag{3.2}$$

where, I_p is the maximum primary current (resonant current I_r), $T_{on\,max}$ is the maximum ON time of either Q_3 or Q_4, ΔV is the primary voltage permissible droop due to C_b.

However, in the designed topology, the DC blocking capacitor is considered as the SRC resonant capacitor which is calculated from the fundamental resonant equation:

$$C_r = \frac{1}{L_r(2\pi f_{sw})^2} \tag{3.3}$$

The CDR inductors values are given as [3-10]:

$$L_1 = L_2 = \frac{(V_s - V_{out})D}{f_{sw}\, \Delta i_L} \tag{3.4}$$

The output capacitor can be estimated as:

$$C_o = \frac{\Delta i_L}{2\pi f_{sw} \Delta V_{out}} \tag{3.5}$$

But the calculated output capacitor C_o value is much smaller than the simulated value as the equation is very simplified and does not consider the harmonics of the 100 kHz AC voltage rectified by the CDR. So to obtain the desired output voltage waveform, the output capacitor used in the experimental prototype C_o is 6600 µF as shown in Table 3.1.

3.4 Proposed Converter Topology Simulation

Figure 3.3 presents the output current and voltage for the open loop operation, while the main simulation waveforms of the converter topology operating at 64 kHz are shown in Figure 3.4. As can be seen, the transformer primary current (I_r) is a sinusoid indicating the SRC is in resonance. To achieve a close-to-unity power factor, low harmonic contents, and high efficiency across the full operating range of the converter, a controller is applied. Two independent proportional-integral (PI) controllers are designed for the PFC and SRC stages to operate with voltage feedback.

Table 3.1. Converter component values.

Component	Value	Component	Value
L_s	270 µH	L_1 , L_2	10 µH
C_{PFC}	470 µF	C_o	6600 µF
C_1, C_2	6.8 µF	HF-XFMR Ratio	10:9
C_r	0.1 µF		

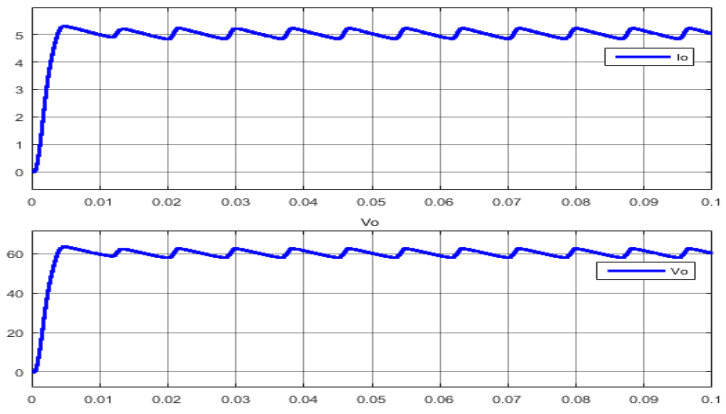


Figure 3.3. The converter output current and voltage.

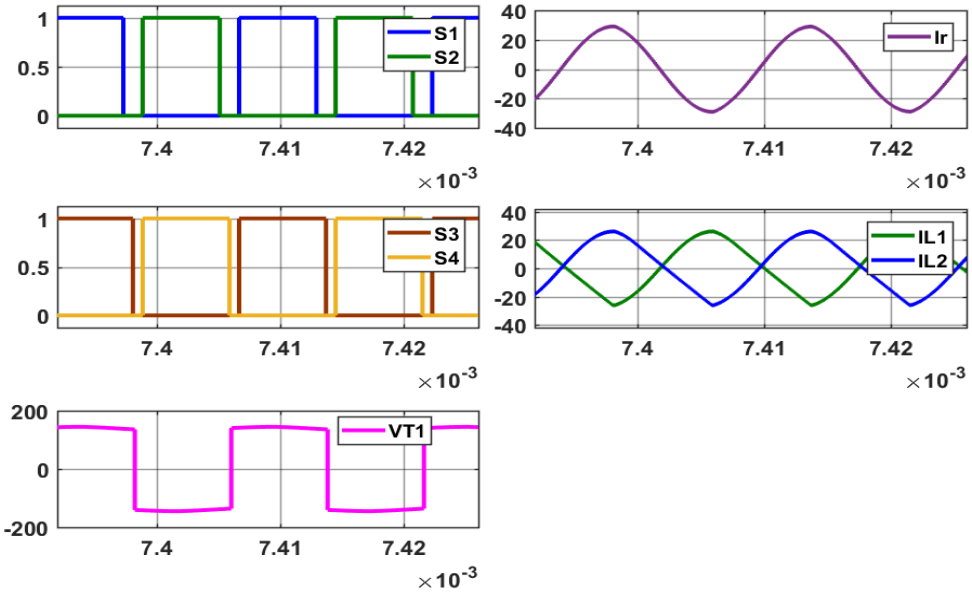


Figure 3.4. Main simulation waveforms of the proposed converter at 64 kHz.

Figure 3.5 shows the PFC voltage and input current waveforms for the open loop simulation. This input current has a large spike at the beginning because of not using an input filter for the simulations. Without a controller, the PFC circuit draws a harmonics distorted current. The output voltage from the PFC can be controlled by changing the duty cycle for Q_1 and Q_2. The gate driver signals shown in Figure 3.4 for the simulation waveforms are designed to have the top switches of the PFC and SRC half-bridges (Q_1 and Q_3) synchronized by turning on together, and the bottom switches of the PFC and SRC half-bridges (Q_2 and Q_4) also synchronized.

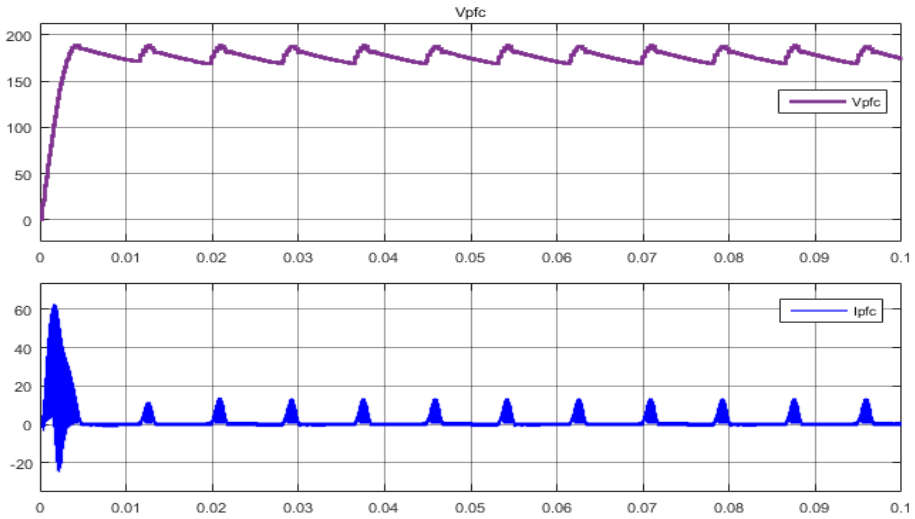


Figure 3.5. PFC voltage and input current open-loop simulation waveforms.

This switching sequence is better to yield more regulated DC voltage at the PFC output link, because the capacitor C_{PFC} is not totally decoupling the PFC stage from the SRC stage. Synchronizing the gate pulses for the switches Q_1 and Q_3 provides the conducting path from the positive input line to the series resonant capacitor to discharge the boost inductor stored energy at that particular mode when both top switches Q_1 and Q_3 are on. However, the switching sequence can be adjusted to have Q_1 turned on with Q_4 which will be the same if C_{PFC} is larger to regulate the DC voltage link. As the PFC stage is a rectifier to feed the half-bridge inverter stage switching the transistors in either sequence produce no difference for the transformer primary voltage and the converter output.

Figure 3.6 presents the main simulation waveforms of the proposed converter for different duty cycles of the switches Q_1, Q_2, Q_3, and Q_4 while Figure 3.7 presents the regulated output voltage for the open loop operation using large output capacitors to smooth the output voltage.

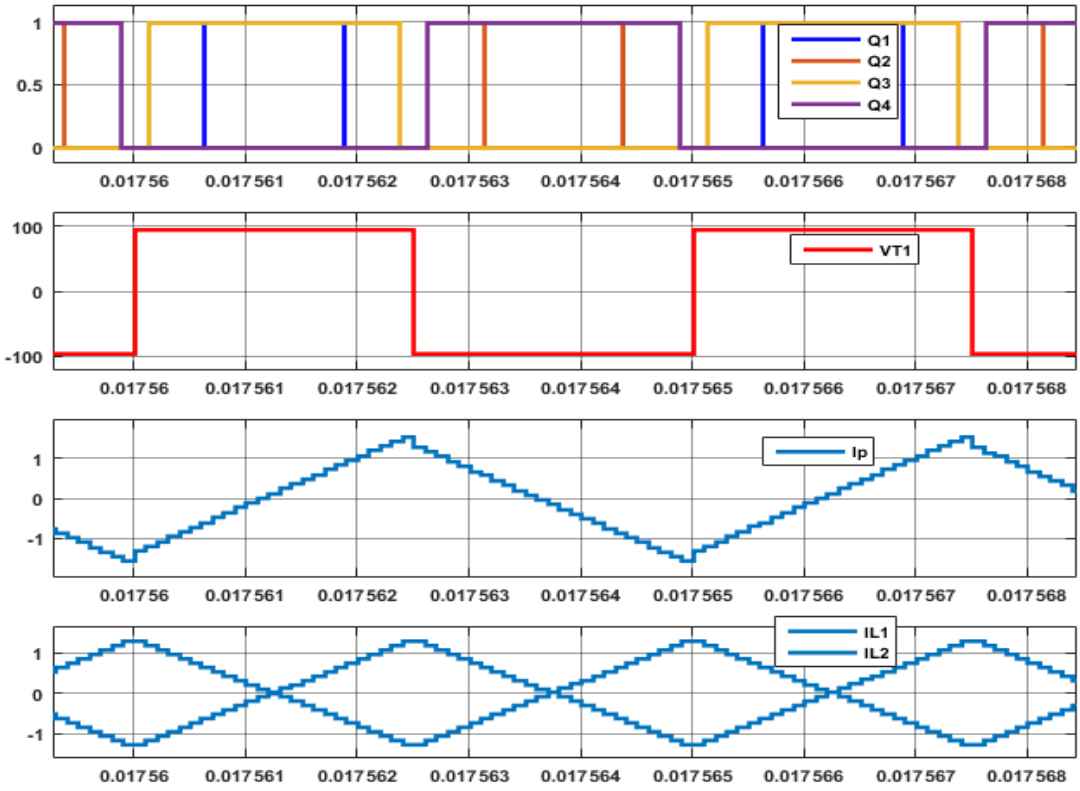


Figure 3.6. Key simulation waveforms of the proposed converter at f_s= 200 kHz.

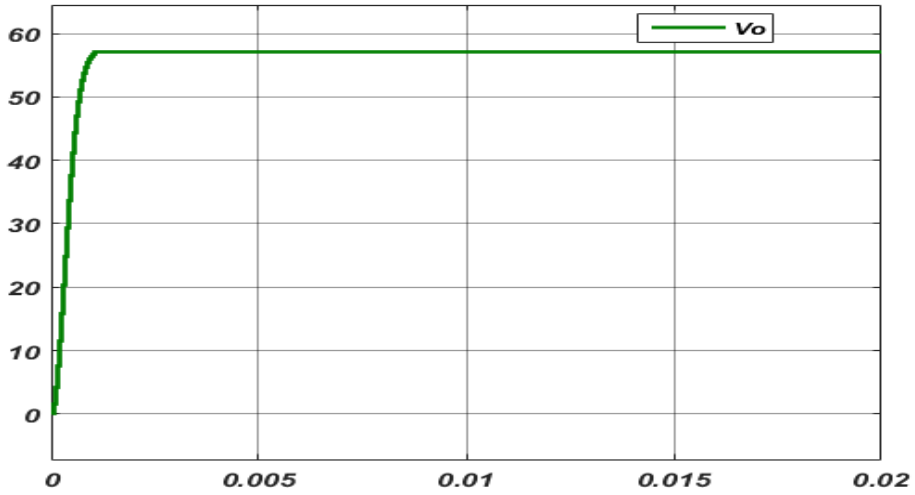


Figure 3.7. The converter regulated output voltage (V_o = 57 V).

Next Figure 3.8 is the switching pulses, transformer primary voltage and current, and diode currents for the mode when D_1 is ON while D_2 is OFF for different Q_1 and Q_2 switching conditions.

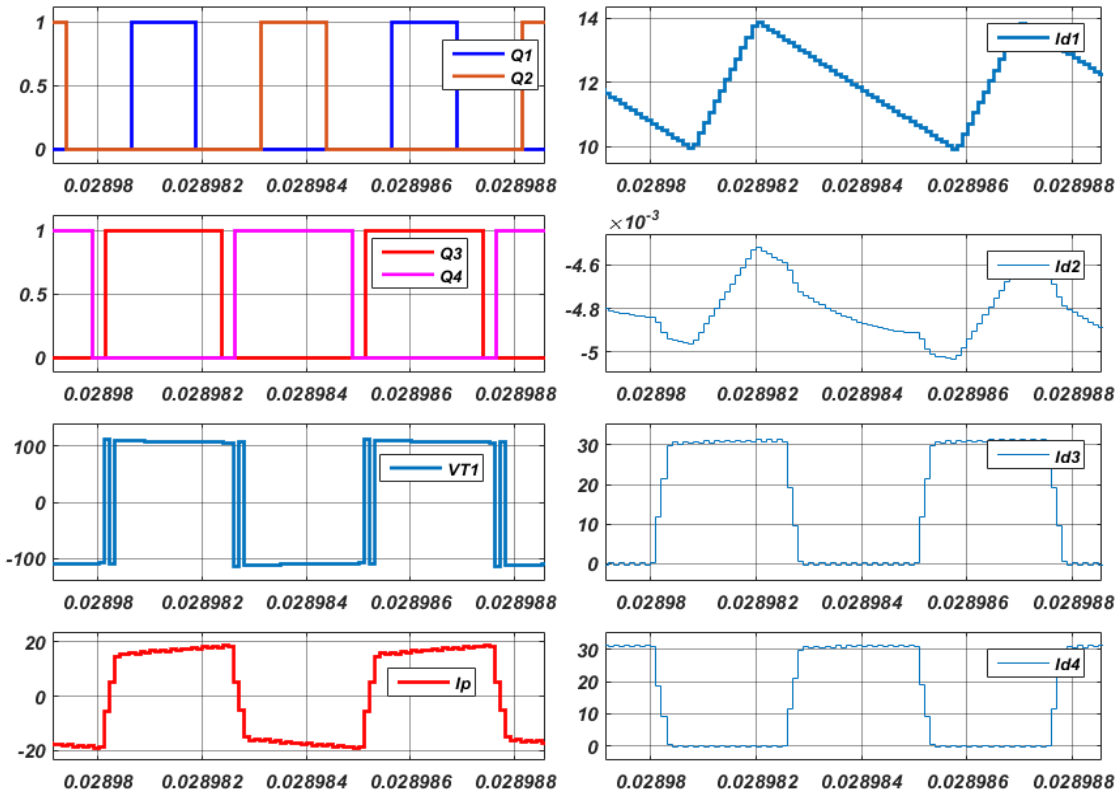


Figure 3.8. Switches' pulses, V_{T1}, I_p, and diodes' currents when D_1 is ON and D_2 is OFF.

As can be noticed, the PFC top-side diode (D_1) is conducting a positive average current of 12 A for the converter load, while the PFC low-side diode (D_2) has very small leaking negative current. CDR diodes (D_3 and D_4) are conducting the 30 A DC current to the load each for half-cycle of the time period. Figure 3.9 shows the switching pulses, transformer primary voltage and current, and diode currents for the mode when D_2 is on while D_1 is off for both different Q_1 and Q_2 status. As can be seen, the PFC top-side diode (D_1) has very small leaking negative current, while the PFC low-side diode (D_2) is conducting a positive average current of 11.2 A for the converter load. CDR diodes (D_3 and D_4) are alternatively conducting the 30 A DC current to the load.

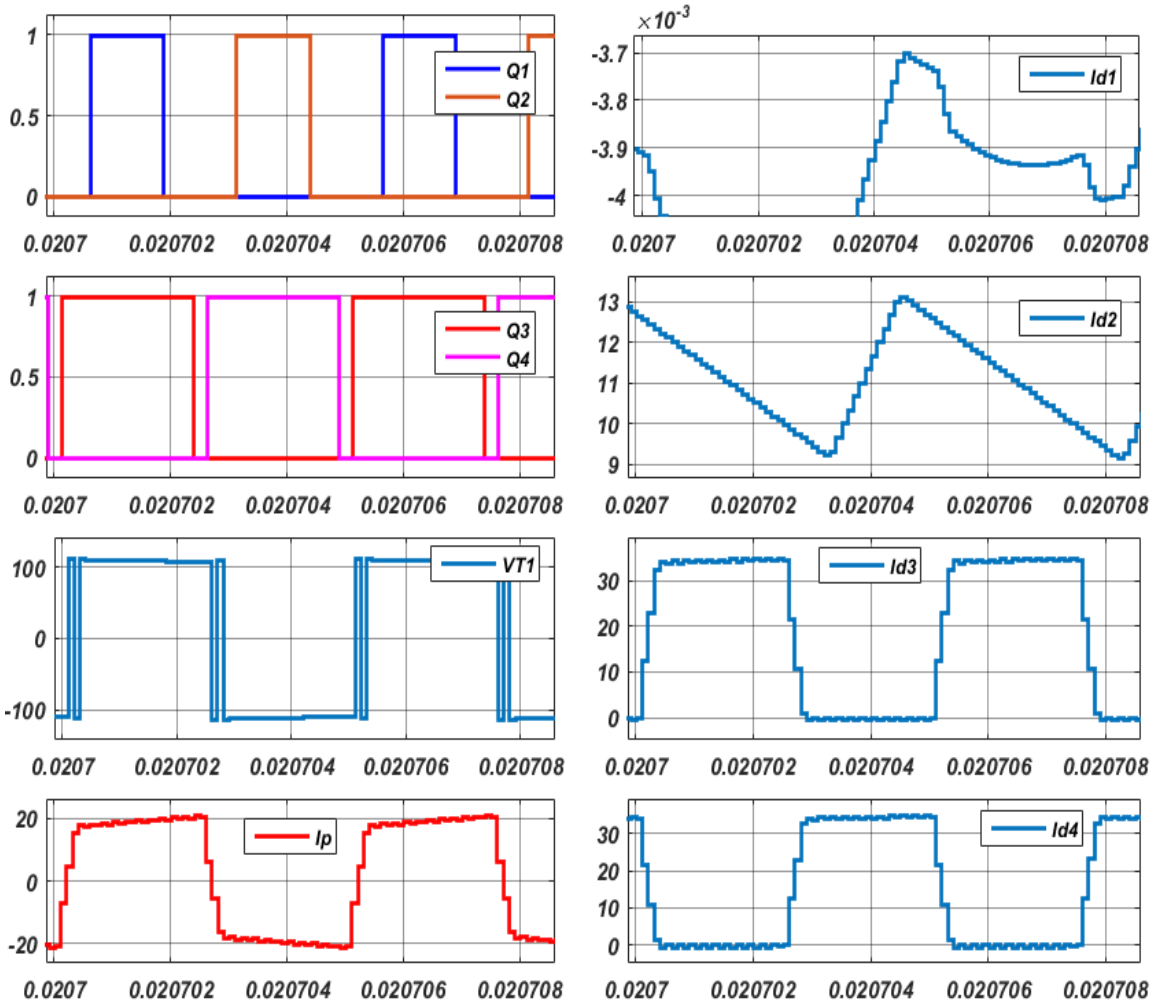


Figure 3.9. Switches' pulses, V_{T1}, I_p, and diodes' currents when D_2 is ON and D_1 is OFF.

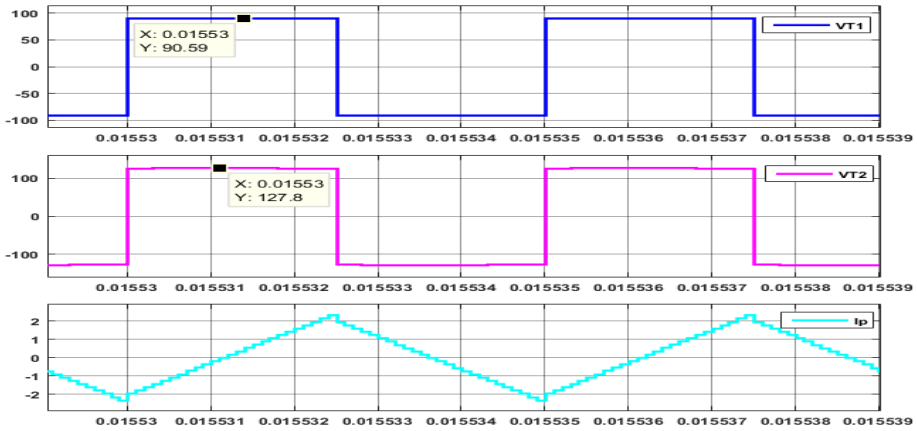


Figure 3.10. V_{T1}, V_{T2}, and I_p of the proposed converter for 200 kHz, 300 W load.

For the proposed isolated GaN AC/DC converter, a 100 kHz HF transformer is designed using the programmed methodology (reviewed in Chapter 4) to determine the transformer optimum specifications. Leakage inductance evaluation is a critical step which is affected by the transformer winding and core arrangements, and eventually presents the SRC resonance inductance in the topology [3-8]. Figure 3.10 presents the simulation results of the high-frequency transformer primary and secondary voltages, and primary current (V_{T1}, V_{T2}, and I_p) for a 200 kHz switching frequency, a PFC with D = 0.25, a 90 V to 127 V transformer ratio, and a 300 W load for a scaled down prototype converter to yield a 60V output voltage. Simulation waveforms shown in Figure 3.10 are performed with the assumption that the HF transformer has a zero primary and secondary inductance and zero leakage inductance. However, the transformer ratio for the experimental prototype is designed to be 130 : 117 (10 : 9), to either step up or down the voltage to yield output voltage of 60 or 48 V, respectively. This is to enable its low-power niche applications in telecom loads or battery charging application.

3.5 Closed-loop Simulation and Controller Design

This section shows simulation and modeling of the proposed converter with the designed controllers. To avoid instability issues and develop an appropriate feedback controller;

converter operation analysis is conducted, and equivalent model for the designed converter is investigated. Figures 3.11 shows the proposed GaN isolated AC/DC converter topology with a proportional integral (PI) controllers' feedback. The first PI controller is for the PFC rectifier switches (Q_1 and Q_2) to adjust their gate driver duty ratios, while the second PI controller is for the SRC inverter switches (Q_3 and Q_4) to adjust their gate driver duty ratios or switching frequency so the output voltage and current will be regulated as desired.

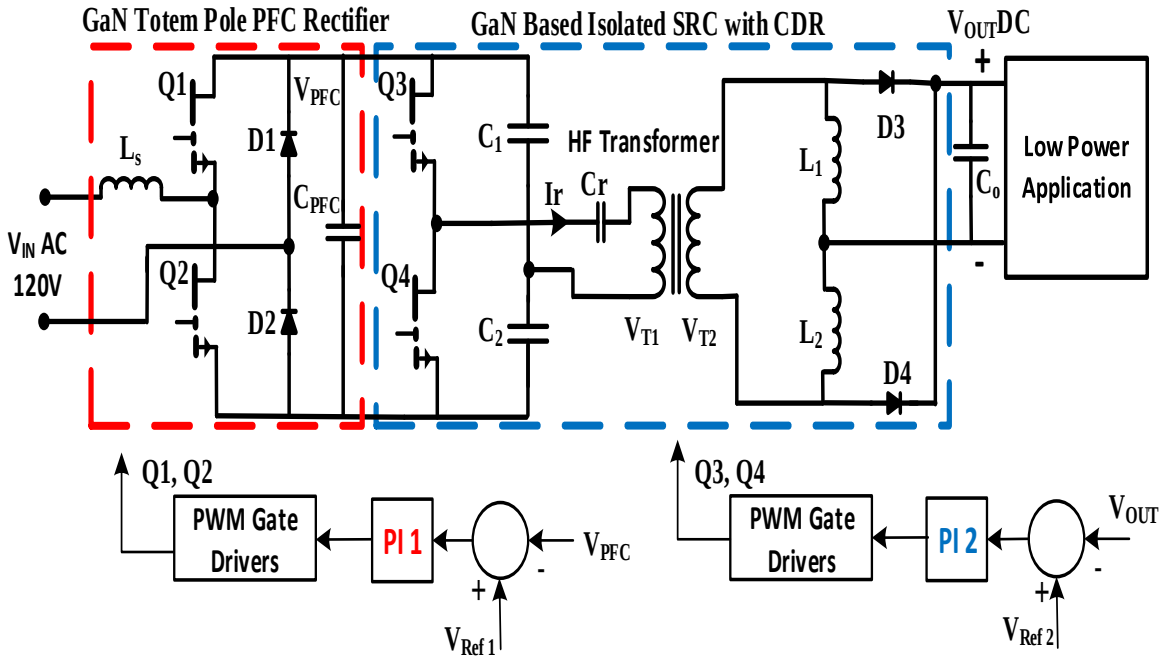


Figure 3.11. The proposed GaN AC/DC converter with PI controllers.

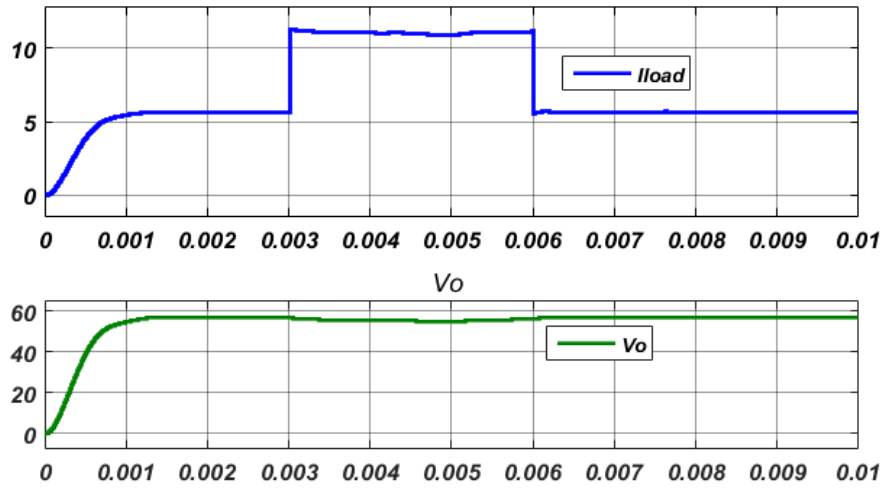


Figure 3.12. The converter output current and voltage for load step disturbance.

Figure 3.12 presents the simulation for output current and voltage during a load disturbance step change. The proposed converter simulations were performed for different loading currents and switching duty ratios. Figure 3.13 shows the main waveforms at 100 kHz which are shown before in Figure 3.4 at 64 kHz, but the output CDR inductors in Figure 3.4 have higher currents and the switches S_1 and S_2 have relatively larger duty ratios to reduce the PFC inductive current spike. The peak current values of the CDR inductors (L_1 and L_2) is around 10 A, while in Figure 3.4 it is around 22 A because of the difference between large and small loading conditions. The resonant current is sinusoidal waveform for the resonant condition (at 64 kHz) as shown in Figure 3.4, while it is a triangular current waveform for the above-resonant mode (100 kHz).

Figure 3.14 presents MATLAB simulation schematic of the isolated AC/DC topology with the two designed PI controllers. To obtain close-to-unity power factor (~0.98) and higher efficiency conversion with low harmonic distortion, the converter employs a totem-pole power-factor-correction (TP-PFC) active front end. Each PFC half-cycle of operation has an equivalent circuit produces identical operation of a bridge-rectified based boost PFC topology. Therefore, the same traditional bridge-rectified boost PFC is used as an equivalent model for the controller design.

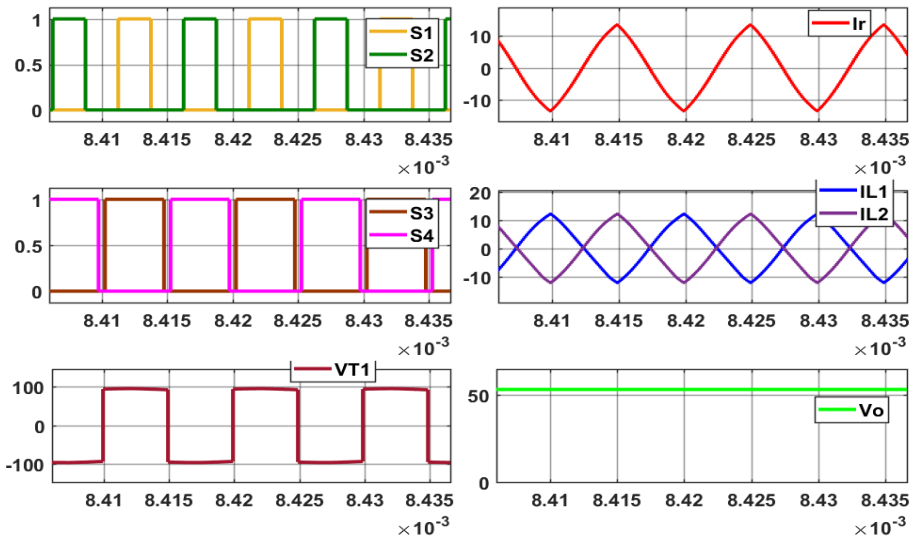


Figure 3.13. Key simulation waveforms of the proposed converter at 100 kHz.

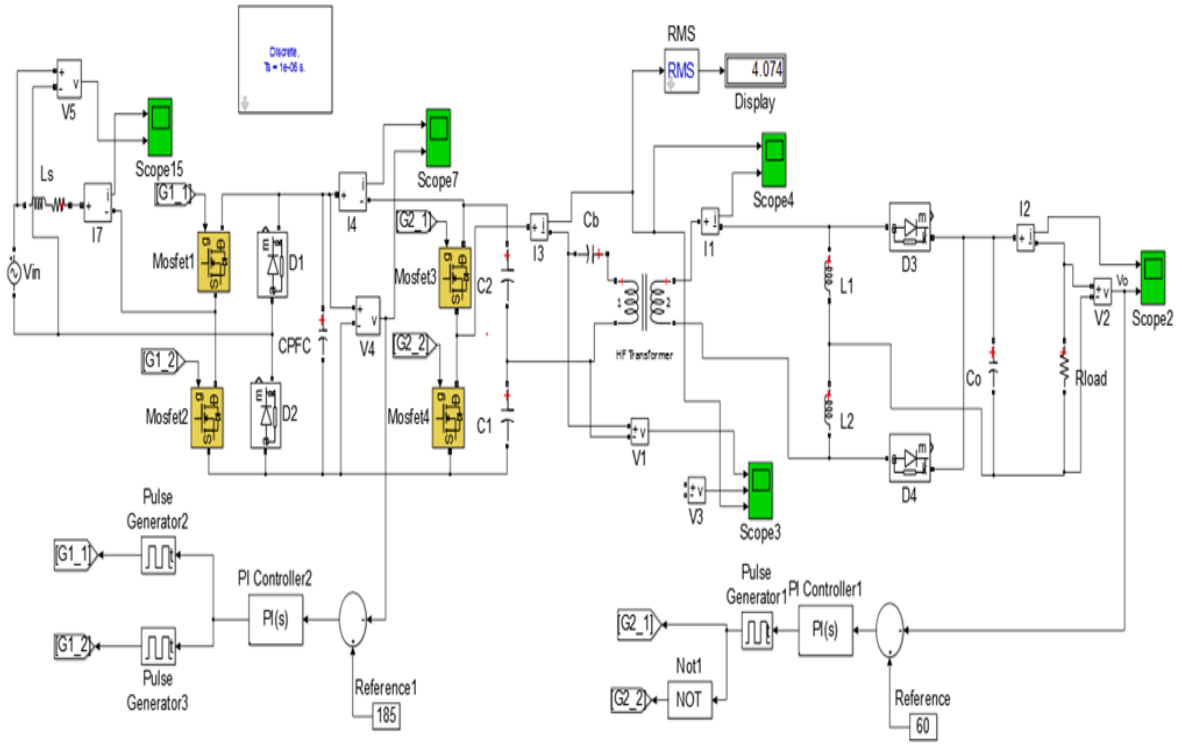


Figure 3.14. Converter closed-loop MATLAB schematic.

Figure 3.15 shows the PFC simulation waveforms of the power factor, input current (i_{Lac}), input voltage ($V_{in\,ac}$), and output voltage (V_{pfc}) which attains close-to-unity power factor, and reduced harmonic distortion to produce an average PFC output voltage of 200 V as stable dc-link [3-8]. As can be seen in Figure 3.15, the PFC ac input voltage and current are in phase. For example, at the instances t = 0.05s or t = 0.1s, both the PFC input voltage and current cross the zero at the same moment.

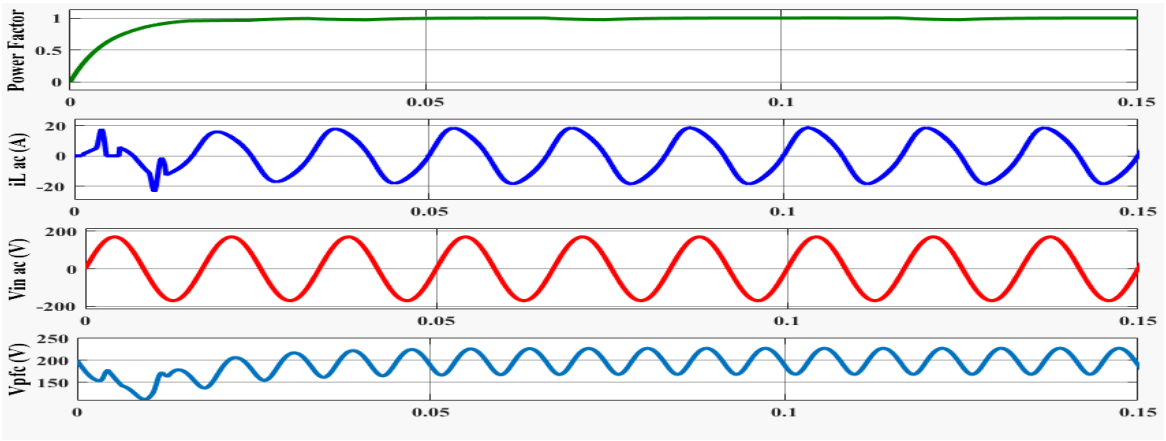
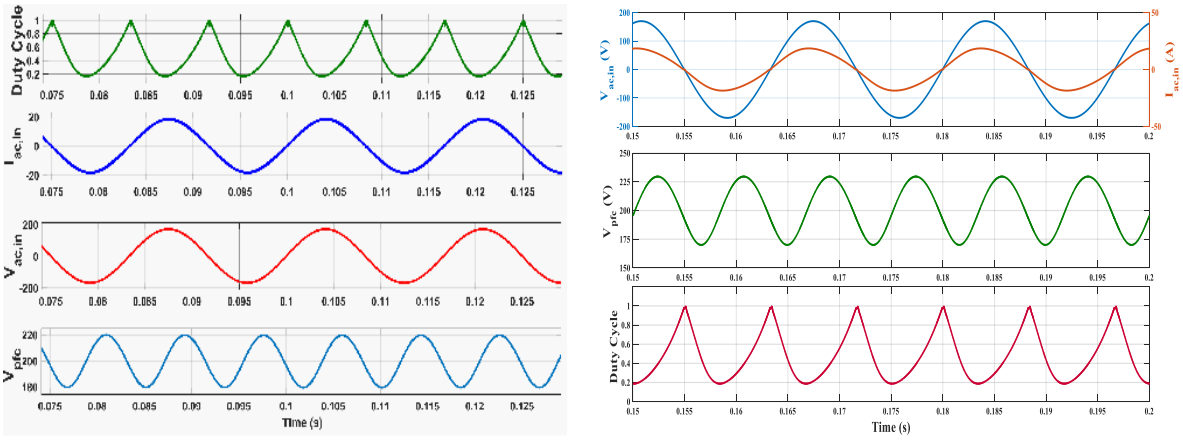


Figure 3.15. PFC control simulation waveforms [3-8].

PFC rectifier is analyzed and modeled by replacing the switch network with voltage and current sources to obtain time-invariant linearized models. The traditional bridge-rectified boost PFC is used to design average current mode control to maintain a close-to-unity power factor, and low harmonic components as shown in the simulation waveforms of Figure 3.16. Both the switching and averaged PFC models simulation give low harmonics distortion current, and close-to-unity power factor. The duty cycle waveform approaches 1 when the input voltage and current are instantaneously zero, while it becomes 0.2 when the input voltage and current are instantaneously at peak values, because it depends on the controller regulation to regulate the output voltage. Similarly, the SRC with the CDR is able to regulate the output current and voltage [3-11].

The gate driver signals for the SRC switches operating at 1 MHz and the resonant tank discontinuous conduction mode (DCM) current for light load are presented in Figure 3.17. The load resistance characteristics are affecting the current discontinuous subinterval and the current peak value. The SRC is designed for soft-switching operation such as the switching frequency matches the desired resonant frequency of the series resonant capacitor and inductor. However, in this proposed converter, SRC switches Q_3 and Q_4 are controlled by a fixed frequency PWM scheme.



A. PFC switching model simulation B. PFC averaged model simulation

Figure 3.16. PFC average current mode control simulation waveforms [3-11].

The difference between the reference voltage and the output voltage of the CDR will let SRC PI controller provide the required gate driver duty ratios for the SRC leg. Ultimately the SRC with CDR will regulate the load current and voltage as shown in Figure 3.18. The peak value of the resonant current depends on the load, while the DCM depends on the SRC switching frequency and Q_3 and Q_4 duty cycles. Applying low duty ratio signals to SRC switches yields discontinuous current in the resonant tank. A simple PI control strategy for the proposed converter is applied to rectify the AC input at near-unity power factor and produces a regulated output voltage from the CDR as shown in Figure 3.11. Two independent PI controllers are employed for the switches in the PFC and SRC blocks. Converter output voltage and current are regulated for the load through the feedback loops of the PWM duty cycle control.

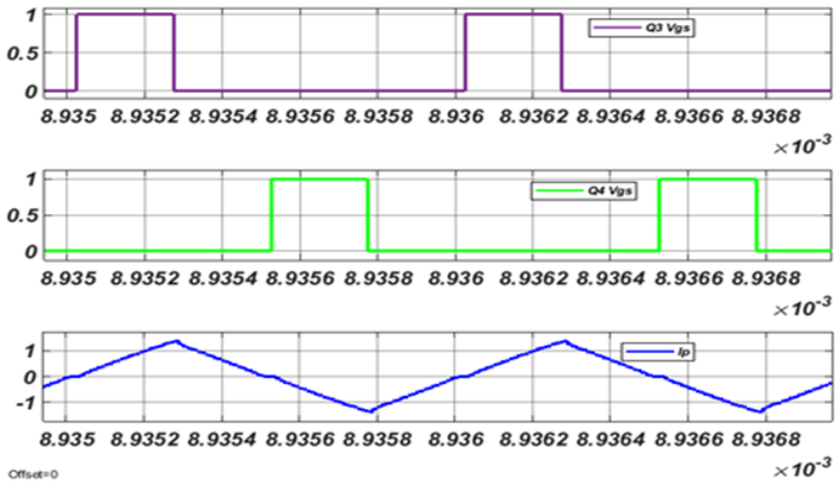


Figure 3.17. SRC gate pulses and DCM resonant tank current [3-8].

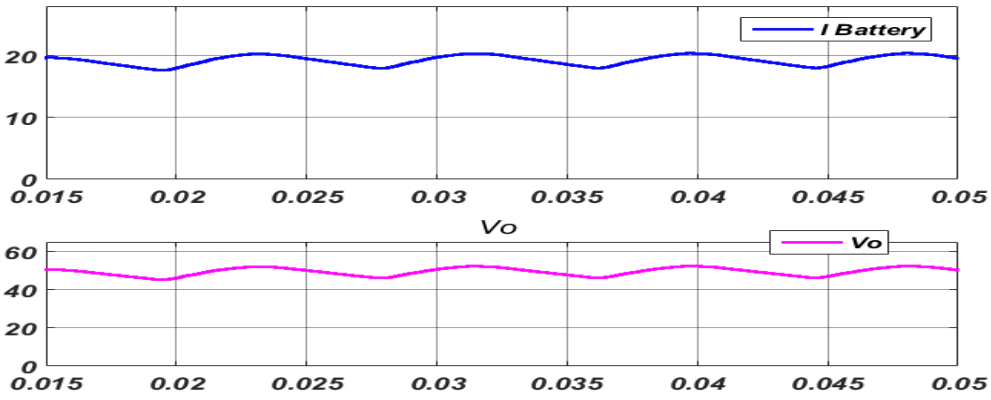


Figure 3.18. Battery voltage and charging current.

The PFC is controlled using the first PI controller with a reference voltage for the desired DC voltage, while the SRC switches duty ratios are governed by the second PI controller. The voltage open-loop transfer function of the SRC with CDR converter can be described as in [3-12]:

$$\frac{v_o}{v_i} = \left| \frac{s^2 2nC_b R_e}{s^3 C_b L_{lk} + s^2 C_b R_e c + s + \frac{R_e}{L_1}} \right| \tag{3.6}$$

where R_e is the load equivalent resistance, n is the transformer turns ratio, L_{lk} is the transformer leakage inductance employed as the resonant inductance, and L_1 is the self-inductance of the CDR inductor. The transformer magnetizing inductance is large and its effect is neglected for the sake of simplicity. The variable c is the CDR inductors (L_1, L_2) mutual inductance relationship and it is considered as:

$$c = 4 + \frac{L_{lk}}{L_1} \tag{3.7}$$

Figure 3.19 shows the control of the proposed converter for battery charging applications that requires the PFC to rectify the AC input at near-unity power factor to feed the DC-DC converter stage – this is one set of controls for the converter that will be described. The SRC operates as a voltage/current regulator for charging the battery using variable-frequency control. The PFC is controlled using an average current mode control with an input voltage feedforward path that provides a waveform shape for the inductor current to track. Combined with sensing of the current waveform, this will be referred to as the current loop control [3-11]. The bode plots of the PFC voltage and current loop are presented in Figure 3.20, while the SRC with CDR transfer function bode plot is presented in Figure 3.21. The PFC voltage loop gains are presented for the compensated, uncompensated, and for approximated voltage loop gains as well.

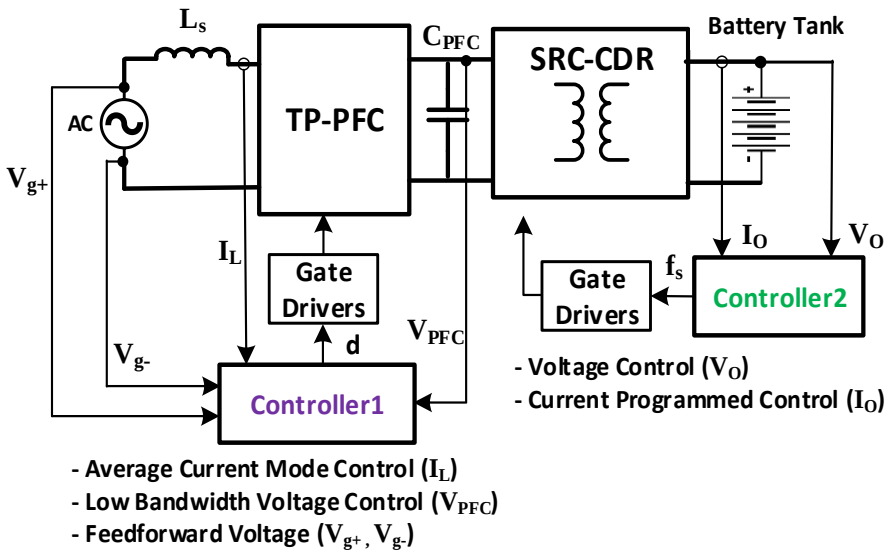


Figure 3.19. The controller diagram for the proposed converter [3-11].

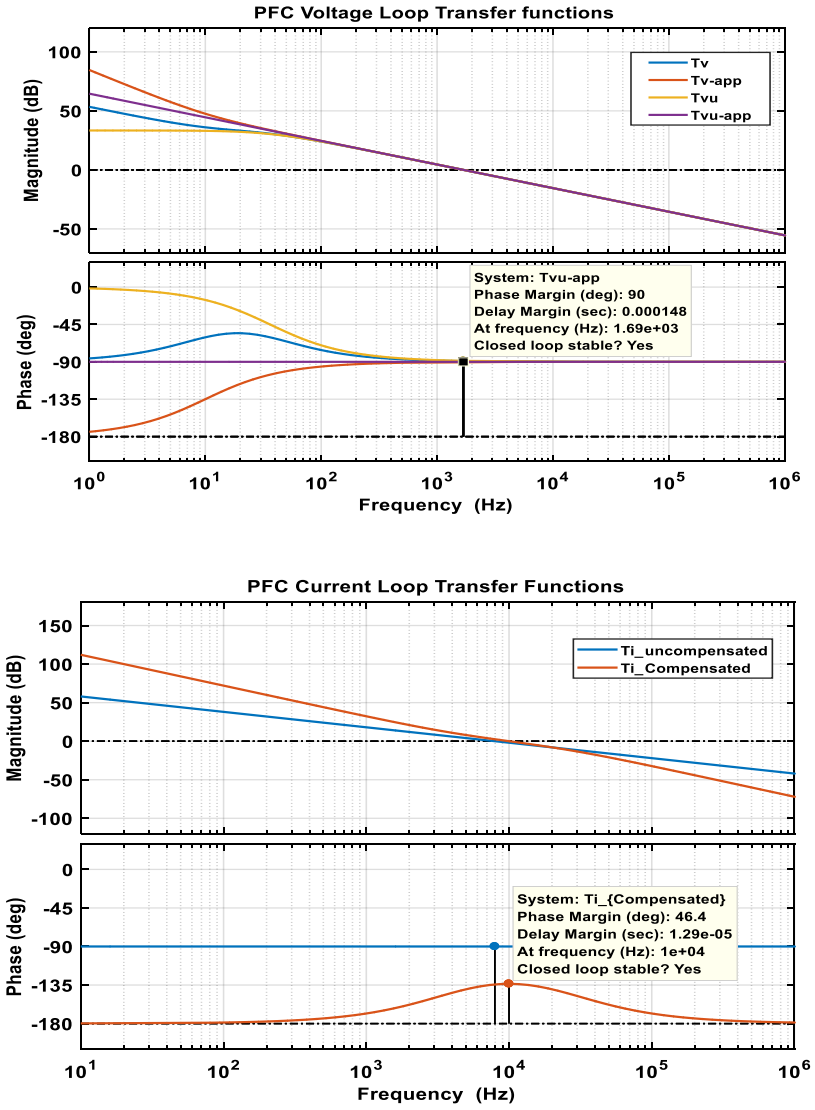


Figure 3.20. PFC voltage and current controller bode plots [3-8][3-11].

These bode plots basically show the frequency response characteristics of the closed-loop converter with 90º phase margin of the PFC voltage loop gains, and 46.4º phase margin of the PFC current loop gains. However for the SRC with CDR closed-loop stability, the phase margin is 115º for the compensated voltage transfer function. The SRC with CDR open loop transfer function can be deduced from the magnitude response shown in Figure 3.21. The slope of the magnitude is +40 dB/decade due to the two zeros, then at the second crossover frequency of the compensated loop it became -20 dB/decade because of the three poles of the transfer function as in equation 3.6. Therefore, the proposed converter with the designed PI controllers will avoid instability issues and produce the desired dynamic performance for disturbances. So, the controller design guarantees a stable steady-state performance and an appropriate transient response of the converter.

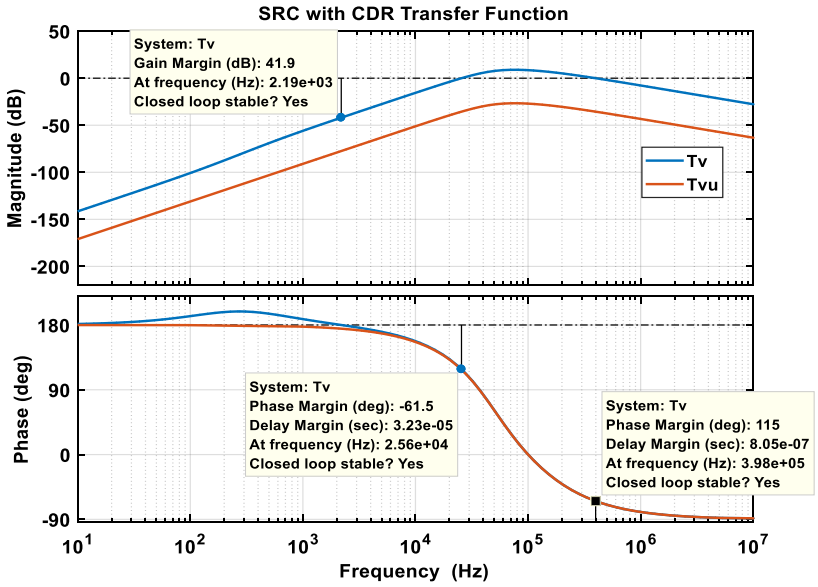


Figure 3.21. Compensated and uncompensated SRC with CDR bode plots.

3.6 Converter Modes of Operation and Equivalent Modelling

Models of the switching converter dynamics are needed for the converter control system design. Figure 3.22 shows the equivalent simplified main operating modes of the entire proposed converter referred to the transformer primary side. Mode 1 is for the interval when Q_1 and Q_3

are ON as shown in Figure 3.3 and Figure 3.13, while Mode 2 is for the interval when Q_2 and Q_4 are ON. The equivalent simplified steady-state space equations of the proposed converter operating modes have been derived using KVL and KCL for the topology. In any well-designed converter, the output voltage switching ripple should be small and minimized by appropriate low-pass filters to block the switching harmonics. Also, it is desirable to only model the important dc components of any waveform, and ignore the complicated small ripples [3-13].

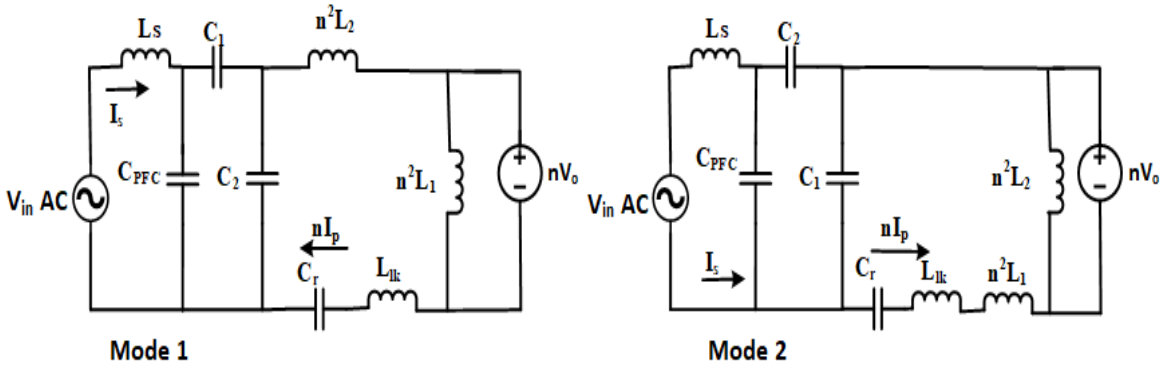


Figure 3.22. Converter equivalent circuits referred to the HF-XFMR's primary side.

The state variables are considered as: PFC inductor (Ls) current, C_1 and C_2 voltages, transformer primary current, and resonant capacitor voltage, i.e., X = [i_s, V_{c1}, V_{c2}, i_p, V_{cr}]. Applying KVL and KCL to the converter mode 1 equivalent circuit yields the following state equations, where L_{lk} is transformer leakage inductance, and n is its turns ratio.

$$V_s = L_s \frac{di_s}{dt} + V_{C1} + V_{C2} \tag{3.8}$$

$$i_s = C_1 \frac{dV_{C1}}{dt} + C_{PFC} \frac{dV_{CPFC}}{dt} \tag{3.9}$$

$$I_{C2} = C_2 \frac{dV_{C2}}{dt} = i_s - ni_p - I_{CPFC} \tag{3.10}$$

$$V_{C2} = n^2 L_2 \frac{ndi_p}{dt} + nV_o + L_{lk} \frac{ndi_p}{dt} + V_{Cr} \tag{3.11}$$

$$nV_o = n^2 L_1 \frac{nd(i_p - i_o)}{dt} \tag{3.12}$$

$$ni_p = C_r \frac{dV_{Cr}}{dt} \tag{3.13}$$

From equation (3.8): $$\frac{dx_1}{dt} = \frac{1}{L_S}(V_s - V_{C1} - V_{C2}) \tag{3.14}$$

The equivalent values of the CDR inductors (L_1, L_2) referred to the primary-side are n^2L_1 and n^2L_2, respectively.

Equations (3.9) and (3.10) are simplified by assuming that C_{PFC} in the topology is much larger than C_1 and C_2, so neglecting the effects of I_{CPFC} in equations (3.9) and (3.10) yields:

$$\frac{dx_2}{dt} = \frac{i_s}{C_1} \tag{3.15}$$

$$\frac{dx_3}{dt} = \frac{1}{C_2}\left(i_s - ni_p\right) \tag{3.16}$$

From equations (3.11) and (3.12) and by assuming that $\frac{d(i_p - i_o)}{dt} = \frac{di_p}{dt}$ as the load current is not a state variable, and then after mathematically simplifying the equation,

$$\frac{dx_4}{dt} = \frac{V_{C2} - V_{Cr}}{n\,L_{lk} + n^3(L_1 + L_2)} \tag{3.17}$$

From equation (3.13),

$$\frac{dx_5}{dt} = \frac{n\,i_p}{C_r} \tag{3.18}$$

From equation (3.12), the output voltage is,

$$v_o = n^2 L_1 \frac{dx_4}{dt} = \frac{nL_1(V_{C2} - V_{Cr})}{L_{lk} + n^2(L_1 + L_2)} \tag{3.19}$$

The averaged state-space model for the equivalent simplified steady-state operating modes of the converter is shown below. This state-space model is a mathematical model derived to obtain an average description of the converter topology for one switching cycle to present the main

modes of operation. The main modes of operation are analyzed by considering the switches pulses of the key waveforms shown in Figure 3.13.

$$\dot{X} = \begin{bmatrix} 0 & \frac{-1}{L_s} & \frac{-1}{L_s} & 0 & 0 \\ \frac{1}{C_1} & 0 & 0 & 0 & 0 \\ \frac{1}{C_2} & 0 & 0 & \frac{-n}{C_2} & 0 \\ 0 & 0 & \frac{1}{nL_{lk}+2Ln^3} & 0 & \frac{-1}{nL_{lk}+2Ln^3} \\ 0 & 0 & 0 & \frac{n}{C_b} & 0 \end{bmatrix} \begin{bmatrix} i_s \\ V_{c1} \\ V_{c2} \\ i_p \\ V_{cb} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_s} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} U \tag{3.20}$$

$$Y = V_{out} = \begin{bmatrix} 0 & 0 & \frac{nL}{L_{lk}+2Ln^2} & 0 & \frac{-nL}{L_{lk}+2Ln^2} \end{bmatrix} X \tag{3.21}$$

where, $C_1 = C_2 = C$, $L_1 = L_2 = L$, L_{lk} is transformer leakage inductance, L_s is the primary PFC inductance, D is the duty cycle for mode 1 operation, and n is the transformer turns ratio. The transfer function is derived from the above state-space equations (3.20) and (3.21) as:

$$T(s) = \frac{V_{out}(s)}{V_{in}(s)} = C(SI - A)^{-1}B = \frac{L\,S^2}{\Delta C L_s\,(n^3\,L_{lk}+2nL)} \tag{3.22}$$

where, Δ is the determint of $(SI - A)$.

$$\Delta = |SI - A| =$$

$$\begin{vmatrix} s & {}^{1}/_{L_s} & {}^{1}/_{L_s} & 0 & 0 \\ {}^{-1}/_{C_1} & s & 0 & 0 & 0 \\ {}^{-1}/_{C_2} & 0 & s & {}^{n}/_{C_2} & 0 \\ 0 & 0 & {}^{-1}/_{(nL_{lk}+2Ln^3)} & s & {}^{1}/_{(nL_{lk}+2Ln^3)} \\ 0 & 0 & 0 & {}^{-n}/_{C_r} & s \end{vmatrix}$$

$$\Delta = S^4 + \frac{2\,S^2}{CL_s} + \frac{n}{(nL_{lk}+{}^{2L}/_{n})}\left[\frac{S^2}{C_r} + \frac{S^2}{C} + \frac{2}{CC_rL_s} + \frac{1}{C^2L_s}\right] \tag{3.23}$$

Figure 3.23 depicts another equivalent model for the entire converter. As shown, M is the HF transformer primary and secondary mutual inductance. The PFC is presented as a two-port model for the ideal rectifier called loss-free resistor (LFR) model, while the SRC is modeled

by the equivalent first harmonic approximation (FHA) method as documented in [3-13]. The PFC lossless two-port network includes the average power transferred to the dependent power source as drawn. Then the CDR is modeled for positive coupling configuration as explained in [3-12] for the coupled inductors. In the proposed series resonant converter (SRC) investigated in this dissertation, the output current doubler rectifier (CDR) is primarily driven by the resonant tank current. The output voltage from the CDR is regulated by the large output capacitor to remove switching frequency harmonics. To simplify the circuit analysis for the designed SRC topology, it is modeled as a fundamental voltage source, while the power factor correction (PFC) rectifier is modeled using the effective resistor R_e. Then the entire equivalent circuit model of the topology is solved by a standard linear analysis approach including deriving voltage transfer function.

Figure 3.24 shows a feedback control model simulated to study the stability issues for the converter. With this feedback control model, the controller is designed to maintain a close-to-unity power factor, low harmonic components, and high efficiency power supply. The PFC state-space model is used with the first PI controller to provide the control signal to the second PI for the half-bridge SRC and CDR transfer function model.

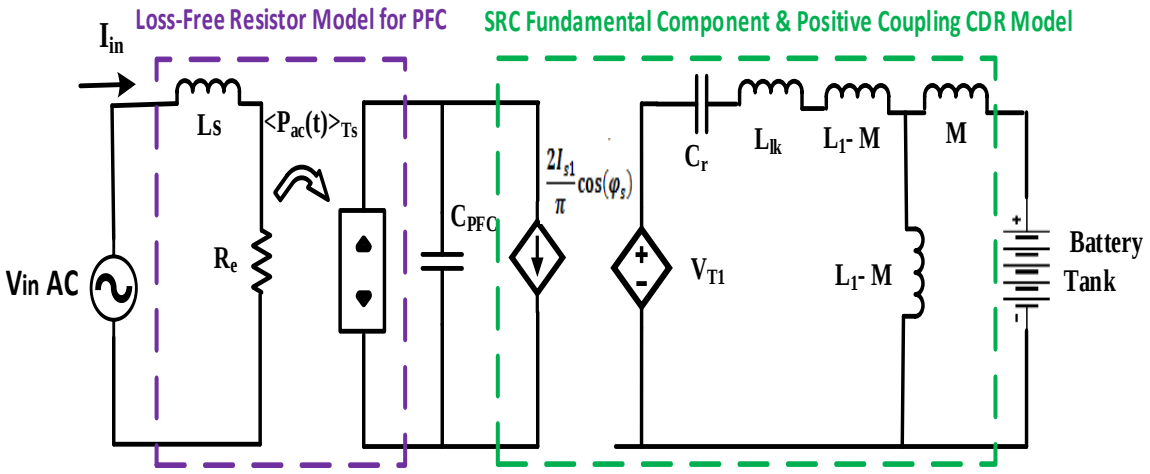


Figure 3.23. The equivalent model for the proposed converter.

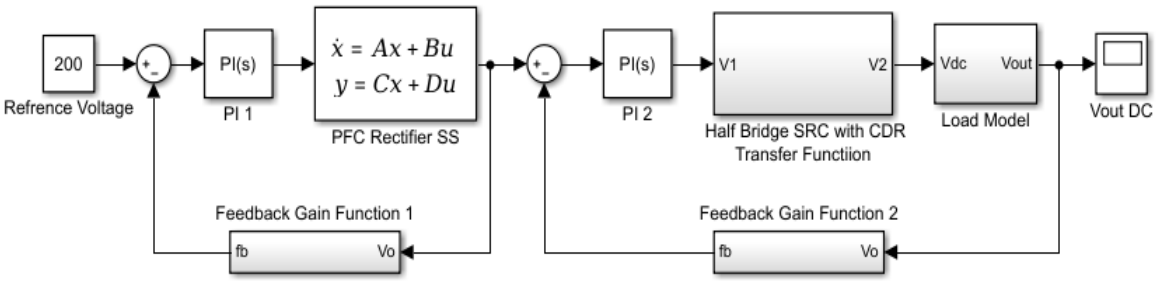


Figure 3.24. Feedback control simulation for the power supply converter.

3.7 Converter Loss Analysis

Losses in any converter come typically from inductor winding resistances, semiconductors ON resistances and forward voltage drops, and switching losses. So a converter model is developed to account for all of the loss elements to predict the voltages, currents and efficiency of non-ideal converters. Basically inductor volt-second balance and capacitor charge-balance principles are applied to derive the simplest dc equivalent circuit for the converter under consideration [3-13]. In addition, GaN-based high-frequency converters are highly sensitive to the design layouts and their parasitics. Therefore, parasitics mitigation and signal integrity of the high-frequency converters experimental setups are of high priority. However, in this section the investigated GaN converter is only analyzed from the perspective of conduction and switching losses of the circuit components.

Considering the efficiency and losses in the switching converter is an important step in equivalent circuit analysis. The obvious components in the proposed converter as shown in Figure 3.1 and Figure 3.11 are categorized as follow [3-8]:

- Semiconductors losses: Diodes (D_1:D_4) and GaN switches (Q_1: Q_4).
- Passive losses: Inductors (L_s, L_1, L_2) and capacitors (C_{PFC}, C_1, C_2, C_r, C_o).
- High-frequency transformer losses: Leakage and magnetizing inductances (L_{lk}, L_M), core and winding losses. A designed 1 MHz transformer efficiency is 99.3 %, while the

fabricated 100 kHz nanocrystalline transformer efficiency is 98.2 % as explained in Chapter 4.

The GaN switches drain-to-source ON resistance $R_{DS}(on)$ typically is 100 mΩ for GS66504B at T_J = 25 °C. Also, its drain-to-source leakage current I_{DSS} is 1 µA. So the average switching, conduction, and leakage power loss for the GaN switches (Q_1:Q_4) can be estimated as:

$$P_{GaN} = 4\left(0.5V_d I f_s\left(t_{on} + t_{off}\right) + I^2 R_{DS(on)} D + I_{DSS} V_d\right) \quad (3.24)$$

where V_d is the applied voltage on the transistor during OFF state, I is the transistor average ON current, f_s is the switching frequency (1 MHz), (t_{on}+ t_{off}) are turn ON and turn OFF transition times intervals, $R_{DS(on)}$ is the transistor ON resistance. For the proposed 120Vac to 48Vdc/60Vdc converter, operating at 1 MHz for 1.4 kW load, the average power loss taking into account the GaN switching, conduction, and leakage current losses is:

$P_{GaN} = 4(0.5*160*12*10^6(0.02*10^{-6}) + 12^2 *0.1*0.375 + 10^{-6} * 160) = 98.4$ W.

The diodes power loss can be estimated by:

$$P_D = 4(V_D I_{Dav} + I_{Drms}^2 r_D + 0.25\, Q_{rr} V_{Drr} f_s) \quad (3.25)$$

where V_D is the diode forward voltage, I_{Dav} and I_{Drms} are the diode forward average and rms currents, respectively, r_D is the diode resistance during conducting, Q_{rr} and V_{Drr} are the diode reverse-recovery charge and voltage, respectively.

3.8 Converter Simulation in PSpice

Figure 3.25 shows the PSpice simulation schematic for a simplified isolated DC/DC converter, which is a half-bridge inverter with CDR as an output stage of the entire AC/DC converter. The simulation results of the transformer secondary-side voltage and the output DC voltage are shown in Figure 3.26.

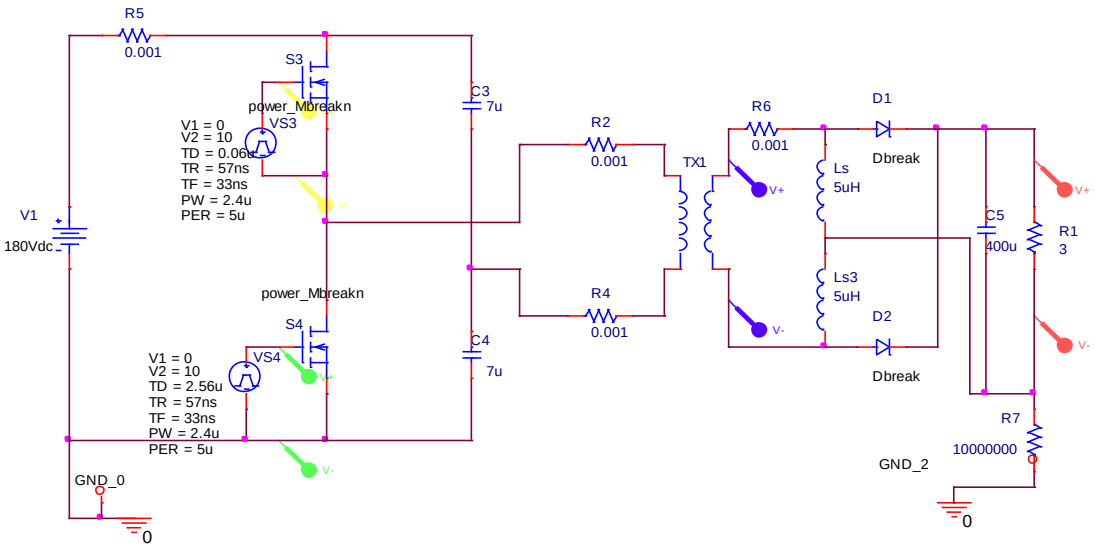


Figure 3.25. PSpice simulation schematic for an isolated half-bridge inverter with CDR.

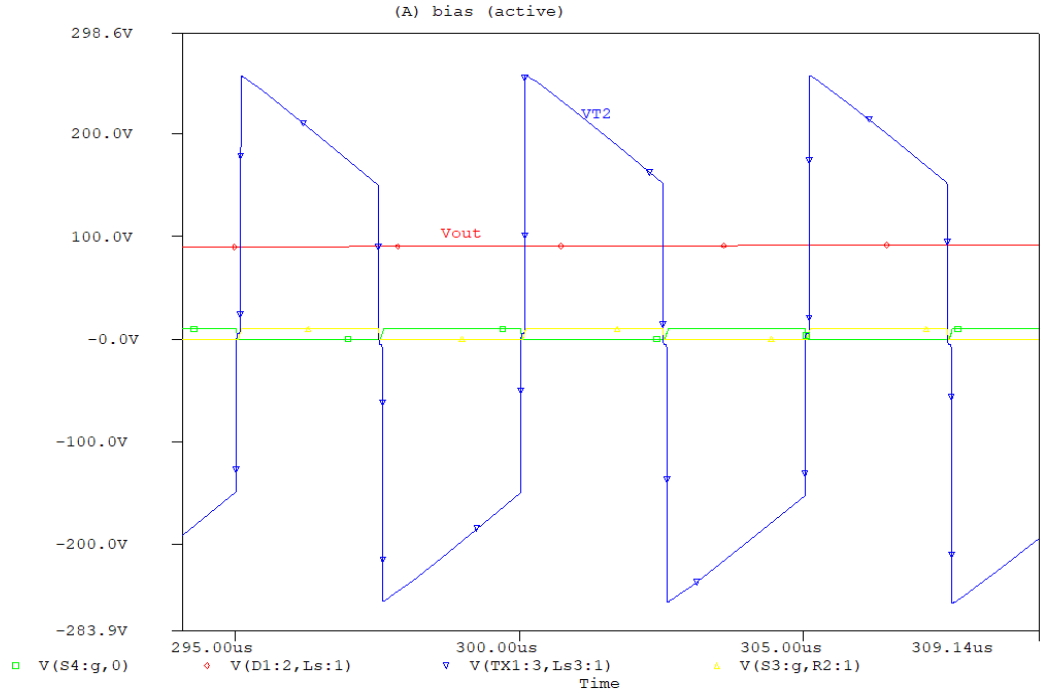


Figure 3.26. PSpice simulation waveforms for the half-bridge with CDR topology.

The DC input voltage is assumed 180 V, which yields a transformer secondary-side voltage of 200 V high-frequency (200 kHz) rectangular signal, and an output DC voltage of 85 V. The PFC stage also has been separately simulated in PSpice as shown in Figure 3.27 for its input and output voltages waveforms operating in an open loop power factor correction rectifier model. As can be seen, the PFC AC input voltage is 120 V at 60 Hz and the output dc voltage has an average voltage of 270 V.

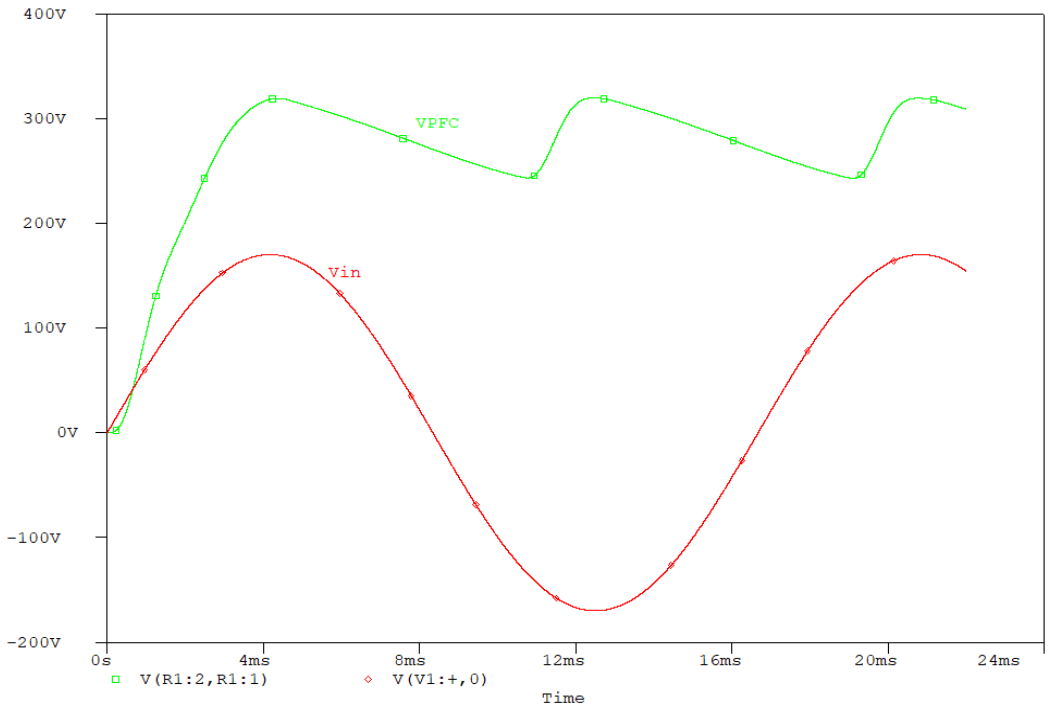


Figure 3.27. PSpice PFC stage simulation input and output voltages waveforms.

Figure 3.28 illustrates the PSpice schematic for the proposed AC/DC converter which contains the PFC with an isolated half-bridge inverter and CDR. This is simulated for hard-switching operation as the half-bridge inverter on the transformer primary does not have a series resonant capacitor, and as such, it is not a series resonant converter. The results (V_{PFC}, V_{T1}, V_o) of this PSpice converter are shown in Figure 3.29 and Figure 3.30 for the simulated waveforms at a switching frequency of 200 kHz for an RMS input voltage of a 71 V and a 120 V input voltage, respectively.

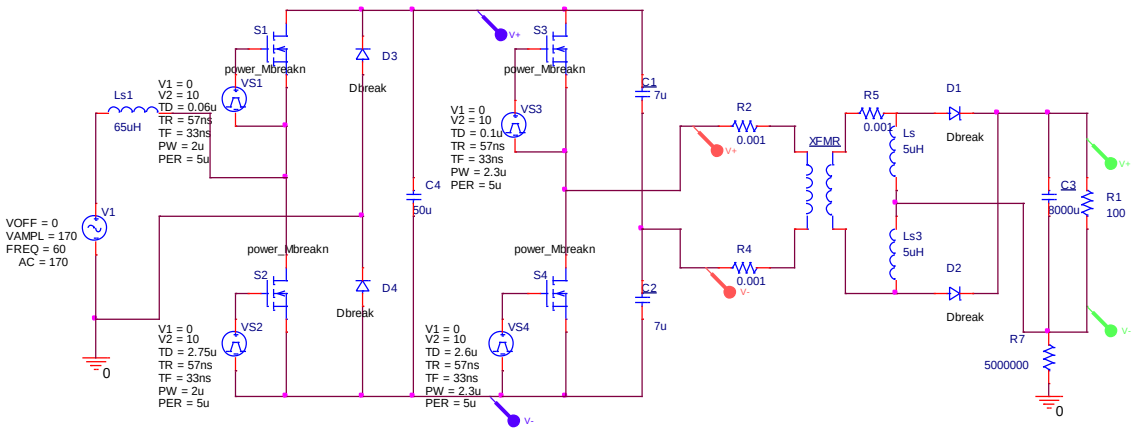


Figure 3.28. PSpice schematic for a PFC with an isolated half-bridge inverter and CDR.

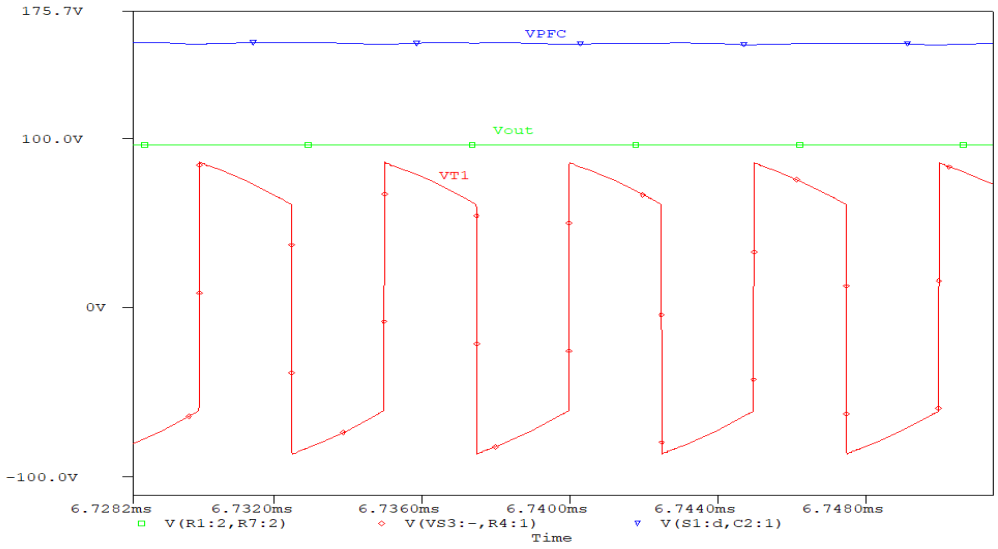


Figure 3.29. PSpice simulation waveforms (V_{PFC}, V_{T1}, V_o) at 200 kHz for low input voltage.

The PFC output voltage is 205 V and the output DC voltage is 80 V as presented in Figure 3.30. The transformer primary voltage presents voltage oscillations and ringing due to the low capacitor (50 µF) used at the PFC output DC bus, so for the rated input voltage of 120 V a larger PFC output DC bus capacitor (around 450 µF) must be used. Also the effects of the half-bridge inverter capacitors (C_1 and C_2) as their midpoint voltage is increasing and decreasing with charging and discharging cycles, which causes the voltage sag of the simulated V_{T1} waveform. Moreover, the dead time period of the used 46% duty ratio of the transistors caused the noticed voltage oscillations at the end of each half cycle.

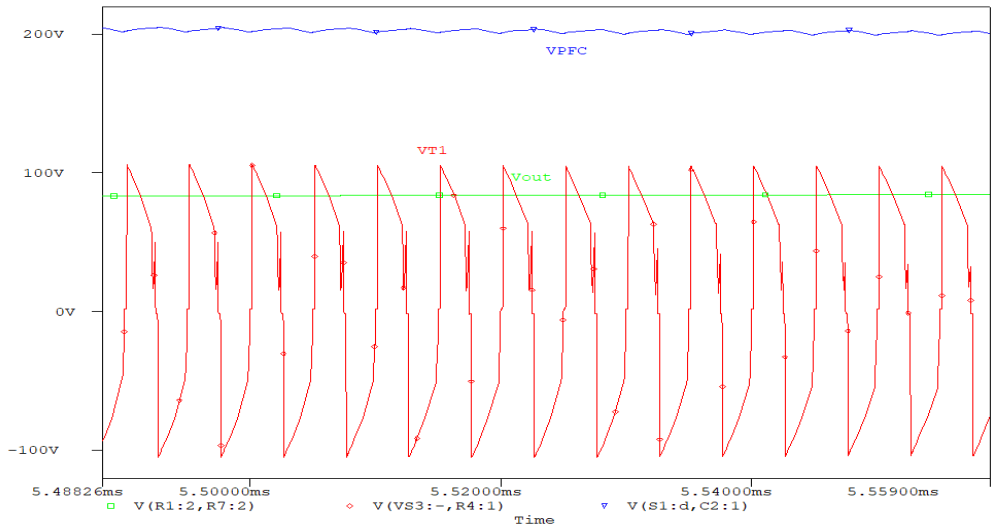


Figure 3.30. PSpice simulation waveforms of V_{PFC}, V_{T1}, V_o for V_{in} = 120 V.

3.9 Conclusion

This Chapter illustrates the analysis, simulation and modeling of the GaN isolated AC/DC converter to achieve a conversion of 120Vac to 48Vdc/60Vdc at 100 kHz and 200 kHz for a 1.4 kW application. Moreover, among the desired features of the designed converter is to obtain a high-efficiency power supply converter maintain close-to-unity power factor, low-harmonic input contents (<5%). The theoretical operation concepts, modeling and simulation of the investigated GaN AC/DC converter are covered and discussed. The investigated converter topology is extensively simulated in MATLAB and PSpice, and the main simulation waveforms of the proposed converter with the output current and voltage are illustrated for various gate driver duty ratios and switching frequencies. The converter offers the advantages of power flow control of the solid-state transformer, low harmonics and close-to-unity power factor of the PFC rectifier, soft-switching of the half-bridge SRC, reduced size of high-frequency transformer, and smaller leakage inductance of the CDR which is used for low-voltage high-current applications as the CDR draws half of the load current in the transformer secondary side. Also, state-space analysis for the converter is performed in order to derive the transfer function of the isolated AC/DC converter. Then the closed-loop converter controller is designed, simulated, and discussed. Stability operation of the converter is shown through the sufficient phase margins of the converter frequency response. Furthermore, a new equivalent circuit model for the converter is constructed consisting of a loss-free resistor model for the PFC rectifier with first harmonic approximation model for the SRC and the CDR. Positive coupling configuration is used for the CDR model as it yields almost zero current ripple in the output capacitor. The PFC lossless two-port network includes the average power transferred to the dependent power source as drawn. Then the CDR is modeled for positive coupling configuration for the coupled inductor. In the SRC investigated in this dissertation, the output CDR is primarily driven by the resonant tank current, while the output voltage of the CDR is

regulated by a voltage feedback controller with a large output capacitor to remove any high-frequency harmonics. The contribution of this work is the new equivalent circuit model for the demonstrated GaN isolated AC/DC converter, state-space equations, transfer function, and controllers design which are derived and presented.

3.10 References

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CHAPTER 4

HIGH-FREQUENCY TRANSFORMER DESIGN

4.1 Introduction

Solid-State Transformer (SST) has been utilized with promising features for several niche applications. High-frequency (HF) transformer is the isolation and significant element in any SST topology. This chapter reviews, highlights, and explains the methodology steps of designing medium and HF transformer, and its optimum electrical and magnetic specifications. Then it demonstrates two different design examples for low power SST topologies. Experimental HF transformers are demonstrated for building 25 kHz, 5 kVA, 440/110V amorphous core transformer, and 100 kHz, 350 VA, 130/117V nanocrystalline core transformer. These two examples have been tested for low power operation. Also, theoretical concepts about the operation of selected transformer cores are addressed. The fabrication and experimentally investigation for constructing the two different transformers and their main operational features are presented. Also, evaluation of the two different magnetic materials at wide frequency range in term of cost, losses, and volume is presented. MATLAB has been used for programming the design methodology of the HF transformers.

SST has reduced weight and size, moreover, it allows bidirectional power flow control with additional voltage regulation and voltage disturbance rejection functionality. SST is very convenient for many applications since better automation and control algorithm can be developed. Also, SST will help gaining more advantages for power quality, storage management, and power flow control in addition to the reduction of volume and weight compared to the traditional transformer [4-1, 4-2]. The essential part of the SST is the isolated DC/DC converter which is operated at a medium or high frequency. Therefore, HF transformer design steps will be reviewed and demonstrated to utilize the advantages of SST operation and

functionalities. The designed 100 kHz, 350 VA, 130/117V nanocrystalline core transformer (example 2) in this dissertation is adopted in the investigated GaN AC/DC converter topology to achieve some of the SST features and functionality advantages for low power applications.

4.2 High-Frequency Transformer Design Methodology

The design methodology for medium and high-frequency transformer has been described in [4-3, 4-4, 4-5], and further investigated and disscussed in [4-6, 4-7, 4-8]. Figure 4.1 shows the main steps for designing HF transformer which are sumarized and reviewed in this chapter.

1. Topology Specifications: The following fundamental specifications of the topology are identified: rated power, voltage, frequency, temperature, target effieciency, duty cycle, and desired leakage inductance for the optimum operation of the topology.

2. Select the magnetic core: core material should be chosen taking into account cost, efficiency and volume. Amorphous, ferrite, and nanocrystalline magnetic materials were compared in [4-9] regarding the core losses at 10, 20, 50, and 100 kHz. Since the amorphous magnetic material has the highest saturation density, it yields the smallest core volume. Also, the cost for amorphous magnetic material is less than nanocrystalline material. Therefore amorphous magnetic material was chosen for the first transformer design example, while the second transformer design example is nanocrystalline material based on the desired switching frequency. After selecting the core material, its coefficients (K_c, α, β) and saturation flux density (B_{sat}) are taken from the manufacturer datasheet.

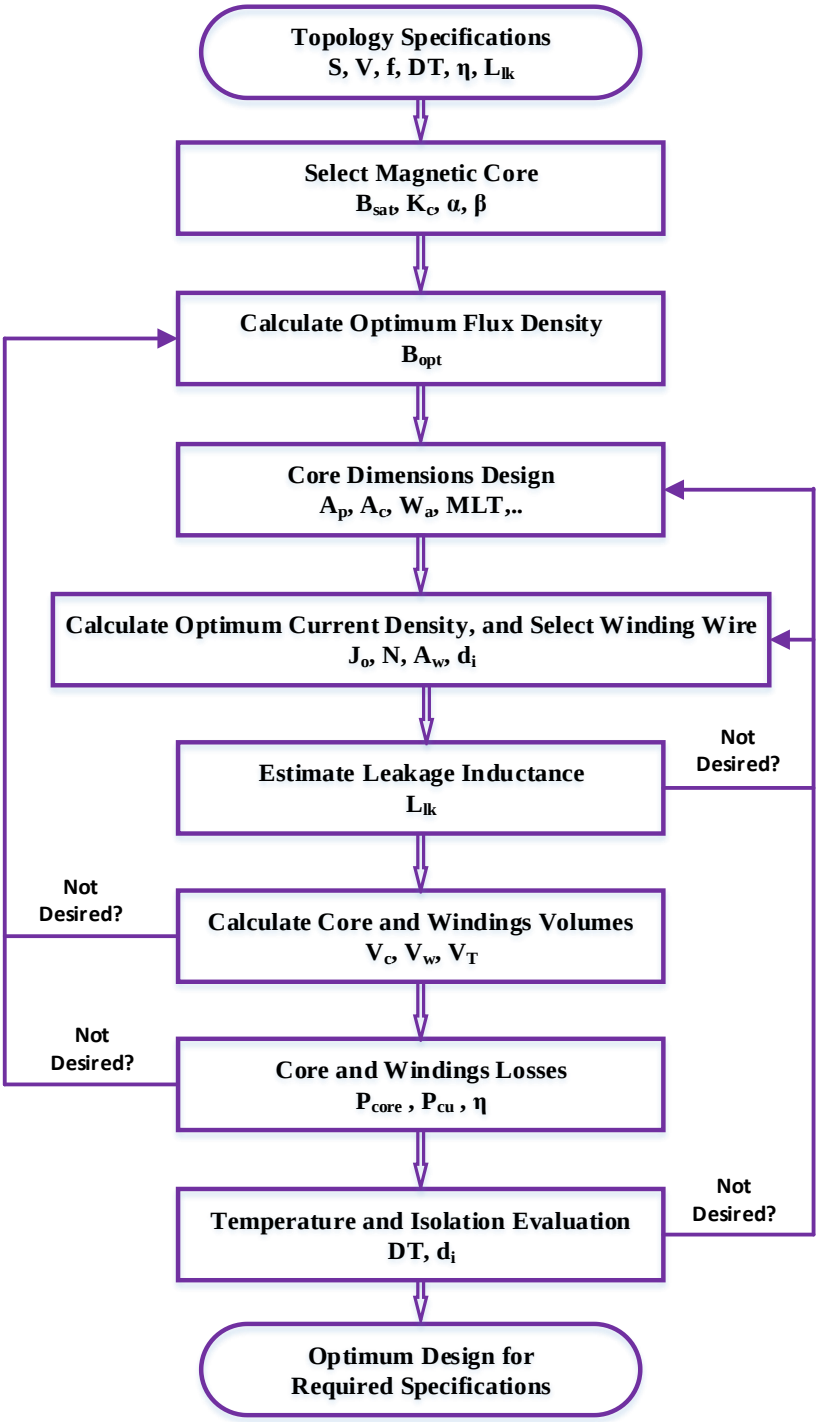

Figure 4.1. HF Transformer Design Procedure [4-3:4-8].

According to Figure 4.2 [4-9], at 50% duty cycle, 0.1T peak flux density, and f =100 kHz, the nanocrystalline material (Vitroperm 500F) has approximately 8 times lower losses than that of the ferrite (3C94) material, and the latter has approximately 1.5 times lower losses than the amorphous (Metglas 2605SA1) material.

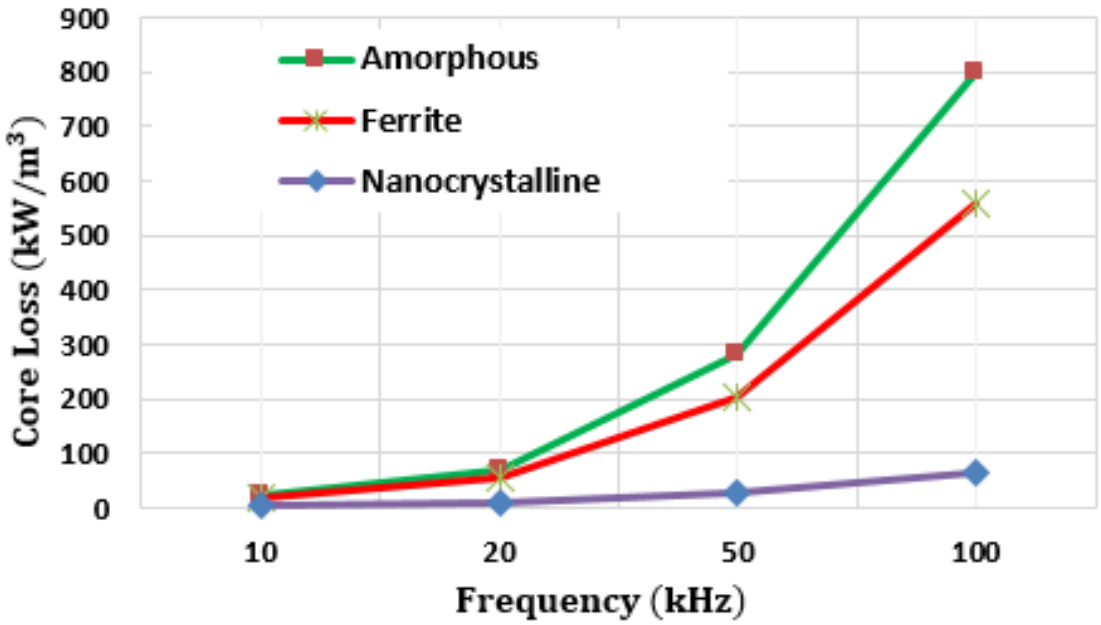

Figure 4.2. Magnetic materials core losses (kW/m^3) versus frequency [4-7][4-9].

So, for higher frequency (100 kHz or higher) nanocrystalline is much more efficient than ferrite and amorphous magnetic materials. However, for a frequency of 25 kHz, the losses are similar to each other, while the amorphous core material is cheaper than the nanocrystalline material. Table 4.1 shows the main properties parameters for the selected soft magnetic materials [4-9].

Table 4.1. Selected soft magnetic materials properties parameters [4-9].

Parameter	Amorphous	Nanocrystalline
B_{sat} (T)	1.56	1.2
Curie Temperature (^{o}C)	399	600
Permeability μ_i (x10^3)	10-150	15
K_c (W/m^3)	1.3617	2.3
α	1.51	1.32
β	1.74	2.12

3. Calculate optimum flux density: Equation 4.1 is the formula derived in [4-3, 4-5] to calculate the flux density which yields the minimum total losses of the transformer core and copper.

$$B_{opt} = \frac{(h_c k_a \Delta T)^{2/3}}{2^{2/3}\,(\rho_w k_w k_u)^{1/12}\,(k_c K_c f^{\alpha})^{7/12}} \left(\frac{k_v f k_f k_u}{\sum VA}\right)^{1/6} \quad (4.1)$$

where, the core coefficient parameters are typically as: k_a = 40, k_c = 5.6, k_w =10 [4-3, 4-5, 4-6], h_c is the heat transfer coefficient, the suggested value for the window utilization factor k_u is 40% [4-3, 4-5, 4-6], the core stacking factor k_f typically is 0.95 for laminated cores, and the winding voltage waveform factor k_v is 4 for a square voltage waveform and 4.44 for sinusoidal waveform [4-4, 4-6]. Figure 4.3 shows transformer core, winding, and total loss verses the flux density. The optimum flux density is targeted to yield the minimum total loss.

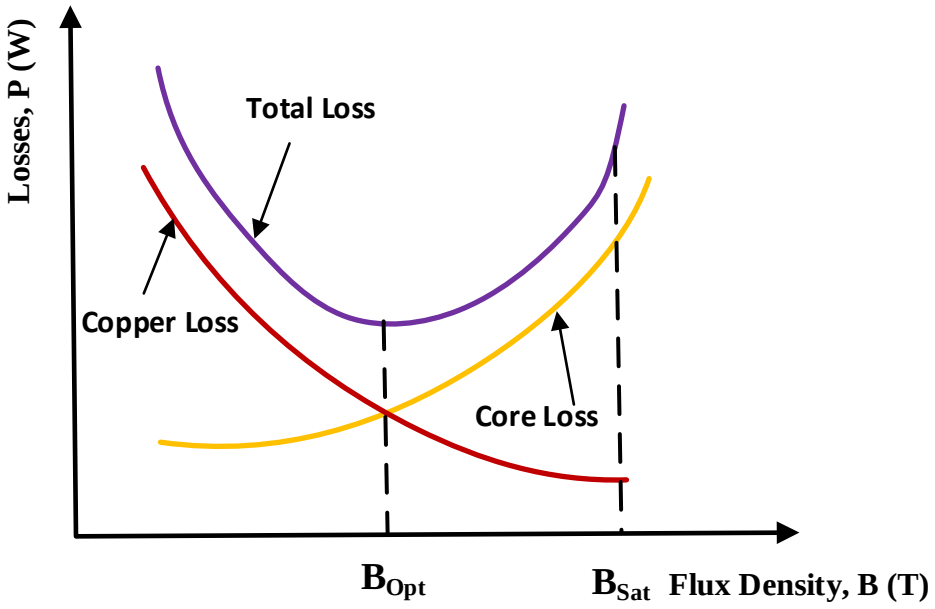

Figure 4.3. Core, winding, and total loss verses flux density [4-5] [4-7].

4. Core dimension design: The area product is calculated from equation 4.2 in cm^4 [4-3, 4-5] for the obtained optimum flux density, then the appropiriate core size is selected. The area product (A_p) is the prodcut of a transofrrmer window area (W_a) with the core cross sectional area (A_c) as shown in Figure 4.4.

$$A_p = \left(\frac{\sqrt{2}\,\sum VA}{k_v f B_{opt} k_f k_t \sqrt{k_u \Delta T}}\right)^{8/7} \quad (4.2)$$

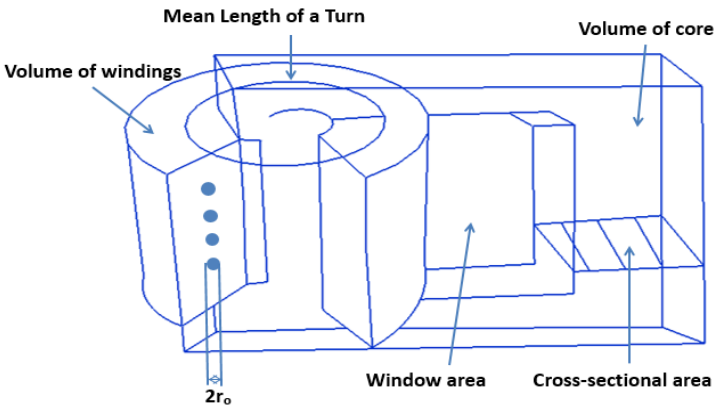

Figure 4.4. Transformer core and winding typical layout [4-5].

5. Calculate optimum current density and select winding wire: Equation 4.3 is used to determine the desired current density in A/m^2, taken into acount copper and core losses, and the thermal heat transfer for the transformer [4-3, 4-5, 4-6].

$$J_o = \sqrt{\frac{h_c k_a}{\rho_w k_w}} \cdot \sqrt{\frac{\Delta T}{2k_u}} \cdot \frac{1}{\sqrt[8]{A_p}} \tag{4.3}$$

where: ρ_w is the selected wire resistivity. Next are typical values for flux density and area product calculations:

ρ_w =1.72* 10^{-8} Ω-m, h_c = 10 W/m^2 C^o [4-5].

Then the primary and secondary windings number of turns are calculated from equation 4.4 [4-5]:

$$N = \frac{V_{rms}}{K_v f B_{max} A_m} \tag{4.4}$$

where B_{max} is the the smaller value of either B_{opt} or the material saturation flux density (B_{sat}). The conduction area of windings should be determined for the obtianed current density, and the radius of desired wire strand which considers the skin effect is calculated by equation 4.5 [4-4] to choose the appropriate wire equivalent size.

$$\varepsilon = \frac{6.62}{\sqrt{f}} \tag{4.5}$$

where, ε is the skin depth which is the distance under the wire surface where the AC current density is 37% of its surface current value [4-4].

Conductors losses are reduced for Litz wires which can reduce the skin and proximity effects at high frequencies. Litz wire contians many thin wire strands, individually insulated and twisted together to obtain low wire resistance. For Litz wire with N number of strands, American wire gauge (AWG) is used to calculate the cross sectional area of the wire and the wire (of particular gauge) resistance per length (ohm/cm) as demonstrated in [4-7]. The gauge number is increased in AWG to denote decreasing wire diameters.

6. Estimate leakage inductance:

The critical steps for HF transformer design are calculating the optimal flux density, core dimensions, winding dimensions, and leakage inductance. The leakage inductance is related to the power transfer and phase shift for the dual active bridge (DAB) and similar topologies. The winding and core arrangements are typically adjusted to obtain the required leakage inductance for the transformer. Also, it is desired to utilize the leakage inductance for many converters topologies as a resonant inductance, or for optimum power transfer. There are some methods to evaluate the transformer leakage inductance reported in [4-3, 4-5, 4-6]. Equation 4.6 is the formula used for the shell type core reffered to the transformer primary-side [4-6, 4-7, 4-10].

$$L_{lk} = \frac{1}{3}\ \mu_0 N_p^2\ MLT\ \frac{h}{w} \tag{4.6}$$

where μ_0 is the free space permeability constant ($4\pi * 10^{-7}$ H/m), MLT is the mean length of a turn, w is the windings width (the core window width), and h is the window height. In [4-10], different cores arrangments and orthogonal flux effects are analyzed. Reducing the shell core leakage inductance can be achieved by reducing the number of turns, using long narrow core, or utilizing interleaving windings. For a toroid core of an r radius, the leakage inductance is estimated by equation 4.7.

$$L_{lk} = \frac{1}{2}\ \mu_0 N_p^2\ MLT \tag{4.7}$$

This estimation equation is a modified formula developed to estimate the leakage inductance of the used toroid core transformer. It has verified the fabricated tarnsformer leakage inductance measured value which is very critical for the series resonant converter operation at the resonant frequency. If the desired leakage inductance is not obtained, the core and windings dimensions have to be modified to run another design iteration. The mean length of a turn (MLT) for a shell core (2 C-cores) is estimated as in [4-11] by equation 4.8.

$$MLT = 2(w + 2l)+0.8*l_w*(2+\pi) \tag{4.8}$$

where w is the core cross sectional width, l is the cross sectional thickness of the core, and l_w is the windings width for the C core.

However, MLT for toroid core is given by equation 4.9 [4-4].

$$MLT = 0.8*(OD + 2*H_t) \tag{4.9}$$

where OD is the toroidal core length, and H_t is the windings hight.

The magnetizing inductance of the designed transformer typically is very high, and can be estimated by equation 4.10 [4-5].

$$L_m = \mu_0 \mu_r N_p^2 \frac{A_c}{l_c} \tag{4.10}$$

where A_c is the core cross sectional area, and l_c is magnetic path mean length.

7. Calculate core and winding volumes: Equations 4.11 and 4.12 are the core and windings volumes related to the transformer area product [4-3, 4-6]:

$$V_c = k_c\ A_p^{3/4} \tag{4.11}$$

$$V_w = k_w\ A_p^{3/4} \tag{4.12}$$

$$V_T = V_c + V_w \tag{4.13}$$

where the dimensionless parameters are $k_c = 5.6$, $k_w = 10$ [4-3, 4-5, 4-6]. If the required volumes for the core and winding are not fulfilled, the area product should be updated by compromising the flux density.

8. **Core and winding losses:**

The transformer efficiency depends on the core and winding losses which are calculated by equations 4.14, 4.15, and 4.17. The improved general Steinmetz equation (iGSE) is used to calculate core losses per unit volume (in W/m^3) [4-5, 4-6]. The transformer efficiency is estimated by equation 4.18.

$$P_{core} = \frac{1}{T} \int_o^T k_1 \left|\frac{dB(t)}{dt}\right|^{\alpha} |\Delta B|^{\beta-\alpha} dt \tag{4.14}$$

$$k_1 = \frac{K_c}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^{\alpha} |\sin\theta|^{\beta-\alpha} d\theta} \tag{4.15}$$

Equation 4.16 is the approximation used for the coeffiecient k_1 [4-5]:

$$k_1 = \frac{K_c}{2^{\beta-1}\, \pi^{\alpha-1}\, (1.1044 + \frac{6.8244}{\alpha+1.354})} \tag{4.16}$$

where K_c is core Steinmetz constant or core loss density (shown in Table 4.1) [4-9].

$$P_{cu} = I_p^2 R_p + I_s^2 R_s \tag{4.17}$$

$$\eta = \frac{\text{Output Power}}{(\text{Output Power} + P_{core} + P_{cu})} \tag{4.18}$$

9. Temperature and isolation evaluation:

The transformer temperature rise must be within the acceptable limit as targeted in step 1 specifications, and the conductors distance is calculated by equation 4.19 to ensure the isolation level requirement [4-12].

$$d_i = \frac{V_i}{vE_i} \tag{4.19}$$

where V_i is the required isolated voltage, E_i is the isolation material dielectric strength, and v is safe margin parameter which accounts for non-uniformities of the electric field [4-12].

10. Optimum design for the desired sepecifications and appropriate cost, volume and efficiency compromise is eventially obtained. The matlab code for the flowchart shown in figure 4.1 was dveloped by Roderick [4-7]. The program code has been updated and applied for two diferent design examples which are presented in this chapter (power, voltage, core, wire, and frequency,… etc). All the associated equations for all the calculations have been reviewed and applied to yield the transformer specifications.

4.3 Transformer Design Examples

The literature for medium and high-frequency transformer design has been reviewed and investigated. Two diferent (core, frequency, rated power) design examples are demonstrated with their experimental testing measurements.

4.3.1 Design Example 1: (25 kHz, 5 kVA, 440 V/110 V Amorphous shell core)

Table 4.2 shows the obtained specifications for HF transformer example 1. Figure 4.5 shows the Metglas Amorphous AMCC – 63 core used in this design example.

Figure 4.5. Metglas Amorphous AMCC – 63 laminated core.

Table 4.2. Example 1 (25 kHz) transformer specifications.

Power	5 kVA
Input – output voltage	440 V – 110 V
Frequency	25 kHz
Efficiency	96 %
Core	Metglas Amorphous AMCC - 63
Wire	105/30 Served Litz wire
Number of turns	32 primary/ 8 secondary
Optimum flux density	0.19 T
Volume	683 cm^3
Leakage inductance	210 µH
Magnetizing inductance	30 mH

Amorphous Metal C-Core (AMCC–63) was selected as well as 105/30 served Litz wire after running Matlab program to obtain the winding and core arrangements and all transformer specifications. A 25 kHz transformer has been constructed for 5 kVA rating with amorphous AMCC–63 core and 0.21 mH leakage inductance (Table 4.2). It was also tested using a half-bridge inverter and it gave the expected output results. The gate drivers for the half bridge were controlled using the TMS320F28335 digital signal processor (DSP). This design has been done for shell type core as it is easier to estimate its leakage inductance, and also it is easily cooled as mentioned in the literature [4-10]. The bobbins for the shell core have not been utilized and 105/30 served Litz wire is chosen for the transformer windings.

An AWG 30 of 105 strands are used, and the diameter of AWG 30 is 0.254 mm. The primary and secondary wire areas have been calculated for the desired current density, and the desired wire radius for skin effect to calculate the total equivalent Litz wire size. Figure 4.6 demonstrates the fabricated 5 kVA, 440V/110V amorphous transformer which was built using

the aforementioned core and Litz wire. The primary and secondary winding resistances were measured and found as expected for the copper losses (R_p = 1.1 Ω, and R_s = 0.9 Ω).

Figure 4.6. The developed 25 kHz, 5 kVA, 440 V/110 V amorphous transformer.

4.3.1.1 Experimental Testing for the fabricated transformer of Example 1

Half-bridge inverter board was fabricated to test the constructed transformer. The TMS320F28335 DSP is used to generate the control signals for the half-bridge transistors gate drivers. The experimental test setup shown in Figure 4.7 is to measure the inverter output voltage. The gate drivers to control the switching devices are placed on the top of the board as depicted in Figure 4.7.

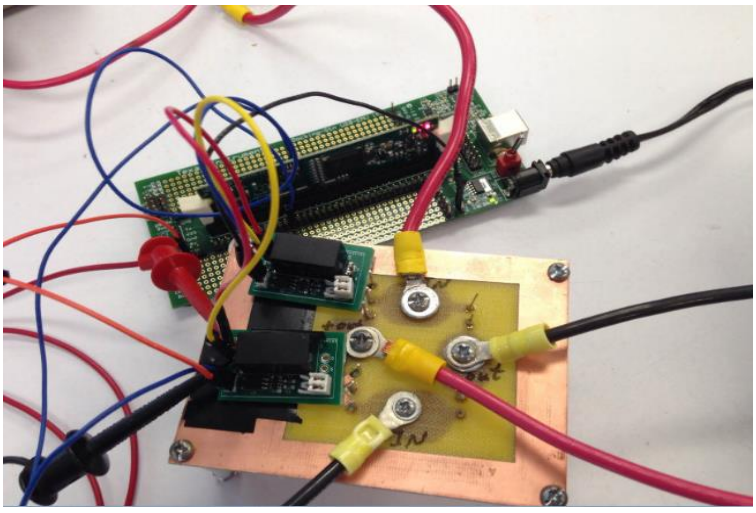

Figure 4.7. TMS320F28335 DSP to control the gate drivers of the half-bridge inverter.

The half-bridge inverter was built to obtain the required high frequency AC voltage. After making all the connections and using a 5 Ω resistor as a load at the transformer output, a dc power supply was increased gradually from 0 V to 40 V and the measurements are taken from the oscilloscope. Figure 4.8 shows the experimental setup to test the transformer using the DSP to control the gate drivers with PWM pulses of 25 kHz and 50% duty cycle. Figures 4.9 and 4.10 show the measured output voltage of the half bridge inverter for an input of 20 V, and 30 V, respectively.

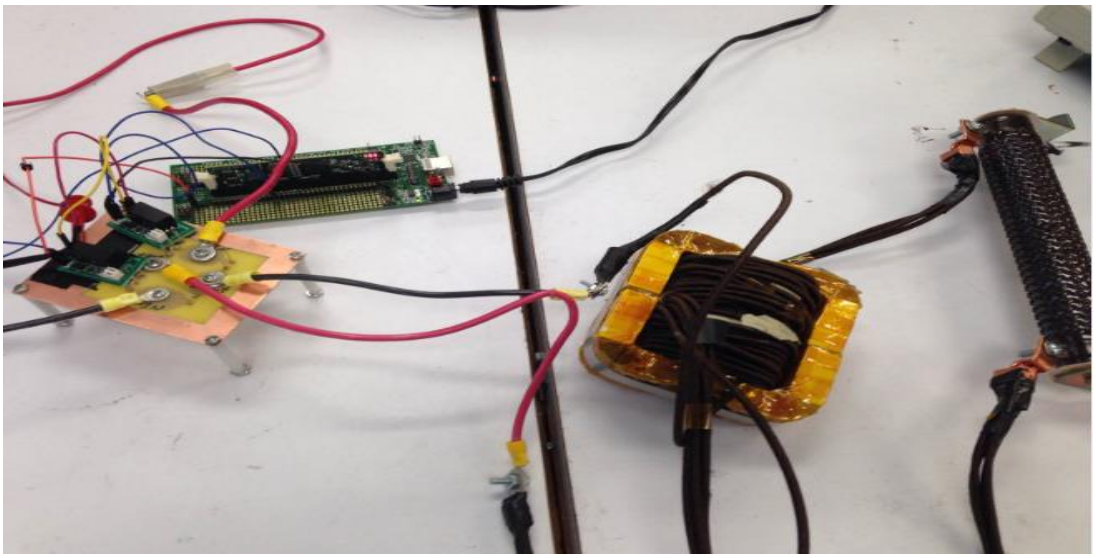

Figure 4.8. Half-bridge inverter and 25 kHz transformer testing setup.

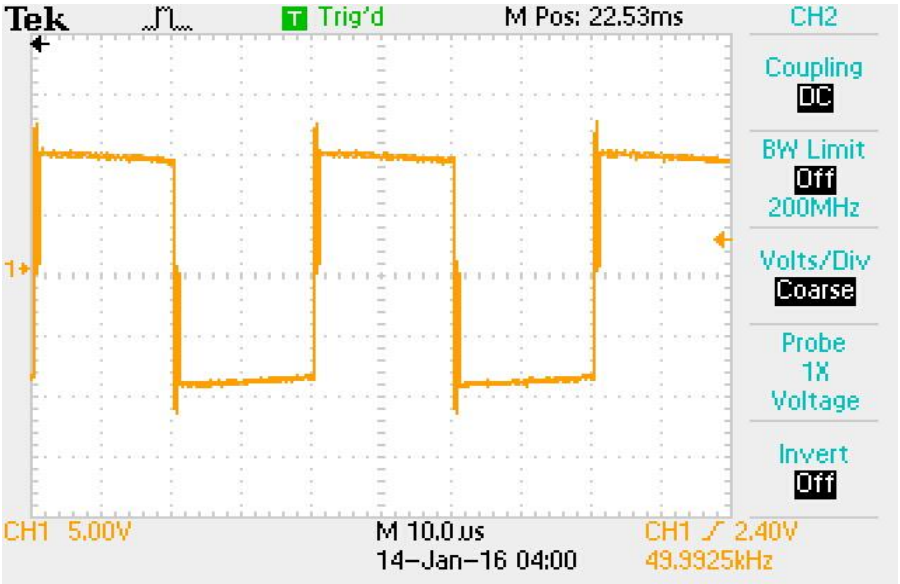

Figure 4.9. Transformer input voltage for V_{in} = 20 V.

Figure 4.10. Transformer input voltage for V_{in} = 30 V.

The applied input voltage was up to 46 V, and the secondary winding of the transformer was connected to 5 Ω resistor as a load. Figure 4.11 shows example 1 transformer output voltage for a DC input voltage of 20 V. Because the inverter output is the square pulse of +10 V and -10 V, then the transformer secondary output is a fourth of the primary input as the ratio of stepping the voltage down. The frequency is 25 kHz, as the time period is 40 µs. Finally, Figure 4.12 shows the transformer output AC voltage for a DC input of 46 V. It is obvious from the transformer measured waveforms that the 25 kHz output voltage have sloppy smooth transitions between the positive and negative values, and not rectangular as the input signals shown in Figures 4.9 and 4.10. That is because of the transformer non-ideal effects including the leakage inductance and losses.

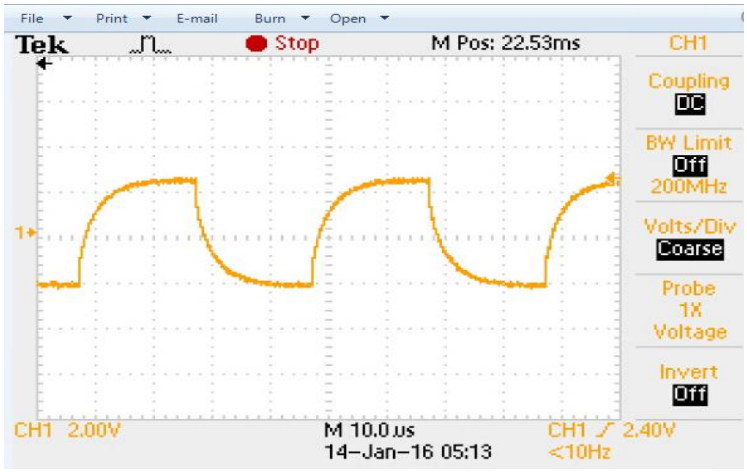

Figure 4.11. Example 1 transformer output voltage for V_{in} = 20 V.

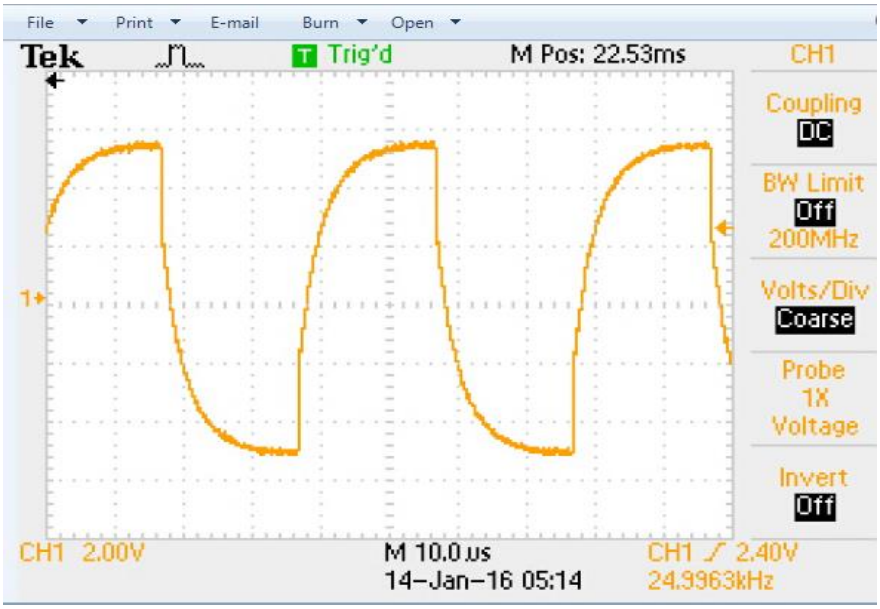

Figure 4.12. Example 1 transformer output voltage for V_{in} = 46 V.

4.3.2 Design Example 2: (100 kHz, 350 VA, 130V/117V, nanocrystalline toroid core)

The proposed topology specifications are the starting parameters for this 100 kHz transformer design (Example 2). The chosen core is the W376-04 nanocrystalline toroid core for higher efficiency since the core losses are higher for amorphous and ferrite materials at higher frequencies. Leakage inductance evaluation is a critical step which is affected by the transformer winding and core arrangements, and eventually determines the resonance inductance of the series resonant converter in the proposed isolated converter. Figure 4.13 shows the W376-04 nanocrystalline toroid core from VAC Magnetics, and its main dimensions.

Core dimensions are in cm.

A_{fe} = 0.57 cm^2.

l_{fe} = 7.85 cm.

m_{fe} = 32.9 g.

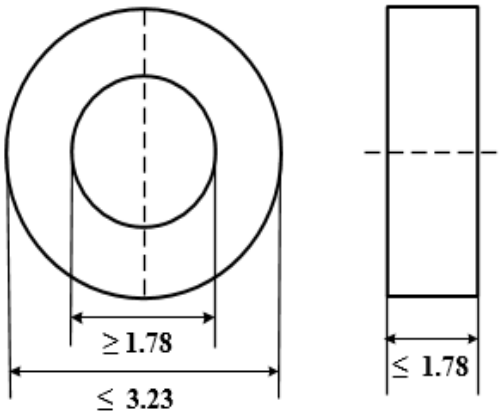

Figure 4.13. W376-04 nanocrystalline toroid core [4-13].

The completed 100 kHz transformer using the W376-04 nanocrystalline toroid core is shown in Figure 4.14. It has been designed according to the optimum specifications for the proposed GaN-based AC/DC converter as shown in Table 4.3.

Table 4.3. Example 2 (100 kHz) transformer specifications.

Power	350 VA
Input – output voltage	130 V – 117 V
Frequency	100 kHz
Efficiency	98.2 %
Core	Nanocrystalline Vitroperm W376-04
Wire	16/30 Served Litz wire
Number of turns	25 primary/ 22 secondary
Optimum flux density	0.16T
Volume	31.51 cm^3
Total Leakage inductance	50.31 µH
Magnetizing inductance	18.7 mH

Figure 4.14. The fabricated 100 kHz nanocrystalline toroid transformer.

The resistances and inductances for each of the windings of the 100 kHz fabricated transformer are measured by an RLC meter, they are as follows:

Primary side:

L_m = 1.395 mH.

L_{lk} = 25.48 µH.

R_c = 135.7 kΩ (ac)- 170 mΩ (dc).

R_s = 62 Ω (ac)- 130 mΩ (dc).

Secondary side:

L_m = 1.13 mH.

L_{lk} = 20.15 µH.

R_c = 95.75 kΩ (ac)- 170 mΩ (dc).

R_s = 51 Ω (ac)- 110 mΩ (dc).

Therefore, the transformer total leakage reactance is calculated by 4.20 [4-5].

$$X_{eq} = X_{l1} + n^2 X_{l2} \tag{4.20}$$

Therefore, the total leakage inductance of this transformer is calculated as:

$$L_{lk\_eq} = 25.48 + 1.11^2 (20.15) = 50.31\ \mu H. \tag{4.21}$$

Tests are performed on the example 2 transformer (100 kHz Nanocrystalline toroid core) and Figure 4.15 shows its primary and secondary voltages, and primary current for the fabricated GaN converter prototype. The primary current is increasing when the voltages are positive, while it is decreasing when the voltages are negative. The proposed GaN isolated AC/DC converter is illustrated in Chapter 3. It includes a totem-pole power-factor-correction (TP-PFC), a half-bridge series resonant converter (SRC), and a current doubler rectifier (CDR) at the secondary of the high-frequency (100 kHz) transformer. Chapter 6 demonstrates the experimental converter prototype and its results.

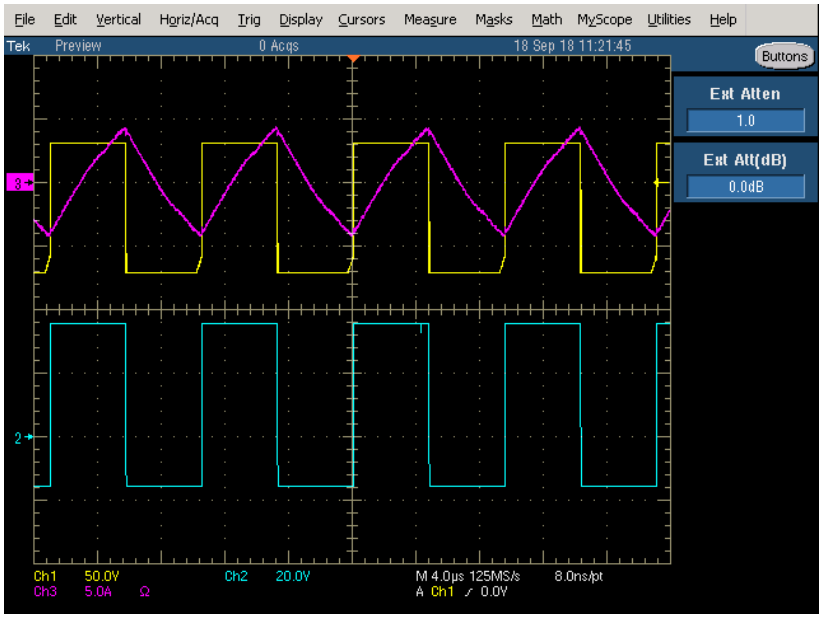

Figure 4.15. 100 kHz transformer voltages (V_{T1}, V_{T2}), and primary current.

4.4 Conclusion

The literature and main steps to design medium and high frequency transformer are reviewed and explained, and MATLAB code was applied to obtain the specifications for two different transformers design examples. Amorphous shell type (25 kHz, 5 kVA, 440/110V) and nanocrystalline toroid core (100 kHz, 350 VA, 130/117V) are used as the material cores in the two design examples. Served Litz wires were selected for the transformers windings. Nanocrystalline core yields higher efficiency than amorphous core at 100 kHz or higher frequency, while at 25 kHz their efficiencies are close but the amorphous core is much cheaper than nanocrystalline core for the same power ratings. The high-frequency nanocrystalline toroid transformer is designed and fabricated to satisfy the performance specifications of the investigated AC/DC converter. More importantly, a new equation is developed to determine the toroid transformer leakage inductance. The measured value of the fabricated nanocrystalline transformer total leakage inductance is 50.31 µH, which proves the new equation developed in this work. The fabrication for the two transformers and their main operational features are presented and discussed.

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CHAPTER 5

TMS320F28335 DIGITAL SIGNAL PROCESSOR PROGRAMMING

5.1 Introduction

This chapter describes how to program the Texas Instruments™ (TI) TMS320F28335 digital signal processor (DSP) through code composer studio (CCS) version 6 and MATLAB Simulink embedded Coder. First, it shows how to setup Simulink and Embedded Coder and produce code to program the TMS320F28335 and variant of TI's C2000 DSPs. It describes how to interact between MATLAB and CCS V6 and provides an explanation of the vital steps and settings needed to program the DSP. Basic functions such as pulse width modulation, analog digital conversion, and proportional-integral controllers are explained. Finally, the control model for the proposed AC/DC converter topology is developed.

A TMS320F28335 DSP is shown in Figure 5.1. It is a C2000 class, 32-bit, floating-point microcontroller from Texas Instruments™ designed for real-time control with a system clock of up to 150 MHz to achieve a fast processing speed. The TMS320F28335 has up to 18 pulse width modulation (PWM) outputs, including 12 enhanced PWM outputs which allow easy initialization and implementation of PWM schemes. As such, TMS320F28335 applications are used for motor control, renewable energy, and power electronic converters.

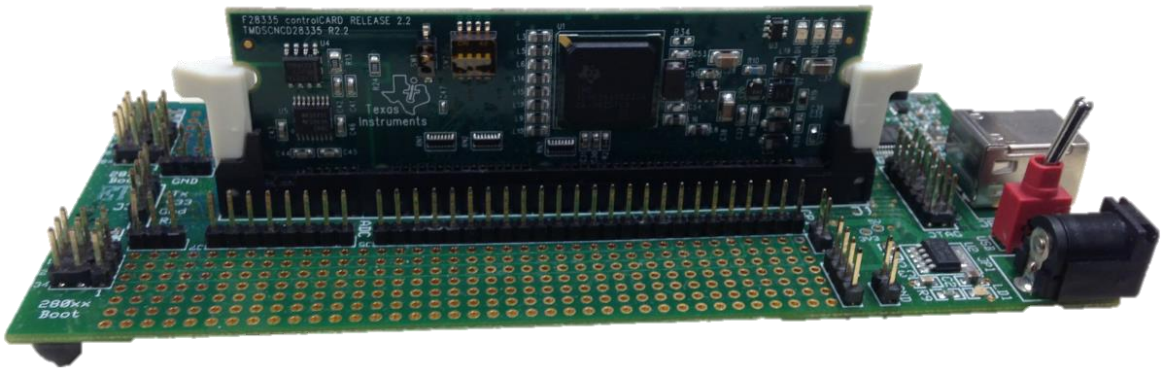

Figure 5.1. TMS320F28335 DSP with the USB docking station.

In addition to a 12-bit analog-to-digital (ADC) converter, with up to 16 ADC input channels, which provides real-time measurement and control. All pins of the TMS320F28335 DSP have a 3.3-V input/output voltage. Generally, it is an appropriate microcontroller to provide maximum control for many power conversion systems [5-1]. The TI TMS320F28335 DSP has many code examples available through TI's website and support community. The TI's website resources include schematics, reference manuals, software, and other development tools. ControlSUITE is an important software developed for TI's C2000 class of microcontrollers and is free downloadable. This software includes many example projects and file libraries which can be utilized to develop a new project [5-1]. Figures 5.2, and 5.3 present the CCS home screen after building the project, and after running it respectively. Entering *CCS Debug* mode means to download the executable output file to the DSP. This project is the program *Example_2833xEPwmTimerInt.c* which is used in [5-1], and downloaded from TI website. Designing closed-loop feedback multi PWM control schemes is much harder and more time consuming in CCS than in MATLAB Simulink Embedded Coder for Texas Instruments™ TMS320F28335 Digital Signal Processor (DSP).

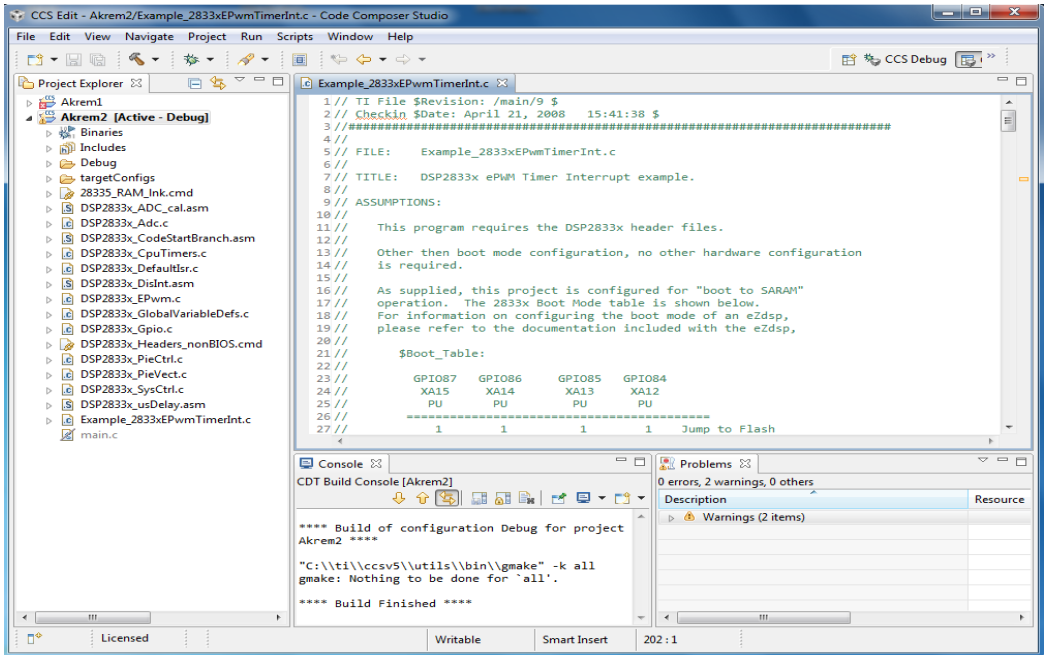

Figure 5.2. CCS home screen after building the project.

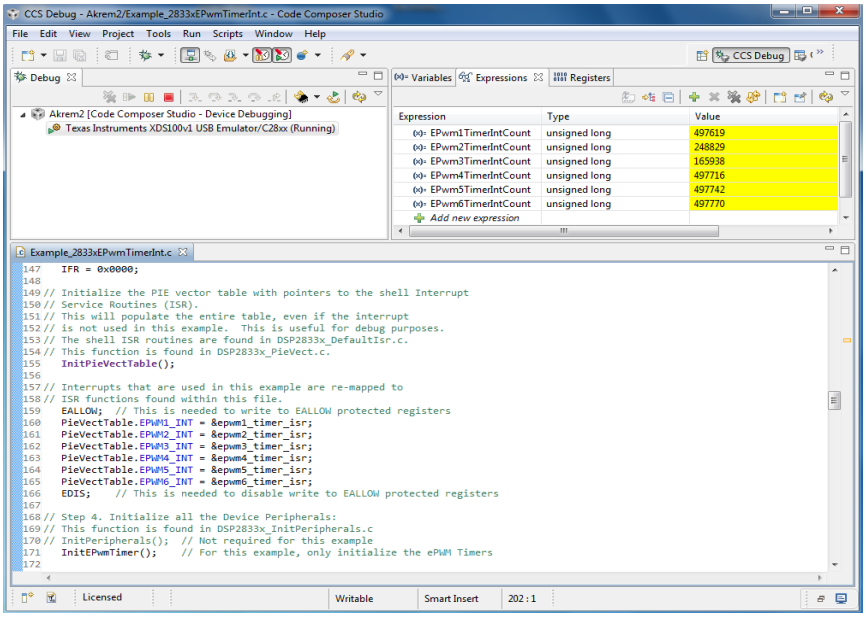

Figure 5.3. CCS debug home screen.

The TMS320F28335 DSP is a cheaper controller which proved excellent convergence, and real time control for significant reduction of output ripple [5-2]. The code is automatically generated using the embedded coder, and so time for programming and control implementation is reduced. MATLAB Simulink for DSP controller is highly valuable as model design, simulation, code generation, debugging and running can be accomplished for control algorithm [5-3]. MATLAB Simulink environment is especially recommended for control algorithm implementation into micro controller [5-4][5-5]. This chapter provides a simple and clear tutorial to learn how to program the TMS320F28335 DSP from Texas Instruments™ (TI) through CCS and MATLAB Simulink Embedded Coder. Using Simulink code generation is more effective than writing line-by-line code in CCS which takes a long time for users to program the DSP [5-6][5-7]. To begin, the Embedded Coder, MATLAB Coder, and Simulink Coder toolboxes must be installed on the PC. Embedded coder sits on top of MATLAB and Simulink coder; it allows the user to add device specific code (ADC's, DAC's, CAN, etc.) to what it produces by the respective coders. An easy way to check the toolboxes installed on MATLAB version is by entering the "ver" command into the command window [5-7] as shown in Figure 5.4.

```
Datafeed Toolbox                                Version 5.5          (R2017a)
Econometrics Toolbox                            Version 4.0          (R2017a)
Embedded Coder                                  Version 6.12         (R2017a)
Financial Instruments Toolbox                   Version 2.5          (R2017a)
Financial Toolbox                               Version 5.9          (R2017a)
Fixed-Point Designer                            Version 5.4          (R2017a)
Fuzzy Logic Toolbox                             Version 2.2.25       (R2017a)
Global Optimization Toolbox                     Version 3.4.2        (R2017a)
HDL Coder                                       Version 3.10         (R2017a)
HDL Verifier                                    Version 5.2          (R2017a)
Image Acquisition Toolbox                       Version 5.2          (R2017a)
Image Processing Toolbox                        Version 10.0         (R2017a)
Instrument Control Toolbox                      Version 3.11         (R2017a)
MATLAB Coder                                    Version 3.3          (R2017a)
MATLAB Compiler                                 Version 6.4          (R2017a)
MATLAB Compiler SDK                             Version 6.3.1        (R2017a)
Mapping Toolbox                                 Version 4.5          (R2017a)
Neural Network Toolbox                          Version 10.0         (R2017a)
Optimization Toolbox                            Version 7.6          (R2017a)
Parallel Computing Toolbox                      Version 6.10         (R2017a)
Partial Differential Equation Toolbox           Version 2.4          (R2017a)
RF Blockset                                     Version 6.0          (R2017a)
RF Blockset                                     Version 6.0          (R2017a)
RF Toolbox                                      Version 3.2          (R2017a)
RT-LAB                                          Version v11.2.1.100     (R2017a.x)
RT-XSG                                          Version v2.3.6.104sgUnsupported     (Rx.x)
Robotics System Toolbox                         Version 1.4          (R2017a)
Robust Control Toolbox                          Version 6.3          (R2017a)
Signal Processing Toolbox                       Version 7.4          (R2017a)
SimBiology                                      Version 5.6          (R2017a)
SimEvents                                       Version 5.2          (R2017a)
Simscape                                        Version 4.2          (R2017a)
Simscape Driveline                              Version 2.12         (R2017a)
Simscape Electronics                            Version 2.11         (R2017a)
Simscape Fluids                                 Version 2.2          (R2017a)
Simscape Multibody                              Version 5.0          (R2017a)
Simscape Power Systems                          Version 6.7          (R2017a)
Simulink Coder                                  Version 8.12         (R2017a)
Simulink Control Design                         Version 4.5          (R2017a)
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Figure 5.4. MATLAB installed toolboxes.

5.2 CCSV6 Target Configuration

First, Code Composer Studio (CCS) version 6 must be installed. If an older version of CCS was installed, it should be upgraded to CCS version 6 which is recently supported in Simulink for code generation. Embedded Coder (EC) works for previous versions but they are no longer supported by Texas Instruments. For setting up xMakefile in Simulink which tells EC where the CCS 6 compiler is installed among other programs. So MATLAB can call the command lines provided by CCS 6, and where MATLAB can find the compiler needed to create the makefile code. However, “xmakefilesetup” command in MATLAB is no longer needed because of the Embedded Coder Support package for TI C2000 Processors which permits the settings for model configuration parameters easily. Typing “supportPackageInstaller” command will launch the Support Package Installer Graphical User Interface in MATLAB.

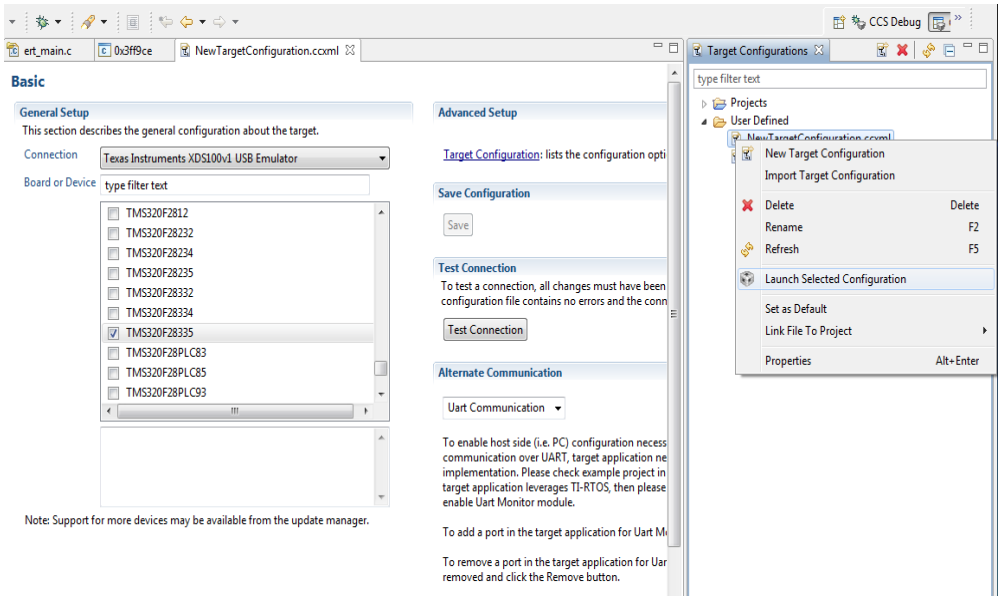

Figure 5.5. Launch new target configuration.

From the connection drop down box “Texas Instruments XDS100v1 USB Emulator” and “TMS320F28335” board or device must be selected. CCS 5 allows to test the target configuration right after it has been saved. Then for the New Target Configuration Launch Selected Configuration is clicked as shown in Figure 5.5. Then the debugger is brought up, you can right click on the board and click connect target. When the contents of the disassembly pane are displayed as in Figure 5.6, there is no problem with the connection to the DSP board. So CCS is ready to interact with MATLAB Simulink for TMS320F28335.

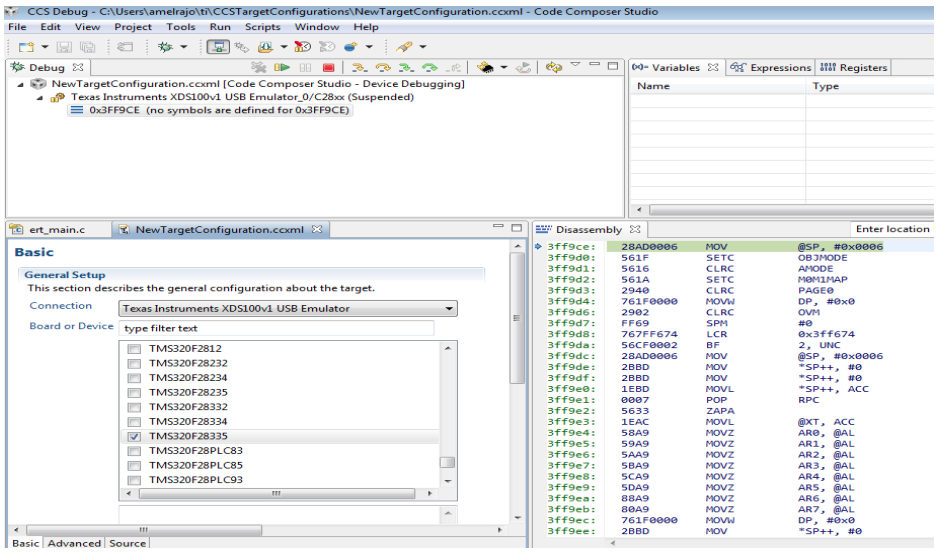

Figure 5.6. Debugged target configuration.

5.3 Setup of xMakefile for CCS v5

Type “xmakefilesetup” into MATLAB command line and after a few moments the configuration window should open up as in depicted Figure 5.7. Deselect the “Display operation configurations only” option and select “ticcs_c2000_ccsv5” option from the configuration dropdown menu. Then click Apply to change the tool directories as shown in Figure 5.8, you need to browse all CCS installation, Code generation tools, and DSP/BIOS installation folders to be entered correctly. The compiler directory should be incorrect when using CCS 5, so click on the new button to the right where you will be prompted to for a new configuration name. After it is named (clone), all of the options should be available to fill out the needed information.

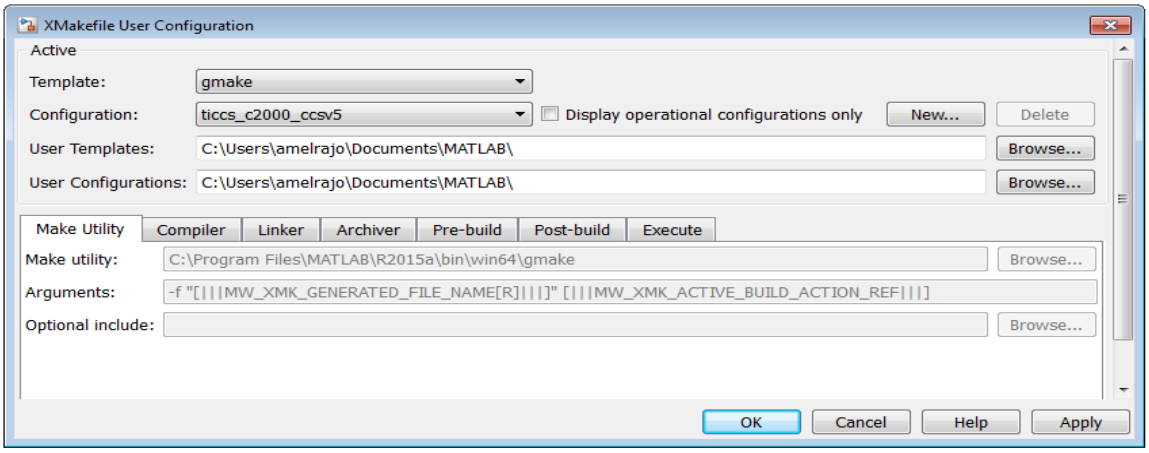

Figure 5.7. xMakefile configuration.

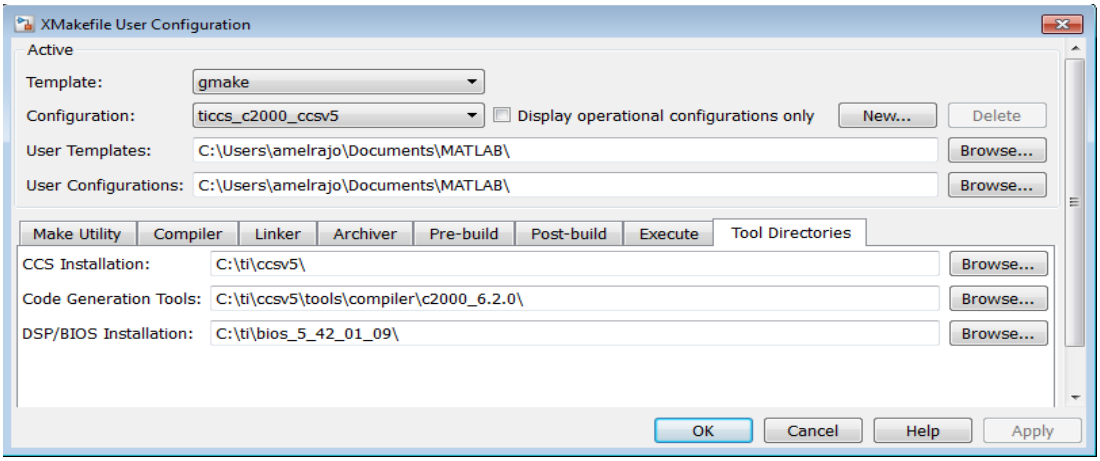

Figure 5.8. xMakefile configuration tool directories.

Select the compiler tab and browse to the CCS 5 compiler directory. It is located at "C:\ti\ccsv5\tools\compiler\c2000_6.1.3\bin\cl2000". Similarly, select the linker tab and browse to "C:\ti\ccsv5\tools\compiler\c2000_6.1.3\bin\cl2000". Finally setup the archiver tab so that it's pointed to the "C:\ti\ccsv5\tools\compiler\c2000_6.1.3\bin\ar2000" directory. Pre-build and Post-build should be empty as the defaults are for both tool and "Arguments". Also, "Execute" should be kept as the default. Figure 5.9 shows the compiler tab and its directory.

With the above mentioned setup, building in Simulink now can be started. The help files for all the blocks are very useful, and references [5-8, 5-9, 5-10] provide some links for further information. Then type this command "checkEnvSetup('ccsv5','f28335','check')" in MATLAB to make sure that the tools are installed properly as shown in Figure 5.10. For F28335, header files are not needed but it is needed to install Flash APIs from TI ControlSUITE webpage. The compiler cab be checked by typing in the command window: mex –setup, or mex.getCompilerConfigurations. Then an environment variable for "Flash APIs" has to be created on the computer. Go to "Advanced system settings" and click environment variables, the prompt will show up as presented in figure 5.11. Then restart MATLAB, so it will be able to detect this flash APIs installed. Then the system is ready to create a Simulink model to blink an LED.

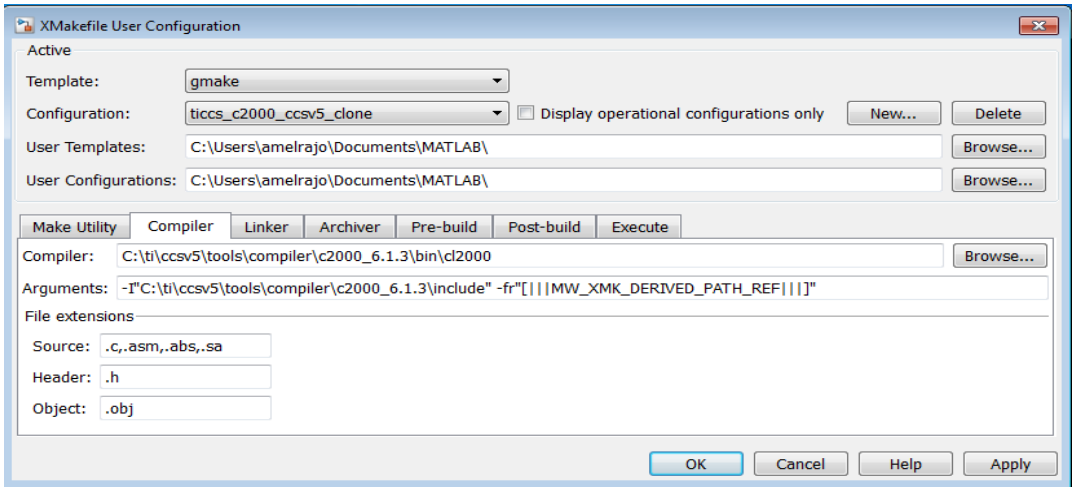

Figure 5.9. xMakefile configuration clone compiler.

```
>> checkEnvSetup('ccsv5','f28335','check')

1. CCSv5 (Code Composer Studio)
   Your version    : 6.1.0
   Required version: 5.0 or later
   Required for    : Code Generation
   TI_DIR="C:\ti\ccsv6"

2. CGT (Texas Instruments C2000 Code Generation Tools)
   Your version    : 5.12.3
   Required version: 5.2.1 to 6.0.2
   Required for    : Code generation
   C2000_CGT_INSTALLDIR="C:\ti\ccsv6\tools\compiler\c2000_15.12.3.LTS"

3. DSP/BIOS (Real Time Operating System)
   Your version    : 5.41.11.38
   Required version: 5.33.05 to 5.41.11.38
   Required for    : Code generation
   CCSV5_DSPBIOS_INSTALLDIR="C:\ti\bios_5_41_11_38"

4. XDC Tools (eXpress DSP Components)
   Your version    :
   Required version: 3.16.02.32 or later
   Required for    : Code generation

5. Flash Tools (TMS320C28335 Flash APIs)
   Your version    : 2.10
   Required version: 2.10
   Required for    : Flash Programming
   FLASH_28335_API_INSTALLDIR="C:\ti\controlSUITE\libs\utilities\flash_api\2833x\28335\v210"
```

Figure 5.10. MATLAB checkEnvSetup command for F28335 DSP.

5.4 Embedded Coder Support Package for TI C2000 Processors

Open up a new file and go to the library browser and open up the following library tree: Embedded Coder > Embedded Targets. Within that library there are many blocks for TI C2000 processors as shown in Figure 5.12. Embedded Coder Support package for TI C2000 Processors has to be installed for MATLAB 2015a, and 2017a. But for MATLAB 2011b, and 2013a versions, the library already exists. Then the desired C2833x processor can be chosen for the DSP control card under consideration. There is no block called target Preferences in the MATLAB 2011b version, but instead we will initialize “Configuration Parameters” by clicking on the Simulation menu then model configuration parameters. The window in Figure 5.13 will show up to change code generation parameters. The default solver is fixed step type and discrete.

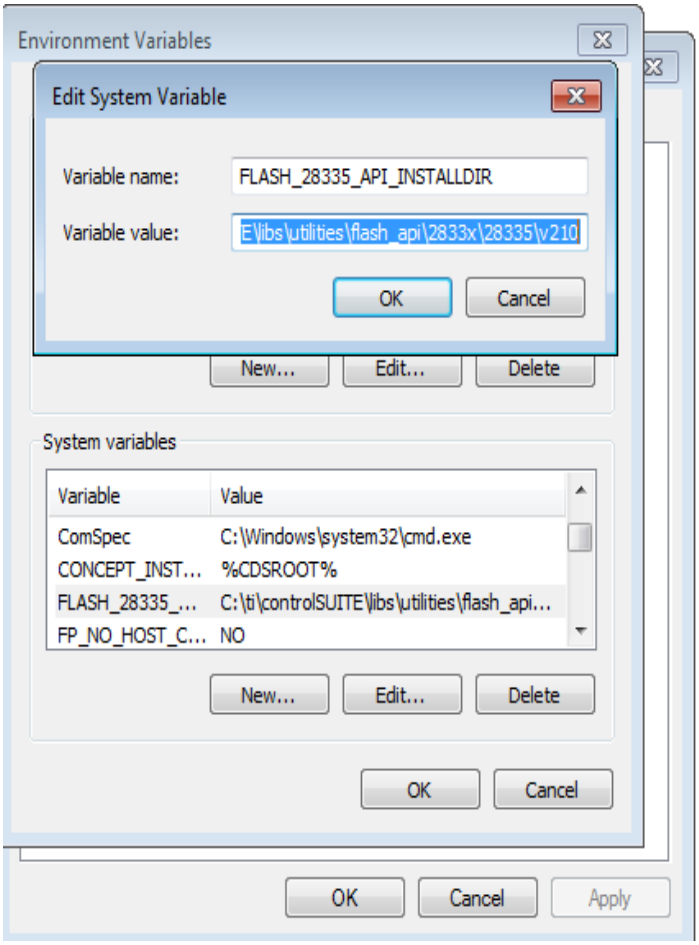

Figure 5.11. Flash APIs environment variable.

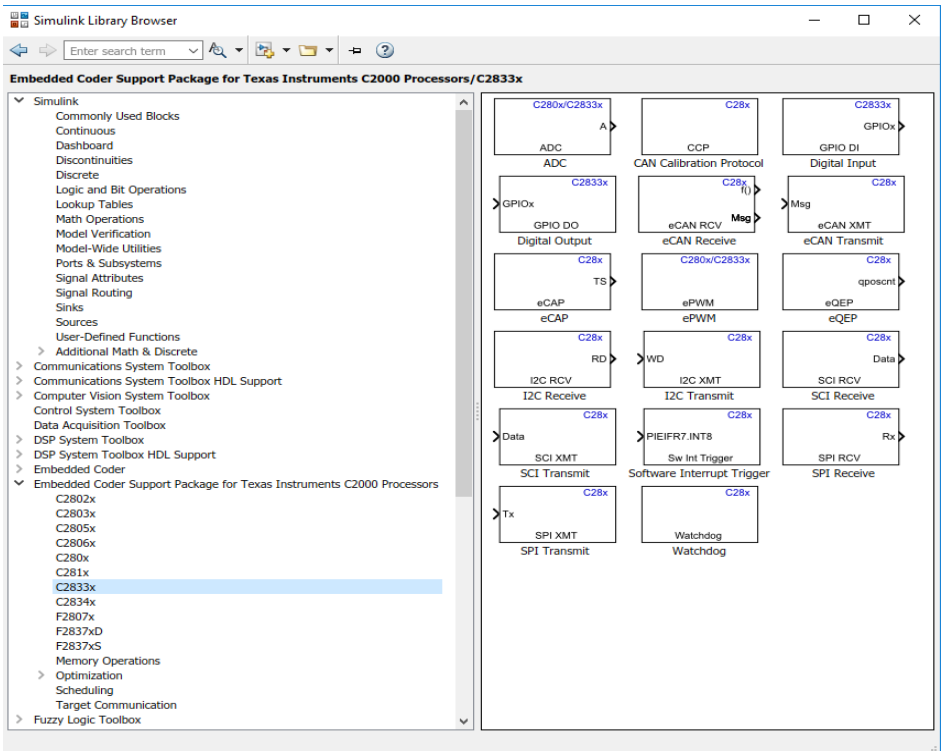

Figure 5.12. Embedded coder support package.

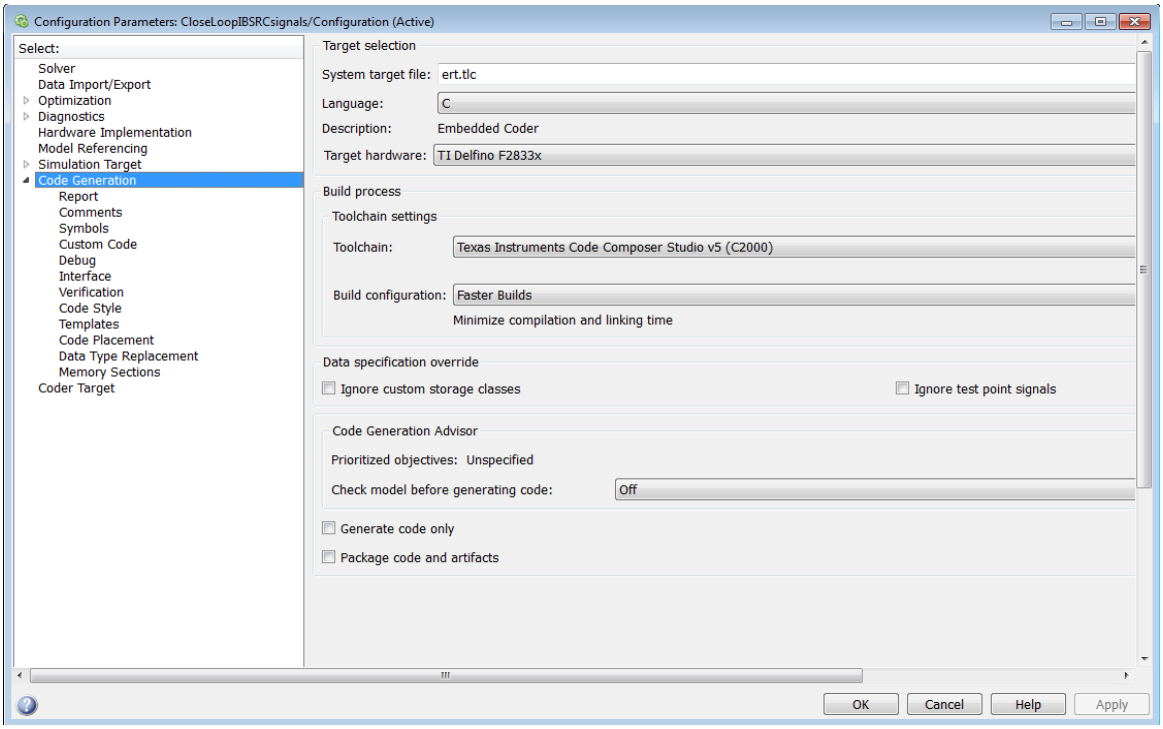

Figure 5.13. Code generation parameters configuration.

5.5 Flash Memory Programming (Stand-Alone Mode)

Choosing to work on RAM programming mode requires to set the configuration parameters to make the system target file as either “ert.tlc” or “idelink_ert.tlc” on the code generation page. For stand-alone mode, the program will be saved in the flash memory of the DSP, so it will not be erased when the DSP control card is unplugged from the computer. Check boot from flash option in configuration parameters window as shown in Figure 5.14. This setting in “Model Configuration Parameters” window tells EC what sort of DSP is being programmed so that it initializes the right peripherals, uses the correct operation frequency, knows how much memory is available, etc. Open the configuration parameters and ensure that the solver is set to fixed-step and discrete, the fixed-step size should remain auto. The hardware implementation page should show Texas Instruments, C2000, and Little Endian [5-7][5-8][5-9]. The code can be generated by clicking “Deploy to Hardware” (build model) icon. It will build a dot out file which is a downloadable program file in CCSV6. MATLAB will build the model and put everything into an .out file which you will load onto the DSP using CCS.

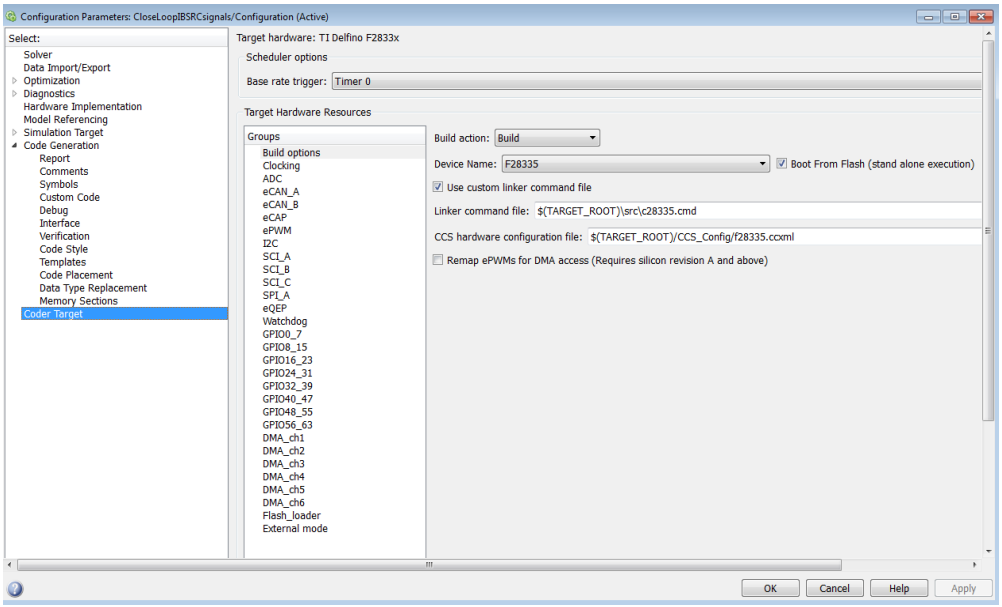

Figure 5.14. Stand-alone execution configuration parameters.

This .out file is placed in MATLAB current folder directory called Name_of_model_file_ticcs\CustomMW\Name_of_model_file.out. For a simple example, the model file is called “PI_Pulses”. Before loading the program, open up the debug drop down menu (The arrow next to the bug) and select debug configurations. Make sure to see the target and F28335 Flash settings as in Figure 5.15 for the flash mode operation.

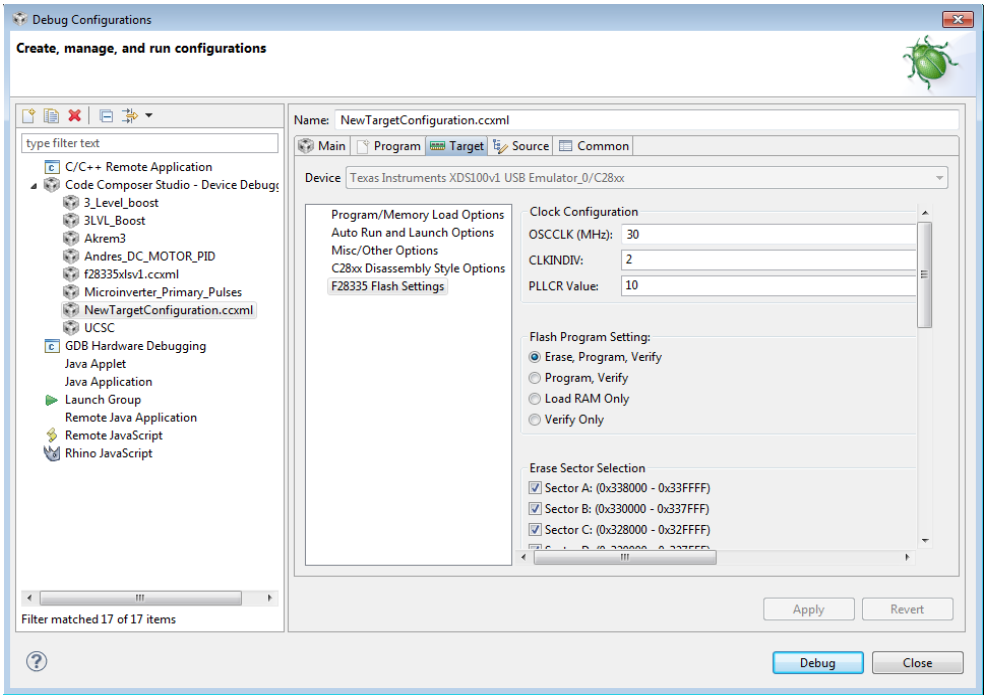

Figure 5.15. CCS debug configurations.

5.6 Debug Configurations and Code Running

Once you open CCS, you can select the configuration from the debug dropdown menu and CCS will automatically connect to the DSP and load the .out file for that project as shown in Figure 5.16. You can check code generation report after loading the model to see the comments and the highlighted hyperlinks for specific blocks in the Simulink model.

Finally in the target tab click on “auto run and launch options”, then select “connect to target” on debugger startup. After that is done, click debug at the bottom and CCS should take it from there. A new configuration for each one of the projects has to be setup, because when opening CCS the configuration can be selected from the debug dropdown menu, and CCS will automatically connect to the DSP and load the .out file for that project.

A TMS320F28335DSP board is shown in Figure 5.17 with the blinking GPIO34 LED after running the program. Since this programming was done on the DSP flash memory, the USB switch can be turned ON and OFF to see that the program is still working and has not been erased from the RAM by turning the power off.

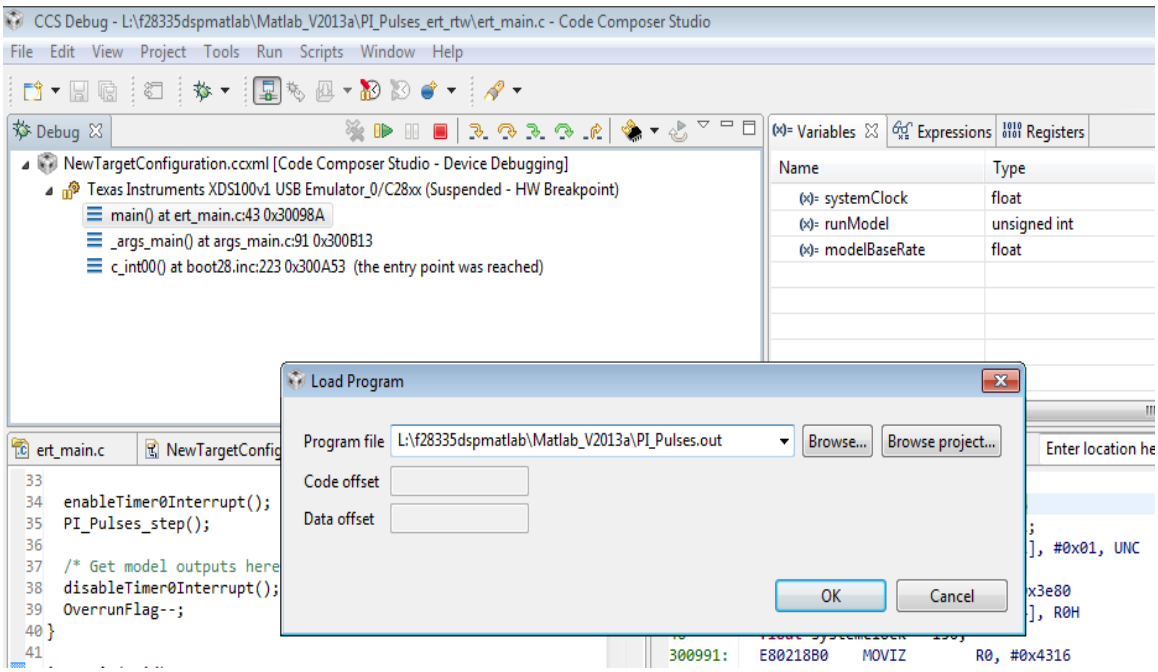

Figure 5.16. Loading the .out file for the project.

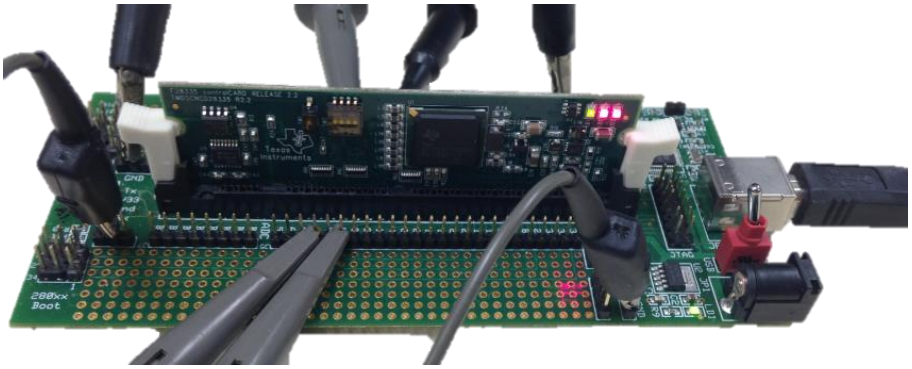

Fig 5.17. TMS320F28335 DSP board.

5.7 ePWM, ADC, GPIO, and PI Blocks

Figure 5.18 shows ePWM block parameters to generate two complementary PWM signals with a frequency of 20 kHz and duty cycle of 0.5. For frequency of 40 kHz, the timer period would be 1875. But for up counting mode it would be 3750. The duty cycle is depending on the CMPA value and the counting mode specified in ePWM block of Figure 5.18. Here it is up counting mode so D= 0.5 since 1875/3750 = 0.5. As can be noticed, the frequency and duty cycle can be specified as input ports or via dialog. Under the General tap, the timer period can be specified and it is calculated as by equation 5.2.

There are several options (Do nothing, Clear, Set, and Toggle) that can be chosen. As can be seen from Figure 5.18, when counter=CMPA on up-count (CAU) is "Set", and when counter=CMPA on down-count (CAD) is "Clear". Also counting mode can be chosen (Up, Down, or Up-Down). This is illustrated in the reference [5-1] and shown in Figure 5.19 for ePWM output signal generation. Set the period of the PWM waveform in clock cycles or in seconds, as determined by the Timer period unit's parameter. The term *clock cycles* refers to the Time-base Clock on the processor. In this simple example, the timer period equals 3750 with the "Up-Down" counting mode. So the frequency is set to 20 kHz as the time based clock is calculated by equation 5.1.

$$TBCLK = \frac{SYSCLK}{HSPCLKDIV * CLKDIV} \tag{5.1}$$

where, *SYSCLK* is the system clock speed set to 150 MHz, which is the maximum clock speed of the TMS320F28335 as specified in the CPU clock. HSPCLKDIV is the high speed time based clock pre-scale, and CLKDIV is the time based clock pre-scale. For Up-Down counting mode:

$$\text{Timer period} = 150\ \text{MHz} / (2 * 20\ \text{kHz}) = 3750 \tag{5.2}$$

For frequency of 40 kHz, the timer period would be 1875. But for up counting mode it would be 3750.

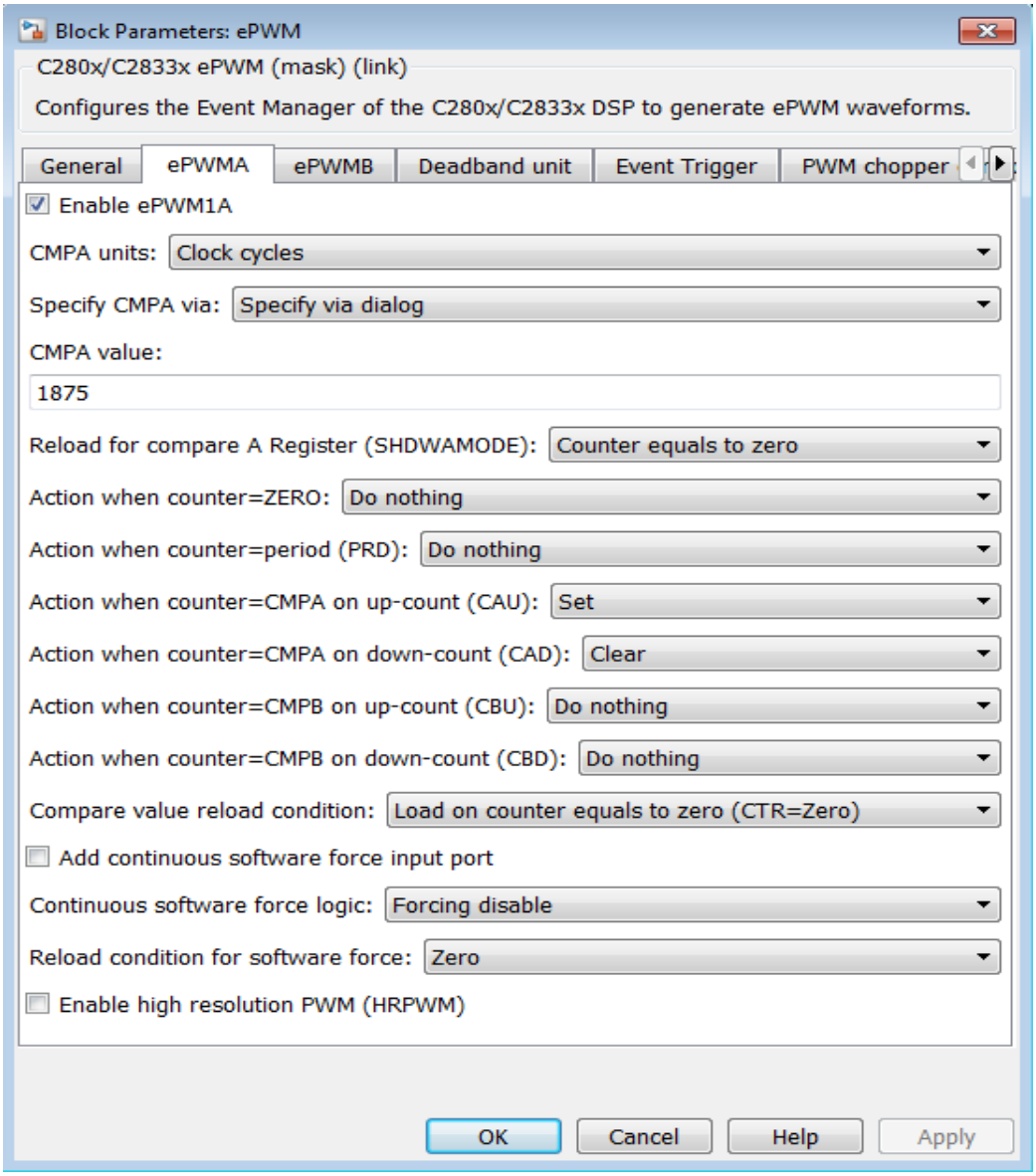

Figure 5.18. ePWM block parameters.

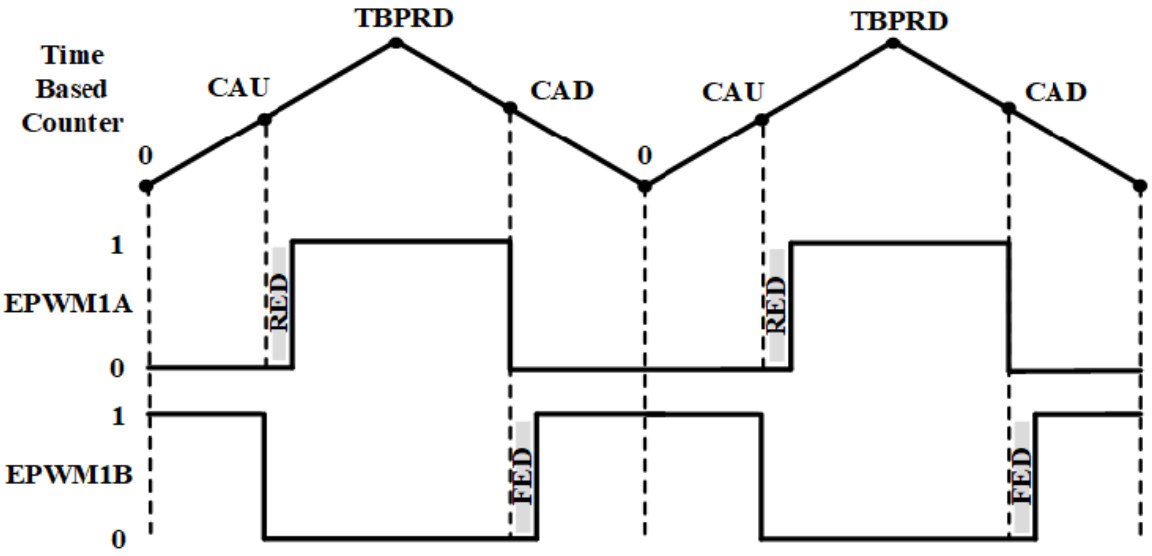

Figure 5.19. ePWM signal generation.

For compliment ePWMA and ePWMB, the “Deadband” polarity is chosen as either AHC or ALC as shown in Figure 5.20.

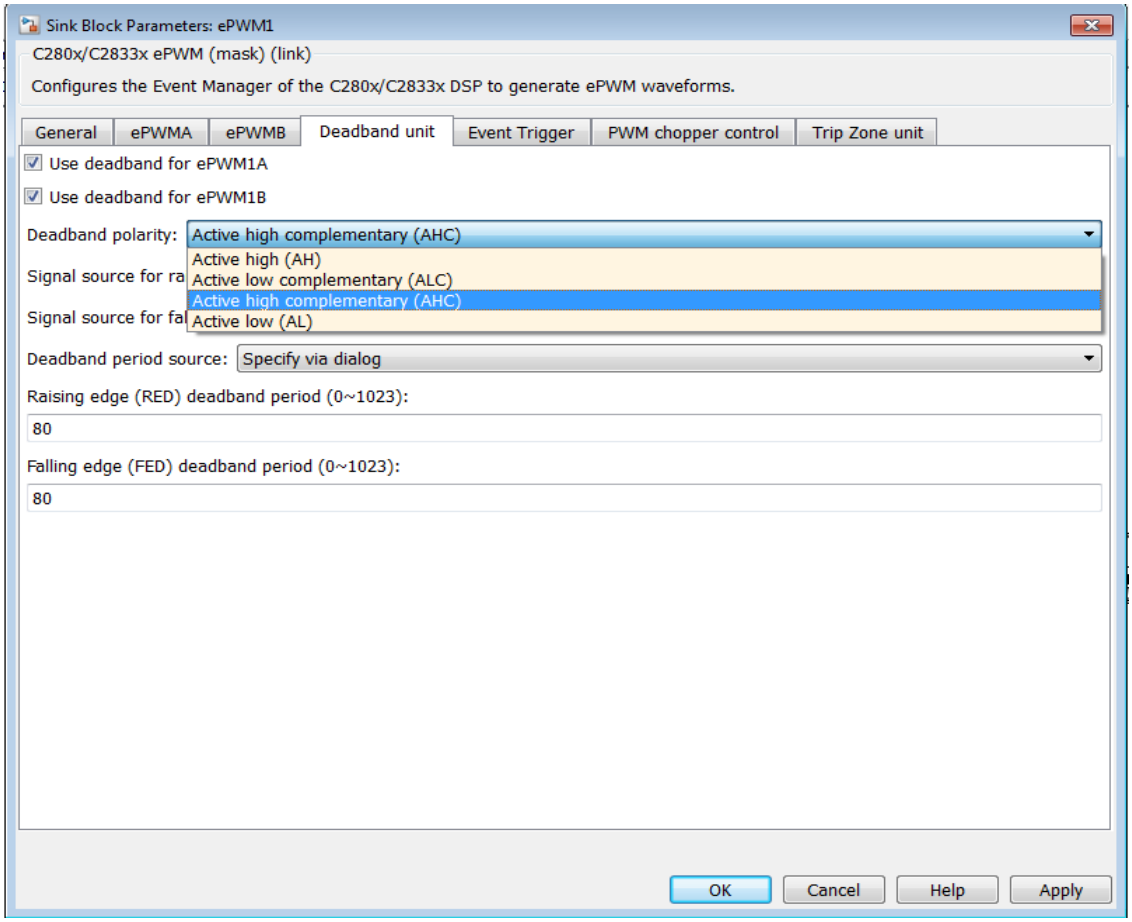

Figure 5.20. ePWMA and ePWMB deadband.

Figure 5.21 shows two synchronized enhanced pulse width modulator (ePWM) blocks using the same frequency and duty cycle as inputs. The measured pulses for the two ePWM outputs are shown in Figure 5.22 as synchronized with a phase shift of TBPHS = 750 (number of cycles for the time period). Notice that these two ePWM outputs are 180 degree shifted, the switching frequency is 100 kHz, and each ePWM has two complementary signals. The duty cycles are 0.48 (=720/(2*750)) and 0.46 (=690/(2*750)) for channel 1 (ePWM1A) and channel 3 (ePWM2A), respectively.

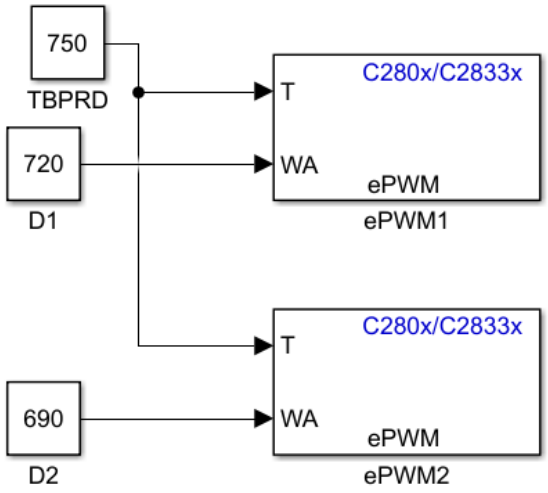

Figure 5.21. Synchronized two ePWM blocks.

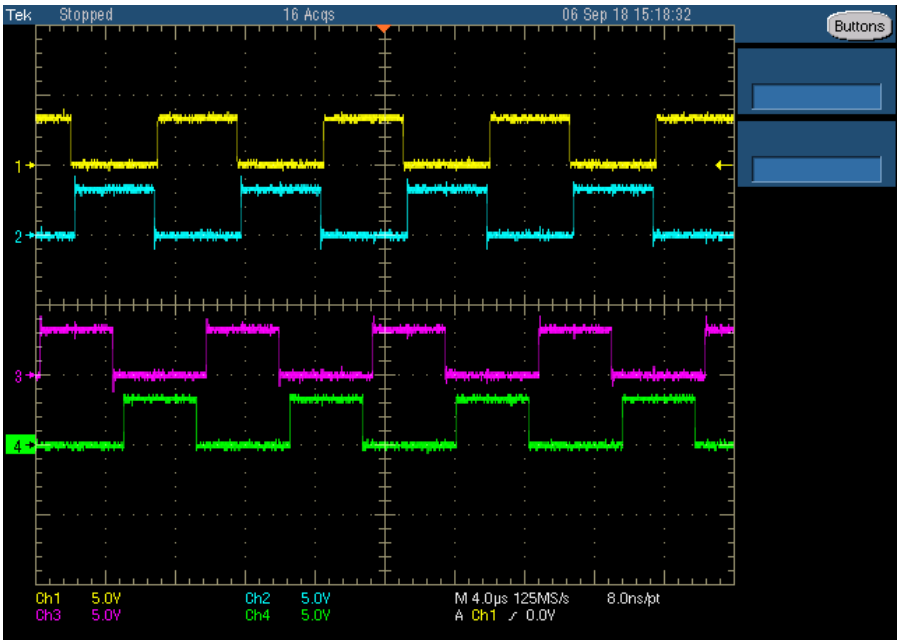

Figure 5.22. Synchronized ePWM pulses at 100 kHz.

Figure 5.23 presents the parameters for the two ePWM blocks used in Figure 5.21 model. It should be noted that the counting mode is Up-Down, so for a timer period of 1500 a phase shift of 1500 presents a 50% duty cycle. Also, notice that ePWM1A is set when counter equals zero and cleared when counter equals CMPA as shown below. The synchronization action is set as needed. The TMS320F28335 DSP has up to 18 PWM outputs which is adequate to control many three phase power converters. Twelve of these outputs are ePWM modules which are shown in Table 5.1.

Figure 5.24 shows a simple example to use the analog digital converter (ADC) block to perform analog-to-digital conversion of signals connected to the selected ADC input pins. The output of the ADC is a vector of 16 values. The output values are in the range 0 to 4095 because the ADC is a 12-bit converter, the input channel is ADCINA0. Notice in Figure 5.25 that the option (Post interrupt at the end of conversion) has been unchecked, and the sample time is equal to the time period of the ePWM output pulse (f=20 kHz). When this simple model is built, and uploaded to the DSP board, the power supply DC voltage is connected to the pin ADCINA0, and the negative to the ground point.

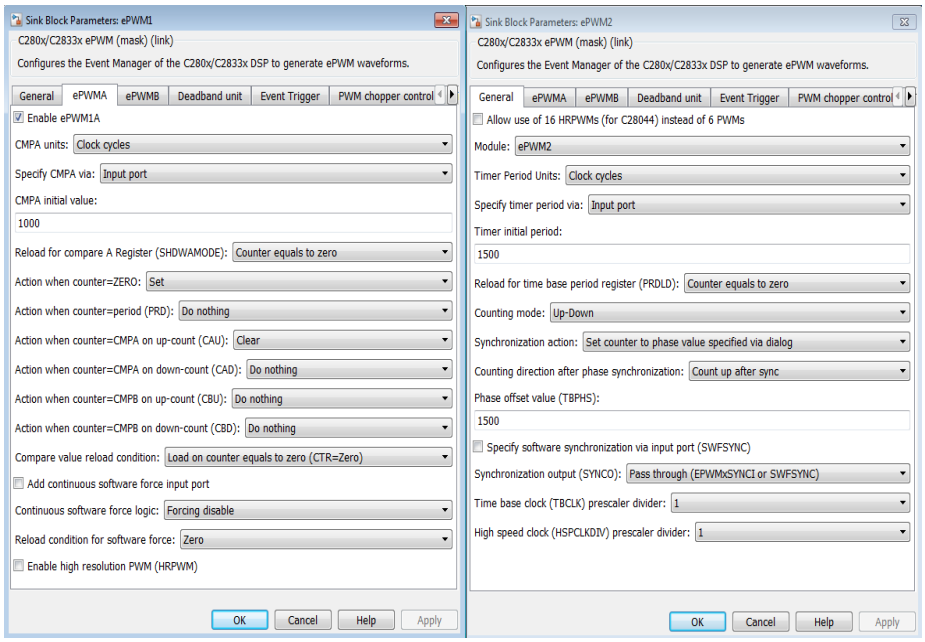

Figure 5.23. ePWM parameters for synchronization.

Table 5.1. ePWM output signals [5-1].

ePWM Module	Module Outputs	GPIO Pin
ePWM1	ePWM1A	GPIO00
	ePWM1B	GPIO01
ePWM2	ePWM2A	GPIO02
	ePWM2B	GPIO03
ePWM3	ePWM3A	GPIO04
	ePWM3B	GPIO05
ePWM4	ePWM4A	GPIO06
	ePWM4B	GPIO07
ePWM5	ePWM5A	GPIO08
	ePWM5B	GPIO09
ePWM6	ePWM6A	GPIO10
	ePWM6B	GPIO11

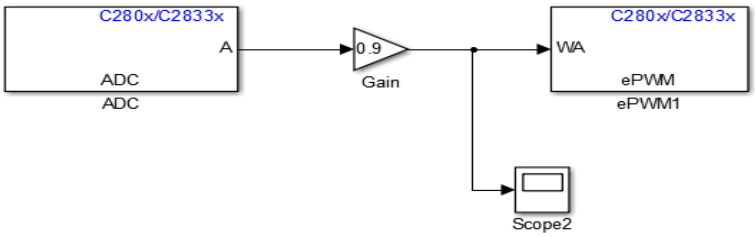

Figure 5.24. ADC example.

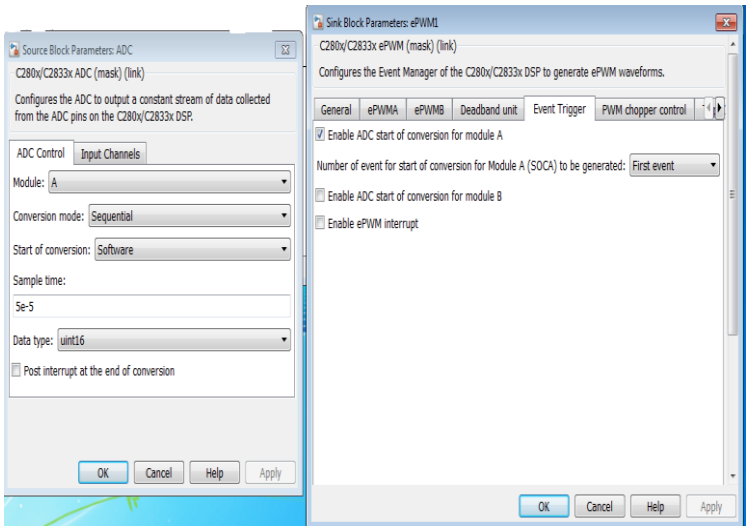

Figure 5.25. ADC and ePWM blocks parameters.

So, the duty cycle of this PWM signal can be controlled by changing the voltage from 0 to 3 V as can be seen on the oscilloscope. Notice that on the ePWM block you need to check the option (Enable ADC start of conversion for module A) as shown in Figure 5.25. Likewise the frequency of the ePWM output pulse can be controlled by the ADC input when we make it an input port. Figure 5.26 shows an example model of using the proportional integral (PI) controller to change the duty cycle of the ePWM output signals. The PID Controller block implements set-point weighting in the controller to achieve both smooth set-point tracking and good disturbance rejection [5-10]. Here the frequency was set to 40 kHz by making the time period 3750 in up counting mode.

It is important to have the system controller designed conveniently to make sure the response is as desired. Notice that data type conversion block and rate transition block have been included to convert input signal to specified data type, and handle transfer of data between blocks operating at different rates. The aforementioned instructions are the basic settings to program the TMS320F28335 DSP; there are a couple other things that can be done to improve the code output. For instance, we can set objectives for the code output in "Configuration Parameters" window under the code generation advisor, such as execution efficiency, ROM efficiency, and RAM efficiency. If you click on the set objectives button, you will see a pop up and you can import the options in a prioritized list.

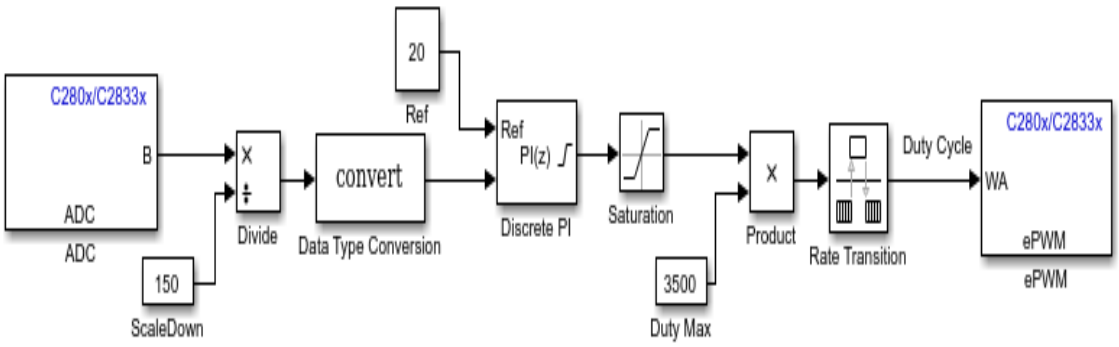

Figure 5.26. PI controller for duty cycle of ePWM output.

After you have a model built, you can click on the check model button and Simulink will analyze your model and provide tips to improve the generated code. Now it is good to start building your model. You can use any blocks from math, logic, and discrete block sets. Other blocks can be used as long as they do not have continuous states, the best way to check is by trial and error, add a block to your model and build the program. If the block is not compatible Simulink will tell you. In order to go to the DSP specific blocks (ADC, GPIO, CAN, PWM, etc.), scroll down to Embedded Coder > Embedded Targets > Processors > Texas Instruments C2000 > C2833x. There are also a number of IQ math and motor control blocks located in the optimization subgroup. Some of these blocks include Clark transformation, proportional integral derivative (PID) controller, Park transformation, speed measurement, and space vector generator.

5.8 Closed-Loop Control model for the Developed AC/DC Topology

The Model in Figure 5.27 has been developed to control the gate drivers of the proposed converter by controlling the duty cycles of the transistors. Each ePWM block generates two complementary pulses, so this model produces 4 pulses for the AC/DC converter prototype. The DSP generates the signals for the gate drivers to switch the GaN devices ON and OFF as desired. The ePWM blocks are coordinated to these 4 switches as ePWM1A, ePWM1B, ePWM2A, and ePWM2B for S_1, S_2, S_3, and S_4, respectively.

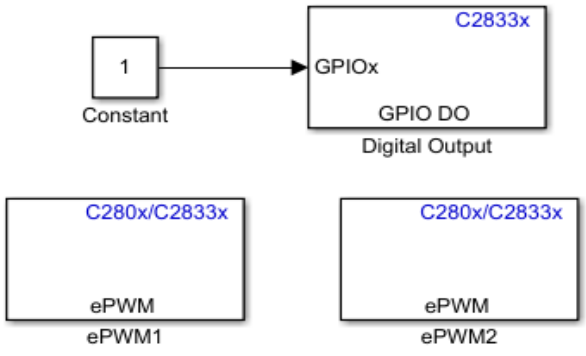

Figure 5.27. TMS320F28335 DSP model for the AC/DC converter prototype.

In Figure 5.28, a feedback model with four sensors is designed for the input signals of ADC1 and ADC2, and the PI controllers implemented a discrete-time controller in Simulink model. The reference values for the PI controllers are for the comparison with the ADC output to obtain the targeted time period for ePWM blocks in order to regulate the voltage levels for the power factor correction (PFC) stage and the series resonant converter (SRC) stage.

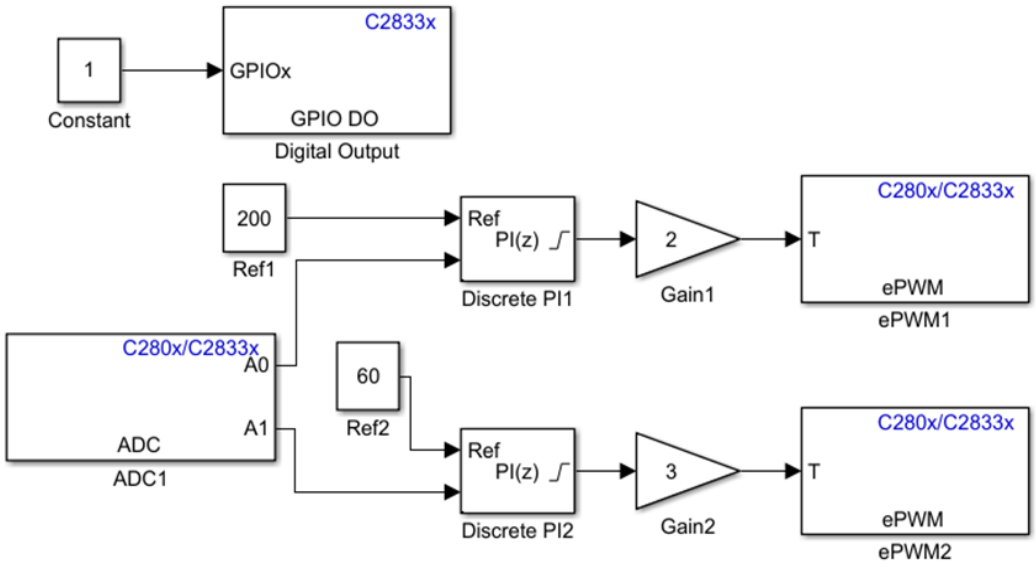

Figure 5.28. Designed AC/DC converter closed-loop DSP model.

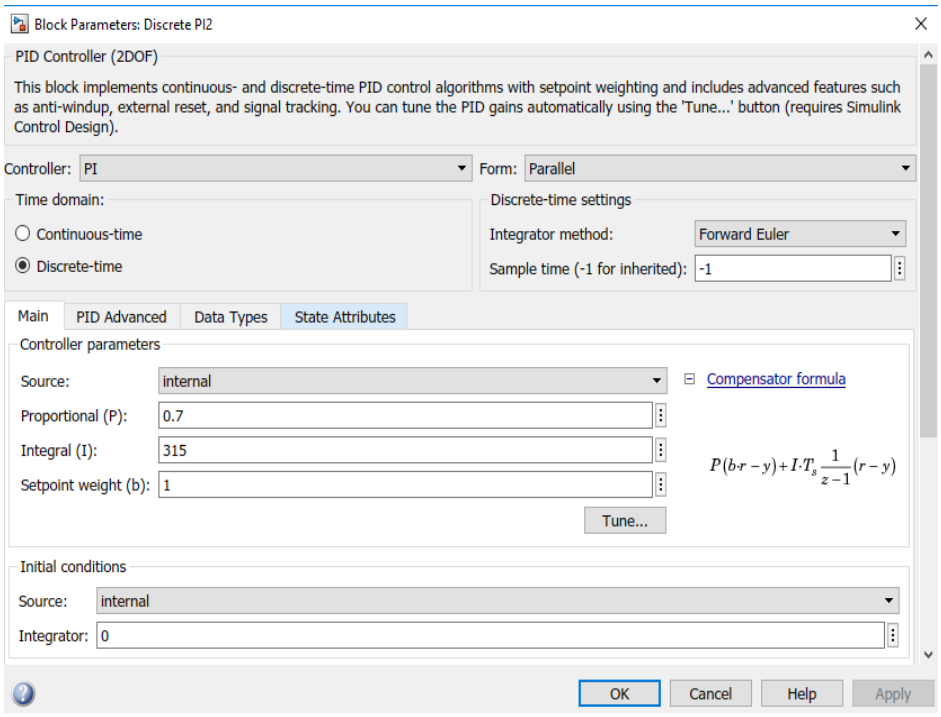

Figure 5.29. Designed SRC PI controller.

Figure 5.29 shows the designed PI Controller block for the SRC inverter. Chapter 6 describes the experimental DSP signals and results for the designed converter topology prototype.

5.9 Conclusion

Using MATLAB Simulink embedded coder tools is time saving, efficient, and great for research and industrial control design. The Embedded Coder Support package for TI C2833x Processor provides the fundamental blocks needed for any power electronic, smart grid or motor drives applications.This chapter presents the instructions on how to program the TMS320F28335 micro-controller using a make file approach with embedded coder in MATLAB Simulink, and then debugging the program in CCS V6. This is a new programming methodology to interact between MATLAB and CCS V6 which provides an explanation of the vital steps and settings needed to program the DSP. This DSP programming method is better approach than only using the CCS code writing in term of the speed of the system prototyping, especisally when the converter has few swtching transistors to be controllerd so the memory of the TMS320F28335 is not overwhelmed and no need to optimize the microprocessor speed and memory. All basic functions such as pulse width modulation, analog-digital conversion, and proportional-integral controllers are explained and integrated. Also, the target configuration and xMakefile configuration tool directories are presented and explained. Hence, the main steps for the interaction between MATLAB and CCS V6 are investigated and explained. Different versions of MATLAB have some differences to interact with CCS, TMS320F28335 DSP could be programmed using MATLAB 2011b and 2013a, but there are some errors for flash programming mode. Finally, the TMS320F28335 DSP control model for the proposed AC/DC converter topology is developed through MATLAB Simulink embedded coder programming approach and flash memory programming mode. The designed model has been described and presented.

5.10 References

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https://www.mathworks.com/matlabcentral/answers/uploaded_files/56491/Simulink%20Code%20Generation.pdf

[5-7] A. Elrajoubi, S. S. Ang and A. Abushaiba, "TMS320F28335 DSP programming using MATLAB Simulink embedded coder: Techniques and advancements," *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Stanford, CA, 2017, pp. 1-7.

[5-8] http://www.mathworks.com/help/ecoder/ug/tutorial-using-xmakefile-with-code-composer-studio-4-x-1.html?searchHighlight=code+composer+studio.

[5-9] http://www.ti.com/tool/tmdscncd28335

[5-10] http://www.mathworks.com/products/embedded-coder/webinars.html#.

CHAPTER 6

EXPERIMENTAL RESULTS AND DISCUSSIONS

6.1 Introduction

This chapter describes the printed circuit board (PCB) design and fabrication steps for the gallium nitride (GaN) AC/DC converter topology. The experimental results are presented, followed by discussions.

6.2 Converter Topology Prototype Design

Printed circuit board (PCB) layout was performed using Allegro Cadence software. Four layer PCB is recommended in [6-1] for driving GaN devices to obtain a suitable switching performance. The design methodology of the experimental prototype for the GaN AC/DC converter is described.

6.2.1 OrCAD Capture Circuit Schematic Design

The first step to design the PCB layout for the converter is to draw the circuit schematic using the software OrCAD capture. The designed topology schematic drawing in OrCAD is shown in Figure 6.1. The components are selected from the PSpice library. Each component has to be associated with the correct PCB footprint using the dimensions specified by the manufacturer data sheet. The connection of the gate drivers is considered to provide the gate signal to each switching transistor using the off-page connectors. The jumpers J_1, J_2, J_3, and J_4 are used to obtain the desired connections for the input and output terminals.

6.2.2 Allegro PCB Editor Layout Design

In this chapter the designed 4-layer PCB for the prototype is described. After drawing the circuit schematic in OrCAD and associating a PCB footprint for each component, the design is exported to Allegro PCB Editor. By creating a Netlist which contains the information of the

circuit schematic; OrCAD generates the netlist and opens its in Allegro PCB Editor [6-2]. Then, all the components of the converter are placed and connected with the fundamental considerations to mitigate as much parasitics as possible. The PCB layout in OrCAD Cadence Allegro PCB Designer is depicted in Figure 6.2. The four-layers of the PCB layout can be seen in Figures 6.3, 6.4, 6.5, and 6.6, respectively. Layer 2 is the ground return and layer 3 is the gate drivers and DSP card power supplies sources. A trace parasitic inductance analysis is considered for the converter layout, and briefly described in this dissertation. When operating at high frequencies, the parasitic inductances of the traces in a PCB and the intrinsic capacitance of the switching devices can cause over-voltages and high-frequency oscillations [6-3].

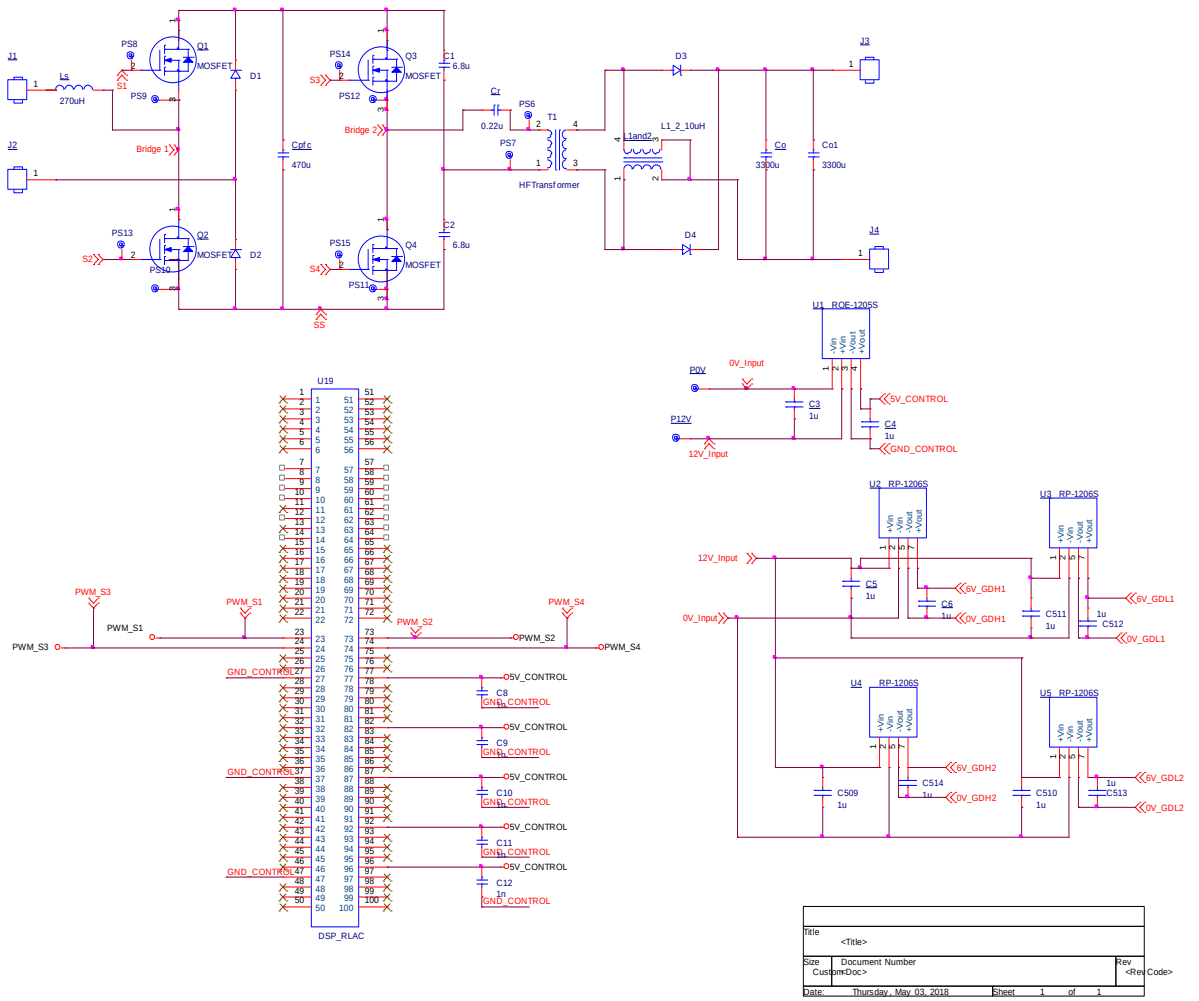


Figure 6.1. OrCAD Capture schematic of the AC/DC converter.

Therefore, a careful analysis of the trace parasitic inductances should be accomplished before building any converter board. The trace parasitic inductances should be less than 20 nH per inch and can be calculated using equation 6.1 [6-3, 6-4]:

$$L_t = 2l\left(\ln\left(\frac{2l}{w}\right) + \frac{1}{2} + 0.2235\left(\frac{w}{l}\right)\right) \quad \text{nH} \tag{6.1}$$

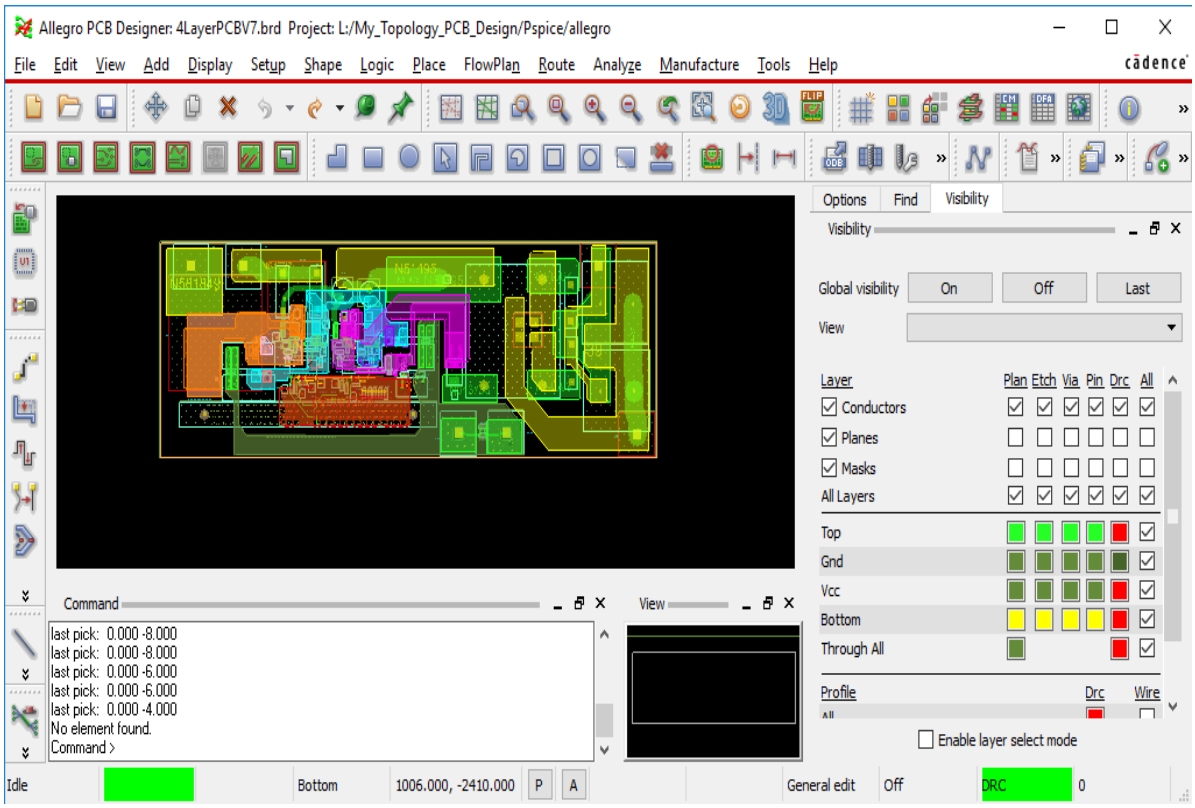


Figure 6.2. 4-layer converter layout in Cadence Allegro PCB Designer.

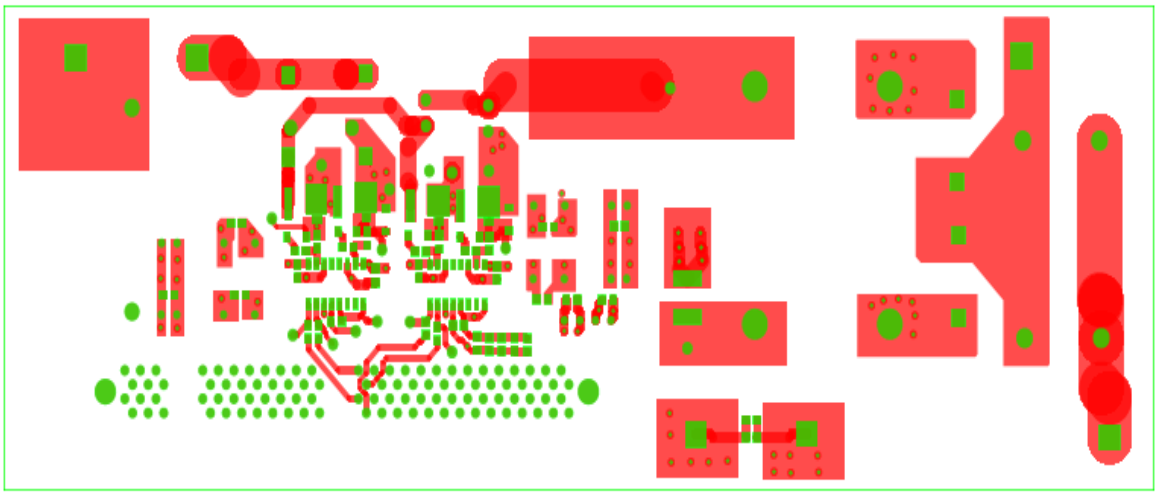


Figure 6.3. Top layer PCB layout.

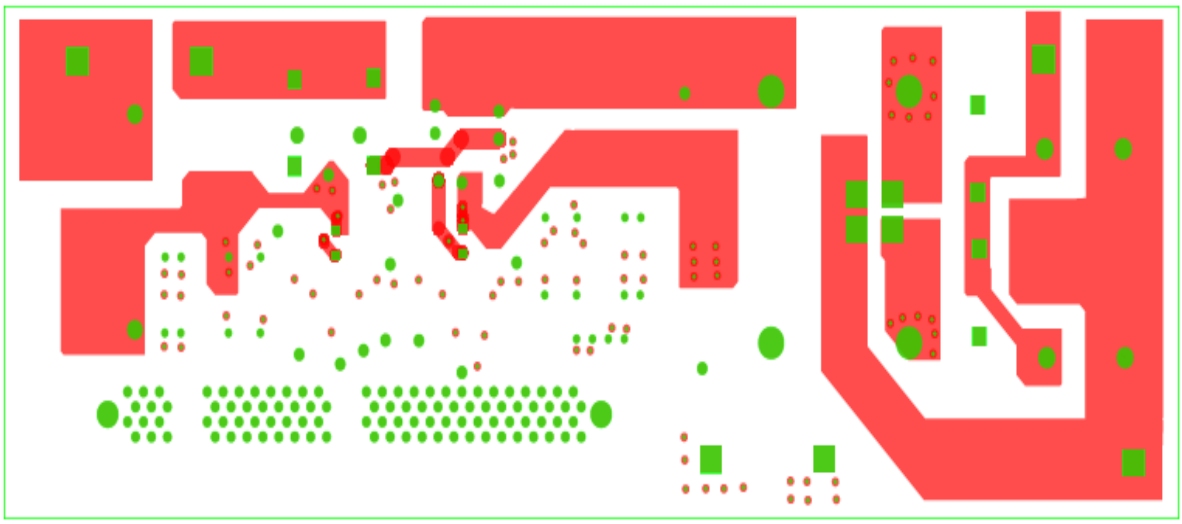


Figure 6.4. Bottom layer PCB layout.

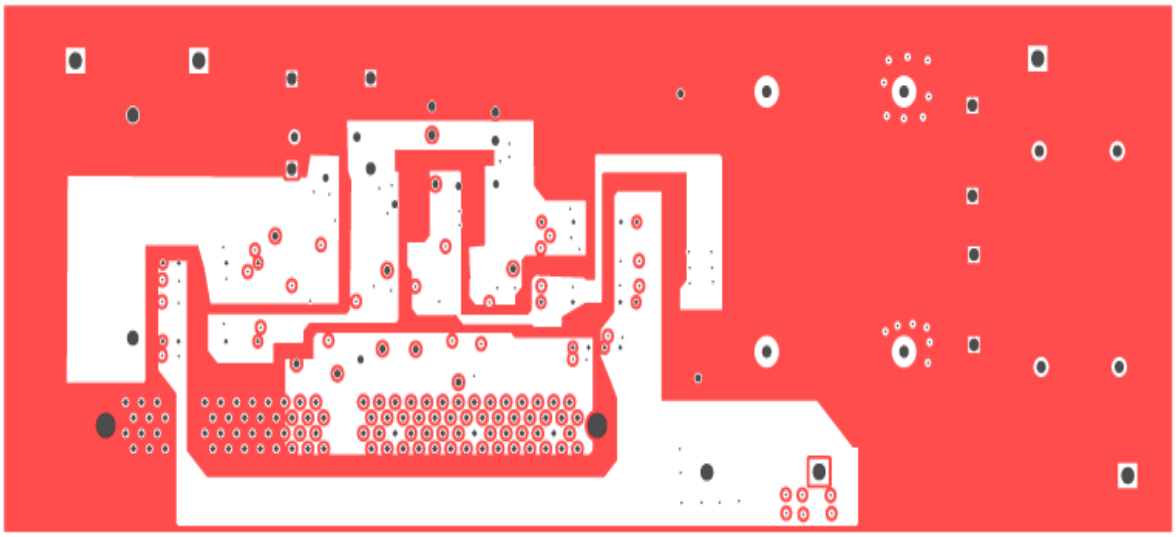


Figure 6.5. Layer 2 layout with drill holes.

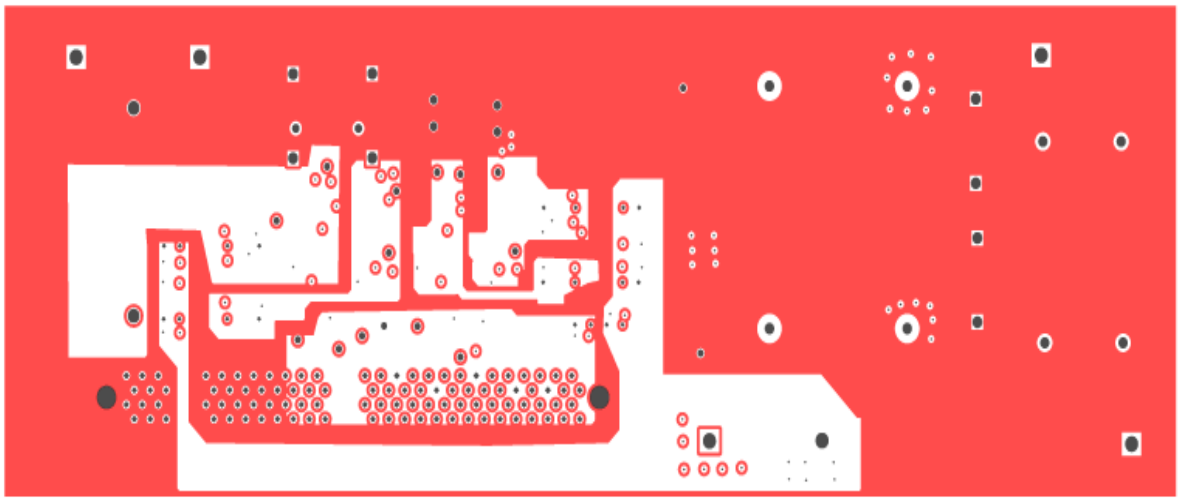


Figure 6.6. Layer 3 layout with drill holes.

From equation (6.1), it can be seen that the trace parasitic inductance is a function of the length and width of the trace. Therefore, a gate driver PCB copper traces have to be as short as possible to avoid false triggering due to the deleterious effects of copper trace parasitics [6-4]. Once the PCB layout design is done with mitigating the effects of trace parasitic inductances, the next step is to create the Gerber and drill files for fabrication. All Cadence Allegro PCB design steps to take a circuit design from paper to a physical PCB are illustrated in [6-2].

6.3 GaN Gate Driver Considerations

GaN high-electron-mobility transistors (HEMT) are voltage driven devices. Totem pole gate-driver integrated circuits (ICs) can be used to apply the required voltage level to either turn the switch on or off. Gate driver design considerations recommended in [6-1] for GaN devices have been applied in the design of the 4-layer PCB. Driving the top switches of the power factor correction (PFC) and series resonant converter (SRC) of the converter can be accomplished by using either bootstrap circuits or isolated gate drivers power supplies. In this dissertation work, isolated power supplies and isolated gate drivers are implemented without the bootstrap circuit as explained in Chapter 2. Attention was paid to the gate driver layout design considerations and best practices illustrated in [6-1] for GaN devices. These considerations include controlling noise coupling, choosing the right gate resistors, setting the dead times, minimizing gate ringing, controlling Miller effect, high-side switch driving, minimizing layout parasitics, and applying quasi-Kelvin source for gate driver return. Decoupling capacitors are placed at the output of the power supply and at proximities to the drivers ICs to supply switching transient current and reduce voltage ripples. The voltage level to drive a HEMT needs to be higher than the threshold voltage which defines the point when the device shall conduct. It is necessary to apply quasi-Kelvin connections for the driver return loops, and minimize the parasitics of the pull-down and pull-up loops by locating the components (gate resistances, capacitors, and diodes) as close as possible.

Moreover, all gate, drain, and control traces have been isolated to prevent overlapping between different traces as recommended in [6-1]. The prototype utilized gate resistors $R_{G(ON)}$ of 10 Ω, and $R_{G(OFF)}$ of 1 Ω with a low forward voltage Schottky diode as depicted in Figure 6.7. Silicon fast recovery with low capacitance Schottky diodes are selected for gate pull-down path and gate-to-source spike clamping as the gate driver has single output for gate pull up and down. To avoid false turning on of the HEMT, the current flowing in Miller capacitance (C_{GD}) will has a low impedance circuit through D_1 diode back to the driver circuit. A Silicon Labs Si8273 isolated gate driver [6-5] with desired features, like high dv/dt immunity, low propagation delay (60 ns or less), high DC bus voltage level (1500 V), and very high reliability is used. Figure 6.8 shows the schematic of the designed gate drivers utilizing the isolated driver (Si8273) for the GaN switches in the half-bridges of the PFC and the SRC. The Silicon Labs Si8273 gate driver has convenient isolation barrier for 2.5 kVRMS withstand voltage and 200 kV/μs common-mode transient immunity (CMTI), also it has an Under-voltage Lockout (UVLO) protection for voltage drops as described in [6-5]. The peak output current of the Si8273 is 4 A. The schematic designed in OrCAD PSpice capture for the gate drivers is shown in Figure 6.8. As can be seen, U404 and U504 are the gate drivers 16-Small-outline integrated circuit (SOIC) which drive both the top (S_1 or S_3) and bottom (S_2 or S_4) switches.

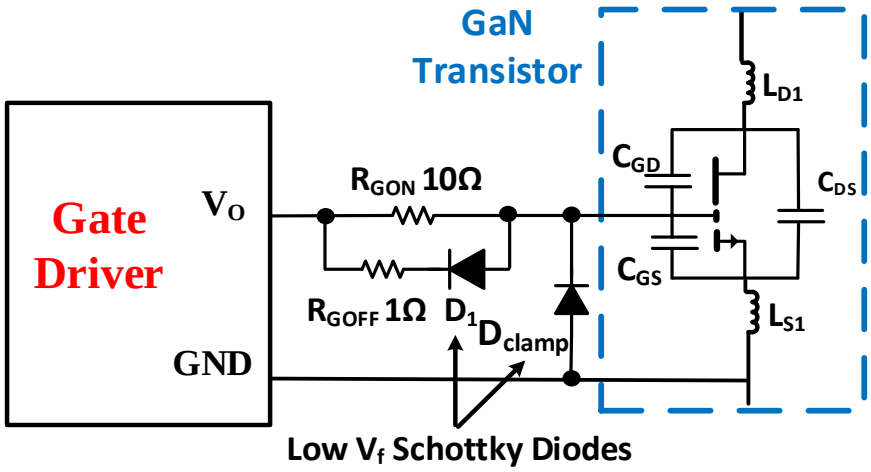
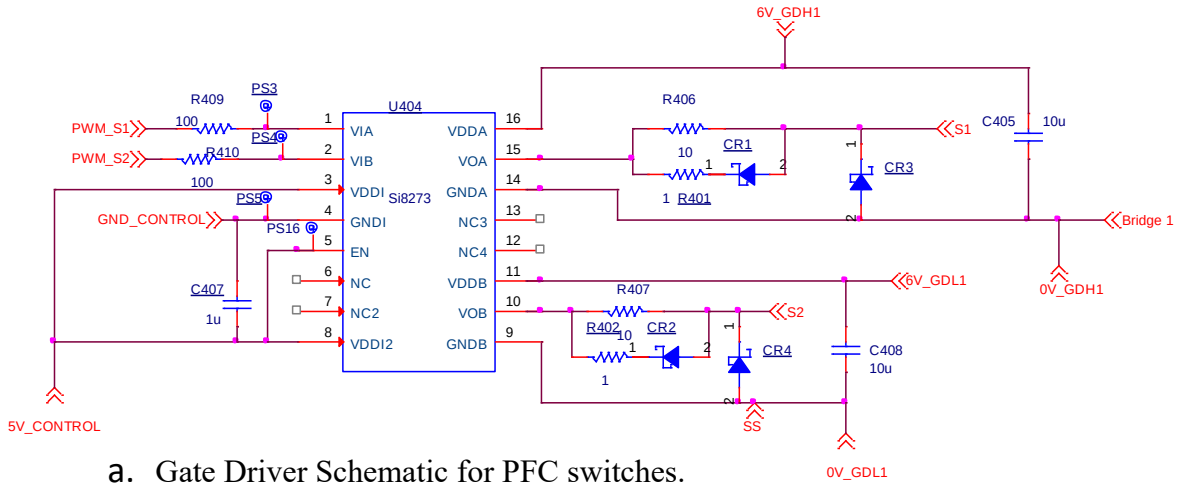
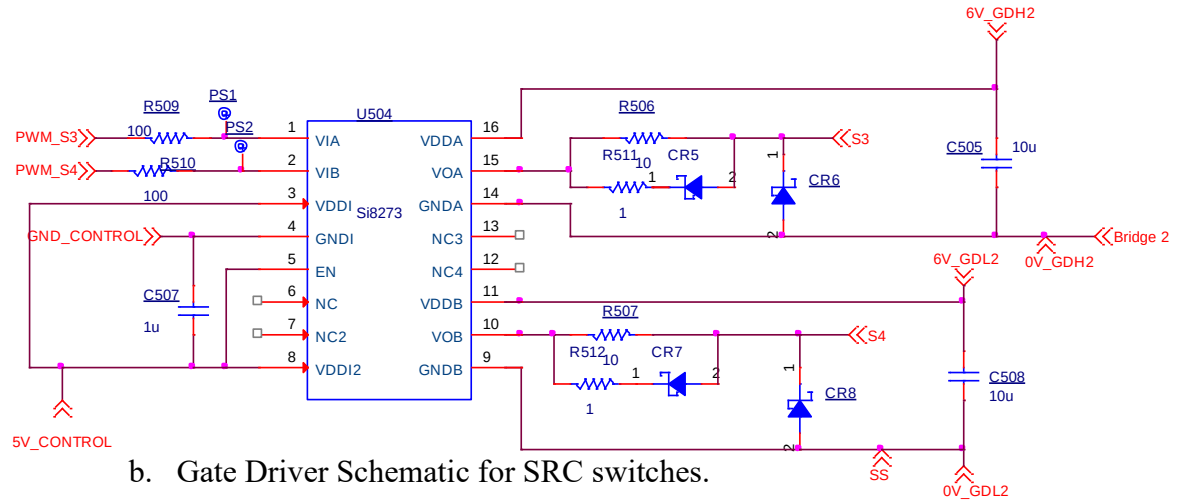


Figure 6.7. Gate driver for GaN transistor.

The 10 Ω gate turn on resistances for S_1, S_2, S_3, and S_4 are R406, R407, R506, and R507, respectively, while the 1 Ω gate turn off resistances for S_1, S_2, S_3, and S_4 are R401, R402, R511, and R512, respectively. All fast recovery Schottky diodes used for turn off paths and Miller effect control are CR1 to CR8. The 100 Ω input signal resistances are to protect the DSP from high currents, which are placed at the VIA and VIB of the gate driver U404 and U504. C405, C408, C505, and C508 are the 10 µF, 25 V capacitors used to yield smooth 6 V supply very close to the driver IC, while the 5 V input voltages of the Si8273 have 1 µF, 25 V capacitors (C407 and C507). The Si8273 enable signal is connected to the 5 V input voltage rather than using a DSP signal.



a. Gate Driver Schematic for PFC switches.



b. Gate Driver Schematic for SRC switches.

Figure 6.8. Designed gate drivers schematic for GaN half-bridge legs.

A Texas Instruments TMS320F28335 DSP and two Silicon Labs Si8273 gate drivers are used for switching control. Figure 6.9 shows the 3.3 V DSP signals at 50 kHz, while the gate drivers' 6V outputs (V_{GS}) to switch the PFC and SRC transistors at 100 kHz are presented in Figure 6.10. The 50 kHz switching frequency is used for below resonant operation mode, while the converter resonant frequency is 64 kHz. The experimental measurements results are shown in this Chapter for ZVS operating condition. The top side switches of the PFC and SRC (S_1 and S_3) are synchronized together, while the bottom side switches S_2 and S_4 are synchronized together in order to avoid large spikes during turning on transitions.

The gate signals shown in Figure 6.10 are the synchronized PWM signals obtained from the TMS320F28335 DSP through Si8273 gate drivers to operate the converter switches at 100 kHz switching frequency. The top two signals are S_1 and S_2 V_{GS} voltages while the bottom two signals are S_3 and S_4 V_{GS} voltages. GaN devices do not have intrinsic body diodes to conduct the boost inductor current during the freewheeling stages. The used GS66504B 650V E-mode, 15 A GaN transistors rise and fall time is extremely small, and the propagation delay of the Si8273 gate driver is 60 ns or less.

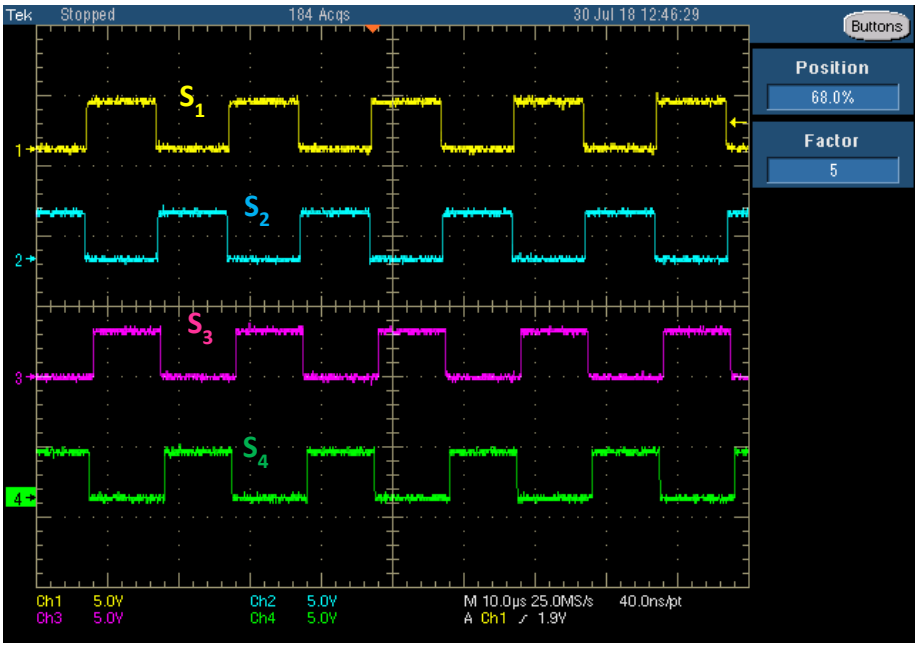


Figure 6.9. 3.3 V DSP signals for gate drivers at 50 kHz.

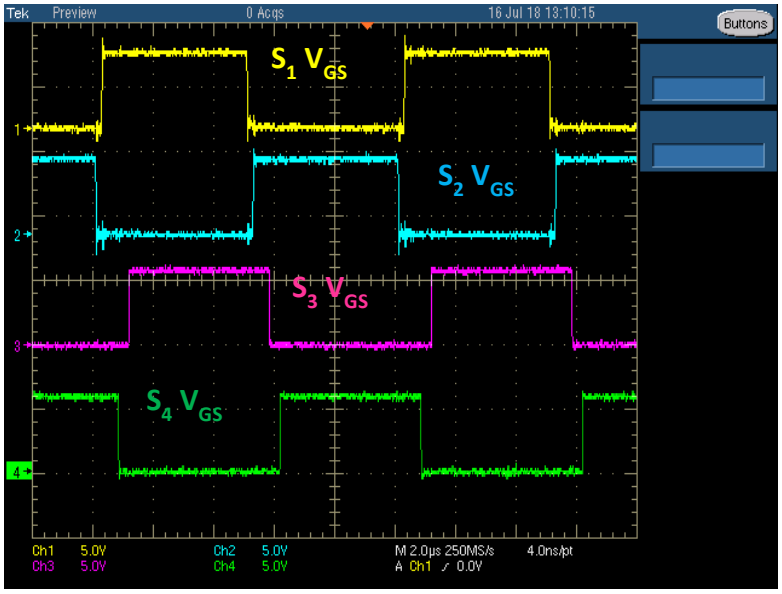


Figure 6.10. Gate drivers' synchronized signals for GaN switches (V_{GS}) at 100 kHz.

So the dead time for the PFC V_{GS} (S_1 and S_2) is made very small to minimize the time that the boost inductor is interrupted to avoid any inductive spike at the midpoint of S_1 and S_2. The V_{GS} dead time of the PFC switches is minimized to 30 ns in order to minimize the boost inductor current spike and obtain best V_{PFC} waveform, while the V_{GS} dead time for the SRC transistors is adjusted to 90 ns at which the converter yields a minimum spike of the output voltage. However, Figure 6.11 shows the gate-to source voltages from the Si8273 drivers to operate the PFC and the SRC switches with 180^o phase shifted signals at 105 kHz switching frequency.

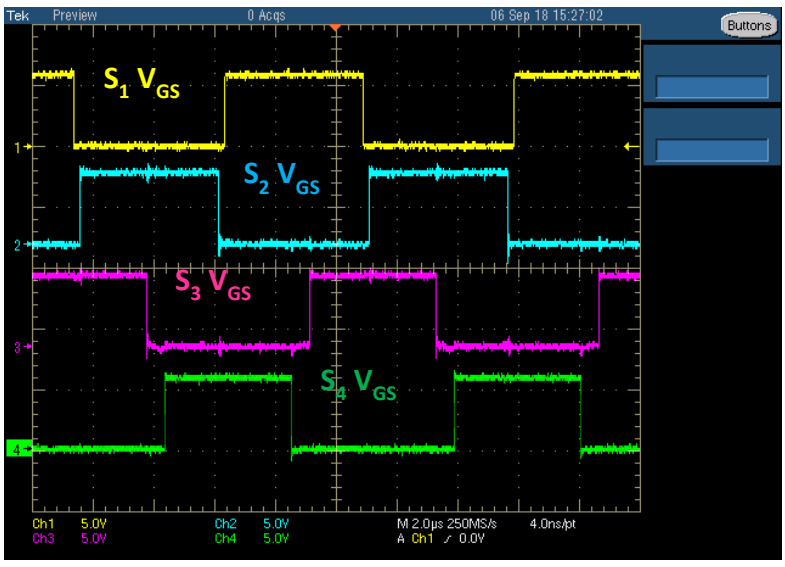


Figure 6.11. Phase shifted V_{GS} signals for switching at 105 kHz.

That is performed to investigate the effect of the PFC and SRC switching sequence. Also, changing the dead time for the GaN half-bridge switches demonstrated significant effect on the PFC DC voltage and output voltage spikes.

6.4 Converter Components Selection

The main circuit components of the constructed converter are shown in Table 6.1 along with some of their key features. Two parallel capacitors of (C_o) are used in the converter prototype to obtain 6600 µF for regulating the output voltage.

Table 6.1. Constructed experimental prototype main parts.

Element	Description	Features
PFC Boost Inductor (L_s)	PCV-2-274-10L	270 µH, I_{rms} = 7.2 A.
GaN Devices (S_1 : S_4)	GS66504B 650V E-mode, 15 A. $V_{GS(th)}$ = 1.3 V.	$R_{DS(on)}$ = 100 mΩ, V_{GS} = 0:6 V, Q_{RR}= 0, Q_G = 3 nC.
Power Diodes (D_1 : D_4)	FFH60UP40S 60 A 400 V	Ultrafast Recovery, Low V_f.
Gate Drivers	Si8273, 1500 V, 16-pin SOIC, 200 kV/µs CMTI	60 ns propagation delay, high performance and speed isolation technology.
Schottky Diodes	30 V 2 A DB2230600L	Silicon epitaxial fast recovery with low capacitance.
PFC Capacitor (C_{PFC})	CAP ALUM 470 µF 20% 350 V, LQS2V471MELA50	Nichicon electrolytic radial.
SRC Capacitors (C_1 & C_2)	CAP ALUM 6.8 µF 20% 250 V, ULD2E6R8MPD1TD	Nichicon electrolytic radial.
Resonant Capacitor (C_r)	CAP CER 0.1 µF 500 V	X7T 2220 ceramic.
High-Frequency Transformer	100 kHz, 350 VA, 130/117 V	Nanocrystalline toroid core (W376-04).
CDR Coupled Inductor (L_1 & L_2)	IHCL-4040DZ-5 A 10 µH	Low profile, high-current coupled inductor, shielded construction.
CDR Output Capacitor (C_o)	CAP ALUM 3300 µF 20% 100 V, UVZ2A332MRD	Nichicon electrolytic radial.
TMS320F28335 DSP	Texas Instruments TMDSDIM100CON5PK	C2000 class, 32-bit, 150 MHz.

The designed converter is constructed onto a 4-layer PCB. The TMS320F28335 DSP is programmed as explained in Chapter 5 to generate the PWM signals (for S_1 to S_4) for the gate drivers (Si8273) which are initially set for 100 kHz fixed duty cycle operation. Multiple vias have been used to reduce resistive losses as well as increasing the width of all traces as much as possible. Quasi-Kelvin source connections for the GaN transistors gate driver returns are carefully used in the designed prototype.

6.5 Experimental Prototype Testing

Zero-voltage switching is implemented and verified in the series resonant converter to minimize switching stresses and losses. The resonant capacitor and the transformer leakage inductance determine the resonant frequency and the characteristic impedance values. The quality factor (Q) of the proposed converter is given by:

$$Q = \sqrt{L_r / C_r} / R_{Load} \tag{6.2}$$

So the SRC characteristics depends on the load resistance and resonant tank [6-6].

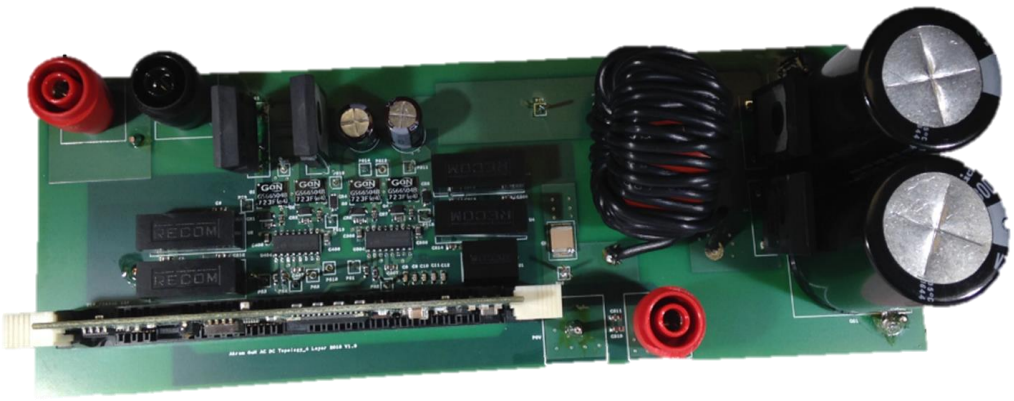
From Figure 3.22, at high frequency and with large output capacitor (C_o = 6600 µF) C_o is shorting one inductor of the CDR inductors (L_1 and L_2) at each mode. So, the total equivalent resonant inductance which includes the CDR inductance referred to the transformer primary side is calculated as:

$$L_r = 50.31 + 1.11^2\ (10) = 62.63\ \mu H. \tag{6.3}$$

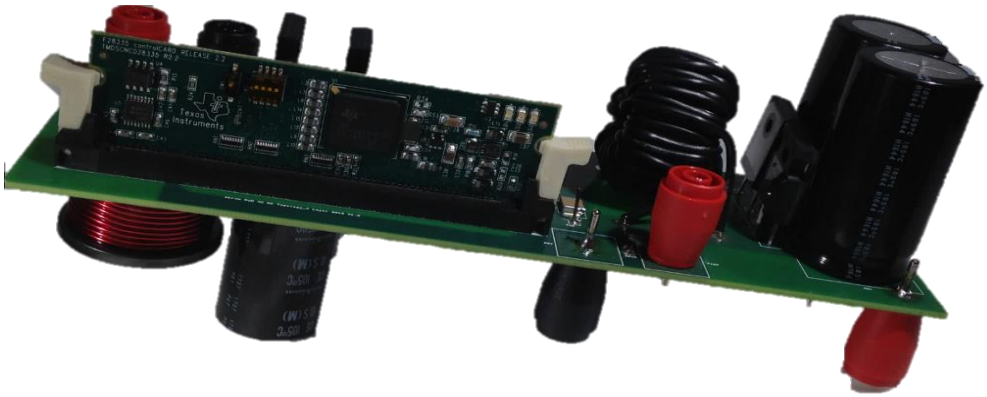
Then the resonant frequency of the fabricated converter is given by:

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{1}{2\pi\sqrt{0.1\ \mu F * 62.6\ \mu H}} = 64\ \text{kHz}. \tag{6.4}$$

The experimental prototype for the investigated GaN AC/DC converter is shown in Figure 6.12.



a. Prototype top view.



b. Prototype side view.

Figure 6.12. The fabricated GaN AC/DC converter prototype board.

For the converter prototype, a 100 kHz transformer is designed as explained in Chapter 4 to obtain the optimum flux density and satisfy the transformer specifications. Experimental work is conducted to verify the feasibility of this GaN based converter for various load conditions. The fabricated converter has been tested for AC/DC conversion operation as shown in Figure 6.13. The RMS value of the output DC voltage shown in Figure 6.14 is 46 V.

The designed gate drivers are working to switch the GaN transistors appropriately. The signals from each gate driver are 6 V pulses as designed in Figure 6.8 and shown in Figure 6.10. Schottky diodes are utilized for gate-to-source spike clamping (gate pull-down paths) to mitigate Miller effects, eliminate the ringing, and avoid false turn-on or gate oscillation as described in section 6.3 and explained in [6-1].

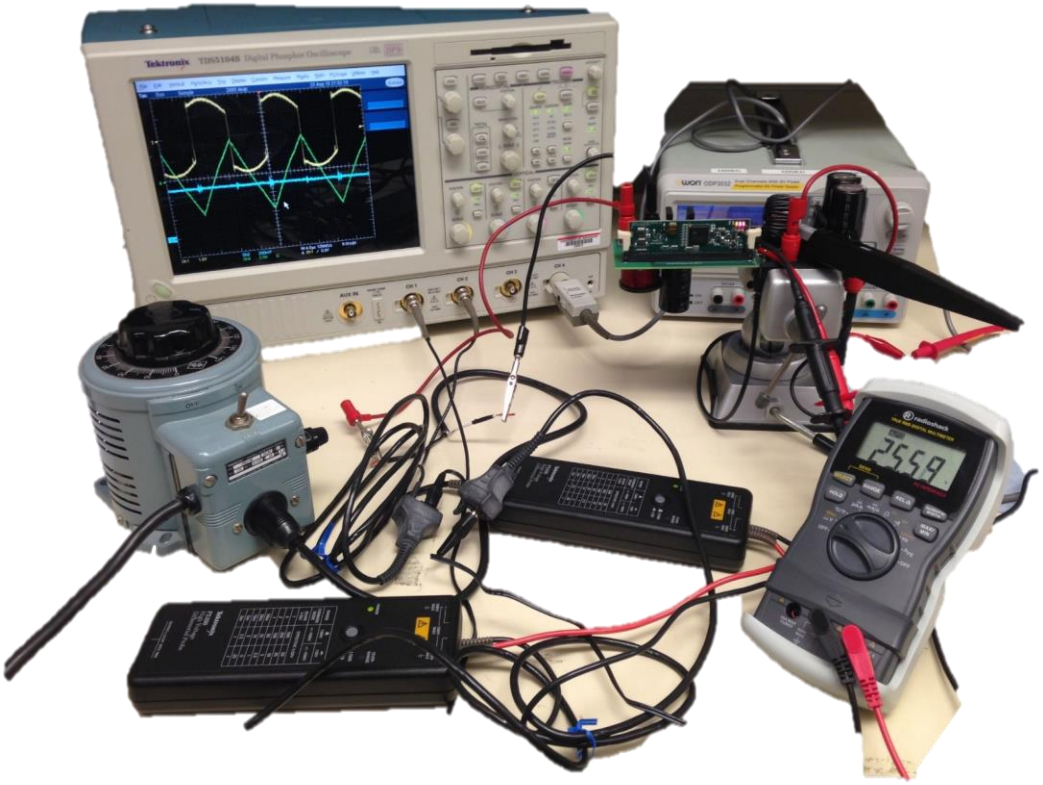


Figure 6.13. Experimental setup using P5200 isolated voltage differential probes.

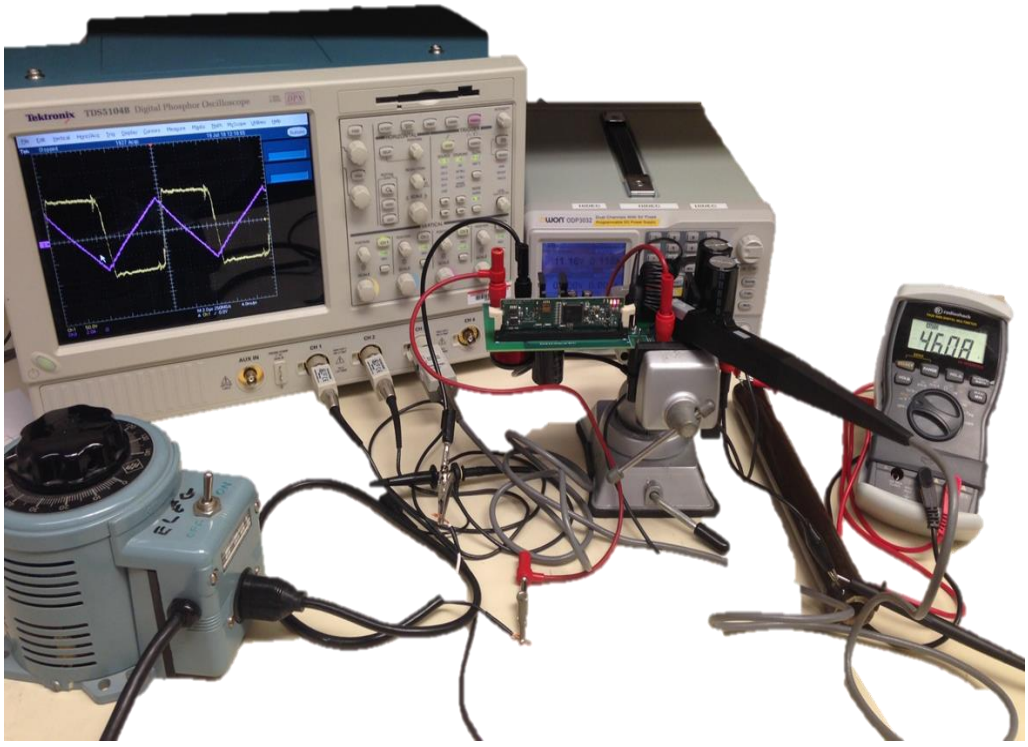


Figure 6.14. Converter experimental testing setup for DC output voltage of 46 V.

6.6 Experimental Results

The transformer primary voltage ($-V_{T1}$) and primary resonant current (I_r) are shown in Figure 6.15 for a reduced input voltage level and very large load resistance (100 kΩ) operating at 100 kHz. V_{DS} across the transistors exhibited noticeable parasitic noise and over voltage oscillation which showed V_{T1} having some switching ringing. Optimum switching performance is a challenge, and depends on the designed gate driver performance and the developed board layout design. Series resonant converter characteristics have been shown to depend on the load resistance value. Hence, the transfer characteristics of the converter may change with the load as the q-factor of the series resonant converter changes.

Matching the switching frequency for S_3 and S_4 with the resonant frequency of the SRC results in soft-switching to reduce the switching losses. Also, adjusting the switching frequency and duty ratios for S_3 and S_4 will yield the discontinuous conduction mode (DCM) operation for the SRC current.

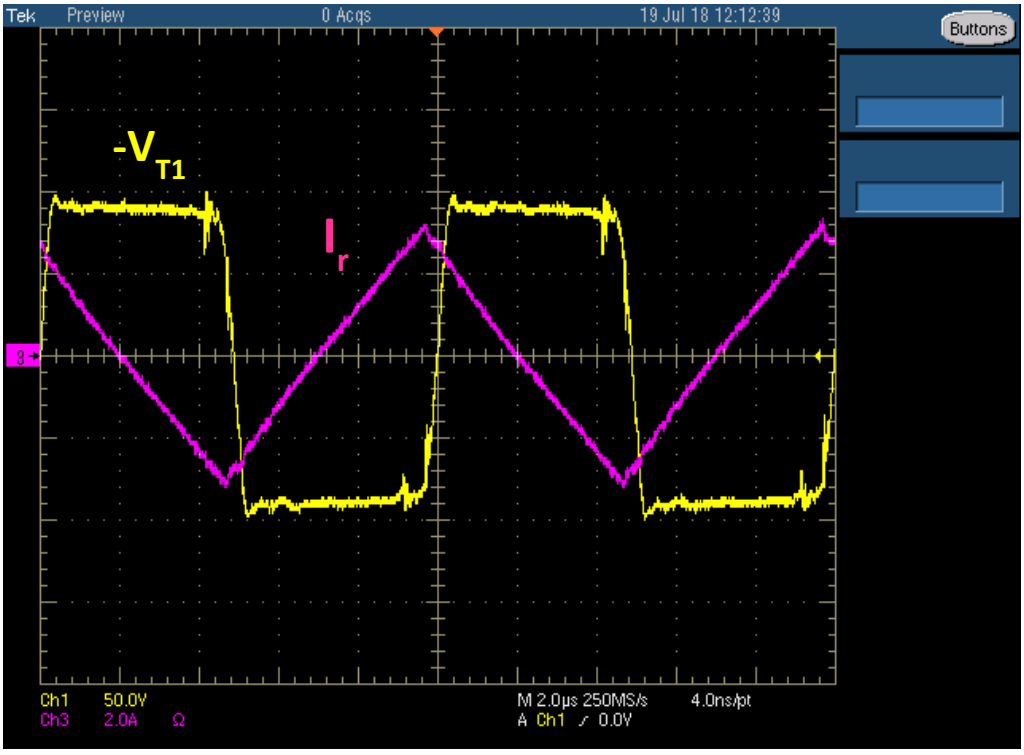


Figure 6.15. $-V_{T1}$ and I_r experimental results for V_{in} = 60 V and R_L = 100 kΩ.

Applying low duty ratio signals to SRC switches S_3 and S_4 results in discontinuous conduction mode operation while high duty ratio signals yields continuous conduction operation for the SRC stage. The half-bridge SRC switching signals have dead time of 100 ns and 46% duty cycle as the gate drivers signals shown in Figure 6.10 were used for this measurement. Therefore, the transformer primary voltage ($-V_{T1}$) shown in Figure 6.15 decreases from 90 V to -90 V in 0.6 µs, and it also increases from -90 V to 90 V in 0.6 µs. The experimental result for the transformer primary voltage (V_{T1}), PFC output voltage, and primary current (I_r) are shown in Figures 6.16 and 6.17 for V_{in} of 70 V operating at 105 kHz with loads of 1 kΩ and 2 kΩ, respectively.

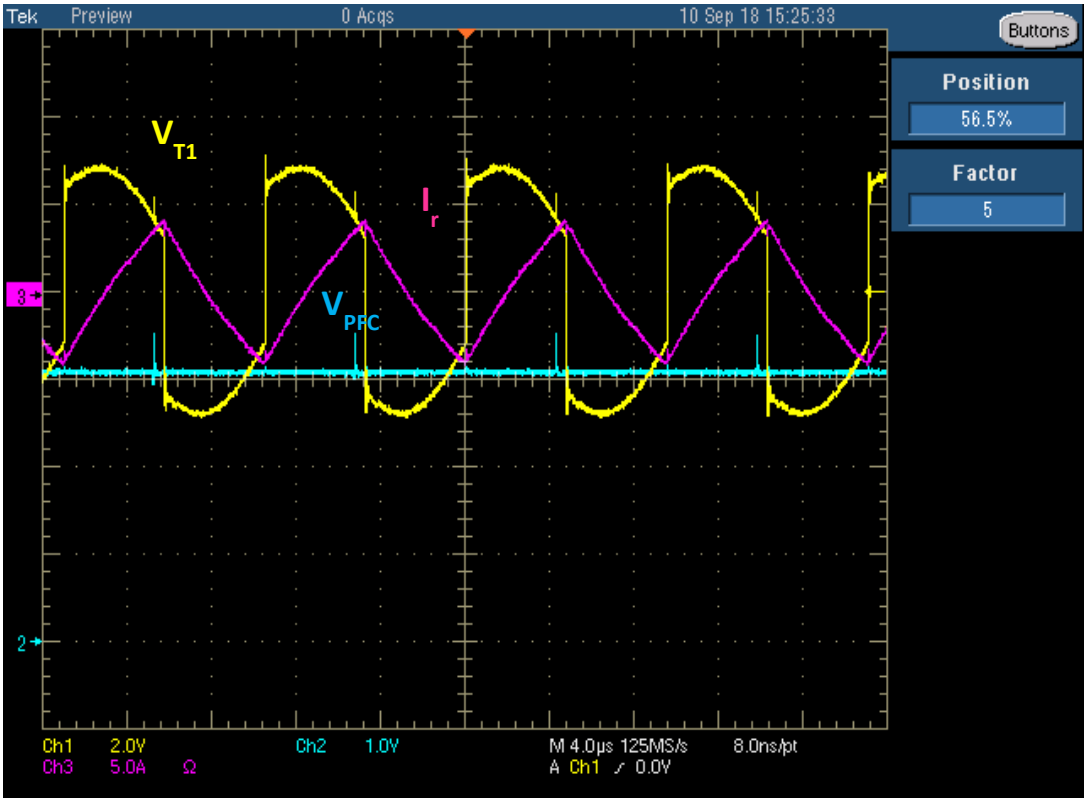


Figure 6.16. V_{T1}, V_{PFC}, and I_r waveforms for Vin = 70 V and 1 kΩ @ 105 kHz.

The measured PFC output voltage is 150 V. As can be noticed from the voltage measurements scales of Figures 6.16 to 6.24, P5200 isolated voltage differential probes have been used with the range sets the attenuation to 1/50. So 1 V is 50V/DIV for all voltage measurements of Figures 6.16 to 6.24.

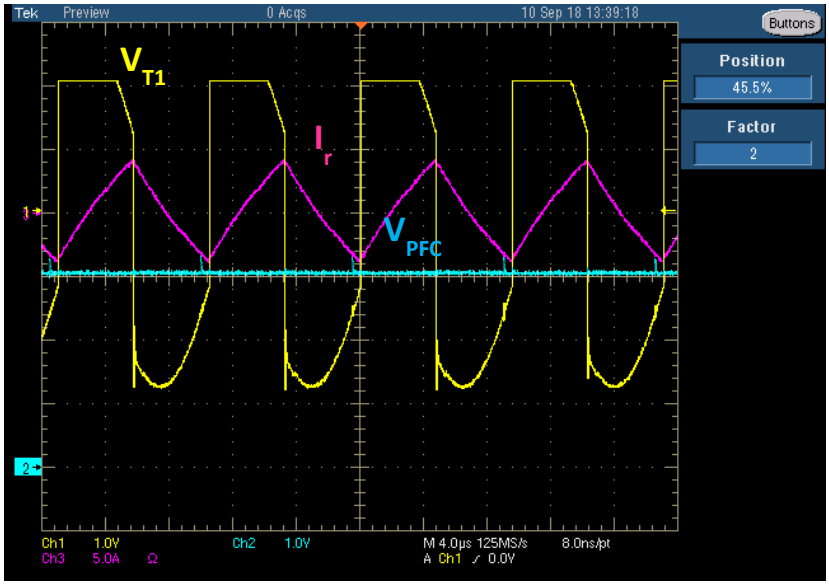


Figure 6.17. V_{T1}, V_{PFC}, and I_r waveforms for Vin = 70 V and 2 kΩ @ 105 kHz.

The waveforms of V_{T1}, V_{PFC}, and I_r are shown in Figure 6.16 for an input voltage of 70 V and a load resistance of 1 kΩ operating at the switching frequency of 105 kHz. This measured PFC DC bus voltage is 154 V, and the transformer primary voltage is around 130 V. The waveforms for the gate-to-source voltage (V_{GS}: the yellow signal), and drain-to-source voltage (V_{DS}: the blue signal) for S_3 and S_4, and the SRC resonant current when operating at 105 kHz for a reduced input voltage with a load of 2 kΩ and 1 kΩ are shown in Figures 6.18, 6.19, and 6.20, respectively.

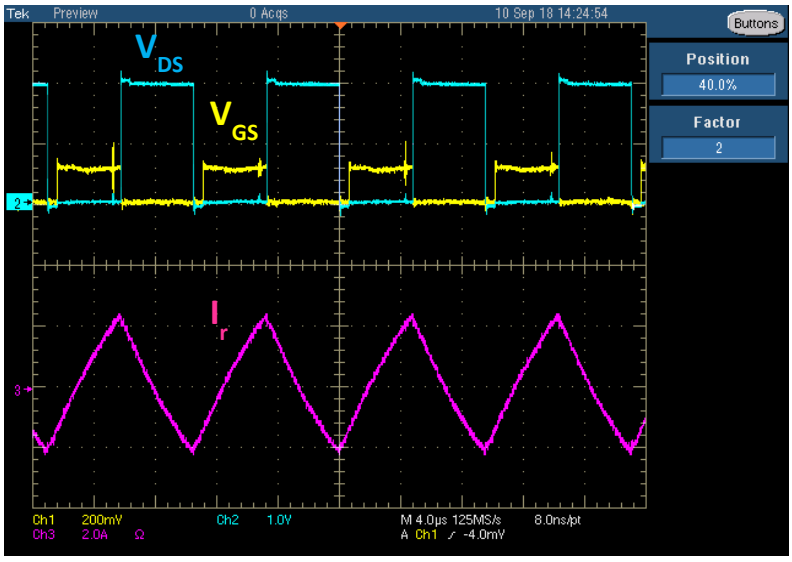


Figure 6.18. S_3 V_{GS} V_{DS}, and I_r waveforms for R_L = 2 kΩ @ 105 kHz.

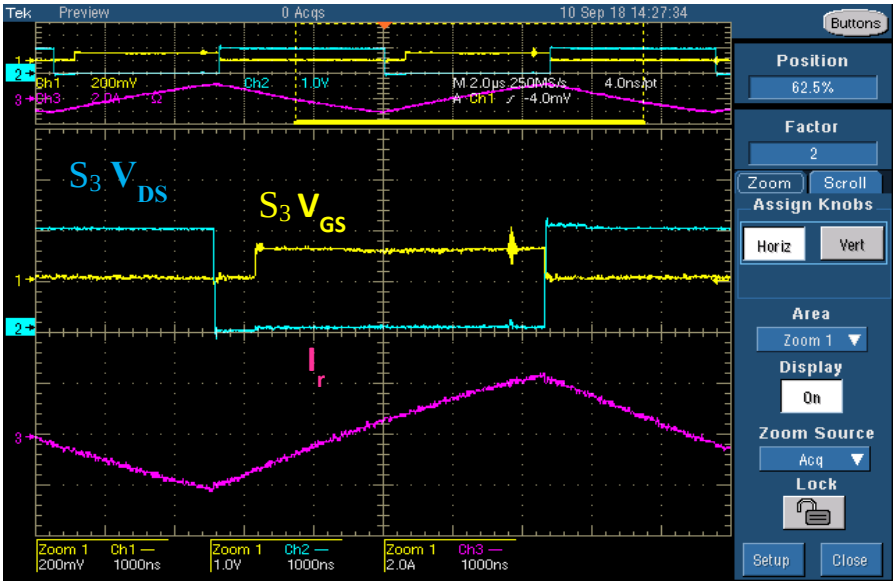


Figure 6.19. S_3 V_{GS} V_{DS}, and I_r waveforms for R_L = 2 kΩ @ 105 kHz.

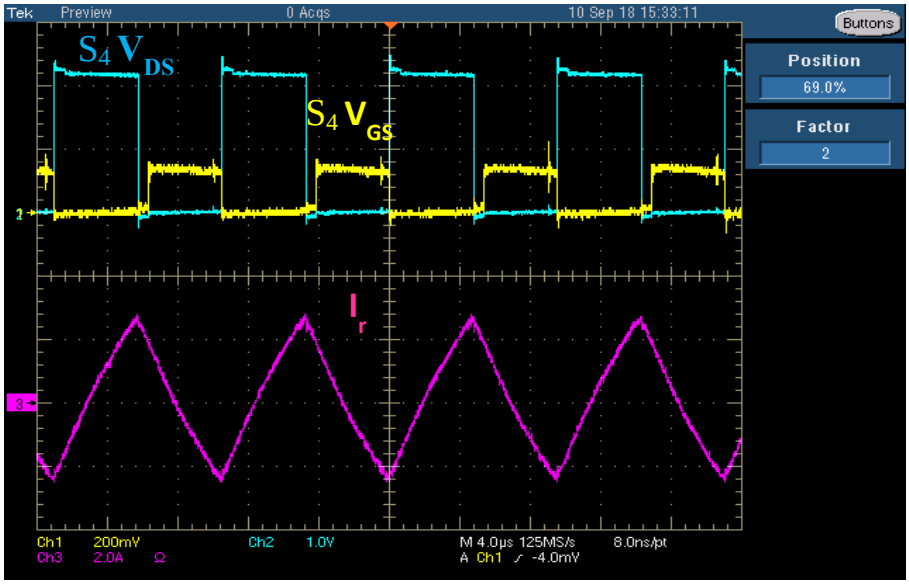


Figure 6.20. S_4 V_{GS} V_{DS}, and I_r waveforms for R_L = 1 kΩ @ 105 kHz.

Zero-voltage-switching (ZVS) is achieved for the SRC transistors (S_3 and S_4) as demonstrated in these waveforms at an above-resonant frequency of 105 kHz. The transformer primary current is not resonant sinusoidal waveform as the converter prototype resonant frequency is smaller than 105 kHz and so the converter is operated as a regular PWM converter for the above-resonant continous conduction mode of operation. However, the ZVS occurs because of the condition when the drian-to-source voltage is zero across the transistor as the current is flowing in the reverse direction through the body-drain diode of a MOSFET, at that moment

the transistor is turned on as can be seen from the ZVS results in Figures 6.19 and 6.20 according to the direction of the transformer primary current (I_r). By analyzing the converter equivalent circuit and modes of operation shown in Figure 3.22; when the transformer primary current is positive either S_3 is on or the S_4 is carrying the current form the source to the drain direction, so S_4 is turned on at ZVS. Similarly, when the transformer primary current is negative either S_4 is on or S_3 is carrying the current form the source to the drain direction, therefore S_3 is turned on at ZVS.

Figure 6.21 also shows the gate-to-source voltage (V_{GS}: the yellow signal), and drain-to-source voltage (V_{DS}: the blue signal) for S_4, and the SRC resonant current when operating at 105 kHz for a reduced input voltage with a load of 100 kΩ where the gate signals of the PFC and SRC are 180^o phase shifted. There is an explicit voltage spike at the mid-point of S_4 V_{GS} due to the switching transition of the PFC transistors. That is when S_1 is turned on and S_2 is turned off as shown previously in Figure 6.11. At that moment when S_1 is turned on and S_2 is turned off, the source terminal of the switch S_4 is getting large common mode voltage spike due to the interruption of the inductive current of the input inductor L_s. Therefore, the synchronized gate signals for the PFC and SRC (shown in Figure 6.10) are preferred for the converter operation to avoid this severe gate-to-source voltage spike.

Figure 6.22 depicts the drain-to-source voltages of PFC switches which shows the smooth transition between switch voltages to avoid possible shoot-through or voltage spikes. GaN systems lateral devices do not include intrinsic body diodes, so there is a challenge of getting voltage spikes if the modes of operations have larger dead time periods with no freewheeling paths to conduct any interrupted current. Moreover, the PFC switches drain-to-source voltages and the PFC input current waveforms are shown in Figure 6.23. The PFC input current waveform verifies the low harmonic contents of the converter input stage.

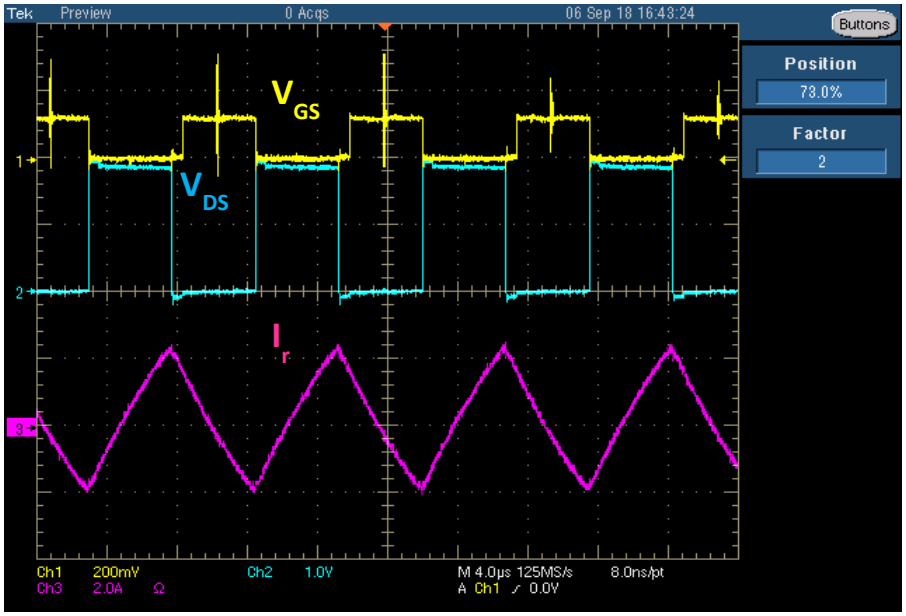


Figure 6.21. S_4 V_{GS} V_{DS}, and I_r waveforms for phase shifted V_{GS} @ R_L = 100 kΩ, 105 kHz.

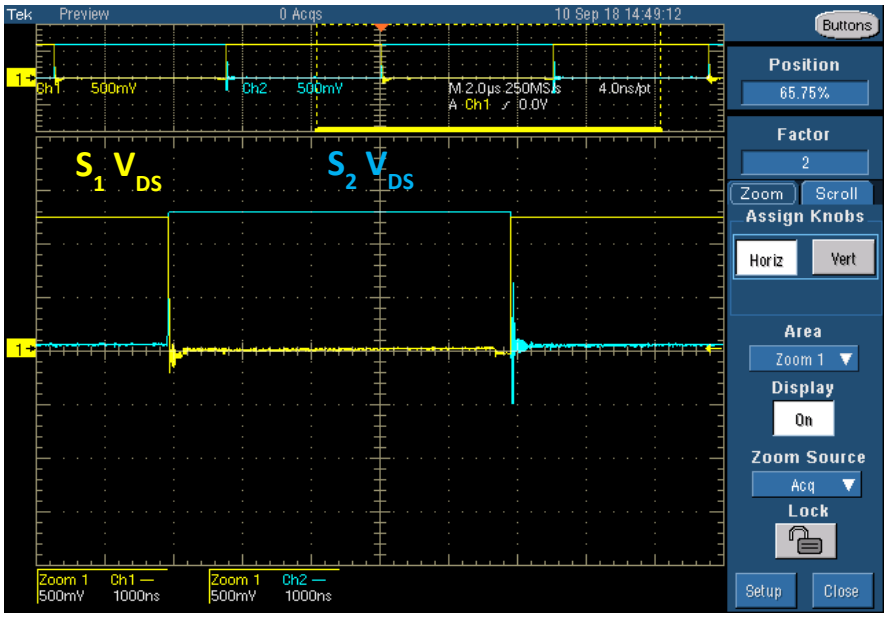


Figure 6.22. S_1 and S_2 V_{DS} waveforms for Vin = 40 V and 2 kΩ @ 105 kHz.

Also, the drain-to-source voltages of SRC switches are presented in Figure 6.24 which shows that there is no short circuit occurred for the converter bridges. Figure 6.25 presents the high-frequency transformer primary and secondary voltages (V_{T1} and V_{T2}), and the primary current (I_r) for an input of 80 V and 2 kΩ load at the switching frequency (105 kHz). The attenuation scale for this measurement is 1:1, hence the transformer primary and secondary measured voltages are 130 V and 100 V as shown.

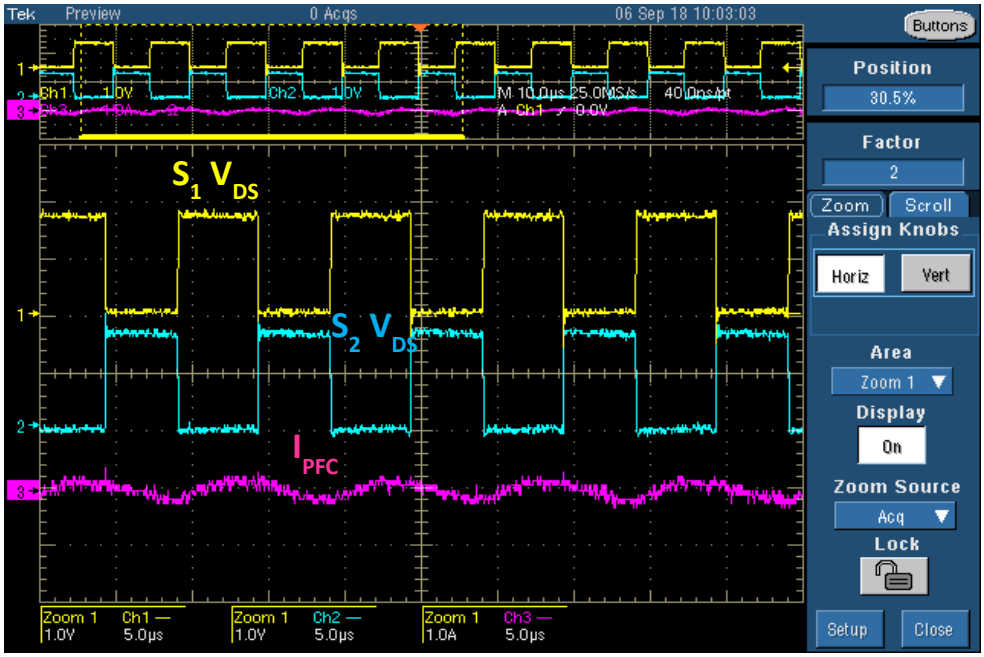


Figure 6.23. S_1 and S_2 V_{DS}, and I_{PFC} waveforms for Vin = 35 V and 100 kΩ @ 100 kHz.

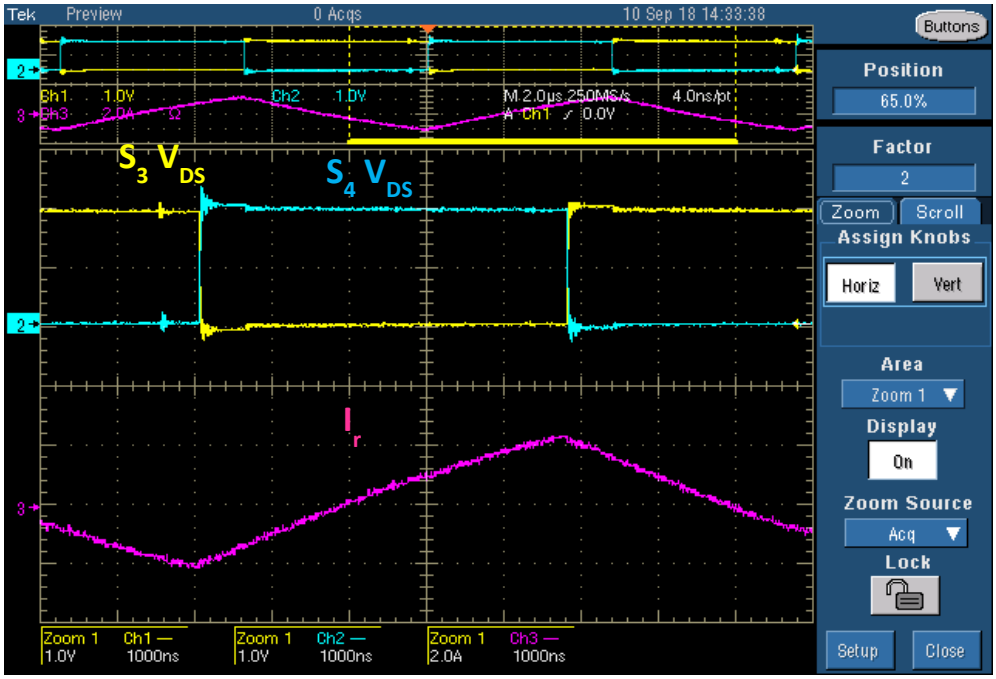


Figure 6.24. S_3 and S_4 V_{DS} and I_r waveforms for Vin = 40 V and 2 kΩ @ 105 kHz.

The secondary voltage (V_{T2}) displays some voltage fluctuations and ringing because of the leakage inductance di/dt effects during the high-current periods, while V_{T2} is pure when the resonant current is close to the zero crossing value. The resonant current slope is positive when the primary and secondary voltages are positive, while the slope of the current is negative for the negative voltages of the transformer.

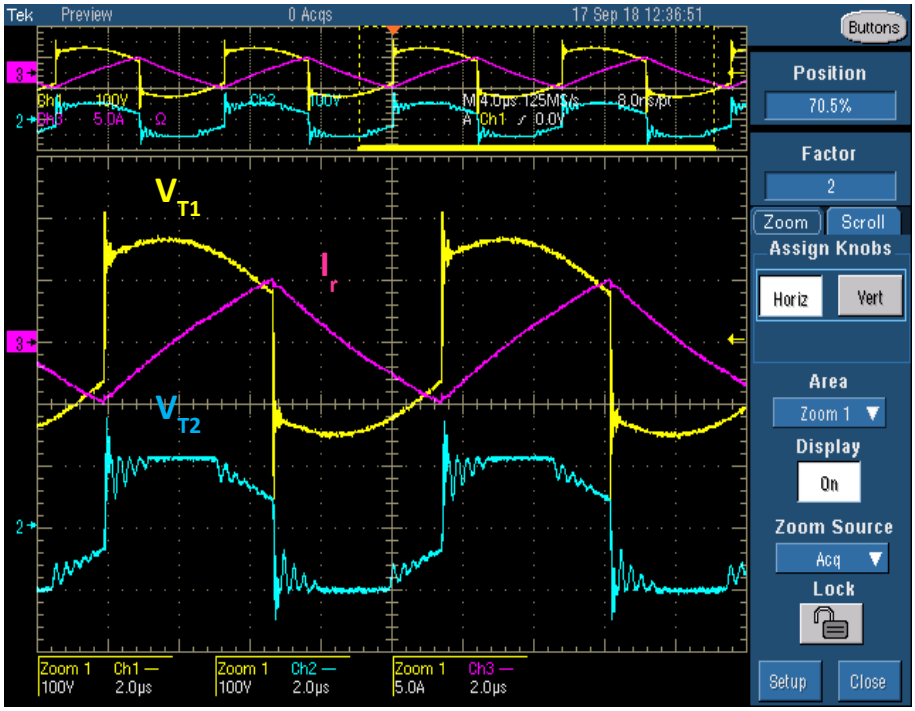


Figure 6.25. V_{T1}, V_{T2}, and I_r waveforms for V_{in} = 80 V and 2 kΩ @ 105 kHz.

Figures 6.26, 6.27, 6.28, and 6.29 show the experimental results for the transformer primary voltage (V_{T1}), output voltage (V_o), and primary current (I_r) by gradually increasing the input voltage with different load resistances when operating the converter at the selected switching frequencies. As series resonant converter (SRC) characteristics depend on the load resistance of the experimental testing and the operating switching frequency, (250 Ω, 1 kΩ, 2 kΩ, and 100 kΩ) load resistances are used for the conducted measurements. Figures 6.26 and 6.29 present the voltage waveforms with the attenuation scale of 1:1, while Figures 6.27 and 6.28 are the voltage waveforms using the P5200 isolated voltage differential probes with an attenuation of 1/50.

So 1 V equals 50 V per the oscilloscope division for all voltage measurements of Figures 6.27 and 6.28. Figure 6.26 shows V_{T1}, V_o, and I_r for a 50 V input voltage and 2 kΩ load, at the resonant switching frequency (105 kHz) which resulted in an output DC voltage of 34 V, while the output DC voltage presented in Figure 6.27 is around 30 V for V_{in} of 60 V and a load of 250 Ω at 72 kHz.

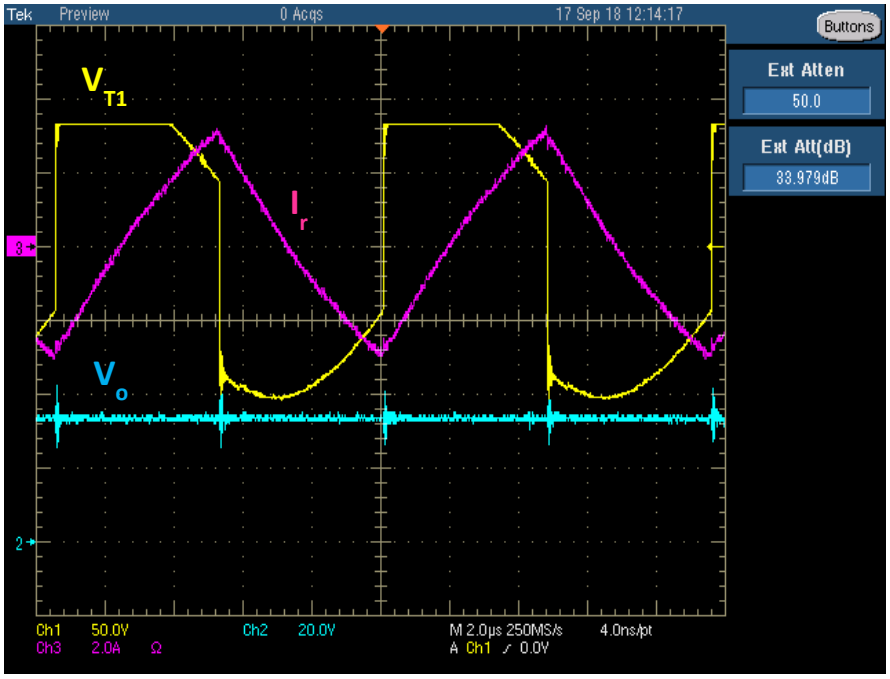


Figure 6.26. V_{T1}, V_o, and I_r waveforms for V_{in} = 50 V and 2 kΩ @ 105 kHz.

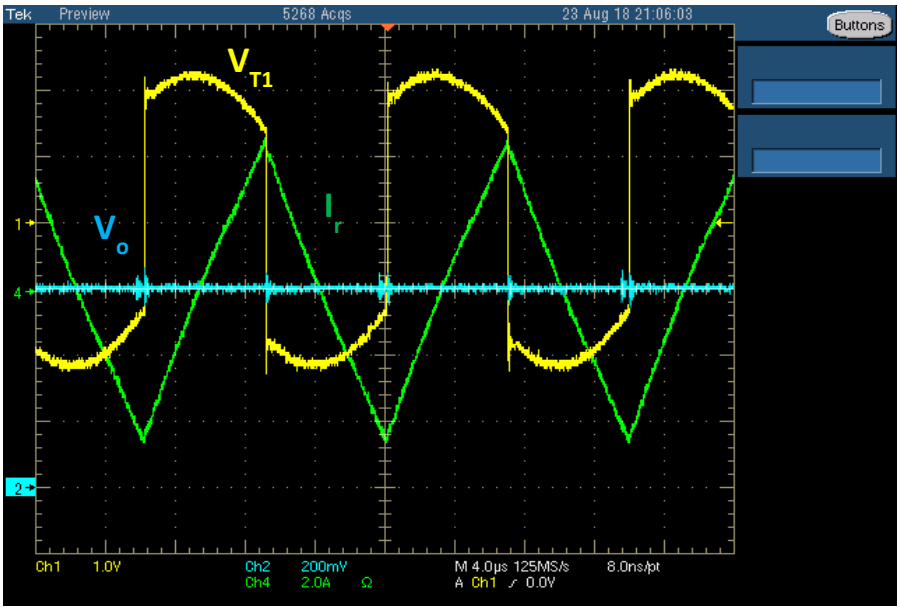


Figure 6.27. V_{T1}, V_o, and I_r waveforms for V_{in} = 60 V and 250 Ω @ 72 kHz.

As can be seen, the higher load resistance at the resonant frequency provided a higher output voltage even with slightly lower input voltage value. Figure 6.28 presents the results for 70 V input voltage and 2 kΩ load at 105 kHz which resulted in an output DC voltage of 47 V. Finally the experimental results for the transformer primary voltage (V_{T1}), output voltage, and primary current (I_r) for an input voltage of 120 V with a large load resistance of 100 kΩ at the resonant

switching frequency is presented in Figure 6.29. The maximum measured output DC voltage for very light load condition at the rated input voltage is around 71 V as shown in Figure 6.29.

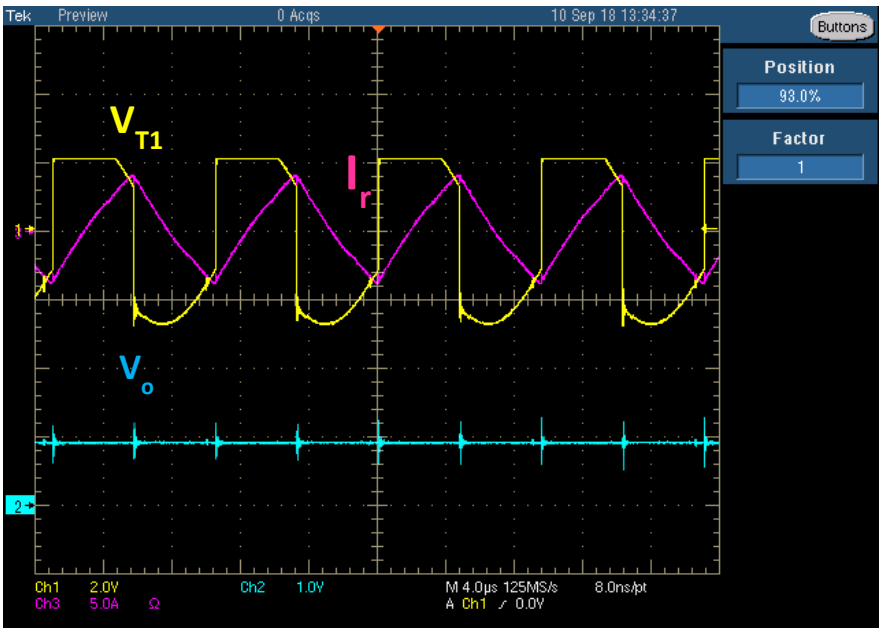


Figure 6.28. V_{T1}, V_o, and I_r waveforms for Vin = 70 V and 2 kΩ @ 105 kHz.

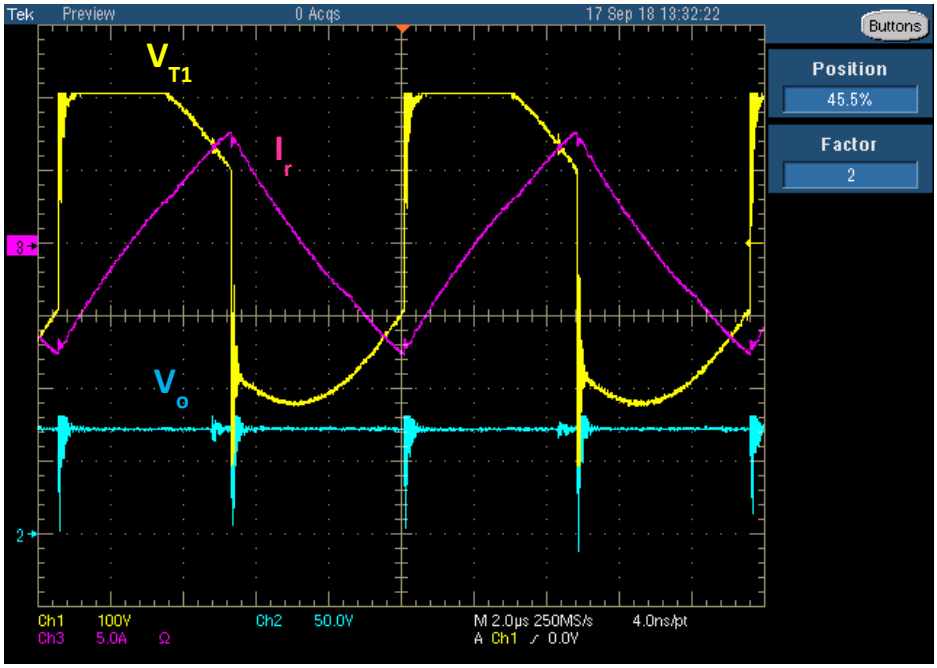


Figure 6.29. V_{T1}, V_o, and I_r waveforms for V_{in} = 120 V and 100 kΩ @ 105 kHz.

Figure 6.30 shows the transformer primary voltage (V_{T1}), output voltage (V_o), and load current (I_o) for an input voltage of 80 V with a 2 kΩ load at 105 kHz. The measured output voltage (V_o) is 40 V and the measured load current (I_o) is around 70 mA for the 2 kΩ load resistance.

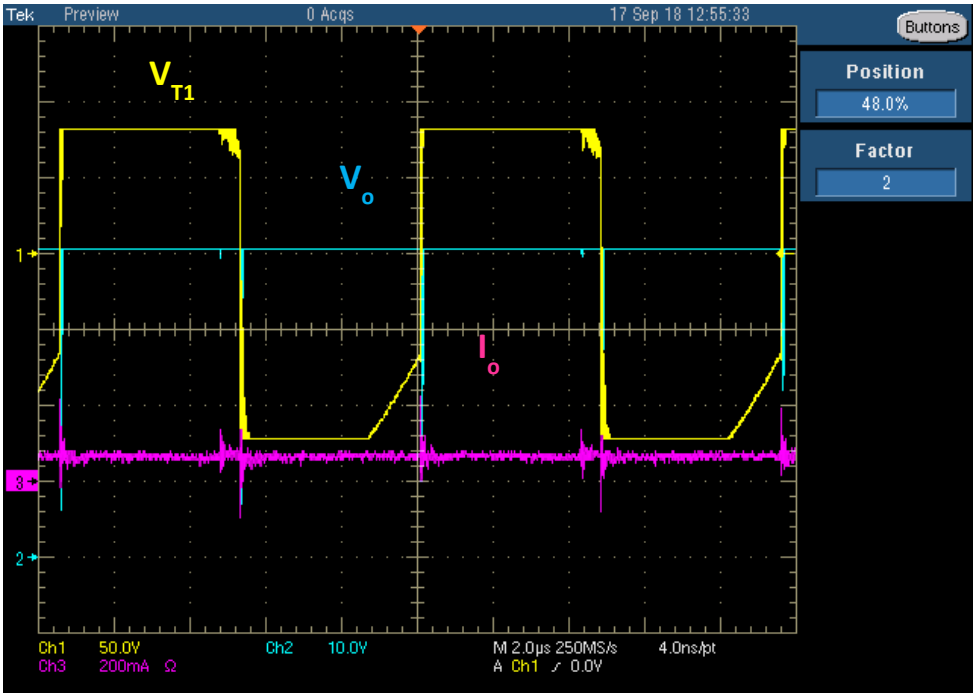


Figure 6.30. V_{T1}, V_o, and I_o waveforms for V_{in} = 80 V and 2 kΩ @ 105 kHz.

At high load resistance less current flows through the CDR coupled inductors L_1 and L_2 (although its common resistance is very low) becuase the common mode inductor only allows the differential signals to flow through as the voltage across the inductor can change instantaneously while its current do not change instantaneously.

6.7 Conclusion

AC/DC power supplies desire higher efficiency high densities power electronics converters utilizing the merits of GaN devices. A GaN-based AC/DC converter is successfully designed and experimentally verified in this Chapter which yields a scaled-down isolated power supply to convert 120 Vac to 48 Vdc/60Vdc switching at 105 kHz. PFC and SRC GaN devices are controlled for PWM soft-switching operation using Silicon Labs Si8273 isolated gate drivers and the TMS320F28335 DSP controller. The gate driver configuration for critical GaN switching requirements is designed and fabricated. Moreover, GaN gate driver design considerations have been addressed and meticulously applied with a quasi-Kelvin source connection in the fabricated 4-layer PCB prototype in order to control Miller effects, minimize

gate ringing, and minimize the parasitics of the pull-down and pull-up loops of the designed layout. The PFC stage converts the 60 Hz AC input to the 300 V DC link to achieve a high power factor with reduced harmonic distortion load for the supply. A SRC operates under soft-switching condition to yield a 105 kHz square-wave voltage for the high-frequency transformer primary winding. Finally the CDR provides the output DC voltage for the converter load. The experimental results verified the desired DSP and gate drivers operation for the control circuit, while the power supply has been applied with 2:1 scale isolation transformer (60 V AC input). The PFC DC voltage (V_{PFC}), the transformer primary voltage (V_{T1}), transformer primary current (I_r or I_p), and CDR output voltage have been measured under varied load conditions. ZVS operation has been demonstrated and verified for the SRC at the above-resonant frequency of 105 kHz.

ZVS has been experimentally verified for the switching frequency of 105 kHz. Since series resonant converter (SRC) characteristics depend on the load resistance and the operating switching frequency, various load resistances are used for the conducted measurements. The dead times for both the PFC and SRC GaN transistors have been adjusted to yield the minimum voltage and current spikes whit PFC signals delay of 30 ns and SRC signals delay of 90 ns. There was an explicit voltage spike at the mid-point of S_4 gate-to-source voltage due to the switching transition of the PFC transistors when S_1 is turned on and S_2 is turned off. Therefore, the synchronized gate signals for the PFC and SRC (shown in Figure 6.10) are preferred for the converter operation to avoid this severe gate-to-source voltage spike. The PFC input current waveform verified the low harmonic contents of the converter input stage, and the transformer output voltage with the CDR verified the voltage regulation capability of the converter. Ground loops are isolated using an isolation transformer for the input AC voltage to separate the oscilloscope probing ground from the converter voltages' ground to obtain the correct measurements. The GaN HEMTs used in the scaled-down protoype (GS66504B) have

maximum operating junction temperature of 150 C^o, so excessive heat dissipation must be avoid during the converter operation. The transformer primary current waveform is triangular because the converter is operating as a regular PWM converter at the the above-resonant continous mode for swtiching frequency of 105 kHz.

6.8 References

[6-1] GaN Systems, GN001 Application Guide, Design with GaN Enhancement mode HEMT, Updated on Feb. 28 2018.

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[6-4] A. M. Elrajoubi and S. S. Ang, "Design and evaluation of a high-current gate driver circuit for six paralleled 1.2kV 36A SiC MOSFETs," 2018 IEEE Power and Energy Conference at Illinois (PECI), Champaign, IL, USA, 2018, pp. 1-8.

[6-5] Silicon Labs Si827x Isolated Gate Drivers Data Sheet available at:

https://www.silabs.com/documents/public/data-sheets/Si827x.pdf

[6-6] A. M. Elrajoubi, K. George and S. S. Ang, "Design and analysis of a new GaN-based AC/DC topology for battery charging application," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, USA, 2018, pp. 2959-2964.

CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

7.1 Introduction

High-density switching converters are being realized with gallium nitride (GaN) power devices due to their high switching speeds that reduce the size of energy-storage circuit components. A new GaN-based power converter utilizing the solid-state transformer (SST) for low power applications is investigated, simulated, and designed in this dissertation. Several advantages have been the motivations for this research including the higher efficiency and fast switching ability of GaN technology, in addition to the reduction in size and volume of the high-frequency (HF) transformer. Moreover, the potential capabilities and functionalities of the SST converters can be combined with the advantages of power factor correction (PFC) rectifier and series resonant converter (SRC) with current doubler rectifier (CDR) to develop a new isolated AC/DC converter. Therefore, the objective of this dissertation is to synthesize the operation of the proposed GaN isolated AC/DC converter to obtain higher efficiency converter due to the zero-voltage-switching operation of all GaN transistors. So, the operation of the PFC and SRC is regulated to achieve full potential and higher performance soft-switching operating conditions. Eventually, the advantages of voltage regulation feature of the solid-state transformer, low harmonics and close-to-unity power factor of the PFC rectifier, soft-switching of the half-bridge SRC, volume reduction of the HF transformer, and smaller leakage inductance of the CDR are offered in this converter topology. CDR is used for low-voltage high-current applications as it draws half of the load current in the transformer secondary side, hence, it yields less copper losses of the transformer secondary winding. The key research conclusions and recommendations for possible future work directions are given in this chapter.

7.2 Dissertation Contributions

High-efficiency, high-density power electronic converters utilizing GaN technology virtues are desired and being analyzed and investigated to develop AC/DC power supplies for several applications. In this dissertation, Chapter 2 gives the literature review of the operation and topologies of the solid-state transformer, and resonant converters soft-switching. Several SST topologies have been reviewed and evaluated for the desired functionalities. SST can provide extra benefits to the distribution grid by offering useful functions such as power flow control, protection monitoring, power factor correction, volume and size reduction, and voltage sag compensation. The designed converter in this dissertation yields a high-efficiency power supply converter assures close-to-unity power factor, low-harmonic distortion (<5%) to convert 120Vac to 48Vdc/60Vdc at 100 kHz for a 1.4 kW application. This GaN AC/DC converter is the simplest topology to yield a low-cost power supply for low-power applications.

The theoretical operation concepts, modeling, and simulation of the proposed GaN AC/DC converter are presented in Chapter 3. The investigated converter topology is extensively simulated in MATLAB and PSpice, and the main simulation waveforms of the proposed converter with the output current and voltage are illustrated for various gate driver duty ratios and switching frequencies. The converter offers the advantages of voltage regulation feature of the solid-state transformer, low harmonics and close-to-unity power factor of the PFC rectifier, soft-switching of the half-bridge SRC, reduced size of high-frequency transformer, and smaller leakage inductance of the CDR which is used for low-voltage high-current applications as the CDR draws half of the load current in the transformer secondary side. Also, state-space analysis for the converter is performed in order to derive the transfer function of the isolated AC/DC converter. Then the closed-loop converter controller is designed, simulated, and discussed. Stability operation of the converter is shown through the sufficient phase margins of the converter frequency response. The frequency response characteristics of the closed-loop PFC

rectifier showed 90º phase margin of the PFC voltage loop gains, and 46.4º phase margin of the PFC current loop gains. However for the SRC with CDR closed-loop stability, the phase margin is 115º for the compensated voltage transfer function. Furthermore, a new equivalent circuit model for the converter is constructed consisting of a loss-free resistor model for the PFC rectifier with first harmonic approximation model for the SRC and the CDR. Positive coupling configuration is used for the CDR model as it yields almost zero current ripple in the output capacitor. The PFC lossless two-port network includes the average power transferred to the dependent power source as drawn. Then the CDR is modeled for positive coupling configuration for the coupled inductor. In the SRC investigated in this dissertation, the output CDR is primarily driven by the resonant tank current, while the output voltage of the CDR is regulated by a voltage feedback controller with a large output capacitor to remove any high-frequency harmonics.

The literature and fundamental steps to design medium and high-frequency transformers are reviewed and explained in Chapter 4, and MATLAB code was applied to obtain the specifications for two different transformers design examples. Amorphous shell-type (25 kHz, 5 kVA, 440/110V) and nanocrystalline toroid core (100 kHz, 350 VA, 130/117V) are used for the demonstrated examples. Served Litz wires were chosen for the transformers windings. Nanocrystalline core yields higher efficiency than amorphous core at 100 kHz or higher frequency, while at 25 kHz their efficiencies are close but the amorphous core is cheaper than nanocrystalline for the same power ratings. A high-frequency nanocrystalline toroid transformer is designed and fabricated to satisfy the performance specifications of the converter. More importantly, a new equation is developed to determine the toroid transformer leakage inductance. The measured value of the fabricated nanocrystalline transformer leakage inductance is 50.31 µH, which verifies the modified equation developed in this work.

The instructions for programming the TMS320F28335 DSP controller using MATLAB Simulink embedded coder tools and then debugging the program in CCS V6 are documented in Chapter 5. MATLAB embedded coder support package for TI C2833x processors provides the required fundamental blocks for any power electronic, smart grid or motor drives applications. This is a new programming methodology to interact between MATLAB and CCS V6 which provides an explanation of the vital steps and settings needed to program the DSP. All basic functions such as pulse width modulation, analog-digital conversion, and proportional-integral controllers are explained and integrated. Also, the target configuration and xMakefile configuration tool directories are presented and explained. Finally, the TMS320F28335 DSP control model for the proposed AC/DC converter topology is developed through MATLAB Simulink embedded coder programming approach and flash memory programming mode.

The fabricated GaN AC/DC converter experimental prototype and measurement results are presented and discussed in Chapter 6. PFC and SRC GaN devices are controlled for PWM soft-switching operation using Silicon Labs Si8273 isolated gate drivers and the TMS320F28335 DSP controller. The gate driver configuration for critical GaN switching requirements is designed and fabricated. Moreover, GaN gate driver design considerations have been addressed and meticulously applied with a quasi-Kelvin source connection in the fabricated 4-layer PCB prototype in order to control Miller effects, minimize gate ringing, and minimize the parasitics of the pull-down and pull-up loops of the designed layout. The scaled-down experimental prototype demonstrated a power supply converter for $120V_{ac}$ to $48V_{dc}/60V_{dc}$ conversion, operating at 105 kHz for various load conditions. The Texas Instruments TMS320F28335 digital signal processor (DSP) is used to generate the required gate driver control signals. Also, the dissertation work includes the experimental prototype fabrication to test and demonstrate the feasibility of the designed 4-layer printed circuit board (PCB) for the GaN AC/DC

converter operation. Simulation and experimental prototype have demonstrated the feasibility of the designed GaN AC/DC converter topology for low power applications. ZVS has been experimentally verified for the above-resonant continous mode of operation at the switching frequency of 105 kHz. Since series resonant converter (SRC) characteristics depend on the load resistance and the operating switching frequency, various load resistances are used for the conducted measurements. The dead times for both the PFC and SRC GaN transistors have been adjusted to yield the minimum voltage and current spikes whit PFC signals delay of 30 ns and SRC signals delay of 90 ns. There was an explicit voltage spike at the mid-point of S_4 gate-to-source voltage due to the switching transition of the PFC transistors when S_1 is turned on and S_2 is turned off. Therefore, the synchronized gate sequence for the PFC and SRC (shown in Figure 6.10) is preferred for the converter operation to avoid this severe gate-to-source voltage spike. The PFC output voltage waveform verified the converter input stage stable rectification, and the CDR output verified the output voltage regulation capability of the converter.

7.3 Dissertation Recommendations for Future Research Work

Although GaN technology has been recently developed and widely studied by many researchers for emerging electric power systems and power electronics applications, there are still many challenges needed to be carefully addressed, analyzed and investigated. The work presented in this dissertation could be extended per the following recommendations and possible directions for future work.

First, the work in Chapter 3 needs to be extended and developed to find out more about the proposed converter optimum controller strategies in order to achieve higher efficiency operation conditions. Moreover, the small signal model should be derived and developed for the proposed and designed GaN AC/DC converter.

Secondly, there are more objectives for designing an optimized high-frequency transformer which would potentially improve the converter performance and resonant operation. Nanocrystalline toroid core transformer (100 kHz, 350 VA, 130/117V) is designed and built for the demonstrated converter experimental prototype. It is very attractive and practical to balance the transformer design tradeoff to achieve the desired optimal design regarding the cost, efficiency, volume, and layout configuration for higher frequency operation with smaller leakage inductance value. Interleaving winding arrangements to utilize the transformer leakage inductance targeting 500 kHz as the converter resonant frequency is recommended. Moreover, for different toroid core sizes, more accurate estimate for the leakage inductance should be obtained and derived by finite element analysis and simulations.

Also, this dissertation has presented the designed AC/DC converter control strategy and the methodology for programming the TMS320F28335 DSP controller using MATLAB Simulink embedded coder. However, programming the TMS320F28335 DSP controller for the designed AC/DC converter control strategies is challenging and there are some operating conditions and constraints on this approach that will need to be further investigated.

Furthermore, electromagnetic interference (EMI) issues have not been addressed in this work for the GaN isolated AC/DC converter. Therefore, the EMI aspect could be considered to mitigate their effects on the designed GaN converter and its performance.

Finally, the experiments provided valuable insights into the operation of the designed converter. So the future research work should consider the experimental testing which needs more advanced measurements, like measuring the converter efficiency with an appropriate laboratory power analyzer, and verifying the converter stability for transient responses through input voltage or load change.

Appendix A: MATLAB Code for HF Transformer Design Example 1.

```
% FOR HIGH-FREQUENCY TRANSFORMER DESIGN. Example #1
% Includes General and Improved Steinmetz Equations for non-sinusoidal excitation

clc
%Specifications for Amorphous core.
phase=1;              %Phase of input signal
Pout=5000/phase;  %Output Power in VA (EX - 15000VA/phase)
n=0.98;               %Desired Efficiency (EX 0.98 = 98%)
Pin=Pout/n;          %Input Power (VA)
SVA=Pin+Pout;     %Sum of input power and output power
Vp=440;               %Primary voltage (V)
Vs=110;               %Secondary voltage (V)
Ip=11.36;            %Primary current (A)
Is=45.45;            %Secondary Current (A)
f=25000;             %Frequency (Hz)
T=1/f;               %Period (s)
DT=70;              %Temperature rise (C)
D=0.5;              %Duty Cycle

%Coefficients and dimensional parameters , typical values.
hc=10;               %Coefficient of heat transfer 10W/m^2C for natural convection. Up to 30W/m^2C
ka=40;               %Dimensionless Quantity See page 61
kw=10;               %Dimensionless Quantity See page 61
kc=5.6;              %Dimensionless Quantity See page 61
Kv=4;                %Waveform Excitation (Square wave=4 / Sinusoidal=4.44)
kf=0.95;             %Core stacking factor
ku=0.4;              %Window utilization factor (recommended 40% of window area)
phiw=1.72e-8;      %(ohm*m) initial wire resistivity for flux density and area product calculations
Kt=(hc*ka/(phiw*kw))^0.5;   %48.2x10^3 eq. 3.29 page 61

% Amorphous Core Parameters
Kc=1.3617;          %Coefficient of the Steinmentz equation in (W/m3)
alpha=1.51;         %Coefficient of the Steinmentz equation
beta=1.74;          %Coefficient of the Steinmentz equation
Bsat=1.56;          %Maximum flux density before saturation
ki = Kc/(2^(beta-1)*pi^(alpha-1)*(1.1044+(6.8244/(alpha+1.354)))); %Improved General Steinmetz Equation
Constant, k1 (Hurley P.204)

%Optimum Flux Density
Bop=(((hc*ka*DT)^(2/3))./((1.5874).*((phiw*kw*ku)^(1/12)).*(kc*Kc.*f.^alpha).^(7/12))).*((Kv.*f.*kf*ku./S
VA).^(1/6))   %Teslas (T) (Hurley P.126)

Bop=0.19      %Introduce a different value when the optimum is not desired
DB=2*Bop;   %Peak to Peak Flux Density
Llk_Desired=Vp^2/(8*f*Pout)  % approximation for desired leakage inductance Llk at Maximum.

%Optimum Area Product
Ap=(((sqrt(2))*SVA./(Kv.*f.*Bop*kf*Kt.*((ku*DT).^(0.5)))).^(8/7))*1e8 %(cm^4)(Hurley P.125)

%Core Dimensions (Amorphous C-Core AMCC-63) from data sheet.
c=1;                %number of cores needed to complete the optimum Ap /shell-core
w = 3*c;          %total width (cm)
hwa = 7;          %height of window area (cm)
lw=2;               %length of the window area (cm)
lc=5.2;             %length of the core (cm)
l = 0.5*(lc-lw);   %length of cross sectional area (cm)
```

```
lm=25.3*2;          %mean length of the core (cm)
Ac = 3.9*2;         % ~= 2*l*w Cross sectional area of shell-core (cm^2)
Wa = lw*hwa;        %Window Area (cm^2)
m = 703*c*2;        %mass of core (x2 if shell type)(grams)
density = 7.18;     %(g/cm^3)
Ap = Wa*Ac          %Area product (cm^4)
Apm = Ap/(100^4);  %Area product (m^4)

%Current Density Calculation
J = (((hc*ka*DT)/(2*phiw*kw*ku))^(1/2))*(1/(Apm^(1/8)))/(100^2) % Primary Current Density (A/cm^2)
page 125

%Number of turns for primary and secondary
Np = Vp./(Kv.*Bop.*kf*Ac*(10^-4)*f)     %Number of turns primary Eq.5.15 pg. 128
Np=ceil(Np)
Ns = Np*(Vs/Vp)                 %Number of turns secondary
MLT = (2*w)+2*(2*l)+(lw*0.8)*(2+pi) %  Mean Length Per turn (cm) McLyman eq. 4-23 and Design
Optimization (K.D. Hoang)(2*l for shell-type xfmr)
% Eq. 4-24 McLyman for Toroid Core MLT.

%Volume
Vw=MLT*Wa;    %Volume of the windings cm^3
Vc=lm*Ac;         %Volume of the core cm^3
Vt=Vw+Vc          %total volume in cm^3
Vtd=(1e-3).*Vt;   %  in dm^3
Vtm=(1e-6)*Vt;    %in m^3

%Volume based on Ap
% Vw=kw.*Ap.^(3/4) %Volume of the windings
% Vc=kc.*Ap.^(3/4) %Volume of the core
% Vt=Vw+Vc   %total volume in cm^3
% Vtd=(1e-3).*Vt; % in dm^3
% Vtm=(1e-6).*Vt; %in m^3

%Leakage Inductance for the Shell-type core
Lkp=(4*pi*10^-7).*(Np^2).*MLT*hwa*(10^-2)/(3*lw) %  lw: winding width Design Optimization (K.D.
Hoang)
Lks=(4*pi*10^-7).*(Ns^2).*MLT*hwa*(10^-2)/(3*lw)
Lm= (4*pi*10^-7)*15000*(Np)^2*Ac/(lm*100)  %  Magnetizing Inductance in H.

%Copper winding dimension calculations
skin = 6.62/(sqrt(f));    % radius of skin effect (also the radius of desired wire)(cm), McLyman eq. 4-5
dskin = 2*skin            % maximum diameter of each strand  (cm)
Askin = pi*skin^2;        % ideal copper cross sectional area (cm^2)
PCA = Ip/J                % Primary conduction Area of windings (cm^2)to choose the wire equivalent size.
SCA = Is/J                % Secondary conduction Area of windings (cm^2)

%Copper Winding selection data (assuming litz wire with n # of strands)
Aw = 0.000509;          %Cross Sectional Area of each strand (cm^2) AWG strand # 30
rho = 3386;             %Wire (of particular gauge) resistance per length (µOhm/cm)

PS = round(PCA/Aw)        %IDEAL Primary strands in litz wire
SS = round(SCA/Aw)        %IDEAL Secondary strands in litz wire
rhop = rho/PS;            %Primary Resistance per cm (µOhm/cm)
rhos = rho/SS;            %Secondary resistance per cm (µOhm/cm)
RP = rhop*Np*MLT*(10^-6)  %Total Primary Resistance (Ohm)
RS = rhos*Ns*MLT*(10^-6)  %Total Secondary Resistance (Ohm)
```

```
%Window utilization factor check
Wap=PS*Np*Aw              % Window area of primary winding (cm^2)
Was=SS*Ns*Aw              % Window area of secondary winding (cm^2)
kux=(Wap+Was)/Wa          % Total window utilization

%Copper Losses
Pcup = RP*(Ip^2);         %Primary Copper Losses(W)
Pcus = RS*(Is^2);         %Secondary Copper Losses (W)
Pcu = Pcup + Pcus         %Total Copper Losses (W)

%Core Losses per Unit Volume
Pv = Kc*(f^alpha)*(Bop^beta);         %Losses per unit volume (General Steinmetz Equation) (W/m^3)
Pvi = ki*(DB^(beta-alpha))*(1/T)*(2*DB^alpha*(D*T)^(1-alpha));    %Losses per unit volume (Improved
Steinmetz Equation) (W/m^3)(Hurley P.205)

%Core Losses
Pfe = Vtm*Pv;      %Total core losses (General Steinmetz Equation) (W)
Pfei = Vtm*Pvi     %Total core losses (Improved Steinmetz Equation) (W)

%TOTAL LOSSES
Ptot = Pfe + Pcu;         %TOTAL LOSSES (GENERAL STEINMETZ EQUATION) (W)
Ptoti = Pfei + Pcu        %TOTAL LOSSES (IMPROVED STEINMETZ EQUATION) (W)

%Efficiency
Eff = Pout/(Pout + Ptot);      %Efficiency (%)(GENERAL STEINMETZ EQUATION)
Effi = Pout/(Pout + Ptoti)     %Efficiency (Improved Steinmetz Equation) (%)

% Temperature Rise and Isolation Level check
Eins=16;      % Dielectric Strength of the Isolation material in KV/mm.
Vins=2;       % Voltage Required to be isolated in KV.
vv=0.41;      % Safe margin parameter , from Isolation material datasheet.
dins=Vins/(vv*Eins); % Minimum Distance for Isolation in mm.

%Temperature Rise and Isolation distance
Ks=39.2;                %For C core Table 5-4 McLyman
At=Ks*(Ap)^0.5      %Surface area (cm^2)Eq. 5-30 McLyman
Pdis=Ptoti/At;          %power dissipated per unit area (W/cm^2)Eq. 6-17
Tr=450*(Pdis)^0.826  %Temperature rise (C) Eq. 6-19 McLyman
dins=Vins/(vv*Eins)  %Minimum isolation distance between primary and secondary windings (mm) (Optimized
design of Medium Freq. Trans _Ortiz)
```

Appendix B: TMS320F28335 DSP C Code for the AC/DC converter model.

File: ert_main.c

```
1  /*
2  * Academic License - for use in teaching, academic research, and meeting
3  * course requirements at degree granting institutions only. Not for
4  * government, commercial, or other organizational use.
5  *
6  * File: ert_main.c
7  *
8  * Code generated for Simulink model 'APEC_Topology_Model_V12_105KHz'.
9  *
10 * Model version : 1.25
11 * Simulink Coder version : 8.12 (R2017a) 16-Feb-2017
12 * C/C++ source code generated on : Mon Sep 17 21:37:53 2018
13 *
14 * Target selection: ert.tlc
15 * Embedded hardware selection: Texas Instruments->C2000
16 * Code generation objectives: Unspecified
17 * Validation result: Not run
18 */
19
20 #include "APEC_Topology_Model_V12_105KHz.h"
21 #include "rtwtypes.h"
22
23 volatile int IsrOverrun = 0;
24 static boolean_T OverrunFlag = 0;
25 void rt_OneStep(void)
26 {
27 /* Check for overrun. Protect OverrunFlag against preemption */
```

```
28  if (OverrunFlag++) {
29  IsrOverrun = 1;
30  OverrunFlag--;
31  return;
32  }
33
34  enableTimer0Interrupt();
35  APEC_Topology_Model_V12_105KHz_step();
36
37  /* Get model outputs here */
38  disableTimer0Interrupt();
39  OverrunFlag--;
40  }
41
42  int main(void)
43  {
44  volatile boolean_T runModel = 1;
45  float modelBaseRate = 0.5;
46  float systemClock = 150;
47  c2000_flash_init();
48  init_board();
49
50  #ifdef MW_EXEC_PROFILER_ON
51
52  config_profilerTimer();
53
54  #endif
55
56  ;
```

```
57  rtmSetErrorStatus(APEC_Topology_Model_V12_105K_M, 0);
58  APEC_Topology_Model_V12_105KHz_initialize();
59  configureTimer0(modelBaseRate, systemClock);
60  runModel =
61  rtmGetErrorStatus(APEC_Topology_Model_V12_105K_M) == (NULL);
62  enableTimer0Interrupt();
63  globalInterruptEnable();
64  while (runModel) {
65  runModel =
66  rtmGetErrorStatus(APEC_Topology_Model_V12_105K_M) == (NULL);
67  }
68
69  /* Disable rt_OneStep() here */
70
71  /* Terminate model */
72  APEC_Topology_Model_V12_105KHz_terminate();
73  globalInterruptDisable();
74  return 0;
75  }
76
77  /*
78  * File trailer for generated code.
79  * [EOF]
```

File: APEC_Topology_Model_V12_105KHz.c

```
1   /*
2   * Academic License - for use in teaching, academic research, and meeting
3   * course requirements at degree granting institutions only. Not for
4   * government, commercial, or other organizational use.
5   *
```

```
6  * File: APEC_Topology_Model_V12_105KHz.c
7  *
8  * Code generated for Simulink model 'APEC_Topology_Model_V12_105KHz'.
9  *
10 * Model version : 1.25
11 * Simulink Coder version : 8.12 (R2017a) 16-Feb-2017
12 * C/C++ source code generated on : Mon Sep 17 21:37:53 2018
13 *
14 * Target selection: ert.tlc
15 * Embedded hardware selection: Texas Instruments->C2000
16 * Code generation objectives: Unspecified
17 * Validation result: Not run
18 */
19
20 #include "APEC_Topology_Model_V12_105KHz.h"
21 #include "APEC_Topology_Model_V12_105KHz_private.h"
22
23 /* Real-time model */
24 RT_MODEL_APEC_Topology_Model__T APEC_Topology_Model_V12_105K_M_;
25 RT_MODEL_APEC_Topology_Model__T *const APEC_Topology_Model_V12_105K_M =
26 &APEC_Topology_Model_V12_105K_M_;
27
28 /* Model step function */
29 void APEC_Topology_Model_V12_105KHz_step(void)
30 {
31 /* S-Function (c280xgpio_do): '<Root>/Digital Output' incorporates:
32 * Constant: '<Root>/Constant'
33 */
34 {
```

```
35  GpioDataRegs.GPBTOGGLE.bit.GPIO34 =
36  (APEC_Topology_Model_V12_105KH_P.Constant_Value != 0);
37  }
38  }
39
40  /* Model initialize function */
41  void APEC_Topology_Model_V12_105KHz_initialize(void)
42  {
43  /* Registration code */
44
45  /* initialize error status */
46  rtmSetErrorStatus(APEC_Topology_Model_V12_105K_M, (NULL));
47
48  /* Start for S-Function (c280xgpio_do): '<Root>/Digital Output' incorporates:
49  * Constant: '<Root>/Constant'
50  */
51  EALLOW;
52  GpioCtrlRegs.GPBMUX1.all &= 0xFFFFFFCF;
53  GpioCtrlRegs.GPBDIR.all |= 0x4;
54  EDIS;
55
56  /* Start for S-Function (c280xpwm): '<Root>/ePWM1' */
57
58  /*** Initialize ePWM1 modules ***/
59  {
60  /*-- Setup Time-Base (TB) Submodule --*/
61  EPwm1Regs.TBPRD = 714;
62
63  /* // Time-Base Control Register
```

```
64  EPwm1Regs.TBCTL.bit.CTRMODE = 2; // Counter Mode
65  EPwm1Regs.TBCTL.bit.SYNCOSEL = 3; // Sync output select
66  EPwm1Regs.TBCTL.bit.PRDLD = 0; // Shadow select
67  EPwm1Regs.TBCTL.bit.PHSEN = 0; // Phase load enable
68  EPwm1Regs.TBCTL.bit.PHSDIR = 0; // Phase Direction
69  EPwm1Regs.TBCTL.bit.HSPCLKDIV = 0; // High speed time pre-scale
70  EPwm1Regs.TBCTL.bit.CLKDIV = 0; // Timebase clock pre-scale
71  */
72  EPwm1Regs.TBCTL.all = (EPwm1Regs.TBCTL.all & ~0x3FBF) | 0x32;
73
74  /* // Time-Base Phase Register
75  EPwm1Regs.TBPHS.half.TBPHS = 0; // Phase offset register
76  */
77  EPwm1Regs.TBPHS.all = (EPwm1Regs.TBPHS.all & ~0xFFFF0000) | 0x0;
78  EPwm1Regs.TBCTR = 0x0000; /* Clear counter*/
79
80  /*-- Setup Counter_Compare (CC) Submodule --*/
81  /* // Counter-Compare Control Register
82  EPwm1Regs.CMPCTL.bit.SHDWAMODE = 0; // Compare A block operating mode.
83  EPwm1Regs.CMPCTL.bit.SHDWBMODE = 0; // Compare B block operating mode.
84  EPwm1Regs.CMPCTL.bit.LOADAMODE = 0; // Active compare A
85  EPwm1Regs.CMPCTL.bit.LOADBMODE = 0; // Active compare A
86  */
87  EPwm1Regs.CMPCTL.all = (EPwm1Regs.CMPCTL.all & ~0x5F) | 0x0;
88  EPwm1Regs.CMPA.half.CMPA = 357;
89  EPwm1Regs.CMPB = 357;
90
91  /*-- Setup Action-Qualifier (AQ) Submodule --*/
92  EPwm1Regs.AQCTLA.all = 96;
```

```
93  EPwm1Regs.AQCTLB.all = 144;
94
95  /* // Action-Qualifier Software Force Register
96  EPwm1Regs.AQSFRC.bit.RLDCSF = 0; // Reload from Shadow options
97  */
98  EPwm1Regs.AQSFRC.all = (EPwm1Regs.AQSFRC.all & ~0xC0) | 0x0;
99
100 /* // Action-Qualifier Continuous S/W Force Register Set
101 EPwm1Regs.AQCSFRC.bit.CSFA = 0; // Continuous Software Force on output A
102 EPwm1Regs.AQCSFRC.bit.CSFB = 0; // Continuous Software Force on output B
103 */
104 EPwm1Regs.AQCSFRC.all = (EPwm1Regs.AQCSFRC.all & ~0xF) | 0x0;
105
106 /*-- Setup Dead-Band Generator (DB) Submodule --*/
107 /* // Dead-Band Generator Control Register
108 EPwm1Regs.DBCTL.bit.OUT_MODE = 3; // Dead Band Output Mode Control
109 EPwm1Regs.DBCTL.bit.IN_MODE = 0; // Dead Band Input Select Mode Control
110 EPwm1Regs.DBCTL.bit.POLSEL = 2; // Polarity Select Control
111 */
112 EPwm1Regs.DBCTL.all = (EPwm1Regs.DBCTL.all & ~0x3F) | 0xB;
113 EPwm1Regs.DBRED = 35;
114 EPwm1Regs.DBFED = 35;
115
116 /*-- Setup Event-Trigger (ET) Submodule --*/
117 /* // Event-Trigger Selection and Event-Trigger Pre-Scale Register
118 EPwm1Regs.ETSEL.bit.SOCAEN = 0; // Start of conversion A Enable
119 EPwm1Regs.ETSEL.bit.SOCASEL = 1; // Start of conversion A Select
120 EPwm1Regs.ETPS.bit.SOCAPRD = 1; // EPWM1SOCA Period Select
121 EPwm1Regs.ETSEL.bit.SOCBEN = 0; // Start of conversion B Enable
```

```
122  EPwm1Regs.ETSEL.bit.SOCBSEL = 1; // Start of conversion B Select
123  EPwm1Regs.ETPS.bit.SOCBPRD = 1; // EPWM1SOCB Period Select
124  EPwm1Regs.ETSEL.bit.INTEN = 0; // EPWM1INTn Enable
125  EPwm1Regs.ETSEL.bit.INTSEL = 1; // EPWM1INTn Select
126  EPwm1Regs.ETPS.bit.INTPRD = 1; // EPWM1INTn Period Select
127  */
128  EPwm1Regs.ETSEL.all = (EPwm1Regs.ETSEL.all & ~0xFF0F) | 0x1101;
129  EPwm1Regs.ETPS.all = (EPwm1Regs.ETPS.all & ~0x3303) | 0x1101;
130
131  /*-- Setup PWM-Chopper (PC) Submodule --*/
132  /* // PWM-Chopper Control Register
133  EPwm1Regs.PCCTL.bit.CHPEN = 0; // PWM chopping enable
134  EPwm1Regs.PCCTL.bit.CHPFREQ = 0; // Chopping clock frequency
135  EPwm1Regs.PCCTL.bit.OSHTWTH = 0; // One-shot pulse width
136  EPwm1Regs.PCCTL.bit.CHPDUTY = 0; // Chopping clock Duty cycle
137  */
138  EPwm1Regs.PCCTL.all = (EPwm1Regs.PCCTL.all & ~0x7FF) | 0x0;
139
140  /*-- Set up Trip-Zone (TZ) Submodule --*/
141  EALLOW;
142  EPwm1Regs.TZSEL.all = 0;
143
144  /* // Trip-Zone Control Register
145  EPwm1Regs.TZCTL.bit.TZA = 3; // TZ1 to TZ6 Trip Action On EPWM1A
146  EPwm1Regs.TZCTL.bit.TZB = 3; // TZ1 to TZ6 Trip Action On EPWM1B
147  */
148  EPwm1Regs.TZCTL.all = (EPwm1Regs.TZCTL.all & ~0xF) | 0xF;
149
150  /* // Trip-Zone Enable Interrupt Register
```

```
151  EPwm1Regs.TZEINT.bit.OST = 0; // Trip Zones One Shot Int Enable
152  EPwm1Regs.TZEINT.bit.CBC = 0; // Trip Zones Cycle By Cycle Int Enable
153  */
154  EPwm1Regs.TZEINT.all = (EPwm1Regs.TZEINT.all & ~0x6) | 0x0;
155  EDIS;
156  }
157
158  /* Start for S-Function (c280xpwm): '<Root>/ePWM2' */
159
160  /*** Initialize ePWM2 modules ***/
161  {
162  /*-- Setup Time-Base (TB) Submodule --*/
163  EPwm2Regs.TBPRD = 714;
164
165  /* // Time-Base Control Register
166  EPwm2Regs.TBCTL.bit.CTRMODE = 2; // Counter Mode
167  EPwm2Regs.TBCTL.bit.SYNCOSEL = 3; // Sync output select
168  EPwm2Regs.TBCTL.bit.PRDLD = 0; // Shadow select
169  EPwm2Regs.TBCTL.bit.PHSEN = 0; // Phase load enable
170  EPwm2Regs.TBCTL.bit.PHSDIR = 0; // Phase Direction
171  EPwm2Regs.TBCTL.bit.HSPCLKDIV = 0; // High speed time pre-scale
172  EPwm2Regs.TBCTL.bit.CLKDIV = 0; // Timebase clock pre-scale
173  */
174  EPwm2Regs.TBCTL.all = (EPwm2Regs.TBCTL.all & ~0x3FBF) | 0x32;
175
176  /* // Time-Base Phase Register
177  EPwm2Regs.TBPHS.half.TBPHS = 0; // Phase offset register
178  */
179  EPwm2Regs.TBPHS.all = (EPwm2Regs.TBPHS.all & ~0xFFFF0000) | 0x0;
```

```
180  EPwm2Regs.TBCTR = 0x0000; /* Clear counter*/
181
182  /*-- Setup Counter_Compare (CC) Submodule --*/
183  /* // Counter-Compare Control Register
184  EPwm2Regs.CMPCTL.bit.SHDWAMODE = 0; // Compare A block operating mode.
185  EPwm2Regs.CMPCTL.bit.SHDWBMODE = 0; // Compare B block operating mode.
186  EPwm2Regs.CMPCTL.bit.LOADAMODE = 0; // Active compare A
187  EPwm2Regs.CMPCTL.bit.LOADBMODE = 0; // Active compare A
188  */
189  EPwm2Regs.CMPCTL.all = (EPwm2Regs.CMPCTL.all & ~0x5F) | 0x0;
190  EPwm2Regs.CMPA.half.CMPA = 357;
191  EPwm2Regs.CMPB = 357;
192
193  /*-- Setup Action-Qualifier (AQ) Submodule --*/
194  EPwm2Regs.AQCTLA.all = 96;
195  EPwm2Regs.AQCTLB.all = 264;
196
197  /* // Action-Qualifier Software Force Register
198  EPwm2Regs.AQSFRC.bit.RLDCSF = 0; // Reload from Shadow options
199  */
200  EPwm2Regs.AQSFRC.all = (EPwm2Regs.AQSFRC.all & ~0xC0) | 0x0;
201
202  /* // Action-Qualifier Continuous S/W Force Register Set
203  EPwm2Regs.AQCSFRC.bit.CSFA = 0; // Continuous Software Force on output A
204  EPwm2Regs.AQCSFRC.bit.CSFB = 0; // Continuous Software Force on output B
205  */
206  EPwm2Regs.AQCSFRC.all = (EPwm2Regs.AQCSFRC.all & ~0xF) | 0x0;
207
208  /*-- Setup Dead-Band Generator (DB) Submodule --*/
```

```
209  /* // Dead-Band Generator Control Register
210  EPwm2Regs.DBCTL.bit.OUT_MODE = 3; // Dead Band Output Mode Control
211  EPwm2Regs.DBCTL.bit.IN_MODE = 0; // Dead Band Input Select Mode Control
212  EPwm2Regs.DBCTL.bit.POLSEL = 2; // Polarity Select Control
213  */
214  EPwm2Regs.DBCTL.all = (EPwm2Regs.DBCTL.all & ~0x3F) | 0xB;
215  EPwm2Regs.DBRED = 120;
216  EPwm2Regs.DBFED = 120;
217
218  /*-- Setup Event-Trigger (ET) Submodule --*/
219  /* // Event-Trigger Selection and Event-Trigger Pre-Scale Register
220  EPwm2Regs.ETSEL.bit.SOCAEN = 0; // Start of conversion A Enable
221  EPwm2Regs.ETSEL.bit.SOCASEL = 1; // Start of conversion A Select
222  EPwm2Regs.ETPS.bit.SOCAPRD = 1; // EPWM2SOCA Period Select
223  EPwm2Regs.ETSEL.bit.SOCBEN = 0; // Start of conversion B Enable
224  EPwm2Regs.ETSEL.bit.SOCBSEL = 1; // Start of conversion B Select
225  EPwm2Regs.ETPS.bit.SOCBPRD = 1; // EPWM2SOCB Period Select
226  EPwm2Regs.ETSEL.bit.INTEN = 0; // EPWM2INTn Enable
227  EPwm2Regs.ETSEL.bit.INTSEL = 1; // EPWM2INTn Select
228  EPwm2Regs.ETPS.bit.INTPRD = 1; // EPWM2INTn Period Select
229  */
230  EPwm2Regs.ETSEL.all = (EPwm2Regs.ETSEL.all & ~0xFF0F) | 0x1101;
231  EPwm2Regs.ETPS.all = (EPwm2Regs.ETPS.all & ~0x3303) | 0x1101;
232
233  /*-- Setup PWM-Chopper (PC) Submodule --*/
234  /* // PWM-Chopper Control Register
235  EPwm2Regs.PCCTL.bit.CHPEN = 0; // PWM chopping enable
236  EPwm2Regs.PCCTL.bit.CHPFREQ = 0; // Chopping clock frequency
237  EPwm2Regs.PCCTL.bit.OSHTWTH = 0; // One-shot pulse width
```

```
238  EPwm2Regs.PCCTL.bit.CHPDUTY = 0; // Chopping clock Duty cycle
239  */
240  EPwm2Regs.PCCTL.all = (EPwm2Regs.PCCTL.all & ~0x7FF) | 0x0;
241
242  /*-- Set up Trip-Zone (TZ) Submodule --*/
243  EALLOW;
244  EPwm2Regs.TZSEL.all = 0;
245
246  /* // Trip-Zone Control Register
247  EPwm2Regs.TZCTL.bit.TZA = 3; // TZ1 to TZ6 Trip Action On EPWM2A
248  EPwm2Regs.TZCTL.bit.TZB = 3; // TZ1 to TZ6 Trip Action On EPWM2B
249  */
250  EPwm2Regs.TZCTL.all = (EPwm2Regs.TZCTL.all & ~0xF) | 0xF;
251
252  /* // Trip-Zone Enable Interrupt Register
253  EPwm2Regs.TZEINT.bit.OST = 0; // Trip Zones One Shot Int Enable
254  EPwm2Regs.TZEINT.bit.CBC = 0; // Trip Zones Cycle By Cycle Int Enable
255  */
256  EPwm2Regs.TZEINT.all = (EPwm2Regs.TZEINT.all & ~0x6) | 0x0;
257  EDIS;
258  }
259  }
260
261  /* Model terminate function */
262  void APEC_Topology_Model_V12_105KHz_terminate(void)
263  {
264  /* (no terminate code required) */
265  }
266
```

```
267  /*
268   * File trailer for generated code.
269   *
270   * [EOF]
271   */
```

File: APEC_Topology_Model_V12_105KHz.h

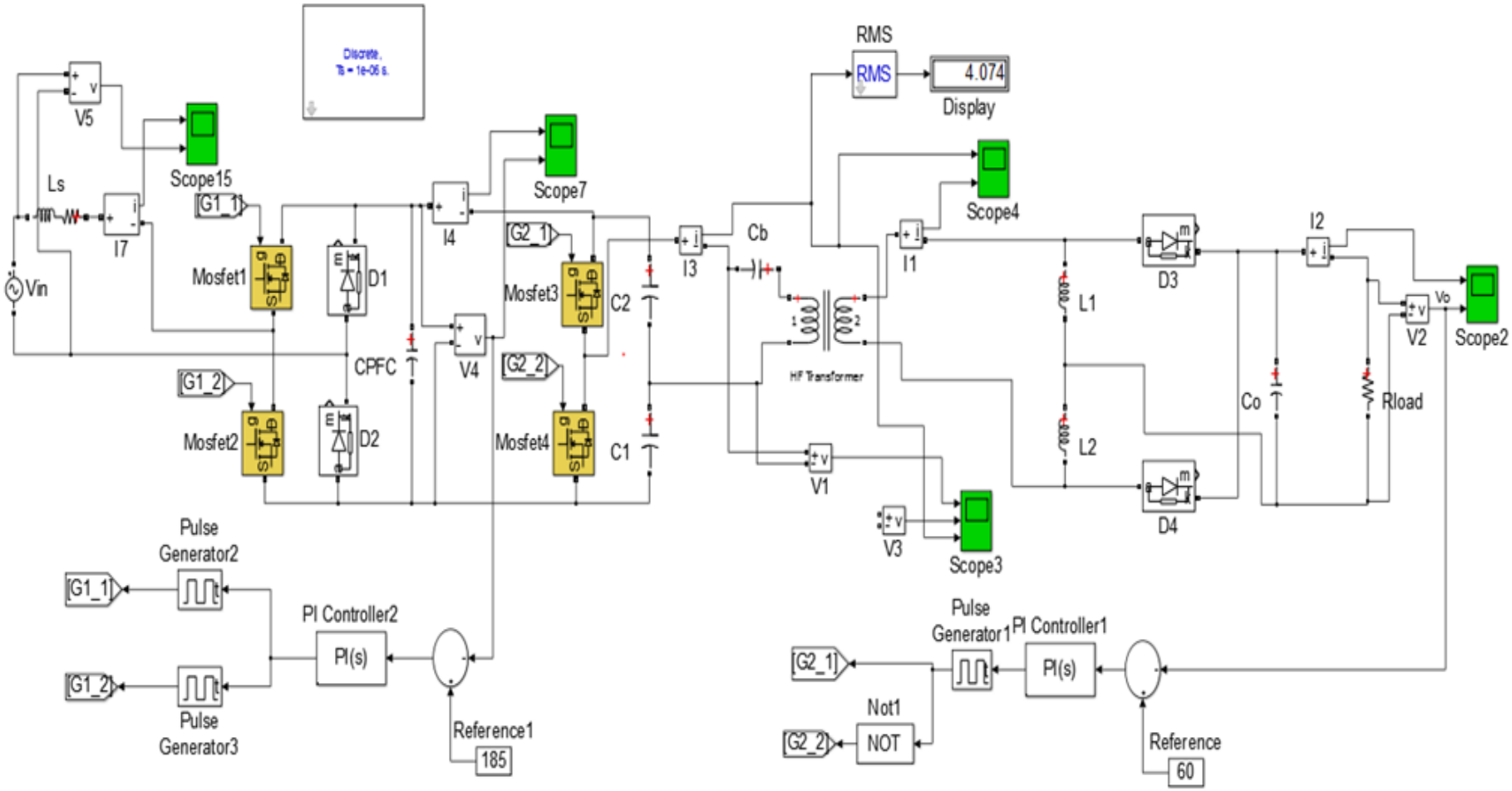
```
1   /*
2   * Academic License - for use in teaching, academic research, and meeting
3   * course requirements at degree granting institutions only. Not for
4   * government, commercial, or other organizational use.
5   *
6   * File: APEC_Topology_Model_V12_105KHz.h
7   *
8   * Code generated for Simulink model 'APEC_Topology_Model_V12_105KHz'.
9   *
10  * Model version : 1.25
11  * Simulink Coder version : 8.12 (R2017a) 16-Feb-2017
12  * C/C++ source code generated on : Mon Sep 17 21:37:53 2018
13  *
14  * Target selection: ert.tlc
15  * Embedded hardware selection: Texas Instruments->C2000
16  * Code generation objectives: Unspecified
17  * Validation result: Not run
18  */
19
20  #ifndef RTW_HEADER_APEC_Topology_Model_V12_105KHz_h_
21  #define RTW_HEADER_APEC_Topology_Model_V12_105KHz_h_
22  #include <stddef.h>
23  #ifndef APEC_Topology_Model_V12_105KHz_COMMON_INCLUDES_
```

```
24 # define APEC_Topology_Model_V12_105KHz_COMMON_INCLUDES_
25 #include "rtwtypes.h"
26 #include "DSP2833x_Device.h"
27 #include "DSP2833x_Gpio.h"
28 #include "DSP2833x_Examples.h"
29 #include "IQmathLib.h"
30 #endif /* APEC_Topology_Model_V12_105KHz_COMMON_INCLUDES_ */
31
32 #include "APEC_Topology_Model_V12_105KHz_types.h"
33 #include "MW_target_hardware_resources.h"
34
35 /* Macros for accessing real-time model data structure */
36 #ifndef rtmGetErrorStatus
37 # define rtmGetErrorStatus(rtm) ((rtm)->errorStatus)
38 #endif
39
40 #ifndef rtmSetErrorStatus
41 # define rtmSetErrorStatus(rtm, val) ((rtm)->errorStatus = (val))
42 #endif
43
44 #define APEC_Topology_Model_V12_105KHz_M (APEC_Topology_Model_V12_105K_M)
45
46 extern void enable_interrupts(void);
47 extern void config_ePWM_GPIO (void);
48
49 /* Parameters (auto storage) */
50 struct P_APEC_Topology_Model_V12_105_T_ {
51 uint16_T Constant_Value; /* Computed Parameter: Constant_Value
52 * Referenced by: '<Root>/Constant'
```

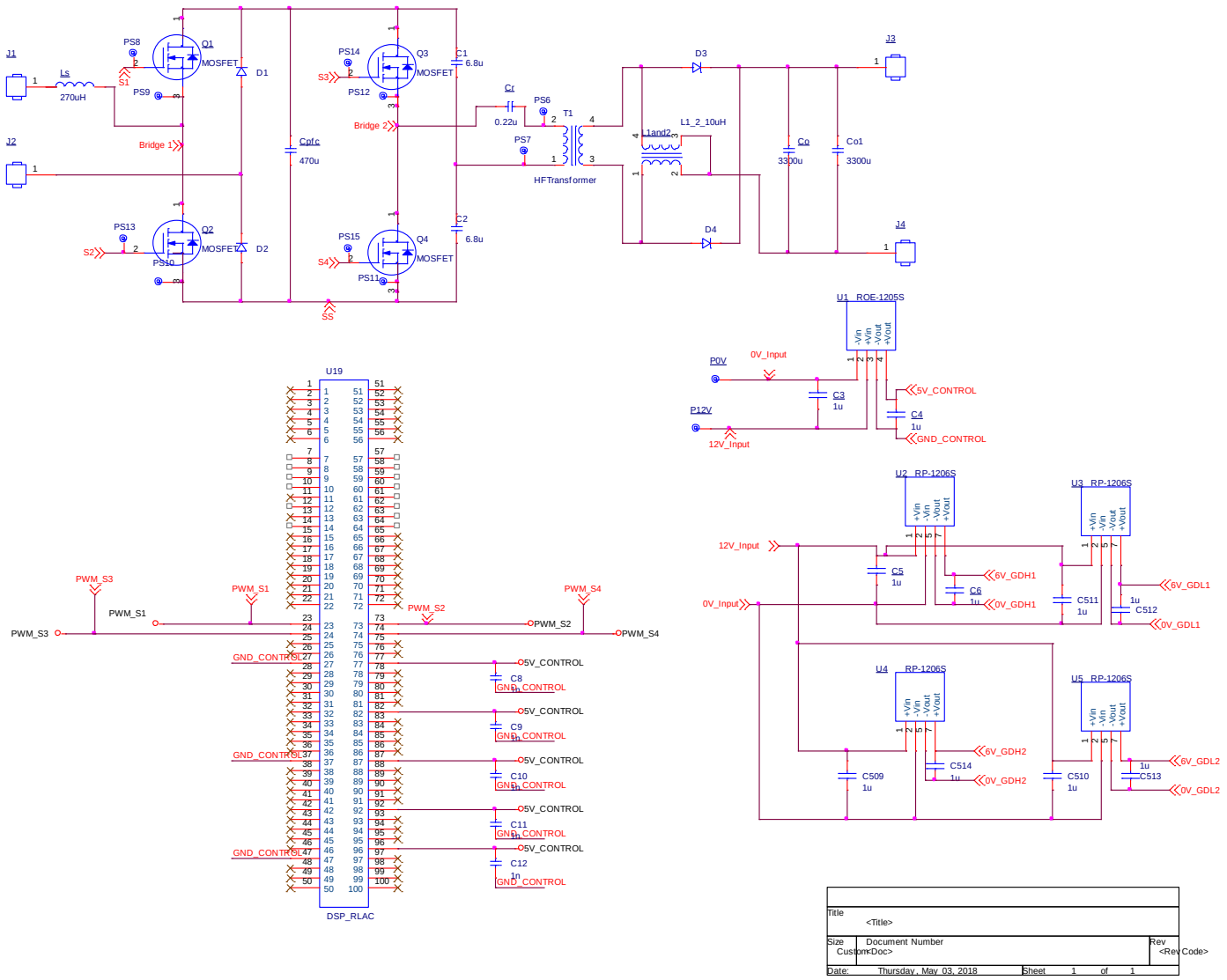
```
53  */
54  };
55
56  /* Real-time Model Data Structure */
57  struct tag_RTM_APEC_Topology_Model_V_T {
58  const char_T *errorStatus;
59  };
60
61  /* Block parameters (auto storage) */
62  extern P_APEC_Topology_Model_V12_105_T APEC_Topology_Model_V12_105KH_P;
63
64  /* Model entry point functions */
65  extern void APEC_Topology_Model_V12_105KHz_initialize(void);
66  extern void APEC_Topology_Model_V12_105KHz_step(void);
67  extern void APEC_Topology_Model_V12_105KHz_terminate(void);
68
69  /* Real-time Model object */
70  extern RT_MODEL_APEC_Topology_Model__T *const
    APEC_Topology_Model_V12_105K_M;
71
72  /*-
73  * The generated code includes comments that allow you to trace directly
74  * back to the appropriate location in the model. The basic format
75  * is <system>/block_name, where system is the system number (uniquely
76  * assigned by Simulink) and block_name is the name of the block.
77  *
78  * Use the MATLAB hilite_system command to trace the generated code back
79  * to the model. For example,
80  *
```

```
81  * hilite_system('<S3>') - opens system 3
82  * hilite_system('<S3>/Kp') - opens and selects block Kp which resides in S3
83  * Here is the system hierarchy for this model
84  *
85  * '<Root>' : 'APEC_Topology_Model_V12_105KHz'
86  */
87  #endif /* RTW_HEADER_APEC_Topology_Model_V12_105KHz_h_ */
88  /*
89  * File trailer for generated code.
90  * [EOF]
```

Appendix C: Converter closed-loop MATLAB schematic.



Appendix D: The OrCAD Capture schematic of the AC/DC converter.



Appendix E: The OrCAD Allegro PCB Editor 4-Layer PCB Layout Design.