A Power Constrained 433-MHz Low Noise Amplifier

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A Power Constrained 433-MHz Low Noise Amplifier

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

by

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University of Arkansas
Bachelor of Science in Electrical Engineering, 2018

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This thesis is approved for recommendation to the Graduate Council.

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Abstract

Within wireless communication systems, low noise amplifiers are critical for the performance of receivers. They are primarily responsible for providing enough gain while adding little noise to overcome the noise of the subsequent stages. The LNA presented here is part of a battery-powered transceiver meant to measure crop nutrient data and relay the information. Therefore, power consumption and area become import considerations. To design for a specific power level, a power-constrained noise optimization method is used. The method sizes the amplifying transistor for a fixed source impedance, power dissipation, technology, and operating frequency.

The chosen topology is the cascode stage with inductive source degeneration. This allows for an input impedance match without much added thermal noise. For area considerations, all inductors were made internal. The LNA was fabricated in a 130 nm SiGe BiCMOS8HP technology from GLOBALFOUNDRIES. Designing the amplifier for operation at 433 MHz produced a 12 dB gain, 4.9 dB noise figure, 6.3 mW power consumption, -5 dBm input referred 1 dB compression point, and unconditional stability.
Acknowledgments

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I would also like to thank all of the students that have been a part of the IC design group during my time here. Thank you to the Ph.D. students for their valuable guidance and feedback. They have had to take on many responsibilities and I am glad they were always more than happy to answer any questions I had. I have learned a great deal from all of them. A special thanks to Affan Abbasi and Marvin Suggs for their help in the testing of the LNA as well as design-related questions.
Dedication

This work is dedicated to all my family members who have been supportive both financially and spiritually along the way. To my parents, Pablo Alvarez and Maria Alvarez, thank you for all the sacrifices you have made to give me this opportunity. To my siblings, Joselyn Alvarez-Marquez and Gerardo Alvarez, thank you for always being there any time I needed help. Lastly, to my amazing wife, thank you for believing in me and for all your love and support.
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CHAPTER 1 – INTRODUCTION

The field of RF communications has grown tremendously over the past few decades. This growth is only expected to continue as more systems take advantage of what wireless communication has to offer. Many applications are already using wireless technology with demand for increased performance. This includes things such as home applications, vehicles, GPS tracking devices, medical equipment, etc.

The main reason for the wide use and availability comes from the integration capabilities in existence. By scaling down, the device’s performance metrics tend to increase. Such metrics include power consumption, area, speed, and of course cost. This allows for new applications to take advantage of wireless technology and combine it with existing IC technologies.

The work presented here deals with the fact that wireless signals can be quite weak, therefore amplification that does not substantially degrade the signal to noise ratio is necessary. The gain and noise present in the first stage of a receiver chain are largely responsible for the system’s performance. This means, no matter the application, it’s likely a low noise amplifier (LNA) will be needed at the front end of the receiver. What will be application dependent is how important different aspects of the LNA are. For the work presented here, the end application is part of a transceiver which is a circuit that can both transmit and receive. The transceiver, shown in Fig. 1.1, is ultimately part of a battery-powered in-field crop nutrient sensor. For that reason, the power consumption and size become important considerations when designing the LNA.
The challenge is balancing trade-offs and understanding which parameters can be reasonably sacrificed. Two very important considerations are already gain and noise. Therefore a design method that balances the two as well as takes into account power dissipation is needed. The work presented begins with a description of noise; mainly, what noise is and how it is characterized. Then, the aspects of impedance matching, gain, and power transfer are introduced. Later several topologies are analyzed to determine which is the most robust in terms of noise and power transfer at the input. Finally, the design method characterizes noise within a MOSFET to find an expression that balances noise performance, gain, and power consumption. Other important parameters such as stability and linearity are discussed in Chapter 6 when the testbench and simulation results were used to tweak the component values.
CHAPTER 2 – RELEVANT SOURCES OF NOISE

In electronics, noise is seen as an unwanted disturbance in an electrical signal. Essentially it is everything but the actual desired signal. There are many different types of noise since the sources they originate from vary significantly. Some can come from unnatural sources such as the 60-Hz power line and others have a more fundamental nature to them. Some examples of fundamental noise sources are thermal noise, shot noise, flicker noise, and popcorn noise. The main one that will be discussed here is thermal noise since it is the dominating source in MOSFETs.

2.1 Thermal Noise

Thermal noise was first reported by John B. Johnson as a random variation of potential across the ends of a conductor [1]. This variation was described as the result of the random motion of electric charges within the conductor caused by thermal agitation. The main findings from his measurements revealed that the resistance and absolute temperature of the conductor had a proportional effect on the mean-square potential fluctuation over the conductor. With the help of colleague Harry Nyquist, the findings were also proved in a purely theoretical manner with agreeable results [2]. The average thermal noise power in a resistor was shown to be

\[ P_{NA} = kT\Delta f \]  \hspace{1cm} (2.1)

where \( k \) is Boltzmann’s constant, \( T \) is the absolute temperature in kelvins, and \( \Delta f \) is the measurement bandwidth. It is called the available noise power since it is the maximum power delivered to another resistor of equal value. By definition, it is the power delivered to another resistor of equal value. If an open-circuit RMS noise voltage \( e_n \) is generated by a resistor \( R \), then the power delivered to an equal resistor value can be equated to (2.1) as shown in (2.2).
\[ \frac{\overline{e_n^2}}{4R} = P_{NA} = kT\Delta f \]  \hspace{1cm} (2.2)

An expression for the mean-square noise voltage generated by a conductor of resistance \( R \) and temperature \( T \) can now be given as

\[ \overline{e_n^2} = 4kTR\Delta f \]  \hspace{1cm} (2.3)

A Norton equivalent model can also be used to express the mean-square noise current as

\[ \overline{i_n^2} = \frac{\overline{e_n^2}}{R^2} = \frac{4kT\Delta f}{R} \]  \hspace{1cm} (2.4)

Using a resistor, \( R \), the noise voltage and current sources are modeled in Fig. 2.1 and Fig. 2.2, respectively.

![Mean-square noise voltage model](image1)

![Mean-square noise current model](image2)

**Fig. 2.1 Mean-square noise voltage model**  \hspace{1cm} **Fig. 2.2 Mean-square noise current model**

### 2.2 Thermal Noise in MOSFETs

Now that the thermal noise present in resistors has been expressed, the noise in field-effect transistors (FETs) can be calculated. This is because FETs are essentially voltage-controlled resistors. A detailed analysis arrived at the following expression for the mean-square short-circuit noise current within the conducting channel [3].

\[ \overline{i_n^2} \]
\[
\overline{i_{nd}^2} = 4kT\gamma g_{d0} \Delta f
\]  \hspace{1cm} (2.5)

This will be known as the drain current noise. Here, \(g_{d0}\) is the drain to source conductance with zero \(V_{DS}\) voltage. To account for a nonzero \(V_{DS}\) voltage, the parameter \(\gamma\) is introduced. At zero \(V_{DS}\) the parameter has a value of one. For long channel devices, this value decreases to 2/3 in the saturation region.

At high frequencies, another important source of noise can come from the coupling formed between the gate and channel. This is a consequence of the thermal agitation of the channel as well as a resistive gate material. The coupling results in a conductance \(g_g\) that is expressed as

\[
g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}}
\]  \hspace{1cm} (2.6)

The conductance can be used to express the thermal gate noise current as

\[
\overline{i_{ng}^2} = 4kT\delta g_g \Delta f
\]  \hspace{1cm} (2.7)

where \(\delta\) is the gate noise coefficient. In long channel devices, the gate noise coefficient is given as 4/3, which is double that of the drain noise coefficient [4]. When conservative estimates are done, the gain and drain noise coefficients will be assumed to triple for the short channel case.

### 2.3 Classical Two-Port Noise Model

To simplify the LNA design it is important to understand the generic macroscopic model of noise in two-ports. This helps understand the effect that the source impedance has on the noise performance. Once this is established the circuit design may be targeted towards the best noise performance.

To start with, consider a linear noisy two-port circuit shown in Fig. 2.1. The circuit is driven by a noisy source with admittance \(Y_s\) and an equivalent shunt noise current \(i_s\). The circuit...
can be replaced by Fig. 2.4, which shows an equivalent noiseless two-port circuit with noise sources placed externally. The external noise sources are represented by a noise voltage $e_n$ in series with the input voltage and a noise current $i_n$ in parallel with the input current.

![Noisy two-port circuit driven by a noisy source](image)

**Fig. 2.3 Noisy two-port circuit driven by a noisy source**

![Equivalent noiseless two-port with external noise sources](image)

**Fig. 2.4 Equivalent noiseless two-port with external noise sources**

A useful metric to establish the noise performance of a system is known as the noise factor ($F$). It is defined in (2.8) as the ratio of total output noise power to the output noise due to the input source.

$$F = \frac{\text{total output noise power}}{\text{total output noise power due to input source}}$$

(2.8)

Since only the behavior of the input and output ports are concerned, the effect that the source admittance has on the noise performance can be quickly determined. Now the goal is to derive a general expression for the minimum achievable noise factor given a source admittance.

To find the noise factor of Fig. 2.4, the individual noise powers at the output must be divided by the noise power at the output due to the input. Since each of the power terms is
directly proportional to the individual mean-square noise current terms, they can be written in terms of the mean-square noise currents. Also, since the proportionality constant is related to the way the two-port circuit transforms the current at the input into power at the output, all the terms will have the same constant \([5]\). Therefore the noise factor for Fig. 2.4 is given as

\[
F = \frac{i_s^2 + |i_n + Y_s e_n|^2}{i_s^2} \quad (2.9)
\]

This assumes that the noise of the source and the two-port are uncorrelated but it does not assume that the voltage and current noises of the two-port are uncorrelated with each other. This may often be the case since they may originate from the same source. To take this into account, the noise current, \(i_n\), can be separated into a correlated, \(i_c\), and an uncorrelated, \(i_u\), term between \(e_n\).

\[
i_n = i_c + i_u \quad (2.10)
\]

The correlated term can be written in terms of the noise voltage and a correlation admittance as such

\[
i_c = Y_c e_n \quad (2.11)
\]

Where \(Y_c\) is the correlation admittance. Substituting (2.10) and (2.11) into (2.9) gives the following noise factor:

\[
F = \frac{i_s^2 + |i_c + i_u + Y_s e_n|^2}{i_s^2} = \frac{i_s^2 + |i_u + Y_c e_n + Y_s e_n|^2}{i_s^2}
= \frac{i_s^2 + |i_u + (Y_c + Y_s)e_n|^2}{i_s^2} = 1 + \frac{i_u^2 + |Y_c + Y_s|^2 e_n^2}{i_s^2} \quad (2.12)
\]

Further substitution of (2.3) and (2.4) into (2.12) gives

\[
F = 1 + \frac{4kT G_u \Delta f + |Y_c + Y_s|^2 4kT R_n \Delta f}{4kT G_s \Delta f}
\]
\[ F = 1 + \frac{G_u + |Y_c + Y_s|^2 R_n}{G_s} \]  

(2.13)

where the current noise sources’ associated resistances, \( R \) were placed as conductances \( G \). Since each source is at the same temperature and measured with the same bandwidth, the common factor \( 4kT\Delta f \) can be eliminated. Going further, each admittance, \( Y \), can be separated into a conductance, \( G \), and susceptance, \( B \). The noise factor can now be expressed as

\[ F = 1 + \frac{G_u + [(G_c + G_s)^2 + (B_c + B_s)^2]R_n}{G_s} \]  

(2.14)

It is now evident that the two-port’s noise factor can be obtained once its four noise parameters, \( G_u, G_c, B_c, \) and \( R_n \), have been established.

The goal is now to identify the two-port parameters that would give the minimum noise factor. First, since \( B_s \) is only inside the parenthesis, setting its value to \( -B_c \) would be required to give the minimum \( F \). This gives the optimum source susceptance as

\[ B_{s, opt} = -B_c \]  

(2.15)

To find the needed \( G_s \), the first derivative of (2.14) is taken with respect to \( G_s \) when \( B_s = -B_c \) and set equal to zero:

\[ \frac{\partial F}{\partial G_s} = \frac{\partial (G_u G_s^{-1} + (G_c + G_s)^2 R_n G_s^{-1})}{\partial G_s} \]

\[ = -\frac{G_u}{G_s^2} - \frac{(G_c + G_s)^2 R_n}{G_s^2} + 2(G_c + G_s)R_n \frac{1}{G_s} \]

\[ G_{s, opt} = \sqrt{\frac{G_u}{R_n} + \frac{G_c^2}{G_s}} \]  

(2.16)

Substituting (2.15) and (2.16) into (2.14) gives the minimum noise factor achievable:
\[
F_{\text{min}} = 1 + \frac{G_u + (G_c^2 + 2G_cG_{\text{opt}} + G_{\text{opt}}^2)R_n}{G_{\text{opt}}}
\]

\[
= 1 + 2R_n \left[ \frac{G_u}{R_n} + G_c^2 + 2G_cR_n \right] = 1 + 2R_n \left[ \frac{G_u + G_c^2 + G_c}{R_n} \right]
\] (2.17)

In the case of a source admittance that is not the optimal one, the noise factor can be expressed in terms of \(F_{\text{min}}\) as

\[
F = F_{\text{min}} + \frac{R_n}{G_s} \left[ (G_s - G_{s,\text{opt}})^2 + (B_s - B_{s,\text{opt}})^2 \right]
\] (2.18)

It is clear from (2.18) that the noise factor is dependent on \(R_n\). It can be shown that circuits with a large \(R_n\) imply a low bias current. For the design of low noise amplifiers, this means the conditions for better noise performance contradict those of better power performance. Although they may end up close, it is evident that the conditions for the best noise performance are not necessarily the same as those for the best power transfer. This will be a major area where trade-offs will be necessary.

### 2.4 Importance of 1st Stage Noise Performance

To understand why so much emphasis is given to noise performance in the 1st stage of the receiver it’s important to look at Friis’ formula expressed below [6].

\[
F_{\text{tot}} = F_1 + \frac{F_2 - 1}{G_{A_1}} + \frac{F_3 - 1}{G_{A_1}G_{A_2}} + \cdots + \frac{F_m - 1}{G_{A_1}G_{A_2} \cdots G_{A(m-1)}}
\] (2.19)

Here, \(F_{\text{tot}}\) is the total system noise factor, \(G_{A_m}\) is the available power gain of the \(m^{th}\) stage, and \(F_m\) is the noise factor of the individual \(m^{th}\) stage. It can be seen that the 1st stage has the most significant effect on a system’s total noise factor. Even more so if its gain is high. For this reason, emphasis on the first stage’s gain and noise factor may be all that is needed for the overall noise factor.
CHAPTER 3 – POWER TRANSFER AND PORT IMPEDANCE MATCHING

Fig. 3.1 Impedance matching to transform a circuit for maximum power transfer

Since in the microwave realm power quantities largely replace discussion of voltage or current quantities, impedance matching becomes important. The concept of impedance matching is illustrated in Fig. 3.1. In AC circuit theory, maximum power transfer is obtained when the load impedance, \( Z_L \) is the complex conjugate of the source impedance \( Z_S \). This happens when the inductive reactance, \( X_S \), and capacitive reactance, \( X_L \), cancel each other and when \( R_S \) is equal to \( R_L \). This only occurs when the frequency is at the resonant frequency of \( \frac{1}{\sqrt{LC}} \). At other frequencies, the voltage is attenuated when it arrives at the load. In other words, power is reflected towards the source [7]. Knowing that impedance matching affects how well power is transferred, it is useful to model circuits in terms of parameters that can be obtained through power measurements. One such set of parameters is called the scattering parameters, or S-parameters.

3.1 S-Parameters

S-parameters are used to describe the way RF energy moves through a multiport network. More specifically, they describe the response to signals incident to any or all ports. By only needing the behavior at the input and output ports they allow for the simplification of complex
networks. The response and incident ports are denoted in the notation $S_{ij}$. Where the $i$ indicates the response port and $j$ the incident port. Thus $S_{12}$ is the response at port 1 due to port 2.

At low frequencies, the usual way to obtain two-port characterizations is to use open or short-circuit conditions to set incident signals that are not of interest to zero. In the case of S-parameters, the signals of interest are commonly at higher frequencies where proper shorts or opens are hard to make. This is why, for these two-port parameters, the lines are terminated in their characteristic impedances when wanting to set incident signals to zero.

It can be seen from Fig. 3.2 that the variable $a_1$ represents the signal traveling into port 1. Likewise, $b_2$ represents the signal traveling out of port 2. If the signals traveling out of a port are a result of both signals traveling into their respective ports, the signals coming out can be written as

$$b_1 = S_{11}a_1 + S_{12}a_2 \quad (3.1)$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \quad (3.2)$$

Thus to easily obtain the $S_{11}$ and $S_{21}$ parameters, port 2 should be terminated with an impedance load equal to the characteristic impedance $Z_0$ of the wave propagation medium [8]. This will cause $a_2$ to be zero. The same can be done with port 1 to set $a_1$ to zero. This gives the four S-parameters for a two-port network as
\[ S_{11} = \frac{b_1}{a_1} \] (3.3)

\[ S_{21} = \frac{b_2}{a_1} \] (3.4)

\[ S_{22} = \frac{b_2}{a_2} \] (3.5)

\[ S_{12} = \frac{b_1}{a_2} \] (3.6)

From the expressions for the S-parameters, \( S_{11} \) and \( S_{22} \) are known as the input and output reflection coefficients, respectively. They indicate how well the input and output impedances of the circuit match with those of the source and load. The smaller the values, the less the reflective energy will be. If the \( S_{11} \) is very small it would mean that most of the incident power at the input port is transferred to the circuit. Likewise, if the \( S_{22} \) is very small it means most of the power at the output is transferred to the load. \( S_{21} \) is known as the forward voltage gain and \( S_{12} \) as the reverse voltage gain. In amplifier design a higher \( S_{21} \) is desirable. A low \( S_{12} \) is also preferable to keep the input isolated from the output.

It is worth noting exactly what kind of signals are being described by these parameters. From Fig. 3.2, the variables \( a_i \) and \( b_i \) represent normalized voltage waves which are also known as power waves. These power waves can be expressed as

\[ a_1 = \frac{V_{i1}}{\sqrt{Z_0}} \] (3.7)

\[ b_1 = \frac{V_{r1}}{\sqrt{Z_0}} \] (3.8)

\[ a_2 = \frac{V_{i2}}{\sqrt{Z_0}} \] (3.9)
\[ b_2 = \frac{V_{r2}}{\sqrt{Z_0}} \]  \quad (3.10)

Where \( V_{i1} \) and \( V_{i2} \) are the incident voltage waves at port 1 and 2 respectively, and \( V_{r1} \) and \( V_{r2} \) are the reflected waves at port 1 and 2 respectively [9]. It is common to normalize the voltage waves using the characteristic impedance \( Z_0 \) because the power relations can be easily obtained simply by squaring the S-parameters as shown below.

\[
|S_{11}|^2 = \left| \frac{b_1}{a_1} \right|^2 \bigg|_{a_2=0} = \frac{\text{Reflected power at port 1}}{\text{Incident power at port 1}} \quad (3.11)
\]

\[
|S_{12}|^2 = \left| \frac{b_1}{a_2} \right|^2 \bigg|_{a_1=0} = \frac{\text{Reflected power at port 1}}{\text{Incident power at port 2}} \quad (3.12)
\]

\[
|S_{21}|^2 = \left| \frac{b_2}{a_1} \right|^2 \bigg|_{a_2=0} = \frac{\text{Reflected power at port 2}}{\text{Incident power at port 1}} \quad (3.13)
\]

\[
|S_{22}|^2 = \left| \frac{b_1}{a_2} \right|^2 \bigg|_{a_1=0} = \frac{\text{Reflected power at port 2}}{\text{Incident power at port 2}} \quad (3.14)
\]

### 3.2 Types of Power Gain

Due to the quality of impedance matches, the power gain can be defined in multiple ways. The simplest is the basic power gain that comes to mind, which is the ratio of the power actually delivered to a load to the power actually received at the input. This is called the operating power gain, commonly denoted by \( G_p \). Available power gain, \( G_A \), is the ratio of the power available to be delivered to a load to the power available from the source. The distinctions between available and actual come from the fact that perhaps not all the power will be transferred at the ports. The transducer power gain, \( G_T \), is the ratio of the power actually
delivered to a load to the power available at the source. This is the same definition for the S-parameter $S_{21}$ when both the source and load impedances are equal and expressed in dB.

If the input impedance is the complex conjugate of the source impedance the available input power will be the actual power delivered. Therefore, the transducer gain will equal the operating power gain. Similarly when the load impedance is also matched to the output impedance, the available power gain, transducer gain, and operating gain will all be equal.

During the simulation, comparisons can be made among these types to examine the quality of the port matching.
CHAPTER 4 – LOW NOISE AMPLIFIER TOPOLOGIES

In designing an LNA there are several goals to aim for. The major ones include minimizing noise figure, providing a good gain, maximizing power transfer from the source, and keeping power consumption reasonable. Juggling all of these can be very complicated but a good strategy is to start by looking at topologies that will provide a maximum power transfer and also keep noise low. As discussed in Chapter 3, input matching to the source impedance is important for maximum power transfer. In this case, the source is a 50 Ω antenna therefore a 50 Ω input impedance is needed. To keep noise low, the use of physical resistors should be avoided, due to thermal noise. Keeping this in mind, several basic common source amplifier topologies will be looked at.

4.1 CS Stage with Shunt Resistor

An easy way to achieve the desired input match is by simply putting a 50 Ω shunt resistor at the input of the MOSFET as shown in Fig. 4.1. Because it is a physical resistor, it is a poor choice due to the thermal noise added. Furthermore, it will cause voltage attenuation at the gate since it is acting as a resistor divider.

Fig. 4.1 Common-source stage with a shunt resistor match
4.2 CS Stage with Feedback Resistor

To overcome the signal attenuation, a feedback resistor can be used to provide the input match as shown in Fig. 4.2. The problem with this solution is that some thermal noise is still added. Typical noise figures easily exceed 3 dB [6].

![Resistive Feedback Circuit](image)

**Fig. 4.2 Common-source stage with resistive feedback**

4.3 CS Stage with Degenerative Inductive Feedback

The main issue thus far is unwanted thermal noise from a physical resistor. To solve this, the transit time effects of the charges in the channel can be enhanced. Departing from the ideal capacitive lag between gate voltage and channel current introduces a resistive component in the input impedance. By introducing an inductor at the source node, the current flow lag with respect to the applied gate voltage can be controlled. This method is known as inductive source degeneration and is shown in Fig. 4.3.

![Inductive Source Degeneration Circuit](image)

**Fig. 4.3 Common-source stage with inductive source degeneration**
The resistive component can be expressed by obtaining the input impedance of a simple small-signal model of Fig. 4.3, which is shown in Fig. 4.4. It is important to note that this simplified model only contains a transconductance and a gate to source capacitance.

![Small signal model of CS stage with inductive source degeneration](image)

**Fig. 4.4** Small signal model of CS stage with inductive source degeneration

First, if the current through the capacitance $C_{gs}$ is simply the input current and denoted as $i_{in}$ then the current through the inductor can be expressed as

$$i_{ls} = g_m v_{gs} + i_{in}$$

(4.1)

The input voltage is directly connected to the gate in this case, which makes $v_{in} = v_g$. Since $i_{ls}$ can also be expressed as

$$i_{ls} = \frac{v_{in} - v_{gs}}{sL_s}$$

(4.2)

the two above equations can be equated and rearranged to express $v_{in}$ as

$$v_{in} = i_{in}sL_s + v_{gs}(1 + g_m sL_s)$$

(4.3)

Also, $v_{gs}$ can be given as

$$v_{gs} = \frac{i_{in}}{sC_{gs}}$$

(4.4)

Substituting (4.4) into (4.3) gives
\[ v_{in} = i_{in} s L_s + \frac{(1 + g_m s L_s) i_{in}}{s C_{gs}} \]  

Finally the input impedance \( Z_{\text{in}} \) can be written as

\[ Z_{\text{in}} = \frac{v_{in}}{i_{in}} = s L_s + \frac{1}{s C_{gs}} + \frac{g_m L_s}{C_{gs}} \approx s L_s + \frac{1}{s C_{gs}} + \omega_r L_s \]

This expression shows that the input impedance can be viewed as a simple series RLC network. The resistive term shows up as \( \frac{g_m L_s}{C_{gs}} \). This is attractive for input matching because the term is not actually made up of a physical resistor and thus does not add the unwanted thermal noise.

Furthermore, the input impedance is only purely resistive at the resonant frequency where the inductive and capacitive components cancel each other out. This is a good thing for narrowband LNAs. The problem is when the frequency is fixed and an extra degree of freedom is needed to set the resonant frequency. This is where another inductor \( L_g \) is added at the input as shown in Fig. 4.5. The small-signal model shown in Fig. 4.6 can be used to find the new input impedance.

![Small-signal model with inductive source degeneration](image-url)

**Fig. 4.5** Narrowband common-source stage with inductive source degeneration
Fig. 4.6 Small signal model of narrowband CS stage with inductive source degeneration

By inserting $L_g$, the input voltage is no longer simply $v_g$ and the current through $L_s$ is modified as

$$i_{L_s} = \frac{v_{in} - v_{Lg} - v_{gs}}{sL_s} \quad (4.7)$$

As before, equating (4.1) with (4.7) and solving for $v_{in}$ gives

$$v_{in} = i_{in}sL_s + (1 + g_m sL_s)v_{gs} + v_{Lg}$$

$$= i_{in}sL_s + (1 + g_m sL_s) \frac{i_{in}}{sC_{gs}} + i_{in}sL_g \quad (4.8)$$

Finally, the input impedance is expressed as

$$Z_{in} = \frac{v_{in}}{i_{in}} = s(L_s + L_g) + \frac{1}{sC_{gs}} + \omega_L L_s \quad (4.9)$$

The additional inductor at the gate can now be used to set the resonant frequency at the input and tune out the capacitance, while the inductor at the source is used to set the input match. By equating the first two terms of (4.9) to zero, the expression for $L_g$ can be given as

$$L_g = \frac{1}{(2\pi f)^2 C_{gs}} - L_s \quad (4.10)$$
4.4 Cascode CS Stage with Degenerative Inductive Feedback and Inductive Load

![Image of Cascode CS stage with degenerative inductance and a load inductor]

**Fig. 4.7 Cascode CS stage with degenerative inductance and a load inductor**

The use of inductive source degeneration can be expanded upon by adding a cascode transistor at the output followed by an inductive load. An output inductor serves to provide gain without being limited by the supply voltage. This can be seen by expressing the voltage gain of a single CS transistor as

\[ A_v = g_m R_D = \frac{2I_D}{V_{GS} - V_{TH}} \frac{V_{RD}}{I_D} = \frac{2V_{RD}}{V_{GS} - V_{TH}} \]  \hspace{1cm} (4.11)

Where \( V_{RD} \) is the voltage drop across the resistor \( R_D \). This results in higher supply voltages since enough headroom must be created to provide sufficient gain. To overcome this issue an inductor \( L_D \) is used at the output. Smaller supply voltages can now be afforded since the dc voltage drop is very small. The load can also be resonated with capacitances at the output to operate at higher frequencies.

A separate issue arises when using an inductive load. A negative resistance can appear at frequencies other than resonance due to the gate-drain overlap capacitance [6]. This can make the amplifier unstable. For this reason, a cascode transistor is added to provide isolation. Moving
forward, the design will be based on this cascode common source stage with inductive degeneration and an inductive load.
CHAPTER 5 – LOW NOISE AMPLIFIER DESIGN STRATEGY

A strategy to balance tradeoffs is often necessary since the conditions that minimize noise figure will most likely differ from those that maximize power gain. Also, to achieve the minimum noise figure an impractically high power consumption is required. Therefore, when designing the LNA the goal will be to express the minimum noise achievable in terms of power consumption. This will provide a method to balance gain, noise figure, and power. To start with, the four classical two-port noise parameters necessary to fully describe the noise model will be found for a MOSFET. Those parameters will then be used to express the minimum noise figure in terms of power. Finally, this will lead to an expression for an optimal transistor width. The derivations shown are obtained from Thomas H. Lee’s *The Design of CMOS Radio-Frequency Integrated Circuits* [5].

5.1 Classical Two-Port MOSFET Noise Parameters

As mentioned previously, a two-port circuit’s noise factor can be obtained once its four noise parameters, $G_u$, $G_c$, $B_c$, and $R_n$, have been established. According to the classical two-port noise model shown in Section 2.3, the noise sources within the circuit can be extracted to the input port. To obtain the parameters for a MOSFET, the two noise sources are first reflected back to the input as one voltage and one current source. As previously mentioned, the MOSFET noise model contains two sources. These sources, which are the mean-square drain current noise and gate current noise, are repeated below

\[
\overline{i_{na}^2} = 4kT\gamma g_{d0}\Delta f \quad (5.1)
\]

\[
\overline{i_{ng}^2} = 4kT\delta g_{g}\Delta f \quad (5.2)
\]

where $g_g$ is expressed as
\[ g_g = \frac{\omega^2 C_{gs}^2}{5 g_{d0}} \]  

Since both the gain and drain noise current sources come from the same source, being thermal noise, the implication is that these values are correlated. The correlation factor \( c \) is defined below.

\[ c \equiv \frac{\bar{i}_{ng} i_{nd}^*}{\sqrt{\bar{i}_{ng}^2 \cdot i_{nd}^2}} \]  

(5.4)

For long channel devices, the theoretical value of \( c \) is 0.395j [4], the sign of which is flipped when the direction for the gate noise is from the source to gate, causing its value to be \(-0.395j\) [5]. For simplicity, this value is the one which will be used moving forward even though it is the theoretical long-channel value.

The induced gate current noise is already at the input, therefore it can be left as is. As for the drain current noise, it is reflected back to the input as a voltage and current. The noise voltage generator is responsible for the output noise when the input is short-circuited. Its value is given by reflecting the drain current noise back to the input as a noise voltage and simply using \( g_m \) to express their relationship as such

\[ \bar{e}_{n}^2 = \frac{i_{nd}^2}{g_m} = \frac{4kT g_{d0} \Delta f}{g_m^2}. \]  

(5.5)

Since one of the four noise parameters, \( R_n \) can be thought of as the source of the thermal noise from the voltage generator it can be expressed as

\[ R_n = \frac{\bar{e}_{n}^2}{4kT \Delta f}. \]  

(5.6)

Substituting (5.5) into (5.6) gives
\[ R_n = \frac{\gamma g_{d0}}{g_m^2} = \frac{\gamma}{\alpha g_m} \]  \hspace{1cm} (5.7)

where

\[ \alpha = \frac{g_m}{g_{d0}}. \]  \hspace{1cm} (5.8)

The relationship of noise performance to bias current can be easily seen here. Since bias current is directly related to \( g_m \) it will also affect \( R_n \). Since the second term in the noise factor from (2.18) is proportional to \( R_n \), the current will have an inverse effect on noise.

This noise voltage generator on its own does not complete the reflected drain current noise modeling. Since a drain current noise at the output still exists when the input is open-circuited and the induced gate current noise is disregarded, the reflected drain current noise at the input must also be present as a noise current generator. If the drain current noise is divided by the transconductance and then multiplied by the input admittance, the equivalent input current noise is obtained. This gives the complete model of \( i_{nd} \).

\[ \overline{i_{n1}} = \frac{i_{nd}^2}{g_m^2} \left( j\omega C_{gs} \right)^2 = e_n^2 \left( j\omega C_{gs} \right)^2 \]  \hspace{1cm} (5.9)

The total input current noise would then be the sum of the induced gate current noise that was already at the input and the reflected drain noise current from (5.9). Fig. 5.1 shows the classical two-port noise model for a MOSFET according to the derivation.
The next step is to obtain the correlation admittance $Y_c$ among the total current sources and the voltage source. The induced gate noise can be seen as the sum of one term that is fully correlated with the drain current noise, $i_{ngc}$, and another that is fully uncorrelated, $i_{ngu}$. Since $i_{n1}$ is fully correlated with $e_n$, the expression for the correlation admittance can be written as

$$Y_c = \frac{i_{n1} + i_{ngc}}{e_n} = j\omega C_{gs} + \frac{i_{ngc}}{e_n} = j\omega C_{gs} + g_m \frac{i_{ngc}}{i_{nd}} \quad (5.10)$$

The goal is now to express the correlation admittance using the correlation coefficient, $c$.

To do so, the numerator and denominator of the last term are multiplied by the conjugate of the drain noise current and then each is averaged as such

$$g_m \frac{i_{ngc}}{i_{nd}} = g_m \frac{i_{ngc}^* i_{nd}^*}{i_{nd}^* i_{nd}} = g_m \frac{i_{ngc} i_{nd}^*}{i_{nd}^* i_{nd}} = g_m \frac{i_{ngc} i_{nd}^*}{i_{nd}^* i_{nd}} \quad (5.11)$$

The last substitution of the correlated portion of induced gate current noise, $i_{ngc}$, with the full gate current noise, $i_{ng}$, is made because the uncorrelated portion would contribute nothing to the cross-correlation term. The correlation admittance can then be expressed as

$$Y_c = j\omega C_{gs} + g_m \frac{i_{ng} i_{nd}^*}{i_{nd}^* i_{nd}} = j\omega C_{gs} + g_m \frac{\frac{i_{ng}^2}{i_{nd}^2}}{\frac{i_{nd}^2}{i_{nd}^2}} \frac{i_{ng}^2}{i_{ng}^2}$$
\[ 
Y_c = j \omega C_{gs} + g_m c \sqrt{\frac{\delta g_g}{\gamma g_{d0}}}.
\] (5.12)

The correlation coefficient, \(c\), from (5.4), can then be substituted, as well as the mean-square drain and gate current noise expressions from (5.1) and (5.2).

\[ 
Y_c = j \omega C_{gs} + g_m c \sqrt{\frac{\delta g_g}{\gamma g_{d0}}}.
\] (5.13)

Further substitution of \(g_g\) from (5.3) leads to

\[ 
Y_c = j \omega C_{gs} + g_m c \sqrt{\frac{\delta \omega^2 C_{gs}^2}{5 \gamma g_{d0}^2}} = j \omega C_{gs} + \frac{g_m c}{g_{d0}} \sqrt{\frac{\delta}{5 \gamma}} \omega C_{gs}
\] (5.14)

Once the minus sign and the imaginary part of \(c\) is extracted and its absolute value is left, the expression for the correlation admittance is

\[ 
Y_c = j \omega C_{gs} \left(1 - \frac{g_m c}{g_{d0}} \left| \frac{\delta}{5 \gamma} \right| \right) = j \omega C_{gs} \left(1 - \alpha |c| \frac{\delta}{5 \gamma} \right).
\] (5.15)

It is apparent that the correlation admittance is purely imaginary, which leaves the parameter \(G_c\) as zero. This is a result of ignoring any resistive noise at the input from the resistive gate material. It is also evident that power transfer cannot be maximized while simultaneously minimizing the noise figure. This is because \(Y_c\) is not simply \(C_{gs}\) but rather a multiple of it. This leaves one more noise parameter to derive from the two-port model, \(G_u\).

By definition, the correlation coefficient can be used to express the total induced gate noise current as the sum of the correlated and uncorrelated portions.

\[ 
\overline{i_{ng}^2} = (i_{ngc} + i_{ngu})^2 = 4 kT \Delta f g_g |c|^2 + 4 kT \Delta f g_g (1 - |c|^2)
\] (5.16)

Since \(G_u\) is seen as the conductance that produces the noise \(\overline{i_u^2}\), it can be expressed as
\[ G_u = \frac{i_u^2}{4kT\Delta f} \]  

(5.17)

The only uncorrelated input noise current comes from the second term in (5.16). Therefore, it can be substituted into the numerator in (5.17). This gives the parameter \( G_u \) as

\[ G_u = \frac{4kT\Delta f\delta g_g(1 - |c|^2)}{4kT\Delta f} = \frac{\delta \omega^2 c_{gs}^2 (1 - |c|^2)}{5g_{d0}} \]  

(5.18)

**Table 5.1 Two-port MOSFET noise parameters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_n )</td>
<td>( \frac{\gamma}{\alpha g_m} )</td>
</tr>
<tr>
<td>( G_c )</td>
<td>0</td>
</tr>
<tr>
<td>( B_c )</td>
<td>( \omega C_{gs} \left(1 - \alpha</td>
</tr>
<tr>
<td>( G_u )</td>
<td>( \frac{\delta \omega^2 c_{gs}^2 (1 -</td>
</tr>
</tbody>
</table>

Table 5.1 summarizes the four parameters for the MOSFET. Having them, the optimum source impedance, as well as the minimum noise figure, can be determined. The optimum source susceptance is obtained using (2.15) and is shown below.

\[ B_{opt} = -B_c = -\omega C_{gs} \left(1 - \alpha |c| \sqrt{\frac{\delta}{5\gamma}}\right) \]  

(5.19)

The optimum source conductance is obtained using (2.16).
\[ G_{opt} = \frac{G_u}{R_n} + G_c^2 = \frac{\delta g_m^2 \omega^2 C_{gs}^2 (1 - |c|^2)}{5 g_d \gamma} \]

\[ = \alpha \omega C_{gs} \sqrt{\frac{\delta}{5 \gamma}} (1 - |c|^2) \quad (5.20) \]

Finally, the minimum noise factor achievable can be expressed using (2.17).

\[ F_{min} = 1 + 2 R_n \left[ \frac{G_u}{R_n} + G_c^2 + G_c \right] \approx 1 + \frac{2}{5} \frac{\omega}{\omega_T} \sqrt{\gamma \delta (1 - |c|^2)} \quad (5.21) \]

The issue with simply following the noise matching requirements is that it does not take into account power. Being conservative with estimates for noise still leads to impractically high power requirements if one wants to achieve the minimum noise factor for a fixed source impedance. The requirements come from a necessarily high \( C_{gs} \), when \( G_{opt} \) comes from a 50 \( \Omega \) source impedance. Since it will be the case that the source conductance is fixed, \( C_{gs} \) must be set to around 4 pF to make it the optimum value [5]. If device capacitance is roughly 1 pF per millimeter, a 4mm wide device would be needed to achieve the minimum noise factor. This unrealistically large device would also require a large amount of current. Usually a bias current greater than 100 mA. Therefore it is beneficial to express the noise factor in terms of a specified power and optimize for it.

### 5.2 Optimizing Noise Under a Fixed Power Consumption

Beginning with the general expression of the noise factor, the goal will be to rewrite the expression in terms of power dissipation variables. The power terms that make up the expression will then be treated as constants when finding the minimum noise figure. The expression will be differentiated with respect to another variable which is related to gain. Afterward, a noise
optimizing width for the amplifying transistor can be obtained based on the fixed power consumption.

The general noise factor expression from Chapter 2 is given as:

$$F = F_{\text{min}} + \frac{R_n}{G_s} \left[ (G_s - G_{\text{opt}})^2 + (B_s - B_{\text{opt}})^2 \right]$$  \hspace{1cm} (5.22)

To simplify things, the source susceptance $B_s$ is assumed to be selected near to $B_{\text{opt}}$ to establish the second term in brackets as zero. Doing so means this method will sacrifice a noise match in favor of a power match at the input. This is because $B_{\text{opt}}$ from (5.19) is not exactly the considered input capacitance of $C_{gs}$. Rather, it is a multiple of it. Hence $B_s$ is not set as a noise match but will still be close to it. The expression for noise factor is then reduced to

$$F = F_{\text{min}} + \frac{R_n}{G_s} \left[ (G_s - G_{\text{opt}})^2 \right]$$ \hspace{1cm} (5.23)

For clarity, the conductances are expressed in terms of dimensionless quality factors. The expression for $G_{\text{opt}}$ from (5.20) can be rearranged and written as

$$\frac{G_{\text{opt}}}{\omega C_{gs}} = \alpha \sqrt{\frac{\delta}{5\gamma}(1 - |c|^2)} = Q_{\text{opt}}$$ \hspace{1cm} (5.24)

The same can be done for $G_s$

$$Q_s = \frac{G_s}{\omega C_{gs}} = \frac{1}{\omega C_{gs}R_s}$$ \hspace{1cm} (5.25)

Using the expression for $R_n$ from (5.7) and expressing $G_{\text{opt}}$ and $G_s$ in terms of the quality factors, the noise factor is rewritten as

$$F = F_{\text{min}} + \frac{\gamma}{\alpha g_m Q_s \omega C_{gs}} \left[ (Q_s \omega C_{gs} - Q_{\text{opt}} \omega C_{gs})^2 \right]$$

$$= F_{\text{min}} + \frac{\gamma}{\alpha g_m Q_s} \omega C_{gs} \left[ Q_s^2 - 2Q_s Q_{\text{opt}} + Q_{\text{opt}}^2 \right]$$
\[
F = F_{\text{min}} + \frac{\gamma Q_S \omega C_{gs}}{a g_m} \left[ 1 - 2 \frac{Q_{\text{opt}}}{Q_S} + \frac{Q_{\text{opt}}^2}{Q_S^2} \right]
\]

\[
= F_{\text{min}} + \frac{\gamma Q_S \omega C_{gs}}{a g_m} \left[ 1 - \frac{Q_{\text{opt}}}{Q_S} \right]
\]  (5.26)

Next, expressions for \(Q_s\), \(\alpha\), and \(g_m\) are found in terms of power. A typical expression for \(C_{gs}\) is given as

\[
C_{gs} = \frac{2}{3} C_{ox} WL
\]  (5.27)

Since \(Q_s\) is a function of \(C_{gs}\) it can be expressed as

\[
Q_s = \frac{1}{\omega \frac{2}{3} C_{ox} W L R_s}
\]  (5.28)

where \(C_{ox}\) is the gate oxide capacitance per unit area. It is also known that the expression for drain current is

\[
I_D = W L C_{ox} v_{sat} E_{sat} \frac{\rho^2}{1 + \rho}
\]  (5.29)

where

\[
\rho = \frac{V_{gs} - V_t}{E_{sat}} = \frac{V_{od}}{E_{sat}}
\]  (5.30)

and

\[
v_{sat} = \frac{\mu_n}{2} E_{sat}
\]  (5.31)

If the width \(W\) is solved for and substituted into (5.28), \(Q_s\) can be written as

\[
Q_s = \frac{1}{\omega \frac{2}{3} I_D R_s} = \frac{3 v_{sat} E_{sat} \rho^2}{2 \omega R_s} \frac{1}{1 + \rho I_D}
\]  (5.32)
In the above expressions $v_{sat}$ is the saturation velocity and $E_{sat}$ is the velocity saturation field strength. The drain current can also be expressed as a function of power dissipation and supply voltage

$$I_D = \frac{P_D}{V_{DD}} \quad (5.33)$$

leaving $Q_s$ as

$$Q_s = \frac{3}{2} v_{sat} E_{sat} \frac{\rho^2}{\omega R_s} \frac{V_{DD}}{1 + \rho} \frac{P_D}{P_0} \frac{\rho^2}{1 + \rho} \quad (5.34)$$

where

$$P_0 = \frac{3}{2} V_{DD} v_{sat} E_{sat} \omega R_s \quad (5.35)$$

Furthermore, an expression for the transconductance $g_m$ can be found by differentiating (5.29) with respect to $V_{gs}$, which gives

$$g_m = \left[ \frac{1 + \frac{\rho}{2}}{(1 + \rho)^2} \right] \left[ \mu_n C_{ox} \frac{W}{L} V_{od} \right] = \left[ \frac{1 + \frac{\rho}{2}}{(1 + \rho)^2} \right] g_{d0} \quad (5.36)$$

This not only gives the expression for $g_m$ but also $\alpha$ since $g_{d0} = \mu_n C_{ox} \frac{W}{L} V_{od}$ and $\alpha = \frac{g_m}{g_{d0}}$,

giving

$$\alpha = \left[ \frac{1 + \frac{\rho}{2}}{(1 + \rho)^2} \right] \quad (5.37)$$

To simplify things, $\rho \ll 1$ is assumed to be true, which is the case for circuits not operating in the high power regime. Using the simplification, and by substituting (5.27), (5.34), (5.36), (5.37), and (5.24), into (5.26) as well differentiating with respect to $\rho$ and setting the final expression to zero, the minimum noise figure can be found. The solution is shown below [10].
\[ \rho^2 \approx \frac{P_D}{P_0} |c| \sqrt{\frac{5\gamma}{\delta}} \left[ 1 + \sqrt{1 + \frac{3}{|c|^2} \left( 1 + \frac{\delta}{5\gamma} \right)} \right] \]  

(5.38)

Finally, by substituting the approximation of \( \rho^2 \) back into (5.34) the value for \( Q_s \) that gives the power-constrained minimum noise figure is given as

\[ Q_{sp} = |c| \sqrt{\frac{5\gamma}{\delta}} \left[ 1 + \sqrt{1 + \frac{3}{|c|^2} \left( 1 + \frac{\delta}{5\gamma} \right)} \right] \]  

(5.39)

To get a general approximation for the value of \( Q_{sp} \), a few assumptions on the values of the parameters, \( c, \gamma, \) and \( \delta \) must be made. As mentioned previously, the correlation factor \( c \) is assumed to be the theoretical long channel value of 0.395j. As for the gate and drain noise coefficients \( \gamma \) and \( \delta \), they will be estimated as 2 and 4 respectively, which is triple their long channel values of 2/3 and 4/3. This way, their increase from the long to short channel case will be conservatively accounted for. Plugging these values into (5.39) gives

\[ Q_{sp} \approx 4 \]  

(5.40)

Lee states that a more exact analysis gives a value closer to 4.5 [5]. Regardless, the noise figure is relatively insensitive to \( Q_{sp} \) values on the range from 3.5 to 5.5.

The final goal is to have an expression for the optimal width that gives minimum noise figure. If the value of \( Q_{sp} \) is taken as 4.5 or 9/2, then from (5.28), the expression for the width of a device is

\[ W = \frac{3}{2} \frac{1}{\omega LC_{ox} R_s Q_{sp}} = \frac{3}{2} \frac{2}{\omega LC_{ox} R_s 9} = \frac{1}{3\omega LC_{ox} R_s} \]  

(5.41)

To recap, noise optimization was done for a constant power dissipation. The noise factor expression from (5.26) was differentiated with respect to \( \rho \). Once the optimal width is found for a specified current, the bias point is set to achieving that current. In Chapter 6 it will be shown
that $\rho$ is related to the stage transconductance, $G_m$, through $\omega_T$. Therefore, the gain is not able to be set as a starting point. The design will then start by declaring a power budget and optimizing for it. In the traditional approach, the source noise is varied to optimize for specific device characteristics or vice versa. The power-constrained method outlined above takes advantage of the fact that better performance could be obtained for the same power when compared to the traditional approach. This is because the noise mismatch degradation can be more than offset by improvements to $\omega_T$ [10]. The result is a width decrease and an increase in overdrive voltage to keep the same current but raise the transit frequency.
CHAPTER 6 – DESIGN AND SIMULATION

As mentioned previously, a common-source amplifier topology with inductive source degeneration will be used for the design. The schematic including the biasing network is shown in Fig. 6.1. L1 is the source degenerative inductor previously referred to as $L_s$. Together, L2 and L3 make up the gate inductance for resonance, referred to as $L_g$. Here, a cascoding transistor, T2, is used to provide isolation from the output to the input. Its width is chosen to be equal to that of the main amplifying transistor T1. The load inductor L4 tunes out the output capacitance at the drain of T2. Current through the transistor T3 is set by R2, the supply voltage, and T3’s $V_{gs}$. R1 is made sufficiently large at 2 kΩ to be able to neglect its equivalent noise current.

![Fig. 6.1 LNA schematic](image-url)
6.1 Calculation of Component Values

Table 6.1 Key design specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>S21 (dB)</td>
<td>10 – 20</td>
</tr>
<tr>
<td>S12 (dB)</td>
<td>≤ -20</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>≤ -10</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>≤ 3.5</td>
</tr>
<tr>
<td>Power Dissipation (mW)</td>
<td>≤ 6</td>
</tr>
</tbody>
</table>

Table 6.1 summarizes the target specifications. The design begins by specifying a 6 mW power consumption through the amplifying branch. If after simulations the other values were not able to be met, consideration would have been given to increase the power. A supply voltage of 1.2 V gives a bias current of 5 mA. Therefore (5.41) is used to find the optimal width of T1 that would give the minimum noise figure for a 5 mA bias current. At an operating frequency of 433 MHz, the value of ω is about 2.72 Grps. The length L is 92 nm which is the technology’s effective minimum channel length. The source resistance $R_s$ comes from the antenna which is 50 Ω. Knowing the relative permittivity $\varepsilon_r$ to be 4.1 and the gate oxide thickness $t_{ox}$ as 3.15 nm, the gate oxide capacitance $C_{ox}$ is calculated as

$$C_{ox} = \frac{\varepsilon_0 * \varepsilon_r}{t_{ox}} = \frac{8.854 * 10^{-12} * 4.1}{3.15 * 10^{-9}} = 11.524 \text{ mF/m} \quad (6.1)$$

Having all the values necessary, the optimal width can be calculated as
\[ W = \frac{1}{3\omega L C_{ox} R_s} \]

\[ \approx \frac{1}{3 \times 2\pi \times 433 \times 10^6 \times 92 \times 10^{-9} \times 11.524 \times 10^{-3} \times 50} \]

\[ \approx 2,300 \text{ um} \quad (6.2) \]

(4.6) is used to find the values of the inductors \( L_s \) and \( L_g \), and is repeated below.

\[ Z_{in} \approx s(L_s + L_g) + \frac{1}{sC_{gs}} + \omega_T L_s \quad (6.3) \]

The approximation \( \omega_T \approx \frac{g_m}{C_{gs}} \) was used to find \( L_s \) at a bias current of 5 mA. In simulation \( \omega_T \) was found to be about 507 Grps. Having \( \omega_T \) and the value of the source impedance, \( L_s \) is calculated as

\[ L_s = \frac{50}{\omega_T} = \frac{50}{507 \times 10^9} \approx 1 \text{ nH} \quad (6.4) \]

Using (5.27), the value of \( C_{gs} \) comes to about \( 1.63 \text{ pF} \). The value of the inductor \( L_g \) is then calculated using (4.10), to give \( L_g \approx 80 \text{ nH} \). Due to technology limitations, two inductors in series were necessary to make up the total inductance.

The overall voltage gain can be found by finding the overall stage transconductance, \( G_m \).

At resonance, the voltage at the gate of the common source transistor can be found by multiplying the input voltage by the input quality factor \( Q_{in} \). The overall stage transconductance is then the device transconductance multiplied by \( Q_{in} \).

\[ G_m = g_m Q_{in} = \frac{\omega_T C_{gs}}{\omega C_{gs}(R_s + \omega_T L_s)} = \frac{\omega_T}{2\omega R_s} \quad (6.5) \]

Since the overall gain can be given as \( G_m R_{out} \) and \( R_{out} \) can be estimated by the output inductor’s equivalent resistance, the voltage gain can be given as
\[ A_v = \frac{R_d}{2\omega L_s} \]  

(6.6)

Now, the output inductor needs to only be set to tune out the output capacitance at resonance.

Even with \( R_d \) relatively small, the gain will still be sufficient. It may even be the case that the gain is too high. If so a resistor could be placed parallel to the inductor \( L_d \) to lower the output resistance. Using simulation, a value of 30 nH was sufficient for \( L_d \) to provide a good \( S_{21} \). Table 6.2 summarizes the calculated component values.

**Table 6.2 Calculated component values**

<table>
<thead>
<tr>
<th>Component Parameters</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>Source degeneration inductance</td>
<td>1 nH</td>
</tr>
<tr>
<td>L2</td>
<td>Gate inductance</td>
<td>40 nH</td>
</tr>
<tr>
<td>L3</td>
<td>Gate inductance</td>
<td>40 nH</td>
</tr>
<tr>
<td>T1 (W)</td>
<td>Common source transistor width</td>
<td>2300 µm</td>
</tr>
<tr>
<td>T2 (W)</td>
<td>Cascode transistor width</td>
<td>2300 µm</td>
</tr>
<tr>
<td>T3 (W)</td>
<td>Bias transistor width</td>
<td>230 µm</td>
</tr>
<tr>
<td>T1,2,3 (L)</td>
<td>All transistor lengths</td>
<td>120 nm</td>
</tr>
</tbody>
</table>
6.2 Testbench and Simulation Results

The simulation was performed using Cadence SpectreRF [11]. The component values arrived at in the previous section were tweaked using an iterative simulation process. The final values are listed in Table 6.3.

<table>
<thead>
<tr>
<th>Component Parameters</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>Source degeneration inductance</td>
<td>1.609 nH</td>
</tr>
<tr>
<td>L2</td>
<td>Gate inductance</td>
<td>38.585 nH</td>
</tr>
<tr>
<td>L3</td>
<td>Gate inductance</td>
<td>38.585 nH</td>
</tr>
<tr>
<td>L4</td>
<td>Output load inductance</td>
<td>27.371 nH</td>
</tr>
<tr>
<td>T1 (W)</td>
<td>Common source transistor width</td>
<td>1900 μm</td>
</tr>
<tr>
<td>T2 (W)</td>
<td>Cascode transistor width</td>
<td>1900 μm</td>
</tr>
<tr>
<td>T3 (W)</td>
<td>Bias transistor width</td>
<td>190.08 μm</td>
</tr>
<tr>
<td>T1,2,3 (L)</td>
<td>All transistor lengths</td>
<td>120 nm</td>
</tr>
<tr>
<td>R1, R2</td>
<td>Bias resistors</td>
<td>2.038 kΩ</td>
</tr>
</tbody>
</table>
Fig. 6.2 Testbench Setup

The testbench, shown in Fig. 6.2, is made up of two 50 Ω ports at the input and output. Capacitors C1 and C2 are 10 pF DC blocking capacitors and are made external. Load capacitor C3 models the next stage of roughly 15 fF. The input power is set to -20 dBm at a frequency of 433 MHz. The final power dissipation, including the biasing circuitry, was 6.42 mW. A summary of the simulation results is shown in Table 6.4. Each parameter is discussed in further detail below. All simulation results were of the parasitic extraction views from the final layout.

Table 6.4 Simulation results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF (dB)</td>
<td>2.85</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>-18.87</td>
</tr>
<tr>
<td>S21 (dB)</td>
<td>18.3</td>
</tr>
<tr>
<td>S12 (dB)</td>
<td>-37.4</td>
</tr>
<tr>
<td>Rollett Stability</td>
<td>3.05</td>
</tr>
<tr>
<td>1dB Compression Point (dBm)</td>
<td>-12.41</td>
</tr>
<tr>
<td>Total Power Consumption (mW)</td>
<td>6.42</td>
</tr>
</tbody>
</table>
6.2.1 S-parameters

The S-parameter simulations were ran using an SP analysis, which is the most useful linear small-signal analysis for LNAs. The frequency was linearly swept from 1 MHz to 1 GHz with a 0.1 MHz step size. Fig. 6.3 shows the $S_{11}$, which is an indicator of how well the input is matched. At 433 MHz, the value is -18.87 dB. Usually, a value of -10 dB is acceptable which means the input is well matched. From Fig. 6.4, the $S_{21}$ is 18.3 dB at 433 MHz. This is within the acceptable range of 10 – 20 dB. The $S_{12}$, shown in Fig. 6.5, is -37.4 dB at 433 MHz. This is good enough to effectively isolate the input from the output. The output reflection coefficient is not shown since it was largely meaningless for the application as the output was not matched to 50 $\Omega$ [12]. This is because the next stage was to a peak detector. For stability, the $S_{22}$ only needs to be below zero.

![Fig. 6.3 Input reflection coefficient $S_{11}$](image)
6.2.2 Comparison of Power Gains

The same analysis was used to obtain the operating, available, and transducer power gains. A comparison of the three in simulation is useful for analyzing if the power available was the power delivered. The transducer gain, GT, is the ratio of power delivered to the load to the power available from the source. The operating power gain, GP, is the ratio of the power delivered to the load to the power delivered at the input of the device. Since the two are very
similar at 433 MHz, the input can be said to be well matched. In other words, the available and actual powers at the input are about the same. The available gain $G_A$ indicates that most of the available power at the output of the device is actually delivered to the load.

Fig. 6.6 Simulated comparison of the operating, available, and transducer power gains

6.2.3 Noise Figure

The noise figure was also simulated by using the small-signal SP analysis. The frequency is also swept across the 1 MHz to 1 GHz range. Fig. 6.7 shows the actual noise figure, $NF_{dB}^{10}$, as well as the minimum noise figure achievable, $NF_{min}^{dB}$. At 433 MHz the actual noise figure is shown to be 2.85 dB. It can be seen that a compromise between low noise and high gain is made at the input. The minimum achievable noise figure shown is 1.7 dB at 433 MHz. This value would be achieved if the source admittance $Y_s$ was set equal to the optimal admittance, $Y_{opt}$. Fortunately, using the power-constrained noise optimization method, the actual noise figure was able to get close to $NF_{min}$ by a little over 1 dB.
6.2.4 Stability

Stability is important for any amplifier. When an amplifier is considered unconditionally stable it means it is stable for any source and load impedance where the real part is positive. The Rollet stability factor, $k$, is the most commonly used measure of stability and is defined as [13]

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \quad (6.7)$$

where

$$\Delta = |S_{11}S_{22} - S_{12}S_{21}|. \quad (6.8)$$

For unconditional stability to be achieved it is required that $k > 1$ is met. This is not only desired for frequencies close to the operating frequency but also for those that are far from it. That is because unwanted signals with varying frequencies can still be present at the input.
For this reason, it is important to observe the stability factor from 0 Hz up to the frequency where the maximum available gain of the amplifier drops below unity, also known as $G_{\text{max}}$. Fig. 6.8 shows $G_{\text{max}}$ in decibels plotted as a function of frequency. It can be seen to cross the 0 dB axis at a frequency of about 2.6 GHz. The $k$ factor shown in Fig. 6.9 was therefore plotted up to 3 GHz. The criteria for unconditional stability is again $k > 1$. This is met for the entire frequency range of interest. At the operating frequency of 433 MHz, the value is 3.05 and at the $G_{\text{max}}$ frequency it is 11.29. The minimum occurs at roughly 370.5 MHz with a value of 2.96. The amplifier is therefore considered unconditionally stable.
6.2.5 Linearity

A linear relationship between the output and input is very important for maintaining good sensitivity and suppressing interferences. One common measure of linearity is called the 1 dB compression point. As the input power is swept, the gain of the device is tracked until it decreases, or compresses, by 1 dB. A graphical representation is shown in Fig. 6.10. The input power is shown on the x-axis with the output power on the y-axis. The ideal gain is extrapolated out and wherever the actual gain falls below 1 dB of the ideal linear gain is where the 1 dB compression point is located.
The analysis is made using a large signal periodic steady-state analysis (PSS). The sweep is done from -40 dBm to 10 dBm. It is common to express the point in terms of the input power that caused the nonlinearity. From Fig. 6.11, the input referred 1 dB compression point is -12.41 dBm.

Fig. 6.10 Representation of 1 dB compression point [14]

Fig. 6.11 Simulated 1 dB compression point
6.3 Comparison to Similar LNA Designs

To give a sense of the expected performance of the LNA presented here relative to other work, Table 6.5 shows a comparison among several similar designs. The comparisons include both simulated and experimental results, with the distinction noted, as well as various frequencies. From these efforts, the minimum power dissipation is at 2 mW. With this design, the power level is an improvement compared to the simulations of the work presented here, but both the noise figure and gain degrade to 3.1 dB and 10 dB, respectively.

The two designs that provide the highest gain are both above 20 dB. Though the noise figure for both is under 3 dB at about 2.7 dB for each. The power consumption is quite large with both above 16 mW.

The second entry shows a similar power level to this work at 7.5 mW, with an improvement in noise figure at 1.25 dB but a degradation of the gain to 13.5 dB.

The first entry does a similar job of balancing the various parameters at a lower power level of 3.96 mW. The gain in the design is lower at 16 dB. The $S_{11}$ also is worse at -11.8 dB. By observing these other works, the LNA designed here can confidently be said to be well balanced considering the gain, noise figure, and power consumption.
Table 6.5 Comparing similar LNA designs

<table>
<thead>
<tr>
<th>Simulation or Experimental [Reference]</th>
<th>S21 (dB)</th>
<th>S12 (dB)</th>
<th>S11 (dB)</th>
<th>NF (dB)</th>
<th>Pd (mW)</th>
<th>1 dB CP (dBm)</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Exp. [15]</td>
<td>16</td>
<td>-35.8</td>
<td>-11.8</td>
<td>2.4</td>
<td>3.96</td>
<td>-13</td>
<td>431 MHz</td>
</tr>
<tr>
<td>Exp. [16]</td>
<td>13.5</td>
<td>-60</td>
<td>-11</td>
<td>1.25</td>
<td>7.5</td>
<td>-26</td>
<td>433.92 MHz</td>
</tr>
<tr>
<td>Sim. [17]</td>
<td>23.9</td>
<td>N/A</td>
<td>-17.9</td>
<td>2.73</td>
<td>16.17</td>
<td>N/A</td>
<td>2.4 GHz</td>
</tr>
<tr>
<td>Exp. [18]</td>
<td>10</td>
<td>-20</td>
<td>-10</td>
<td>3.1</td>
<td>2</td>
<td>N/A</td>
<td>2.4 GHz</td>
</tr>
<tr>
<td>Exp. [19]</td>
<td>9.5</td>
<td>N/A</td>
<td>N/A</td>
<td>3.5</td>
<td>10</td>
<td>-4</td>
<td>2 GHz</td>
</tr>
<tr>
<td>Sim. [20]</td>
<td>23.54</td>
<td>-47.51</td>
<td>-21.18</td>
<td>2.7</td>
<td>16.5</td>
<td>N/A</td>
<td>2.4 GHz</td>
</tr>
<tr>
<td>Sim. [This work]</td>
<td>18.3</td>
<td>-37.4</td>
<td>-18.87</td>
<td>2.85</td>
<td>6.42</td>
<td>-12.41</td>
<td>433 MHz</td>
</tr>
</tbody>
</table>
CHAPTER 7 – LAYOUT CONSIDERATIONS

7.1 Circuit Layout

In RFIC design, the layout of the circuit can have a considerable impact on performance. Therefore, taking proper care is critical for ensuring a successful design. Trace length is usually kept short to reduce parasitics along with the need to pay attention to impedance control. A rule of thumb for when trace length should be considered a transmission line is if it exceeds a tenth of the wavelength. At a frequency of 433 MHz, the wavelength is roughly 692 mm. Any trace in the layout will be far below one tenth of this length, therefore transmission line effects are not taken into account.

![Fig. 7.1 Full LNA layout](image)

The final layout for the LNA is shown in Fig. 7.1. The inductors take up the majority of the space and make up the main footprint. These inductors are made as octagonal single planar spirals. They were selected from other variations due to a high Q and low parasitic capacitance. The separation between different inductors was made a distance of at least 20% of the larger
inductor’s diameter. According to the PDK training manual, this helps to keep the mutual coupling coefficient to less than 0.1. The inductors also contain a ground plane shield made up of metal to isolate them from substrate noises. They also help prevent induced currents within the substrate. Most noise issues due to coupling come from the capacitive coupling between networks. Care is taken to reduce parallel signal traces and keep intersections as perpendicular as possible.

Reducing resistive parasitics is important for reducing thermal noise. Therefore, it is important to keep signal traces wide. This is done in the transistors by implementing multiple gate devices. This helps minimize thermal noise contribution from the gate. Both the common source transistor and the cascode transistor were divided into 95 fingers with an individual width of 20 μm. Contacting both ends of the device with a metal-to-poly contact ring helps in reducing the resistance further. Substrate guard rings are used around the devices to provide shielding and a low impedance return path to ground [21]. The layout for both the common source and cascade transistors is shown below in Fig. 7.2.

![Fig. 7.2 Common source and cascade transistor layout](image)
7.2 PCB Layout

The PCB layout is shown in Fig. 7.3. The chip contained various other circuits and therefore the board was made to include testing for all the circuits. The section outlined in red contains the LNA components. A 4-layer board patterned as signal, ground, power, and ground was used. This helps with the RF decoupling of the power supply. A 1 \( \mu \)F power supply bypass capacitor was also placed close to the chip. 50 \( \Omega \) SMA connectors were used at the input and output ports of the LNA. Lastly, the RF signal traces on the PCB were treated as transmission lines and therefore the width was taken into account to match the characteristic impedance to 50 \( \Omega \). An illustration of the parameters that make up the characteristic impedance is shown in Fig. 7.4. The parameters \( w, t \, CU \), and \( h \) represent the trace width, trace thickness, and dielectric
thickness, respectively. With a trace thickness of 18 – 35 μm, a dielectric thickness of 110 μm, and a dielectric constant of 4.3, the width required for a 50 Ω characteristic impedance was about 0.19 mm. An attempt was made to keep the signal lines straight but when necessary 45-degree bends were used.

Fig. 7.4 Microstrip transmission line
CHAPTER 8 – TEST RESULTS

All tests were done with a 1.2 V supply to the amplifier using a HAMEG HM7044 power supply. For a more accurate power dissipation measure, a Keithley SourceMeter was used. It showed a dissipation of 6.3 mW.

8.1 S-parameters

The S-parameters were measured with a Keysight E5061B ENA Vector Network Analyzer. Before running the test, instead of connecting the board to the input and output cables, a calibration kit is put in place. After calibration is done, without much movement to the current cable placements, the kit is replaced with the board. The frequency ranges from 0 – 3 GHz for all S-parameter measurements.

The $S_{11}$ is shown in Fig. 8.1 and has a value of -5.3 dB at the operating frequency. This is outside the goal specification and worse than the expected value. The measured $S_{21}$ is shown in Fig. 8.2. At 433 MHz the value is 12.24 dB. This value is within the specified range but worse than expected. Finally, the $S_{12}$ is shown in Fig. 8.3. with a value of -32.9 dB at 433 MHz. This is close to simulation and provides good isolation from output to input.
Fig. 8.1 Measured input reflection coefficient, $S_{11}$

Fig. 8.2 Measured forward transmission coefficient, $S_{21}$
Fig. 8.3 Measured reverse transmission coefficient, $S_{12}$

8.2 Noise Figure

The noise figure measurements were made based on the Y-factor method [22]. This method consists of using a noise source to provide two known levels of input noise to the device and a power detector. The noise source used was an NC346A model from ValueTronics. For power detection, a Tektronix MDO4034B-3 mixed oscilloscope with a spectrum analyzer was used. The equation below can be used to find the noise factor of a system that includes the noise measurement system as a second stage.

$$F_{sys} = \frac{ENR}{Y - 1}$$  \hspace{1cm} (8.1)

Here ENR is the excess noise ratio and $Y$ is called the Y-factor. ENR is the ratio, expressed in dB, of the difference between $T_h$ and $T_c$ divided by 290 K. The parameters $T_h$ and $T_c$ are the
equivalent noise temperatures when the source bias is on and off respectively. The ENR is expressed below

\[
ENR = 10 \log \left( \frac{T_h - T_c}{290K} \right)
\]

(8.2)

For the noise source used, the ENR near the operating frequency range is 6.8 dB.

With the noise source connected to the device under test (DUT), the Y-factor is given as the ratio between the output power corresponding to the noise source on and the noise source off. It is expressed as

\[
Y = \frac{N_2}{N_1}
\]

(8.3)

where \(N_2\) is the power measured with the noise source on and \(N_1\) with the noise source off. Since the noise of the measurement system is also included it is important to de-embed it. Recalling that the noise factor of a system can be written using Friis’ formula and in terms of the noise factor of the individual stages, the expression for the DUT noise factor can be written as

\[
F_1 = F_{sys} - \frac{F_2 - 1}{G_1}
\]

(8.4)

\(F_1\) is the noise factor of the DUT, \(F_2\) is the noise factor of the measurement device, and \(G_1\) is the gain of the DUT. To measure the noise factor of the measurement device, the same Y-factor method is used with the noise source directly connected to the spectrum analyzer.

The results are shown below in Fig. 8.4. At 433 MHz the noise figure is 4.99 dB. The average value within the displayed range is 3.77 dB. The reason for the increase in the measured noise figure can be attributed to several factors. The accuracy of the spectrum analyzer can be a large source of noise figure measurement uncertainty but it is still likely the true measured noise figure is still higher than the simulated. Possible areas where the noise was unaccounted for are parasitic bond pads and wires, as well as PCB parasitics. Also, due to the sensitivity of RF
circuits, external wireless signals can affect the measurement. Isolation from external signals could have been improved with the use of a faraday cage [23].

![Noise Figure](image1)

**Fig. 8.4 Measurement of noise figure**

### 8.3 Stability

![Rollet Stability Factor](image2)

**Fig. 8.5 Measured Rollet stability factor**

The measure of stability was done using the S-parameters. With MATLAB’s RF Toolbox, the Rollet stability factor defined in (6.7), was obtained. Aside from the second
frequency of 1.9 MHz, the value never goes below 1. This is most likely attributed to start-up conditions. For all other plot points, it is evident that the amplifier is unconditionally stable across the frequency range of 0 – 3 GHz. This includes the operating frequency where the value is 2.81.

8.4 Linearity

For the measurement of the 1 dB compression point, the gain at 433 MHz was measured across input power. The starting input power was -45 dBm, where the gain was 12.26 dB. This was used as the reference to check where the gain dropped by 1 dB or went below 11.26 dB. Fig. 8.6 shows the gain vs input power plot. At -5 dBm the gain finally drops by more than 1 dB at 10.73 dB. The input-referred 1 dB compression point is therefore about -5 dBm. This is a better value than that of the simulated prediction. This is most likely due to the reduced gain of the amplifier.

Fig. 8.6 Measured 1 dB compression point
8.5 Comparison to Simulation and Possible Improvements

Table 8.1 Comparison of simulated and measured results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Simulated Value</th>
<th>Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF (dB)</td>
<td>2.85</td>
<td>4.9</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>-18.87</td>
<td>-5.3</td>
</tr>
<tr>
<td>S21 (dB)</td>
<td>18.3</td>
<td>12.24</td>
</tr>
<tr>
<td>S12 (dB)</td>
<td>-37.4</td>
<td>-32.9</td>
</tr>
<tr>
<td>Rollet Stability</td>
<td>3.05</td>
<td>2.81</td>
</tr>
<tr>
<td>1dB Compression Point</td>
<td>-12.41</td>
<td>-5</td>
</tr>
<tr>
<td>(dBm)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Dissipation (mW)</td>
<td>6.42</td>
<td>6.3</td>
</tr>
</tbody>
</table>

Table 8.1 shows a summary comparing the simulated and measured results. Testing revealed the amplifier as functional with some metrics performing worse than expected. The $S_{11}$, $S_{21}$, and noise figure are the parameters that would most likely be improved upon given a redesign. The measured $S_{11}$ was below the expected results by about 13 dB. The $S_{21}$ was under by about 6 dB. Noise figure exceeded the simulations by about 2 dB.

The likely culprit for the $S_{11}$ and $S_{21}$ degradation was not accounting for parasitic inductances included in the degeneration inductor. This could come from the added inductances in the bond wire or PCB traces. This would affect both the 50 Ω resistive input and the cancellation of reactances. Fig. 8.7 shows simulation results for the $S_{11}$ and $S_{21}$ with some
additional inductance at the source. Increasing the inductance from 1.6 nH to just 5 nH degraded the $S_{11}$ to -8.32 dB and the $S_{21}$ to 13.85 dB. These values are much closer to the measurements and the minimum peak for the $S_{11}$ also shifts to the right much like the measured $S_{11}$. In the event of a redesign, the source inductor would most likely be internally removed and made up of the parasitic inductances. If additional inductance would be needed the amount of area needed on the PCB would be very small.

![Graph showing Simulated effect on $S_{11}$ and $S_{21}$ of a 5 nH source inductance](image)

**Fig. 8.7 Simulated effect on $S_{11}$ and $S_{21}$ of a 5 nH source inductance**

The integrated gate inductors may also have added unwanted coupling. In the event of a redesign, consideration would be given to make some of the gate inductance external even if some more area is needed on the PCB. This would avoid placing two planar inductors side by side and add flexibility in changing the values.

For the noise figure, measurement uncertainty could have been a factor. This uncertainty can come from several sources such as impedance mismatch, the excess noise ratio uncertainty, and receiver measurement variation. The reduction of parasitics in several areas may also improve noise performance. An increase in the number of gate fingers and a decrease of
individual widths may reduce the thermal noise from the gate [24]. Finally, as mentioned previously, a Faraday cage could eliminate other unwanted signals in the air.
CHAPTER 9 – CONCLUSION

The work presented outlined the design and testing of a low noise amplifier operating at 433 MHz. Since low area and power consumption were critical in the end application, the chosen design method was based on a constrained power optimization. To understand how power consumption played a role in noise performance, the design started with the generic classical two-port noise model. The noise model was used to find an expression for the minimum noise figure. From this, the noise parameters necessary to describe the model were found for a MOSFET. These parameters were then expressed in terms of power dissipation. Taking into account a given source impedance, operating frequency, technology, and power dissipation, an expression for device width was found that would minimize noise figure.

After the width of the device was found, the matching networks were investigated. At the input, transit time effects within the channel of the device are taken advantage of to vary the real part of the input impedance. The use of an inductor at the source of the amplifying device allowed a real 50 Ω impedance at the operating frequency. This meant input matching was possible without the use of an actual physical resistor that would add thermal noise. An additional inductance was then added before the gate at the input to provide resonance without affecting the 50 Ω match. The output inductor was based on sufficiently tuning out a DC blocking capacitor in series with a gate capacitance from a peak detector. The circuit also contained a simple self-biasing network.

Simulation using SpectreRF was used to tune each parameter value. This was done to reach satisfactory values for the S-parameters, noise figure, power dissipation, stability, and linearity. Care was taken in both the integrated circuit and PCB layout processes to reduce noise.
sources such as coupling and parasitic resistances. The device was fabricated using a SiGe BiCMOS8HP 130 nm technology from GLOBALFOUNDRIES.

Test results showed a decrease in performance relative to simulations with possible functionality for the end application. It was shown in simulation that the $S_{11}$ and $S_{21}$ parameters were sensitive to a few extra nH’s of inductance at the source. Better preparation for external parasitics could improve the design in terms of these parameters. It is strongly believed that for the same power level, either noise, gain, or both could be improved upon in this technology.
BIBLIOGRAPHY


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