Design and Simulation of Power Electronics Modules

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

by

Haonan Jia
Binzhou University
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University of Arkansas

This thesis is approved for recommendation to the Graduate Council.

______________________________
Simon S. Ang, Ph.D.
Thesis Director

______________________________
Fang Luo, Ph.D.                          Roy A. McCann, Ph.D.
Committee Member                        Committee Member
ABSTRACT

Silicon carbide (SiC), a wide-bandgap semiconductor material, greatly improves the performance of power semiconductor devices. Its electrical characteristics have a positive impact on the size, efficiency, and weight of the power electronics systems. Parasitic circuit elements and thermal properties are critical to the power electronics module design. This thesis investigates the various aspects of layout design, electrical simulation, thermal simulation, and peripheral design of SiC power electronic modules. ANSYS simulator was used to design and simulate the power electronic modules. The parasitic circuit elements of the power module were obtained from the device parameters given in the datasheet of these SiC bare devices together with the model established in the Q3D simulator. A temperature simulation model is established using SolidWorks to investigate the thermal performance of the power module. The designs of soldering and sintering fixtures are presented. A 1.7kV silicon carbide (SiC) junction field-effect transistor (JFET) cascode power electronic module was designed as an example. By comparing the different module designs, some conclusions are elucidated.
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Chapter 1. Introductions

Power semiconductor devices are the core circuit elements to realize power conversion and control in power electronics applications. Due to its stable chemical properties, silicon carbide (SiC) has high thermal conductivity, a small coefficient of thermal expansion, and a high breakdown electric field. Its device properties surpass those of the conventional silicon (Si) based power semiconductor devices. By comparing the 4H-SiC with the traditional Si, the SiC power devices can operate at high temperature in the several hundred-degree centigrade and have ten times the breakdown voltage of those Si power devices [1]. SiC power devices made an appearance since the 1970s. Nowadays, silicon power devices have almost reached their physical property limits [2]. The application of SiC broadens the field for the development of power electronics. Because of these advantages, SiC power devices have been widely used in uninterruptible power supply, AC motor driver, electric energy vehicles, and other fields [3]. In these applications, DC voltages often exceed 1000V, while AC voltages range from 480 to 650AC.

This thesis reports the design and simulation of 1.7kV power modules. First, the modules were laid out according to design requirements. Choosing the appropriate topology is the first step of the power electronics module design. Then, a three-dimensional (3D) model design was built using the ANSYS software. The parasitic inductance and thermal simulation of the system were studied for each module. Thermal simulations were performed using the SolidWorks software.

Chapter 1 provides the rationale for this thesis study. Chapter 2 describes the tutorial for using the various software tools to design and simulate the power electronic modules. Chapter 3 presents the designs for the cascade power electronic modules. Chapter 4 presents the simulation and peripheral designs for the module. Chapter 5 presents the fixture design process. Chapter 6 concludes this thesis study.
Chapter 2. Power Module Design and Simulation

This chapter gives the tutorial for the various design tools for the power electronic modules. The use of the ANSYS Electronics Desktop simulation tool is described in detail. This includes the layout design, electrical simulation, and thermal simulation of the power electronic modules.

2.1 Electrical Modeling of Power Module Using ANSYS Q3D

2.1.1 Introduction

This design uses ANSYS to model the power module. ANSYS is the finite element analysis (FEA) software developed by ANSYS Corporation. ANSYS can be used with most computer-aided-design software (SolidWorks CAD) to complete the power module design and simulation. It also provides many functions to verify the reliability and performance of electronic devices. In ANSYS 16.0 and subsequent releases, the ANSYS Electronics Desktop application combines electromagnetic fields, circuitry, and system analysis into a seamless working environment within a single, highly integrated interface. This tool is adopted for the design and simulation of the power modules in this thesis. The basic procedures for using this software are:

- Draw a geometric model.
- Modify a model's design parameters.
- Set up a simulation.
- Run a simulation.
- Review the results.

2.1.2 Draw a Geometric Model

After double-clicking on the icon to launch the ANSYS Electronics Desktop, a new project named “Project1” was created by default in the project management window. The “Project1” could
be used directly or a new project file could be created. Right-click on Project1 and insert a Q3D Extractor Design, the initial interface of the software is shown in Figure 2.1.

![Fig. 2.1. The initial interface of ANSYS Electronics Desktop.](image)

After right-clicking on the name of the project and insert a “Q3D Extractor Design” as shown in Fig. 2.2. Then click on the “Module-Units” in the menu bar to set the units for the model as “mm”.

![Fig. 2.2. Insert a Q3D extractor design in the Project Manager.](image)
The “Draw” function or the shortcut options in the toolbar can be used to draw the geometric model for the power module as shown in Fig. 2.3. A 4*2*1.3mm rectangle in ANSYS shows in Fig. 2.4. As shown, the “position” values are 2 mm, 4 mm, and -1.3mm. This means that a rectangle with dimensions of 2mm on the X-axis, 4mm on the Y-axis, and 1.3mm on the Z-axis is created. Fig. 2.5 shows the length, width, and height of the power module displayed in the parameter column. The dimensions of the power module (X = 76 mm and Y = 116 mm) are given in terms of “X Size”, “Y Size”, and “Z Size” are the maximum distance in three directions based on the initial position of the module.

Fig. 2.3. Path of Draw-Box and Draw box icon.

Fig. 2.4. A 4 *2*1.3mm basic object in ANSYS.
Fig. 2.5. Geometric parameters of the power module in ANSYS.

Dragging objects directly can always cause problems in a 3D display drawing interface. The most common problem with dragging an object directly is the movement of coordinates beyond what is expected. The objects could be moved precisely by modifying the values of $dx$, $dy$, and $dz$. Figure 2.6 shows the operation of adjusting $dx$, $dy$, and $dz$ parameters to move the object in the process of making fixtures. The irregular shape of the object makes it difficult for the software to determine the reference point, moving the object directly will fail due to the lack of reference points. This kind of movement also avoids the overlap of the two objects to some extent.

As shown on the toolbar in Fig. 2.7, most of the devices are a cuboid combination. Hence, the irregular shape objects could be drawn by combining various functions. For example, the DBC's lower layer of copper and ceramic plates are cuboids, but the upper layer of copper will have different shapes depending on the layout. Operations that combine simple objects into complex objects include unite, subtract, intersect, split, and imprint. In a practical power module, there are many non-right-angle edges. Hence, it was necessary to adjust the right-angle radians in the software by right clicking the "select edge" function as shown in Fig. 2.8.
Fig. 2.6. Move an object to its proper position in ANSYS.

Fig. 2.7. Combine two objects into one in ANSYS.

Fig. 2.8. Change the right angle to an arc angle in ANSYS.
Next, right-click on the “drawn model” and “assign material” to input the material properties. The select definition dialog box appears as shown in Fig. 2.9. The materials can be selected according to the material list as shown in Fig. 2.10. For materials not shown, new material could be added as shown in Fig. 2.11. Although each component can be drawn to define the component's material, setting the material for each component after the entire module has been drawn usually reduces the simulation errors.

![Fig. 2.9. Assign material in ANSYS.](image)

![Fig. 2.10. The “Select material interface” in ANSYS.](image)
The power substrate, in our case a direct bond copper (DBC) substrate, has an aluminum oxide (Al₂O₃) or aluminum nitride (AlN) thickness of 0.635mm sandwiched by a 0.3mm of copper layer on the top and bottom. The AlN has a high thermal conductivity than that of the Al₂O₃. This also means that AlN has a higher unit price. SiC power devices are often used in the high voltage (>600V) modules while gallium nitride (GaN) power devices could be used for low voltage (<600V) modules.

Different module layouts are used to assess their module parasitic inductances. Wide and short current paths reduce the parasitic inductances of the circuit, but a shorter current path is a better choice. This is because the parasitic inductance is directly proportional to the length of its current path [4]. Fig. 2.12 shows the different layouts for a similar power module.
2.1.3 Modify a Model’s Design Parameters

The design parameters for the module terminals are illustrated. As shown in Fig. 2.13, the three copper terminals are 6mm wide, 31mm long, and 8mm tall. The center-to-center M3 (the outer diameter of the tap is 3mm) holes are 10.00~10.25mm. Fig. 2.14 shows the four rectangles that make up the terminals. Fig. 2.15 shows the construction of cylinders in rectangles. Finally, the geometric model of the terminal is obtained by subtracting the rectangle from the cylinder using the subtract function in the 3D modeler Boolean bar. The model of the terminal is shown in Fig. 2.16.

Fig. 2.13. Terminal size parameters used in this design.
Fig. 2.14. The four rectangles that make up the terminals.

Fig. 2.15. The construction of cylinders in rectangles.

Fig. 2.16. The model of the terminal in ANSYS.
The electrical interconnections were drawn in ANSYS using the “Draw Bond wire” button or the “Draw Bond wire” in ANSYS. The diameter and number of bond wires are determined according to the current-carrying capacity of the bond wire conductor and the rated current requirements of the power module. Aluminum and copper bond wires are usually used in the power electronic modules. Aluminum wires have a high current density and a relatively lightweight. Generally, the diameters of the aluminum bond wire are either 0.3048mm (12mil) or 0.127mm (5mil). The 5mil-diameter aluminum bond wire is used for signal interconnections. Wire bonds of different diameters can carry different levels of current. A 5mil-diameter aluminum bond wire can carry a 5A current while the 12mil-diameter aluminum bond wire can carry a 21A current. The number of bond wires is determined according to different design requirements. When drawing the bond wires, it is important not to let bond wire get too close to the edge of the copper layer as this may cause problems in actual wire bonding. For a high current interconnect, a 12mil bond wire is usually selected. The larger diameter bond wire needs higher ultrasonic energy for the bonding process. For the signal or gate interconnect, a 5mil bond wire is enough. Fig. 2.17 shows the bond wires of different diameters.

![Fig. 2.17. Bond wires of different diameters in the power module.](image)

The height of the bond wires is also important. In the ANSYS software, two bond wires shall not intersect or cross each other. This is also not allowed in actual welding. The height problem of wire bonding should also be considered in the later fixture design process. Fig. 2.18
shows the parameter settings for the “Draw Bond wire” command. As shown, the diameter of the bond wire is 0.025mm with heights h1 of 0.2mm and height h2 of 0.18mm.

![Parameter settings of a bond wire](image)

**Fig. 2.18. Parameter settings of a bond wire.**

### 2.1.4 Set Up and Run a Simulation

The parasitic inductance and resistance values are calculated by first setting the source and sink for the designed module. The specific area was selected by right-clicking on the drawing area and selected the “Select Faces” option as shown in Fig. 2.19. One face of the module model was selected and then assigned “Excitation as Source or Sink” as shown in Fig. 2.20. This is because the source and sink cannot be set in whole or in part on a surface that is at the intersection of two conductors. If the source and sink are set on such a contact surface, the software will then fail to simulate and report an error. It can be assumed that the current enters the plane as the source and leaves the plane as the sink. In general, the stray or parasitic inductances from the DC+ terminal to the DC- terminal are desired in a power module. A separate current source must be connected to each of the source terminals in the power module. Right-click on the “Select Face” function and then right-clicking on one face of the module model to select the “face”. This “face” can then be assigned as a source or a sink by right-clicking on the “Assign Excitation” function.
Each part of the circuit needs to be emulated separately because they are electrically connected. The conductivities of the materials are changed to separate the parts of the circuit. One approach is to set the substrate of the module as a non-conductor. Another method is to change the physical structure of the model and set the cube module to two cubes with very narrow space. This not only achieves electrical isolation, but also guarantees the accuracy of the subsequent simulation results. After setting up the source and sink for each group, the network is set up using the “Auto identify nets” function.
Right-click on the “Analysis” button, then click on “Add Solution Setup”. Assign the parameter you want to test, such as frequency, capacitance, conductance, DC resistance/inductance, and AC resistance/inductance, etc. Click on the “Q3D Extractor Validation Check” or “Validate” icon to do a check. If there are no errors, a table will display a validation check completed. Click on “Q3D Extractor Analyze All” or “Analyze All” icon to run the simulation. The analysis setting and validation check interface are shown in Fig. 2.21.

![Fig. 2.21. Analysis setting icon and validation check in ANSYS.](image)

When the simulation is completed, the simulation data can be obtained in the project using the “Manager-Results-Solution Data”. This is the basic process for drawing a power module using ANSYS Q3D.

### 2.1.5 Review the Results

When the simulation is complete, open the design tree to the left of the Q3D interface, right-click on the “Result”, then click on the “Solution Data”. In the solution dialog box, click on the “export >RLGC” and an export matrix dialog box appears as shown in Fig. 2.22. Locate and double-click on the folder where the export results are to be saved. Click on the “Modeler>Export”, the geometric model is then exported as a .step file.
2.2 Thermal Modeling for Power Module Using SolidWorks

This design uses SolidWorks as the temperature simulation software. SolidWorks is a Windows-based 3D CAD system and is relatively easy to use.

To launch the SolidWorks software, double-clicks on the “SolidWorks” icon in the ANSYS Electronics Workbench. The geometric model created using the ANSYS Q3D is then imported. Click on the “Open” button and then open the .step file. For modules imported from the ANSYS Q3D, the material for each component needs to be re-defined. Drawing the temperature module directly in the SolidWorks requires each component to be assigned. For simpler power modules, it is recommended to first import, and then, assign the materials. Fig. 2.23 shows the “Edit Material” icon.

Fig. 2.23. Edit material in SolidWorks.
For materials that are not in the library, click the “Custom Materials” button as shown in Fig. 2.24, then right-click on the library and select “New Material”. In the “Properties” window, the material parameters are defined and then these properties are adopted by clicking on the “Apply” button.

The thermal simulation is set up by clicking on “New Study”, then “Thermal” in “Advanced Simulation” and finally clicking on “√”. In the “Heat Power”, the faces of the power devices as power sources are selected. Define the heat power to be the dissipated power as either “Per Item or Total”. In the “Convection” part, heat dissipation surfaces are selected. The convection coefficient is defined in “Convection Coefficient”. The ambient temperature is defined as the “Bulk Ambient Temperature”.

The mesh size for the simulation is defined. In the “Thermal Study” window, right-click on the “Mesh”, and select “Create Mesh” as shown in Fig. 2.25. In the mesh window, modify the mesh density, mesh parameters, and advanced settings as needed. In general, the finer the mesh, the better the result.
If mesh selection has no error, thermal simulation can be performed next. Right-click on the “Mesh” button and select the “Mesh and Run”. When the simulation is complete, click the name of the thermal project in “Results” to display the temperature distribution plot as shown in Fig. 2.26. As shown, the regions with the highest temperature of 475K are colored red and these are where the SiC power devices are placed. The lowest temperature regions are in the middle of the power module where the negative terminal blocks are placed.

Fig. 2.26. A temperature simulation of a power in SolidWorks.
Chapter 3. Design of a SiC JFET Cascode Power Module

To improve the energy efficiency of high voltage power supply systems, designers often actively use economical high-performance power FET. The SiC FET with cascode structure can significantly improve the switching efficiency of the power supply system [5] because of the extremely low conduction and switching losses and the superior reverse recovery (Qrr) characteristics compared those of the conventional Si MOSFET [6]. SiC JFET common-source common-gate or cascode configuration is a hybrid device with the wide bandgap (WBG) semiconductor switching characteristics, as well as the flexibility and durability of Si MOSFETs. SiC JFET can be used in conventional power electronic systems as well as to design new power converters or inverters. SiC cascode is a modern adaptation of the conventional power electronic design method.

Silicon-based MOSFETs are limited by their slow reverse recovery performance of its bulk or body diode. The large current stress requires a larger safety margin rating for the device. The SiC JFET Cascode configuration shown in Fig. 3.1 allows the hybrid design to work in the continuous conduction mode. This design can effectively reduce current peak, improve efficiency, reduce inductor size, and optimize filtering and EMI problems at fixed operating frequencies. In this SiC JFET/Si MOSFET cascode switch, a SiC JFET is connected in series of a silicon based MOSFET. The gate of the Si MOSFET is the gate of the hybrid switch while the source of the cascode switch is the source of the Si MOSFET connected to the gate of the SiC JFET through a gate resistor. The drain of the SiC JFET is the drain of the cascode switch. A case study using UnitedSiC’s UJC06505K on a 1.5kW, 230 VAC system demonstrated a surprising 99.4% efficiency [7].
The purpose of using the SiC JFET cascode switch configuration is to improve the output impedance of the hybrid switch. The purpose of increasing the output impedance is to improve the constant-current characteristics of the constant-current source switch. In general, constant current sources are used for biasing purposes. When the Si MOSFET gate is at a logic high state, the MOSFET conducts and presents as a short across the SiC JFET gate and source, thus forcing SiC JFET to conduct. When the Si MOSFET gate voltage is low, its drain voltage increases until the SiC JFET gate-source voltage reaches about -7V. The SiC JFET is turned off and the Si MOSFET drain voltage drops to about 7-10V. The cascode switch is usually switched off, so the body diode of the Si MOSFET recovers quickly, with a very low reverse recovery charge and a reduced voltage drop [8]. These characteristics are derived from the fact that the Si MOSFET is a low voltage device.

For the designed power module, a SiC JFET (UF3N170006) bare die with two Si MOSFET (AW1060) bare dies to form a cascode switch. To increase current handling capability, 5 of these SiC JFETs are connected in parallel. Usually, the parasitic inductance decreases with increasing frequency. For this power module, the parasitic inductance is mainly introduced by the power and gate terminals, copper traces, and the bonding wires between the bare dies and copper traces on the DBC power substrate. The operating frequency is not too high, so the simulation needs to be in the range of 1 kHz to 10MHz. The size, spacing, terminal size, and other internal structure and
parameters of the DBC power substrate are first extracted. SiC JFET (UF3N170006) and Si MOSFET (AW1060) specifications can be obtained from their datasheets.

The power module comprises a 5.7 mΩ 1.7 kV SiC JFET paired with two 1.1 mΩ 35V Si MOSFETs in a cascode configuration. The low voltage MOSFET can be driven by a gate drive from 0V to 10V. Thus, one can use SiC devices without providing a negative gate drive or a high gate voltage (usually greater than 18V), as is the case for the SiC MOSFET. The reason for using one JFET with two MOSFETs is that the SiC JFET continuous drain current is 200A, while a single Si MOSFET continuous drain current is 100A.

According to the schematic diagram, except SiC JFET and Si MOSFET gate circuits, the rest of the interconnections are all high currents. The maximum continuous current for the SiC JFET is 200A, as such 10 aluminum bond wires of 12-mil diameters are desired. Similarly, one SiC JFET is paired with two Si MOSFETs, so each Si MOSFET’s drain and source must have five aluminum bond wires of 12-mil diameter.

After setting the sources and sinks in the ANSYS Q3D, the parasitic resistances and inductances are calculated. The current is defined to enter the source terminal and leave the sink terminal in the power module. However, the current flow direction set in the software from the source to the sink is the opposite of the actual current flow. The result of this simulation needs to be corrected by adding a minus sign. The influence of high di/dt on parasitic inductances should not be ignored under fast switching, especially in the multi-chip high power module (MCPM). Accurate estimation of parasitic inductances is very important to improve switch performance and ensure the safety and reliability of the power module [8]. Moreover, voltage isolation between power terminals must also be maintained. As such, proper spacing between high-voltage terminals should be maintained to abide by the voltage breakdown specifications.
In temperature simulation, multiple sets of parameters are usually tested. If the model is complex, this can be a very time-consuming process. According to the datasheet, the main heat sources in the power module are two sets of ten SiC JFETs. Bare dies near the edges of the power module affect the heat dissipation. This requires SiC JFETs to be distributed to dissipate the heat generated due to conduction and switching losses. The use of appropriate encapsulation is also conducive to overall cooling. This module uses a silicone encapsulation for environmental protection. Solidified silicone can reduce the temperature dissipation from the top of the power module due to its low thermal conductivity [9].

However, when silicone encapsulation is applied to the power electronic module, the presence of large air pockets or voids impedes further the thermal dissipation [9]. Because power modules are high-power switches, they generate a lot of heat which must be lost quickly enough to avoid overheating. Most of the heat dissipation is transferred down the DBC substrate to the base plate. The power devices are attached to the DBC ceramic power substrate using die attach materials which must be a high thermal conductivity material as shown in Fig. 3.2. The DBC substrate is soldered to the base plate, again using a high thermal conductivity material. Any void in this soldered layer will impede the thermal dissipation of this power module by reflecting the heat conducting back to the power device [10] as shown in Fig.3.2.

Fig. 3.2. The cross-sectional view of a power device attached to the DBC and heat sink.
An example of the layout of the 1.7kV SiC JFET cascode power module (116*76mm) is shown in Fig. 3.3. It consists of two separates SiC JFET cascode switches, one on the left and the other on the right of the power module. The power terminal blocks are on both sides of the module. Also shown are the gate terminals on the top of the power module. Fig. 3.4 shows the dimensional parameters for the power module.

Fig. 3.3. A 1.7kV SiC JFET cascode power model in ANSYS Q3D.

Fig. 3.4. The parameters of the power module.
Chapter 4. Simulation of a SiC JFET Cascode Power Module

Parasitic inductances introduced by electrical paths must be carefully managed in the power module as these inductances affect the fast switching characteristics of the SiC devices. The gate loop parasitic inductance causes the voltage oscillation in the gate circuit. The common source parasitic inductances reduce the switching speed and cause voltage oscillation. The extracted parasitic inductance can be imported into a circuit simulator software like the LTSpice to analyze the switching characteristics of the power module as shown in Fig. 4.1. As shown, the L1 and L3 are the common-drain and common-source parasitic inductances, respectively. The Lg-mosfet is the gate loop parasitic inductance while the Ls-mosfet is the parasitic inductance in the Kelvin source. The Kelvin source is the source connection for the gate circuit with no source current flow.

Fig. 4.1. 1.7kV SiC JFET cascode power module circuit diagram.

To determine these parasitic inductances, the network is to be established according to the equivalent circuit of Fig. 4.1 for the power module as shown in Fig. 4.2.
Fig. 4.2. Nets of the module for the power module (left part only).

Because bonding wires are on both sides of JFET, the five MOSFETs and JFETs are electrically connected. The parasitic inductance between the JFET gate and MOSFET source simulated by ANSYS is a total value, instead of five separate values for each group. If a single set of values is desired, the electrical connections between these five groups need to be isolated.

In the exported data shown in Table 4.1, the first set of data labeled as “AC Inductance Matrix” is used. The diagonal from the top left to the bottom right is the self-inductance value of each network. The rest of the data is the mutual inductance between the two networks [8]. Figure 4.3 shows the specific expression of inductance calculation formula in AC matrix. The calculation formula of stray inductance is:

\[
L_{\text{Module}} = L_1 + L_2 + L_3 + 2(M_{12} + M_{13} + M_{23})
\]  

(1)

Fig. 4.3. The expression of this formula in AC inductance matrix.
Table 4.1. The AC inductance simulation results of the designed module.

<table>
<thead>
<tr>
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Using these inductance values, the circuit model for the SiC JFET cascode power module is shown in Fig. 4.4. As can be seen, the Lg-jfet, Lg-mosfet, and L3 exhibit more than 2nH of parasitic inductances.

![Diagram of 1.7kV JFET cascode module](image)

**Fig. 4.4.** Parasitic inductances for the 1.7kV SiC JFET cascode power module.

To simulate the thermal performance for the 1.7kV SiC JFET cascode power module, a 3D model was first built in the Solidworks software. All surfaces in contact with air except the base of the module are normally set to normal air cooling. The cooling demand for the module bottom usually determines the cooling method to be selected [9]. Therefore, in the design of the power module, the power module is evaluated by assuming the heat dissipation parameters and the ideal heat dissipation state.

Power semiconductor die is placed on the DBC substrate (include a copper layer, AlN/Al₂O₃ layer, and another copper layer) and base plate. Because the solder layers between the power semiconductor die/DBC and DBC/base plate are very thin, these solder layers can be
ignored during the simulation. Similarly, in order to simplify the simulation time, bonding wire, as well as source and gate on the bare dies, which cannot have an effective impact on the simulation results, can also be ignored. It is impossible to avoid the heat dissipation of two adjacent high-power chips at such a module size without affecting each other. Because the distance would be on the order of tens of millimeters [9].

According to the datasheet, the Al₂O₃’s thermal conductivity at 20°C is 24 (W/mK), the AlN’s thermal conductivity at 20°C is 170 (W/m. K). However, AlN is more expensive than Al₂O₃. If higher performance is desired, AlN should be used as the substrate. If from an economic consideration, Al₂O₃ should be used as the substrate.

The module from ANSYS Q3D is imported into the SolidWorks or the module can be drawn directly in the SolidWorks. Then, the materials are defined. A new study can be started to simulate the temperature of the module. The simulation is designed to test the cooling conditions required by the tested module under specific conditions. There are four basic parameters: All surfaces in contact with air except the bottom surface, bottom surface, the bottom surface of all MOSFETs, and the bottom surface of all JFETs. For all surfaces in contact with air except the bottom surface, the convection coefficient value is about 25 W/m²K. For the bottom surface, the convection value depends on the cooling method applied to the power module. Also is the temperature simulation to determine the parameters. The heating powers for power chips (MOSFET and JFET) are obtained by the formula Id²R. Fig.4.5 and Fig.4.6 show the thermal models in ANSYS and SolidWorks, respectively.
Fig. 4.5. Thermal module in ANSYS Q3D.

Fig. 4.6. Thermal module in SolidWorks.

Fig. 4.7 shows the power module after defining the mesh. It can be seen that the module is divided into many parts to simulate the temperature. There are usually two ways to resolve errors: Let the mesh density is coarser or change the standard mesh to curvature-based mesh. Because the model of this module is relatively simple, the standard mesh can be used. The highest temperature usually occurs at the center of the power die. If the model is simple and there are no curved edges, the mesh usually does not report errors. Once bonding wires are added to the model, the software is very easy to report errors.
Fig. 4.7. Effect diagram of power module mesh.

Fig. 4.8 shows the worst-case temperature analysis at the maximum drain currents of the SiC JFET. All exposed surfaces except the bottom are set to dissipate heat with ordinary air. The material for the substrate is Al₂O₃. The difference in cooling conditions can be changed in the application. In the power module design, we assume that the cooler can effectively dissipate heat and ensure the temperature uniformity on the back of the base plate [11]. As the main cooling surface, the bottom surface selects the value (3000W/m²K) that can be achieved by forced water cooling. The SiC JFET's power dissipation is $I_d^2 \times R$ or 216W while the Si MOSFET’s power dissipation is $[I_d^2(JFET)]/2 \times R$ or 10.3W. The simulation results show that the junction temperature of SiC JFET reaches an astonishing 220℃. According to the datasheet of SiC JFET of this model, the recommended maximum operating temperature is 175℃ even though the operating temperature for SiC JFET is much higher. Junction Temperature ($T_j$) is the actual operating temperature of a semiconductor in a power device. The maximum junction temperature ($T_{j,max}$) is the maximum allowable temperature on a power module, usually at the center of the die.
Several layout schemes are designed and the best one is chosen. This chapter two 1.7kV SiC JFET cascode power module designs with dimensions of 114mm * 77mm and 116mm * 77mm. The only difference between the two module layouts is that the larger power module consists of two separate DBC power substrates. The use of two separate DBC power substrates has two distinct advantages. First, the thermal expansion coefficients of the DBC power substrate and base plate are different. This means that a smaller deformation occurs in the two DBC power module after the soldering process. The second point is that a smaller substrate is more economical for cutting. The substrates sold on the market are of fixed size, and smaller cuts can better improve the utilization of the substrates. Unfortunately, in order to reduce the area of the module, the four corners of the module require an oblique cutting design. The substrate is either AlN or Al₂O₃. This oblique corner design makes it easier to damage the substrate during the actual manufacturing process.

Figures 4.9(a) and (b) show the thermal simulation plots of two power modules with two DBC power substrates and a single DBC power substrate carrying 100A, respectively. The SiC JFET's thermal power dissipation is 57W and the Si MOSFET's thermal power dissipation is 2.75W. As shown in Figures. 4.9(a) –(b), the maximum junction temperature is 342K or 60°C for
a two-DBC power module compared to that of 338K or 65°C for a single-DBC power module when a convective coefficient of 5000 W/m²K is applied at the bottom of the base plate. Figures 4.10(a) and (b) show the thermal simulation plots of two power modules with two DBC power substrates and a single DBC power substrate carrying 150A, respectively. The SiC JFET's thermal power dissipation is 128.25W and the Si MOSFET's thermal power dissipation is 6.12W. Figures 4.11(a) and (b) show the thermal simulation plots of two power modules with two DBC substrates and a single DBC power substrate carrying 200A, respectively. The SiC JFET's thermal power dissipation is 228W and the Si MOSFET's thermal power dissipation is 11W.

Fig. 4.9. Thermal simulation for the power module with 100A.

Fig. 4.10. Thermal simulation for the power module with 150A.
By comparing the temperature simulation results of the two power module substrate designs under three operating conditions, it can be found that the maximum temperatures for the two-DBC version are always higher than the one with just one DBC. Although the difference between the two simulation results is not large, it can be determined that the version of a single DBC has better heat dissipation than the two-DBC version. The advantage of the power module with two DBC power substrate is to reduce the warpage of the DBC power substrate and the base plate after their soldering.
Chapter 5. Fixture Design

Fixtures are used during the die attach as well as the terminal attachment processes in the course of power electronic fabrication. The function of the fixture is to hold the semiconductor dies or terminals in place during the soldering or sintering process. Three fixtures are required for the designed power module. This is because a single fixture cannot complete the process. The designs for these three fixtures are shown in Fig. 5.1. Fixture A is used for soldering between the DBC power substrate and the copper base plate as well as for soldering between the semiconductor bare dies and the DBC power substrate. Fixture B is used in conjunction with fixture A to provide proper pressure on the semiconductor bare dies to enhance the soldering process. After the die attachment, DBC and base plate soldering, wire bonding is performed to electrically connect the semiconductor dies to the interconnections on the DBC substrate. Fixture C is used for the electrical terminal soldering process after the die attach, DBC and base plate attachment process is completed. Fixture C leaves rooms for the wire bonding. It is not an option to do the wire bonding after terminal soldering as the electrical terminals will block the movement of the wire bonding machine. Fig. 5.2 shows the application scenario fixtures A and C.

Fig.5.1. Three fixtures designed for this project.
For power dies, the hollow out area size in fixture A is usually 0.05mm longer than the length of each side of the die, which means the gap on each side of the die is 0.025mm. Take MOSFET AW1060 as an example, its size is 2.83mm * 4.32mm, so the size of the hollow out area is 2.88mm * 4.37mm. For DBC, the design requires the hollow areas to be 0.3mm larger than the dimensions of the DBC on each side. This means that each side needs a gap of 0.15mm. For the base plate, a hollowed-out area of 0.5mm larger than the size of each side of the base plate is required. This means that a gap of 0.25mm is required on each side.

Therefore, for this design, the dimensions for the base plate are 116mm * 76mm. The external dimensions of fixture A are then 121mm * 81mm. The fixture thickness of the base plate layer shall be less than the thickness of the base plate. This is because this design allows the fixture to be pressed against the module better. The base plate of this module is a 3mm copper plate, so the fixture substrate layer is set as 2mm. The specific parameters for fixtures A and C are shown
in Fig. 5.3.

Fig.5.3. The specific parameters of fixtures (a) A and (b) C.

The purpose of designing “dog-ear” holes in the fixtures is to facilitate adjusting the position of die or terminal. The size of the base plate and DBC is relatively large, and whether the “dog-ear” hole is designed has no obvious effect on the position adjustment. Normally, the “dog-ear” hole is only present in the die during the design process. The diameter of the “dog-ear” cavity is usually between 0.5mm and 1mm. The smaller the size of the hollow out area, the higher the height requirements of the hollow out area. This is because too deep a hollow out area will result in a cross-section of the hollow out area is a trapezoid with a wide top and a narrow bottom. For this reason, the depth of the hollow area should less than or equal to 2mm.

The three acceptable “dog-ear” designs are shown in Fig. 5.4. The most preferred bare die “dog-ear” is the first design on the left. The diameter of the “dog-ear” hole can be 0.5mm when the bare die is smaller than 5mm * 5mm, but the fixture’s thickness should not exceed 0.8mm.
Fig. 5.4. Three possible designs for dog-ear.

The length of the pin depends on the thickness of the die and the thickness of the fixture plus 0.11 mm to 0.25 mm, the median is 0.15mm. In this design, the height of the bare dies is 0.15mm. The length of the pin is set to 1.9mm. The size of the top graphite die pins should be 50 to 250 microns smaller than that of the bare die pins. For example, a 5mm * 5mm * 0.6 mm semiconductor die in a 2mm deep fixture will have a counter pin of 4.85mm * 4.85mm * 1.5mm–1.6mm. The specific parameters of fixture B are shown in Fig. 5.5.

Fig. 5.5. The specific parameters of model B.
Chapter 6. Conclusion

In this thesis, the design and simulation procedures for a power electronic module are studied. A 1.7kV SiC JFET cascode switch power module was designed, layout, simulated, and studied. The layout of the power module is limited by many design constraints. Several designs and layouts are simulated, studied, and compared using the ANSYS Electronics Workbench. The parasitic inductances are extracted using the ANSYS Q3D Extractor and the thermal simulations are performed using the SolidWorks. Finally, the fixture designs required for the soldering or sintering process in the course of the fabrication of the power module are presented.
References


