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Design, Fabrication, and Characterization of an Array of Graphene Based Variable Capacitors

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Design, Fabrication, and Characterization of an Array of Graphene Based Variable Capacitors

A dissertation submitted in partial fulfillment
of the requirements for the degree of
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by

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Abstract

Since it was first isolated and characterized in 2004, graphene has shown the potential for a technological revolution. This is due to its amazing physical properties such as high electrical conductivity, high thermal conductivity, and extreme flexibility. Freestanding graphene membranes naturally possesses an intrinsic rippled structure, and these ripples are in constant random motion even room temperatures. Occasionally, the ripples undergo spontaneous buckling (change of curvature from concave to convex and vice versa) and the potential energy associated with this is a double well potential. This movement of graphene is a potential source of vibrational energy.

In this dissertation, we want to exploit this movement of freestanding graphene to design and create an array of freestanding graphene-based variable capacitors on 100 mm silicon wafer substrates. Our intent is to develop a device that can be highly duplicated and potentially incorporated into an integrated circuit to power low power electronics.

This work is based on a two-mask photolithography process. The first photolithographic mask creates long trenches terminated by square wells which have a cone-shaped tip feature etched at its center. These trenches, wells, and tip features are created by isotropic wet etching of the underlying sacrificial SiO_2 layer with hydrofluoric acid for 5 minutes at room temperature. The second photolithographic mask lays out metal traces from the tip to its bonding pad along the trench, and a second bonding pad opposite the square well. Creation of these conductive pathways and contact pads is done by deposition of Cr and Au. Finally, I perform large area graphene transfer to the tip regions and use critical point dryer to dry the substrate. This ensures that graphene is left freestanding over the tip feature.

This graphene-tip feature junction forms a variable capacitor where graphene is the movable plate, and the etched tip feature is the fixed plate. Capacitance of up to 60aF is measured from these device structures. In a broad picture, this graphene-tip variable capacitor can be incorporated in a low power energy harvesting circuit as the power source component. It can be used to power low power electronics such as remote sensors. Harnessing this energy associated with graphene vibrations could be source of clean renewable energy and an alternative to batteries.

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CHAPTER 1

1   Introduction

Initial studies of two-dimensional (2D) graphite dates back to as early as 1947, when tight binding approximation was used by Wallace to investigate the electronic energy bands in crystalline graphite [1]. Since it had been proven that the semi-metallic phase was unstable in 2D [2, 3], free standing monolayer graphene had long been regarded as an 'academic' material. Nevertheless, many experimental efforts were made to obtain monolayer graphene [4, 5].

Graphene, a 2D allotrope of carbon was first isolated and characterized in 2004 in a series of papers by Novoselov et al. at the University of Manchester [6-8]. Novoselov and Geim presented a robust and reliable approach for producing monolayer graphene by repeatedly peeling highly oriented pyrolytic graphite (HOPG). This technique was called mechanical exfoliation method (also known as the scotch tape method). This caused great excitement and many scholars started to investigate the structure and properties of graphene. Much of the excitement around graphene was and is still related to its great technological promise especially in the field of flexible electronics due to its many amazing properties. These properties include ballistic transport [9, 10] , high charge carriers mobility [11-13], non-magnetism [14, 15], and high electrical and thermal conductivity [15-17].

In this chapter we will review some properties of graphene membranes and some techniques involved in synthesis of graphene membranes.

1.1 Graphene: Sp^2 hybridization, honeycomb lattice and Brillouin zone

Carbon is the 6th element in the periodic table and has an electronic configuration of $1S^2 2S^2 2P^2$. The nucleus in carbon atom is surrounded by 6 electrons, 4 of which are valence. These valence electrons in carbon form three types of hybridization namely sp, sp^2 and sp^3. Graphene is a 2D monolayer of sp^2 hybridized carbon atoms. Sp^2 hybridization occurs when bonding occurs between 2s orbital with 2p orbitals as illustrated in Fig 1.1. It is the combination of one s-orbital electron with two p-orbital electrons, p_x and p_y. These 3 electrons then result in formation of σ bonds which are responsible for strength of graphene. The fourth electron is left on the $2p_x$ orbital. This electron left in the p_z orbital is perpendicular to the sp^2 hybrid orbitals and form π bond which is associated with graphene's electronic properties [18-21].
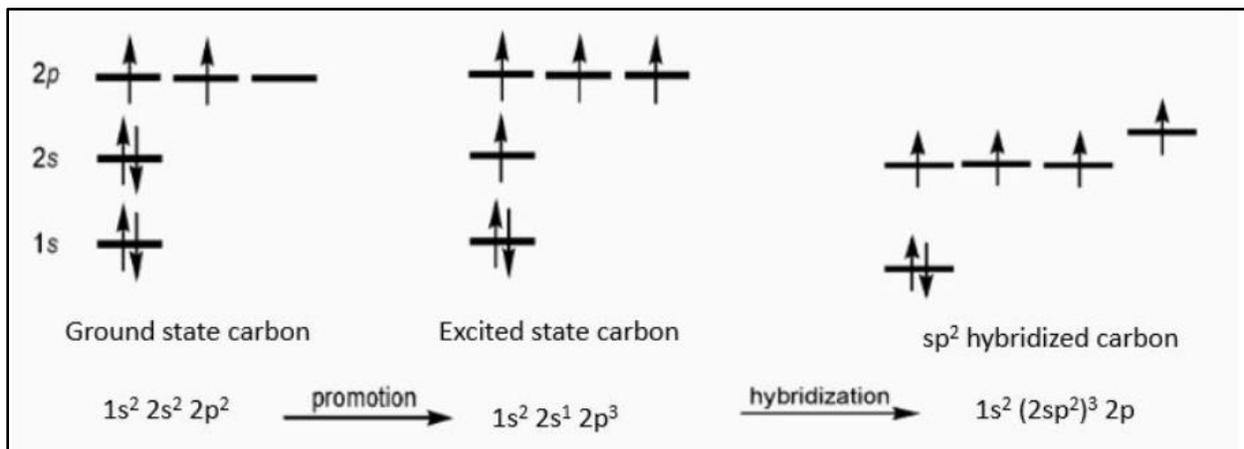
Figure 1.1: Illustration of carbon sp^2 hybridization. Image adapted from [21]

Graphene has a non-Bravais honeycomb crystal lattice structure. It consists of a single layer of carbon atoms arranged in a hexagonal lattice, built out of two interwoven triangular sub lattices as shown in Fig 1.2(a). The unit cell consists of two carbon atoms represented by A and B (blue and yellow circles) which form the honeycomb lattice structure. The lattice unit vectors are labeled

as a_1 and a_2 and space vectors that connect the two sub lattices (three nearest neighbor vectors) are labelled as δ_1, δ_2 and δ_3 [17, 22]. These space vectors are given by

$$\delta_1 = \left(\frac{a}{2}, \frac{a\sqrt{3}}{2}\right)$$

$$\delta_2 = \left(\frac{a}{2}, -\frac{a\sqrt{3}}{2}\right)$$

$$\delta_3 = -a(1,0)$$

Where $a = 1.4\text{Å}$ is the carbon-carbon distance.

The primitive lattice basis vectors that make up this lattice are

$$a_1 = \left(\frac{3}{2}a, \quad \frac{\sqrt{3}}{2}a\right)$$

$$a_2 = \left(\frac{3a}{2}, -\frac{\sqrt{3}}{2}a\right)$$

Using $a.\,a^* = 2\pi$, the reciprocal lattice therefore becomes

$$b_1 = \left(\frac{2\pi}{3a}, \frac{2\pi\sqrt{3}}{3a}\right)$$

$$b_2 = \left(\frac{2\pi}{3a}, -\frac{2\pi\sqrt{3}}{3a}\right)$$

The first Brillouin Zone (BZ) of the reciprocal lattice is a honeycomb lattice rotated at an angle of $\frac{\pi}{2}$ with respect to the real space lattice as shown in Fig 2.1(b). It represents a set of inequivalent points in the reciprocal space. These are points which may not be connected to one another by a reciprocal lattice vector. The six corners of the first BZ consist of two set of inequivalent points, K and K′, these are called the Dirac points.

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$$K = \left(\frac{2\pi}{3a}, \frac{2\pi}{3\sqrt{3}a} \right)$$

$$K' = \left(\frac{2\pi}{3a}, -\frac{2\pi}{3\sqrt{3}a} \right)$$
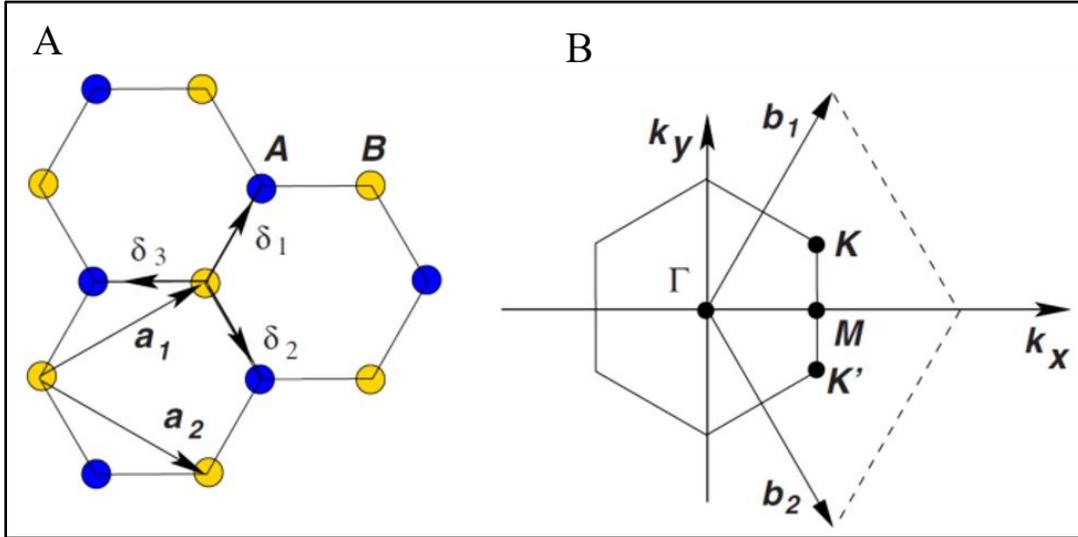
Figure 1.2: Schematic illustration of honeycomb lattice structure of graphene. (a) Hexagonal lattice structure. (b) Brillouin zone showing the high-symmetry points. Figure adapted from [22].

1.2 Electronic, Mechanical and Thermal Properties of graphene

Graphene is known as the most promising 2D material in the design of a wide array of Nano devices due to its amazing material properties. In particular, graphene membranes exhibit exceptional properties such as high electrical conductivity, high thermal conductivity, unusual flexibility, non-magnetic, remarkable biocompatibility and enormous specific surface area [17, 23-28]. Vast applications of its potential applications lie in the field of electronics and hence a lot of emphasize has been placed on analyzing graphene properties for its potential integration in electronic circuits. Here, we will review some of the prominent graphene properties and current advances in graphene-based electronics applications.

Due to the remarkable electronic and optical properties observed in graphene crystallites, extensive experimental and theoretical efforts have been placed on graphene while ignoring the existence of other 2D materials [29]. Graphene electronic structure can be predicted by density function theory (DFT) simulations. Graphene is a zero electronic bandgap semiconductor with charge carrier mobility of approximately 200,000cm^2/Vs at ambient conditions [6, 7, 30-32]. With this, nearly ballistic transport is observed in the sub-micron regime and at room temperature [33]. A challenge to this is that due to its zero bandgap, it is not possible to turn off the device graphene devices completely without high leakage current hampering its prospects for applications in Field Effect Transistors (FETs). Graphene is 70% – 90% transparent and its transparency or opacity of is dependent on the fine-structure constant $\alpha = \frac{e^2}{hc} \approx 7.299 * 10^{-3}$ [34-36] and also its thickness [37]. The electronic applications of graphene include photodetectors, light emitting diodes, solar cells, electronic sensors, biomolecular sensors, and gas molecule sensors [38-42].

Impressive mechanical properties of graphene make it stand out both as an individual material and as a reinforcing agent in composites. Graphene has very high elastic modulus and intrinsic strength which originates from the stability of the sp^2 bonds that form the hexagonal lattice and oppose a variety of in-plane deformations. Nanoindentation experiments on graphene sheets have been used to study its mechanical properties. For example, Hone and his coworkers first measured the mechanical properties of graphene using nanoindentation in an AFM where they described it as the strongest material ever measured [43-45].

Fracture toughness of graphene is one of its most important mechanical properties and is very relevant for its applications. Zhang et al [46] developed an insitu micromechanical testing device to measure the toughness of graphene. Thermoelectric properties of graphene are a function

of its electronic and structural properties. Extensive research has been done to improve these properties by various techniques such as chemical doping, isotopic substitution, isoelectronic impurities and hydrogen adsorption [47]. Specific heat capacity of graphene has not been directly measured but calculations have been done by referencing graphite data. Specific heat is a distinct characteristic of a material that expresses the change in the energy density with the change in temperature (1K or 1^0C). The specific heat capacity of graphite at room temperature is $C_{ph} \approx 0.7 \, J \, g^{-1} \, K^{-1}$, which is approximately 30% higher than that of diamond. This is due to the higher density of states (DOS) at low phonon frequencies caused by the weak coupling of graphite layers.

For a graphene sheet at room temperature, a similar result is expected, but the specific heat can be altered when graphene interfaces with a substrate. Studies on the effects of number of layers and edges of graphene on its properties have been done to understand their significance in applications as a layer in the multilayered configuration of the devices [48-50].Thermal conductivity of graphene is $K \sim 4000 W/mK$. A recent trend with shrinking sizes of electronic devices has led to a need for thermal management and hence the need for study of thermoelectric (TE) effects in graphene-based systems. Thermoelectric effects refer to the voltage induced by a temperature gradient. Experimental studies indicated that graphene has a thermal electric power (TEP) of $\sim 50 - 100 \, \mu V \, K^{-1}$ with a maximum of $80 \, \mu V \, K^{-1}$ at room temperature [51, 52]. Some of the thermal applications of graphene include electronic skins (E-skins) temperature sensors, thermoelectric sensors and thermal biosensors [53-59].

Table 1: Properties of graphene in comparison with other metals

Property	Value	Comparison	Citation
Thermal conductivity	$\sim 4000 W/mK$	10 times > Copper	[17, 60-64]
Elastic limit	20%	< 1% for steel	[44, 64, 65]
Carrier Mobility	$200,000\ cm^2V^{-1}S^{-1}$	100 times >Si	[33, 34, 63]
Elastic stiffness	$-690 \pm 50Nm^{-1}$		[44, 64, 66]
Breaking strength	$42N/m$	200times > steel	[43, 44]
Max Current density	$> 10^8\ A/cm$	100 times > Cu	[67]
Optical absorption coefficient	2.30%	50 > GaAs	[37]

1.3   Synthesis of Graphene

This refers to the different processes or techniques used in fabrication of graphene. Graphene has great promise as an alternative or a replacement for silicon in the photonics industry. However, a lot of effort is required in the development of its techniques. The main obstacle to this has been to commercially produce graphene with the key challenge being synthesis and bulk production of graphene sheets. In this attempt to commercially fabricate single layer graphene or Few Layer Graphene (FLG), various fabrication techniques have been developed for mass production of graphene for practical application.

Graphene synthesis techniques can be either top-down or bottom-up as shown in the process flowchart in Fig 1.3. In top-down processes, graphene sheets are produced by exfoliation or separation of graphite or graphite derivatives such as graphite oxide and graphite fluoride. Some

of the common top-down fabrication processes are direct sonication of graphene (segregation), electrochemical exfoliation, micromechanical exfoliation, manual exfoliation, and super acid dissolution of graphite (liquid phase exfoliation) [6, 68-74]. In bottom up processes, graphene is built from smaller carbon precursors[75]. Some common bottom-up fabrication techniques include chemical vapor deposition, epitaxial growth, arch discharge, unzipping of carbon nanotubes, and reduction of CO [63, 71, 75-81].

The synthesis technique used depends on the desired size, purity level and crystallinity. Due to this, each technique has different possibilities for its applications [63, 82]. Here, we will review a few of the commonly used techniques for graphene fabrication and discuss the merits and demerits of each technique.
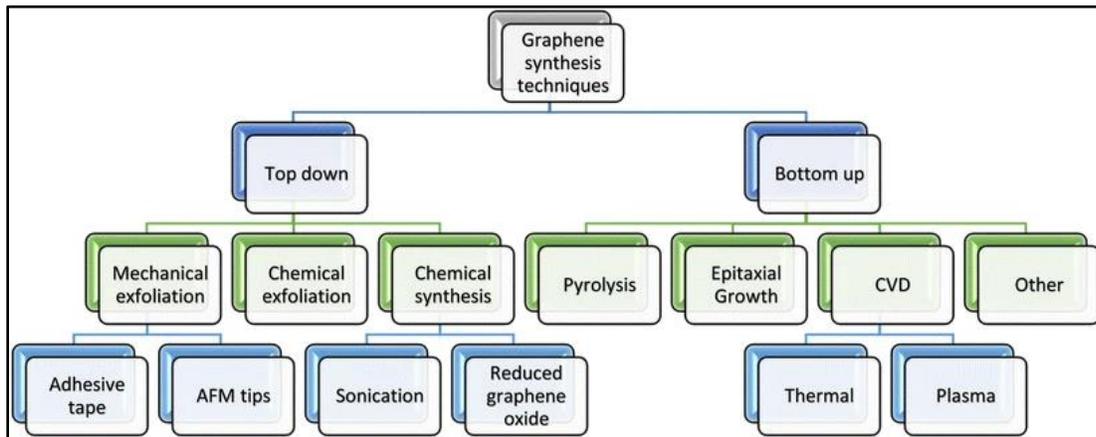
Figure 1.3: Process flow chart of graphene synthesis showing top down and bottom up techniques. Figure adapted from [63]

1.3.1 Manual exfoliation

This method was originally advertised as the scotch tape method [6, 7]. It is the simplest of all the techniques and is the method that made stand-alone graphene a reality and led to Geim and Novoselov being awarded the Nobel Prize in 2010 [83]. In the manual exfoliation technique, a piece of tape is repeatedly applied to the top layer of highly oriented pyrolytic graphite (HOPG) and then peeled off. The tape is peeled off such that it will have multiple layers of graphene as shown in Fig 1.4. By repeating this process, it is possible to generate single layer graphene. The number of layers peeled can be evaluated using a simple optical microscope, Raman spectroscopy, atomic force microscopy (AFM) or scanning tunneling microscopy (STM). Manual exfoliation gives rise to the highest quality graphene crystals[44].

Major disadvantage of this method is that the size of the crystals produced is typically in the order of a few microns and it is a very labor-intensive method. Graphene crystals produced by manual exfoliation are among the most expensive materials in the world.

Figure 1.4: Graphene scotch tape exfoliation method from a HOPG crystal. Figure adapted from [83].

1.3.2 Molecular Beam Epitaxial growth

This technique was developed by a research group in Georgia Tech led by Claire Berger and Walt de Heer [84, 85]. This is growth of graphene exposing an epitaxially grown hexagonal Silicon carbide (SiC) crystal ($4H_-$) or ($6H_-$) to temperatures of about 1300^0 C in order to evaporate the less tightly bound Si atoms from the surface (thermal decomposition). When SiC crystal is heated and the loose Si atoms leave the surface, the remaining carbon atoms rearrange themselves in order to form a graphene layer (graphitic layer). This is called graphitsation.

Graphene crystals produced are much larger than those produced by manual exfoliation and so it is a more technologically promising route for large scale productions. However, the challenge with this technique is that SiC substrate must be considered as an integral part of the whole system of epitaxial graphene. It is the parent compound and the physical properties of the first graphitic layer formed depend on the chosen SiC surface [36, 86-89].

1.3.3 Segregation

This method is used for the graphene synthesis on metals which have high carbon solubility such as Ni and Ru or metals which when heated to very high temperature, their carbon solubility becomes significant such as Pt [86, 90-94]. Segregation technique involves 'squeezing' carbon atoms directly out of the bulk metal. The metal bulk containing carbon atoms is loaded at high temperatures and then when cooling, carbon atoms travel to the surface and form ordered layer of graphene.

This technique involves a series of steps namely: diffusion of carbon atoms in in the bulk metal, segregation of the carbon atoms from the bulk to the surface, surface diffusion, nucleation

and growth of graphene on the metal surface. With this method, multilayer graphene can be easily grown since the thicknesses of deposited layers depend on cooling rate and the loading and segregation temperatures [95-97]. These temperatures also determine the quality of graphene formed.

1.3.4   Liquid phase exfoliation (LPE)

LPE of graphite was first initiated in 2008 via sonication and extensive progress has been made since then [73]. LPE includes two exfoliation stages: Cavitation in a sonicator and shear forces in a high-shear mixer [71, 98]. There are two types of sonication: Bath sonication and tip sonication. With this technique, sonication is used to induce physical or chemical changes into the system through generation of cavitation bubbles. Sonication assisted LPE involves the following steps: preparation of dispersion graphite in a specific solvent, exfoliation of dispersion via sonication and lastly purification of graphene. Growth and collapse of microbubbles is attributed to pressure pulsations. Cavitation results in high-speed shock waves which produce normal and shear forces on graphite. The exfoliation depends on the power of sonication, the liquid medium used to disperse graphene nanosheets, and the rate of centrifugation [38]. The suitable solvents include organic solvents such as N-methyl-2-pyrrolid(NMP) [99], ionic liquids such as trifluoro-methane-sulfonyl [68], water surfactant such as sodium dodecyl benzene sulfonate [100], water polymers such as polyvinylpyrrolidone (PVP) [70] and pure water[72].

In sonication, FLG can be produced at high concentrations. The challenge of this technique is that with this technique, production of single layer and large size graphene sheets is not possible. Also, the yield is too small and so this technique can't meet the macroscopical requirements for industrial applications [73].

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1.3.5   Chemical vapor deposition (CVD)

This is a chemical process used to deposit fully dense thin solid films resulting from decomposition of a gaseous precursor on various substrates such as metals and ceramics. CVD is classified into: plasma-enhanced CVD (PECVD), atmospheric pressure CVD (APCVD), low-pressure CVD (LPCVD), microwave plasma-assisted CVD (MPCVD), hot filament CVD (HFCVD), and ultra-high vacuum CVD (UHVCVD).

Complexity of the CVD process and the high energy demands add to the difficulties, but CVD still remains one of the most successful methods for large-area graphene production. It has been given much emphasis in the research on growth of high-quality large quantity graphene sheets [44, 78-80, 101]. CVD growth on metal substrates has attracted tremendous attention due to its high growth-quality, scalability, high structural tunability, and therefore this technique holds great promise in a wide range of applications.

1.4   Transfer of CVD graphene to substrates

Intact and clean transfer of graphene is desirable in improving the efficiency and functionality of devices. Despite improved efficiency in fabrication of high-quality graphene, graphene transfer to desired substrates is subject to experiencing contaminations and structural damages (wrinkles and tears) [102, 103]. Significant progress and efforts have been placed in the development of transfer techniques to ensure that the structural integrity of graphene is maintained when it's transferred to desired substrates.

The transfer processes are divided into etching transfer and etching free transfer. Etching transfer can either be wet etching or dry etching. Chemical etching offers a relatively mild way to separate graphene from metals, but it suffers from several drawbacks such as significant metal

consumption, etching contamination, incompatible with noble metal substrates, and severe environmental pollution for large-scale production. Etch free methods are preferred since they are both clean and environmentally friendly. Some etch free transfer method include bubbling transfer and mechanical transfer.

It is very challenging to achieve intact and clean transfer in large-area graphene transfers. It is common to use a versatile supporting material during the transfer process to enable intact transfer. The commonly used transfer process of graphene to substrates is done by spin coating Polymethyl methacrylate (PMMA) on the graphene/metal surface and later chemically etching away the metal. The PMMA/graphene membrane is then scooped onto the target substrate and then PMMA is etched off or dissolved off [77, 104-106].

1.5   Suspended graphene NEMS devices

Over the last decade, several suspended graphene NEMS have been fabricated. They have also been used to study and probe the properties of suspended graphene.

I.   Resonators

This is by far the most extensively studied suspended graphene device. First fabricated in 2007 by Bunch et al [102, 107-109] using a single layer of graphene.

II.   Graphene NEM switches

NEM switches are some devices with a promising future in helping to solve the problems of high-power consumption in complementary metal-oxide semiconductor (CMOS) circuits[110]. Milaninia et al [111] demonstrated a few layers of CVD graphene switch which had a suspension aspect ratio of 40 and a 5V operating voltage. Graphene NEM switches help to fulfill the high

demand in low power device applications. Fig 1.5 below shows a schematic illustration of a graphene switch.
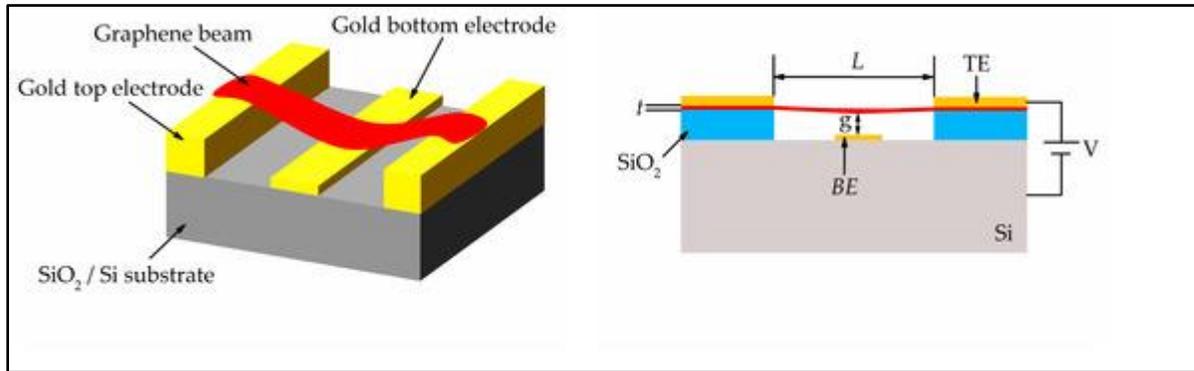
Figure 1.5: Schematic illustrations of NEM switch and the side view. Figure adapted from [110].

III. **Pressure sensors**

Graphene's piezoresistive property (independence to changes in crystallographic orientation for small uniaxial strain) has been leveraged for pressure sensors, strain gauges and accelerometer applications. Graphene's devices have a higher sensitivity due to the big difference in the area and thickness of suspended graphene in comparison to other materials like silicon and due to its ultimate thinness [45, 112-114]. Fig 1.6 below shows a static capacitive pressure sensor that was used to detect capacitance changes of a graphene drum down to 50aF[114]. Few-layer graphene membrane as a squeeze-film pressure sensor was developed which was based on the pressure dependence of the membrane's resonance frequency caused by compression of the surrounding gas. As the pressure outside the cavity varies, it causes a deflection and straining of the graphene membrane, thereby changing its electronic properties.
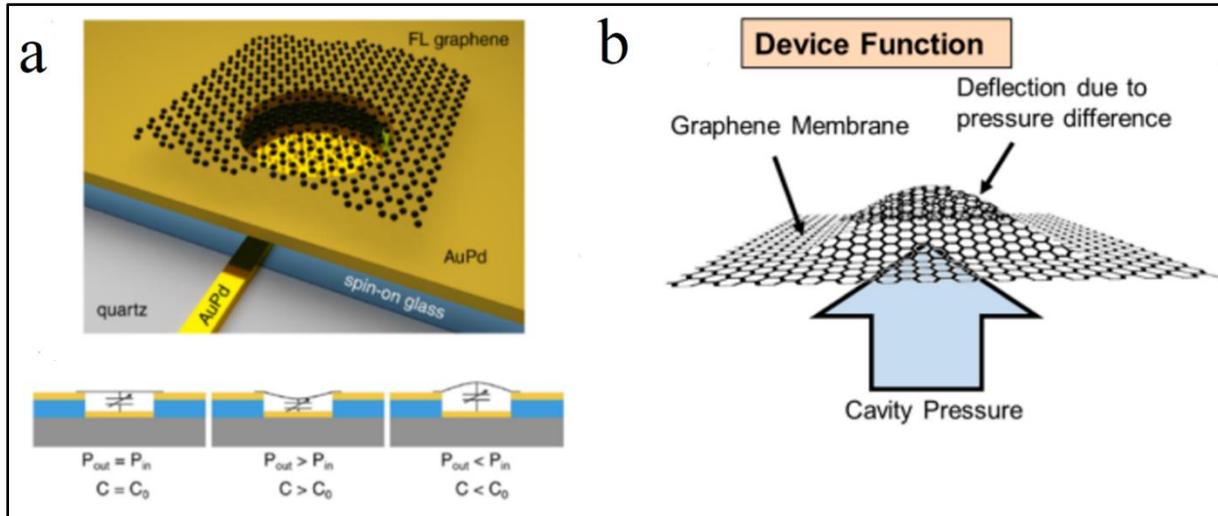
Figure 1.6: Graphene pressure sensors. (a) 3D schematic of graphene capacitive pressure sensor and an illustration of graphene at stationary, with attractive capacitive forces and with repulsive capacitive forces applied to the fixed electrode. (b) Representation of membrane functionality in a graphene pressure sensor. Figure adapted from [114].

IV.   **Suspended graphene varactors (SGVs)**

Studies on electrostatic actuation of suspended graphene suggests that a suspended graphene varactor (SGV) is very promising [115]. Ideal SGV was achieved by patterning the underlying electrode to eliminate parasitic capacitance, using large area graphene and a small ratio of trench length to trench separation to ensure highest variable capacitance per unit area. Large arrays of suspensions are needed to achieve 50pF capacitance as shown in Fig 1.7 below.
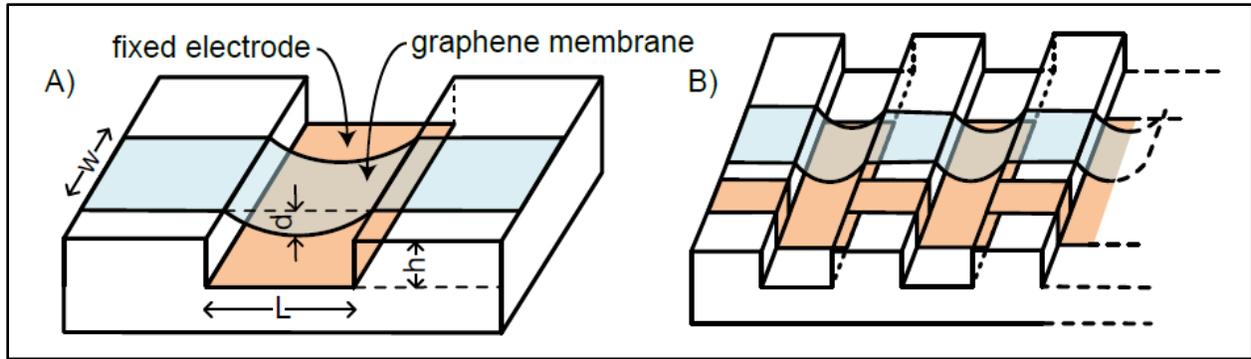
Figure 1.7: Graphene varactor. (a) Schematic illustration of suspended varactor. (b) An array of varactors used to increase the total capacitance. Figure adapted from [115]

1.6 Graphene flexural mode (ZA mode): Plate flexural deformation

Graphene flexural mode is also known as bending mode, or out-of-plane transverse acoustic mode. Studies around flexural modes in novel materials have intensified significantly in recent years due to the discovery of graphene. Flexural modes control the behaviors and properties of graphene NEMS and Nano resonators, which have been proposed for various sensing applications. Also, monolayer graphene is so highly flexible that its flexural mode is important for its thermal and mechanical properties. It is therefore important to understand graphene's ZA mode in order to understand the limits it imposes and its impact on graphene's physical properties [24, 116].

Graphene ZA branch is derived from the flexural mode of plate bending or a plate out of plane movement [117-119]. Imagine a thin plate subjected to a time varying initial displacement w in the z direction as shown in Fig 1.8 below.

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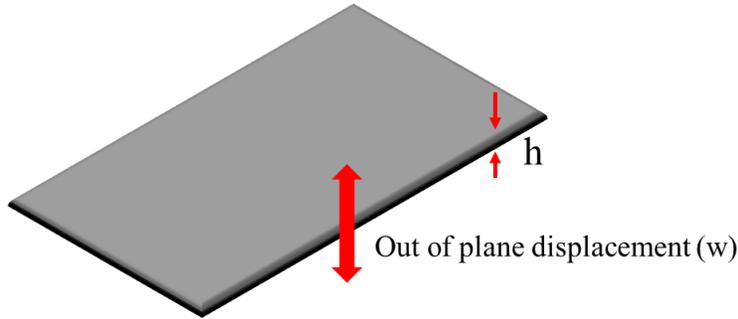
Figure 1.8: Schematic illustration of a beam with an out of plane displacement in the z direction

The equation governing the vertical displacement is given by the Hamilton's principle and is a variation of conservation principle that balances potential and kinetic energies within a deformed body with an applied load F. For plate flexural deformation without any applied force the equation is given by [120, 121]

$$\rho h \frac{d^2 w(x,t)}{dt^2} + D \frac{d^4 w(x,t)}{dx^4} = 0$$

Where

$D \equiv \frac{E_Y h^3}{12(1-v^2)}$ is the plate bending stiffness

$\rho =$ Plate density

$h =$ plate thickness

$E_Y =$ Young's modulus (a measure of the stiffness)

$v =$ Poisson ratio

Since we assumed a time varying displacement, the solution to this equation can assume a periodic solution

$$w(x,t) = \hat{w}e^{i\omega t}$$

Where $\hat{w} = Ae^{ik_j x}$ and it is the displacement amplitude and k_j are the allowable flexural wave numbers.

$$w(x,t) = Ae^{ikx}e^{i\omega t}$$

The displacement equation now becomes

$$\frac{d^2 w(x,t)}{dt^2} + \frac{D}{\rho h}\frac{d^4 w(x,t)}{dx^4} = 0 = (iw)^2 Ae^{ikx}e^{i\omega t} + (ik)^4 Ae^{ikx}e^{i\omega t} = 0$$

$$-w^2 Ae^{ikx}e^{i\omega t} + \frac{D}{\rho h}k^4 Ae^{ikx}e^{i\omega t} = 0$$

$$k^4 = \frac{\rho h}{D}w^2$$

K will have two imaginary roots and two real roots.

$$K_1 = \pm\sqrt{w}\left(\frac{\rho h}{D}\right)^{1/4}$$

$$K_2 = \pm i\sqrt{w}\left(\frac{\rho h}{D}\right)^{1/4}$$

Therefore, from the dispersion relation using only the positive values, the frequency becomes

$$\omega = \sqrt{\frac{D}{\rho h}}\,k^2$$

From this, it's clear that the flexural plate bending produces a quadratic dispersion and the plate's stiffness acts as the spring constant. Graphene's elastic stiffness depends on the crystal orientation

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and is approximately $D \approx 1eV = 1.6 * 10^{-19} Nm$. Graphene's area mass density $\rho h = 7.6 *$

$10^{-7} kg/m^2$

Using these values, the dispersion relation of graphene becomes

$$\omega = \left(5 \times 10^{-7} \frac{m^2}{s}\right) K^2$$

Using $K = \frac{2\pi}{\lambda} = \frac{n\pi}{L}$, $L = 7.5\,\mu m$ where n is the number of modes, the ZA branch

approximation is shown in Fig 1.8
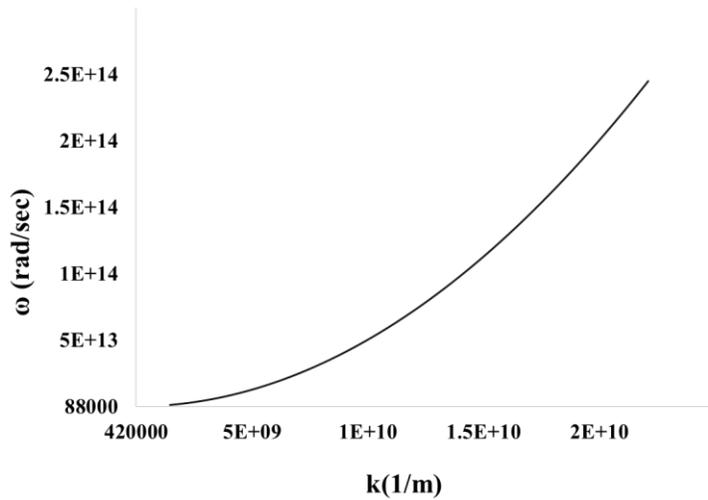
Figure 1.9: Approximation of graphene ZA branch using continuum flexural plate bending

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2   Graphene Rippling Mechanism

Differentiating them from their 1D and 0D counterparts, 2D nanomaterials exhibit surface wrinkles, ripples and crumples as shown in Fig 2.1 below. Stability in 2D materials is achieved by ripple formation resulting from the partially decoupled bending and stretching modes. The presence of these ripples plays an important influence on the mechanical behavior of 2D material [122, 123].

When graphene was first suspended in early 2000's [23, 124, 125], it was found to naturally form ripples due to its self-compression stability property and mechanical properties (Young's modulus, interfacial energy and number of layers) [25, 126-129]. These out-of-plane deformations have been studied and characterized in transmission electron microscopy (TEM) and scanning tunneling microscopy (STM) experiments [23, 130, 131]
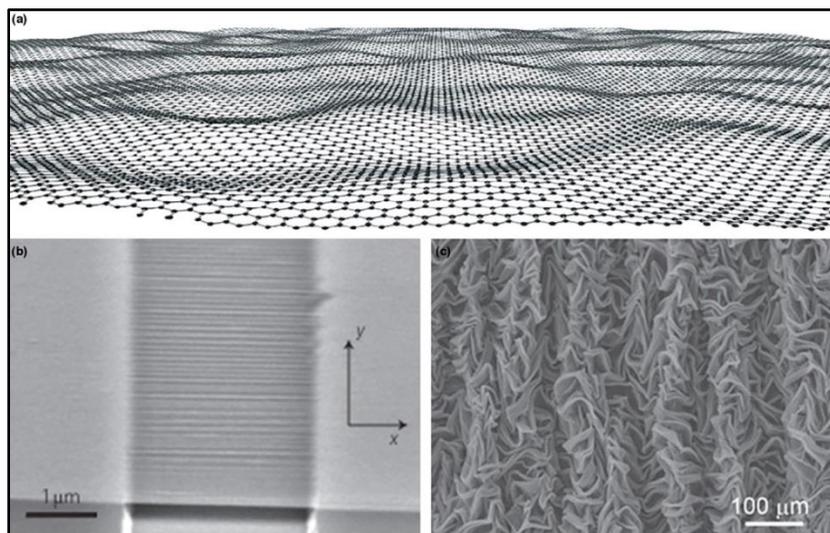
Figure 2.1: Wrinkled, Rippled and crumpled graphene. (a) Rippled graphene; (b) wrinkled graphene and (c) crumpled graphene. Figure adapted from [25].

In this chapter, we will explore and study the rippling dynamics of freestanding graphene and its potential application in vibrational energy harvesting.

2.1 Strain and length of a ripple.

Understanding the rippling effect on the mechanical behavior of 2D materials is useful for strain-based ripple manipulation for their applications [132-134]. By symmetry the ripple can be either concave or convex (curved up or curved down). A schematic illustration of ripple formation is shown in Fig 2.2. Starting with a flat sheet of graphene, small regions at the beginning and at the end of each ripple are kept flat and fixed to mimic typical nanoindentation experiments and prevent the structure from relaxing into its ground state. With this, edge effects can also be ignored.
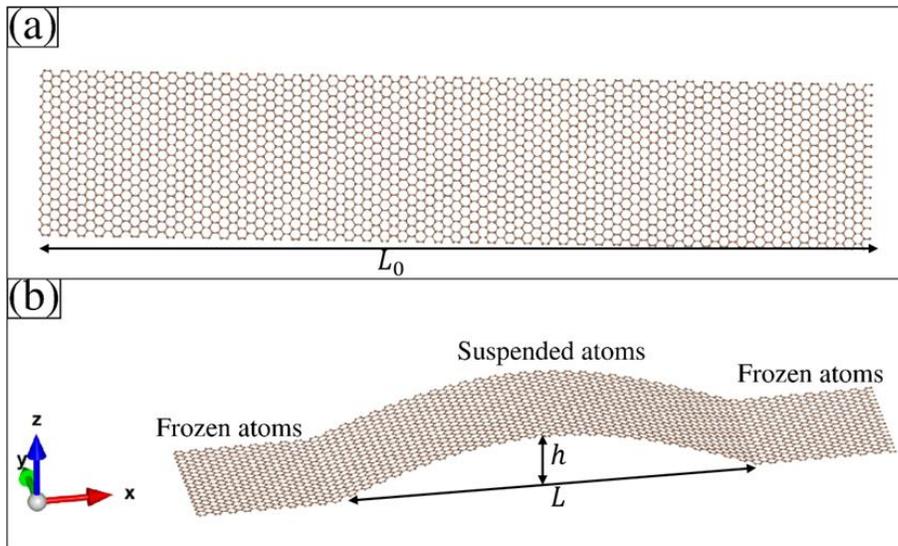
Figure 2.2: Illustration of graphene ripples formation. (a) Flat sheet of graphene. (b) Rippled sheet of graphene.

For a sheet with an original length L_0 and a curved length L as shown in Fig 2.2, the compressive strain is defined as $\varepsilon = \frac{L_0 - L}{L_0}$

To create the third dimension (z), we define

$$z = h \cos\left(\frac{\pi x}{2L}\right)$$

$$\frac{\partial z}{\partial x} = -\frac{\pi h}{2L} \sin\left(\frac{\pi x}{2L}\right)$$

$$L_0 = \int_{-L/2}^{L/2} 1 + \left(\frac{\partial z}{\partial x}\right)^2 dx = \int_{-L/2}^{L/2} 1 + \left(\frac{\pi h}{2L} \sin\left(\frac{\pi x}{2L}\right)\right)^2 dx$$

As the strain on the ripple increases, the height of the ripple also increases.

2.2   Shape transformations during ripple curvature inversion: LAMPPS simulations.

Shape transformations that occur during curvature inversion cannot be studied using Scanning Probe Microscopy (SPM). We use simulations in Large-scale Atomic/Molecular Massively Parallel Simulator (LAMPPS) to detail the evolution of ripple inversion and shape transformations involved in the process and this work has been published in Membrane's journal [135].

First, we first study the energy required to stretch and compress graphene ripple. Fig 2.3 shows part of a circular graphene lattice that consisted of close to 7000 carbon atoms. Potential energy for the lattice is found at different bond lengths using the AIREBO C-C potential at zero Kelvin. The minimum energy of the lattice was found to be at a bond length of 0.14nm. Starting with this bond length, a series of lattices with systematically larger and smaller bonds were created

and the potential energy associated with each lattice found as shown in Fig 2.3b which is a plot of energy per bond versus % strain. The energy increases more rapidly when compressed $(-\% \, \varepsilon)$ than when stretched with energy remaining systematic at low strains. Fig 2.3c shows the change in total energy for low strains $(-1\%$ to $1\%)$ which is the commom compression range for carbon sigma bonds [136, 137]. The dotted line shows the energy associated with either compression or stretching of 0.7%. This compression was found to be the zero-Kelvin barrier height for a ripple compressed by 0.7%.
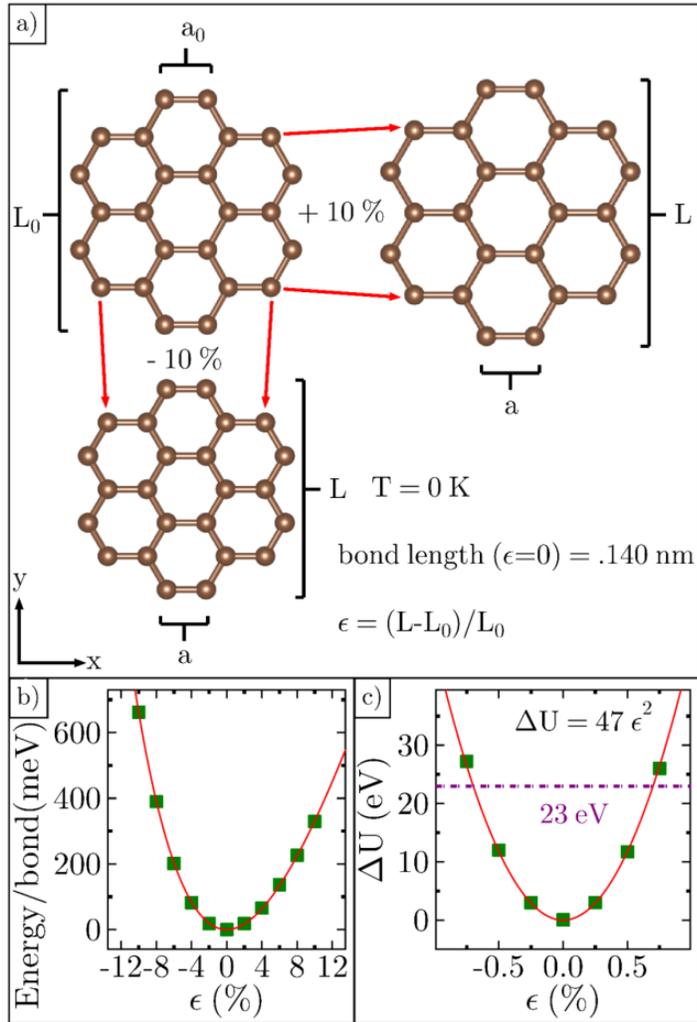
Figure 2.3: Energy required for curvature inversion. (a) A flat circular sheet of graphene with bonds compressed and stretched by 10%. (b) Graphene potential energy per bond versus % strain. (c) Change in total potential energy versus strain.

2.2.1 Zero-Kelvin barrier height for a flat sheet of graphene

Circular ripples with 15 nm diameter and a bond length of less than 0.14nm were constructed. To the middle section of a radius of about 7.5 nm, a third dimension (h) is added as illustrated in Fig 2.4a. This is done by adding a z component defined by

$$z = h\cos\left(\frac{\pi}{2(7.5)}\sqrt{x^2 + y^2}\right)$$

Where h is the central height of the ripple and x, y are the original coordinates of the carbon atoms.

As the height (h) of the ripple increases, length L_0 also increases and as a result, the bond length increases. A 1.5 nm wide graphene annulus around the ripple is left at zero height and is fixed in place to eliminate any edge effects. Fig 2.4b shows the two minima positions which correspond to the concave and convex configurations of the ripple. The value 23eV is referred to as the barrier height and it is the energy required for the ripple to invert its curvature at 0K and 0.7% compressive strain. The energy associated with the ripple curvature inversion is a double well potential and is given by

$$U(z) = \Delta U\left(\frac{z^4}{z_0^4} - 2\frac{z^2}{z_0^2}\right)$$

Where $\Delta U$the barrier height, z is the central height of the cosine shaped ripple, and z_0 is the central height of the ripple at its minimum energy positions. The formula relating the original planar % strain to the relaxed final height in nm is given by

$$\varepsilon = -1.08h^2$$
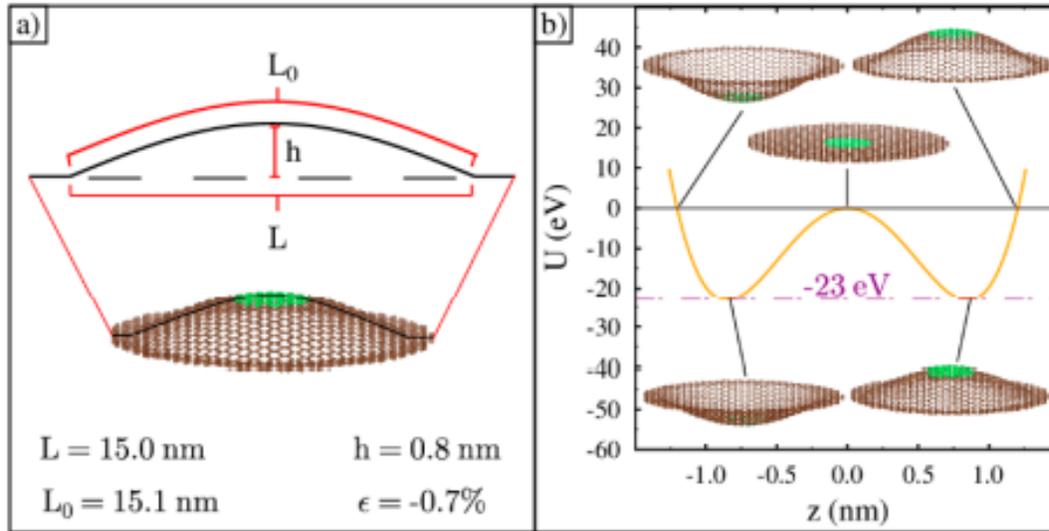
Figure 2.4: Illustrations of the mechanisms of curvature inversion. (a) Compressed circular graphene ripple with added third dimension (b) Ripple curvature inversion modeled as double-well potential for a circular of graphene. Figure adapted from [135]

2.2.2   Role of strain in ripple curvature inversion.

At room temperature, energy $(k_B T = \sim 0.025 eV)$ is about 1000 times less than the Zero Kelvin energy of the ripple with a 0.7% strain shown in Fig 2.4b above. This implies that the ripple has an extremely low probability to invert its curvature at room temperatures. However, we do know that this is not the case as experimental studies prove graphene has moving ripples at room temperature. This suggests graphene does not go through uniform flattening to invert its curvature. To study the ripple dynamics and effects of strain, we increased the temperature of simulated graphene ripples to 3000K. Fig 2.5 shows the simulation results for various levels of strain and depict the three working regimes. At high compression $(\varepsilon \sim 0.78\%)$, the ripple is trapped in one of the minima as shown in Fig 2.5(a-b). For under compression $(\varepsilon \sim 0.13\%)$, the system oscillates around $x = 0$ as shown in Fig 2.5c.

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A bistable behavior is observed with long swings from one well to another at optimal compression ($\varepsilon \sim 0.67\%$) as shown in fig 2.5d. These swings are the curvature inversions. Inversion occurs when the ripple transitions from one side of the potential well to the other. This observation implies that the dynamics of the graphene system can be controlled by changing the compression levels. Optimal compressions are desirable in the making of bistable devices.
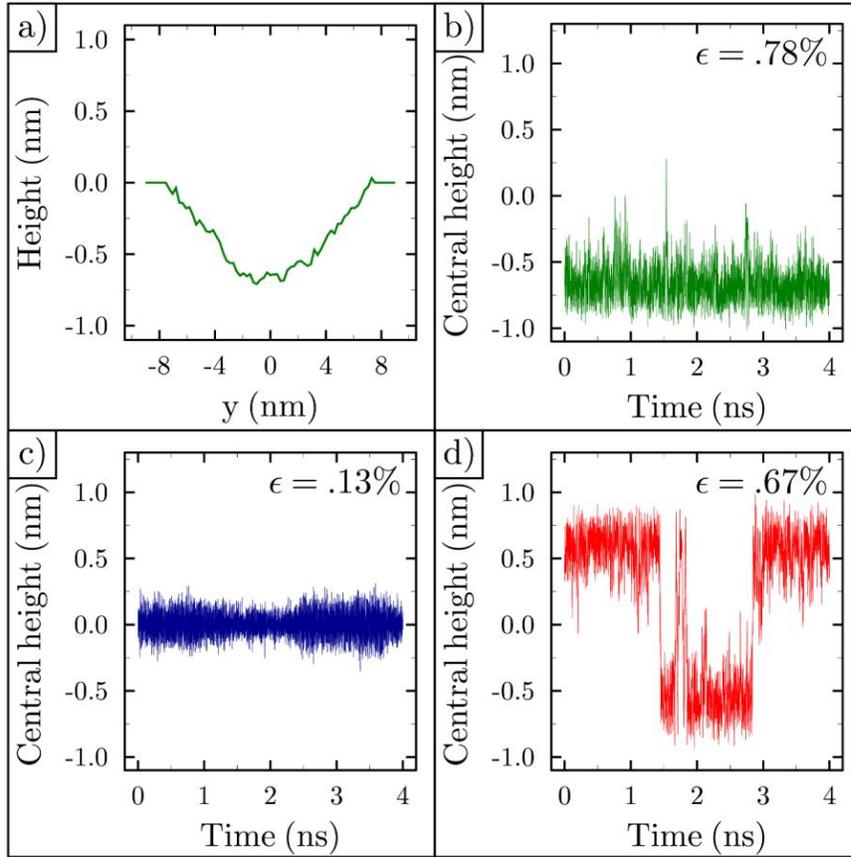
Figure 2.5: Role of strain in ripple dynamics. (a) A typical cosine shaped cross-sectional profile of a ripple. (b) High compressions. (c) Under compressions. (d) Optimal compressions. Figure adapted from [135]

2.2.3   Average time between curvature inversion

After identifying strain range associated with bistable behavior, simulations were done on about 10 ripples to study the average time between curvature inversions. Fig 2.6a shows the average time between the inversions vs the applied lattice strain. The larger the strain the longer the ripple stays on one side. The average time $\langle t \rangle$ to cross a barrier height ΔU is given by Kramer's rate[138]

$$\langle t \rangle \propto e^{\frac{\Delta U}{k_B T}}$$

Where k_B is Boltzmann's constant and T is the absolute temperature. Fig 2.6b shows the quadratic relationship between the change in energy ΔU and strain with an extrapolation for the stretched ripple+% ε. Energy required for inversion to occur $U = 3.4\varepsilon^2$eV. The blue dotted line shows the barrier energy of a ripple with 0.7% strain. This energy is similar to density function theory (DFT) calculated value [139].
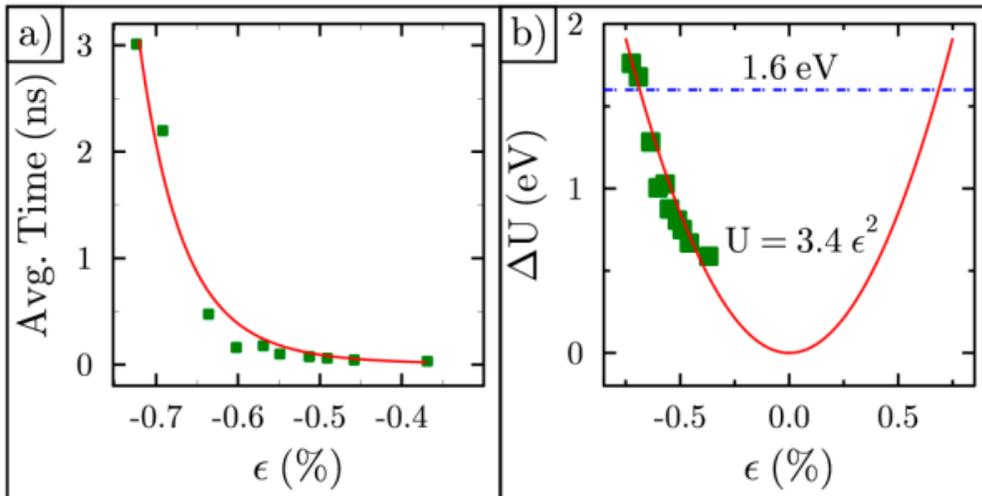
Figure 2.6: Average time and energy barrier. (a) Average time between curvature inversion vs strain. (b) Barrier height vs strain. Figure adapted from [135]

A comparison of this barrier height with the energy barrier height for a flat ripple (23eV) shows that uniform flattening is not the mechanism behind curvature inversion. There is a probability for a ripple to alter its shape as illustrated in Fig 2.7 where the ripple shifts its maximum to the right as the other half of the ripple starts the inversion.
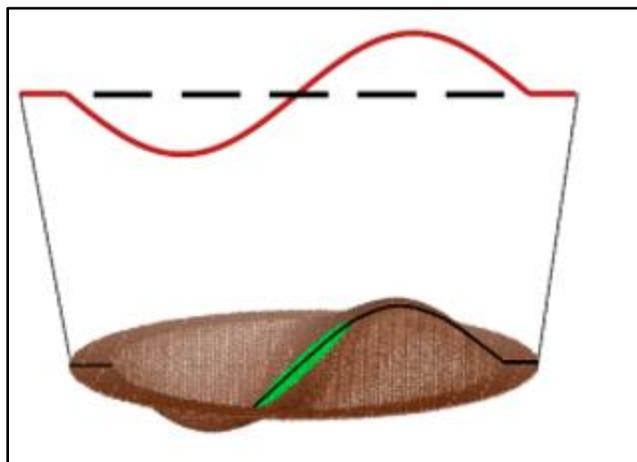
Figure 2.7: Illustration of a possible ripple shape change during curvature inversion. Figure adapted from [135]

2.2.4 Physical transformation during ripple inversion

Since uniform flattening is not the mechanism behind curvature inversion, there was need to investigate the physical transformation involved in ripple curvature inversion. To study the ripple's physical transformations, we first identify all the inversion events in a ripple simulation by plotting the central height over time, as shown in Fig 2.8a. Root-mean-square deviation (RMSD) analysis confirms the atom positions have stabilized within the first 0.2 ns. The initial time data before the stabilization are not included in the plot. After stabilizing, the ripple's height is positive in the beginning, and then flips 6 times during the next 8 ns.

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In order to track the larger structure of the ripple, we recorded the height of the ripple along both the x-axis and y-axis every picosecond. From these data sets, we determined the (x, y) coordinate for the maximum height of the ripple along these axes in time. The ripple maximum begins near the center of the ripple (0, 0), then shifts to the edge of the ripple just before inversion. This process of starting near the center and moving toward the edge was repeated for all the ripple curvature inversions, as shown in Fig 2.8 (b–g). Given that a large displacement of the maximum away from center and toward the edge occurs just prior to inversion for every event, we believe that this displacement triggers ripple curvature inversion.
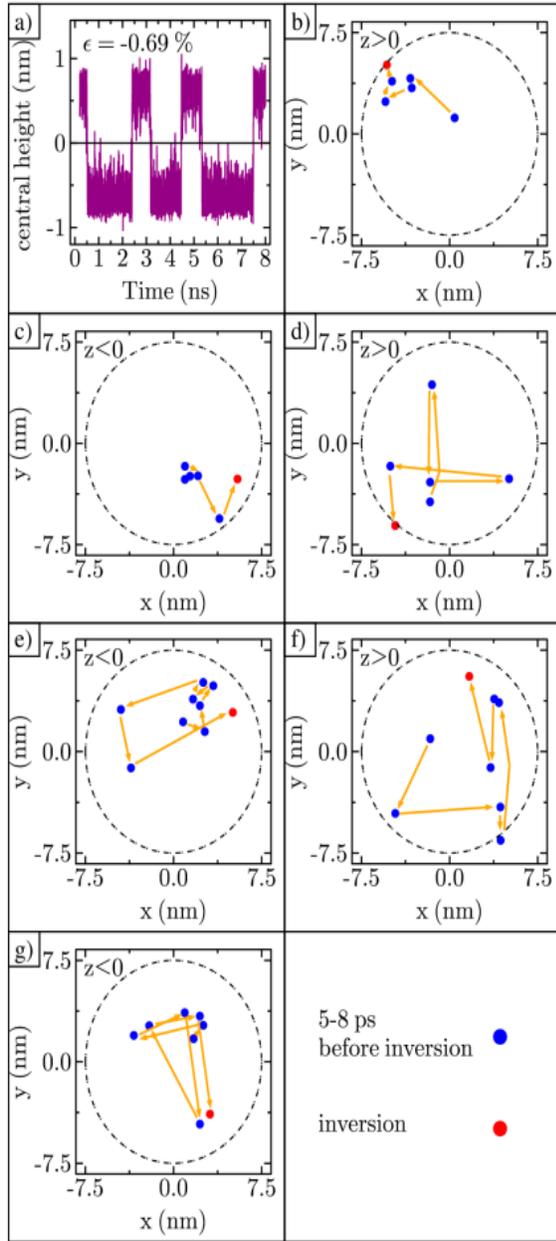
Figure 2.8: Curvature inversion illustration: (a) Central height of ripple in time with six complete inversions; (b–g) Displacement of the maximum along the x and y axes every picosecond, just before curvature inversion. Lower right box shows the legend. Figure adapted from [135]

The primary path of ripple inversion is illustrated in fig 2.9 below starting with a cosine-shaped convex ripple. Due to random collective motion, the maximum of the ripple (marked with

a red circle) begins to move away from the center and toward the fixed edge, as illustrated in fig 2.10b. As the maxima moves to the right, the carbon atoms on the left side are pulled inward and downward toward the x–y plane ($z = 0$) and eventually cross the plane of the fixed outer edge. Now, the cross-sectional shape of the ripple is best described as a sine function. The ripple minimum is marked with a green circle as shown in Fig 2.9c. The ripple maxima then suddenly flip from above the central fixed plane to below, and the ripple is concave, as shown in Fig 2.10d. This is the dominant pathway for ripple inversion.
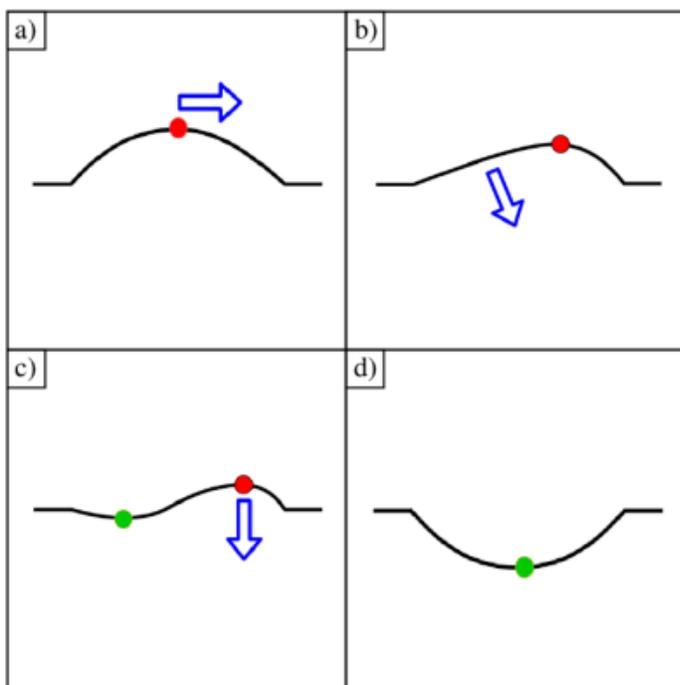
Figure 2.9: Illustration of ripple physical shape transformation. (a) The maximum of the ripple moves from center point to the right. (b) Ripple curvature is lower on the left side. (c) The left side passes through the x–y plane and the ripple form a sine-like shape. (d) The left sub-ripple has pulled the right sub-ripple down and a single ripple is formed below the x-y plane. Figure adapted from [135].

2.3 Quantification of graphene vibrations

Graphene vibrations are quantified using current collected when an electrically charged sheet of freestanding graphene is placed near a stationary metal electrode. The graphene - electrode junction form a variable-gap capacitor, where graphene is the movable part. When connected to an electrical circuit with diodes as shown in Fig 2.10, the Brownian thermal motion of graphene induces an alternating current in the electrode. The thermal motion of graphene induces an alternating current in the circuit at room temperature. Diodes produce a pulsing direct current that performs work on a load resistor [140].
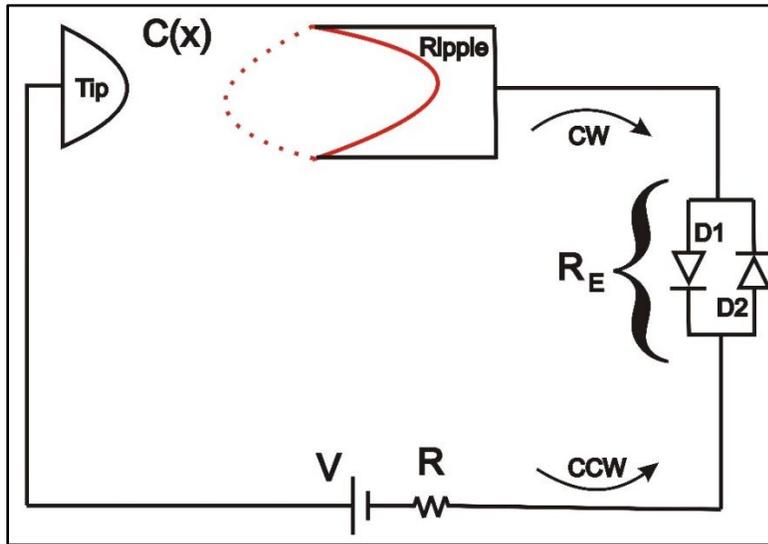
Figure 2.10: Sketch of circuit model with energy barrier diagram. Figure adapted from [140]

Graphene fluctuation displacement current has been determined using AFM at zero tunneling current as shown in Fig 2.11. To measure the displacement current at zero tunneling current, STM tip was incrementally backed away from the sample using the coarse motion stage until the distance was too great for electrons to tunnel through the vacuum barrier. Current I-V characteristics of D2 were measured and are shown in Fig 2.11(b-c) with resistance labels.

Combining the voltage data with the displacement current data the power dissipated in D2 was calculated and is shown in Fig 2.11d. The maximum instantaneous power reached is 40 pW. The average power for a large number of data sets acquired across this sample and other identically prepared samples of flexible freestanding graphene is shown in Fig 2.11e. The average power significantly rises for bias voltages above 10 V. When this same measurement is repeated for rigid graphene, we do not observe current D2C . This result is shown near the bottom of Fig 2.11e. Current on D2 flows opposite the bias voltage and only a displacement current can flow in this direction. Any current due to field emission effects, for example, will flow through D1.
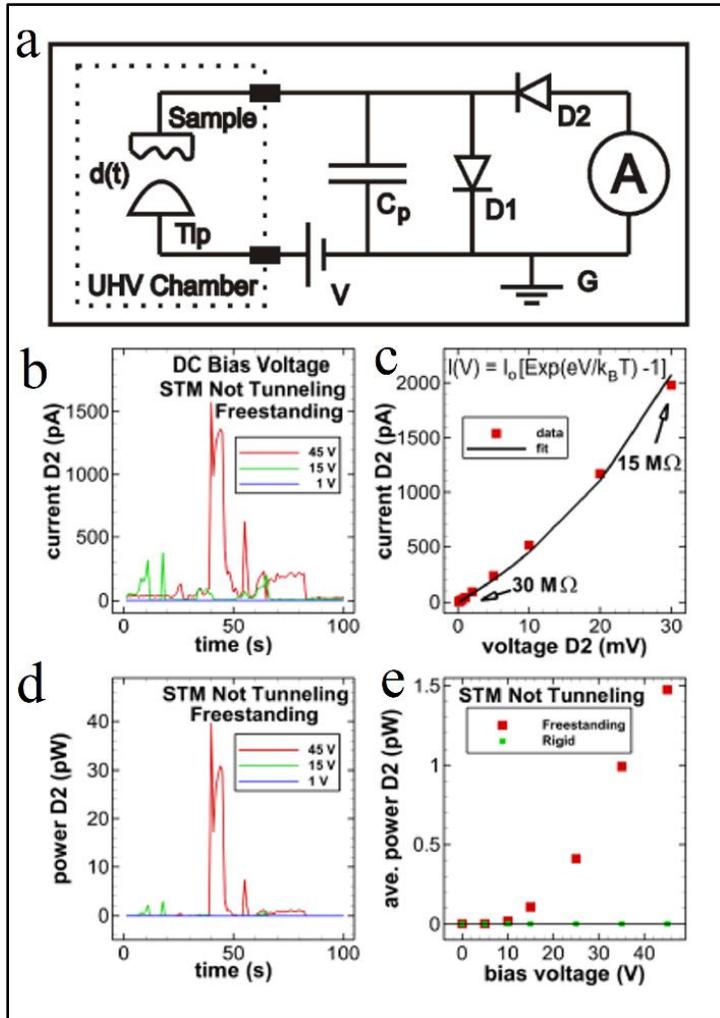
Figure 2.11: Quantification of graphene vibrations using STM. (a) Circuit diagram (b) STM current vs time for freestanding graphene when STM is not tunneling electrons. (c) Average current vs voltage through diode 2. (d) Power through diode 2 versus time for different voltages. (e) Average power through diode 2 vs voltage bias Voltage. Figure adapted from [140].

MDS was also utilized to predict the current produced by the thermal movement of the graphene. For the MDS simulations, imagine a parallel plate capacitor with a time-varying capacitance given by $C(t) = \varepsilon A / z(t) + 1.5$, where ε is the permittivity, $A = 177 \ nm^2$ is the area of the graphene, z(t) is the height of the graphene, and the fixed frame of the capacitor is

placed 1.5 nm away from the upper electrode (graphene). This distance was chosen such that graphene did not contact the electrode.

As graphene fluctuates, the distance between the ripple and the electrode varies with time as shown in Fig 2.12a. The capacitance also varies with time as shown in Fig 2.12b. If we set the bias voltage to be 1 V, then the charge, $Q(t) = C(t)V$ on the capacitor and the rectified current varies with time, as shown in Fig 2.12d.
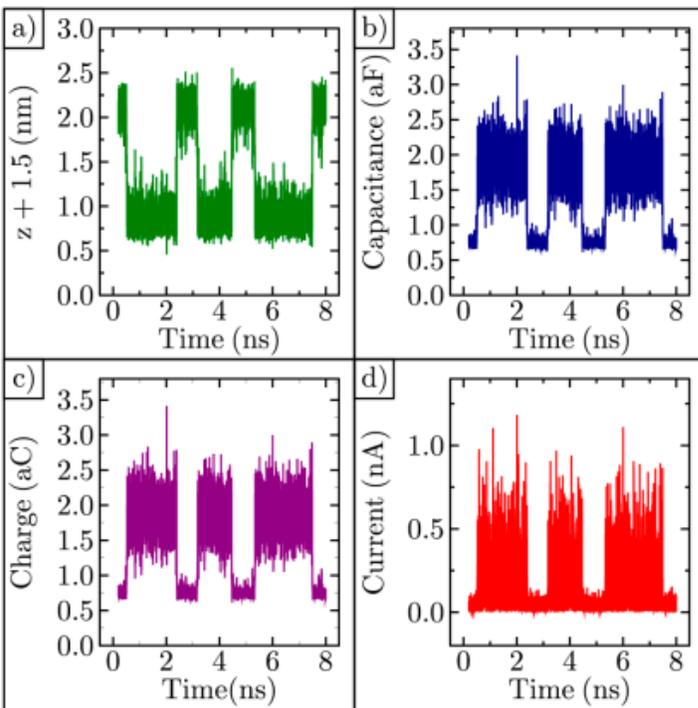
Figure 2.12 MDS simulations to quantify graphene vibration motion. (a) The variation of distance between the electrode and the ripple. (b) Varying capacitance of the graphene-electrode capacitor. (c) Charge on the graphene capacitor. (d) Rectified portion of the alternating current flowing in the circuit. Figure adapted from [135]

With these experiments, thermal fluctuations of graphene have been quantified using current collected by a nearby electrode. This proves that graphene has potential for being incorporated in a circuit as a capacitor component and can be incorporated in vibrational energy harvesting circuits.

CHAPTER 3

3 Graphene as a Nano-Electromechanical Systems (NEMS) Material

NEMS are a class of devices that integrate electrical and mechanical functionality at the nanoscale level. Due to this integration, NEMS play an important role and have great potential for applications in the fields of computing and sensing. NEMS are the logical miniaturization step from the Microelectromechanical systems (MEMS) [141]. Thin films and nanomaterials are used in NEMS to reduce the device sizes while maintaining or reducing the devices actuation voltage.

With the current rapid device miniaturization and increased growth in autonomous systems and devices, there's an increased need for devices that can operate for prolonged time periods without the need for human intervention. A special emphasis lies in the search for battery alternatives because the slow development of batteries is a setback to technological progress. Batteries run most of the portable devices such as smartphones, tablets, computers, and watches. There is hence a need to develop new sources and storage. These developments make possible the potential use of ambient vibrations as a power source, in lieu of batteries [142-144].

Graphene is the ultimate limit of thinness (single carbon layer) and hence it's a prime candidate for NEMS material. Graphene nanoelectromechanical systems show a promising future. Due to its amazing electronic properties, when combined with nanoscale movable structures, graphene has the potential for development of devices that can interact with single atoms [145]. Graphene processing is also compatible with other top-down processing techniques making its integration with other components possible.

Challenges facing graphene NEMS are mostly scaling and reliability since most fabricated devices are based on the fabricating laboratory demonstrations. They cannot be produced on large scale.

3.1   Efficient circuit design for low power vibrational energy harvesting.

With device miniaturization and reduced power requirements for devices, there's need for optimized power harvesting and optimized efficiency in the energy conversion [146, 147]. Many studies have been done on this research area [148, 149]. We performed studies to determine the circuit topography for low power energy harvesting. This work has been published in the AIP Advances journal [150].

The most efficient circuit uses a variable capacitor (VC) as the power source, a DC bias voltage to charge the variable capacitor, two transistors for rectification, and two storage capacitors as shown in Fig 3.1a. The VC has both movable and fixed semi-circular plates. Maximum capacitance occurs when the plates are aligned, and minimum capacitance occurs when the plates have no overlap as shown in Fig 3.1(b-c) respectively. As the VC plates rotate, capacitance changes linearly from maximum to minimum and back for each complete rotation as shown in Fig 3.1d.
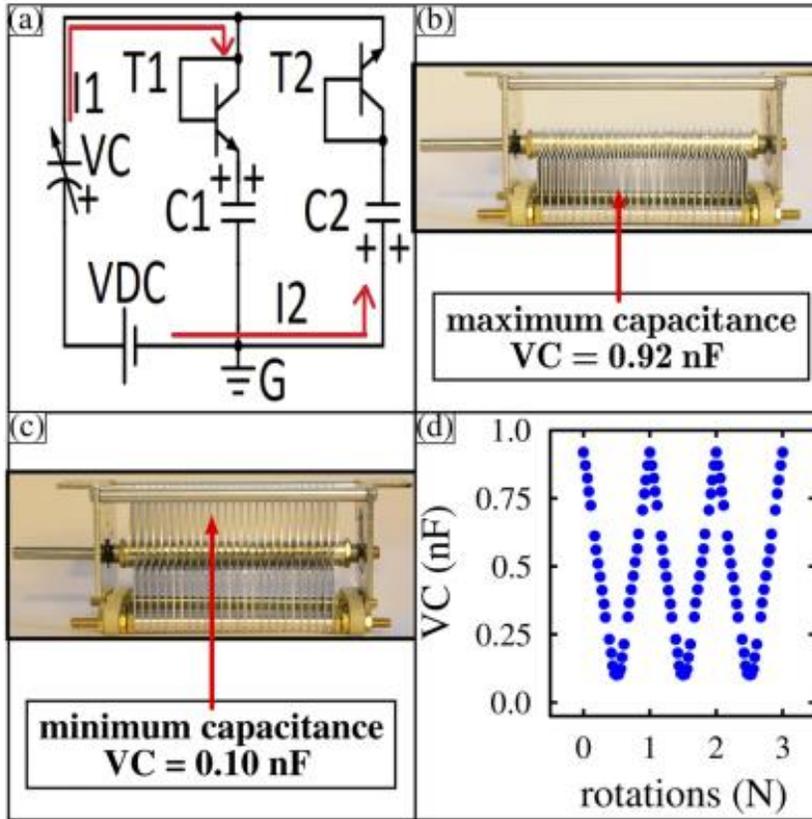
Figure 3.1: Vibrational energy harvesting (a) Schematic for the energy harvesting circuit. (b) Photograph of the variable capacitor at maximum capacitance. (c) Photograph of the variable capacitor at minimum capacitance. (d) Capacitance variation vs the number of 360 rotations. Figure adapted from[150].

Energy harvesting occurs when the VC is rotated. To test the circuit, DC voltage was set at 6.0 V and VC rotated with a frequency of 1 Hz. The voltage on C2 (V_{C2}) was then measured as a function of number of rotations N, as shown in blue in Fig 3.2 a. Voltage increases continuously and saturates at $V_S = 4.2\,V$. The voltage on C1 was also measured, and it matches that on C2. Note that it is not possible for the battery to contribute to V_{C2}. Since voltage V_{C2} is a function of rotations (or seconds for 1Hz rotations), we fit the voltage using the following function

$$V_{C2}(t) = V_S \left(1 - e^{-\left(\frac{t}{\tau}\right)}\right)$$

where τ is the only fitting parameter and was found to be 819 s. The fit line is shown in red in Fig 3.7a.

Current flowing into C2 was also measured as a function of the VC rotations. In the early stages of charging (zero to ten rotations), the current oscillates at 1 Hz, as shown in Fig 3.7 (b). The maximum current is about 12 nA, and the width of each current spike is about half the cycle. As the number of rotations increases, the capacitor continues to charge. The height of the current spikes remains relatively the same, but the width of the current spikes decreases, as shown in Fig 3.7(c-d). This implies that as the number of rotations increase, less current is flowing onto the capacitor.
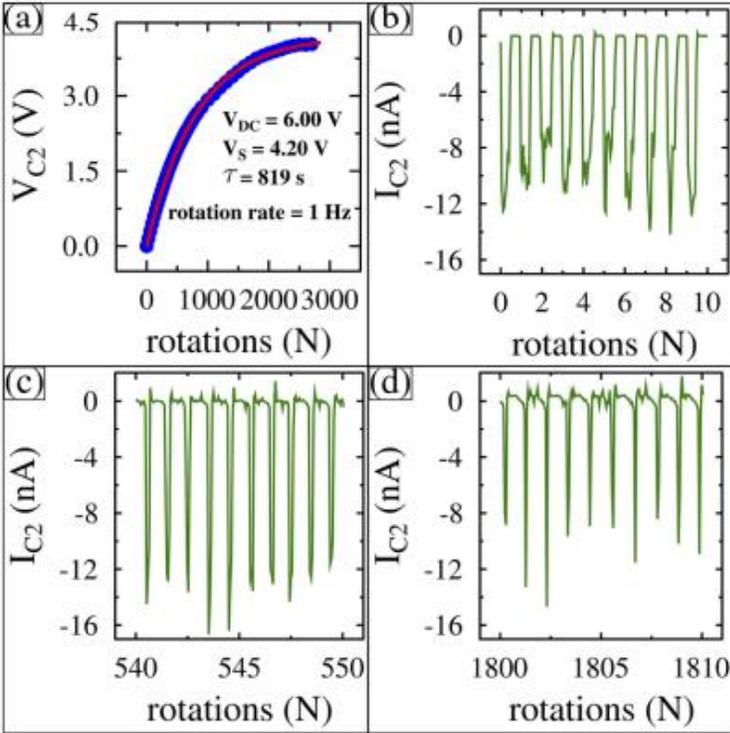
Figure 3.2: Voltage and current measurements (a) Measured voltage on C2 (blue) and fit (red). (b) Measured current flowing to C2 near VC2 = 0.00 V, (c) near VC2 = 2.03 V, and (d) near VC2 = 3.75 V as a function of the rotation number for ten rotations. Figure adapted from[150].

Using the voltage data VC2, the charge stored on C2 as a function of time was calculated using $Q = CV$ and is shown in Fig 3.3a. Next, the average current was calculated using $I = dQ/dt$ and is shown in Fig 3.3b. The average current starts off at a maximum and decreases with time. This is consistent with the decreasing width of the current spikes shown in Fig 3.2. The average power delivered to C2 as a function of time was calculated using the voltage data in Fig 3.2a multiplied by the average current data in Fig. 3.3b and the results are shown in Fig.3.3c. The maximum power delivered to C2 is found to be 5 nW, and this occurs at 570 s. In order to determine

the role of the DC power source, its value was varied from 3 V to 6 V in 1 V increments. Raising VDC raises V_S linearly, as shown in Fig 3.3d.
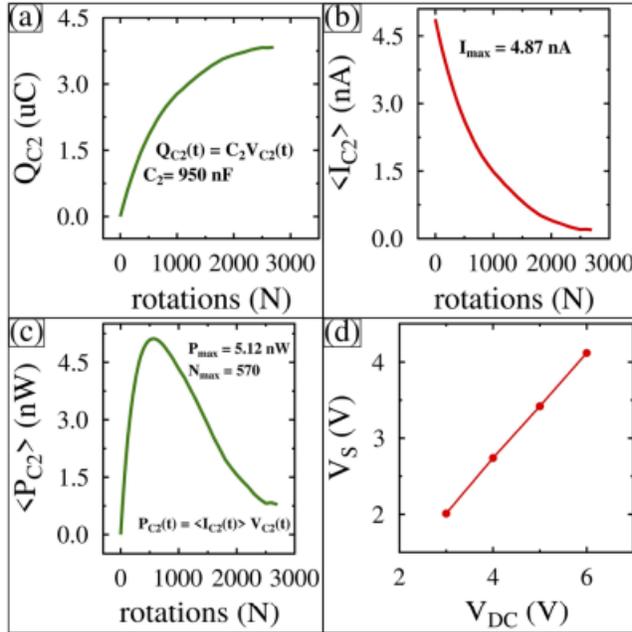
Figure 3.3: Effects of rotations. (a) Charge versus number of rotations (b) Average DC current versus number of rotations. (c) Power versus number of rotations. (d) Linear relation between maximum voltage Vs versus DC bias voltage V_{DC}. Figure adapted from[150].

Results from this study found that the power is delivered to C2 at a maximum efficiency of 25%. Given the same power is delivered to C1, the circuit has an efficiency near 50% [2]. Even though the capacitance in this experiment was manually rotated to produce power, this proves that a varying capacitance from ambient sources can be used as well. Such a circuit can be integrated in a silicon circuit and duplicated for vibrational energy harvesting. Since graphene is a highly flexible and conductive membrane, it has potential for application in a vibrational energy harvesting circuits.

3.2 Graphene application in vibrational energy harvesting

With current environmental concerns due to global warming and depletion of fossil fuels, renewable energy sources are becoming popular. Also, advancement in wearable and portable devices, there is need for development of miniature energy harvesting and storage devices. Despite the development in the conventional energy harvesting and storage devices, their application in smaller devices faces challenges such as their large rigid volume, uncustomizable shapes and inability to achieve large scale integration. There is therefore great need for exploring and developing designs and materials that tackle this challenge. There is need for a light weight, flexible and miniature power sources and storage devices. Graphene with its many amazing physical and chemical properties, such as high flexibility and electrical conductivity, is a great candidate. Extensive electrode materials ranging from 0D quantum dots, 1D nanotubes, graphene nanoribbons, Nano-rods, nanowires and 2D Nano-sheets have been developed.

Graphene has been utilized in harvesting electrical energy from light energy, mechanical strains, vibrational sources and many others. Some examples include graphene Solar cells, Piezoelectric Nanogenerators (PENG), Triboelectric Nanogenerator (TENG), and thermoelectric Nanogenerators, micro batteries, and micro supercapacitors. Focus on vibrational energy harvesting is mainly on using magnets or piezoelectric materials as the basis of energy transduction. Very few experiments have been done on variable capacitance based vibrational energy scavenging. A device can have the capacity to generate its own energy via self-charging. One way of making these self-charging devices is by harvesting ambient energy by using mechanical vibrations using variable capacitor.

Consider a variable plate capacitor connected to a battery at a voltage V as the plate separation is increased by moving the negative plate rightwards as illustrated in figure 3.4 below. The energy stored by the capacitor is $U_{Cap} = \frac{1}{2}CV^2$ and after separation $U'_{Cap} = \frac{1}{2}C'V^2$. The change in capacitors energy $\Delta U_{Cap} = -|\Delta C|V^2$ where the $-$ve sign emphasizes the decrease in the capacitor's energy. The capacitance decrease implies that the capacitor must partially discharge through the battery. If this was a rechargeable battery, it would be charged [151].
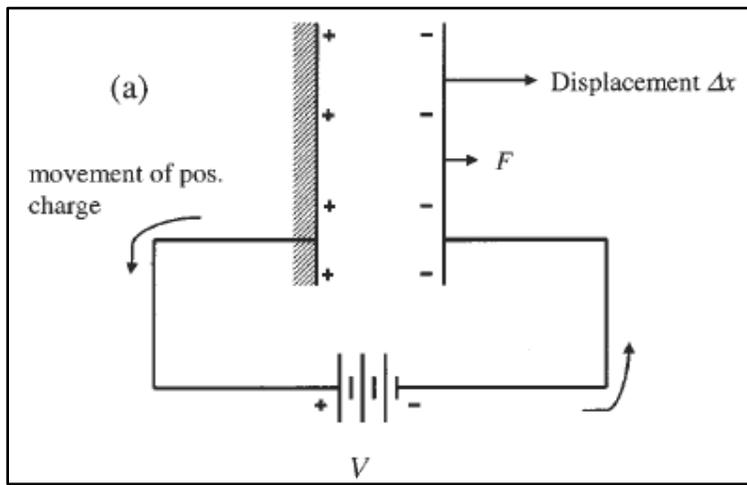
Figure 3.4: An illustration of a variable plate capacitor. Figure adapted from [151].

Since graphene is highly flexible and electrically conductive, it can be incorporated into a circuit for vibrational energy harvesting. A schematic illustration of a graphene-based variable capacitor connected to an energy harvesting circuit is shown in Figure 3.5 below. The graphene membrane is suspended above a fixed metal electrode. As the graphene membrane vibrates up and down, the distance between the graphene and electrode changes, causing the capacitance to fluctuate. Electrical charge q is forced on and off the graphene as the capacitance fluctuates with time for a fixed voltage (V) based on the equation $q(t) = C(t)V = I\,dt$.

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When charge flows clockwise it is passes through diode D1 and charges capacitor C1. When charge flows counterclockwise, it moves against the bias voltage V, charges capacitor C2, and then passes through diode D2. If the bias voltage source is a rechargeable battery, then it will be recharged during this half cycle [148, 151]. Even if the current level is Nano amps, this circuit was found to be 50% efficient when operated at its maximum output power as seen in section 3.1 [150]. Magnitude of this induced current is consistent with the constant voltage varying capacitance[151].
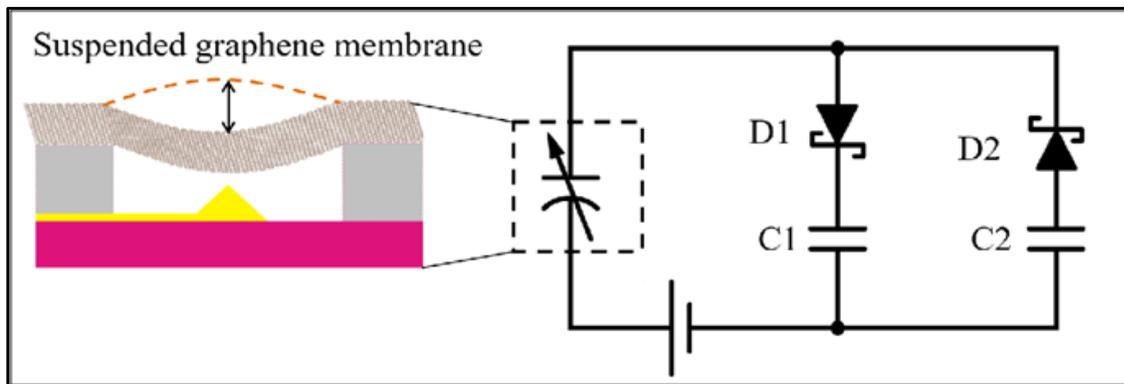
Figure 3.5: Schematic of graphene energy harvesting circuit using two Schottky diodes, two storage capacitors, a variable capacitor, and a DC bias voltage. The variable capacitor represents the suspended graphene over a fixed metal electrode as shown in the side illustration.

CHAPTER 4

4   Fabrication of an Array of Graphene Variable Capacitors on 100 mm Silicon Wafer.

We describe the procedures involved in fabrication of an array of graphene based variable capacitors on 100 mm silicon wafers utilizing the standard silicon fabrication processes and other techniques [152, 153]. The design and fabrication is presented in a 3-step process. First, there is creation of trench, well and tip feature by etching an underlying sacrificial silicon dioxide layer with 5:1 buffered oxide etch (hydrofluoric acid) [152-155]. Next, there is creation of conductive metal traces and bonding pads and lastly, we perform large area graphene transfer and graphene suspension using a critical point dryer.

We use 100 mm diameter, low resistivity, 500 µm thick, ⟨100⟩-oriented silicon wafers which have a 2 µm high quality SiO_2 layer purchased from University WAFER. A final design concept for a completed wafer containing thousands of graphene variable capacitors is illustrated in Fig 4.1 below. The pattern is aligned to the wafer cleavage planes and has 57 identical 1 cm by 1 cm patterns as shown in Fig. 4.1(a). Each unit is numbered and a zoomed-in view of unit 21 is shown. The unit has over 100 graphene variable capacitor test structures with varying trench lengths.

The shortest trench length in section F is shown with a zoomed-in view just below. Each variable capacitor has two metal contacts separated by a long trench. In the top view of a single variable capacitor, it shows the two metal contacts separated by a long trench. The tip-well structure is on the right also with a zoomed-in view. The semi-transparent green sheet is graphene covering the square well and simultaneously touching the metal pad on the right.

A metal trace runs from the tip along the bottom of the trench to the metal pad far off to the left. The long trench provides space for the graphene placement without contacting the left metal contact, which connects to the tip. A cross-sectional side view of the single variable capacitor is shown in Fig. 4.1(b). A zoomed in view of the graphene suspended over the square well with the metal cone underneath is also shown. In this zoomed-in side view, it is easy to visualize how the capacitance of this structure will alternate in time if the graphene moves up and down.
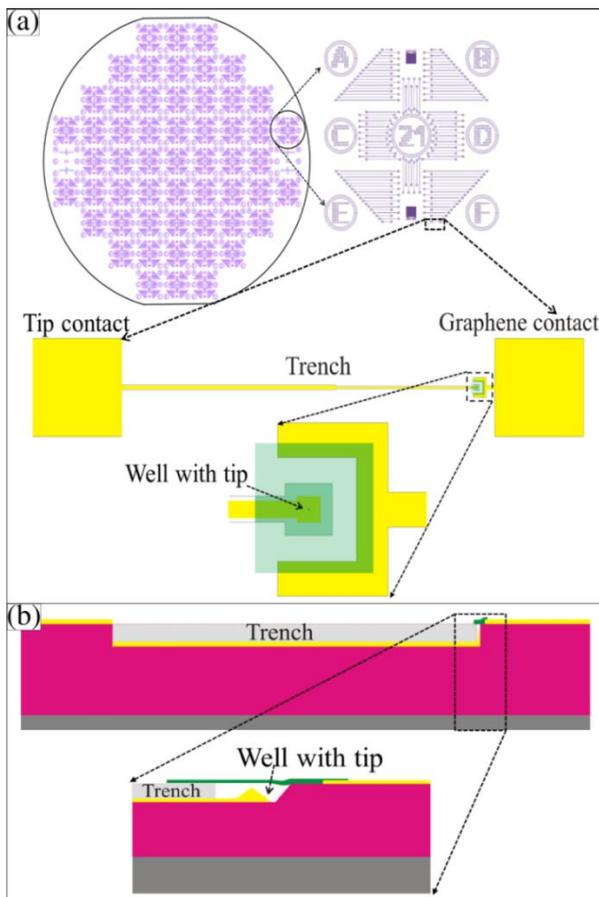
Figure 4.1: Schematics of the wafer design layout. (a) 100 mm silicon wafer with an array of 57 identical patterns next to a zoomed-in view of a single 1 cm square unit. A top view illustration of a single graphene variable capacitor with metal contacts is also shown. (b) Cross-sectional side view and a zoomed side view of a single graphene variable capacitor.

To create the trench, well, and tip structures into the silicon dioxide we use 5:1 buffered oxide etch (hydrofluoric acid) for isotropic wet etching. Wet etching refers to the process of dissolving material from a substrate which is immersed in an etchant. In Isotropic etching, materials are removed uniformly in all directions (etching processes with equal etch rates for all directions). Wet etching is a common microfabrication technique used in silicon photonics. Etching plays a critical role in microsystems technology and in fabrication of integrated circuits (IC) [156-159]. The chemical equation involved in HF etching is

$$SiO_2 + 6HF \rightarrow SiF_6 + 2H_2O + H_2$$

The depth of etched channels is controlled by concentration of the etchant (controls etch rate) and etch time. AFM and optical microscopy to are used to characterize the etched surface morphology. The images obtained from AFM are analyzed in Gwyddion to create a linear representation of the etched region. We characterize the etch depth, the height and width of the created tip feature and also the width of the created well. These are critical dimensions in the creation of the capacitors.

4.1 Mask 1 processes: Creation of trenches, wells, and tip features

Mask 1 defines the location and size of the trench, well, and tip features as shown in Fig 4.2 below. It is designed to pattern a 100 mm silicon wafer all at once, creating 57 identical regions each measuring 1 cm by 1 cm. The edges of the square regions are oriented along the cleavage planes as shown in Fig 4.2(a). A zoomed in view of one square unit is shown in Fig 4.2(b). Each square unit contains more than 100 patterns that ultimately give rise to the long trench, the square well, and the tip. A zoomed in view of one complete pattern is shown in Fig 4.2(c). The shaded areas of the pattern will be etched, while the white areas remain protected from the etchant.

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The 5 µm by 5 µm shaded region with a 2 µm by 2 µm unshaded region inside it allows the square well to form and a central cone-shaped tip to be created in a single etch step. As the shaded section etches, the etchant will begin to undercut the 2 µm by 2 µm protected region. Over time, the etchant will fully undercut the central region causing the protective resist to ultimately float away. A cone-shaped tip feature in the middle of the etched out square-well structure is left behind.
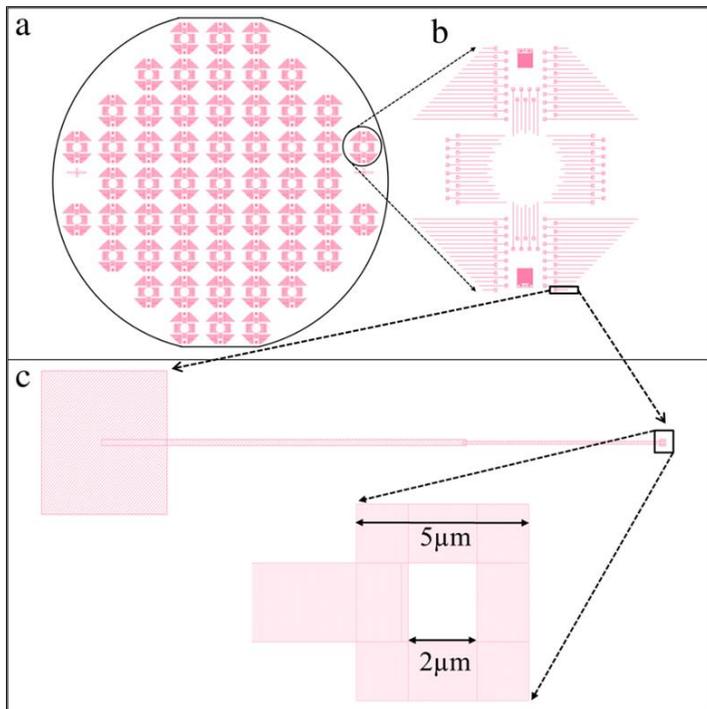
Figure 4.2: Mask 1 design pattern. (a) Fully patterned wafer with an array of 57 identical square sections. (b) Zoomed-in view of a $1cm$ by $1cm$ region. (c) A pattern that will yield a single trench, well, and tip structure and a zoom in of the region where the tip feature is formed.

A detailed processing procedure for creating the trench, well and tip feature using photolithography are illustrated in Fig 4.3(a-f) below. First, a layer of AZ 5214E resist is spin-coated on the SiO_2 layer and baked at 180^0 C for 5 minutes. Next, photolithographic mask 1 is then

used during the exposure process to mark the pattern on the wafer. Once exposed, the pattern is developed for 30 seconds in n-amyl acetate, 20 seconds in Methyl isobutyl ketone (MIBK) and rinsed in Isopropyl alcohol (IPA) to remove the exposed resist.

This patterning step is done at Sandia National laboratory. The challenge we had was resolving the 2 µm by 2 µm region using the photolithography machinery available on campus. Once we receive the fully patterned and developed wafer, we dice it into $1cm * 1cm$ patterns and do all the procedures in Fig 4.3(d-f) on these individual wafer samples. This is done to establish the etch rate. The entire wafer is next placed in a 5:1 buffered oxide etch containing hydrofluoric acid (HF) for 5 minutes at room temperature. This etches the exposed SiO_2 material isotropically and undercuts the resist to form the tip as illustrated in Fig 4.3(e). The duration of etch determines the depth of etched trench and the height of the tip structure.

After etching, the wafer is double rinsed in deionized water to stop any further etching. The sample is then soaked overnight in Remover PG to remove the resist, rinsed with IPA, and then blow dried with Nitrogen to keep the wafer spot free. Double rinsing the sample in remover PG helps prevent re-deposition of the resist.
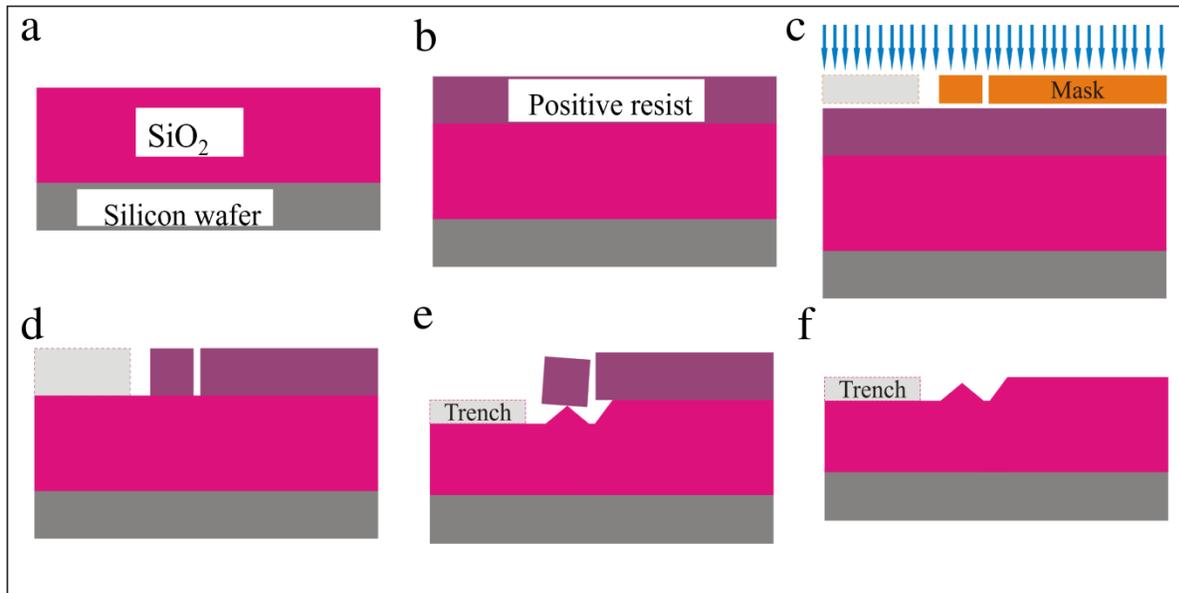
Figure 4.3: Schematic illustration of trench, well and tip structure formation processing steps. (a) Low resistivity silicon wafer with a 2 µm thick SiO_2 layer(b) resist layer spin-coated on wafer and baked for 5 minutes (c) mask 1 is applied during photolithography exposure; (d) patterned wafer after developing (e) isotropic etching of SiO₂ layer in hydrofluoric acid for 5 minutes to create the trench, well, and tip feature and (f) final wafer with trench, well, and tip feature after resist is removed.

To confirm that the wafer has been successfully etched and resist completely removed, we acquire optical microscope images as shown in Fig 4.4(a-b). The pattern has transferred to the wafer and uniformly covers the entire wafer. Next, we use AFM to measure the topology of various tip-well structures throughout the wafer. A typical AFM image and its cross-sectional line profile are shown in Fig 4.4(c-d). In this image, the top of the wafer is white, and the square well is mostly black with a central feature inside the well that is white. Notice the lower edge of the image of the square well is black because this is where trench structure intersects the well.

From the cross-sectional line profile, that cuts horizontally through the tip in the AFM image, one can see that the well is 0.5 μm deep and that is has a tip protruding from the bottom and is in the center of the well. Also, notice that the top of the tip feature is 0.15 μm from the top of the wafer. This pattern was reproduced with a high degree of accuracy across the entire wafer. The distance between the top of the tip and the top of the wafer is an important parameter that we control and reproduce. This parameter is critical since it determines the distance between the two plates of the variable capacitor (suspended graphene and this fixed tip).
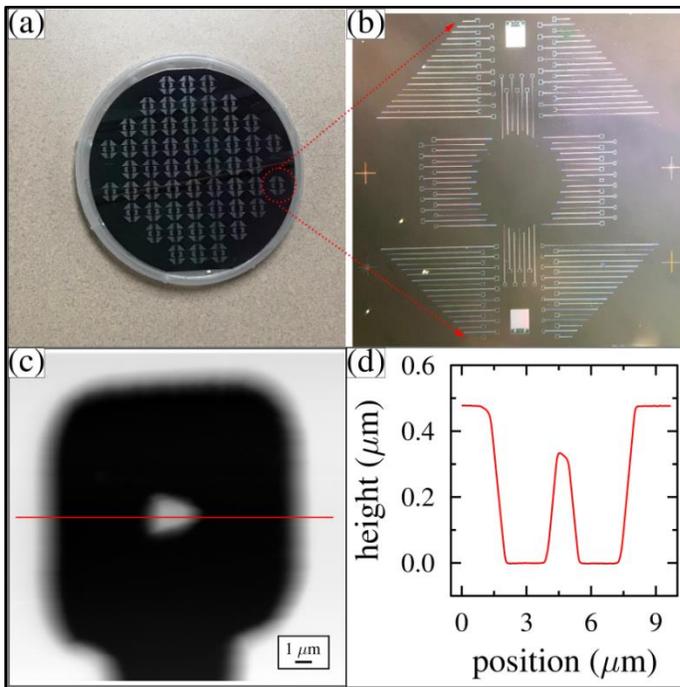
Figure 4.4: Optical microscopy and AFM images after mask 1. (a) patterned 100 mm wafer with an array of 57 identical features; (b) high resolution optical image of a single 1 cm square unit; (c) AFM image of a single square well with cone-shaped tip at its center; and (d) AFM line profile taken horizontally through the tip from the image shown in (4.4c).

Optical microscope is also used to make comparison of the structures before and after etching with resist removed as shown in fig 4.5(a-b) below. The obvious color difference gives an optical confirmation.

Figure 4.5: Optical images to confirm etching: (a) Optical image before HF etching, and (b) Optical images after 5 minutes HF etching and resist removal.

4.2 Mask 2 processes: Metal traces and bonding pads

Mask 2 processes define the position and size of the conductive metal traces and electrical contact pads. The full wafer mask design is shown in Fig 4.6(a). A zoomed-in view of a single 1 cm square of mask 2 design region is shown to the right. Mask 2 must be precisely aligned to mask 1. To ensure that these two masks are aligned, several alignment markers are written into the wafer during the mask 1 etching. These marks can be seen in Fig 4.4(b) .This mask writes the labels into each 1cm unit (unit number 21 is shown).

A zoomed-in view of single trench, well, and tip structure is shown in Fig 4.6(b), which also contains another zoomed-in view of the tip-well region. A metal footprint smaller than the square well but larger than the tip is used to ensure the tip is coated with metal. In addition to a metal contact pad to the right of the tip-well region, we also add a metal horseshoe type design

around the tip-well structure but on the top of the wafer. This will guarantee electrical contact to the graphene when placed on top of the wafer during a later step in the fabrication process.
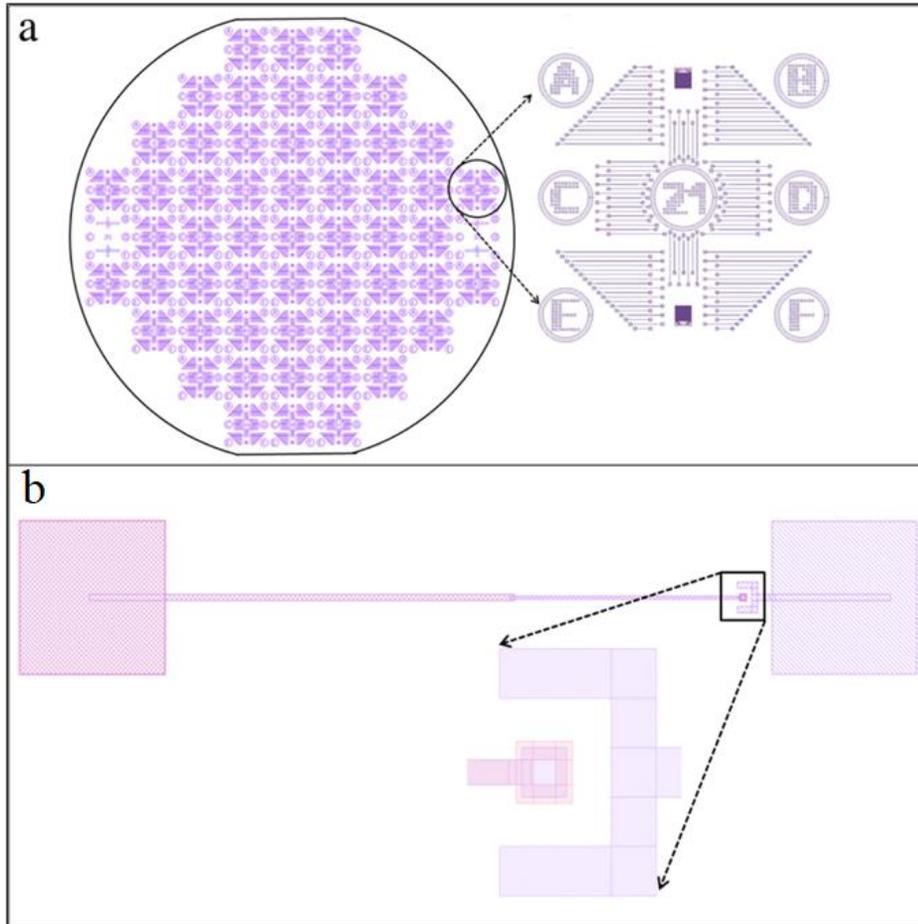
Figure 4.6: Mask 2 design pattern. (a) Fully patterned wafer with 57 identical units and a zoomed-in view of one of the 1 cm units; and (b) A single trench, well, and tip structure with a zoomed-in view of the tip-well region with a graphene bonding pad to the right of the tip-well structure.

A detailed illustration of mask 2 processing is shown in Fig 4.7(a-f) below. First, AZ 5214E resist layer is spin-coated and baked at 180^0C for 5 minutes. Mask 2 is the used to pattern the conductive paths and bonding pads onto the wafer. The wafer is developed for 30 seconds in n-Amyl acetate, 20 seconds in Methyl isobutyl ketone (MIBK) and rinsed in IPA. To create the

electrical pathways, we deposit 5 nm Chromium onto the substrate followed by 100 nm of gold. The thickness of this gold layer is a variable parameter used to control the capacitance by varying the distance between the graphene and this fixed metal tip. The wafer is soaked overnight in 50-50 acetone-Remover PG mixture for liftoff and then rinsed in IPA. We then blow dry the sample with Nitrogen gas to ensure that the sample dries without spotting.
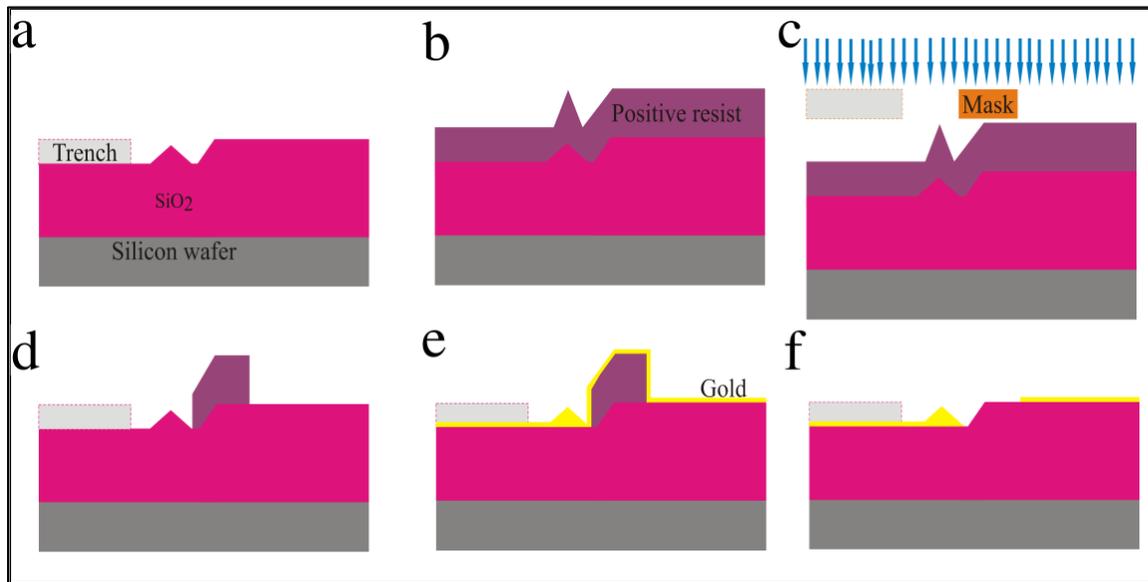
Figure 4.7: Schematic illustration of mask 2 processes. (a) Wafer with trench, well, and tip feature throughout. (b) Resist layer spin-coated and baked for 5 minutes. (c) Mask 2 is applied during photolithographic exposure. (d) Patterned device after developing. (e) Deposition of 100 nm of gold. (f) Final metallized wafer after liftoff.

Optical microscopy and AFM images are used to characterize the wafer after completing the mask 2 processes. An optical photograph of the full wafer is shown in Fig 4.8a. The pattern was successfully reproduced across the entire wafer. A high-resolution image of the gold coated tip, trench, and pad around the well is shown in Fig 4.8b. Notice how the horseshoe spans three

sides of the tip-well structure. AFM is also used to characterize the position of the metal deposition inside the well and to determine the thickness of the metal layer as shown in Fig 4.8(c-d). From the cross-sectional line profile that cuts horizontally through the tip in the AFM image, one can see that the well is 0.5 µm deep and the thickness of deposited metals is 0.1µm. From these, we can confirm the desired amount of gold was deposited and use it to control the height of the tip feature during this part of the process. This pattern was reproduced with a high degree of accuracy across the entire wafer.
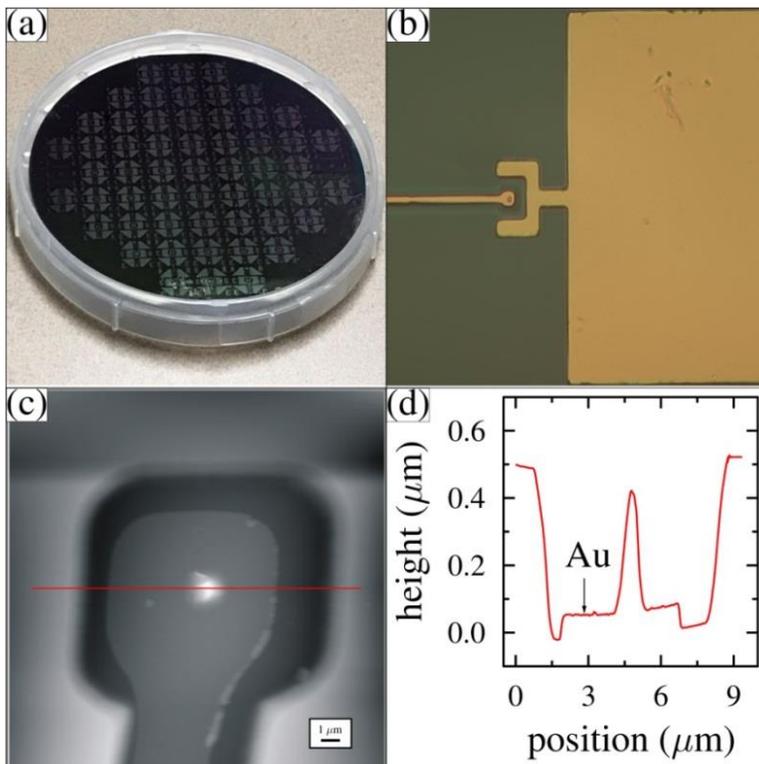
Figure 4.8: Optical and AFM images. (a) Mask 2 patterned full wafer; (b) tip-well feature with bonding pad after gold deposition; (c) AFM image of a single tip-well structure; and (d) Horizontal line profile through the tip in (c) that reveals the gold thickness.

Figure 4.9(a-b) show optical images the tip region before and after gold deposition.
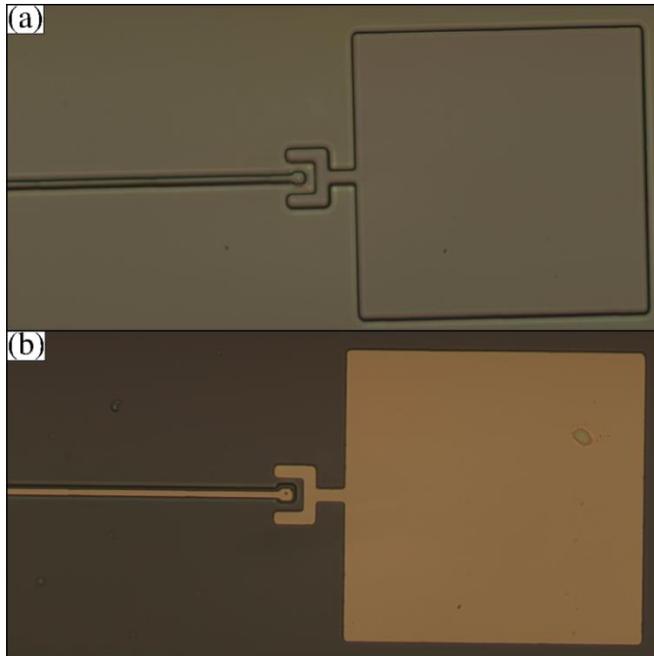
Figure 4.9: Optical images showing the patterns before and after gold deposition: (a) Before gold deposition, and (b) after gold depostion.

4.3 Graphene placement and suspension

We use commercially available multilayer graphene that is grown on Ni that has been deposited on a silicon chip (graphene-Ni-Silicon chip). This is purchased from graphene supermarket. The main goal is to ensure that graphene is properly placed to make electrical contact with the graphene bonding pad but not electrically shorted to the tip bonding pad.

We also require that the graphene be suspended over the array of tip features and not make direct electrical contact with them (shorted). The ideal placement location for the graphene on one of the 1 cm square regions of the wafer is shown schematically as a rectangular green strip in the upper right corner in Fig 4.10 below.
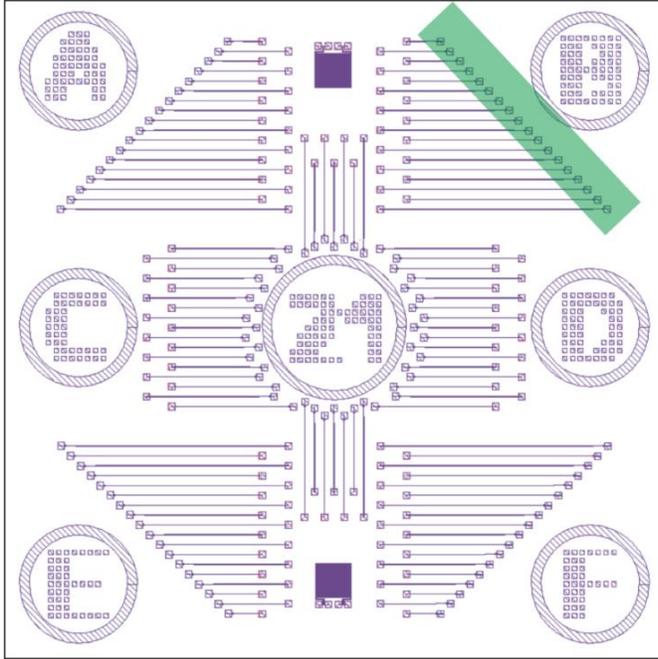
Figure 4.10: Illustration of graphene location on the wafer.

The large area graphene transfer process is schematically illustrated in Fig 4.11. We start with the commercially prepared graphene-Ni-Silicon chip. Graphene grown on metals and transferred to other substrates tend to form wrinkles. To counter this, a layer of polymer is spin-coated on the graphene on metal [25]. In this case, we then spin coat a layer of PMMA over the graphene and bake it at 180^0 C for 4 minutes.

Next, Scotch tape is used to peel off a thin strip of the PMMA-graphene-Ni layer from the silicon chip. The pealed strip is then placed in $FeCl_3$ etchant for 20 minutes to dissolve the nickel layer. We transfer the tape-PMMA-graphene stack to DI water to wash off the $FeCl_3$ solution. The tape is separated from the PMMA-graphene stack and the graphene is placed on the desired region of wafer. The entire wafer with the PMMA-graphene is then set at an angle for 10 minutes to dry in position.

The PMMA is then dissolved off soaking the sample in acetone for 10 minutes. To prevent the sample from air drying, it is quickly transferred to hexane. The sample is then quickly introduced into a critical point dryer (CPD) instead of air drying. We use Tousimis Autosamdri 815B model of CPD shown in Fig 4.13 with hexane as the transitional liquid and then replaces it with Liquid Carbon dioxide (LCO$_2$). Critical point drying eliminates the surface tension associated with the liquids by avoiding the phase transition boundary from liquid to gas as illustrated in the critical point drying curve in Fig 4.14. The process converts the liquid to a supercritical fluid and then to gas (the red path).
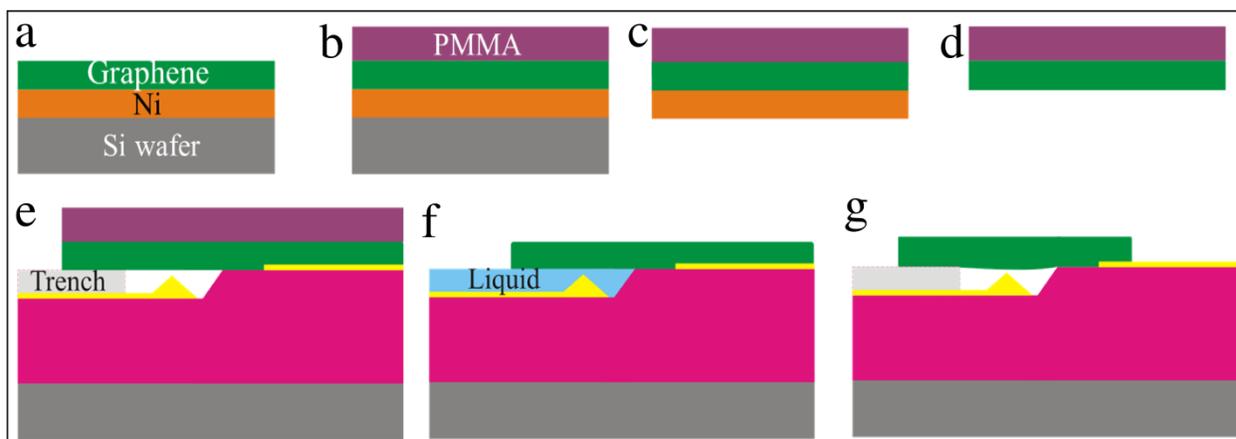
Figure 4.11: Graphene transfer steps. (a) We start with a graphene-Ni-Silicon chip. (b) Spin coat a PMMA layer. (c) Using tape to peel away PMMA-graphene-Ni layer. (d) Etch away the Ni layer. (e) Place the PMMA-graphene on our patterned wafer over an array of tip-well structures. (f) Use hexane followed by the CPD. (g) Final graphene suspended over the tip.

The various graphene transfer steps are shown as photographs in Fig 4.12(a-f). Tape is used to peel off the PMMA-graphene-Ni layer from the silicon chip as shown in Fig 4.12a and then immediately transferred to the FeCl$_3$ etching solution. FeCl$_3$ etches off Ni. After 20 minutes, the

tape-PMMA-graphene is scooped out of the etchant and transferred to DI water bath to rinse off

FeCl₃. The tape is cut off to separate it from PMMA-graphene as shown in Fig 4.12d. Next,

PMMA-graphene layer is transferred to another DI water bath and then we align and place it on

the tip regions of the devices as illustrated in Fig 4.10. The sample with PMMA-graphene is then

placed over the tip regions and set at an angle to dry as shown in Fig 4.12e. Fig 4.12f shows the

graphene location on the tip regions of the devices
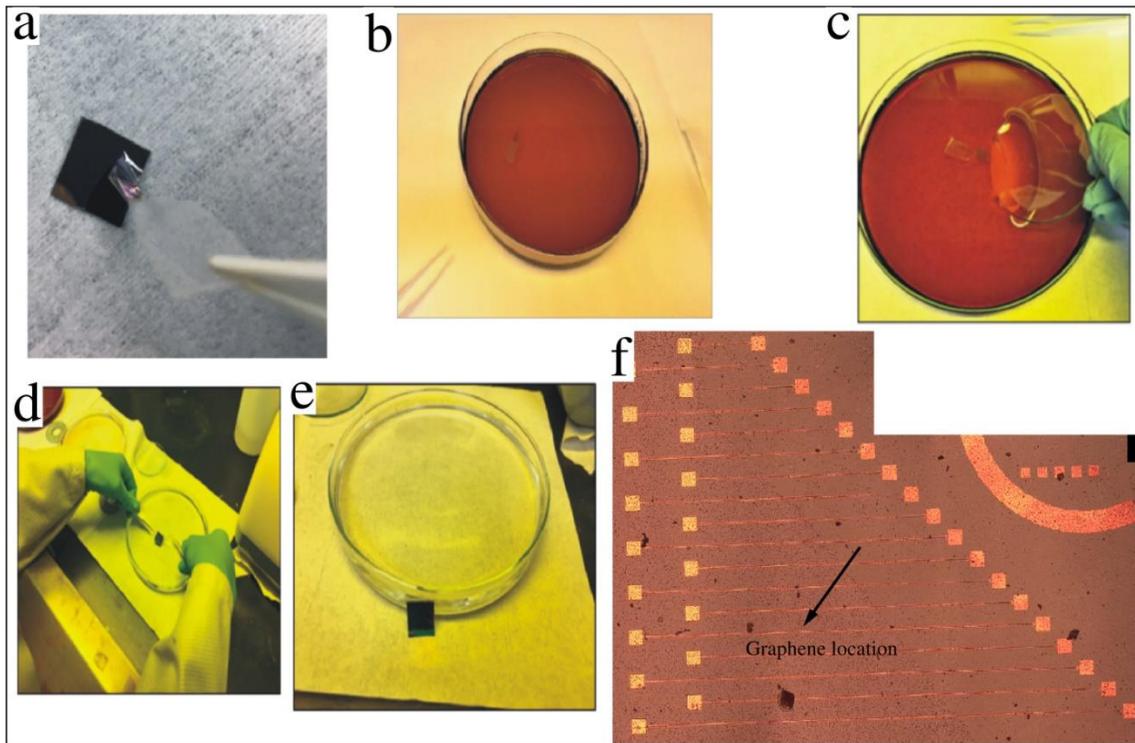
Figure 4.12: Images of graphene transfer process: (a) Tape used to peel off a thin strip of Ni-graphene-PMMA layer; (b) Nickel-graphene-PMMA layer in $FeCl_3$ solution to etch off Nickel; (c) Watch glass used for scooping graphene; (d) Aligning graphene to the tip regions of the device; (e) Placing the sample at an angle for graphene-PMMA layer to stick to our sample; and (f) Optical image showing graphene location on the devices.

The CPD not only dries the graphene-wafer system, but it also aids the suspension of the graphene over the tip features. The CPD is automated to ensure that it attains the critical point drying. The drying is a 4-step process:

i. Cool and fill: The sample still in the transitional liquid (hexane) is first cooled and then high-pressure liquid carbon dioxide(LCO_2) flows in to fill the chamber. The pressure rises drastically while the temperature remains constant.

ii. Purge: Hexane is purged and replaced with liquid CO_2. At this step, the CPD replaces and rinses off all hexane with LCO_2. If the purge time is not long enough the sample will come out with residual hexane (wet). This leads to possibility of graphene being sticking to the tip feature (not suspended).

iii. Heat: The chamber is heated and kept under high pressure until the LCO_2 is pushed past the critical point (Temperature >300K, Pressure >1072PSI)

iv. Bleed and vent: Pressure is released, and the chamber is now safe for opening to retrieve the sample. If the critical point was not achieved, then this process is repeated.

For this experiment, the CPD settings were set to the parameters Cool 0.75, Fill 1, Purge/Vent 0.75, Bleed 0.3 and purge timer 3. These settings can be adjusted based on the size and the sensitivity of the substrates being dried.

Figure 4.13: Tousimis Autosamdri 815B model Critical point dryer
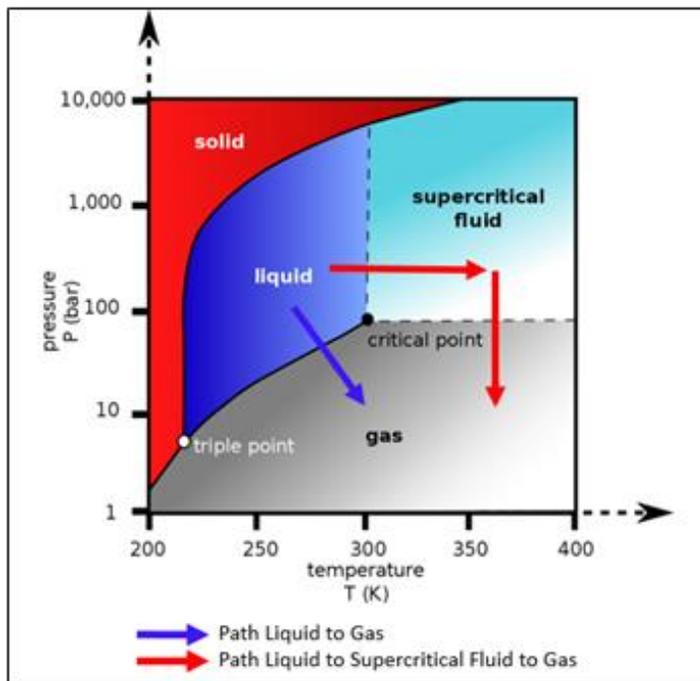
Figure 4.14: Liquid carbon dioxide critical point cycle curve

After using the CPD, graphene dries and is suspended over the tip well structures as shown in the optical image in Fig 4.15(a-b). There are instances when graphene is torn Fig 4.15c or when graphene just falls over the tip feature Fig 4.15d.
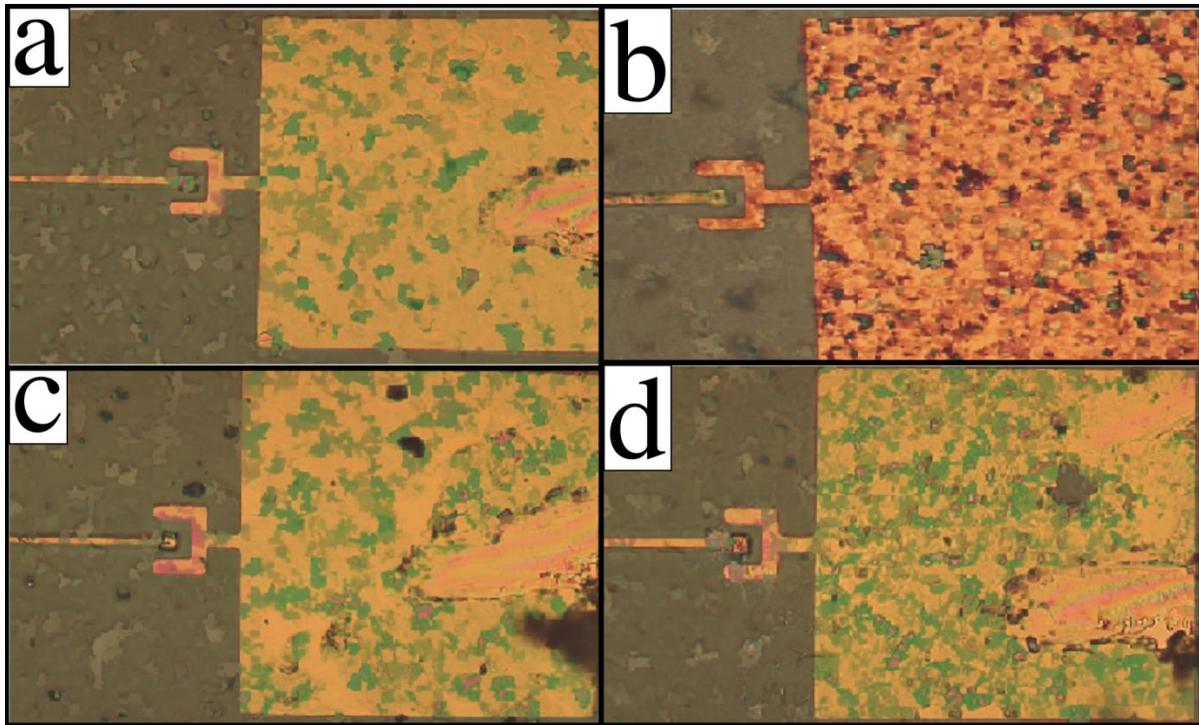
Figure 4.15: Graphene transfer images. (a-b) Graphene suspended over the tip feature. (c) Graphene ripped around the tip feature. (d) Graphene touching the tip feature (shorted)

To increase the chances of successful devices (devices that are not shorted), we can introduce Liftoff resist (LOR) windows as shown in Fig 4.16. This step is done after device metallization. First, spin coat LOR on the sample and bake at 180^0 for 5 minutes. Next, E-beam is used to expose and write this pattern on the sample followed by development. Graphene suspension is then done.
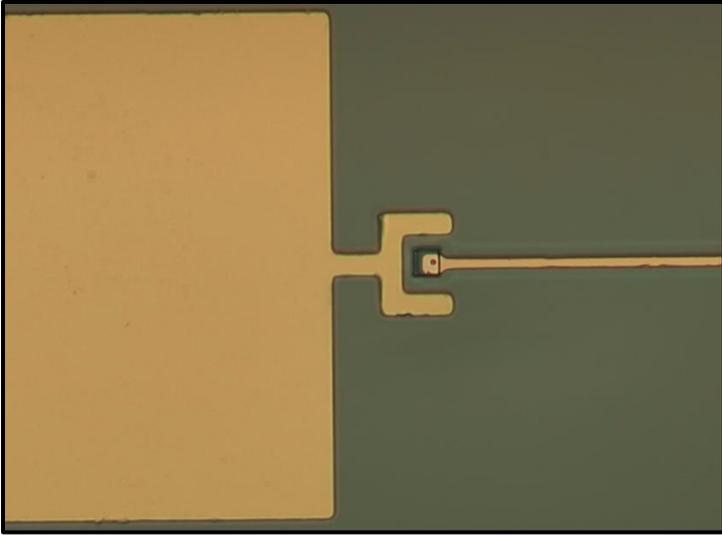
Figure 4.16: LOR windows on the tip feature

CHAPTER 5

5   Processing Bare Die with an Incorporated Integrated Circuit

In addition to developing the graphene variable capacitor fabrication process on 100 mm silicon wafers, we also reproduced the process on a bare die containing an integrated circuit below the top surface. The integrated circuit was built by Taiwan Semiconductor Manufacturing Corporation (TSMC). The TSMC chip measures 5 mm by 5 mm and contains an inbuilt rectifier amplifier circuit. The very top of the TSMC chip has bonding pads around the parameter as well as a 3 mm by 3 mm bonding pad in the center. This is an aluminum pad and can be seen in Fig 5.1(a). To remove the central Aluminum, we first cover the outer regions of the TSMC chip with carbon paint as shown in Fig 5.1(b).

Next, the TSMC chip is etched in Aluminum etchant (Aluminum Etch 80-15-3-20) for 20 minutes followed by a DI water double rinse. Fig 5.1(c) shows the chip after etching.
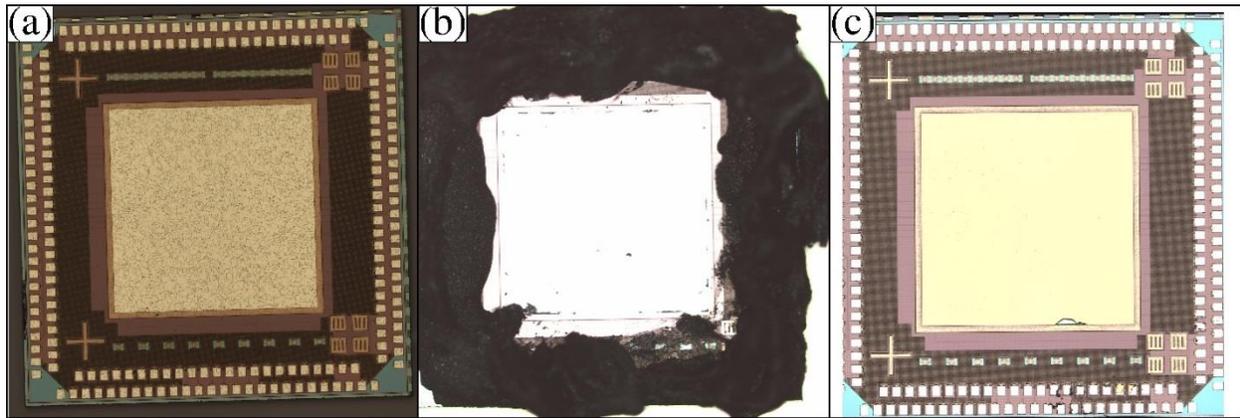
Figure 5.1: TSMC chip procedure. (a) Chip obtained from TSMC (b) Chip with the outer bonding pads covered with carbon paint; (c) Chip after etching away the central Al bonding pad.

After aluminum etching, we use AFM to confirm the etching of the Al layer. The location of the chip that is images and the resulting AFM image are shown in Fig 5.2. The Al layer is about 4µm. Next, the chips are sent to Georgia Tech for deposition of a 1µm SiO_2 layer. This layer of SiO_2 is deposited at low temperatures SiO_2 to avoid damaging of the circuit system that's already incorporated in the chip from the manufacturer.
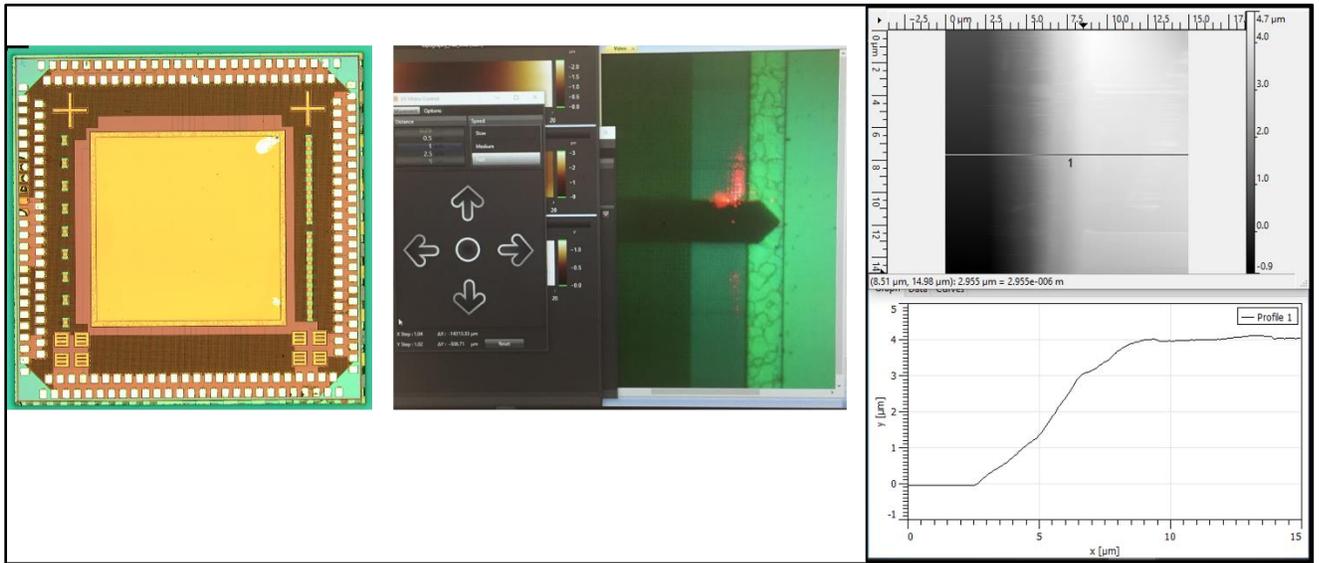
Figure 5.2: AFM confirmation of Al etching of the mid-section of the TSMC chips

These chips are then sent back, and they undergo a three-step process similar to what was discussed above to create and characterize a variable capacitor.

5.1   Alignment markers, mask 1 and mask 2

First, CSAR   is spin coated on the chip and baked at 180^0 C for 5 minutes. Next E-beam used to write alignment markers as shown in Fig 5.3a. We then deposit 5nm Cr and 50nm Au on the chip. The chip is soaked overnight in 50-50 acetone - remover PG for liftoff.

Next, CSAR is spin coated on the chip and baked at 180^0 C for 5 minutes and E-beam used to write mask 1 pattern as shown in Fig 5.3b. This layer marks the location of the devices on the sample. To develop the patterns after E-beam exposure, we soak the sample for 30 seconds in n-amyle acetate, followed by 20 seconds in MIBK and rinse in IPA. We then etch the sample for 4 minutes in diluted 16:1 hydrofluoric acid. The samples are then double rinsed in DI water, soaked in acetone for 10 minutes and rinsed in IPA. We blow dry the sample with N_2 gun to ensure the sample dries without spotting. Optical confirmation that the tip feature is created on the device after etching is shown in Fig 5.4(a-b).

Next, second layer is patterned on the chip as shown in Fig 5.3c. This layer defines the location of the metal and graphene contacts as previously discussed. CSAR is spin coated on the chip and baked at 180^0 C for 5 minutes and E-beam used to write the pattern. To develop the patterns after E-beam exposure, the sample is soaked for 30 seconds in n-amyle acetate, followed by 20 seconds in MIBK and 10 seconds rinsed in IPA. We then deposit 2nm Cr and 50 nm Au and lift off in 50-50 acetone remover PG. This process is similar to what was discussed for the full wafer.
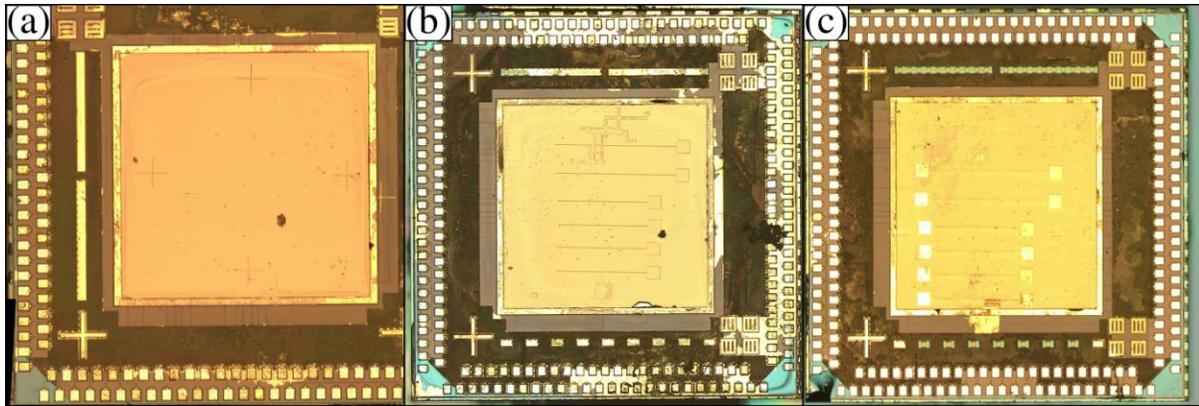
Figure 5.3: Optical images showing the chip processing stages. (a) Alignment markers on the chip, (b) First layer etched on the chip , and (c) The send layer on the chip after gold deposition and lift off.
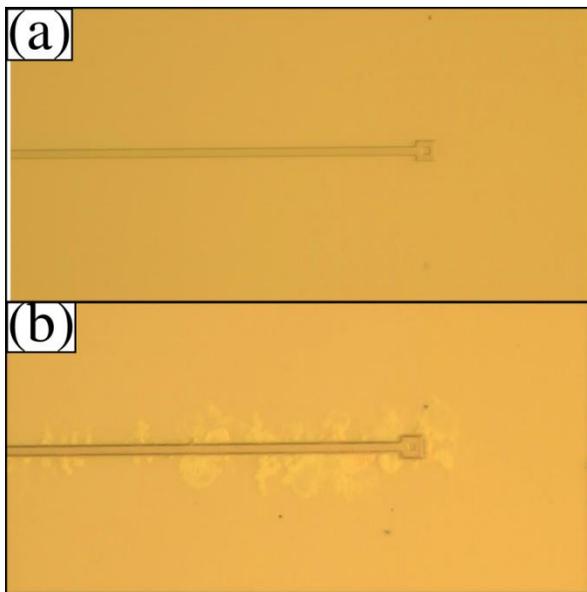
Figure 5.4: Optical images confirming tip feature formation after etching. (a) Devices before etching and, (b) Device after 4 minutes etching and resist removal.
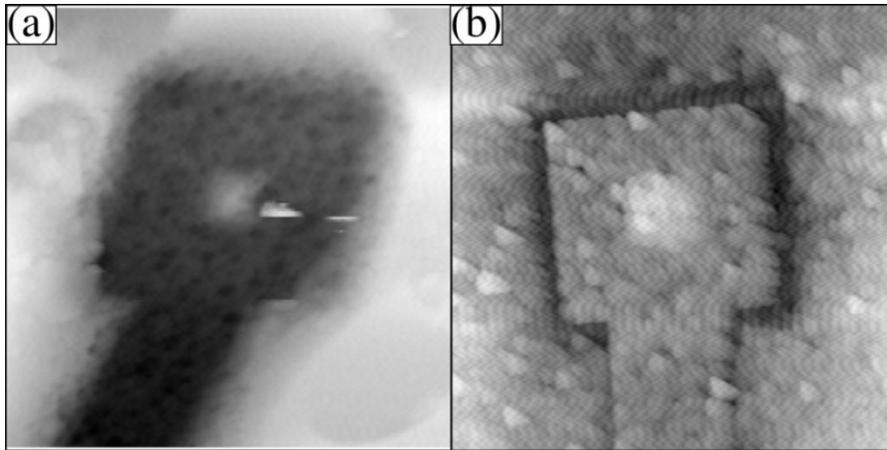
Figure 5.5: AFM images before and after gold deposition. (a) AFM image of the chip tip region after etching, (b) AFM image of the device tip region after gold deposition

After gold deposition, graphene is then suspended over the tip features. The transfer and suspension process is similar to the one described above on 100mm wafers.
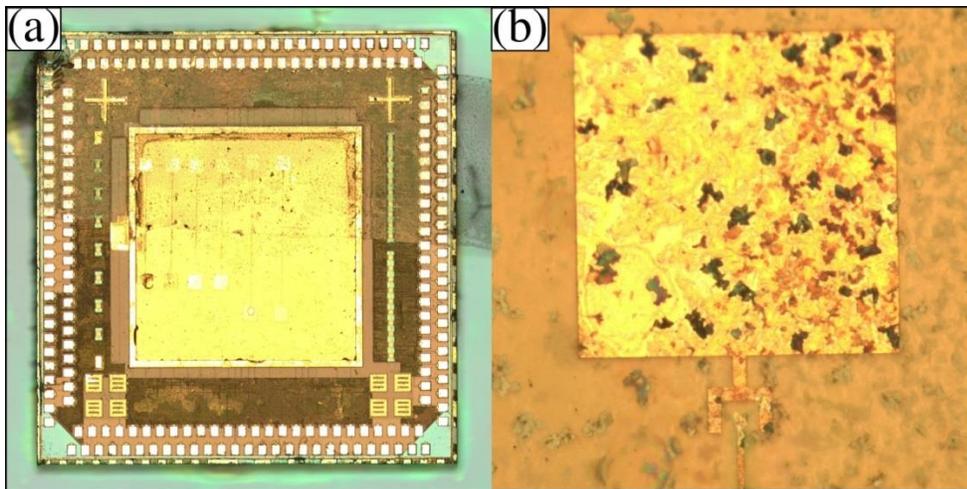
Figure 5.6: Images showing graphene location and showing suspended graphene. (a) Graphene location on the 3mm by 3mm region. (b) Graphene suspended over a tip feature.

CHAPTER 6

6   Capacitance Measurements

We use a precision high-resolution capacitance meter (AH 2550A) to measure the capacitance and resistance between graphene metal contact pad and the tip metal contact pad. A photograph of our setup is shown in Fig 6.1(a). It consists of two shielded measurement probes to touch both the graphene metal contact and tip metal. Only the small region that makes contact with the sample are left exposed. This minimizes the parasitic capacitance introduced. This experimental setup is completely grounded and sits inside a dark box to avoid interference from the surroundings (eliminate external parasitic capacitance and noises).

We can determine if the graphene is directly contacting the tip (shorted) by first measuring the resistance between the two contact pads. The resistance is much higher than $10G\Omega$ for non-shorted devices. The capacitance variations in time for the graphene variable capacitors made using the 100 mm wafer is shown in Fig 6.1(b). The variation in capacitance is about 60 aF for the graphene capacitor. The capacitance variations in time for the graphene variable capacitors made using the TSMC bare die is shown in Fig 6.1(c). The variation in capacitance is about 2 fF for the graphene capacitor. A control for each measurement is also shown.

For the control, the measurement probes are lifted just off the sample and the capacitance measurement are made in time. This control helps to determine that the measured capacitance is not just noise from the surrounding. The parasitic capacitances that are subtracted from the measured capacitance include: Capacitance from the contacts before graphene is suspended (capacitance contribution from the measurement probes), the tip-base well capacitance, and capacitance from graphene covering the trench (narrow and wider parts of the trench).

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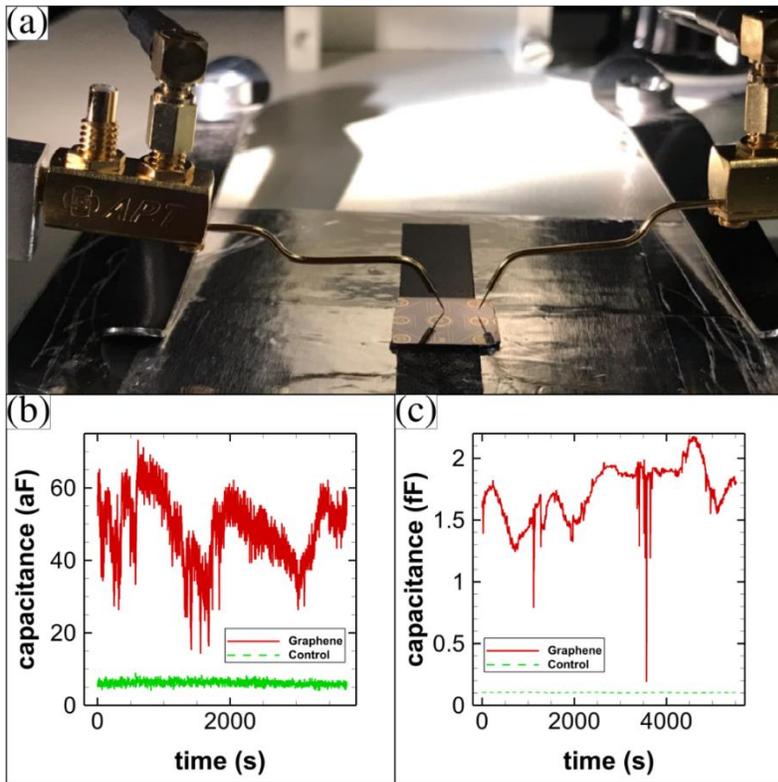
Figure 6.1: Capacitance measurements. (a) Photograph of measurement probes on the wafer. (b) Capacitance in time for the capacitors made using the 100 mm silicon wafers. (c) Capacitance in time for the capacitors made using the TSMC bare die.

CHAPTER 7

7   Effects of Temperature Variation on a Graphene Based Variable Capacitor Circuit

From the work discussed on quantification of graphene's fluctuation by observing the induced current, Ito-Langevin simulations proved that in a system made up of a variable capacitor modeled as a stochastically driven particle in a double well, a resistor and a battery, the work done by the capacitor is equal to the work done on the resistor when the temperature of the resistor and capacitor are the same. It is important to study the non-equilibrium fluctuations due to different temperatures [140, 160-162].

In this chapter, we I present a Langevin equation study using the Euler-Maruyama method of a bistable variable capacitor coupled to a resistor, with the components at different temperatures. We will model graphene ripple as a particle in a double well potential coupled to an electric circuit with Langevin and Kirchhoff's equations. First, we will fix the resistor's temperature (T_R) and investigate the effects on power generated by the capacitor's temperature (T_C) is varying. Next, we will fix T_C and investigate the effects on power generated when T_R is varying.

7.1   Circuit Model

The system is modeled as a variable capacitor with a curved membrane as the mobile plate, in series with a resistor and a battery. The atoms of the membrane closer to the electrode are modelled as a Brownian particle in a double-well potential, which is represented by the convex and concave curvature configurations of the ripple. The system is in contact with a thermal baths at temperatures T_C and T_R as illustrated in Fig 7.1.

As the particle fluctuates to and away from the fixed electrode, it acts as a variable capacitor. The position of the particle with respect to the flat configuration of the graphene membrane is given by $x(t)$ and so the instantaneous distance between the electrode and the particle is $d + x(t)$ where $d \gg x$.
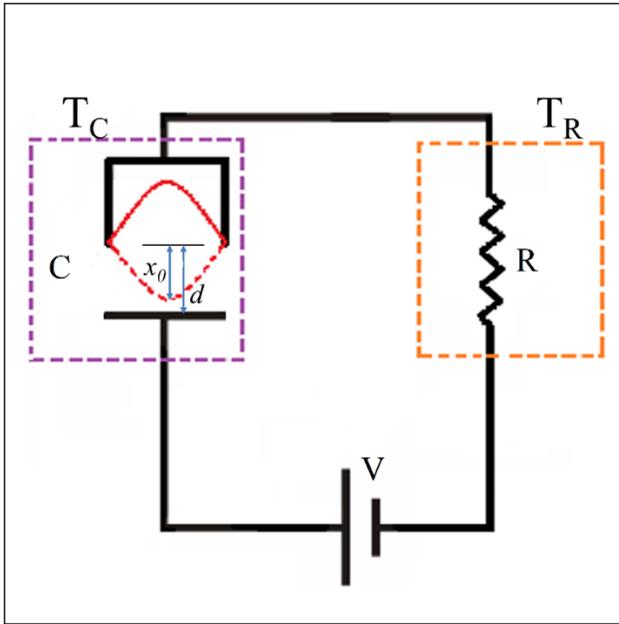
Figure 7.1: Illustration of the circuit model for the components at different temperatures

7.2 Modelling graphene ripple curvature inversion using Langevin's equation

The dynamics of the system is described by the Langevin's equation of motion. Simulations are done by modelling Ito-Langevin equations of motion coupled to a circuit containing diodes. Langevin equation is ideal because it reduces the dynamics of clamped graphene sheet to equivalent dynamics of a free point-like mass who's mass $m = 0.4M$, where M is the mass of the graphene sheet.

Ito-Langevin equations of motion associated with the particle as it fluctuates are:

$$\dot{x} = v$$

$$m\dot{v} = -\eta v - U'(x) - \frac{q^2 - C_0^2 V^2}{2C_0 V d} + \sqrt{2k_B T_G \eta}\, \xi_v(t)$$

Where

$U(x) \propto x^4 - 2x^2$ is the double well potential energy associated with the ripple.

$-\eta v$ is the damping force.

$-\frac{q^2}{2C_0 V d}$ is the electrostatic force on the particle given that the instantaneous charge and voltage drop across the tip-sample capacitor is $q(t)$ and $u(t) = \frac{q}{C(x)}$, respectively.

$\frac{-C_0 V^2}{2d}$ is a constant tension correction term for membrane curvature to compensate for the oversimplification of substituting the ripple as a particle instead of a membrane.

$\sqrt{2k_B T_G \eta}\, \xi_v(t)$ is a stochastic term associated with the random motion.

As $x(t)$ varies, it results in capacitance $C(x)$ varying from a maximum to a minimum. The capacitance is given by

$$C(x)_{min} = \frac{C_0}{1 + \frac{x_0}{d}}$$

$$C(x)_{max} = \frac{C_0}{1 - \frac{x_0}{d}}$$

Where

$$C_0 = \frac{\varepsilon_0 A}{d}$$

Since the particle is connected to a circuit, the circuit equations are defined by the Kirchhoff's circuit equations. Since the voltage drop across the capacitor is $u = q/c(x)$, the current through the resistor will be $dq = -\frac{u}{R} dt = -\frac{q}{RC(x)} dt$ where the $-ve$ sign indicates that as $I \to 0, t \to \infty$.

Using Kirchhoff's second law and the law of junctions

$$dq = -\frac{V}{R} dt - \frac{\frac{q}{C(x)}}{R} dt + \sqrt{\frac{2k_B T_R}{R}} dt\, \xi_q(t)$$

Where $\sqrt{\frac{2\,k_B T_R}{R}} \xi_q(t)$ is stochastic term for a resistor.

The Hamiltonian or the total energy of the system is given by

$$H(x, v, q) = \frac{v^2}{2} + \frac{q^2}{2C(x)} + \frac{-C_0 V^2}{2d} + U(x) + qV$$

$$\frac{dH}{dq} = \frac{q}{C(x)} + V = V_R$$

$$\frac{\partial^2 \mathcal{H}}{\partial q^2} = \frac{1}{C(x)}$$

$$\frac{dH}{dx} = U'(x) + \frac{q^2}{2C_0 d}$$

$$\frac{dH}{dV} = V + \dot{x}$$

From the viewpoint of graphene ripple (particle), the circuit is an external system that does work on it. And, from the resistor's perspective, movement of the particle produces a constant source of thermal power. Heat produced in the system is due to friction and noise forces and is given by

$$dQ = \frac{\eta}{m}(k_B T_C - mv^2)dt + v\sqrt{2k_B T_C \, \eta \, dt} \, \xi_v(t)$$

This can be used to calculate the average heat flux

$$\langle \frac{dQ}{dt} \rangle = \frac{\eta}{m}(k_B T_C - m\langle v^2 \rangle)$$

The change in entropy $dS = \frac{dQ}{T}$ becomes

$$dS = -\eta v^2 dt + v\sqrt{2k_B T_C \, \eta \, dt} \, \xi_v(t)$$

From the first law of thermodynamics

$$dH = d'Q + d'W$$

The work done on the particle by the circuit is

$$dW = \left(-\frac{1}{R}\left(\frac{dH}{dq}\right)^2 + \frac{k_B T_R}{R}\left(\frac{d^2 H}{dq^2}\right) \right) dt + \sqrt{\frac{2k_B T_R}{R}} \frac{dH}{dq} \xi_q(t) = \langle \frac{k_B T_R}{RC(x)} \rangle - \langle \frac{V_R^2}{R} \rangle$$

The average power now becomes

$$\frac{dW}{dt} = \langle \frac{k_B T_R}{RC(x)} \rangle - \langle \frac{V_R^2}{R} \rangle$$

Power is separated into term 1 $\langle\frac{k_B T_R}{RC(x)}\rangle$ and term 2 $\langle\frac{V_R{}^2}{R}\rangle$ which represent the power contribution of the capacitor and the power dissipation of the resistor respectively.

7.3   When $T_R = T_C$

For the system with all the components at the same temperature, simulations were done when $k_B T_C = k_B T_R = .5$, $V = 1$, $C_0 = 1$, $R = 10$, $\eta = 1$, $m = 1$ and $d = 5$ and averaged 20 runs with a time step $dt = 0.0002$ for a total of one million timesteps to ensure numerical convergence. Long run time ensures that thermal equilibrium is reached, and that time averages equal the ensemble averages.

When $T_R = T_C$, the membrane fluctuates between the two equilibrium positions and spends equal time in both as shown in Fig 7.2a. A current is produced in the circuit as the capacitor fluctuates, causing the charge to vary according to $I = \frac{\Delta C(t)}{dt} V = \frac{\Delta Q(t)}{dt}$. The charge stored in the capacitor is shown in Fig 7.2b. Charge average is around -1, or $-C_0 V$, which is in agreement with Kirchhoff's loop equation.
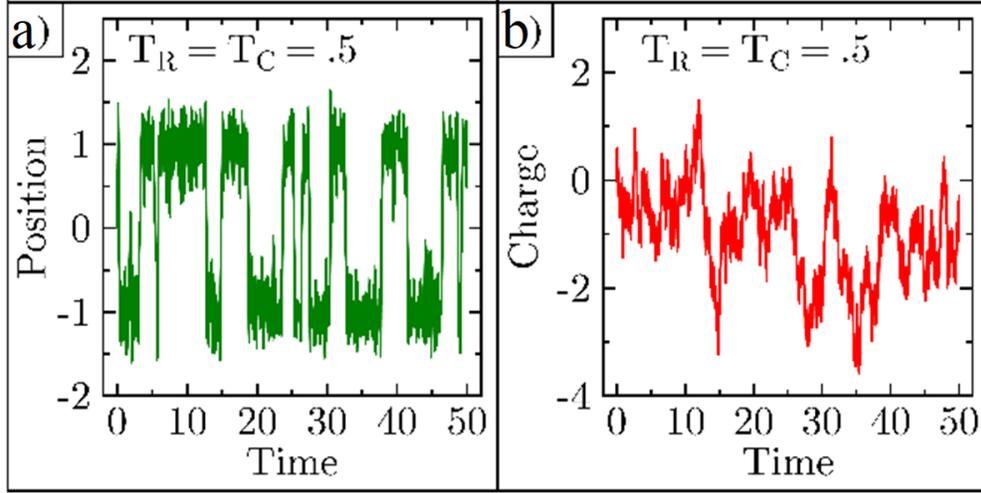
Figure 7.2: Ito-Langevin equation simulation when $T_R = T_C$. (a) Height of graphene ripple as a function of time (b) charge on the capacitor over time.

     With long time correlations, the system approaches equilibrium, meaning the average total power is zero. This indicates that the power generated by the capacitor is equal to the power dissipated by the resistor as illustrated in Fig 7.3 (a-b). Therefore, when all the components are at the same temperature, and in thermodynamic equilibrium, the capacitor and resistor perform equal work on each other.

$$\frac{dW}{dt} = 0 = \langle \frac{k_B T_R}{RC(x)} \rangle - \langle \frac{V_R^2}{R} \rangle$$

$$\left\langle \frac{T}{RC(x)} \right\rangle_{Equil} = \left\langle \frac{V_R^2}{R} \right\rangle_{Equil}$$
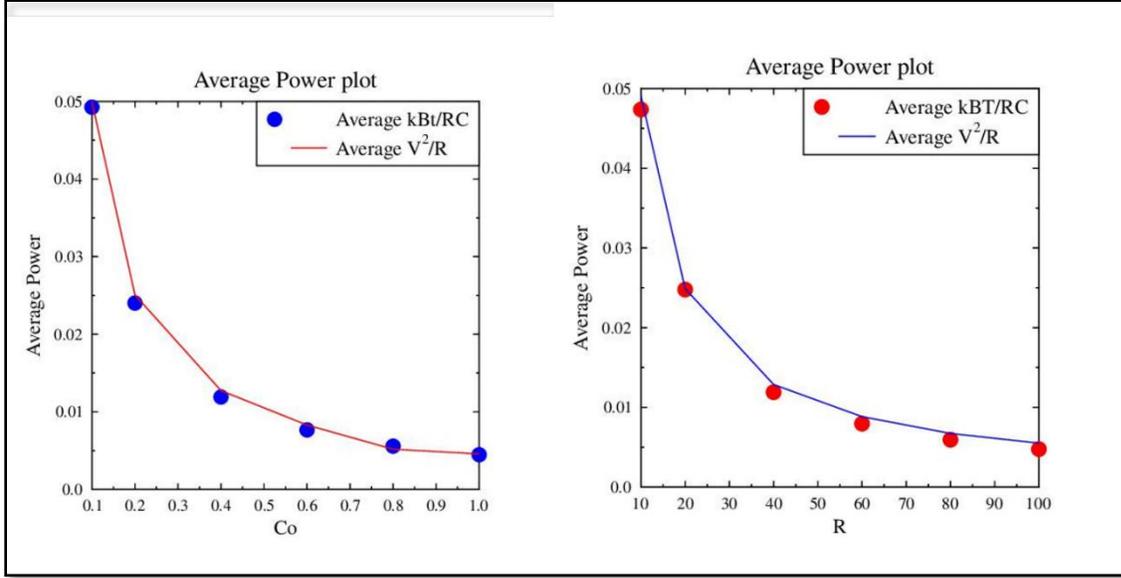
Figure 7.3: Power dissipation at $T_C = T_R$. (A) Varying Co. (b) Varying R

7.4 Varying the Capacitor Temperature T_C

Here, we vary T_C while keeping T_R constant. The simulation parameters for this were set as $V = 1, C_0 = 2, R = .5, k_B T_R = .5, \eta = .04$ and d = 5. We ran these simulations with a time step dt = .0001 for 10 million total time steps averaging 100 runs. The energy $k_B T_C$ was varied from 5 to 50 and the simulation results are shown in Fig 7.4.

As T_C increases the time-averaged heat flow to the resistor steadily increases, as shown in Fig 7.4a. The average heat flux and total average power increase equally in magnitude and with opposite signs with temperature, in agreement with the first law of thermodynamics and the average energy rate remains near zero, as shown in Fig 7.4(b). Average power is the difference between power terms 1 and 2. The average energy of the system increases as T_C increases as shown in Fig 7.4(c). The power contribution of the capacitor term 1 $\langle \frac{k_B T_R}{RC(x)} \rangle$ and the power dissipation of the resistor term 2 $\langle \frac{V_R{}^2}{R} \rangle$ are shown in Fig 7.2(d).

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The contribution of power term 1 is temperature invariant while power term 2 increases with temperature, becoming linear at high temperatures. At high temperatures, the resistor dissipates much more power than the capacitor contributes, consistent with a comparatively large heat flow from the capacitor to the resistor.
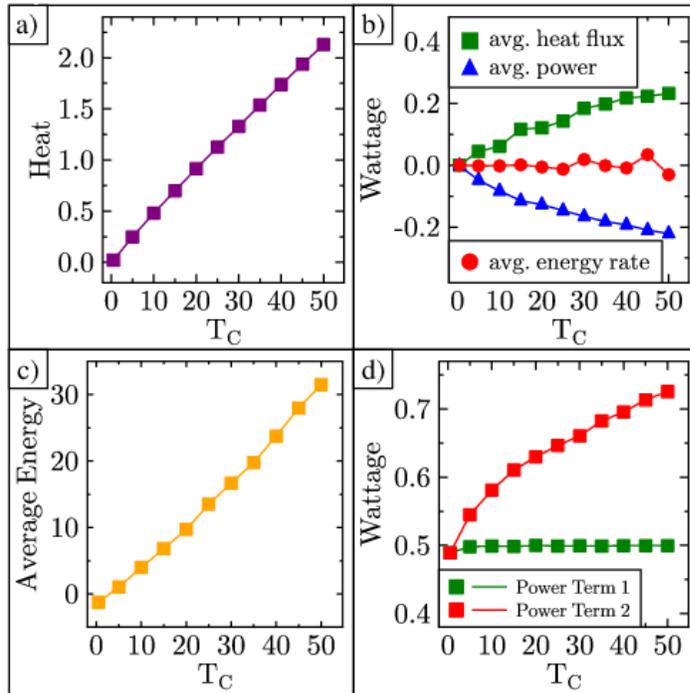
Figure 7.4: Numerical simulations for varying T_C. (a) Ensemble average heat. (b) Ensemble average heat flux, power, and energy rate. (c) Ensemble average energy over the entire time. (d) Ensemble average of power terms 1 and 2.

We also tracked the position of the capacitor and the accumulation of charge as shown in Fig 7.5(a-d). There are long periods of coherent motion, with few directional changes (curvature inversion occurrences) as T_C increases. This is consistent with the fact that crossing rates of double-well systems increase with temperature (Kramer's rate)[163].
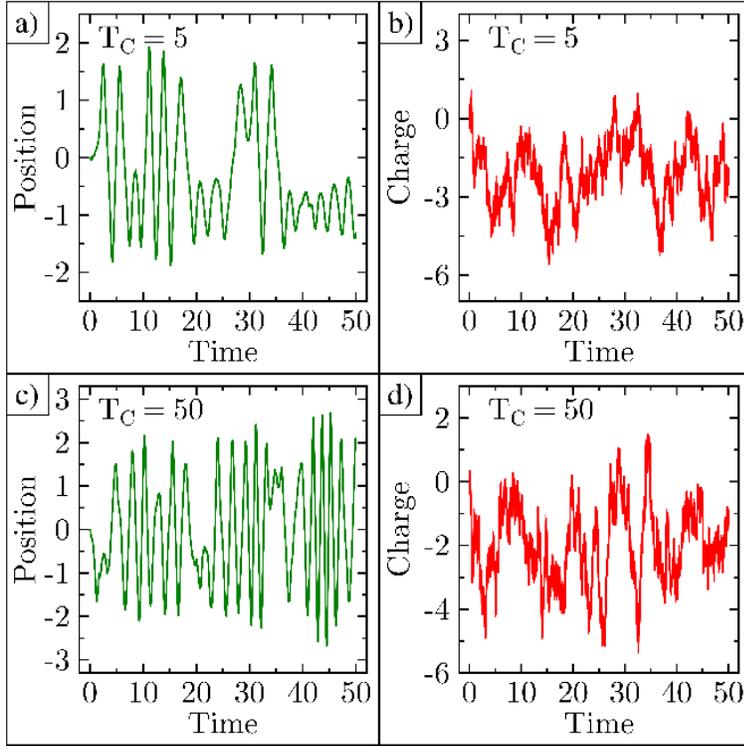
Figure 7.5: Dynamics of position and charge. (a-b) Position and charge plots for T_C=5. (c-d) Position and charge plots for T_C=50

7.5 Varying resistor temperature T_R

We vary T_R while keeping T_C constant. The parameters for this set of simulations were $V = 1$, $C_0 = 1$, $R = 10$, $\eta = 1$, and $d = 5$ and $k_B T_C = .5$. We ran these simulations with a time step $dt = .001$ for 10 million total time steps averaging 100 runs. $k_B T_R$ was varied from 5 to 50 and the resulting data is shown in Fig 7.4.

As T_R increases, an increasing amount of heat flows into the capacitor, as shown in Fig 7.6(a). Unlike in the previous section, the magnitude of heat flow increases at an increasing rate with temperature. Fig 7.6(b) shows the heat flux, power and energy rate in the capacitor. The signs of the power and heat terms are the opposite of what they were in the previous section of varying T_C,

consistent with the reversal of the temperature gradient. The average energy of the system increases steeply with T_R, as shown in Fig 7.6(c).

The two power terms increase steeply as T_R increases as shown in Fig 7.6(d). Though power term 1 dominates, power term 2 is only slightly smaller. The capacitor is contributing more power than the resistor is dissipating, consistent with heat flow from the resistor to the capacitor. The fact that the system's heat flux is small compared to either of the two power terms indicates a high level of efficiency. When the T_R is 100 times the T_C, the total power generated by the capacitor is seven times higher than when the T_C is 100 times the T_R. The data clearly indicate that increasing T_R is a more efficient power generation strategy than increasing T_C. This implies that varying T_R has a greater effect on the total energy of the system than varying T_C.
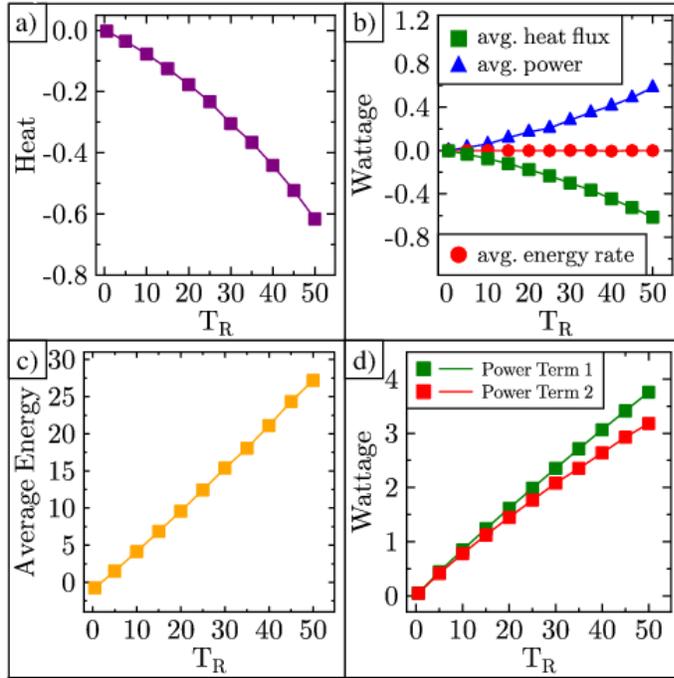
Figure 7.6: Numerical simulations for varying T_R. (a) Ensemble average heat. (b) Ensemble average heat flux, power, and energy rate. (c) Ensemble average energy. (d) Ensemble average power 1 and 2 terms. (e) Ensemble variance of velocity. (f) Ensemble variance of charge.

To understand why T_R has a greater effect on the system, position and charge was plotted for $k_B T_R = 5$ and $k_B T_R = 50$, as shown in Fig 7.7. At $k_B T_R = 5$ the ripple is trapped more in one minimum but frequently shift between the two equilibria as shown in Fig 7.7a. The average charge on the capacitor is 5 as shown in Fig 7.7b. At $k_B T_R = 50$ the capacitor plates remain almost entirely on one minimum with fewer transitions to the other minima as shown in Fig 7.7c. The average charge on the plates is 50, which is a substantial increase from the $T_R = 5$ case as shown in Fig 7.7d.
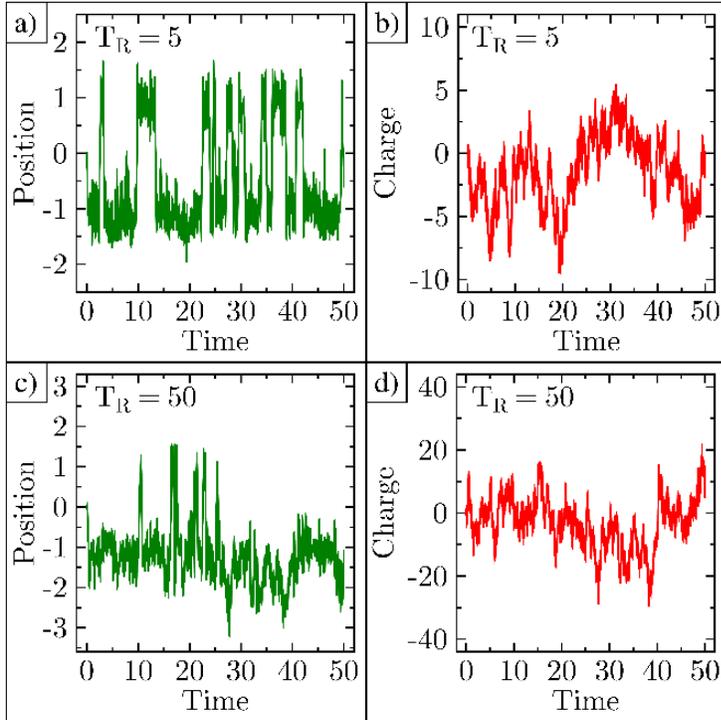
Figure 7.7: Dynamics of position and charge. (a-b) Position and charge plots for T_R=5. (c-d) Position and charge plots for T_R=50

From these simulation results of spontaneously varying temperatures in capacitor-resistor systems, power dissipation by the resistor increases with temperature regardless of which temperature is being varied. However, power generation by the capacitor is more efficient only increases when the temperature is higher in the resistor. This implies that heat flow from the resistor provides the capacitor with the necessary energy to increase current output.

Therefore, if one plans to use a device modeled after the simulated system to harvest energy near a waste heat source, it is advantageous to create a layout with the resistor near the heat source and the capacitor far away, or to insulate the capacitor from the heat source.

CHAPTER 8

8   Conclusions

Graphene holds   great potential for applications in the semiconductor industry, mechanical applications, and for incorporation in Integrated circuits. In particular, the highly flexible and electrically conductive freestanding graphene membranes have great potential for applications in vibration driven energy harvesting. In this dissertation, I have described the design and fabrication of an array of graphene based variable capacitor on both 100 mm silicon wafer and a bare die purchased from TSMC. I have also shown simulation results for graphene potential applications in a circuit and simulation results when the circuit components are at the same or different temperatures.

Photolithography and E-beam lithography are used to pattern the wafer. Trenches and tip feature are created by isotropic wet etching of SiO_2 with HF for 5 minutes at room temperature. Creation of conductive pathways and contact pads is done by patterned deposition of gold. We perform large area graphene transfer to the tip regions and use critical point dryer to dry our substrate. This ensures that graphene is left freestanding over the tip feature. This graphene-tip feature junction forms a variable capacitor where graphene is the movable plate. Lastly, capacitance and resistance measurements are taken from these devices to confirm that graphene is freestanding over the tip structure.

This study demonstrates the feasibility of performing graphene energy harvesting on a chip using graphene-tip feature and furthers the graphene energy harvesting research.

9   Bibliography

9.1   List conference presentations (Talks and posters)

1. APS March meeting, 2020 – A new source of thermal power.

2. APS March meeting, 2019 – Battery alternative: Harvesting energy from vibrations.

3. APS March meeting, 2018 – Alternative Power Source with Nanotechnology.

4. Physical Electronics Conference, 2017 - Alternative energy source with Nanotechnology.

9.2   List of referred journal publications

1. **Millicent N. Gikunda**, Ferdinand Harerimana, James M. Mangum, Sumaya Rahman, Joshua P. Thompson, C. Thomas Harris, Hugh O. H. Churchill, and Paul M. Thibado. Array of graphene variable capacitors on 100 mm silicon wafers for vibration energy harvesting applications.

2. Harerimana F, Peng H, Otobo M, Luo F, **Gikunda MN**, Mangum JM, et al. Efficient circuit design for low power energy harvesting. AIP advances. 2020;10(10):105006,105006-6.

3. Mangum JM, Harerimana F, **Gikunda MN**, Thibado PM. Mechanisms of Spontaneous Curvature Inversion in Compressed Graphene Ripples for Energy Harvesting Applications via Molecular Dynamics Simulations. Membranes. 2021;11(7):516.

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