Analysis and Optimization of the Two-Phase Series Capacitor Buck DC-DC Converter

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Analysis and Optimization of the Two-Phase Series Capacitor Buck DC-DC Converter

A dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Engineering, with a concentration in Electrical Engineering

by

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Abstract

Current sharing schemes for conventional multi-phase converters are based on sensing each phase current to deliver the current information to their controllers. In conventional buck converters, this fact may require a preset current sharing ratio at the expense of efficiency, which eventually requires a larger sensing circuit to achieve the sensing accuracy of each phase. Introducing the concept of automatic current sharing is one of the solutions to tackle this issue. Automatic current sharing (Current Sharing Mechanism CSM) is an advanced way to distribute heat generation in multi-phase switching topologies at full load. A two-phase series capacitor buck converter (2-pscB) was introduced to power laptops as low-voltage and high-current Voltage Regulator Modules (VRMs) as well as non-isolated Point-of-Load (PoL) converters. The current sharing concept is the main feature of this 2-pscB topology, where series capacitor voltage is used to achieve current sharing without the need for a phase current sensing circuit or complicated control loop. In this work, a complete state-space average model for the series capacitance buck switching regulators is linearized to develop a robust controller satisfying the stability and converter performance specifications. The presented averaging model includes the simplest model of the regulator’s parameters and only the main parasitic components. Both, an improved derivation of the main design parameters and a novel design methodology of MOSFETs isolated gate driver circuit are proposed and verified. Different high voltage input 2-pscB power density dc-dc converters are successfully investigated to examine the capability of current sharing at a higher voltage level and its impact on efficiency. Another novel approach of eGaN gate driver circuitry is designed with a Current-Mode Controller CMC using one current path to minimize propagation delays and reduce phases parasitic components, which helps enhance overall performance.
110V/12V/6A experimental prototype converter of Si MOSFETs was designed, its current sharing characteristics were experimentally tested and verified. Since eGaN technologies have attracted great attention in power electronics applications due to their capabilities and efficient energy conversion, another design, and analysis of a sensor-less eGaN-based 48V/5V 2-pscB buck switching converters were verified, and their current sharing characteristics were predicted by the state-space modeling technique. A theoretical comparison is conducted between conventional buck converter and 2-pscB. The results show the following characteristics of 2-pscB topology: a small inductor current ripple, low switching loss, inherited current sharing mechanism, duty cycle flexibility, and filter component size reduction. In a word, new modeling methods of various 2-pscB control schemes are proposed and broadly studied. This dissertation simulates most of these methods to provide the designers with a better comprehensive view of the 2-pscB converter topology.
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In the memory of my mother

Mrs. Zaina Saaid

Always in my mind, forever in my heart
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1. Chapter 1: Motivation and Objectives.

1.1 Research Motivation

Due to an increase in the demand for broad applicability domains, researchers are especially focusing on finding highly efficient converter topologies for various power conversion rates, which include computers, telecommunication systems, appliances, industrial electronic equipment, Electric Vehicles (EV), Uninterruptible Power Supplies (UPS), and much more. Multiphase topologies increasingly become the best choice that accomplishes the conversion demand objectives and quickly gain interest due to many benefits they provide, such as enabling a higher power density and efficiency. Multiphase converters offer excellent performance advantages in transient response and efficiency. These advantages can only be fully achieved if we confirm the load current sharing between all the phases of the topology design. Fulfilling this goal while at the same time guaranteeing another very significant parameter - namely, equalization of the case temperature of the switching eGaN FETs / MOSFETs. However, current sharing and designing control mechanisms are the main problematic issues since the default design goal is for all phases to equally share the current cost-effectively. Multiplying control loops increase the complexity of the circuit to maintain proper current sharing. The main motivation for this research is to shed light on a new multiphase topology that can address these design issues and have a more effective solution for multiphase design converters. This study is the first comprehensive study of two-phase series capacitor buck converters. That is why, amongst all variety of converters, this thesis is mainly concentrated on providing the necessary information for designing this topology, which has some interesting properties and applications. Tackling the control problem in detail for every type of controller is partially the scope of a thesis.
1.2 Objectives

The main objectives of this dissertation are categorized into four main parts, which are as follows:

a. Develop a new approach based on previous studies conducted on multi-phase topologies starting from state-space modeling and basic transfer functions that describe these topologies to help design a robust control system.

b. Study and formulate the topology’s important parameters and conduct simulation to prove the current sharing mechanism.

c. Explore the differences between conventional buck and 2-pscB converters in terms of efficiency, size, losses, and heat distribution and find solutions that help in enhancing the performance even further by using a different approach of gate driving of MOSFETs and enhancement mode transistors eGaN FET devices.

d. Design and fabricate 2-pscB converters with a high voltage level (48V-110V) and examine its performance and efficiency.

1.3 Dissertation Outline

The organization of this dissertation is as follows: Chapter 2 provides a brief overview of the background and introduction to the two-phase series capacitor buck converter. This chapter provides information about the advantages and disadvantages of this topology. Based on the literature review, Chapter 3 introduces the topology interleaving and state-space averaging models of the series-capacitor buck switching regulators. This chapter aims to explain in detail the modeling steps, derivation of characteristic formula, and derivation of transfer functions. It also presents some recommendations and suggestions for component selection to avoid inappropriate performance. From this, set goals for what we need to learn from the proposed experiments.
Chapter 4 focuses on the 2-pscB ac small-signal variation model and discusses possible VMC, CMC control schemes of different approaches. Also, the proposed $I^2$ average current mode controller, and constant-frequency average current mode controller are covered in addition to the gate driving design for Si MOSFETs / eGaN FET switches. Chapter 5 introduces two-phase series capacitor step-down topology parameter analysis and case study analysis supported by calculations, including comparing the parameter derivation of conventional buck converters and obtaining information on designing inductance, capacitance, and MOSFET essential parameters. These parameters are the input voltage range, the regulated output voltage, the maximum output current, and the converters switching frequency. This chapter covers the amplitude and phase spectrum of the two-phase node switching voltage under the condition of full current sharing. Chapter 6 focuses on a novel isolated gate driving circuit design for both Si MOSFETs/eGaN FETs approach of 48V/5V. Experimental work has been conducted to define different aspects of losses, efficiency, and analysis. A 110V/12V isolated evaluation model with detailed data and schematics is addressed as theory and equations, applicable estimations of changes and differences with 48 V and 110 V models are included. Finally, the Experimental prototype circuits and results are fully covered, and their performance is successfully tested. At the end of this chapter, EMI emissions, EMI of DC input circuit design, and frequency interference measurements are covered. This chapter includes a summarized discussion, and a comparison between different lab measurements of the models' results and other aspects like loss modeling, EMI design, suggestions, and further work. This comprehensive analysis could lead to a better understanding of the “democratic” current sharing concept of this topology. Chapter 7 summarizes the research content of the thesis and highlights the main contributions of this article. Suggestions for future work are also listed.
1.4 References


1.4 https://www.eia.gov/energyexplained/?page=renewable_home


2.1 Background

A Switched-Mode Power Converter (SMPC) is one of the most common technologies among power conversion [2.1]. Voltage input is converted to another level by releasing the temporarily storing energy to the output at different voltage levels. These converters can switch at high frequency in a very efficient way when controlling the timing of the electronic switches in “on-time” and “off-time”. In this project, a much greater emphasis is committed to achieving high-power efficiency in low-power level electronic technology. Owing to its wide range of applicability, DC-DC converters have become more popular and recently alert the interest in the current market. These unidirectional devices are designed to transfer power from the input to the output in low-power circuits, as Personal Computers (PCs), cellular phones, and electric vehicles (EVs). This fact may rely on other sub-circuits that require an own voltage level from an external power supply like batteries with different power storage.

DC-DC conversion is a variable-structure system where its topologies are dependent on a periodical switching function. In many cases, the signal controlling the switches is a pulse-width modulated signal thus, such topologies are called Pulse-Width Modulation converters (PWM). Two main characteristics that can be derived from one of these topologies are its duty cycle and its switching frequency. The definition of duty cycle is the ratio between the on-time of the cycle and the cycle itself, and this frequency will be expressed as the fundamental switching frequency \( f_{sw} \). For many designs, the signal frequency is fixed, which gives the duty cycle a certain degree of freedom as one variable to actuate the input and control the converter. In order to drive the switching device, it is necessary to reach the driving stage, where the PWM signal can generate
the voltage level required by the gate driver with a stable deadtime level. The common task for
design engineers is to design ideal, effective, and robust control structures by deriving Linear Time
Invariant (LTI) Transfer Functions (TFs), which can translate the relationship between the
converter output $V_o$ to actuating inputs. This part includes studying the common disturbance
inputs, parasites, and load variation.

![Diagram of power distribution system](image)

Fig.2.1. Traditional intermediate bus of electrical power distribution.

Electrical power distribution systems are widely used in networking, communications, and
high-end server applications. These applications mainly use the 48V bus voltage supplied from the
telecom industry. The 48V bus feeds several isolated PoL converters to power the end loads, with
isolation being required for safety. Besides modern microprocessor Voltage Regulation Modules
(VRM), multi-phase buck converters are widely used in VRMs for their simplicity. As seen in
Fig.2.1, the VRM can be placed in the motherboard to feed the CPU. In many cases, the paralleling
module approach for point-of-load converters is successfully used in these power systems [2.2].
Traditional intermediate bus power distribution architecture, as shown in Fig.2.1, uses AC/DC
front-end converters consisting of power factor correction and isolation means to deliver the 48 V
bus voltage. From the 48 V bus voltage, several isolated DC/DC regulated PoL converters are used
to deliver the required voltage and power to individual loads. This architecture has become more complex, the number of loads has increased significantly, and the voltages and currents demanded have increased with different technologies installed to deal with increasing the cost, volume, and complexity of the system.

There are many attempts to simplify the design of these systems, one of them is introducing the concept of intermediate bus architecture that was proposed mainly to reduce the number of complex isolated PoL converters required. The intermediate bus voltage that feeds from the 48 V bus usually ranges between 8 V and 12 V, which leaves smaller, lower overall system cost, and more efficient regulated PoL converters as the final regulation to the loads. The multi-phase switching topologies are considered to make use of their benefits in terms of thermal management, reliability, and power density at different voltage levels. In this case, the paralleling power system becomes the main concern throughout the establishment of one converter to deliver a certain voltage level in parallel with other converters or within the same device. In practical usage, even a small variation between paralleled modules will lead to current imbalances. This change problem will get worse with uneven load distribution. Hence, the stress placed on the individual converter will be unmatched, with higher temperatures resulting in some converter units. However, the reliability of the whole system will be reduced, the main challenge in paralleling converter supplies is to make sure the whole system is predictable, uniform current sharing regardless of load levels and the number of power units is used.

Current sharing is essential to distribute the generated heat in multi-phase switching converters at full load. Current sharing implementation for multi-phase switching converter topologies is reported in [2.3-2.7]. There are many control methods to provide complete current sharing between
different switching phases. One of the most popular methods is the active current sharing method with Current-Mode Control (CMC) [2.8]. To achieve high reliability, these methods need complicated control circuits and include reliable sensors, which is not the case. Even little noise generated in the modulation process will be amplified, and the control speed response cannot be matched with other converter units.

This research will focus on one of the new methods to tackle this problem, where a series capacitor is added to achieve complete current sharing without complicated current sensing circuits.
or external control loop in a multiphase converter [2.9]. The two-phase series-capacitor buck converter (2-pscB) is a unique converter topology that essentially combines the benefits of a switch capacitor circuit as a DC source and a two-phase buck converter [2.10, 2.11]. Fig.2.2 shows the main proposed prototypes of GaN transistors and Si/SiC MOSFETs 2-pscB converters, which are designed and fabricated throughout the dissertation. Usually, these types of topologies are used as point-of-load voltage regulators rating less than 12 V input, and they become common for their capabilities of paralleling multiple buck converters, a relatively achievable control bandwidth (response speed), and high load current. Another main reason for using multiphase converters is because they help to ensure efficient operation and evenly distribute the thermal dissipation between phases due to power switching and conduction loss. Uneven load current sharing is also executable but is less common [2.12, 2.13]. These papers examine the automatic current sharing mechanism in a multiphase series capacitor buck converter. The sharing mechanism does not require phase current measurements or external control loops yet provides accurate load current.

Fig.2.3 Comparison between 2-pscB converter (above) and conventional buck (down).
sharing, and one phase feedback loop works as a master and could be used to control the rest of the phases as long as design requirements are applied [2.14]. This paper presents the first monolithically integrated two-phase series capacitor where increasing switching frequency can reduce the physical size of power converters for PoL voltage regulators to minimize the circuit space, especially the size of inductor elements. It is (Internal-FET) Regulators and targeted at 12 V input and 10 A output. A comparison between conventional buck and 2-pscB converter in terms of physical size is shown in Fig.2.3.

2.2 Power Semiconductor Devices

For many years, the power semiconductor market dominated by silicon-based devices (Si MOSFETs, IGBTs). Nowadays, new wide-bandgap technology like eGaN and SiC MOSFET compete for that silicon-based devices' domination in terms of speed and efficiency. Although eGaN and SiC MOSFETs devices are expensive technologies with various challenges, their existence again depends on the expected cost reductions [2.15]. For lower voltages, less than

![Fig.2.4. A possible future scenario of semiconductor market.](image-url)
600V, SiC MOSFETs and eGaN devices still share the market. For the future, the data and market speculations clearly show a significant increase in Wide BandGap devices (WBG) design and manufacturing therefore, traditional silicon-based devices sales will also increase in a growing market. Fig.2.4 is a view of the possible future market share in power switches according to operating frequency for power semiconductor devices. Interestingly, at 100V rating, the available eGaN devices are not better than traditional silicon-based devices for on-state resistance, and therefore the main advantage is their speed capabilities.

2.3 The 2-pscB Topology Advantages and Disadvantages

Some benefits of two-phase series capacitor buck converters are listed as follows:

1- Reducing switching voltage level (reducing $V_{DS}$ by half). This results in greater efficiency with lesser switching losses $E_{oss}$, and becomes suitable for high-frequency switching.

2- Reducing output voltage ripple and current ripple by the third.

3- Reducing the size of the filter inductor by almost a half.

4- The inductors act as current sources to softly charge and discharge the series capacitor in four-mode power stages (self-charging).

5- Flexible intervals time where intervals can (nearly) be reduced to two as a regular buck.

6- Automatic current balancing between phases can be achieved very easily when the two inductors have the same size, same storage energy, and the inductors’ current shapes are the same. In special cases, even if the inductors are not the same, e.g., manipulating the pulse intervals can achieve the current balancing by increasing one or more switching duty cycles.
7- The current sharing can be achieved without any phase current sensing element, which is a very critical issue for the distribution of heat, especially when the current demand is high.

8- Compared with the traditional buck converter with the same conversion ratio, the duty cycle is doubled to achieve a similar specification of a single 2-pscB, which makes the series capacitor step-down easier to control in high-frequency applications.

Generally, from the first benefit listed, the physical size of output filter elements becomes smaller at higher switching frequencies. Increasing the switching frequency can improve the dynamic response and output ripple. However, there is a practical limit to the switching frequency as conduction switching losses increase with frequency. The main benefit here is power management to obtain the highest performance of the regulator, automatic power management between phases is used, and the current is evenly distributed between the phases. If the current balance cannot be fully achieved, the advantages of input and output ripple cancellation will be interrupted, causing stability problems. With complete current sharing, better thermal performance and efficiency at higher loads are guaranteed, because all output load is not concentrated in one group of Si MOSFETs/eGaNs or in a single inductor, which may cause a sharp drop in efficiency instead of two or more phases sharing the thermal burden. The only exception is the first switch $Q_{11}$, which is the main path of the entire circuit current, as shown in Fig. 2.5. The conduction loss in $Q_{11}$ will dominate total losses, so special consideration is needed when choosing FETs with very low on-state resistance.

During the transient period, the multiphase controller maximizes the duty cycles of both phases to the limit of 25% of the period without overlapping between them and maintaining 25% of the
time between both duty cycles. All phase inductors that parallel to each other are reduced by several phases where a smaller equivalent inductance can charge the output capacitor faster than bigger ones. This issue also reduces the overshooting when the excess charge stored in the inductor of each phase partially discharges at phases turn-off state, and then the rest transfers to the output capacitor.

On the other hand, the first drawback of this topology is that it has a 50% duty cycle limit. This limitation means that the high-side switches $Q_{11}$ and $Q_{21}$ cannot be turned on at the same time, coupled with the fact that conventional buck gives the converter an inherent 2:1 step-down, therefore, the theoretical minimum input voltage rate is four times the output voltage. In another word, the minimum input voltage is going to be almost five times the output voltage when we take losses into account.

$$V_{in} \geq 4(V_o + E_{oss}) \quad (2.1)$$
Adding more phases and more powerful components means decreasing the overall gain, increasing the PCB area and cost to achieve the expected return. At the final stage, a balance between those factors such as thermal, current function, and the number of phases must be fulfilled.

This topology needs an additional control circuit that can limit the inrush current at the $Q_{1/2}$ caused by series capacitance and output capacitor charging period at the beginning of the transient time. This inrush current can cause damage to the first switch in the long run. For this topology, intervals can be different from each other to add more flexibility to the desired specifications in terms of the charging time and discharging of the capacity.
2.4 References


3.1 The 2-pscB Regulator States Equations

The main objective of this chapter is to derive the transfer functions governing the operation of the 2-pscB converter. Because of the switching properties of the power elements, the operation of this converter varies over time. Since this converter is non-linear and time-varying, it utilizes the switching function of the buck converter power device to achieve high efficiency. Due to the non-ideal characteristics of the switches and their conduction mode resistance, and because the voltage and current will not suddenly become zero during the switching time, this response brings a certain power loss to the system. In modeling, the load current is assumed to be unknown, as such assumed that this topology consists of non-ideal (resistor, inductor, and capacitor) and they have resistance in conduction conditions. The nonlinear regulator active switches-circuit elements have other non-ideal effects like a voltage drop of conduction mode of active switches, which is neglected due to the complexity of modeling. This state-space averaging model could be used to design a robust controller that can satisfy the stability and performance conditions of the converter. A small-signal model linearization of four switching intervals using a state-space average model is required. The switching capabilities of the buck power device are utilized to achieve the highest efficiency. However, the non-idealistic nature of switches with their conduction mode resistance generates some power losses due to the finite voltage and current during switching transitions. As such, a complete model includes all the system parameters, such as the turn-on resistance of the diode switch, the parasitic resistances of the inductor and capacitor, and the unidentified load current that can be delivered from the converter. The first step in modeling is to convert a complex circuit into a simplified circuit, in which circuit rules can be
established. In a switching regulator, the elements that store the energy in a circuit or system (such as capacitor voltage and inductor current) are of great significance. The linear and time-invariant system consists of four regions: the two on-regions of input source and series-capacitor energy storage source, and two off-regions. The on-time is denoted by $D_1T, D_3T$, and the off-time is denoted by $D_2T, (1-D_1-D_2-D_3)T$

Thus
\[
d_1T = D_1T \\
(d_2-d_1)T = D_2T \\
(d_3-d_2)T = D_3T \\
(1-d_3)T = (1-D_1-D_2-D_3)T.
\]

In which $T$ is the period of the steady-state output voltage. Fig 2.1. shows a two-phase series capacitor buck switching regulator. The four switches are turned on (off) by a pulse with a period of $T$, and its duty cycle is $d$ seconds. Therefore, we can represent the simple equivalent circuit of the system in four on and off modes. To look at the stages of operation of this converter in a steady state. During mode-I, the high-side switch of phase A, switch $Q_{11}$, is on, and the inductor current in inductor $L_1$ charges up the series capacitor a small amount. This topology has a duty cycle as follows.

\[
\frac{V_o}{V_{in}} = \frac{d_1(d_3-d_2)}{d_1+d_3-d_2} = \frac{D_1D_3}{D_1+D_3}
\]

(3.2)

Where $d_1, d_2, d_3$ represent intervals for capacitor series buck modes

When these intervals are equal $D_1= D_2 = D_3 = D= t_{on}/T$. Hence,

\[
\frac{V_o}{V_{in}} = \frac{D}{2} = \frac{t_{on}}{2T}
\]

(3.3)

At current sharing balance between the two phases, switching voltage must be the same where,

\[
d_1(V_{in} - V_{cs}) = V_{cs}(d_3 - d_2)
\]

(3.4)
or
\[
\frac{V_{CS}}{V_{in}} = \frac{d_1}{d_1 + d_3 - d_2} = \frac{D_1}{D_1 + D_3}
\]  
(3.5)

From equations (3.2), (3.5) at steady state condition we conclude that.
\[
\frac{V_o}{V_{CS}} = D_3
\]  
(3.6)

where,
\[
\frac{V_o}{V_{in}} = \frac{V_o}{V_{CS}} \frac{V_{CS}}{V_{in}}
\]

Consideration to \(i_L, v_{CS}\) and \(v_{Co}\) as our state variables of the continues time LTI system consist of state equation and output equation. Writing the KVL for the loops of first interval of Fig 3.1 we will have:

\[\text{Fig 3.1} \quad \text{Four intervals schematic a) 2-pscB b) first stage interval of } D_1 T, \text{ c) second and fourth interval of } D_2 T \text{ and } (1-d_3) T. \text{ d) third interval of } D_3 T.\]
\[
\begin{cases}
\dot{x} = A_i x + B_i u \\
y = C_i x + F_i u
\end{cases}
\tag{3.7}
\]

Where \(i\) denote the corresponding operation mode. Consider this converter operating in the continuous conduction mode, where the converter circuit contains independent states of \(x(t)\), and the converter is driven by input vectors \(u(t)\) of independent sources and output vector \(y(t)\).

\[
x = [I_{L1} \ I_{L2} \ V_{Co} \ V_{Cs}]', \quad U = [V_{in}] , \quad y = [V_o \ V_{rc} \ I_{in}]'
\tag{3.8}
\]

For this description of circuit operation, the following assumptions are made; leakage inductance for both phases are neglected. Components are considered ideal except otherwise indicated, and the converter operates in steady state.

For mode I, according to Fig.3.1, a set of two equations must be written using KVL and KCL. Representing \((i_{L1}, i_{L2})\), The main difference between this model and the lossless model is that the output voltage is not equal to the capacitor voltage. The two equations are having three unknowns. Thus, it is necessary to find the third equation to solve the system of equations. To see the effect that every state variable is having on the output voltage, the last equation can be found using the superposition principle.

\[
v_o(t) = \frac{R}{R+r_c}[i_{L1}(t) + i_{L2}(t)] + \frac{R}{R+r_c}v_{co}(t)
\tag{3.9}
\]

The first term represents current divider at short circuit capacitive part where the second term is voltage divider of open circuit inductance.

Therefore,

\[
C_o \frac{dv_c(t)}{dt} = \frac{R}{R+r_c}[i_{L1}(t) + i_{L2}(t)] - \frac{1}{R+r_c}v_{co}(t)
\tag{3.10}
\]

**Mode I \((0 < t < d_1T)\)**

Hence, \(I_{in} = I_{L1}\) in mode I
To obtain system state-transition matrixes during the on time of switch $Q_{II}$, $A_I$, $B_I$, $C_I$ and $F_I$ are shown in eq (3.11):

$$A_I = \begin{bmatrix}
-k_1 & -Rr_c & -R & -1 \\
L_1(R+rc) & L_1(R+rc) & L_1(R+rc) & L_1 \\
-Rr_c & -k_2 & -R & 0 \\
L_2(R+rc) & L_2(R+rc) & L_2(R+rc) & 0 \\
-R & -1 & -R & 0 \\
Co(R+rc) & Co(R+rc) & Co(R+rc) & 0 \\
\frac{1}{Cs} & 0 & 0 & 0 \\
\end{bmatrix}$$

$$B_I = \begin{bmatrix}
\frac{1}{L_1} \\
L_1 \\
0 \\
0 \\
0 \\
\end{bmatrix}$$

$$C_I = \begin{bmatrix}
Rr_c & Rr_c & R & 0 \\
R+rc & R+rc & R+rc & 0 \\
Rr_c & Rr_c & Rr_c & 0 \\
R+r_c & R+r_c & R+r_c & 0 \\
1 & 0 & 0 & 0 \\
\end{bmatrix}$$

$$F_I = 0$$

(3.11)

Where

$$k_1 = (Rr_{on1} + r_c r_{on1} + R r_{L1} + r_{L1} r_c + R r_{CS} + r_c r_{CS} + R r_C)$$

$$k_2 = (-R r_{on4} - r_c r_{on4} + r_{L2} R + r_{L2} r_c + R r_C)$$

**Mode II** ($d_1 T < t < d_2 T$)

Also, for off-time at the second interval or $d_2 T$ time the circuit elements are connected differently and reduced to another linear circuit, the KVL equations from Fig.3.1 can be represented as, $A_2$, $B_2$, $C_2$ and $F_2$ as shown in eq (3.12):
where

\[ k_3 = (-R r_{on2} - r_C r_{on2} + R r_{L1} + r_{L1} r_C + R r_C) \]

\[ k_4 = k_2 \]

**Mode III \((d_2 T < t < d_3 T)\)**

Writing the KVL for the loops of third on-time interval of Fig.3.1 we will have:

\[
A_3 = \begin{bmatrix}
-k_3 & -R r_C & -R \\
L_1(R+rc) & L_1(R+rc) & L_1(R+rc) \\
-R & -k_4 & -R \\
L_2(R+rc) & L_2(R+rc) & L_2(R+rc) \\
R & R & R \\
\frac{1}{Co(R+rc)} & \frac{1}{Co(R+rc)} & \frac{1}{Co(R+rc)} \\
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & 0 \\
0 & 0 & 0 \\
\end{bmatrix}, \quad F_3 = 0
\]

\[ (3.13) \]
where
\[ k_5 = k_3 \]
\[ k_6 = k_7 = (R r_{on2} + r_c r_{on2} - R r_C) \]
\[ k_8 = R r_{on2} + r_c r_{on2} - R r_{L2} - r_{L2} r_c - r_c r_{on3} - R r_{on3} + R r_{Cs} + r_c r_{Cs} - R r_C \]
Hence, \( I_{in} = 0 \) in mode III.

**Mode IV \( (d_3 T < t < T) \)**

For the fourth off-time interval, which is similar to the second interval.

\[ A_4 = A_2 , \ B_4 = B_2 , \ C_4 = C_2 , \ F_4 = F_2 \]  \hspace{1cm} (3.14)

The set of state equations (3.11) to (3.14) shows the state of the series capacitance buck switching regulator in the on and off time of the switches. These states may differ, the averaging is the state equation of equilibrium and ac small-signal model where natural frequencies of the converter and a small variation at input signal are still smaller than the switching frequency. These four sets of equations can be combined as follows:

\[
\dot{X} = A_t X + B_t U = 0 \\
Y = C_t X + F_t U
\]  \hspace{1cm} (3.15)

\( X, U, \) and \( Y \) are equilibrium quantities, input and output vectors of the converter where \( A_t \) is total system matrix, \( B_t \) is the total input matrix, \( C_t \) is the total output matrix and \( F_t \) is the total transmission matrix.

For \( n \) intervals

\[
A_t = A_1 D_1 + A_2 D_2 + A_3 D_3 + \cdots + A_{n-1} D_{n-1} + A_n (1 - D_1 - D_2 - D_3 - \cdots - D_{n-1}) \]  \hspace{1cm} (3.16)

or

\[
A_t = D_1 (A_1 - A_n) + D_2 (A_2 - A_n) + D_3 (A_3 - A_n) + \cdots + D_{n-1} (A_{n-1} - A_n) + A_n \]  \hspace{1cm} (3.17)
\[ \begin{align*}
A_t &= A_1 D_1 + A_2 D_2 + A_3 D_3 + A_4 (1 - D_1 - D_2 - D_3) \\
B_t &= B_1 D_1 + B_2 D_2 + B_3 D_3 + B_4 (1 - D_1 - D_2 - D_3) \\
C_t &= C_1 D_1 + C_2 D_2 + C_3 D_3 + C_4 (1 - D_1 - D_2 - D_3) \\
F_t &= F_1 D_1 + F_2 D_2 + F_3 D_3 + F_4 (1 - D_1 - D_2 - D_3)
\end{align*} \] (3.18)

By substitution and re-write equations we can obtain coefficients of \( A_t \) to \( F_t \)

\[ \begin{align*}
A_t &= D_1(A_1 - A_4) + D_2(A_2 - A_4) + D_3(A_3 - A_4) + A_4 \\
B_t &= D_1(B_1 - B_4) + D_2(B_2 - B_4) + D_3(B_3 - B_4) + B_4 \\
C_t &= D_1(C_1 - C_4) + D_2(C_2 - C_4) + D_3(C_3 - C_4) + C_4 \\
F_t &= D_1(F_1 - F_4) + D_2(F_2 - F_4) + D_3(F_3 - F_4) + F_4
\end{align*} \] (3.19)

Then, we can obtain the system steady state values in equilibrium points \( X = [I_{L1} I_{L2} V_{co} V_{cs}'] \) and the DC output voltage \( (V_O) \).

\[ X = -A_t^{-1}B_t U = -A_t^{-1} B_t \begin{bmatrix} V_{in} \end{bmatrix} = V_{in} \begin{bmatrix}
\frac{D_1 D_2^2}{\psi} \\
\frac{D_2^2 D_3}{\psi} \\
\frac{D_1 R (D_2^2 + D_1 D_3)}{\psi} \\
\frac{D_3 (\chi)}{\psi}
\end{bmatrix} \] (3.20)

\[ \chi = D_1(R + r_{l2} - r_{on4}) + D_3 R + D_1 D_3 (r_{cs} - r_{on2} + r_{on3} + r_{on4}) - D_3^2 r_{on2} \]

\[ \psi = D_1^2 (R + r_{l2} - r_{on4} + D_3 (r_{cs} - r_{on2} + r_{on3} + r_{on4})) + D_3^2 (R + r_{l1} - r_{on2} + D_1 r_{on1} - D_1 r_{on2}) + 2 D_1 D_3 R \]

\( I_L \) is representing the total average two-phase inductor current \( I_L = I_{L1} + I_{L2} \). If parasitic components of switches are equals, thus

\[ r_{on1} = r_{on2} = r_{on3} = r_{on4} = r_{on} \quad \text{and} \quad r_{l2} = r_{l1} = r_L \]

\[ I_L = \frac{V_{in} (D_1 D_2^2 + D_2^2 D_3)}{D_2^2 (R + r_L - r_{on} + D_3 (r_{cs} + r_{on})) + D_3^2 (R + r_L - r_{on}) + 2 D_1 D_3 R} \] (3.21)
\[ V_{CO} = \frac{V_{in} D_1 R(D_3^2 + D_1 D_3)}{D_1^2 (R + r_L - r_{on} + D_3 (r_{CS} + r_{on})) + D_3^2 (R + r_L - r_{on}) + 2 D_1 D_3 R} \]  
\[ (3.22) \]

\[ V_{CS} = \frac{V_{in} D_1 (D_1 (R + r_L - r_{on}) + D_3 R + D_1 D_3 (r_{CS} + r_{on}) - D_3^2 r_{on})}{D_3^2 (R + r_L - r_{on} + D_3 (r_{CS} + r_{on})) + D_1^2 (R + r_L - r_{on}) + 2 D_1 D_3 R} \]  
\[ (3.23) \]

For special case when interval duty cycle \( D_1 = D_3 = D \), \( r_{on} = 0 \), \( r_{CS} = 0 \), \( r_L = 0 \), or neglected

\[ I_L = \frac{V_{in} D}{2R} = \frac{V_{sw} D}{R} \]  
\[ (3.24) \]

\[ V_{CO} = \frac{V_{in} D}{2} = V_{sw} D \]  
\[ (3.25) \]

\[ V_{CS} = \frac{V_{in}}{2} \]  
\[ (3.26) \]

For output voltage at \( r_C = 0 \) and the same duty cycle value, voltage is the same as the ideal output capacitor voltage

\[ V_o = -C_{t(rw1)} A_t^{-1} B_t U + F_t U \]
\[ = \frac{V_{in} D_1 R(D_3^2 + D_1 D_3)}{\psi} \]
\[ = V_{sw} D \]  
\[ (3.27) \]

At steady state voltage equilibrium condition between the two phases

\[ V_{sw1} D = V_{sw2} D \]

And output voltage will be the average of the two-phase switch voltages.

\[ V_{sw} = \frac{V_{sw1} + V_{sw2}}{2} \]  
\[ (3.28) \]

\[ V_o = \frac{(V_{in} - V_{CS}) D_1 + V_{CS} D_3}{2} \]  
\[ (3.29) \]

\[ V_{rc} = -C_{t(rw2)} A_t^{-1} B_t U \]  
\[ (3.30) \]

\[ I_{in} = -C_{t(rw3)} A_t^{-1} B_t U \]  
\[ (3.31) \]
\[
\begin{align*}
\frac{V_{in}}{D_1} &= \frac{V_{in} D_1}{(R+r_L-r_{on}+D_3(r_C+r_{on}))+(R+r_L-r_{on})+2R} \\
(3.32)
\end{align*}
\]

which is equal to \( I_{L1} \) at Mode I, hence \( I_{in} \) at other modes is zero.

As shown in Fig.3.2, the transfer function plot of output vector variables is varying with duty cycles at the natural resonant frequency, this is clearer in Fig.3.3, where the Bode plot of the system output voltage at different duty cycles. As shown, its magnitude responses are underdamped except for the case when \( D_1 = 0.125 \) and \( D_3 = 0.375 \). Also, its phase transition is smooth when the duty cycles are similar at 0.25.

![Bode Diagram](image)

Fig 3.2 \( v_o, v_{rc}, i_{in} \) transfer function plot at \( D_1, D_3 \) variation.
Fig 3.3 $v_o$ transfer function plot at $D_1, D_3$ variation.

Fig 3.4 $v_o, v_{rc}, i_{in}$ frequency response at $D_1, D_3$ variation.

Fig. 3.4 shows the frequency response simulated using MATLAB for the output state vectors at different duty cycles of the 2-pseB converter. As can be seen, the waveforms for $v_o, v_{rc}$, and $i_{in}$
are oscillatory, but the least oscillatory behaviors are found when the duty cycles for the two phases are similar ($D_1 = D_2 = 0.25$).

![Bode Diagram](image)

**Fig 3.5** Output voltage transfer function at small changing of two-phase inductance at same duty cycle.

![Bode Diagram](image)

**Fig. 3.6** Output voltage transfer function at $D_1, D_3 = 0.25$ and output capacitor $C_o$ variation from $10\mu F$ to $100\mu F$. 
As seen in Fig 3.5, the effect of inductor size is similar to the effect of duty cycle variation where its magnitude responses are underdamped except for the case when \( L_1 < L_2 \). Also, its phase transition is smooth when the inductors are similar. As shown in Fig. 3.6, the output capacitor or its parasitic ESR variation does not affect the output transfer bode plot except by varying the frequency bandwidth since these effects cancel each other in Mode-I and Mode-III.

The new state equations based on coefficients of \( A_t \) to \( F_t \) equation (3.16) to equation (3.19) may now be perturbed and linearized to obtain the small-signal model of the converter. All state variables may be represented as a dc component plus a small perturbation. To linearize the system, on basis of the classic method, we divided our variables into two parts. The first part is the static part (a fixed DC level), and the second part is a small amplitude that modulates the DC level. On this basis, where each of them has small variations (denoted with \( \hat{\cdot} \) around nominal values of equilibrium solution or quiescent operating point.

\[
\begin{align*}
\{ x(t) &= X + \hat{x} \\
\{ u(t) &= U + \hat{u} \\
\{ d(t) &= D + \hat{d} \\
\{ v_o(t) &= V_o + \hat{v}_o
\end{align*}
\] (3.33)

By substituting equations (3.33) in (3.7) to (3.13), the variables in the state equations of the small signal ac model can be defined as follows:

\[
\hat{X} + \dot{\hat{x}} = A_t \dot{x} + B_t \dot{u} + A_t \hat{x} + B_t \hat{u} + \\
\hat{u} = \sum \left( A_{1} - A_{4} \right) \left( D + \hat{d} \right) + \sum \left( B_{1} - B_{4} \right) \left( D + \hat{d} \right) + \sum \left( C_{1} - C_{4} \right) \left( D + \hat{d} \right) + D + \hat{d}
\] (3.34)
\[\dot{V}_o + \ddot{v}_o = C \ddot{x} + F \ddot{u} + \dot{V}_o + \]
\[\{[(C_1 - C_4) + (C_2 - C_4) + (C_3 - C_4) + C_4]X + [(F_1 - F_4) + (F_2 - F_4) + (F_3 - F_4) + F_4]U\} \ddot{d} \quad (3.35)\]

In another word

\[\dot{x} = A_t \dot{x} + B_t \dot{u} + M_t \ddot{d} \]
\[\ddot{v}_o = C_t \ddot{x} + F_t \ddot{u} + N_t \ddot{d} \quad (3.36)\]

For simplicity, the resulted parasitic components of the four switches and two inductors are set to be zero. The remained perturbation value is presented only with load and series capacitor ESR.

\[r_{on1} = r_{on2} = r_{on3} = r_{on4} = 0, r_c = 0 \text{ and } r_{L1} = r_{L2} = 0 \]

\[M_t = V_{in} \begin{bmatrix} \frac{1}{L_1} \left[ 1 - D_1 \left( \frac{R((D_1 + D_2)(1 + D_3) + r_{cs}D_2D_1)}{\Delta} \right) \right] \\ \frac{D_1}{L_2} \left( \frac{(D_1 + D_2)(1 - D_3)R}{\Delta} \right) \\ 0 \end{bmatrix}, \quad (3.37)\]

\[N_t = V_{in} \begin{bmatrix} D_1(RD_2^2 + D_1D_2R) \\ \Delta \frac{D_1D_2^2}{\Delta} \\ 0 \end{bmatrix}, \quad (3.38)\]

\[\Delta = D_1^2 (r_{cs} D_3 + R) + D_3 R (2D_1 + D_3) \]

These small variations around the nominal equilibrium solution will form second-order nonlinear ac terms, which are small in magnitude compared to the first order ac terms, therefore, they can be canceled and kept linearized model.

### 3.2 The Two-Phase Series Capacitor Buck Transfer Function

After presenting the complete model, analysis and design formulas were derived where the automatic current sharing concept is the main feature of this 2-phase buck topology. The series capacitor voltage is varying to balance the two-phase currents.
Where,

\[ D_1(V_{in} - V_{cs}) - V_{cs} D_3 = 0 \] \hspace{1cm} (3.39)

\[ D_1(V_{in} - V_{cs}) + V_{cs} D_3 - 2V_o = 0 \] \hspace{1cm} (3.40)

Equations (3.39) and (3.40) lead to the same expression of (3.2) when \( V_{cs} \) works as an internal feedback voltage loop to adjust the current sharing for the two phases. Inductor current \( i_{L1} \) charges the series capacitor \( C_s \) while the inductor current \( i_{L2} \) discharges the \( C_s \). Fig.3.7 shows a simplified mathematical representation of 2-pscB converter with its internal current sharing mechanism resulting from the series capacitor voltage \( V_{cs} \) including parasitic components.

Assuming all initial conditions are zero and parasitic components are neglected, there is a need to understand the automatic current sharing mechanism, which is gained by examining the converter waveforms. Because inductor current charges the series capacitor and inductor current discharge the series capacitor, as seen in Fig.3.8 of the average model of the two-phase system, which can be generalized for multiphase structure [3.1]. We need to simplify the mathematical expressions from the previous figure, the average model of 2-pscB excluding all parasitic
components of the inductor currents, series capacitor voltage, and power switches. Assuming all initial conditions are zero, the inductor currents formulas are estimated as follows.

For simplicity at \( r_{on} = 0, \ r_{CS} = r_C = 0 \)

\[
V_{Cs}(t) = \frac{1}{Cs} \int_0^\infty (i_{L1} - i_{L2}) \, dt \tag{3.41}
\]

\[
V_o(t) = V_{Co}(t) = \frac{1}{Co} \int_0^\infty i_{co} \, dt = \frac{1}{Co} \int_0^\infty (i_L - \frac{V_o(t)}{R}) \, dt \tag{3.42}
\]

Where the two phases’ currents are:

\[
i_{L1}(t) = \frac{1}{L_1} \int_0^\infty (V_{in} \, D_1 - V_{CS} \, D_1 - V_o(t)) \, dt \tag{3.43}
\]

\[
i_{L2}(t) = \frac{1}{L_2} \int_0^\infty (V_{CS} \, D_3 - V_o(t)) \, dt \tag{3.44}
\]

Using above formulas (3.43), (3.44), we get the main second order equations representing the system.
\[
\begin{align*}
\frac{d^2 v_{cs}}{dt^2} + v_{cs} \left( \frac{D_1}{L_1} + \frac{D_3}{L_2} \right) &= v_{in} \frac{D_1}{L_1} + v_o \left( \frac{1}{L_2} - \frac{1}{L_1} \right) \\
\frac{d^2 v_o}{dt^2} + \frac{1}{R} \frac{dv_o}{dt} + v_o \left( \frac{1}{L_1} + \frac{1}{L_2} \right) &= v_{in} \frac{D_1}{L_1} + v_{cs} \left( \frac{D_3}{L_2} - \frac{D_1}{L_1} \right)
\end{align*}
\] (3.45)

(3.46)

The Laplace transformation of the two equations

\[
\begin{align*}
V_{cs} \left( S^2 + \left( \frac{D_1}{C_5 L_1} + \frac{D_3}{C_5 L_2} \right) \right) &= V_{in} \frac{D_1}{C_5 L_1} + V_o \left( \frac{1}{C_5 L_2} - \frac{1}{C_5 L_1} \right) \\
V_o \left( S^2 + S \frac{1}{R C_o} + \left( \frac{1}{C_o L_1} + \frac{1}{C_o L_2} \right) \right) &= V_{in} \frac{D_1}{C_o L_1} + V_{cs} \left( \frac{D_3}{C_o L_2} - \frac{D_1}{C_o L_1} \right)
\end{align*}
\] (3.47)

(3.48)

Taking the Laplace transformation of equations (3.47) and (3.48) yields

\[
V_{cs}(s) = V_{in}(s) \frac{\alpha}{\beta S^2 + 1} + V_o(s) \frac{\gamma}{\beta S^2 + 1}
\]

\[
= \text{Steady state part} + \left\{ \begin{array}{l}
\text{transient state function part} \\
\text{unequal phase parasitic noise}
\end{array} \right\} \] (3.49)

The first term of equation (3.49) represents the permanent part of the steady-state, series capacitor voltage should be constant in steady-state as well, and the two inductor currents should be equal in periodic steady state. The second term of the transient function represents the inequality of the two-phase inductor values and the difference due to parasite components of wires. This term will be reduced to zero when there is 100\% current sharing. During the steady-state, the two inductor currents should be equal. In practical cases, when the PCB layout induces a difference in the inductor currents, the voltage of the series capacitor would drift up or down because a smooth charging balance could not be maintained [3.2]. The average capacitor voltage remains constant only when the charge balance exists. The transient time is a function of inductor sizes and matching current paths. Hence

\[
\alpha = \frac{D_1 L_2}{D_1 L_2 + D_3 L_1}, \quad \beta = \frac{C_5 L_1 L_2}{D_1 L_2 + D_3 L_1}, \quad \gamma = \frac{L_1 - L_2}{D_1 L_2 + D_3 L_1},
\]
If both phase inductances are similar, then the difference between current paths is very small and can be ignored. Equation (3.49) is reduced as

$$\frac{V_{Cs}(s)}{V_{in}(s)} = \frac{\alpha}{\beta s^2 + 1}$$  \hspace{1cm} (3.50)

Where $\alpha = \frac{D_1}{D_1 + D_3}$, $\beta = \frac{C_s L}{D_1 + D_3}$, $\gamma = 0$

Fig. 3.9 Series capacitor voltage to input voltage bode plot at $L_1, L_2$ variation.

Fig. 3.9 shows a frequency response of a second-order low pass filter at a cut-off frequency of $\omega_p$ without damping and an extremely narrow peak with infinite gain right at the natural frequency.

This is a system that needs to be avoided because of the underdamping issue. Taking the Laplace transform of equation (3.50) yields.

$$V_{Cs}(t) = V_{in} \sqrt{\frac{D}{2 C_s L}} \sin \left( \sqrt{\frac{2D}{C_s L}} t \right)$$  \hspace{1cm} (3.51)

The output voltage transfer function can be derived from equations (3.43) to (3.46)

$$\frac{V_o(s)}{V_{in}(s)} = \frac{C_s D_1 S^2 + 2 D_1 D_3}{(C_s L_1 S^2 + S^2 + L_1 + L_1 + 1)(C_s S^2 + D_1 L_1)(D_1 L_1 + D_1 L_1 + D_1 L_1)} \frac{D_1 L_1 + D_1 L_1 + D_1 L_1}{D_1 L_1 + D_1 L_1 + D_1 L_1} \frac{D_1 L_1 + D_1 L_1 + D_1 L_1}{D_1 L_1 + D_1 L_1 + D_1 L_1}$$  \hspace{1cm} (3.52)
When both phase parasitic elements are identical and current is fully shared between two phases at a short transient time, the transfer function can be expressed as:

$$H(s) = \frac{V_o(s)}{V_{in}(s)} = \frac{C_s D_1 L S^2 + 2 D_1 D_3}{(C_o L S^2 + L R^2 + 2)(C_s L S^2 + D_1 + D_3)}$$  (3.53)

$$= G_0 \left( \frac{s^2}{\omega_o^2 + \frac{s}{\omega_o} + 1} \right) \left( \frac{s^2}{\omega_p^2 + 1} \right)$$  (3.54)

$$G_0 = \frac{D_1 D_3}{D_1 + D_3}, \quad \omega_o = \sqrt{2 \frac{C_o L}{2}}, \quad Q_O = R \sqrt{2 \frac{C_o L}{L}}, \quad \omega_Z = \sqrt{\frac{2 D_1}{C_s L}}, \quad \omega_p = \sqrt{\frac{D_1 + D_3}{C_s L}}$$  (3.55)

where $\omega_o$ is the natural angular corner frequency at $f_o = \frac{1}{2\pi \sqrt{C_o L}}$

Fig.3.10 shows the damping ratio of the output transfer function at different damping factor values.

![Damping ratio waveform of output to input voltage transfer function of 2-pscB converter at different damping values.](image)
To understand this behavior of equation (3.52), the output voltage transfer function can be divided into sub-functions. Fig. 3.11 shows the output voltage transfer functions at different duty cycles. Where the effect of two zeros is canceling the impact of two poles of \( \omega_p \), then the transfer function of the system will be stable at duty cycle variations

\[
|H_z(s)| = G_o \sqrt{\left(\frac{\omega}{\omega_z}\right)^4 + 1}
\]

(3.56)

![Fig. 3.11 Output transfer function of 2-pscB converter at Different duty cycle values.](image)

\[
|H_p(s)| = \frac{1}{\sqrt{\left(\frac{\omega}{\omega_p}\right)^4 + 1}}
\]

(3.57)

\[
|H_o(s)| = \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_o}\right)^2\right)^2 + \left(\frac{\omega}{Q_o \omega_o}\right)^2}}
\]

(3.58)

\[
|H_s(s)|_{dB} = 20 \log_{10} \left| \frac{|H_z(s)|}{|H_o(s)||H_p(s)|} \right|
\]

(3.59)
With two zeros at the imaginary axis, two pair conjugate poles on the real axis, and another two poles going to infinity, the equivalent state-space representation of the system can be found in the phase variable canonical form of the two-phase series capacitor buck converter. Equation (3.53) can be re-written as follows:

\[ H(s) = \frac{b_2 s^2 + b_0}{s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \]  
\[ (3.60) \]

Where,

\[
\begin{bmatrix}
\dot{x}_1 \\
\dot{x}_2 \\
\dot{x}_3 \\
\dot{x}_4
\end{bmatrix} =
\begin{bmatrix}
-a_3 & -a_2 & -a_1 & -a_0 \\
1 & 0 & 0 & 0 \\
0 & 1 & 0 & 0 \\
0 & 0 & 1 & 0
\end{bmatrix}
\begin{bmatrix}
x_1 \\
x_2 \\
x_3 \\
x_4
\end{bmatrix} +
\begin{bmatrix}
1 \\
0 \\
0 \\
0
\end{bmatrix} V_{in} \quad (3.61)\]

\[ V_o = [0 \ b_2 \ 0 \ b_0] \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \end{bmatrix} + [0] V_{in} \quad (3.62)\]

The canonical form is constructed as shown in Fig. 3.12, where coefficients values can be easily calculated from the transfer function. Theoretically, in the typical case of current sharing, this topology can achieve the maximum energy conversion but not more than a quarter of the input voltage rate. This is not applicable since there is a need to have a small switching deadtime between charging and discharging the series-capacitor.

Fig.3.12 Canonical form of system when \( D_1 \neq D_3 \).
When \( D_1 = D_3 = D \), then \( \omega_z = \omega_p \) in equations (3.54), (3.55). Thus, the two zeros and two poles cancel each other. The output transfer function is reduced to a second-order non-linear system equation.

\[
H(s) = \frac{\frac{D}{T}}{\frac{1}{\omega_0^2} + \frac{s}{Q_0 \omega_0} + 1} \tag{3.63}
\]

Equation (3.63) is similar to conventional buck converter output transfer function at the half duty cycle and can be rearranged to include damping factor as follows:

\[
H(s) = \frac{\frac{D}{T} \omega_0^2}{s^2 + 2\zeta \omega_0 s + \omega_0^2} \tag{3.64}
\]

Where,

\[
s_{1,2} = \alpha_o + j \omega_o \sqrt{1 - \zeta^2} \quad \zeta = \frac{1}{2Q_o} = \frac{1}{2R} \sqrt{\frac{L}{2C_o}}
\]

\( \omega_o \) is called the corner frequency or frequency breakpoint, and \( \zeta \) is the damping factor.

we can relate the corner frequency and damping factor to the poles,

\[
\omega_o = \sqrt{\alpha_o^2 + \beta_o^2} \quad \zeta = \frac{\alpha_o}{\sqrt{\alpha_o^2 + \beta_o^2}}
\]

Using \( G_0 \) in equation (3.53), which represents the duty cycle of 2-pscB converter and could be illustrated as per four cases as follows:

a) \( D_1 \) increasing along with \( D_3 \) increasing OR \( D_1 \) decrease along with \( D_3 \) increasing.

b) \( D_4 \) fixed along with \( D_3 \) increasing OR \( D_1 \) increasing along with fixed \( D_3 \)

Both case intervals limited to the maximum the duty cycle see Fig.3.13

\[
G_0 = \frac{V_o}{V_{in}} \quad 0 < D_1 & D_3 < 0.5
\]

However, to study the series capacitor behavior according to input voltage variations series capacitor voltage transfer function can be derived from equations (3.43) to (3.46).
Fig. 3.13 DC output voltage vs duty cycle  

a) $G_0$ at $D_1$ increase and $D_3$ decrease.  
b) $G_0$ at $D_1$ decrease and $D_3$ increase.

\[
\frac{V_{CS}(s)}{V_{in}(s)} = \frac{G_{cs} \left( \frac{s^2}{\omega_q^2} + \frac{s}{\omega_q \omega_y} + 1 \right)}{\left( \frac{s^2}{\omega_q^2} + \frac{s}{\omega_q \omega_y} + 1 \right) D_1 L_2 (L_2^2 - L_1^2) + D_3 L_1 (L_2^2 - L_1^2)} \left( \frac{1}{D_1 L_2 + D_3 L_1} \right)
\]  

(3.65)

Where,

\[
G_{cs} = 2 \frac{D_1}{D_1 L_2 + D_3 L_1} \frac{L_1 L_2}{L_1 + L_2}, \quad \omega_q = \sqrt{\frac{(L_1 + L_2)}{L_1 L_2 c_0}}, \quad Q_q = R \sqrt{\frac{(L_1 + L_2) c_0}{L_1 L_2}}
\]  

(3.66)

\[
\omega_y = \frac{2}{\sqrt{c_0 L_2}}, \quad Q_y = R \sqrt{\frac{2 c_0}{L_2}}, \quad \omega_w = \sqrt{\frac{D_1 L_2 + D_3 L_2}{c_s L_1 L_2}}
\]  

(3.67)

As seen in equation (3.65), the last denominator term represents the current sharing differences when there is a mismatch between the two phases inductance and capacitance. Hence

\[
\left[ \frac{D_1 L_2 (L_2^2 - L_1^2) + D_3 L_1 (L_2^2 - L_1^2)}{D_1 L_2 + D_3 L_1} \right] \approx 0 \quad \text{at} \ (L_1 = L_2)
\]

The plots for the complex conjugate poles of nominator are causing a peak that can be calculated as:

Peak height = $-20 \log_{10} (2 \zeta_q \sqrt{1 - \zeta_q^2})$  
at a frequency of $\omega_q$ rad/sec (because $\zeta_q$ is small),  

$(\omega_q \approx \omega_{q'})$, where damped natural frequency is expressed as
\[ \omega_q = \omega_q \sqrt{1 - 2\zeta_q^2} \text{ (rad/sec)}, \]

\[ V_{CS}(s)/V_{in}(s) = \frac{G_{CS} \left( \frac{s^2}{\omega_q^2} + \frac{s}{\omega_q Q_y} + 1 \right)}{\left( \frac{s^2}{\omega_q^2} + \frac{s}{\omega_q Q_y} + 1 \right) \left( \frac{s^2}{\omega_w^2} + 1 \right)} \]  

\[ G_{CS} = \frac{D_1}{D_1 + D_3}, \quad \omega_q = \omega_y = \sqrt{\frac{2}{L C_o}}, \quad Q_q = R \sqrt{\frac{2C_0}{L}}, \]

\[ Q_y = R \sqrt{\frac{2 C_o}{L}}, \quad \omega_w = \sqrt{\frac{D_1 + D_3}{C_s L}} \]

This indicate that when both phase inductors are the same, then \( \omega_q = \omega_y \) and \( Q_q \omega_q = Q_y \omega_y \) Hence,
Fig. 3.15 Series capacitor voltage transfer function at duties variation and \( L_1 \neq L_2 \).

\[
\frac{V_{Cs}(s)}{V_{in}(s)} = \frac{G_{Cs}}{\frac{s^2}{\omega_0^2} + 1} \tag{3.71}
\]

where \( G_{Cs} = \frac{1}{2} \)

This reduced relationship is similar to equation (3.50). At unbalanced current conditions the bode plot is as seen in Fig. 3.15. The bode plot of the series capacitor voltage, the frequency breakpoint \( \omega_0 \), and the damping factor variation when \( \zeta_q = \zeta_y \) at unbalanced phases output inductance are illustrated in Fig. 3.16.

The last derived formula will be the formula that describes the relationship between the output voltage and series capacitor voltage using equation (3.41) to (3.47), where,

\[
\frac{V_o(s)}{V_{Cs}(s)} = \frac{G_{cs}}{\frac{s^2}{\omega_m^2} + \frac{s}{Q_m \omega_m} + 1} \tag{3.72}
\]

\[
G_{cs} = D_3 \quad \omega_f = \sqrt{\frac{2 \cdot D_3}{L_2 C_s}} \quad \omega_m = \sqrt{\frac{2}{L_2 C_s}} \quad Q_m = R \sqrt{\frac{2 \cdot C_s}{L_2}} \tag{3.73}
\]
Hence, the numerator and the denominator are in second-order polynomial with two zeros and two poles, thus.

\[ \omega_f = \omega_m \sqrt{D_3} \]  

\[ \frac{V_o(s)}{V_{Cs}(s)} = \frac{G_{cs} \left( \frac{s}{\omega_f} + j \right) \left( \frac{s}{\omega_f} - j \right)}{(s-p_1)(s-p_2)} \]  

The transfer function has 5 components:

- A constant of \( G_{cs} \)
- zeros at \( z_{1,2} = \pm j \omega_f \)
- Complex conjugate poles at the roots \( s^2 + 2\zeta_m \omega_m s + \omega_m^2 \)

\[ p_{1,2} = -\zeta_m \omega_m \mp j \omega_m \sqrt{1 - \zeta_m^2} \]  

As shown in Fig. 3.17, only the numerator of the transfer function is affected by changes in the duty cycle, while the denominator is affected by changes in the inductance and series capacitors.
Fig.3.17 Output transfer function Bode plot with respect to series capacitor voltage.

The voltage-to-output transfer function of the series capacitor acts as a notch filter, which removes only narrow frequency bands. From the Bode plot, we know that notch filters pass the frequency components above and below the notch frequency. This leads to the notch filter’s strongest attribute: they usually cause little phase lag at the gain crossover frequency. Usually, notch filters are used to remove resonances from the converter system. Both the low-pass filter and notch filter can eliminate resonance. This contribution is accomplished while producing a small phase lag in the control loop of the converter. The sharpness of notch filter is determined by factor of \( \frac{1}{Qm\omega m} \) and the center frequency determined by cut-off frequency of \( \omega_f \), Fig.3.18 illustrated the notch filter which is very similar to “Twin Tee” notch filter circuit [3.3] where the stopband Bandwidth is very little, this frequency BW can be controlled by changing the distance between poles and the two zeros \((j, -j)\) in the imaginary axis.
For the ac analysis as we vary frequency \((s \rightarrow j\omega)\) in the first interval, frequency in the third interval is moving up and down along the imaginary axis toward the zeros and then encounters zero and the output response goes to zero, so the fact that we have two zeros in the imaginary axis means the transfer response goes to zero. As seen the system is almost attenuated for about 100 dB, the damping term can be adjusted to affect the depth of the notch at \(\omega_f\). For higher frequencies, there is a gain rising especially at a higher value of damping factor then the high-frequency gain returns to its flat condition at zero \(dB\). To be at the same \(dB\) level we need to move one pole to the left of the notch filter and the other pole to the right. To change the notch depth and make it narrower without changing the notch location or low/high frequency gain we can move both poles inward.

After presenting the system transfer functions, as seen in Fig.3.19, we can conclude that output transfer function can be directly derived as follows:
\[
\frac{V_o(s)}{V_{in}(s)} = \frac{V_o(s)}{V_C(s)} \times \frac{V_C(s)}{V_{in}(s)}
\] (3.77)

Fig.3.19 The 2-pscB converter typical frequency response of transfer functions.

3.3 The Output Impedance Representation

Model output impedance \(Z_o\) is useful way for determining the feasibility of paralleling converters in modular system design, as shown in Fig.3.20. Thus, the transient response may be done with load step response.

\[
Z_o = \left( sL_1 + r_{L1} \right) / \left( r_c + \frac{1}{sC_o} \right) + \left( sL_2 + r_{L2} \right) / \left( r_c + \frac{1}{sC_o} \right)\] (3.78)

\[
Z_o = \frac{Z_g \left( \frac{s^2}{\omega_k^2} + \frac{s}{Q_l \omega_k} + 1 \right)}{\left( \frac{s^2}{\omega_r^2} + \frac{s}{Q_r \omega_r} + 1 \right)}
\] (3.79)

Where:

\[
Z_g = \left( r_{L1} + r_{L2} \right), \quad \omega_k = \frac{r_{L1} + r_{L2}}{\sqrt{(L_1 + L_2)C_o r_c}}, \quad Q_l = \frac{\sqrt{(r_{L1} + r_{L2})(L_1 + L_2)C_o r_c}}{(L_1 + L_2) + (r_{L1} + r_{L2})C_o r_c},
\] (3.80)

\[
\omega_r = \frac{1}{\sqrt{C_o (L_1 + L_2)}}, \quad Q_r = \frac{1}{(r_c + r_{L1} + r_{L2}) \sqrt{\frac{L_1 + L_2}{C_o}}}
\] (3.81)
To simplify the impedance formula at current sharing conditions \( r_{L1} = r_{L2}, L_1 = L_2 \)

3.4 Summary

The main aim at initial stages of the project was to understand the basic concepts of transfer functions that controls the 2-pscB. This understanding will help in enhancement of the overall performance and derive the main specifications formulas in the next chapters. The perturbed and linearized system to obtain the small-signal model of the converter is still not fully discussed and need more effort to have better understanding for noise and stabilities analysis.
3.5 References


4 Chapter 4: Small Signal Representation of 2-pscB Converter.

4.1 Introduction

In literature, many approaches have been proposed for modeling of DC-DC converters, e.g. averaged nonlinear formulation in which switching-frequency is dependent. Another approach is large-signal presentations of the variable-structure system [4.1] where the state-space averaging approach is widely used, which yields an average and linearized model formulation [4.2] dependents on the switching frequency, this model is non-linear and time-varying [4.3]. For simplifying analyses, it is desired to have a constant output voltage $v_o(t) = V_o$. To obtain the desired output voltage there is a need to limit disturbance when there is an input system perturbation the rest of the converter circuit will perturb as well. The disturbance sources in the circuit input voltage and the switching cycle can cause periodic variations in the second and higher AC frequency harmonics, that variations might additionally lead to output current variations. Certain tolerance in the output filter and components specifications need to be set for output signal ripples. Reducing or eliminating the effect of input voltage and converter elements disturbances (ac periodic harmonics) is the goal of designers to deal with the disturbance in negative feedback circuits and to have an automatic circuit to adjust the duty cycles as necessary.

4.2 Small Signal Average Switching Model

The sources of disturbance in power DC-DC systems are many [4.4], [4.15]. Fig.4.1 shows a functional diagram represents some of these sources, where $v_o$ and $i_L$ dependent on independent inputs
\[ v_o(t) = f_1\{v_{in}(t), i_{out}, D_1(t), D_3(t)\} \quad (4.1) \]
\[ i_L(t) = f_2\{v_{in}(t), i_{out}, D_1(t), D_3(t)\} \quad (4.2) \]

Fig. 4.1 Block diagram illustrated the dependence \( v_o \) on independent inputs.

The equivalent circuit model of the 2-pscB converter can be expressed as in Fig. 4.2 which contains four independent inputs (input voltage, two control input variation and load current) and one output dependent variable. Therefore, the ideal transformer averaging model concept can be directly

Fig. 4.2 The 2-pscB system ac small signal variations model.
applied to represent the converter. By realizing equations (4.3) and (4.4), a large signal average
switch model can be formed with transformers and similar average current equations, where,

\[ V_{sw1} = D_1(V_{T1} - V_{T2}) = D_1(V_{in} - V_{CS}) \]  \( (4.3) \)

\[ V_{sw2} = D_3(V_{T2} - V_{T3}) = D_3 V_{CS} \]  \( (4.4) \)

\[ v_y = v_{in} - v_{CS}, \quad i_L(t) = i_{P1}(t) + i_{P2}(t), \quad \frac{v_o}{i_L} = R // \frac{1}{SCo} \]  \( (4.5) \)

At complete current sharing conditions, ideal transformers for both phases will be symmetrical as

\[ D_1 \hat{i}_1 = D_3 \hat{i}_2 \]  \( (4.6) \)

Another way to illustrate 2-pscB converter system ac small signal variations model is seen in

Fig.4.3. The output voltage variation can be expressed.

\[ v_o(s) = G_{vd}(s)\{D_1(s) + D_3(s)\} + G_{-in}(s)v_{in}(s) - Z_o(s)i_{out}(s) \]  \( (4.7) \)

Where \( G_{-in}(s) \) is the line to output transfer function expression. Manipulate block diagram to
Solve for $v_o(s)$. Hence

$$v_o = V_{ref} \frac{G_c G_r G_{vd} / V_M}{1 + HG_c G_r G_{vd} / V_M} + V_{in} \frac{G_{p-in}}{1 + HG_c G_r G_{vd} / V_M} \pm i_{out} \frac{Z_{out}}{1 + HG_c G_r G_{vd} / V_M} \tag{4.8}$$

which is of the form,

$$v_o = V_{ref} \frac{1}{H} \frac{T}{1 + T} + V_{in} \frac{g_{p-in}}{1 + T} \pm i_{out} \frac{Z_{out}}{1 + T} \tag{4.9}$$

With $T(s) = H(s) G_c(s) G_r(s) G_{vd}(s) / V_M$

$T(s)$ is the product of the small signal gains in the foreword and feedback paths of control loop and the modulator voltage of $V_M$ and $H(s)$ is the current sensor gain. To find the output voltage at equilibrium case and complete current sharing, writing the KVL for the simple loops of Fig.4.4 we will have:

![Complete block diagram of two-phase series capacitor voltage regulator.](image)

Fig.4.4 Complete block diagram of two-phase series capacitor voltage regulator.
\[ v_o = i_L \left( R// \frac{1}{sC_o} \right) = (i_{L1} + i_{L2}) \left( R// \frac{1}{sC_o} \right) \quad (4.10) \]

\[ i_{L1}(2sL) - i_{L2}(sL) = \frac{1}{2} v_{in}D_1 + \frac{1}{2} v_{in}D_3 \quad (4.11) \]

\[ i_{L2}(sL) - i_{L1}(sL) + i_{L2} \left( R// \frac{1}{sC_o} \right) = \frac{1}{2} v_{in}D_3 \quad (4.12) \]

After calculating the previous equations, we conclude

\[ v_o = \frac{2 R}{sL(sRC_o + 1)} \left( \frac{1}{4} v_{in}(D_1 + D_3) - v_o \right) \quad (4.13) \]

In another word

\[ \frac{v_o}{v_{in}} = \frac{D_1 + D_3}{s^2L^2C_o + sL/R + 1} \quad (4.14) \]

This formula represents converter line to output transfer function.

\[ G_{v-in}(s) = \frac{\frac{v_o(s)}{v_{in}(s)} |D_1=D_3=0, \ i_{out}=0}{\frac{D_1+D_3}{s^2L^2C_o + sL/R + 1}} = \frac{D_1+D_3}{s^2 + \frac{s}{\omega_0^2} + \frac{1}{Q_0\omega_0}} \quad (4.15) \]

At \( D_1 = D_3 = D \)

\[ G_{v-in}(s) = \frac{D}{2} = G_{go} \]

And

\[ G_{v-in}(s) = G_{v-in}(s)|_{\text{phase I}} + G_{v-in}(s)|_{\text{phase II}} = \frac{v_o(s)}{v_{in}(s)} |_{D_1=0, i_{out}=0} + \frac{v_o(s)}{v_{in}(s)} |_{D_3=0, i_{out}=0} \quad (4.16) \]

\[ G_{v-in}(s)|_{\text{phase I}} = G_{v-in}(s)|_{\text{phase II}} = \frac{D_{1/3}}{s^2 + \frac{s}{\omega_0^2} + \frac{1}{Q_0\omega_0}} + 1 \quad (4.17) \]
Which is similar to equation (3.61), where,

$$\omega_o = \sqrt{\frac{2}{C_o L}}, \quad Q_o = R \sqrt{\frac{2 C_o}{L}}, \quad \text{as derived in chapter 3}$$

To generate a formula represents converter control-to-output transfer function,

$$G_{vD}(s) = \frac{v_o(s)}{D(s)} \bigg|_{v_{in}=0, \ i_{out}=0} = \frac{v_{in}}{\frac{s^2}{\omega_o^2} + \frac{s}{Q_o \omega_o} + 1}$$  \hspace{1cm} (4.18)

$$G_{vD}(s) = G_{vD}(s)|_{\text{phase I}} + G_{vD}(s)|_{\text{phase II}} = \frac{v_o(s)}{D_1(s)} \bigg|_{v_{in}=0, \ i_{out}=0} + \frac{v_o(s)}{D_3(s)} \bigg|_{v_{in}=0, \ i_{out}=0}$$  \hspace{1cm} (4.19)

At complete current sharing

$$G_{vD}(s)|_{\text{phase I}} = G_{vD}(s)|_{\text{phase II}} = \frac{v_{in}}{\frac{s^2}{4 \omega_o^2} + \frac{s}{Q_o \omega_o} + 1}$$  \hspace{1cm} (4.20)

To derive converter output impedance formula

$$Z_{out} = \frac{v_o(s)}{i_{out}(s)} \bigg|_{v_{in}=0, \ D_1=D_3=0}$$

$$= \left( \frac{R}{\frac{L}{2}} \frac{s L}{1 + \frac{1}{s C_o}} \right) = \frac{s L (s^2 L C_o + s L + 2 R + r_L)}{s^2 L C_o + s L + 2 R + r_L} + 1 = \frac{2 s L}{s^2 + \frac{s}{Q_o \omega_o} + 1}$$  \hspace{1cm} (4.21)

In some analysis, accurate models are needed thus, these formulas represent the transfer functions with output filter parasites,

$$G_{v-in}(s) = \frac{v_o(s)}{v_{in}(s)} \bigg|_{D_1=D_3=0, \ i_{out}=0}$$

$$= \frac{D}{2} \left( \frac{2 C_o r_T C + 2 R r_T}{2 R + r_T} \right) = \frac{s^2 \left( R L C_o + L C_o r_T C \right) + s \left( L R C_o r_T + C_o r_T r_L + 2 R C_o r_T C \right)}{2 R + r_T} + 1$$  \hspace{1cm} (4.22)

$$G_{vD}(s) = \frac{v_o(s)}{D(s)} \bigg|_{v_{in}=0, \ i_{out}=0}$$

$$= \frac{v_{in} R}{2 R + r_T} \left( \frac{s C_o r_T C + 1}{s R + 1} \right) = \frac{s^2 \left( R L C_o + L C_o r_T C \right) + s \left( L R C_o r_T + C_o r_T r_L + 2 R C_o r_T C \right)}{2 R + r_T} + 1$$
\[
\frac{R}{2R+r_L} \frac{vi_n\left(\frac{s}{\omega_x}+1\right)}{s^2 \omega_x^2 + s \frac{s}{Q_o \omega_o} + 1} \tag{4.23}
\]

Where,
\[
\omega_x = \frac{R}{C_o r_C}, \quad \omega_o = \sqrt{\frac{2R+r_L}{L C_o (R+r_C)}}, \quad Q_o = \frac{\sqrt{L C_o (2R+r_L) (R+r_C)}}{(L+R C_o r_L+C_o r_C r_L+2R C_o r_C)} \tag{4.24}
\]

A typical output capacitor always exhibits stray elements such as \( r_C \). This parasitic element introduces a zero in the control to output transfer function see equation (4.23). For the proposed case study specifications (see chapter 5). Hence, using these specifications, the simulated relationship between inductor parasitic and converter control to output transfer function at full current sharing is illustrated in Fig.4.5.

Fig.4.5 \( G_{iD} \) and inductor parasitic \( r_L \) variation from 0 to 90mΩ.
Fig.4.6 $G_{vD}$ and output capacitor ESR parasitic variation from 0 to 90mΩ.

The relationship between output capacitor and converter control to output transfer function is illustrated in Fig.4.6. When using the ceramic output capacitor, the output capacitor $r_C$ relay at relatively high frequencies often above the switching frequency so it can be seen in the gain graph. The parameter $\omega_0$ is the angular corner frequency, which is defined as follows.

$$f_0 = \frac{\omega_0}{2\pi}$$

$$f_0 = \frac{1}{2\pi} \sqrt{\frac{2R+r_L}{R} + \frac{1}{L} + \frac{1}{RC}} = 12.97 \ kHz$$ (4.25)

To get well-regulated average output voltage signal, switching frequency must be greater than ten times of angular corner frequency (cutoff frequency) for small or invisible output voltage ripple.

$$f_{sw} > 10 f_0$$
Fig. 4.7 $Z_{\text{out}}$ and inductor parasitic $r_L$ variation from 0 to 90mΩ.

Thus, $f_{\text{sw}} \approx 20f_o$ is recommended. The converter output impedance transfer functions formula including output filter parasites is presented as follows.

$$Z_{\text{out}} = \frac{s^2 \left( \frac{RLC_o r_C}{2R+r_L} \right) + sR \left( \frac{L+C_o r_C r_L}{2R+r_L} \right) + \frac{R r_L}{2R+r_L}}{s^2 L C_o \left( \frac{R+r_C}{2R+r_L} \right) + s \left( \frac{L+R C_o r_L+C_o r_L r_C+2R C_o r_C}{2R+r_L} \right) + 1} \quad (4.26)$$

Inductor parasitic variation affects output impedance in lower frequencies as can be seen in Fig.4.7. Output capacitor ESR parasitic variation affects output impedance in high frequencies as can be seen in Fig.4.8.

From the previous two figures, we can summarize the observations in another way, where the output impedance is represented by the contribution of the filter component, as shown in Fig. 4.9. By the below graph’s inspection of Fig.4.9, we can see that the inductor resistive path $r_L$ dominates the impedance in DC. As frequency increases, the inductor then enters the spectrum. The capacitor impedance starts to take over the inductive section at higher frequencies until it becomes a short
circuit and leaves the output impedance value to its series loss $r_C$. To solve for the peak value of output impedance at resonance value of $f_o$, since $r_C$ contribution is small and neglected at low frequencies.

![Bode Diagram](image)

Fig. 4.8 $Z_{out}$ and output capacitor ESR parasitic variation from 0 to 90 mΩ.

![Bode Diagram](image)

Fig. 4.9 Output impedance bode diagram spectrum.

$$|Z_{out-Max}| = R \frac{2Z_o^2 + r_L^2}{\sqrt{Z_o^2 + (Z_o + r_L)^2} + r_L^2} \quad (4.27)$$
\[ |Z_{out-Max}|_{dB} = 7.96 \, dB \]

Where \( Z_o = \sqrt{\frac{L}{C_o}} \), is the characteristic impedance of the filter.

The output filter needs to be very carefully selected to minimize voltage drop and power loss, which can be achieved by minimizing the output impedance \[4.5\]. Therefore, in order to get rid of the resonance frequency and maintain a good gain value, it is necessary to select a natural frequency higher than the resonance frequency. The natural frequency should be in the output capacitor region, where the influence of inductance is minimal. Thus,

\[ |Z_o-Min| \approx \sqrt{\left(\frac{1}{2 \pi f_{max} C_o}\right)^2 + r_c^2} \quad (4.28) \]

### 4.3 Inductor Currents and Simulation

To investigate the behavior of the total output inductor current, the two-phase series capacitor buck converter was simulated in \textit{LTspice}, and its results are analyzed and compared with complete model simulation results in \textit{MATLAB}. The simulations were done in different scenarios. Based on the concept of automatic current sharing, we need to study the inductor current of each phase. For steady-state conditions, as seen from Fig.4.10, during state one and state three, the current through the inductors is increasing in phase sequence because energy is being stored in the inductors from the input supply or series capacitors. During the off-time of each phase, the current through inductors is decreasing as both inductors are sourcing energy to the output. Note that the current increase at state one is equal to the decrease in current during state two and state three of the same phase. The average series capacitor voltage \( v_{Cs} \) maintains its value at exactly half of the input voltage with a voltage ripple of less than 0.5V, as shown in Fig. 4.10(a). The output voltage ripple can be controlled by the size of the output filter. The average charging and discharging currents
for the series capacitor are similar, as shown in Fig. 4.10(b), this verifies the steady-state operation of the 2-pscB converter. From Fig.4.10(c & d), the current ripple ($\Delta i_{L_1}$) through the phase inductor

Fig.4.10 The 2-pscB converter waveforms (a) series capacitor voltage, (b) series capacitor current (c) phases voltage and current $V_o, I_o$ and (d) two phase inductor currents.
Fig. 4.11 Waveforms (a) voltage $V_{DS}$ and $I_D$ Current of $Q_{II}$ (b) $Q_{II}$ switching losses (c) $V_{GS}$ voltage of $Q_{II}$ and (d) $I_G$ current. 

is greater than the output current ripple ($\Delta i_L$). State four is a repeat of state two with both inductors connected to the ground and supplying energy to the output capacitor. At state one, the average inductor current of phase A is larger than the average inductor current of phase B the series capacitor voltage would slowly increase. When the series capacitor voltage increases, the average switch node voltage $V_{SW1}$ of phase A would decrease, and the average switch node voltage $V_{SW2}$ would increase. This, in turn, would cause the phase A average inductor current to decrease and the average phase B inductor current to increase. Fig. 4.11(a) shows the waveforms for $V_{DS}$ and $I_{DS}$ of $Q_{II}$ during the $D_1T$ interval. As can be seen, both $V_{DS}$ and $V_{CS}$ are half of the input voltage
of 110V. Its drain current, which is also the phase A inductor current increases linearly to charge
the series capacitor to its maximum voltage. Fig 4.11(b) shows the switching losses of $Q_{11}$. Current
spikes occur during the switching transitions of both $Q_{11}$ and $Q_{22}$. The total switching losses are
nearly 40W during a 4 $\text{ns}$ switching period, these values depend on delay time settings. Fig 4.11(c)
shows $V_{GS}$ of $Q_{11}$, and Fig 4.11(d) shows the $I_G$ where the gate currents are less than 1.5A and 2.5A
during the rising and falling edges of the gate pulses.

![Converter waveforms](image)

Fig.4.12 Converter waveforms (a) Output voltage and output current, (b) two phase inductors
current (c) input and output power losses.

For VRMs application, most processors recommend low-output voltage ripple where these
applications demand keeping the output current ripple low. This implies the need for a large
inductor, the relationship expressed as follows,

$$V_{\text{ripple}} = I_{\text{ripple}} \cdot r_c, \quad I_{\text{ripple}} \propto \frac{1}{L} \quad (4.29)$$
On the contrary, as mentioned before, the other requirement is the fast-transient response, as shown in Fig.4.12. This justifies the need for a small inductor to allow the current through the supply to change quickly, but at the same time, this assumption conflicts directly with the need for a larger inductor to minimize output voltage ripple. Fig.4.12(a) shows the output voltage and current waveforms for the converter from the instant that the converter starts with no energy stored in the storage elements. The two-phase current sharing can be seen in Fig.4.12(b). A large magnitude difference in the inductor currents with 180° out of phase can be seen during the initial transient. This magnitude difference decreases as the steady-state condition is attained. The duration of the transient time depends on deadtime matching between the two phases and can be reduced using a soft start scheme with a pre-charged series capacitor. However, this will introduce a delay time to the circuit. Fig. 4.12(c) shows the input and output power losses spectra. As can be seen, the power losses decrease as the steady-state condition is attained. The efficiency reaches 98% for a perfect deadtime implementation in the steady-state operation. From current equations (3.43), (3.44), The first derivative of two-phase currents is:

At \( D_1 = D_3 = D \) and \( L_1 = L_2 = L \)

\[
\frac{d i_L}{dt} = \frac{d i_{L1}}{dt} + \frac{d i_{L2}}{dt} = \frac{1}{L} V_{in} D - \frac{2}{L C_0} \int_0^T (i_L - \frac{V_o(t)}{R}) \, dt
\]  

(4.30)

(4.31)

The second derivatives of two-phase inductor currents, where,

\[
\frac{d i_{L1}^2}{dt^2} = -i_{L1} \frac{1}{L} \left( \frac{D}{C_s} + \frac{1}{C_0} \right) + i_{L2} \frac{1}{L} \left( \frac{D}{C_s} - \frac{1}{C_0} \right) + \frac{V_o}{L C_0 R} = a_1 i_{L1} + b_1 i_{L2} + c_1
\]  

(4.32)

\[
\frac{d i_{L2}^2}{dt^2} = i_{L1} \frac{1}{L} \left( \frac{D}{C_s} + \frac{1}{C_0} \right) - i_{L2} \frac{1}{L} \left( \frac{D}{C_s} - \frac{1}{C_0} \right) + \frac{V_o}{L C_0 R} = a_2 i_{L1} + b_2 i_{L2} + c_2
\]  

(4.33)
Using Laplace transform we can derive the current time domain formulas as

\[
\begin{bmatrix}
    i''_{L1} \\
    i''_{L2}
\end{bmatrix}
= \begin{bmatrix}
    a_1 & b_1 \\
    a_2 & b_2
\end{bmatrix}
\begin{bmatrix}
    i'_{L1} \\
    i'_{L2}
\end{bmatrix}
+ \begin{bmatrix}
    c_1 \\
    c_2
\end{bmatrix}
\]  

(4.34)

For initial conditions \(i_{L1}(0) = 0\), \(i_{L2}(0) = 0\), \(\frac{di_{L1}(0)}{dt} = \frac{v_{in}}{L} D\), \(\frac{di_{L2}(0)}{dt} = 0\)

\[
\frac{d^2 i_L}{dt^2} = \frac{2}{L C_o} \left( \frac{V_0(t)}{R} - i_L \right) = -\frac{2}{L C_o} i_{Co}
\]  

(4.35)

Since \(V_{in} = 0\) for the second derivatives, the average output capacitor current equal zero \(<i_{Co}> = 0\), Then

\[
\frac{d^2 i_L}{dt^2} = 0.
\]

### 4.3.1 Series Capacitor Calculation

To examine the damping oscillation of the current sharing of the two phases regarding inductor resistive parasitic variation. Back to equation (3.43) we can express its formula as:

\[
L_1 \frac{di_{L1}(t)}{dt} = V_{in}D_1 - i_L r_{on1} - V_{CS} D_1 - i_{L1} r_{CS} - i_{L1} r_{L1} - V_0(t)
\]  

(4.36)

\[
L_2 \frac{di_{L2}(t)}{dt} = -i_L r_{on2} + V_{CS} D_3 - i_{L2} r_{CS} - i_{L2} r_{on3} - i_{L2} r_{L2} - V_0(t)
\]  

(4.37)

Plugging equation (3.41) and substitute equation (4.37) into equation (4.36), the results at full current sharing will be,

\[
\frac{d^2 i_{CS}(t)}{dt^2} + \frac{1}{L} \left( \frac{d i_{CS}(t)}{dt} \right) \left( r_L + r_{on} + r_{CS} \right) + \frac{(D_1 + D_3)}{C_s} i_{CS} = 0
\]  

(4.38)

To analyze the effect of \(r_L\) assume other parasites parameters are very small or zero (ideal conditions) to simplify the results also for homogenous second order differential equation,

\[
\frac{d^2 i_{CS}(t)}{dt^2} + \frac{1}{L} \left( \frac{d i_{CS}(t)}{dt} \right) r_L + \frac{(D_1 + D_3)}{C_s} i_{CS} = 0
\]  

(4.39)
Equation (4.39) can be rearranged to

\[
\frac{d^2i_{Cs}(t)}{dt^2} + 2\zeta\omega_{Cs} \frac{di_{Cs}(t)}{dt} + \omega_{Cs}^2 i_{Cs} = 0
\]  

(4.40)

which is in the form of a second-order differential equation representing the damped harmonic oscillator nature with attenuation \((\zeta \omega_{Cs})\) and the angular resonant frequency of \((\omega_{Cs})\).

\[
\zeta = \frac{r_L}{2} \sqrt{\frac{Cs}{L (D_1 + D_3)}}, \quad \omega_{Cs} = \sqrt{\frac{(D_1 + D_3)}{LCs}}, Q_{Cs} = \frac{1}{\tau L} \sqrt{\frac{L (D_1 + D_3)}{CS}} 
\]  

(4.41)

Where \(\omega_{Cs} = \omega_p\) as equation (3.55) of output voltage transfer function

Setting initial values \(i_{Cs}(0^+) = 0\),

From equation (4.36)

\[
\frac{di_{Cs}(0)}{dt} = Cs \frac{d^2v_{Cs}(0)}{dt^2} = \frac{D}{L} \left( V_{in} - 2v_{Cs}(0) \right) 
\]  

(4.42)

Where,

\[
v_{Cs}(0^+) = V_{Cs} - \frac{\Delta V_{Cs}}{2} = 54.7V
\]

Therefore, for given parameters, the system underdamping \((\zeta = 0.0671)\)

\[
i_{Cs}(t) = 0.0922i \left( e^{(-5000-74370.69)i}t + e^{(-5000+74370.69)i}t \right) 
\]  

(4.43)

\[
v_{Cs}(t) = Cs(6875.0 + 4.6119i)e^{(-5000-74370.69)i}t
\]

\[
+ (6875.0 - 4.6119i)e^{(-5000+74370.69)i}t
\]  

(4.44)

The damped harmonic oscillator can be translated as current perturbation representing the difference in phases average inductor currents see Fig.4.13.

The effect of series capacitor ESR and switches internal on-resistance are similar to the inductor DCR effect. For different parameters settings, to find the solution of second-order, linear, homogeneous differential equations with constant coefficients there is a need to figure out the characteristic equation as

\[
a^2 + P_1 a + P_0 = 0
\]  

(4.45)
Fig.4.13 Example response of (a) the difference in average inductor currents due current perturbation in inductor currents for varying values of lumped converter resistance and (b) the difference in average series capacitor voltage.

Fig.4.14 Series capacitor characteristic equation response of (a) the difference in average inductor currents due current perturbation in inductor currents for varying values of lumped inductor resistance and (b) the difference in average series capacitor voltage.

To solve equations with real coefficients the complex roots are always distinct if they are not purely real. So, for complex roots \( s_{1,2} = \alpha \pm j\beta \)

\[
i_{cs} = C_1 e^{\alpha t} \cos \beta t + C_2 e^{\beta t} \sin \beta t
\]  

(4.46)

Where \( C_1 \) & \( C_2 \) are arbitrary constants, Fig.4.14 depicted this type of solution.
4.3.2 Unbalanced Series Capacitor Voltage

The 2-pscB converter current sharing mechanism tolerance will be discussed here, for many reasons, as the case of unmatched duty cycles, this topology has the ability to maintain adequate current sharing balance for a certain limit, this limit depends on charging time of series capacitor which in general affected by the quality of series capacitor material.

Since
\[
\frac{V_{CS}}{V_{in}} = \frac{D_1}{D_1 + D_3}
\]
\[
V_{sw1} = V_{in} - V_{CS}
\]
\[
V_{sw2} = V_{CS}
\]

Thus
\[
\frac{V_{sw1}}{V_{sw2}} = \frac{D_3}{D_1} = \frac{d_3 - d_2}{d_1}
\]
(4.47)

Transient time under unbalanced conditions of phases different duty cycles is longer than balanced conditions transient time where \( D_1 = D_3 \). For unbalanced conditions, the areas of switching voltage node pulses of both phases are the same.

\[
V_{SW1} D_1 = V_{SW2} D_3 = V_o
\]
(4.48)

An example to present these conditions is, at \( D_1 = 0.2 \) and \( D_3 = 0.35 \) or opposite values as shown in Fig.4.15,

\[
\frac{V_{sw1}}{V_{sw2}} = \pm 1.75 \quad \text{and} \quad V_{sw1} \neq V_{sw2}
\]
(4.48)
As shown in Fig.4.15, in both buck phases, when the high-side switch is turned off, the low-side (synchronous rectifier) switch is turned on, and the current is circulating through the lower MOSFET switch. Since the inductor current cannot instantaneously stop, the "on-time" and "off-time" of the switch are unbalanced. For certain limits, during steady-state operation, the series capacitor voltage still manages to maintain the desired output voltage and stable current sharing among the two phases [4.6].

4.4 Two-Phase Series Capacitor Buck Converter Control System Design

Most of the feedback controller designs have been established using the average model for (multiphase) buck converters [4.7] [4.8]. For all cases, the feedback design of the power conversion must first start from the open-loop transfer function of the power system. With nonlinear frequency response, it is necessary to linearize the system through the small-signal model, a transfer function that varies with the operating point can be obtained. According to the
open-loop transfer parameters and resulting equations, the feedback compensation loop can be designed to make the closed-loop system have adequate line voltage and load regulation rate. The output voltage should have a low overshoot when the load current transient occurs, especially when the design includes a long series capacitance charging period, it should quickly return to the steady state settling time. This can be done by analyzing the loop gain of the power circuit then comparing the response bandwidth and the relative stability performance of the system by crossing the phase margin and frequency. For control scheme robustness, it is also expected to have considerable tolerance to ambient temperature and long-term aging. The next step that needs to be figured out is the power switch arrangements. Various choices must be tested to decide appropriate arrangements, then you can either have internal FETs inside a regulator, an integrated regulator circuit type, or you may have an integrated circuit controller driving external switches. [4.9] [4.10].

4.4.1 Average Current Mode Controller

In this design, A 2-pscB converter is discussed within the average model concept. However, the switching frequency plays a critical role in the loop gain in the high-frequency region. Since the method of the averaging model is based on the state-space averaging as discussed in Chapter 1, the highest achievable bandwidth is related to the switching frequency, which eliminates the inherent sampling nature of a switching converter. Traditional voltage-mode control (VMC) of switching converters has only one feedback loop with an output voltage as a control variable, which is simple despite the drawbacks inherited such as poor input and sensitive load transient response for output load changes [4.11]. Peak current-mode control compared with voltage-mode control, utilizes inductor current as the additional inner control variable, which improves the input transient response [4.12]. By using weight factors of inductor current and output voltage, 2-pscB
converter control is designed a unified constant frequency average current mode. This is done when the inner current loop and outer voltage loop are implemented. The block diagram of a typical voltage regulator with inner current control is shown in Fig.4.16. The objective is to design the current and voltage regulators, as highlighted in the red/green dotted boxes. The outer loop is voltage mode control (VMC), while the inner loop is current control. Depending on the selected plant, it is recommended to use the output inductor as the main controlled current. In this case, the total output current is selected. $V_C$ is the output voltage of the error amplifier, $V_{\text{sense}}$ is the inner current regulation voltage, and $r(t)$ is the sawtooth signal. The PWM signal produces when $u(t)$ is compared to the sawtooth signal.

From Fig.4.16 (b), the inductor current, $i_L$, is sensed and fed to the comparator amplifier, with $K_i$ being the current sense gain. This sensed current, $K_i i_L$, flows through $R_i$ and develops a voltage drop across $R_i$, resulting in reduced output voltage under load. Based on the illustrated block diagram, the output of the error amplifier is given by:

$$v_C = A(s)[V_{\text{ref}} - V_{\text{fb}}]$$

$$= A(s)[V_{\text{ref}} - \frac{Z_c(s)\nu_o + Z_{FB}(s)v_c}{Z_c(s) + Z_{FB}(s)}]$$

(4.49)

With further manipulation, equation (4.49) gives,

$$v_C = \frac{V_{\text{ref}} - \frac{Z_c(s)\nu_o}{Z_c(s) + Z_{FB}(s)}}{\frac{1}{A(s)} + \frac{Z_c(s) + Z_{FB}(s)}{Z_{FB}(s)}}$$

(4.50)

If $A(s) \gg 0$, equation (4.50) degenerates into

$$v_C = \left[1 + \frac{Z_c(s)}{Z_{FB}(s)}\right]V_{\text{ref}} - \frac{Z_c(s)}{Z_{FB}(s)} \nu_o$$

(4.51)

Where $Z_c$ serves originally as the negative feedback network of the error amplifier with the
assumption of infinite open loop gain and bandwidth. However, we stick with equation (4.51) since it accounts for the nonideal gain \( A(s) \).

The complementary version of the PWM signal is:

\[
\begin{align*}
    c'(t) &\triangleq 1 - c(t) \\
e'(t) &\triangleq 1 - e(t)
\end{align*}
\]  

(4.52)  

(4.53)

Analytically, since both resistors of the voltage divider affect the DC level of the converter’s output, from the AC point of view, only the upper resistor counted in the AC analysis [4.13]. So, the lower resistor connected to the ground is usually ignored in control loop (AC) analysis and considered just a DC-biasing resistor, after calculating the equivalent impedance \( Z_C \) placed across the Op-Amp, and dividing it by \( Z_{FB} \), for further rearrange the equation is:

\[
H(s)_{Compensator} = \frac{(sC_2(R_1+R_3)+1)(sC_1R_2+1)}{(sR_1(C_1+C_3))(sC_2R_3+1)(sC_1C_3R_2+C_1+C_3+1)}
\]  

(4.54)

Plugging compensator parameters values results

\[
H(s)_{Compensator} = \frac{5.165 \times 10^5}{s} \frac{s^2+1.944 \times 10^4 s+0.0087}{s^2+2.121 \times 10^5 s+1}
\]  

(4.55)

The dynamic plant of 2-pscB converter is represented with control to output transfer function.

\[
G_{vD}(s) = \frac{v_o(s)}{D(s)} = \frac{6.252 \times 10^{16} s + 1.667 \times 10^{23}}{7.635 \times 10^{11} s^2 + 1.063 \times 10^{16} s + 3.043 \times 10^{21}}
\]  

(4.56)

To produce the \( D_{drive} \) signal, \( u(t) \) signal is derived as shown in Fig.4.17. Regarding the modulator gain that consists of the current regulator and the outer voltage regulator, this modulator depends upon the method that is used for current sensing, where the gain depends upon the current expected to be measured. The larger the sensing resistor value, the more accurate the measurement. If the MOSFET on-resistance is being used as a sensing element, that can become a temperature-
dependent variable. So, consideration needs to be adequate about the current sensing method when high quality costlier op-amps are used to achieve superior performance, it is of interest to minimize the number of devices in the circuit, as shown in Fig.4.17, which uses only two op-amps. A total

(a) Simplified regulator circuit with Average current mode controller (ACM).

(b) Compensation network.

Fig.4.16. Block diagram of a typical voltage regulator with inner current control.
of 0.1% mismatch yields almost 66 dB CMR for $R_1 = R_2$ and $\frac{R_2}{R_1} = \frac{R_3}{R_4}$ to reject common-mode noise matching must be extremely well, this can be done using a Precision Difference Amplifier (PDA) like AMP03, AD629, or OPA380. And since the input impedance seen by $v_1$ and $v_2$ is not balanced using a dual precision difference amplifier is recommended, such as OPA830.

\[ v_3 = (v_2 - v_1) \left( \frac{R_2}{R_1} \right) \text{ and } Z_i = \frac{R_2}{R_1}, \text{ for } Z_i \gg 1 \]  
\[ u(t) = v_c - \left( R_{co} + \frac{1}{sC_{co}} \right) \left( \frac{v_3 - v_c}{R_i} \right) \]

\[ = v_c \left( \frac{sR_{co}C_{co} + 1}{sR_iC_{co}} \right) + \left( \frac{R_2}{R_1} \right) \left( \frac{sR_{co}C_{co} + 1}{sR_iC_{co}} \right) \]

\[ = Z_c \left[ v_c \left( 1 + \frac{sR_{co}C_{co} + 1}{sR_iC_{co}} \right) - (v_2 - v_1)Z_i \right] \]  
\[ = Z_c \left( v_c \frac{sR_{co}C_{co} + 1}{sR_iC_{co}} - (v_2 - v_1)Z_i \right) \]  
\[ = Z_c \left( v_c \frac{sR_{co}C_{co} + 1}{sR_iC_{co}} \right) - (v_2 - v_1)Z_i \]  
\[ u(t) = v_c - \left( R_{co} + \frac{1}{sC_{co}} \right) \left( \frac{v_3 - v_c}{R_i} \right) \]

where,
\[ Z_c = \left( \frac{sR_{co}C_{co} + 1}{sR_iC_{co}} \right) \]  
\[ (4.59) \]

The transient response simulation results are illustrated in Fig.4.18 and Fig.4.19.
Fig. 4.18 Output voltage transient response of ACM with step load.

Fig. 4.19 Simulated control waveforms of (ACM).

The ramp signal frequency is twice the converter switching frequency to generate two-phase pulses, as shown in Fig. 4.20. During a step response, the controller decreases the current passing
through the load to minimize the current surge.

Fig. 4.20 ACM Control $D_{drive}$ pulses generation.

Fig. 4.21 PWM block and external sawtooth reference.
The periodic clock signal of the sawtooth reference \( r(t) \) can be divided into two parts, the first part consists of deadtime ramp (down-ramp) that takes 2% of the period time, the second one will be the active ramp (up-ramp) which lasts almost up to 98% of the clock cycle, as seen in Fig.4.21. Hence, the reference \( u(t) \) is swinging between the two values \((V_H, V_L)\) to obtain the formula for \( D_{\text{drive}} \), which can be approximated as

\[
\text{Sawtooth reference } r(t) = V_L + \left( \frac{V_H - V_L}{0.98 \frac{T}{2}} \right) t
\]

\[
= V_L + \left( \frac{V_H - V_L}{0.98 \frac{T}{2}} \right) [D_{\text{drive}} \frac{T}{2}]
\]  \hspace{1cm} (4.60)

At steady state, the driver duty cycle is

\[
D_{\text{drive}} = 0.98 \left( \frac{u(t) - V_L}{V_H - V_L} \right) = 0.98 \left( \frac{A(V_{t+p} - V_{t-n}) - V_L}{V_{t+p} - V_{t-n}} \right) = 0.98 \left( \frac{A(V_{t+p} - V_{t-n}) - V_L}{V_{pp}} \right)
\]  \hspace{1cm} (4.61)

Fig.4.22 Block diagram of Average Current Mode controller.

The overall block diagram to yield the closed-loop output is divided into different blocks the feedback path and the power stage (plant). Inside each block, the relevant equation or formula governing each stage is seen in Fig.4.22. The feedback controller contains a high gain amplifier, at this block diagram we are not actually dealing with the amplifier design but have just focused
almost exclusively on the closed-loop formulation, except representing the voltage error amplifier block with a symbol A(s). The frequency shape that we get from the close loop bode plot resembles a low pass filter, as can be seen in Fig.4.23. At low frequencies, we got a flat gain of zero dB as well as a phase shift that is close to zero as possible. A flat zero dB gain at low frequencies means that output signal $v_o$ is very close to following or tracking (reference tracking performance) the desired reference signal $V_{ref}$ as long as it stays with system boundaries. Any high-frequency bandwidth should be attenuated, and none affect the output signal. The noise rejection of the close loop bode plot shows that the system has good high frequencies of noise rejection characteristics. As can be seen, if we look at the region way off the crossover when the magnitude of the open-loop transfer function is much less than unity at higher frequencies, the unity dominates the relationship and close loop trace will follow the trace of the open-loop transfer function ($G_{vd}$).

![Bode Diagram](image.png)

Fig.4.23 Bode plot waveforms of open & close loop and inductor current of (ACM).

It is worth mentioning this behavior is excluding the effect of the inductor current transfer function. To have a general overview using LTspice simulation of the system with all parameters and setting
values using operational amplifiers to set the control system as shown in Fig.4.24.

Fig.4.24 Close loop bode plot of (ACM) using LTspice simulation.

4.4.2 Proposed $I^2$ Average Current Mode Controller

To improve the transient response and light load efficiency of ACM, by using $I^2$ current mode control another constant frequency mode controller is proposed. Fig.4.25 illustrates the general representation of the constant on-time $I^2$ average current mode control method, which is consists of two current loops and a voltage loop. The current loop consists of a fast-direct feedback loop and a slow (inductor current) integral feedback loop, which is fed back twice. The first one is fast-direct feedback without a low pass filter, and the other is a slow integral feedback loop. The integrator integrates the error between control signal $V_C$ and inductor current $i_L$ and the output of the integrator. The output is compared with the fast-direct feedback current signal to generate the PWM signal. In this improvement, constant on-time modulation is used to integrate the error between the average current value $V_C$ and the sensed inductor current. The integration provides an
offset between $V_C$ and $V_{\text{sense}}$ to eliminate low-frequency control error. The integration loop is low bandwidth so that the high-frequency components are strongly attenuated.

During transient, the fast change of $V_C$ pass to $V_{\text{sense}}$ as the $C_{co}$ voltage does not have sudden change. The compensation network essentially consists of an Operational Transconductance Amplifier (OTA) in $(A/V)$ whose output drives a single capacitor $C_{thp}$ in parallel with a capacitor $C_{th}$ and variable resistor $R_{th}$ in series [4.13]. The compensation network is a Type II Compensator using an OTA circuit with open-loop gain $A(s)$ and amplifier output impedance $Z_{th}(s)$. Type II compensators are commonly used in current mode-controlled switching converter feedback circuits this can provide a good load regulation, line voltage, and topology transient response. In many cases, at input voltage or load current changes, the stability may deteriorate due to phase margin decreasing. The control loop can be presented as the following transfer functions:

$$A(s) = \frac{V_C(s)}{V_{fb}(s)} = gm \ast Z_{th}(s)$$  \hspace{1cm} (4.62)
\[
\frac{V_c(s)}{V_o(s)} = \frac{V_{fb}(s)}{V_o(s)} \cdot gm \cdot Z_{th}(s) \quad (4.63)
\]

\[
\frac{V_o(s)}{I_e(s)} = Z_{filter}(s) = \frac{R}{1 + SC_oR} \quad (4.64)
\]

\[
Z_{th}(s) = \frac{SC_{th}R_{th} + 1}{S(SR_{th}C_{th}C_{thp} + C_{thp} + C_{th})} \quad (4.65)
\]

\(gm\) is the transconductance of the error amplifier \(s\). Suppose the current sensing gain is \(G_c\)

\[
\frac{I_e(s)}{V_c(s)} = G_c(s) \quad (A/V) \quad (4.66)
\]

Hence, overall loop gain, \(H(s)\), is obtained by multiplying the three transfer functions as mentioned above.

\[
H_{plant}(s) = \frac{V_{fb}(s)}{V_o(s)} \cdot gm \cdot Z_{th}(s) \cdot G_c(s) \cdot \frac{R}{1 + SC_oR} \cdot \frac{SC_{th}R_{th} + 1}{S(SR_{th}C_{th}C_{thp} + C_{thp} + C_{th})} \quad (4.67)
\]

Where we can visualize this feedback stage as a product of three cascade transfer functions. It combines a pole/zero pair plus an origin pole for a high DC gain, and voltage regulator the transfer function is defined as

Fig.4.26. Output voltage transient response of ACM with step load.
\[
H_v(s) = -Z_{FB} \ast gm \ast \frac{SC_{th}R_{th}+1}{S^2R_{th}C_{th}C_{thp}+S(C_{thp}+C_{th})}
\] (4.68)

\(Z_{th}(s)\) is the impedance of the RC compensation network. The proposed control can achieve fast and accurate current sharing control between two phases without the need for an external ramp circuit. In CCM, the switching frequency of \(I^2\) control is independent of the inductor size. The proposed control scheme is verified by simulation, as shown in Fig. 4.26.

### 4.4.3 Proposed Enhanced \(I^2\) Controller

\(I^2\) control is a popular and simple control scheme of Buck converters control, featured with a transient response which is mixed of current-mode control and compensated voltage feedback in \(I^2\) control, the output current is directly fed back to PWM comparator and compared with compensator control signal \(V_C\).

Fig. 4.27 Enhanced \(I^2\) controller scheme of 2-pscB converter.
The output current ripple is used as a PWM signal ramp so that this type of control is called “ripple-based control”. Enhanced I² control scheme feeds back the summing signal of the total output current information via current sensing gain $Z_i$ and voltage divider signal via current sensing gain $Z_v$ which is small compared to the previous signal and can be ignored. The resulted signal is then compared with the compensated voltage regulator signal.

The improved I² control can achieve a fast load transient response when the equivalent series resistor (ESR) of the output capacitors is used as the current sensing resistor. Enhanced I² control scheme with the inner loop uses the voltage $V_{sense}$ across the sensing resistor $R_s$, which generated by inductor current $i_L$ as a feedback control variable, as shown in Fig.4.27. The outer loop uses the control signal $V_C$ by compensating the voltage error between $v_O$ and reference voltage $V_{ref}$ in the error amplifier. The error amplifier is commonly a PID compensator.

![Fig.4.28 Transient response with a) step load b) output voltage c) two phase current.](image)

In this control method, overshooting is less due to fast-direct feedback loop action, where series
capacitor charging starts instantaneously at zero-time. The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during startup.

The load transient response simulation results are illustrated in Fig.4.28 and Fig.4.29. The ramp signal frequency is twice the converter switching frequency to generate two-phase pulses $D_1$, $D_3$ as shown in Fig.4.30.

Fig.4.29 Enhanced $I^2$ controller parameters waveform.

To study the converter figure of merit (FOM) using load transient response of the previous control schemes, when the output voltage dips during a situation of load dump switching frequency remains the same and not affected by transient time. The on-time is the same due to the presence of two phases connection and series capacitor that delivers more output power in order to meet the
load demand, as shown in Fig.4.31. In the case of load release, the off-time also remain balanced and not affected by transient recovery and no need for recovery time or change in switching.
frequency where transient falling dip and transient recovery voltages are the same that can be estimated as follows:

\[ V_T \approx \frac{\Delta i_o}{2\pi f_o C_o} = 0.7 \text{ V} \quad (4.69) \]

### 4.4.4 Proposed Valley Current Mode Controller

There are many methods to control 2-pscB converters, as shown in Fig.4.32, this type of control can be called Valley Current Mode Controller (VCM), where the inner loop uses the voltage \( V_{sense} \) generated by inductor current \( i_L \) as a feedback control variable. The outer loop uses the control signal \( V_C \) by compensating the error between output voltage \( V_{fd} \) and reference voltage \( V_{ref} \). This type of control has a faster load transient response and is essentially a valley ripple-based control technique [4.14,4.15].

Fig.4.32 The 2-pscB converter valley current mode controller.
Fig. 4.33 The effect of larger output capacitor on VCM.

Increasing output capacitor value has a major effect on the transient response speed of the converter, as can be seen in Fig. 4.33. It reduces the fluctuation in series capacitor voltage due to
the reduction of the sensing current value of $V_{\text{sense}}$, but at the same time increases the current surge that is needed to charge this capacitor. Pulse generation of VCM is almost similar to ACM Control $D_{\text{drive}}$ pulses generation, as shown in Fig.4.20. The four control types introduced previously are simulated using case study (Chapter 5) specifications and compared as depicted in Fig.4.34.

4.5 Summary

The main purpose of this chapter is to provide a comprehensive overview of the 2-pscB topology started from the model of the AC small-signal variation of the system to the characteristic equation response of balanced and unbalanced series capacitor voltage. A novel approach for the current-mode controller using one current path to minimize the propagation delays and overall parasitic components, which would help in the enhancement of the overall performance. Theoretical analysis and comparison between control methods were presented, and experimental results were verified in the next chapters. Appendix A shows MATLAB Simulink (m.file) and simulation results for CCM of CMC 2-pscB converter controller. Appendix B & D dealt with VCM and CMC controllers’ simulation.
4.6 References


5 Chapter 5: Case Study.

5.1 Introduction

In the previous chapter, we discussed the 2-pscB converter controller, although the overall performance improvement depends on the selection of parameters and specifications based on the derived formula. In this chapter, to demonstrate the functionality of the prototype 2-pscB converter, design parameters and specifications must be defined. Then the focus will be on the comparison between conventional buck and the multi-phase series capacitor. This step shows the range of benefits, including complete current sharing conditions that are not applicable in a conventional buck. Studying the amplitude and phase spectrum of the two-phases node switching voltages in the frequency domain at complete current sharing conditions will be discussed at the end of this chapter [5.1], [5.2].

5.2 2-pscB Converter Design Parameters and Specifications

For theoretical analysis and practical evaluations specifications, design parameters values have been chosen using table I, these specifications are as follows:

For ideal case at complete current sharing when interval duty cycle

\[ D_1 = D_3 = D \text{ or } d_1 = 0.25, \quad d_2 = 0.5, \quad d_3 = 0.75, \quad \text{and } r_{on}, \quad r_{cs} \text{ are very small or neglected at fixed load of } R = 4\Omega. \]

Let us assume parasitic components of switches are equals,

\[ r_{on1} = r_{on2} = r_{on3} = r_{on4} = r_{on} \text{ and } r_{L2} = 0 \]
TABLE I: 2-pscB Converter Evaluation Parameters

<table>
<thead>
<tr>
<th>Component</th>
<th>Abbri.</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series Capacitor</td>
<td>Cs</td>
<td>&lt; 10 μF</td>
</tr>
<tr>
<td>Phase Inductors</td>
<td>L₁ &amp; L₂</td>
<td>10 μH</td>
</tr>
<tr>
<td>Output Capacitor</td>
<td>Co</td>
<td>&gt;100μF</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>F_{sw}</td>
<td>250 kHz</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>V_{in}</td>
<td>110 V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>V_o</td>
<td>12.5-13V</td>
</tr>
<tr>
<td>Stray Components</td>
<td>r_{cs}, r_c</td>
<td>30 mΩ</td>
</tr>
<tr>
<td>Stray Components</td>
<td>r_{on}, r_{L1}, r_{L2}</td>
<td>0 mΩ</td>
</tr>
<tr>
<td>Output Power</td>
<td>P_o</td>
<td>&lt; 75 W</td>
</tr>
</tbody>
</table>

Implanting previous derived equations in chapter 3, (3.24 – 3.31) and Table I.

\[
\frac{V_o}{V_{in}} = \frac{DR}{2R - 2D r_{on}} \triangleq \frac{D}{2} = 0.125 
\]

\[
I_L = < i_L > = \frac{V_{in}D}{2R} = \frac{V_{sw}D}{R} = 3.49 \text{ A} 
\]

\[
V_{Co} = \frac{V_{in}D}{2} = V_{sw}D = 13.7 \text{ V} 
\]

\[
V_{cs} = \frac{V_{in}(R - DR_{cs})}{2R} \triangleq \frac{V_{in}}{2} = 55 \text{ V} 
\]

Since the average current of low pass filter capacitor is zero, then \(< i_{Co} > = 0 \) from schematic diagram of Fig.3.1 we get,

\[
< i_{Co} > = \frac{R}{R + r_c} < i_L > = \frac{< v_{Co} >}{R + r_c} = 0 
\]

(5.1)

And

\[
< v_o > = \frac{r_c}{R + r_c} < i_L > + \frac{R}{R + r_c} < v_{Co} > 
\]

(5.2)

Where \(< v_o > \approx < v_{Co} > + < v_{rc} > \approx < v_{Co} > \)

\(< v_o > = 13.8 \text{ V} \)

\(< i_L (t) > = < i_{L1} (t) > + < i_{L2} (t) > = < i_R (t) > 
\]

(5.3)
\( < i_R(t) > = < i_{R_1}(t) > + < i_{R_2}(t) > = I_R = 3.49 \ A \)

Where \( < i_{R_1}(t) > \) and \( < i_{R_2}(t) > \) are phases current contribution in output currents which are equal only at full current sharing conditions. At steady state conditions the inductor currents are:

\( < i_{L_1}(t) > = < i_{L_2}(t) > = 1.74 \ A \)

\( \Delta i_{C_0} = 2.68 \ A \)

\( \Delta i_{L_1} = \Delta i_{L_2} = 4.17 \ A \) which considered a high ripple value for this design parameters and bigger than overall output current ripple.

As seen in Fig.4.10(c & d), we can substitute for \( I_{min} \) in terms of phase \( I_{out} \) and determine the upper limit of the inductor ramp current. For phase A of inductor \( L_1 \) as shown in Fig.5.1

\[
I_{L1min} = I_{R_1} - \frac{1}{2} \left[ \frac{V_o}{L_1} (1 - d_1)T \right] = -0.34 \ A
\]

\[
I_{L1max} = I_{R_1} + \frac{1}{2} \left[ \frac{V_o}{L_1} (1 - D_1)T \right] = 3.83 \ A
\]

\[
I_{L1max} = I_{R_1} + \frac{\Delta i_{L1}}{2}, \ I_{L1min} = I_{R_1} - \frac{\Delta i_{L1}}{2}
\]

For Phase B

\[
I_{L2min} = I_{R_2} - \frac{1}{2} \left[ \frac{V_o}{L_2} (d_2 + 1 - d_3)T \right] = I_{R_2} - \frac{1}{2} \left[ \frac{V_o}{L_2} (1 - D_3)T \right] = -0.35 \ A
\]

\[
I_{L2max} = I_{R_2} + \frac{1}{2} \left[ \frac{V_o}{L_2} (d_2 + 1 - d_3)T \right] = I_{R_2} + \frac{1}{2} \left[ \frac{V_o}{L_2} (1 - D_3)T \right] = 3.83 \ A
\]

where \( T_{on} = D_1T = D_3T \). As such, a larger \( L \) and smaller \( T_{on} \) will yield a smaller ripple current.

The total average output current in terms of \( i_L \) will be:

\[
I_{out} = \frac{I_{L1max}+I_{L1min}}{2} = I_{R_1} + I_{R_2}
\]

\[
\Delta i_{L_1} = \Delta i_{L_2} = \frac{1}{L} \left( \frac{V_{in}}{2} - V_o \right) T_{on}
\]
Equation (5.10) represents the peak-to-peak current ripple of both phases at complete current sharing since the value for $I_{L(1,2)max}$ is limited to the high-side power switch current rating, allowing the effective output current of the circuit to approach the switch current rating. There is a need to reduce the ripple current (the difference between the average load current and the peak of the total inductor current). The equation above indicates the following general trends for a 2-pscB converter circuit, some observations can be listed as follows [5.3]:

- Higher phase inductors size allow higher load current for a fixed switching frequency or $(L \propto \frac{1}{\Delta i_L})$
- In contrary, higher switching frequency allows higher load current for a fixed phases inductance level $(T_{on} \propto \Delta i_L)$ and $(T_{on} \propto I_{NFET})$ especially at a high step-down ratio which is the case at $V_{in} \geq 4(V_o + E_{oss})$, where $I_{NFET}$ is peak switch current.
- Reduction of the slope of the inductor current and differential inductor voltage during the ramp-up period can be observed at a lower step-down ratio.
For the total average output inductor current \( i_L(t) = i_{L1}(t) + i_{L2}(t) \) and since the waveforms are out of phase.

\[
I_{L-rms} = \sqrt{I_{L1-rms}^2 + I_{L2-rms}^2} \quad (5.11)
\]

To calculate the minimum value of inductor current waveform

\[
I_{Lmin} = I_{min1} + \left( \frac{v_{in} - v_{cs}}{L_1} \right) t + \frac{2}{3} I_{max2} - \frac{v_o}{L_2} t \quad (5.12)
\]

The total inductor current at zero condition is equal to the minimum value \( I_{Lmin} \), when \( Q_{II} \) is off in mode II, IV, the minimum total inductor current will be:

\[
I_{Lmin} = i_L(0) = I_{min1} + \frac{2}{3} I_{max2} \quad (5.13)
\]

\[
= I_{R1} - \frac{1}{2} \left[ \frac{V_o}{L_1} (1 - d_1)T \right] + \frac{2}{3} \left( \frac{V_o}{L_2} (d_2 + 1 - d_3)T \right) \]

\[
= \frac{5}{6} I_{out} + \frac{1}{2} \left[ \frac{V_o}{L} \left( \frac{2}{3} (1 - D_3) - (1 - D_1) \right) \right] = 2.14 A \quad (5.14)
\]

Which equal to \( \frac{5}{6} I_{out} - \frac{1}{6} \left[ \frac{V_o}{L} (1 - D)T \right] \) at current sharing condition, thus,

\[
I_{R1} = I_{R2} = \frac{1}{2} I_{out} \quad (5.15)
\]

At the same time

\[
I_{Lmin} = i_L(d_2T)
\]

\[
= \frac{1}{3} I_{max2} - \frac{V_o (d_2 - d_1)T}{L_2} + I_{max1} - \frac{V_o (d_2 - d_1)T}{L_1} \quad (5.16)
\]

Or

\[
I_{Lmin} = \frac{2}{3} I_{max1} - \frac{V_o}{L_1} (d_2 - d_2)T + I_{min2} + \frac{(-V_o + V_{cs})}{L_2} (d_2 - d_2)T \quad (5.17)
\]

\[
= 2.21 A
\]

when the load current is contributed by each phase at complete current sharing condition, the maximum inductor current value will be at the fully charging period of the series capacitor in phase A and at fully discharging in phase B.
\[ I_{L_{\text{max}}} = i_L(d_1T) = I_{\text{max}}_1 - \frac{v_o(d_1T - d_4T)}{L_1} + \frac{1}{3} I_{\text{max}}_2 - \frac{v_o(d_4T - d_1T)}{L_2} \]

\[ = I_{\text{max}}_1 + \frac{1}{3} I_{\text{max}}_2 \]

\[ = I_{R_1} + \frac{1}{3} I_{R_2} + \frac{1}{2} \frac{v_oT}{L} \left[ \frac{1}{3} (1 - D_3) + (1 - D_1) \right] \] (5.18)

Also,

\[ I_{L_{\text{max}}} = \frac{2}{3} I_{\text{out}} + \frac{2}{3} \left[ \frac{v_o}{L} \ (1 - D)T \right] = 5.1 \text{ A} \] (5.19)

Thus, the peak-to-peak inductor current ripple is,

\[ \Delta i_L = I_{L_{1_{\text{max}}}} - I_{L_{1_{\text{min}}} - \frac{1}{3} I_{L_{2_{\text{max}}}}} \]

\[ = \frac{5}{6} \left[ \frac{v_o}{L} \ (1 - D)T \right] - \frac{1}{6} I_{\text{out}} \]

\[ = \frac{1}{6} \left[ 5 \Delta i_{L_{\text{phase}}} - I_{\text{out}} \right] \] (5.20)

\( \Delta i_{L_{\text{phase}}} \) is Phase A or B current ripple at fully current sharing.

Using the maximum and minimum values of total inductor current we can represent the slope of inductor current waveform at complete current sharing conditions as:

\[ m_r = \frac{di_L}{dt} = \frac{v_o}{6} \left[ \frac{1}{D} - 1 \right] - \frac{f_{sw}}{D R} \] (Ampere/sec). (5.21)

This formula represents the rising slope of the total average inductor current in terms of load and switching frequency \( m_r = 2.91 \text{ A/\mu s} \) for design specifications. Inductor falling current slope during the decreasing interval is the slew rate.

\[ m_f = 2 \frac{v_o}{L} \] (Ampere/sec). (5.22)

For period duration \( (d_2 - d_1)T \) falling current slope will be in negative sign of \( m_f = 2.794 \text{ A/\mu s} \)
5.2.1 Inductor and Inductor Current Ripple Calculation:

The design specification of the voltage ripple needs to be set before inductor calculations. With multiphase buck topology, the output voltage ripple is greatly reduced, which enables the use of very small inductances in each phase to improve the transient response requirement. Equation (5.14) at continuous current mode (CCM) operation, $I_{L_{\text{min}}}$ is a positive value. During current sharing when $L_1 = L_2$, $I_{L_{\text{min}}} > 0$, we have

$$\frac{5}{6} I_{\text{out}} - \frac{V_{\text{out}} T}{L} \left( \frac{1 - d_1}{2} - \frac{(d_2 + 1 - d_3)}{3} \right) > 0$$

(5.23)

Thus,

$$L > \frac{RT}{5} (1 - 3d_1 - 2d_2 + 2d_3)$$

(5.24)

The critical value for the two-phase inductors is,

$$L_{\text{critical}} > \frac{R}{5 f_{\text{sw}}} (1 - 3D_1 + 2D_3)$$

(5.25)

The size of inductor decreases with the increase of switching frequency, to consider the maximum value of load where,

$$R_{\text{min}} < R < R_{\text{max}}$$

$$L_{\text{critical}} > \frac{R_{\text{max}}}{5 f_{\text{sw}}} (1 - 3D_1 + 2D_3)_{\text{min}}$$

(5.26)

For this case study parameters

$L_{\text{critical}} > 2.4 \mu H$

It is worth noting that the efficiency of the converter increases as the size of the inductor increases, at the expense of its transient response performance. To avoid this effect, the inductance size should be chosen to provide a reasonable efficiency, good transient response, and a small layout area at the same time. Compared to the single-phase inductor current, the total ripple of
output inductor current has a smaller magnitude and is twice the ripple frequency. Multiphase series capacitor buck converter combines all phase-shifted inductor currents from single-channel or phase, the output capacitor charges, and discharges at the same time, and therefore greatly reduced the total current ripple flowing into the output capacitor. Increasing the output current ripple will result in less output filtering effort needed.

Hence,

$$\Delta i_{L1} = I_{L1\text{max}} - I_{L1\text{min}} = 4.17 \, \text{A} $$
$$\Delta i_{L2} = I_{L2\text{max}} - I_{L2\text{min}} = 4.17 \, \text{A}$$

The total current ripple will be less in magnitude,

$$\Delta i_L = I_{L\text{max}} - I_{L\text{min}} = 2.68 \, \text{A}$$

Another expression with phase currents

$$\Delta i_L = I_{L1\text{max}} + \frac{1}{3} I_{L2\text{max}} - \left( I_{L1\text{min}} + \frac{2}{3} I_{L2\text{max}} \right)$$

$$= I_{L1\text{max}} - I_{L1\text{min}} - \frac{1}{3} I_{L2\text{max}}$$

(5.27)

Substitute in the above formula we got the overall output current ripple as follows:

$$\Delta i_L = V_o \left( \frac{(1-d_1)T}{L} - \frac{1}{6R} \left( \frac{d_2 + 1 - d_3}{6L} \right) \right)$$

$$= V_o \left( \frac{T}{L} \left( \frac{5}{6} - D_1 + \frac{D_3}{6} \right) - \frac{1}{6R} \right)$$

$$= \frac{V_o}{6} \left( \frac{1}{L f_{sw}} (5 - 6 D_1 + D_3) - \frac{1}{R} \right)$$

(5.28)

$$= 2.81 \, \text{A}$$

In ideal case of complete current sharing, we conclude

$$\Delta i_L = \frac{V_o}{6} \left( \frac{5}{L f_{sw}} (1 - D) - \frac{1}{R} \right)$$

(5.29)

As such, the phase inductor value can be expressed in terms of its current ripple as

$$L = \frac{5 R V_o (1-D)}{f_{sw} [6 R \Delta i_L + V_o]}$$

(5.30)
For values of case study design specification, we choose $L = 10 \, \mu H$

5.2.2 Output Capacitor Calculation:

The instantaneous capacitor charge stored in one half switching period can be used to determine its output capacitor value, as shown in Fig.5.2. In this case, we find the total charge $q$ held in the positive portion of capacitor symmetrical waveform is:

$$\Delta q = \frac{1}{2} \left( \frac{T}{2} \right) \frac{\Delta I_L}{2} = C_o \Delta V_o$$

(5.31)

The total charge in capacitor is related to the peak-to-peak output voltage ripple.

Assume the limit is $\Delta V_o = \Delta V_{C0} = 0.11 \, V$

Hence,

$$C_o = \frac{T}{16} \frac{\Delta I_L}{\Delta V_o}$$

(5.32)

Substitute with equation (5.28)

$$C_o = \frac{T V_o}{16 \Delta V_o} \left( \frac{T}{L} \left( \frac{5}{6} - D_1 + \frac{D_2}{6} \right) - \frac{1}{6R} \right)$$

(5.33)

The voltage ripple (%)
\[
\frac{\Delta V_o}{V_o} = \frac{T}{16 C_o} \left( \frac{T}{L} \left( \frac{5}{6} - D_1 + \frac{D_3}{6} \right) - \frac{1}{6R} \right) \quad (5.34)
\]

\[
C_o > \frac{V_o}{96 f_{sw} \Delta V_o} \left( \frac{1}{L_{fsw}} (5 - 6D_1 + D_3) - \frac{1}{R} \right) \quad (5.35)
\]

Putting equation (5.35) into different look yields the final equation for the output capacitor \( C_o \)

\[
C_o > \frac{1}{96 f_{sw} (\frac{\Delta V_o}{V_o})_{max}} \left( \frac{1}{L_{fsw}} (5 - 6D_1 + D_3) - \frac{1}{R} \right) \quad (5.36)
\]

At fully current sharing.

\[
C_o > \frac{1}{96 f_{sw} (\frac{\Delta V_o}{V_o})_{max}} \left( \frac{5}{L_{fsw}} (1 - D) - \frac{1}{R} \right) \quad (5.37)
\]

From case study specifications, for \( \Delta V_o \) value the value of output capacitor is \( C_o > 6.61 \, \mu F \).

For smaller output voltage ripple \( \Delta V_o \) this value will gradually increase. The total current in the output capacitor is the sum of four interval currents, which is a continuous output capacitor current. Maximum and minimum values of this current can be calculated from equations (5.38) and (5.39), where the average current will be zero and the charge stored in the capacitor is related to the capacitor size.

\[
I_{C_{o_{max}}} = \frac{R}{R + r_{co}} I_{L_{max}} - \frac{1}{R + r_{co}} \left( V_o + \frac{\Delta V_o}{2} \right) \quad (5.38)
\]

\[
I_{C_{o_{min}}} = \frac{R}{R + r_{co}} I_{L_{min}} - \frac{1}{R + r_{co}} \left( V_o - \frac{\Delta V_o}{2} \right) \quad (5.39)
\]

The first term represents the inductor current, and the second term represents the output current. Depending on the maximum and minimum output capacitor current expressions, we conclude:
\[
\Delta i_{Co} = \frac{1}{R + r_{Co}} (R \Delta i_L - \Delta v_o)
\] (5.40)

For smaller output capacitor parasitic resistance \(r_{Co}\) and smaller \(\Delta v_o\)

\[
\Delta i_{Co} \cong \Delta i_L
\] (5.41)

\[
I_{Co_{max}} = \frac{1}{R + r_c} \left( R \, I_{L_{max}} - v_o - \frac{\Delta v_o}{2} \right) = 1.3 \text{ A} , \quad I_{Co_{min}} = -1.3 \text{ A}
\]

\[
< i_{Co} > = \frac{I_{Co_{max}} + I_{Co_{min}}}{2} = 0
\] (5.42)

For ideal two-phase series capacitor converter with minimum power losses

\[
P_{in} = P_{out}, \quad V_{in} < i_{in} > = V_o \, I_{out}
\]

\[
\frac{<i_n>}{<i_L>} = \frac{<i_s>}{<i_t>} = \frac{D_1 D_3}{D_1 + D_3} = \frac{<i_{in}>}{I_{out}}
\] (5.43)

Where \(<i_L>\) the average of two-phase inductor current. \(<i_L> = I_L\)

The rms value of total inductor current expression is,

\[
I_{L_{rms}} = \sqrt{I_L^2 + \left( \frac{\Delta i_L}{\sqrt{3}} \right)^2}
\] (5.44)

Thus,

\[
I_L = \frac{I_{L_{max}} + I_{L_{min}}}{2} = 3.5 \text{ A}
\]

\[
I_{L_{rms}} = 3.735 \text{ A}
\]

5.3 Defining the Series Capacitor Expressions

Series capacitor voltage (\(v_{Cs}\)) acts as an internal feedback loop quantity to adjust the current
sharing for the two phases. As such, if the inductor currents are not equal, the series capacitor voltage would drift up or down, and a smooth charging balance could not be maintained. This response is because the average capacitor voltage remains constant only when the charge and discharging period balance exists. The inductor currents, $i_{L1}$ and $i_{L2}$ charge and discharge the series capacitor $C_S$ respectively. In a steady-state at automatic current sharing mechanism, the two inductor currents should be equal, then the average series capacitor voltage will be constant as well with approximately half the input voltage across it, and the series capacitor acts as a dc voltage source for the third interval. Hence.

Fig. 5.3 Series capacitor current and voltage at steady state.

Mode I: $< i_{CS} > = < i_{L1} >$

Mode II, IV: $< i_{CS} > = 0$

Mode III: $< i_{CS} > = -< i_{L2} >$,

Where $i_{L1} D_1 - i_{L2} D_3 = 0$
\[ <i_{Cs} > = < i_{L_1} > D_1 - < i_{L_2} > D_3 = 0 \]

Using \( i_{Cs} \) waveform in Fig.5.3, if \( I_{minD1} \) can be neglected, the minimum \( Cs \) value can be generalized and expressed at complete current sharing as follows,

\[
\Delta Q = D_1 T I_{minD1} + \frac{1}{2} D_1 T \frac{\Delta i_{L_1}}{2}
\]

\[ = D_3 T I_{minD3} + \frac{1}{2} D_3 T \frac{\Delta i_{L_2}}{2} = Cs \Delta V_{Cs} \quad (5.45) \]

where

\[ D_1 T = D_3 T = \frac{T}{4} \]

Taking in account one of the two equations

\[ Cs = \frac{D_1 T (I_{minD1} + \frac{V_o}{4L_1} (1 - D_3) T)}{\Delta V_{Cs}} \quad (5.47) \]

\[ Cs = \frac{D_3 T I_{minD3}}{\Delta V_{Cs}} + \frac{D_1 V_o (1 - D_3)}{4f_{sw} L_1 \Delta V_{Cs}} \quad (5.48) \]

From Fig.5.3 at converter simulation efficiency \( \eta = 97\% \), the distance \( h = 0.142 \) A (opposite).

At \( \eta = 91\% \), \( h = 0.62 \) A.

Simulation shows that \( h \) distance increases with efficiency decreases. If we neglected \( I_{minD1} \) and replace it with zero since it is a small value, therefore, the minimum value of \( Cs \) can be generalized and expressed at balancing phases and full current sharing as

\[ Cs > \frac{D V_o (1 - D)}{4f_{sw} L \Delta V_{Cs}}, \quad (5.49) \]
or
\[ \frac{D^2 (1-D)}{4L f_{sw} V_{CS}} \]

For 1% of series capacitor voltage ripple \( \Delta V_{CS} \), voltage at \( C_s \) will be,
\[
V_{CS} = \frac{V_{in}}{2}, \text{ then}
\]
\[ \Delta V_{CS} = 0.55 \text{ V}, \text{ and the critical value of series capacitor of the two-phase converter will be}
\]
\[ C_s > 1.9 \mu F \]

The shape of the series capacitor current waveform is related to the other converter components and the converter efficiency, which is affected by the stored energy in the capacitor and the amount of charging and discharging every cycle of the period.

Inductors average voltage with parasites components:

\[
< v_{L1} > = D_1(v_{in} - v_{CS} - 2i_{L1} r_{on} - i_{L1} r_{CS}) + D_3(i_{L2} r_{on}) - i_{L1} r_{L1} - v_o + i_{L1} r_{on}
\]

\[
< v_{L2} > = D_3(v_{CS} - i_{L1} r_{on} - i_{L2} r_{on} + i_{L2} r_{CS}) + i_{L2} r_{on} - i_{L2} r_{L2} - v_o
\]

For ideal conditions

\[
< v_{L1} > = D_1(v_{in} - v_{CS}) - v_o = 0
\]

\[
< v_{L2} > = D_3(v_{CS}) - v_o = 0
\]

For current sharing equation (5.51) must equal equation (5.52), this gives the expression of the series capacitor in terms of topology parasitic values as follows,

\[
v_{CS} = V_{in} \frac{D_1}{D_1 + D_3} + \frac{i_{L1}(r_{on}(1+D_3-2D_1)-D_1 r_{CS}-r_{L1})+i_{L2}(2D_2 r_{on}+D_3 r_{CS}-r_{on}+r_{L2})}{D_1 + D_3}
\]

(5.53)
Fig. 5.4 shows typical waveform of main variables of 2-pscB converter. Table II depicted the 2-pscB converter design formulas:

\[ V_{L2}(t) \]
\[ V_{L1}(t) \]
\[ i_{G0}(t) \]
\[ i_{L1}(t) \]
\[ V_{C0}(t) \]

\[ D_1(v_{in} - i_{L1}r_{on} - i_{L1}r_{on} - i_{L1}r_{on}) \]
\[ D_2(v_{in} - v_{c0} - 2i_{L1}r_{on} - i_{L1}r_{on}) \]

\[ I_{C0\max} = \frac{1}{R + v_0}(R_i_{Lmax} - v_0 - \frac{\Delta v_0}{2}) \]
\[ I_{C0\min} = \frac{v_{in} + \frac{\Delta v_0}{2}}{L_i} \]

Fig. 5.4 The 2-pscB converter typical waveforms.
Table II The 2-pscB converter design formulas.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Interval</th>
<th>Mode Parameters</th>
<th>$i_{cs}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>$0 &lt; t &lt; d_1 T$</td>
<td>$v_{L_1}(t) = v_g - v_{cs} - v_o$</td>
<td>$i_{L_1}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$v_{L_2}(t) = -v_o$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$i_{L_1}(t) = L_1 I_{min_1} + \frac{(v_g - v_{cs} - v_o)}{L_1} t$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$i_{L_2}(t) = \frac{2}{3} I_{max_2} - \frac{v_o}{L_2} t$</td>
<td></td>
</tr>
<tr>
<td>II</td>
<td>$d_1 T &lt; t &lt; d_2 T$</td>
<td>$v_{L_1}(t) = -v_o$</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$v_{L_2}(t) = -v_o$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$i_{L_1}(t) = L_1 I_{max_1} - \frac{v_o (t - d_1 T)}{L_1}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$i_{L_2}(t) = \frac{1}{3} I_{max_2} - \frac{v_o (t - d_1 T)}{L_2}$</td>
<td></td>
</tr>
<tr>
<td>III</td>
<td>$d_2 T &lt; t &lt; d_3 T$</td>
<td>$v_{L_1}(t) = -v_o$</td>
<td>$-i_{L_2}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$v_{L_2}(t) = -v_o + v_{cs}$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$i_{L_1}(t) = \frac{2}{3} I_{max_1} - \frac{v_o}{L_1} (t - d_2 T)$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$i_{L_2}(t) = L_{min_2} + \frac{(-v_o + v_{cs})}{L_2} (t - d_2 T)$</td>
<td></td>
</tr>
<tr>
<td>IV</td>
<td>$d_3 T &lt; t &lt; T$</td>
<td>$v_{L_1}(t) = -v_o$</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$v_{L_2}(t) = -v_o$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$i_{L_1}(t) = \frac{1}{3} I_{max_1} - \frac{v_o}{L_1} (t - d_3 T)$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$i_{L_2}(t) = L_{max_2} - \frac{v_o}{L_2} (t - d_3 T)$</td>
<td></td>
</tr>
</tbody>
</table>
5.4 Comparison between Conventional Buck and 2-pscB Converter

The main benefit of the multiphase synchronous buck converter is the current ripple cancellation effect which enables the use of the small inductance to improve transient response, minimize the output capacitance, lower the cost of output capacitors, few components, and reduce the power dissipation. These benefits increase with increasing the switching frequency. On the other hand, switching losses increase with frequency, and as a result, efficiency tends to be lower, this effect can be reduced by multiplying the fundamental frequency in every phase used, which improves transient response [5.4].

The comparison between the conventional buck and the multi-phase series capacitor will increase the range of benefits to include complete current sharing, which is not applicable in conventional multiphase buck without additional current sensors.

5.4.1 Inductor Size Selection

For critical inductor of conventional buck converter which are previously calculated, where $d_B$ is duty cycle of conventional buck.

$$L_{cB} > \frac{(1-d_B)R}{2f_{sw}}$$ (5.54)

For critical inductor of two-phase series capacitor buck converter using equation (5.25)

$$L_{2pscB} > \frac{R}{5f_{sw}} (1 - 3D_1 + 2D_3)$$

At balance current sharing and same switching frequency

$$\frac{L_{cB}}{L_{2pscB}} = \frac{5(1-d_B)}{2(1-D)}$$ (5.55)
• At $D = d_B$, $L_{2pscB} = 0.4 L_{cB}$

That means the two-phase series capacitor buck converter will have 60% less inductor size of conventional buck at the same switching frequency, this reduction is vital since it increases the FOM of the converter as shown in Fig.5.5.

• Assuming $L_{cB} = L_{2pscB}$ this led to $d_B = 0.6 + 0.4 D$ e. g. $D = 0.3$ then $d_B = 0.72$

• At $d_B = 0.5$ and $D = 0.5d_B = 0.25$, $L_{2pscB} = 1.6 L_{cB}$

![Critical Inductor vs Duty cycle](image)

Fig.5.5 Conventional Buck inductor size vs 2-pscB.

5.4.2 Inductor Current Ripple

The reduction in the inductor current ripple of the series capacitor buck converter is especially noteworthy because it is related to the core loss of the inductor. As core losses increase with an increase in the switching frequency, that means it is also proportional to the inductor current ripple. Therefore, to reduce core losses, even small reductions in inductor current ripples can be helpful.

Hence, from equation (5.29), the ratio of current ripples is:
\[
\frac{\Delta i_{L,2pscB}}{\Delta i_{L,CB}} = \frac{5RT(1-D)-L}{6RT(1-d_B)}
\] (5.56)

- At \( D = d_B \), \( \Delta i_{L,2pscB} = 0.69 \Delta i_{L,CB} \)

That means the two-phase series capacitor buck converter will have 30\% less inductor current ripple than a conventional buck at the same switching frequency.

### 5.4.3 Output Capacitor Size Selection

To obtain the relationship between output capacitor size of both topologies

For 2-pscB using equation (5.37)

\[
C_{o2pscBCritical} = \frac{1}{96f_{sw}(\frac{\Delta V_o}{V_o})_{max}} \left( \frac{5}{L_{fsw}} (1 - D) - \frac{1}{R} \right)
\]

And for conventional buck

\[
C_{oCBCritical} = \frac{1}{8L_{fsw}^{2}(\frac{\Delta V_o}{V_o})_{max}} (1 - d_B)
\] (5.57)

Hence, the ratio of critical capacitor value at the same voltage conversion conditions is:

\[
\text{Critical Capacitor Ratio} = \frac{C_{o2pscBCritical}}{C_{oCBCritical}} = \frac{5R (1-D) - L_{fsw}}{12R(1-d_B)}
\] (5.58)

- At \( D = d_B = 0.25 \), \( C_{o2pscBCritical} = 0.347 C_{oCBCritical} \)

That means a two-phase series capacitor buck needs only 34\% of the capacitor size of conventional buck at the same switching frequency and inductor size; this reduction is vital since it increases the FOM of the converter as shown in Fig.5.6.
Since the inductor and output capacitor are both small in a 2-pscB converter, we are going to have a much higher circuit resonant frequency or breakpoint where $LC$ filter impedance is less.

$$\omega_o(2\text{pscB}) = \frac{2}{\sqrt{C_oL}}$$

or

$$\frac{\omega_o(2\text{pscB})}{\omega_o(cB)} = \sqrt{2}$$  \hspace{1cm} (5.59)

Also, at complete current sharing and same $LC$ filter values, quality factor has the same ratio.

$$Q_o(2\text{pscB}) = R \frac{\sqrt{2C_o}}{L} = \sqrt{2} Q_o(cB)$$  \hspace{1cm} (5.60)

We conclude that the cut-off frequency and quality factor of the 2-pscB converter are higher than the cut-off frequency and quality factor of the conventional buck converter.

One of the technical advantages of multi-phase is that the combined output ripple (total ripple) is
less than the ripple current in each inductor (phase ripple). This fact occurs due to driving the phases out of phase. In the case of 2-pscB converter, at interleaving the phases with a proper timing circuitry, ripple current reductions can be easily achieved even with improper current sharing since series capacitor voltage can compensate for the current difference with certain limits that results in much less output ripple [5.5].

Assuming all voltage ripples are caused by the pure capacitance of the output capacitor, to generalize the expression representing the output current ripple, the peak-to-peak value of the total output current ripple to be filtered by the output capacitor is:

\[
\Delta i_{L, CB} = \frac{v_o (1-d_B)}{L f_{sw}} N \frac{(D-m\frac{1}{N} - D)}{D(1-D)} \tag{5.61}
\]

Hence,

\[
\Delta i_{L, CB} = \frac{v_o}{L f_{sw}} \frac{(N*D-m)(m+1-N*D)}{N*D} \tag{5.62}
\]

Fig.5.7 Normalized output inductor ripple of conventional buck converter.
\[
\frac{m+1}{N} \geq D \geq \frac{m}{N}, N \geq m \geq 0 \quad (5.63)
\]

For a conventional buck, the combined inductor current ripple to be filtered by the main output capacitor \(C_o\) can be found by using the graph of Fig.5.7.

Fig.5.7 above shows the relationship between the duty cycle and the ratio of the total peak-to-peak ripple to the phase ripple of a conventional buck converter. At certain duty cycle values, there is a total cancellation of the ripple current. Those points are located where the conversion ratio \(v_{\text{in}}/v_o\) is equal to the ratio of the number of phases to any positive integer that is less than it. For example, in the case of a 4-phase regulator, at conversion ratios of 4:1, 4:2, and 4:3, the output ripple is zero. Remember duty cycle is approximately equal to \(v_o/v_{\text{in}}\), i.e., the reciprocal of the conversion ratio.

From equation (5.61) and using the same concept for 2-pscB converter, we conclude that, the peak-to-peak value of the total output current ripple to be filtered by the output capacitor is as follows:

\[
\Delta i_{L,2pscB} = \frac{v_o}{L_{fsw}} \frac{\left(\frac{d_1+d_3}{2d_1d_3} - 2\right)(d_3-d_2)}{d_1(d_2-d_1)} \left\{ \frac{N\left(d_1-\frac{m}{N}\right)(\frac{2m+1}{N} - 2d_1)}{d_4(d_2-d_1)} + \frac{N\left(d_3-\frac{m}{N}\right)(\frac{2m+1}{N} - 2d_3)}{(d_3-d_2)(1-d_3)} \right\} 
\]

(5.64)

This can be reduced to

\[
\Delta i_{L,2pscB} = \frac{v_o(1-2D)}{L_{fsw}} \left\{ \frac{N\left(D-\frac{m}{N}\right)(\frac{2m+1}{N} - 2D)}{D\left(\frac{1}{2}-D\right)} + \frac{N\left(D-\frac{m}{N}\right)(\frac{2m+1}{N} - 2D)}{D\left(\frac{1}{2}-D\right)} \right\} 
\]

(5.65)

\[
\Delta i_{L,2pscB} = \frac{v_o(1-2D)}{L_{fsw}} \left\{ \frac{2N\left(D-\frac{m}{N}\right)(\frac{2m+1}{N} - 2D)}{D(1-2D)} \right\} 
\]

(5.66)

Where \(K_{RCM} = \left\{ \frac{2N\left(D-\frac{m}{N}\right)(\frac{2m+1}{N} - 2D)}{D} \right\} = 2\left(1 - \frac{m}{N+D}\right)(2m + 1 - N \times 2D) \)

(5.67)

\[
K_{\text{norm}} = \frac{v_o}{L_{fsw}} 
\]

(5.68)
Then

\[ \Delta i_{L,2pscB} = K_{norm} \times K_{RCM} \]  \hspace{1cm} (5.69)

\( K_{RCM} \) is the output current ripple cancellation multiplier, \( N \) is the number of the phases, \( K_{norm} \) is a factor, \( D \) is duty cycle at complete current sharing, \( L \) is the inductor of each phase defined in equation (5.30),

\[ m = \text{floor} (N \times D) \]  \hspace{1cm} (5.70)

And the floor function returns the greatest integer value less than the argument.

The same concept for the 2-pscB converter, the relationship between the duty cycle and the ratio of the total peak-to-peak ripple to the phase ripple is shown in Fig.5.8. At certain duty cycle values,

![Graph showing normalized output inductor ripple for 2-pscB converter](image)

Fig.5.8 The 2-pscB converter approximated normalized output inductor ripple.

there is a total cancellation of the current ripple. Those cancellation points are located where the conversion ratio \( (v_{in}/v_o) \) is equal to the ratio of the number of phases to any positive integer that is less than it. For example, total ripple current cancellation for a 2-phase converter occurs beyond a
duty cycle of 0.25. In the case of a 4-phase regulator, this total ripple current cancellation occurs at a duty cycle of 0.125 and may be extended to 0.25 and 0.375. Remember duty cycle is approximately equal to \( v_o/v_{in} \), i.e., the reciprocal of the conversion ratio.

Note, since the two-phases of this topology are not symmetrical, it is not obvious whether this graph is applicable where this topology already has two phases, and the only way to add additional phases is by adding another series capacitor in every phase except the last phase, and mathematical calculations cannot reveal the nature of its work, more analysis could verify the formulas that introduced in this chapter.

### 5.5 Input Capacitor Selection

The input capacitor selection in the two-phase series capacitor buck is quite similar to the conventional buck converter, where the buck’s input current is discontinuous, \( Q_{11} \) is the only switch that turns on for a maximum quarter periodic time and turns off for the rest of time. Input capacitors are very important component for many reasons as:

- Reduce common mode noise in the system.
- Improve input line load transients.
- Reduce the natural variation of the duty cycle.

These duty variations are due to IC controller architecture and processors that may require different input voltages for the different operating modes.

In general, the difference between input and output capacitors is that output capacitors are not evenly distributed between each phase of input and concentrated in a small area of PCB, so you can see more reduction in output capacitance than the reduction of input capacitance [5.6].

The formula of average output current without power losses will be:
\[ I_o = \frac{(D_3+D_4)I_{in}}{D_3D_1} = \frac{P_o}{V_{in}} \frac{(D_3+D_4)}{D_3D_1} \]  
(5.71)

And input capacitor current is,

\[ I_{cin}(t) = \begin{cases} 
-\left(\frac{I_o}{2} - I_{in}\right) & 0 < t < D_1T \\
I_{in} & D_1T < t \leq T 
\end{cases} \]  
(5.72)

To evaluate charge balance on the input capacitor at complete current sharing yields

\[ \left(\frac{I_o}{2} - I_{in}\right) D = I_{in} \left(1 - D\right) \]  
(5.73)

At full load, the constantly changing current, and discharging generate heat in the input capacitor that can degrade its lifetime or even quickly destroy it. Heat losses can be estimated as follows:

\[ P_{cin} = I_{cin}^2 r_{cin}, \]  
(5.74)

To evaluate the peak-to-peak input capacitor voltage ripple at current sharing

\[ \Delta V_{cin_{p-p}} = \frac{\Delta q}{C_{in}} = \frac{I_{in}(1-D)T}{C_{in}} = \frac{I_oD(1-D)T}{2C_{in}} \]  
(5.75)

Or

\[ C_{in} \geq \frac{I_o D_{est} (1-D_{est})T}{2 \left(\Delta V_{cin_{p-p}}\right)} \]  
(5.76)

At estimated efficiency of less than 100\%, the estimated duty cycle in terms of efficiency is:

\[ D_{est} = 2 \frac{V_o}{V_{in} \eta} \]  
(5.77)

\( \eta \) is the efficiency, the maximum voltage ripple occurs at 25\% of duty cycle of \( D_{est} \)

Therefore,

\[ \Delta V_{cin_{p-p}} = \frac{3I_o T}{32C_{in}} \]  
(5.78)

Usually, a combination of aluminum and ceramic capacitors is selected for the input capacitors to detect the DC ripple at steady-state operation and should handle the RMS current ripple.
required by specifications. Large capacitors (bulk) can help to keep the input voltage within its AC limits. Like conventional buck converter the input capacitor current is:

\[ I_{C_{in}} = I_{in} - I_{Q_{1}} \]  \hspace{1cm} (5.79)

The input current RMS ripple can be calculated as follows.

\[ I_{C_{in-rms}} = \sqrt{\frac{1}{T} \int_{0}^{D_{1}T} \left( \frac{I_{o}}{2} - I_{in} \right)^{2} \, dt + \frac{1}{T} \int_{D_{1}T}^{T} (I_{in})^{2} \, dt} = \frac{I_{o}}{2} \sqrt{D_{1}(1 - D_{1})} \]  \hspace{1cm} (5.80)

\[ I_{o} \approx \langle I_{L} \rangle = 3.49 \text{ A} \]

At \( D_{3} = D_{1} \)

\[ I_{in} = \frac{D}{2} I_{o} = 0.44 \text{ A} \]

\[ I_{C_{in-rms}} = 0.755 \text{ A} \text{ (At resistive load of 4 }\Omega\text{)} \]

For a 2-pscB converter, input current ripple RMS value is less comparing with conventional buck. In the two-phase case, the magnitude of the input current ripple is half that of the single-phase solution because only phase A is carrying the load current. Of course, there is still one current pulse each clock cycle.

The graph in Fig.5.9 illustrates the difference between phases ripple in multiphase input capacitor ripple if we look at two-phase and three-phase, the required input RMS ripple current rating of the input capacitor bank is substantially reduced. Generally, as can be seen in the figure, more phases can get us less ripple RMS current, and more chances to hit zero ripple points. The zero ripple points happen at conversion ratios (\( \frac{V_{in}}{V_{o}} \)) that are equal to the number of phases divided by any positive integer (\( m \)) that is less than the number of phases. For example, for \( N=3 \), if \( V_{in} \) is 110 V and \( V_{o} \) is 12.1 V (i.e., the conversion ratio is 9), then the input ripple current is theoretically zero [5.6].
\[ I_{c_{\text{in-rms}}} = \frac{i_o}{2} \sqrt{\left( D - \frac{m}{N} \right) \left( \frac{m+1}{N} - D \right)} \] (5.81)

Fig. 5.9 Plot of 2-pscB converter normalized input capacitor RMS current versus duty cycle.

5.6 Ideal 2-pscB Converter Frequency Response

The step-down power conversion of the 2-pscB converter can be explained using a conceptual diagram of Fig. 5.9. This diagram consists of two functional blocks, the first is a single pole double throw (SPDT) complementary switch, and the second block is ILPF, where SPDT switches hold positions \( Q_{11}, Q_{21} \) for \( T_{on1}, T_{on2} \) and positions \( Q_{12}, Q_{22} \) for \( T_{off1}, T_{off2} \) respectively.

We define \( D_1 = \frac{T_{on1}}{T_s}, \quad D_3 = \frac{T_{on2}}{T_s}, \)

\[ D'_1 = \frac{T_{off1}}{T_s} = \frac{T_s - T_{on1}}{T_s} = 1 - D_1 \] (5.82)

\[ D'_3 = \frac{T_{off2}}{T_s} = \frac{T_s - T_{on2}}{T_s} = 1 - D_3 \] (5.83)
SPDT switches transform the input voltages $v_{in}$, $v_{Cs}$ into rectangular waveform $v_{SW1}$, $v_{SW2}$ respectively, then it is applied to ILPF.

For more analysis, we need to express Fourier series expansion (FS), since $v_{SW1}(t)$ and $v_{SW2}(t)$ are periodic functions at steady-state conditions, with period $T$ with a series of sinusoids, then for
phase A.

\[ v_{SW1}(t) = a_{1(0)} + \sum_{k=1}^{\infty} [a_{1(k)} \cos(k \omega_s t) + b_{1(k)} \cos(k \omega_s t)] \]  
(5.84)

Where \( \omega_s = \frac{2\pi}{T} \)

\[ v_{SW1}(t) = v_{SW1}(t \mp T) \]  
(5.85)

However, in any finite interval \( v_{SW1}(t) \) has at most a finite number of discontinuities and a finite number of maxima and minima,

\[ \int_0^T v_{SW1} dt < \infty \]  
(5.86)

The Fourier coefficients \( a_0, a_k \) and \( b_k \) are determined by the following equations.

\[ a_{1(0)} = \frac{1}{T} \int_0^{d_1 T} V_{SW1} dt = V_{SW1} D_1 \]  
(5.87)

\[ a_{1(k)} = \frac{2}{T} \int_0^{d_1 T} V_{SW1} \cos(k \omega_s t) \, dt = \frac{V_{SW1}}{\pi k} \sin(2\pi k D_1) \]  
(5.88)

At complete current sharing conditions \( D_1 = D_3 = 0.25 \)

\[ a_{1(k)} = \begin{cases} 
\frac{V_{SW1}}{\pi k} & \text{if } k = 1,5,9,\ldots \\
-\frac{V_{SW1}}{\pi k} & \text{if } k = 3,7,11,\ldots \\
0 & \text{if } k \text{ is even}
\end{cases} \]  
(5.89)

\[ b_{1(k)} = \frac{2}{T} \int_0^{d_1 T} V_{SW1} \sin(k \omega_s t) \, dt = \frac{V_{SW1}}{\pi k} [1 - \cos(2\pi k D_1)] \]  
(5.90)

At complete current sharing conditions

\[ b_{1(k)} = \begin{cases} 
\frac{V_{SW1}}{\pi k} & \text{if } k \text{ is odd} \\
2 \frac{V_{SW1}}{\pi k} & \text{if } k = 2,6,10,14,\ldots \\
0 & \text{if } k = 4,8,12,16,\ldots
\end{cases} \]  
(5.91)
For the lower phase

\[ v_{SW2}(t) = a_{2(0)} + \sum_{k=1}^{\infty} [a_{2(k)} \cos(k\omega_s t) + b_{2(k)} \cos(k\omega_s t)] \]  

(5.92)

Where,

\[ a_{2(0)} = \frac{1}{T} \int_{d_2T}^{d_3T} V_{SW2} \, dt = V_{SW2}D_3 \]  

(5.93)

\[ a_{2(k)} = \frac{2}{T} \int_{d_2T}^{d_3T} V_{SW2} \cos(k\omega_s t) \, dt = 2 \frac{V_{SW2}}{\pi k} \left[ \sin(\pi k D_3) \cos(\pi k (d_3 + d_2)) \right] \]  

(5.94)

At complete current sharing conditions

\[ a_{2(k)} = \begin{cases} 
- \frac{V_{SW1}}{\pi k} & \text{if } k = 1, 5, 9, \ldots \\
\frac{V_{SW1}}{\pi k} & \text{if } k = 3, 7, 11, \ldots \\
0 & \text{if } k \text{ is even}
\end{cases} \]  

(5.95)

\[ b_{2(k)} = \frac{2}{T} \int_{d_2T}^{d_3T} V_{SW2} \sin(k\omega_s t) \, dt = -2 \frac{V_{SW2}}{\pi k} \left[ \sin(\pi k D_3) \sin(\pi k (d_3 + d_2)) \right] \]  

(5.96)

Or

\[ b_{2(k)} = \begin{cases} 
2 \frac{V_{SW2}}{\pi k} & \text{if } k \text{ is odd} \\
2 \frac{V_{SW2}}{\pi k} & \text{if } k = 2, 6, 10, 14, \ldots \\
0 & \text{if } k = 4, 8, 12, 16, \ldots
\end{cases} \]  

(5.97)

\[ v_{SW1}(k) = \frac{1}{T} \int_{0}^{d_1T} V_{SW1} e^{-jk\omega_s t} \, dt = \frac{V_{SW1}}{\pi k} \sin(\pi k D_1) e^{-jk\pi D_1} \]  

\[ = V_{SW1} D_1 \text{sinc}(\pi k D_1) e^{-jk\pi D_1} \]  

(5.98)

\[ v_{SW2}(k) = \frac{1}{T} \int_{d_2T}^{d_3T} V_{SW2} e^{-jk\omega_s t} \, dt = \frac{V_{SW2}}{\pi k} \sin(\pi k D_3) e^{-jk\pi (d_3 + d_2)} \]
\[ V_{SW} = V_{SW2}D_3 \text{sinc}(k\pi D_3) e^{-jk\pi(d_3+d_2)} \]  

Fig. 5.11 shows the duty cycles spectrum of the 2-pscB converter using Fourier Series expansion. For practical cases, semiconductor devices cannot be turned on or turned off immediately. The actual representation will be the trapezoidal waveform, as shown in Fig. 5.12, which is close to the real switching node voltage waveform. To simplify the analysis, it is assumed that the rising time \( t_r \) and falling time \( t_f \) are equal for both phases. Therefore, the magnitude asymptote of equations (5.98), (5.99) will be a trapezoidal waveform that can be described as

Fig. 5.12 Switching voltage time-domain trapezoidal waveform.
\[ v_{SW1}(k) = V_{SW1}D_1 \text{sinc}(k \pi D_1) \text{sinc} \left( k \pi \frac{t}{T} \right) e^{-j k \pi D_1} \quad (5.100) \]

\[ v_{SW2}(k) = V_{SW2}D_3 \text{sinc}(k \pi D_3) \text{sinc} \left( k \pi \frac{t}{T} \right) e^{-j k \pi (d_3 + d_2)} \quad (5.101) \]

Where \( k = 1, 2, 3, \ldots \)

For this periodic signal, the Fourier exponential form can be represented as follows

\[ v_{SW1}(t) = \sum_{k=1}^{\infty} c_{k_1} e^{-j k \pi D_1}, \quad c_{k_1} = \sqrt{a_{1(k)}^2 + b_{1(k)}^2} \quad (5.102) \]

\[ v_{SW2}(t) = \sum_{k=1}^{\infty} c_{k_2} e^{-j k \pi (d_3 + d_2)}, \quad c_{k_2} = \sqrt{a_{2(k)}^2 + b_{2(k)}^2} \quad (5.103) \]

Where the exponential terms represent the signal phase or the value of displacements, according to the symmetry property of Fourier Series to draw an even function we need to shift it to the origin.

\[ f(t - t_o) \overset{\text{shifting}}{\longleftrightarrow} F(k) e^{-j k \pi t_o} \quad (5.104) \]

Or

\[ v_{SW1} \left( t - \frac{D_1}{2} T \right) \overset{\text{shifting}}{\longleftrightarrow} \quad v_{SW1}(k) e^{-j k \left( \frac{2\pi}{T} \frac{D_1}{2} T \right)} \quad (5.105) \]

\[ v_{SW2} \left( t - \frac{d_3 + d_2}{2} T \right) \overset{\text{shifting}}{\longleftrightarrow} \quad v_{SW2}(k) e^{-j k \left( \frac{2\pi}{T} \frac{d_3 + d_2}{2} T \right)} \quad (5.106) \]

Fig.5.13 shows the amplitude spectrum of the two-phases node switching voltage at complete current sharing conditions where node square voltage waves represented by sinc function spectrum at (N =101), also the phase spectrum for both signals and surf function that distinguish between them.
Fig. 5.13 Amplitude and phase spectrum of the two-phases node switching voltage at complete current sharing.

5.7 Multiphase Structure

Adding more phases to the 2-pscB converter is possible, this will introduce more division to the duty cycles. To test this possibility at complete current sharing conditions, switching voltages will be at the same values.

\[
D_1 V_{sw1} = D_3 V_{sw2}
\]

\[
D_1 (V_{in} - V_{cs}) = V_{cs} D_3
\]

\[
D_1 T < i_{L1} > = D_3 T < i_{L2} >
\]

Fig. 5.14 The 2-pscB converter node switching voltage.
Fig. 5.15 The 4-Phase series capacitor buck converter.

\[ V_{cs1} = \frac{3}{4} V_{in} \]

\[ V_{cs2} = \frac{1}{2} V_{cs1} \]

\[ V_{cs3} = \frac{1}{4} V_{cs2} \]

\[ V_{cs4} = \frac{1}{4} V_{cs3} \]

\[ V_{sw1} = (V_{in} - V_{cs1}) \]

\[ V_{sw2} = (V_{cs1} - V_{cs2}) \]

\[ V_{sw3} = (V_{cs2} - V_{cs3}) \]

\[ V_{sw4} = (V_{cs3}) \]

\[ V_{cs} = \frac{1}{2} V_{in} \]

These conditions can be generalized for multi-phase series capacitor buck converter. For \( n \) phases we can assume that

\[ V_{Csm} = \frac{n-m}{n} V_{in} \quad m=1,2,3...(n-1) \quad (5.107) \]

For four phase series capacitor buck converter topology (4-pscb) as seen in Fig.5.14 and Fig.5.15.

\[ D_a V_{sw1} = D_a (V_{in} - V_{cs1}) \]

\[ D_b V_{sw2} = D_b (V_{cs1} - V_{cs2}) \]

\[ D_c V_{sw3} = D_c (V_{cs2} - V_{cs3}) \]

\[ D_d V_{sw4} = D_d (V_{cs3}) \]

\[ V_{cs1} = \frac{3}{4} V_{in} \quad V_{cs2} = \frac{1}{2} V_{in} \quad V_{cs3} = \frac{1}{4} V_{in} \]
\[ V_o = \frac{1}{4}(D_a V_{sw1} + D_b V_{sw2} + D_c V_{sw3} + D_d V_{sw4}) \]

\[ V_o = \frac{1}{4}\left(\frac{D_a}{4} V_{in} + \frac{D_b}{4} V_{in} + \frac{D_c}{4} V_{in} + \frac{D_d}{4} V_{in}\right) \]

Or

\[ V_o = \frac{1}{n}\left(\frac{D_a}{n} V_{in} + \frac{D_b}{n} V_{in} + \frac{D_c}{n} V_{in} + \frac{D_d}{n} V_{in}\right) \quad (5.108) \]

If \( D = D_a = D_b = D_c = D_d \)

Then, for \( n \) phase, \( n = 1, 2, 3, \ldots \) And \( \frac{1}{n} > D > 0 \), \( L_1 \geq L_2 \geq L_3 \), \( L_{n-1} = L_n \)

\[ V_o = \frac{1}{n} D V_{in} \quad (5.109) \]

The output voltage will decrease gradually with phase number increases since every phase output switching voltage is divided by two. For 4-Phase series capacitor buck converter simulation

a) At \( L_1 = L_2 = L_3 = L_4 \) at 93% efficiency as seen in Fig. 5.16

![Diagram](image)

**Fig. 5.16.** The 4-Ph series capacitor buck converter at inductors equality a) losses b) current phases c) output voltage.
From Fig.5.16, we can see that the first phase draws the most transient current to charge the output capacitor and series capacitor, the last phase will balance the current of first phase.

b) At $L_1 > L_2 > L_3 = L_4$ at 94% efficiency in Fig.5.17

Fig.5.17. The 4-Ph series capacitor buck converter at inductors inequality a) losses b) current phases c) output voltage.

5.8 ZVS 2-pscB Converter Structure

In order to improve efficiency, a voltage regulator module (VRM) with interleaved phase-shifting can be regarded as a ZVS 2-pscB converter with a synchronous rectifier, operating at a constant frequency, as shown in Fig.5.18. Tanks are composed of inductor $L$ and MOSFET output capacitances $C_{DS}$, $Q_{11}$, $Q_{12}$ have approximately complementary gate drives, but with small delays inserted to allow the resonant transitions to occur. Since $Q_{21}$, $Q_{22}$ operates out of phase with phase A, therefore, there is a substantial cancellation of the input and output current ripples. To make sure resonance is working in parallel with the series capacitor voltage balancing mechanism, more
investigation is needed, where the inductor current ripple of the converter is greater than its DC components so that zero-voltage switching occurs.

![ZVS 2-pscB converter](image)

**Fig.5.18. ZVS 2-pscB converter.**

### 5.9 Summary

In this chapter, we began our analysis by obtaining the nominal plant transfer function of the 2-pscB converter. This allowed us to determine the control signal behavior required to properly identify the system parameters, then an equivalent circuit representation of different methods of current-mode control (CMC) is presented for the sake of easy understanding. The effect of the current loop is equivalent to controlling the inductor current as a current source with a certain amplifying impedance. With one control path and the reduction of sensor components, these control circuits representation provide both the simplicity of the circuit model and the accuracy of the proposed model.

Next, the new modeling approach can be extended in the same way to other CMC methods, such as Hysteretic control and $V^2$ current-mode control taking the advantage of improving transient
response and the current ripple cancellation effect, which enables the use of the small inductance in both converter phases and minimize the output capacitance.
5.10 References


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6 Chapter 6: Gate Driver Circuit Design.

6.1 Introduction to Gate Driver Design

The practical implementation of the 2-pscB converter is a challenging task due to the complexity of the PWM signal galvanic isolation design. The two conventional bootstrap structures, as shown in Fig.6.1(a)(b) [6.1] are unsuitable for higher input voltages ($V_{in} > 14V$), and bootstrap diodes isolation is not adequate to provide stability to gate driver reference voltage because voltage swing is common due to charging and discharging of the series capacitor between the phase A switches gate drivers.

Starting with Fig.6.1(a) configuration ($V_{in} < 14$ V) where bootstrap capacitors $C_1$ and $C_2$ are charged by a voltage difference between the driver source voltage $V_{dr}$ and the additional series capacitors voltage $V_{ci1}$, $V_{ci2}$ during the on-time of the SR low side switches $S_{R1}$, $S_{R2}$ through the bootstrap diodes $D_1$ and $D_2$ [6.2]. One of the drawbacks of this circuit is the gate voltages of the main switches $S_{m1}$, $S_{m2}$ which are not enough to maintain the continuity of gate pulses in a synchronous manner due to poor phase isolation and diodes losses, then for low input voltages,

Fig.6.1 The 2-pscB converter proposed gate driver circuits.
the gate driver is not isolated and protected from the positive voltage of the series capacitor when \( v_{Cs} > 12 \text{ V} \). Fig. 6.1(b) gives another proposed circuit when \( S_{R1} \) is energized \( C_1 \) is charged by the driver source \( V_{dr} \) through \( D_1 \). Also, during on-time of main switch \( S_{m2} \), the \( C_2 \) is charged by voltage \( V_{C3} \), which is equal \( V_{dr} \) through \( D_2 \), as a result, all gate voltages should be the same as source voltage \( V_{dr} \). This circuit still lacks gate isolation and protection from high voltages when \( v_{Cs} > 7 \text{ V} \).

The last circuit of Fig. 6.1(c) presents a 12 V two-phase buck converter with a fixed input rail to refresh the phase A bootstrap capacitor, to charge the bootstrap capacitor there is an external voltage supply diode connected between the converter input and the positive terminal of the series capacitor. Even if the high-side switch is not grounded, this connection should charge the bootstrap capacitor. But this idea obviously is unsuitable for charging because the diode is reversely biased and cannot withstand higher input voltage. The main disadvantages of the system in Fig. 6.1(c) are:

- Input voltage dependability works to interrupt the turning on the process of the high side switch, which may result in a weak gate voltage enhancement.
- Gate driver is not isolated nor protected from input voltage or series capacitor transient variation and spikes.
- The voltage across the bootstrap capacitor is reduced when the input voltage is low.
- The gate voltage level is varying according to the input voltage. As a result, this dependency affects the voltage level of the bootstrap capacitor and the synchronization of deadtime between phases.

Since adding a series capacitor (\( C_s \)) between two gate driver's ground terminals will introduce system unbalance and voltage reference mismatching, the high side gate drive must be connected separately with different reference ground point. It is confirmed that the series capacitor adds a
delay time to the high side gate drive due to the charging and discharging process every cycle. For this reason, high/low gate drives ground paths must be isolated completely where the gate power supply circuit for each gate side and base ground (source terminal of the switching device) isolated to prevent the effect of time delay and gate pulse PWM amplitude distortion.

To adjust the time delay ($DT$), another two double deadtime control circuits can be added to the circuit evaluation module. First circuit will be at the output of logic gates and the second circuit will be at the optocoupler output which can be adjusted separately for each phase due to the fact that series capacitor(s) is only added to one phase.

Two-phase delay time must be identical, there will be no current sharing if there is a mismatch between the gate driver triggering of the switches in the first phase and the gate driver triggering of the second phase. The current will increase in the phase with less power resistance (switching losses) where the multiplication of drain current and drain-source voltage is less, this will cause the current flow primarily in one inductor, which may increase the heat dissipation in one phase and may result in converter failure.

In General, the required switching speed of the switching device during turn-on and turn-off intervals must be as fast as possible to minimize switching power losses. Then, the gate driver device must be able to provide the required peak current for achieving the targeted switching speeds for the targeted power Si MOSFET / eGaN switch.

One of the possible techniques is to place the gate driver device very close to the power switch and design a tight gate drive-loop with minimal PCB trace inductance, this also shall reduce the EMI in voltage switching nodes. The full peak-current capability of the gate driver is an important factor that must be calculated before calculating the parasitic components.
Fig. 6.2. The Si8275 gate drive in Half-Bridge Application and Si8275 EVM gate drive layout.

As seen in Fig. 6.2, Si827x series, which are 4 Amp ISO-driver with high transient \((dV/dt)\) immunity from Silicon Labs is a good choice [6.3]. Since these drivers are configured as isolated dual drivers and Si8275 configured as an isolated dual driver, that makes them favorable and applicable for project designing. In this case, the drain voltages of \(Q_1\) and \(Q_2\) are referenced to a common ground or different grounds with as much as 1500 \(V_{dc}\) isolation barrier between them. Therefore, the voltage at the \(VOA\) side can be higher or lower than that of the \(VOB\) side by \(VDD\) without damaging the driver. \(VDD\) is normally in the range of 2.5 \(V\) to 5.5 \(V\), while the \(VDDA\) and \(VDDB\) output side supplies must be between 4.2 \(V\) and 30 \(V\) with respect to their respective grounds. As specified from the datasheet, a dual low-side or dual high-side driver is unaffected by static or dynamic voltage polarity changes [6.4].

### 6.2 Isolated Si MOSFET Gate Driver Circuit

A new isolated gate driver circuit using a \(UCC27531\) gate driver to accommodate adding a series capacitor between switches \(Q_{11}\) and \(Q_{12}\) of phase A is proposed [6.5].
Fig. 6.3 Typical Si MOSFET isolated circuit of switch $Q_{11}$ with UCC27531 gate driver.

Fig. 6.3 shows the circuit configuration of the proposed isolated gate driver. The gate reference voltage for the isolated high-side switch is the positive side of $C_s$, whereas the gate voltage for the low-side switch circuit requires a different isolation loop since its reference voltage is ground. As such, an isolation scheme must encompass the entire high-side switch circuit because inserting a series capacitor will introduce a time delay between the gate voltages of the two switches. This series capacitor voltage interferes with the synchronization of the switching time and voltage level.

Isolation is required to isolate the ground loops; this means there should be no direct conduction path between the high side driver and the synchronous rectifier switch driver (lower side) of the phase A circuit due to the voltage storage element of $C_s$ in between. The anode of bootstrap diodes $D_{Bstrap1}$ is commonly connected to a driver source $V_{DD}$. Therefore, bootstrap capacitors $C_5$ to $C_8$ are charged by a voltage difference between the driver source voltage $V_{DD}$ and the series capacitor voltage $v_{C_S}$ during the on times of the $Q_{12}$ switch through the bootstrap diode $D_{Bstrap1}$. Since the four bootstraps diodes are isolated using an isolated DC source, the gate voltages
of the main switches $Q_{11}$ and $Q_{21}$ are enough to charge the bootstraps capacitors. As such, phase B uses the same gate drivers as phase A. To reduce the cost of the four matched bootstrap capacitors for each gate driver, $C_5$ to $C_8$, two of them can be eliminated. The gate driver should be located as close to the MOSFETs as possible. Gate drivers must be single, non-isolated dual-gate drivers cannot be used in this gate driving circuit.

The main goal of traditional isolation is to separate data signal from power traces and be capable to block the large common-mode voltages between the switch and controller, for this purpose, there are many galvanic isolation methodologies to achieve that like capacitive, transformer (magnetic) for digital isolation, and traditional optocoupler isolation. Choosing the suitable optocoupler method is subject to simplicity and the ability to provide a good barrier to prevent DC current from flowing from one side to the other. Some disadvantages of this type of isolation are mainly low speed and high-power consumption, using 6N136 of 10 MBd optocoupler.
can be improved up to 50 MBd. This circuit contains 4 bootstrap diodes at the output terminals of the isolated power supply transformer. There are two ways to adjust the deadtime between the high side signal and the low side signal one by adding a resistor at gate driver input connected to the PWM signal, the other way is by using a resistor at the optocoupler input. The converter PCB layout is shown in Appendix E. The self-resistance calculation is done using Autodesk Eagle software see Fig.6.4. For a Copper thickness of 1 oz the wire layout parameters are shown. The PCB circuit is consisting of one input supply 12V with EMI choke circuit and Fly-back Converter to supply four isolated 18V for four gate drivers. The proposed power supply circuit layout of the MOSFET gate drive, phase B is shown in Fig.6.5. The auxiliary power supply includes a Fly-back circuit used in prototypes testing, as shown in Fig.6.6.

Fig.6.5 Phase B schematic diagram with power supply circuit.

To calculate the trace width for printed circuit board conductors, for a given current using formulas from IPC-2221

\[ I_{\text{trace}} = k \Delta T^{0.44} A^{0.725} \]  

(6.1)
Where \( \Delta T \) = temperature rise in \( (^\circ C) \), \( I \) = current in amperes (A), \( A \) = cross section in (mil\(^2\)), outer layer factor \( k = 0.048 \).

Temperature rise is defined as the difference between the maximum safe operating temperature of PCB laminate material and the maximum temperature of the thermal environment that PCB is subject to. Power dissipation of the components is the main reason for temperature rising, but since we use only 2-layer PCB, there is no major concern.

Using 2 oz/ft\(^2\) of copper and output current limit \( I_{trace} = 5 \) A

A copper Thickness of 1 oz/ft\(^2\) = 1.37 mil

Assume Temperature rise = 20 \( ^\circ C \)
Area \([\text{mils}^2]\) = \frac{\text{Current [Amps]}}{(k(\text{Temp}_\text{Rise [deg. C]})^b)^{1/c}}

= 100 \text{mils}^2

where \(b = 0.44, c = 0.725\) constants resulted from curve fitting to the IPC-2221 curves

Width[\text{mils}] = \frac{\text{Area[\text{mils}^2]}}{\text{Thickness[oz]} \times 1.378[\text{mils/oz}]}

= 35.5 \text{mil}

### 6.2.1 Experimental Prototype Circuit

For the PCB layout, as seen in Appendix E, choosing a width of 40 \text{mils} is enough for the power traces. In compliance with IPC-2221 standards \([6.6], [6.7]\), the rule thumb for moderate temperature rise (less than 30\degree C) and currents less than 5A: Using at least 7 \text{mils} width of copper per ampere for 2 oz board is enough. The trace resistance is 0.00288 \Omega/cm and drop voltage almost 0.0144 V/cm with power losses 0.072 W/cm. Traces parasitic inductance formula is:

\[
L_{\text{trace}} = 2 \times l \left( \ln \frac{2l}{w} - 0.5 + 0.2235 \frac{w}{l} \right) nH
\]

Where length \((l)\) and width \((w)\) dimensions are in centimeters and parasitic inductance is in \(nH\).

For PCB trace length of 2.54 \text{cm} and 40 \text{mils} width, the parasitic inductance for one inch of PCB trace is almost 8 \(nH\), which is still below the limitation of 20 \(nH\). The thickness of the copper trace has little effect on the value of the parasitic inductance. For a single via of a standard 1.6 \text{mm} board thickness and 0.4 \text{mm} diameter, parasitic inductance is about 1.2 \(nH\).

\[
L_{\text{via}} = \frac{\text{height}}{5} \left( 1 + \ln \frac{4 \times \text{height}}{\text{diameter}} \right) nH
\]
Varying the parasitic inductances affects the current sharing but the internal mechanism of the series capacitor can compensate for the difference within a certain limit. Eagle software can display some basic information on each trace of the PCB, including the maximum theoretical current you can draw from these traces.

Using two series capacitors \( C_{S1}, C_{S2} \) in parallel will reduce the parasitic resistance \( r_{Cs} \) to half. Two Aluminum electrolytic capacitors of 4.5 \( \mu F \) were chosen with dissipation factor \( (\tan\delta = 0.3) \), thus, the total ESR of parallel capacitors will be

\[
ESR = \frac{\tan\delta}{2 \omega C} = 0.02 \Omega \quad \text{at } 250 \text{ kHz}
\]

(6.6)

<table>
<thead>
<tr>
<th>Component</th>
<th>Abbri.</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Series Capacitor</strong></td>
<td>Cs</td>
<td>9 ( \mu F )</td>
</tr>
<tr>
<td><strong>Phase Inductors</strong></td>
<td>( L_1 ) &amp; ( L_2 )</td>
<td>10 ( \mu H )</td>
</tr>
<tr>
<td><strong>Output Capacitor</strong></td>
<td>Co</td>
<td>&gt;80 ( \mu F )</td>
</tr>
<tr>
<td><strong>Switching Frequency</strong></td>
<td>( F_{sw} )</td>
<td>250kHz</td>
</tr>
<tr>
<td><strong>Input Voltage</strong></td>
<td>( V_{in} )</td>
<td>110V</td>
</tr>
<tr>
<td><strong>Output Voltage</strong></td>
<td>( V_o )</td>
<td>12.5V-13.5V</td>
</tr>
<tr>
<td><strong>Stray Components</strong></td>
<td>( r_{Cs} )</td>
<td>20m( \Omega )</td>
</tr>
<tr>
<td><strong>Stray Components</strong></td>
<td>( r_{on}, r_{L1}, r_{L2} )</td>
<td>&lt; 20m( \Omega )</td>
</tr>
<tr>
<td><strong>Output Power</strong></td>
<td>( P_o )</td>
<td>&lt; 75W</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MOSFET</th>
<th>Ciss</th>
<th>( V_{DS} )</th>
<th>( R_{DS(on)} )</th>
<th>( I_D )</th>
</tr>
</thead>
<tbody>
<tr>
<td>IPB530N15N3</td>
<td>667 pF</td>
<td>150 V</td>
<td>53 m( \Omega )</td>
<td>21 A</td>
</tr>
<tr>
<td>si7898(Fly-back)</td>
<td>900 pF</td>
<td>150 V</td>
<td>85 m( \Omega )</td>
<td>4.8 A</td>
</tr>
</tbody>
</table>

TABLE III: 2-pscB Conv. Experimental Evaluation Parameters

TABLE IV: 2-pscB Converter Si MOSFETs
One drawback of Aluminum electrolytic capacitors that may affect their performance is their large leakage current (DC leakage), while ceramic, foil, and plastic film capacitors have small leakage currents. There is a very small leakage current commonly referred to as “insulation resistance”, which mainly depends on terminal voltage, capacitor temperature, and charging time.

Fig. 6.7 Phase A current sink loops (a) top switch, and (b) bottom switch.

Two ERU(16) helically-wound choke inductors are used for both phases with DCR of 3.7 mΩ and a current saturation setting of 18.3 A. Since this topology is still not fully implemented for voltage levels higher than 12V, two prototypes were built to examine the automatic current sharing mechanism of a 2-pscB converter at a voltage of 110 V/12 Vdc the working parameters are listed in Table III, the first prototype that was made includes designing a new isolated MOSFET gate
driver layout using a *UCC27531* gate drive to accommodate adding a series capacitor between switches of the first phase. Both MOSFETs used for 2-pscB and the one used for the Fly-back power supply converter are shown in Table IV [6.8]. The gate drivers should be designed to be closely attached to the MOSFETs to minimize the distance between the driver and the gate. In this way, self-inductance and the self-resistance of the traces will be reduced, then the EMI and voltage spikes of the circuit will be minimized. There are two ways to adjust deadtime provided to the prototypes between the high side signal and the lower side signal.

For complete current sharing, deadtime must be the same for both phases. In general, separate gate drivers and input signals allow accurate deadtime management. Current sink loops are not similar for both phases the \(dV/dt\) occurs on the MOSFET drain when the MOSFET is already held in the OFF state by the gate driver. The current charging the CGD Miller capacitance during this high \(dV/dt\) is shunted by the pull-down stage of the driver. If the pull-down impedance is not low enough then a voltage spike can result in the \(V_{GS}\) of the MOSFET as Fig.6.8, EN continuous voltage is in the limit of 5 V.

This circuit contains 4 bootstraps diodes at the output terminals of the power supply Fly-back converter transformer, this Fly-back converter is used to supply four isolated 18V for gate drives at frequency 323 kHz as seen in Fig.6.8. In this circuit, there is a tendency to avoid extra “band-aid” circuitry like snubbers since the external Schottky diode clamps may be eliminated because of the presence of the MOSFET body diodes offers low impedance to switching overshoots and undershoots. The feedback resistor \(R_{FB}\) is connected to the transformer primary side at the external MOSFET switch device (si7898). The average current through this resistor during the Fly-back period should be approximately 200 \(\mu A\). The ratio of this resistor to the \(R_{REF}\) resistor that
connected to pin 14, times the internal bandgap reference, determines the output voltage. The resistor should be attached as close to the \textit{LT3748} chip as possible [6.9].

The input signal of the experimental prototype (\textit{D_{Drive}}) is either one 5V PWM signal of twice switching frequency and doubled duty cycle or two 5V PWM signals, as shown in Fig.6.9.

![Fig.6.8: Fly-back gate driver signal, \(V_{GS}\), (top waveform) and drain source voltage, \(V_{DS}\), (bottom waveform) at the transformer input.](image)

![Fig. 6.9. 5V PWM signal of twice switching frequency and doubled duty cycle.](image)
This D-flipflop based circuit implements a non-overlapping two-phase clock signal generator and can be used to derive a two-phase clock signal from a single and possibly non-symmetrical clock signal. For option one, the input signal ($D_{\text{Drive}}$) and phase A generated gate driver signals are as shown in Fig.6.10.

![Waveform Diagram](image)

**Fig.6.10:** Input PWM signal, $D_{\text{Drive}}$, (top waveform) and the gate-source voltages of $Q_{11}$ and $Q_{12}$ (bottom waveforms).

The measured rising time $t_r = (9-13)$ ns, falling time of $t_f = (6 - 7.4)$ ns, at overshooting of 9 % which implies that $I_{\text{source}} = (1-0.67)$ A and $I_{\text{sink}} = (1.45-1.17)$ A. The input PWM signal will be at 500 $kHz$ of 50% duty or less to generate four signals at 250 $kHz$ of 25% duty cycle or less. As such, controlling the four gate signals becomes easier and can be done with only the main input PWM signal. Signal delay time between the optocoupler input and IPB530N15N3 gate is measured at 170$ns$, which includes the rise and first propagation time, the time delay is 57 $ns$ for the fall time and second propagation time together Fig.6.11. The difference represents traces delay, which can
be reduced with enhanced PCB layout and include a multilayer structure to separate power traces from the ground. Improving optocoupler speed up to 50 MBd is a good option to reduce propagation delay since LED needs time to get powered and emits light onto a phototransistor, this will make the phototransistor conduct and change the voltage on the output side, the LED’s

![Signal delay](image)

**Fig.6.11.** Signal delay between the optocoupler PWM input signal and the gate-source voltage of $Q_{11}$.

intensity can degrade resulting in slower performance. Magnetic isolation “transformer” is the best alternative, this improves speed and power consumption at low speeds, especially at low electromagnetic fields. In modern designs, capacitive isolation become more popular in many applications that require no sensitivity to magnetic fields. To achieve the required $dV/dt$, gate drivers must provide $Q_{GD}$ in 20 $ns$ or less, that means ($I_G = 3 \, nC/20ns = 0.15A$ ) or higher but MOSFET gate-source current reaches 1.2 A and the sink current is less ($Q_{GD} = 3 \, nC$ maximum),

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\( dV_{DS}/dt = 20 \, V/ns \) as shown in Fig.6.12 which is almost similar to the simulated gate current value for \( R_{G(on)(ext.)} = 2 \, \Omega \), \( R_{G(off)(ext.)} = 0 \), see Fig.4.11(d). Turn on and turn off driver voltage should be symmetrical, which means the sink current path impedance and voltage drop must be minimized also, separate source and sink current transistors within the gate driver allow for separating drive paths.

![Gate-source voltages waveform](image)

Fig.6.12: Gate-source voltages of \( Q_{12} \) measured before gate resistor \( R_G \) (top waveform), and after \( R_G \) (bottom waveform).

Fig.6.13 shows the second phase MOSFET \( Q_{21} \) typical characteristic waveform of \( V_{DS} \) versus \( V_{GS} \) when \( V_{in} \) equals 110V. The high overshooting voltage at the rising edge is related to the input loop, input capacitor location when this can cause extra-inductance at input loop in addition to other causes like using long leads for voltage measurements, whereas the undershoot at the falling edge is related to the low side MOSFET parasitic inductances or bonding wires and lead frames, the best measurements are the ones performed at highest load and bandwidth setting.
Fig. 6.13: Second phase MOSFET $Q_{21}$ typical waveform of $V_{DS}$ verses $V_{GS}$.

Fig. 6.14: Gate pulses of $Q_{11}$ (top waveform) and $V_{SW1}, V_{SW2}$ at 250 kHz (bottom waveforms).
Fig. 6.14 shows the nodes’ voltages $V_{SW1}$ and $V_{SW2}$ at a switching frequency of 250 kHz. As can be seen, these node voltages have a variation of within 0.5 V. As stated earlier, these node voltages must be the same at fully current sharing. Any difference or a small variation can be caused by deadtime, trace width, and length unbalance of the two-phase paths, or it can be the result of switching speed due to the different charging and discharging times for the MOSFETs input capacitors ($C_{GS}$). Since the switch node voltages slope is caused by the load current, as such, the slope of $V_{SW1}$ is affected by the charging period of both $C_s$ and $C_o$. This is because $V_{SW2}$ charges only $C_o$, then a slope difference can be seen. To eliminate this difference, the value of $C_s$ must be chosen carefully in terms of inductance variations, zero dc bias inductance, saturation profiles, converter layout, and $C_s$ position. Fig. 6.15 shows the discharge period of the series capacitor for load $R = 4.5 \Omega$, thus, for 1 $\mu$s the series capacitor voltage ($V_{SW2}$) decreases to 53.46 V, and the

![Capacitor Discharge Calculation](image)

Fig. 6.15  Discharging behavior of series capacitor ($V_{SW2}$) at $V_{Cs} = 54.8$ V.
Fig. 6.16: Experimental prototype efficiency at 92% and 3.38 A ($I_{in}$, $I_{out}$, $V_{out}$).

Fig. 6.17: The 2-pscB converter series capacitor current waveform (below).

released charge is about 481 µC [6.10]. The maximum efficiency achieved from the experimental
prototype is 93% at 3.38 A of load, see Fig.6.16 where input capacitor current is 442 mA despite the noticed peak-to-peak ripple of about 270 mA due to charging and discharging of both $C_S$ and $C_O$. This proves one of the drawbacks of the 2-pscB converters where the input ripple is worsened due to introducing a series capacitor within the converter. Converter series capacitor current waveform is shown in Fig.6.17. This waveform has been captured with a voltage differential probe, not by current measurement means. Fig.6.18 shows the series capacitor current, $i_{CS}$, and inductor currents, $i_{L1}$ and $i_{L2}$, at a resistive load current of 2.4 A, respectively.

The phase A inductor current ($i_{L1}$) has a slightly higher peak-to-peak ripple, due possibly to slope difference and converter layout parasitic inductance. Experimental prototypes are shown in Fig.6.19. The maximum output power of 73W was achieved from measured efficiency at 91% that can be gained from a full load of 6 A. Prototype efficiency results versus $LTspice$ simulation are illustrated in Fig.6.20.

![Fig.6.18. Inductor currents, $I_{L1}$ and $I_{L2}$, at a load current of 2.4 A.](image-url)
Fig. 6.19: 110 V/12 V Experimental prototypes version 1&2.

Fig. 6.20. Simulation efficiency vs experimental efficiency and related power dissipation curves.
Fig. 6.21 Thermal distribution of Si MOSFET prototype a) at no load b) at $V_{in} = 110$ V and efficiency of 93%.

From Fig.6.21 (a) we noticed that heat is not evenly distributed over PCB layout and temperature of $Q_{11}$ of gate driver reached up to $52^\circ C$ at standby time, this might be due to the complete isolation and charging period of capacitor $C_3$ and $C_2$, [ see Fig.6.3]. The temperature of phase A switches and series capacitors reached $77.4^\circ C$ at an efficiency of 93%, as shown in Fig.6.21(b), which is quite normal. The direct cause of the temperature rising, and the heat generated by the gate driver MOSFETs is due to the existence of the series capacitor current ripple of charging every cycle. To improve the heat distribution, much care needs to be done in terms of parts distribution and PCB layout.

6.2.2 Discussion and Conclusion:

Due to PCB traces drop voltage and two phases layout mismatch, there is an expected variation between simulation and measured efficiency results, wires, and device measurements parasitic noise also have a negative impact on results. Dissipation curves show a normal rising along with
the load. Although there is a small trace resistive unbalance between the two phases, the current sharing mechanism is still functioning for the PCB layout. Almost 1V switching node $V_{SW2}$ reduction is noticed in the second phase. Otherwise, losses are very low when the current sharing condition is completely fulfilled, and complete heat distribution is achieved.

Using only one PWM signal input may give an advantage for a close loop circuit and simplify the control scheme where the control loop frequency and duty cycle should be twice the actual switching frequency and duty cycle of the 2-psCB converter. Since the main switches of both phases are driven with a 180-degree phase shift and with a duty ratio of less than 50%, a Push-Pull controller can be implemented which has a large achievable duty cycle range. The other two MOSFETs of synchronous rectifier switches (lower side) are just complementary switches.

It is worth mentioning, the physical phase current running loop, per Ampere’s law, will form a magnetic field in proportion to the shared current and the phase loop area, this field could then couple with other circuit loops such as control circuit, per Faraday’s law, with more coupling at higher frequencies, resulting in harmful crosstalk but this is not the case of this topology since the first and the third mode current loops are nearly opposite in direction, and the field will be canceled out. A further investigation will be conducted to cover this phenomenon.

The maximum charging time, transient period, and the amount of charge in the series capacitor $C_s$ can be adjusted by adding an extra control circuit that can gradually limit the inrush current caused by the series capacitance charging period at the main switch $Q_{11}$. In addition to the output capacitor charging period at the beginning of transient time, this inrush current can cause damage to the first switch for a long period. This additional control circuit can be accomplished by adding bypass charging time to charge the series capacitor before energizing the first switch. This pre-
charging circuit will be energized before the main converter circuit by a certain time that can be calculated as follows:

\[
t_{pc} = \frac{Q}{I_{pc}} = \frac{C_s V_{cs}}{I_{pc}}
\]  

(6.7)

Where \( Q \) is the total capacitor charge, for half input voltage of \( V_{cs} \), charging current \( (I_{pc}) \) of 20 mA and 9 \( \mu \)F series capacitor size. Thus, pre-charging delay time is:

\[
t_{pc} = 24.7 \text{ ms}
\]

The larger series capacitor results in a longer pre-charge delay which will increase the drawbacks of series capacitor converter topologies.

\[
V_{cs} = V_{in} \left( 1 - e^{-\frac{-t_{pc}}{R_{pc}C_s}} \right)
\]  

(6.8)

For half input voltage,

\[
e^{-\frac{-t_{pc}}{R_{pc}C_s}} = 0.5 \quad \text{In another word, for design specifications } R_{pc} = 3.7 \text{ k}\Omega
\]

During the Lab work, using long ground leads with the oscilloscope generates more noise, the high-frequency components of the common mode noise can be radiated and coupled to the oscilloscope grounding clip. Common-mode noise can produce high-voltage spikes, but the best results can be obtained when a suitable coaxial connector with low inductance is used. Removing the long grounding cable of the probe and adding a short connector to the output terminals of the converter is a good way to measure the ripple. There are many techniques to reduce the output voltage ripple, such as using extra capacitors with low ESR, extra LC filters, and common-mode
chokes. Since the converter input capacitor current and the four switches are discontinuous, therefore they may generate a significant EMI.

Dividing the 2-pscB converter layout into two areas, the red loop area should be as small as possible with low inductance, as seen in Fig. 6.22. The blue loop area has to be larger than the red area since it does not generate a lot of EMI. On the other hand, the non-shielded or semi-shielded output inductors emit a considerable high-frequency magnetic field which can induce interfering switching voltages in nearby loops. In other words, sensitive loops should be kept away from the inductors. For double layer board design, the high current loops need to be kept on the top side and place the input capacitor as close as possible to the chip controller and ground layout this

![Diagram of 2-pscB converter layout](image)

Fig. 6.22. EMI loop areas of 2-pscB converter.

ensures the smallest input loop. Inductors of the two phases need to be placed close to the voltage switching nodes to minimize the switching node area. Eddy currents can increase the stray field of inductors, one way to minimize it is by removing the copper directly beneath the inductors. Small signal components need to be placed away from switching loops. The bottom ground plane should be connected to the controller chip thermal pad through vias. It is highly recommended to add bigger electrolytic capacitors at the input terminals to avoid resonances and hot-plug spikes due to
long input wires. The \( R_2 \) resistor at the input of 6N137 optocoupler, as shown in Fig.6.3 this resistor can be calculated as follows:

\[
I_F = 40 \ mA, \ V_F = 1.3 \ V
\]

\[
R_2 = \frac{5 - 1.3}{0.04} = 93 \ \Omega ,
\]

The value \( R_2 \) of 100 \( \Omega \) will be used for the high side gate driver and 470 \( \Omega \) for the lower side gate driver. For maximum gate charge at \( V_{GS} = 15.5 \ V \) losses dissipated in the \( R_G \) of each (IPB530N15N30) MOSFET with typical internal gate resistor of 2.1 \( \Omega \), according to Fig.6.23

\[
P_G = Q_{G(max)} V_{GS} F_{sw} \quad (6.9)
\]

\[
= 12 \ nC \times 15.5 \ V \times 250kHz = 47 \ mW
\]

Where,

\[
Q_G = Q_{GS} + Q_{GD} + Q_{GS} = 12 \ nC \quad (6.10)
\]

Since choosing bigger \( R_G \) cause more switching delay, it is recommended to use smaller sizes,

\[
R_{G-on} = \frac{V_G}{I_{peak(source)}} = \frac{15.5}{2.5} \quad (6.11)
\]

\[
= 6.2 \ \Omega \quad \text{at source current of 2.5 A, choosing } R_{G-on(external)} = 2 \ \Omega
\]

\[
R_{G-off} = \frac{V_G}{I_{peak(sink)}} = \frac{15.5}{5} \quad (6.12)
\]

\[
= 3.1 \ \Omega \quad \text{at sink current of 5 A, choosing } R_{G-off(external)} = 0 \ \Omega
\]
Fig. 6.23 $V_{GS} = f(Q_{gate})$; $I_D = 18$ A pulsed.

\[ R_G = R_{G-(int.)} + R_{G-(ext.)} \]  \hspace{1cm} (6.13)

Because the series capacitor acts as a dc voltage source ($v_{Cs} = v_{in}/2$), the drain-to-source voltage during switching is half of that experienced in a buck converter. This applies to all switches during both on-time and off-time transitions in the 2-pscB converter also, reduces the loss results of the overlap of switch current and voltage. A simple model for estimating this energy loss component is:

\[ E_{sw} = \frac{V_{DS}I_D}{2} (t_r + t_f) \]  \hspace{1cm} (6.14)

where $V_{DS}$ is the drain-to-source blocking voltage, $I_D$ is the current conducted at on-time of the switch, $t_r$ is the current rise time, and $t_f$ is the voltage fall time during high-side switch on-time.
The two-phase series capacitor buck topology reduces this loss by approximately half. More detailed switching loss models can be applied for greater accuracy if desired [6.11-6.13].

6.3 The Isolated eGaN Gate Driver Circuit

A new isolated gate driver circuit using UCC27611 gate drivers, from TI, to accommodate adding a energy storage between switches $Q_{11}$ and $Q_{12}$ of phase A is proposed in this section. Different approach for low voltage is discussed and experimentally verified.

6.3.1 Sensor-less eGaN Gate Driver Circuit

The specifications for the sensor-less eGaN-based 48V/5Vdc 2-pscB converter are listed in Table V. Fig. 6.24(a) shows the two-phase pulses to trigger $Q_{11}$ and $Q_{21}$. As seen in Fig. 6.24(b), the average $v_{Cs}$ maintained its value at exactly half of the input voltage with a voltage ripple of less than 0.5 V. The output filter value influenced the output voltage ripple. The average charging and discharging currents for the series capacitor are similar, as shown in Fig. 6.23(c), this verifies the steady-state operation of the 2-pscB converter. Fig. 6.24(d) shows the inductor currents $i_{L1}$ and $i_{L2}$.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Abbri.</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Series Capacitor</td>
<td>$Cs$</td>
<td>$&lt;4.7\mu F$</td>
</tr>
<tr>
<td>Phase Inductors</td>
<td>$L_1 &amp; L_2$</td>
<td>$4.7\mu H$</td>
</tr>
<tr>
<td>Output Capacitor</td>
<td>$Co$</td>
<td>$&gt;70\mu F$</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$F_{SW}$</td>
<td>$250kHz$</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>$V_{in}$</td>
<td>$48V$</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_o$</td>
<td>$5V$</td>
</tr>
<tr>
<td>Stray Components</td>
<td>$r_{Cs}$</td>
<td>$10m\Omega$</td>
</tr>
<tr>
<td>Stray Components</td>
<td>$r_{on},r_{L1},r_{L2}$</td>
<td>$&lt;20m\Omega$</td>
</tr>
<tr>
<td>Output Power</td>
<td>$P_o$</td>
<td>$&lt;45W$</td>
</tr>
</tbody>
</table>

Table V: 2-pscB Converter Experimental Evaluation Parameters
which have identical magnitudes and are 180° out of phase in steady-state operation. If converter inductors currents are unbalanced, the capacitor voltages would charge to balance the inductor currents automatically. The total average output inductor current is the sum of both the average phase-inductor currents.

![Diagram](image_url)

Fig.6.24. The 2-pscB converter waveforms (a) two phase pulses, (b) series capacitor voltage, (c) series capacitor current, and (d) two phase inductor currents (e) output current and voltage.

Fig.6.24(c) shows the output voltage and current values. Fig.6.25(a) shows the output voltage waveforms with a step load for the converter from the instant the converter starts with no energy stored in its storage elements [6.14-6.17]. In this 2-pscB converter, during the initial transient, a large difference in the magnitude of the inductor currents with a 180° out of phase from each other can be seen in Fig.6.25(b). This magnitude difference decreases as the steady-state condition is
attained. The duration of the transient time depends on the deadtime matching between the two phases and can be reduced using a soft-start scheme.

![Fig.6.25. CF-ACM controller transient response with a step load a) output voltage b) two phase current sharing.](image)

To reduce the inrush current ($I_{inrush} > 30$ A), a pre-charged series capacitor can be added at the expense of introducing a delay. For a charging current ($I_{pc}$) of 20 mA and a 4.7 $\mu$F series capacitor, the pre-charging delay time is 5.6 ms according to [6.18]:

$$t_{pc} = \frac{Q}{I_{pc}} = \frac{CS v_{CS}}{I_{pc}}$$  \hspace{1cm} (6.15)

The power losses decrease as the steady-state condition is reached. The total switching losses reach 20 W during a 4 ns transient period at an efficiency of 97%. The simulated efficiency reaches 98% for a perfect deadtime implementation in the steady-state operation. The main switches $Q_{11}$ and $Q_{21}$ have less than 50% duty cycle switching at 180° phase out of phase. Note that the two synchronous rectifier switches, $Q_{12}$ and $Q_{22}$ are complementary.
6.3.2 The eGaN Gate Drive Experimental Work:

The component selections for the sensor-less eGaN-based 2-pscB converter were first performed. For a 2.54 cm long and a 40 mil wide copper trace, its parasitic inductance is about 8nH. The parasitic inductance of a 0.4 mm diameter via in a 1.6 mm thick PCB is 1.2 nH [6.19, 6.20]. The Autodesk Eagle software calculates the self-resistance calculations of all traces. Using two parallel aluminum electrolytic capacitors of 2.2 µF with a dissipation factor of 0.15 for the two series capacitors $C_{S1}$ and $C_{S2}$ reduce the parasitic resistance $r_{Cs}$ to just a half. The total ESR of the two paralleled capacitors is:

$$\text{ESR} = \frac{\tan \delta}{2 \omega C_S} = 0.01 \Omega \text{ at } 250 \text{ kHz}$$

(6.16)

The inductors consist of two SER2013-472MLB ferrite inductors with a DCR of 1.8 mΩ and a current saturation of 30 A. To construct the two phases and to simplify the evaluation process of the GaN-based 2-pscB converter, two (EPC9003C) half-bridge boards with a maximum device voltage of 200 V, 5 A and (EPC2010C) enhancement-mode eGaN® FET with $R_{DS(on)}$ equal 25 mΩ [6.21] are used. The two GaN evaluation boards can be easily connected to the main 2-pscB converter board, their bypass-capacitors were removed, and phase A half-bridge switches were separated to accommodate a series capacitor in between, as shown in Fig.6.26. The reference voltage of the gate for the isolated high-side switch is the positive variable voltage of the series capacitor, whereas the gate voltage for the low-side switch circuit has a different isolation loop.
Fig.6.26. Block diagram of EPC9003C development board with modifications.

Fig.6.27 shows the complete 2-pscB converter prototype. The input-gate control signal in the mainboard can be either a 5V PWM signal with twice the switching frequency and double the duty cycle or two 5V PWM signals at the switching frequency. Using a logic latch circuit to generate a non-overlapping two-phase clock signal generator, which generates another two PWM signals.
from a single PWM signal input. The four signals simplify the enhanced I² control scheme where the control-loop frequency and duty cycle of the PWM signal input are twice the actual switching frequency and duty cycle of the 2-pscB converter itself. For this option, one input signal can generate four PWM signals to control switches through a logic gate circuit, as shown in Fig.6.28. The gate input signal will be 500 kHz of a 50% duty or less to generate four signals at 250 kHz of 25% duty cycle or less. Switching node voltages must be the same value at fully current sharing, any difference or any small variation is caused by but not limited to deadtime, trace width, and length unbalance of the two-phase paths or it can be the result of switching speed due to unbalanced charging and discharging of the GaN’s input capacitors. As shown in Fig.6.29, the two inductor currents are fully interleaving at an input voltage of 24V. the phase B inductor current \(i_{L1}\) has a slightly higher peak-to-peak ripple, due to phase A voltage overlapping and slope difference and converter mainboard layout parasitic. This difference will cause unbalanced heat distribution among phases. Fig.6.30 shows the series-capacitor current \(I_{Cs}\) where Tektronix P5200 Differential Probe 50X/500X attenuation was used to measure voltages.

Fig.6.28. One PWM source signal (above) to generate four PWM signals reference to \(Cs\) positive terminal.
Switching spikes on the converter phase A voltage node are higher than the switching spikes on the converter phase B voltage node due to the $Q_{11}$ turn-off delay caused by $C_{DS}$ discharging period and non-zero current of inductors at CCM causing overlapping of the $Q_{11}$ and $Q_{12}$ gate voltages during turn-off.
6.3.3 The eGaN Circuit Implementation Discussion

Inserting a series capacitor between switches, $Q_{11}$ and $Q_{12}$, in phase A will introduce a time delay between the gate voltages of the two switches and increase loop inductances ($L_T, L_B$).

![Gate to sources voltage behavior](image)

Fig. 6.31. Gate to sources voltage behavior a) Turn-off delay of $Q_{11}$ and switching overlap of phase A switches b) Phase A normal turn-on switching waveforms.

This will interfere with the synchronization of the deadtime. Fig. 6.31(a) shows a turn-off delay in the $Q_{11}$ gate pulse at an input voltage $V_{in}$ greater than 80 V which amplifies the parasitic effects and will eventually result in almost no deadtime conduction, cause overlapping between phase A switches and a 1~30 ns shoot-through leading to an increasing switching loss or even device failure.
Turn off delay may be affected by the period time to discharge completely the $C_{DS}$ of the top GaN FET ($Q_{11}$), and is approximated by

$$t_{\text{discharge}} = \frac{C_{DS}i_{in}}{I_{L1}}$$  \hspace{1cm} (6.17)

At an input voltage of 48V and $V_{DS}$ of 24V, $C_{DS}$ will be 0.38 nF to yield a discharge time of 6ns on phase A inductor current of 3A [6.22]. During phase A turn-off as shown in Fig.3.1(c), both the ringing on the $V_{GS(Q22)}$ and $V_{GS(Q11)}$ as shown in Fig.6.31(a) are caused by the overlapping of $V_{GS(Q11)}$ and $V_{GS(Q12)}$ as well as the aggravated parasitic inductances due to adding $C_s$. Fig.6.31(b) shows the phase A turn-on waveforms. The non-overlapping turn-on of $V_{GS(Q11)}$ and $V_{GS(Q12)}$ yields a small ringing amplitude of 22 mV for the $V_{GS(Q22)}$ compared to the ringing amplitude of 153 mV when both $V_{GS(Q11)}$ and $V_{GS(Q12)}$ are overlapping. In both cases, the level shift circuitry, dead-time adjustment circuitry, and gate driver are still functioning well. Fig.6.32 shows the phase A high side switch current sink path when the discharging of the eGaN’s device parasitic capacitances ($C_{DG}$, $C_{GS}$, and $C_{DS}$) occurs through the series capacitor and bottom switch on-resistance ($r_{on2}$). As
such, an isolation scheme must encompass the entire high-side switch circuit to make sure both
the reference voltages of the switches are similar. For the $UCC27611$ gate driver, its ground pins
(pins 7, 2) have to be isolated by adding a small capacitor between the driver ground and switch
source. Besides, the deadtime must be similar for a complete current sharing. Another method is
to slow down the turn-on switching speed by adding resistance in series with the $Q_{12}$ gate or adding
a diode to the $Q_{11}$ turn-off current sink circuit. To limit the loss components of body diodes in the
switches and forward voltages, a deadtime of 20 $ns$ or less is recommended [6.23]. The
approximated sinking current capability (at turn-off) is 2.5 $mA$ which can be calculated as $I_{sink} \geq
1.5 \frac{Q}{Gt_{sw(os)}}$. Hence, for maximum efficiency, the EPC9003C has a minimum deadtime for the
diode conduction time and eGaN FET body diode acts like a Schottky diode with a slightly higher
forward drop. The bootstrap capacitor ($C_{12}$) is discharged when the high-side switch is turned on
with a voltage of $V_{REF} - V_{SS}$, which equals 5V. The voltage at the source of $Q_{11}$, $V_{SS}$, referenced to
the ground, is the sum of the voltage spike due to the $di/dt$ of the source parasitic inductance and
the voltage at the positive terminal of the series capacitor $V_{CS}$ that is always positive.

Fig.6.33 (a) shows the phase A equivalent circuit during the negative $dv/dt$ as $Q_{11}$ turns off
when the Miller effect occurs due to the discharge of the $C_{DSI}$ through $R_G$ and $R_{OL}$ together with
the conduction of the body-drain diode of $Q_{12}$. For fast pull-down, $R_G/R_{OL}$ has to be low at the end
of the first interval with less switching losses at this transition. Fig.6.33(b) shows the phase A
equivalent circuit during the positive $dv/dt$ as $Q_{11}$ turns on at the beginning of the first interval. As
current flows through and charges both the $C_{GD2}$ and $C_{GS2}$, $V_{GS(Q12)}$ increases above its threshold
voltage and switches on $Q_{12}$ randomly and produce the oscillation in the circuit.
The series capacitor voltage prevents a negative gate bias to occur, but traces and pads stray inductances ($L_T, L_B$) aggravate the ringing in the circuit if not managed adequately besides ringing.
caused by the source and common source parasitic inductances ($L_S$ and $L_{CS}$). A series capacitor inserted between the $Q_{11}$ gate, and its source terminal can be used to isolate the gate driver and prevent false turn-on due to gate-to-source voltage spikes. Another solution is to add a diode in parallel with the gate resistor to increase the gate turn-off.

Fig. 6.34. Circuit schematic of gate driver circuit for $Q_{11}$.

Fig.6.34. The positive side of $C_S$ is the gate reference voltage for the isolated high-side switch. The reference voltage of the low-side switch circuit is ground therefore, its gate voltage requires a different isolation loop. $C_{ISO}$ works as an isolating capacitor to prevent any direct conduction between the high side driver and the synchronous rectifier switch driver due to the voltage storage element of $C_S$ in between, this capacitor is not necessary unless there is need to provide a negative bias to the $V_{GS}$. The anode of bootstrap diodes, $D_{Bstrap1}$, is commonly connected to a driver source $V_{DD}$. To minimize voltage spikes and reduce EMI of self-inductance and self-resistance of the traces, gate drivers should be located as close to the GaNs as possible. Each gate power supply
can be directly obtained from the controller IC internal LDOs or an isolated transformer. Optocouplers 5V terminals directly connected to gate drivers LDOs.

![Experimental prototype top view](image)

**Fig. 6.35.** The 2-pscB conv. 48V/5V experimental prototype top view.

An experimental prototype, shown in Fig.6.35, was built with the new design in Fig.6.34. The same specifications were used as listed in Table-I at $D_{\text{Drive}}$ equals to 50% and total $I_L$ of 3.35 A. The measured rising time ($t_r = (5.9-6.3) \text{ ns}$), falling time of ($t_f = 4.5-5$) ns, and approximated overshothing of 20%. To construct the converter GS61004B transistors with $R_{\text{ds(on)}}$ of 15 mΩ are used. Despite two-phases parasitic components unbalance, Fig.6.36 shows output voltage, series capacitor current and the fully automatic current balancing ($\approx 100\%$) between two phases at the voltage of 48V/5V. A peak efficiency of 94.4% measured at 2.3 A output. The simulation in Fig. 6.24 and experimental waveforms are in good agreement. However, there is some discrepancy during the transient turn-on process.
Fig. 6.36. The 2-pscB converter typical waveforms of $i_{CS}$, $V_o$, $i_L$, $i_{L1}$, and $i_{L2}$ at 48V input.

Fig. 6.37 Thermal distribution of GaN prototype a) at no load
b) at $V_{in} = 48V$ and efficiency of 94%.

From Fig.6.37 (a) we noticed that heat is not distributed evenly over PCB board and temperature of $Q_{11}$ gate driver reached up to 52°C this may be due to complete isolation and charging period of isolating capacitor $C_3$. As shown in Fig.6.37 (b), the temperature of phase A switches and series capacitors reached 94.4°C at an efficiency of 94%, the direct cause of the temperature rise, and the heat generated is due to the existence of a series capacitor current ripple that is charging its
direction every cycle. It is clear there is a mismatch heat generation between phases since the series capacitor charging from phase A and discharging into phase B.

6.3.4 Conclusion

A theoretical approach and small-signal average models to design an automatic current sharing scheme without sensors were presented for a 2-pscB converter. The effects of its phase unbalance and parasitic circuit elements were discussed. Experimental results were presented for a sensor-less eGaN-based 48V/5V, 5.5A, 250 kHz 2-pscB converter. This eGaN converter shows a good performance suitable for high-frequency dc/dc conversion applications with high step-down ratios. Large power applications with input voltages up to 600V could be implemented using the high-voltage, high-current eGaN devices.

6.4 EMI of DC Input Circuit Design

DC-DC converters have to be compliant with EMI standards, this requires additional noise filtering and adequate protection module to dictate decoupling requirements. Source, load, and dynamic response characteristics have to be carefully considered for high-reliability applications. Fig.6.38 shows a full system block diagram of 2-pscB converter with all necessary components for the DC-DC system including safety, protection, and EMI filter for input and output side since the line impedance affects the stability, voltage drop, and output ripple. To calculate these factors there is a need to understand the characteristics of the DC power source such as availability, voltage range, and its non-linear behavior for the output side, consideration has to be sufficient for power distribution path and output impedance.
Fig. 6.38 Complete 2-pscB converter block diagram.

Since DC-DC converters are considered negative impedance devices so when the input voltage rises the input current will decrease and vice versa, this, in general, can affect the stability of converter especially when there is a high impedance source. Most DC-DC converters have high switching frequency characteristics which react with components parasitic and generate noise (current harmonics) primarily at dc input, the main types of generated currents are common-modes.

Fig. 6.39 Block diagram of 2-pscB converter EMI noise.
noise which presents in both negative and positive line through parasitic capacitors and EMI ground in the system, the second type is differential-mode noise which circulates between the positive line to the negative inside the converter as shown in Fig.6.39. Looking to DC-DC converter as a full system, this will include all components that needed for EMI Common Mode Chokes for EMC:

All capacitors are MLCC where:

\[ V_{in} = 9\text{--}36 \, V_{dc}, \quad C_1 = 6.8 \, \mu F/50V, \quad C_2 = 6.8 \, \mu F/50V, \quad C_3 = C_4 = 470 \, pF/2kV, \]

"CMC-05 = 450 \, \mu H \times 2, \, 5.2A \, 25 \, m\Omega"

![Fig.6.40 EMI circuit of eGaN experimental prototype.](image)

The given component sizes and specifications are pre-evaluated values and may need to be optimized to suit the application and improve the efficiency of the EMI filter, as shown in Fig. 6.40. The network relies heavily on the use of high-quality capacitors, the layout of the EMI circuit board, and a low impedance path to the ground.

EMI emissions Lab testing includes both conducted and radiated signals. Radiated emissions usually are the major focus for EMI engineers of product designers, for this EMI experiment,
measuring conducted emissions normally is done using a spectrum analyzer (Rigol DSA815) (or EMI receiver) and a Line Impedance Stabilization Network, or LISN, which helps match the power line to 50 $\Omega$. Using Tekbox Digital Solutions LISN models for both line-operated and DC-operated equipment model TBOH01 (DC 5uH LISN). Mini-Circuit power splitter of ZSC-2-2+ is used as shown in Fig.6.41. These test steps are used to verify that electromagnetic emissions from the MOSFET EVM as shown in Fig.6.42 do not exceed the specified requirements for power input power leads, including returns as standards illustrated in Fig.6.43 [6.24]. This requirement is applicable from 10 $kHz$ to 10 $MHz$ for all power leads, including returns, that obtain power from

other sources not part of the Si MOSFET EVM, input power is set to 48 V at 250 $kHz$ and 6 V output, spectrum analyzer testing results is shown in Fig.6.44, this results for specified frequency range showed that EMI occurs at low frequencies less than 250 $MHz$ and no interference above this frequency.

![Fig.6.41 Experimental EMI measurement setup.](image-url)
Fig. 6.42 EMI Lab measurements for Si MOSFET EVM.

Fig. 6.43 EMI standard for DUT power leads, source voltage AC and DC.
Fig. 6.44 EMI spectrum of 2-pscB Converter 48V, 250 kHz, Si MOSFET EVM.

6.5 Proposed Integrated Control Circuit (IC) for 2-pscB Converter.

A functional block diagram of integrated circuit (IC) implementation of the series capacitor buck converter is proposed for high voltage applications (e.g., greater than 5V) powered by a 48V supply rail or above. An overview of the IC is shown in Fig. 6.45 [6.25]. The controller, gate drivers, external power MOSFETs, internal regulators, and supporting circuitry, the chip includes typical protection circuits such as input Under/over-Voltage Lockout UVLO for each phase and output under/over-voltage protection and overcurrent protection. Chip synchronizes is connected to an external clock and new features can be included to manage the series capacitor voltage according to controller method’s requirements. The converter was designed to operate with a high frequency above 500 kHz per phase switching frequency. Three internal linear regulators have to be isolated, which generate 5V supply rail on the $V_{G+}$, $V_{GA}$, and $V_{GB}$ pins. The input comes from the $V_{IN}$ pin, $V_{G+}$ supply rail is used to power the gate drivers of phase A low side switch and phase
B switches. The $V_{GA}$ supply rail is used to power the gate drivers of phase A high side switch and the $V_{GB}$ supply rail is used to power the gate drivers of phase B high side switch. To improve converter efficiency, an external 5 V supply is recommended to be connected to the $V_{G+}$ pin, thereby overriding the internal 5 V regulator.

### 6.6 Summary

In this chapter, different kinds of gate driving approaches were implemented and tested in a full scale. Both isolated Si MOSFET and GaN gate drive circuits were modeled and verified through simulation, experiments, and compared for their performances. For the current sharing issue in the multi-phase buck converters, it is worthwhile to analyze. It was found that full current sharing can be achieved at 110V/12V or higher voltage if all phases have the same physical structure in terms of resistive, inductive, and capacitive trace values. In this chapter, analysis of
EMI emissions including both conducted and radiated signals is introduced with lab measurements to show its impact on the converter which can be improved with proper PCB layout management.
6.7 References


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Chapter 7: Conclusions and Future Work.

7.1 Contribution of This Work

In the past three decades, SMPS technology has been improved to meet the needs of future power supplies to achieve higher efficiency, higher output current, lower cost, and smaller size. Generally, these functions cannot be achieved using conventional techniques. In order to increase frequency and power density, it is necessary to solve the limitations of device loss, passive size, package parasitic elements, thermal management, and layout parasitic parameters.

The research work carried out in this dissertation focused on the analysis of 2-pscB converter in terms of its work capabilities and electromagnetic characterization. As a result of better converter devices, a better understanding of this topology, higher driving efficiency, and good power converter circuit performance. Proper selection of gate driver isolation and heat distribution layout solutions are very significant for improvement in the performance of the converter like reduction in weight and size, improvement in efficiency, stability, and reliability. Also, a brief study on the usage of different types of controllers has been explored that would help in the fabrication of converter state-of-the-art with high efficiency and robustness, and increase in the dynamic response, among others.

One of our research objectives was to simplify the design and fabrication methodology of 2-pscB converters. Initially, a state-space representation and small-signal average model was generated, including converter parasitic components. Different design approach equations also have been generated and analyzed to confirm the behavior of the converter transition and simplify calculations for steady-state performance. Secondly, a case study with practical prototype specification is used to practice and give an example of the converter performance and the
experimental use of Gallium Nitride (eGaN) and Si MOSFET transistors in 2-pscB converters. EMI filter has been added to the power supplies to eliminate the input common-mode (CM) noise to the four gate drivers’ prototypes. Presenting the automatic current sharing mechanism at an input voltage higher than the voltage of a conventional 12V/10A point of load (PoL) converter was the core of this study. This complete current sharing condition was achieved at 110V/6A level using a novel isolated gate driver circuitry at experimental efficiency up to 94%. This is the first work reported in the literature to implement this approach of gate driver circuit.

The Lab results agreed reasonably well with the analytical results obtained from case study specifications. The current sharing percentage was investigated when a series capacitor voltage still manages to maintain the desired output voltage to obtain the stable current sharing among the two phases. The isolated gate driver layout was done in a lossless manner, so as not to impact the converter phase A efficiency negatively. A novel logic latch circuit to generate four PWM signals from a single PWM signal input was implemented successfully, this simplifies the duty cycle modulation scheme where the control-loop frequency and duty cycle of the PWM signal input are twice the actual switching frequency and duty cycle of the 2-pscB converter itself.

Different control methods were proposed in chapter 4, such as Average Current Mode Controller (ACM), $I^2$ Average Current Mode Controller ($I^2$ ACM), and Valley Current Mode Controller (VCM). These methods use a fixed frequency approach and one current path to minimize the overall parasitic components and propagation delays, which will help in the enhancement of the overall performance.

In Chapter 5, a comprehensive analysis was successfully carried out to study the frequency response of the node switching voltage and the shape of the amplitude and phase spectrum under
the condition of the two-phase current balance. The resulting trapezoidal waveform represents the true shape of the duty cycle spectrum, where the amplitude and phase of the shape vary in proportion to the series capacitor voltage and current sharing mechanism. This frequency analysis would give insight into controller perturbation and common-mode noise and converter bandwidth.

7.2 Future Work

Most of the controller methods that have been mentioned in chapter 4 can be further investigated to include other CMC methods, such as $V^2$ enhanced valley mode, hysteresis mode control, and other different methods based on constant frequency, like peak and valley ripple-based (CF-PR) analog control laws with different modulations, their stabilities, and duality. In Chapter 6, a functional block diagram of integrated circuit (IC) chips for high-voltage applications (e.g., greater than 48 V) is proposed. The proposed chip uses a path feedback loop to achieve twice the switching frequency of the series capacitor buck converter, thereby reducing the size of the controller. Soft switching for 2-pscB converters can be implemented using a snubber circuit, resonant circuit, or soft latching circuit to improve efficiency and reduce heat dissipation caused mainly by switching losses. Soft switching allows the operation of converters at very high switching frequencies to leading to high power densities.

Due to the fact that coupled inductors between the phases give different equivalent inductances, for a faster transient response, Coupled Inductor (CI) output filters have been used in power converters without sacrificing converter efficiency. Therefore, compared with uncoupled inductors, inductors are magnetically coupled, and smaller size inductors can be used at the same switching frequency without causing more ripple current. More investigation can be done for 2-pscB converter output to examine the two-phase inductor coupling features and compare with a
non-coupling inductor besides the further reduction in the total volume of inductors and capacitors and the steady-state ripple current that affects the speed of the controller.

Different series capacitor materials can be tested and integrated to reduce phase-to-phase heating mismatches. Further analysis can be conducted in terms of an all-ceramic-output capacitor design, the number of capacitors, the power delivery performance, and the board area. The impedance between individual components of the ceramic capacitor I/O network could produce a poorly combined impedance for the power delivery path. As such, a better design using large bulk electrolytic capacitors for most of the output capacitance can be implemented, which is less expensive per unit capacitance. One main drawback associated with it is the large equivalent series resistance (ESR) compared with ceramic capacitors. For this reason, ceramic capacitors are also used for a high-frequency decoupling. For symmetrically coupled inductors, the output peak-to-peak current ripple is minimized, to the point that bulk filtering capacitors can be eliminated. This issue will have a huge impact on converter size and cost.

Upon the findings in chapter 6 future recommendation is to push for higher levels of integration to test the efficiency of different suggested topologies.
Appendices

Appendix A: 2-pscB Converter CMC in MATLAB.

%% %---------------------------------------------------------------------------------------------------------------%
% This script Two Phase Series Capacitor Buck Converter (2-pscB) in Continuous Conduction Mode
% Author: Salahaldein Ahmed
% Date: January 25, 2022
% Version: 2
% Copyright: Salahaldein Ali Aboajila Ahmed
%---------------------------------------------------------------------------------------------------------------%
% This example shows how to control the output voltage of a 2-pscB converter
% The current flowing through the inductor is never zero, therefore the
% DC-DC converter operates in Continuous Conduction Mode (CCM).
% To convert and maintain the nominal output voltage, the PI Controller
% subsystem uses a simple integral control. During startup, the reference
% voltage is ramped up to the desired output voltage.

%% Open Model
open_system('Two_pscB_converter_ccm.slx');

%% Specify the Design Parameters
% The system is required to generate and maintain an output voltage of
% 12 V with a full load power capability (max) of 73 W. The input voltage is
% 110 VDC the full load includes a constant load and a cyclic load
% The 'Two_pscB_converter_ccm_data.m' script defines the design parameters as variables in the MATLAB(R)
% workspace.
clc
clear all
close all
Input_Voltage           = 110; % Input voltage to the 2_pscB converter [V]
Output_Voltage          = 13.97; % Desired output voltage from the 2_pscB converter [V]
Ser_Cap_Voltage         = Input_Voltage/2 % Series Capacitor Voltage
Output_Power            = 49; % Full load power output [W] (AS EXAMPLE)
fsw_Hz                  = 250000; % MOSFET switching frequency [Hz]
Kp                      = 0.01; % Proportional gain for PI controller
Ki                      = 20; % Integral gain for PI controller
del_I                   = 70; % Peak-peak inductor ripple current as a percentage of full load current
percentage of full load current = 1; % Peak-peak output voltage ripple as a percentage of output voltage
del_V                   = 1; % Peak-peak series capacitor voltage
percentage of output voltage
del_Vcs                 = 1; % Peak-peak series capacitor voltage
ripple as a percentage of series capacitor voltage
share_constload         = 70; % Percentage of load current drawn by constant load
share_cyclicload        = 100-share_constload; % Percentage of load current drawn by cyclic load
cyclic_load_period      = 1/40; % Cyclic load period
cyclic_load_pul_width   = 25; % Pulse width of the current pulses drawn by the cyclic load
Ts                      = 1e-8; % Sampling time for the solver

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%% Calculate the Open-Loop Duty Cycle
% The duty cycle depends on the input voltage and the
desired output voltage.
Duty = 2*Output_Voltage/(Input_Voltage)

%% Determine the Constant Load Resistance
I_ful_avg = Output_Power/Output_Voltage % Full load average current that
flows through the load
R_const = Output_Voltage/I_ful_avg

%% Calculate the Filter Inductance
% Choose the inductance value based on the input and output specifications
% of the converter.
% The inductance value depends on the input and output specifications
% of the converter. For this example, the converter is required to work
% in CCM for 20-100% of full load power. When, at the lower boundary
% condition, the power is 20% of full load power, the average load current
% is 20% of full load average current, I_ful_avg. At the end of each
% cycle at the lower boundary condition, the inductor current goes to zero.
% The inductor ripple current, del_I, at this point is twice the average
% output load current, that is 40% of the full load average output current.
L_min= 5*R_const*Output_Voltage*(1-Duty)/ (fsw_Hz*(6*R_const*del_I*0.01*...
    I_ful_avg+Output_Voltage))

%% Plot Inductance Versus Inductor Current Ripple
% Generate this plot to see how the filter inductance relates to the
% inductor ripple current (expressed as a percentage of full load current).
% For this example, the marker at 70% corresponds to an inductance of
% 1.1e-05 H.
figure;
del_I_range = 20:0.1:80; % Percentage of full load current (20-80%)
L_range = 5*R_const*Output_Voltage*(1-
    Duty)./(fsw_Hz*(6*R_const*del_I_range*...
    0.01*I_ful_avg+Output_Voltage));
plot(del_I_range,L_range);
hold on;
L_del_I =5*R_const*Output_Voltage*(1-Duty)/(fsw_Hz*(6*R_const*del_I*0.01*...
   I_ful_avg+Output_Voltage));
plot(del_I,L_del_I, 'r--o');
xlabel('Inductor current ripple (% of full load current)');
ylabel('Inductance (H)');
title('Inductance Vs Inductor Current Ripple');
%% Choose a Filter Capacitance

\[
C_{\text{min}} = \frac{(5(1-Duty)/\left(L_{\text{min}} \cdot f_{\text{sw Hz}}\right) - 1/R_{\text{const}})}{(96 \cdot f_{\text{sw Hz}} \cdot (\text{del}_V \times 0.01))}
\]

\[
C_{\text{nom}} = 10 \cdot C_{\text{min}} \quad \% \text{Choosing bigger value}
\]

%% Plot Capacitance Versus Voltage Ripple

% Generate this plot to see how capacitance for limiting the output voltage
% ripple varies depending on the design parameters. For this example, the
% marker at 1% Output Voltage Ripple corresponds to a capacitance of
% 4.5e-06 F.

figure;
\[
\text{del}_V\_\text{range} = 0.5:0.1:5;
\]
\[
\text{C}_{\text{range}} = 10 \cdot \frac{(5(1-Duty)/\left(L_{\text{min}} \cdot f_{\text{sw Hz}}\right) - 1/R_{\text{const}})}{(96 \cdot f_{\text{sw Hz}} \cdot (\text{del}_V\_\text{range} \times 0.01))};
\]
plot(\text{del}_V\_\text{range}, \text{C}_{\text{range}});
hold on;
\[
\text{C}_{\text{del}_V} = 10 \cdot \frac{(5(1-Duty)/\left(L_{\text{min}} \cdot f_{\text{sw Hz}}\right) - 1/R_{\text{const}})}{(96 \cdot f_{\text{sw Hz}} \cdot (\text{del}_V \times 0.01))};
\]
plot(\text{del}_V, \text{C}_{\text{del}_V}, '-', 'LineWidth', 2, 'MarkerSize', 10, 'MarkerEdgeColor', 'r', 'MarkerFaceColor', [0.5, 0.5, 0.5]);
xlabel('Voltage Ripple (%)');
ylabel('Capacitance (F)');
title('Capacitance Vs Voltage Ripple');
%% Choose a Series Capacitance
Cs_min = Duty*Output_Voltage*(1-Duty)/(4*fsw_Hz^2*L_min*del_Vcs*0.01*Ser_Cap_Voltage)
Cs_min = (Duty^2*(1-Duty))/(4*fsw_Hz^2*L_min*del_Vcs*0.01)
Cs_nom = Cs_min*5 \% Choosing bigger value

%% Plot Series Capacitance Versus Voltage Ripple
\% Generate this plot to see how capacitance for limiting the output voltage
\% ripple varies depending on the design parameters. For this example, the
\% marker at 1\% Output Voltage Ripple corresponds to a capacitance of
\% 8.4e-06 F.

figure;
\texttt{del\_Vcs\_range = 0.5:0.1:5;}
\texttt{Cs\_range = 5*(Duty^2*(1-Duty))/(4*fsw\_Hz^2*L\_min*del\_Vcs\_range*0.01)}
\texttt{plot(del\_Vcs\_range,Cs\_range);} \texttt{hold\ on;}
\texttt{Cs\_del\_Vcs = 5*(Duty^2*(1-Duty))/(4*fsw\_Hz^2*L\_min*del\_Vcs*0.01)}
\texttt{plot(del\_Vcs,Cs\_del\_Vcs,'r--o');}
\texttt{xlabel('Voltage Ripple (\%)');}
\texttt{ylabel('Cs Capacitance (F)');}
\texttt{title('Cs Capacitance Vs Voltage Ripple');}
\texttt{return}
\% Run the Simulation
\texttt{sim('Two\_pscB\_converter\_ccm\_slx');}
Cs Capacitance Vs Voltage Ripple

Voltage Ripple (%)

Cs Capacitance (F)
Appendix B: 110V 2-pscB Converter VMC in MATLAB.
Appendix C: 110V-2pSMB Converter CMC in MATLAB / Simulink.
Appendix D: 110V/12V PCB Design Layout.
Appendix E: All Publications


**Patent**

1. One provisional patent filed: **S. A. Rmila**, University of Arkansas, "Isolated two-phase series capacitor buck converter (I-2pscB)"