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Development of an Accelerated Life Testing Method for Reliability Assessment of Wire Bonded Interconnects Subjected to Mechanical and Electromigratory Stresses

Whit Vinson
University of Arkansas, Fayetteville

Development of an Accelerated Life Testing Method for Reliability Assessment of Wire Bonded Interconnects Subjected to Mechanical and Electromigratory Stresses

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by

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This thesis is approved for recommendation to the Graduate Council.

_____
David Huitink, Ph.D.
Thesis Director

_____
Paul Millett, Ph.D.
Committee Member

_____
Yarui Peng, Ph.D.
Committee Member

ABSTRACT

Power electronic advancement trends indicate that device power density will continue to increase as a result of increased power requirements and desired device form factor reduction in order to reduce weight and material costs and increase ease of integration into next-generation power systems. With these advancements come concerns regarding device reliability. The compounded effects of increased power density and form factor reduction in electrical conductors will yield amplified joule heating effects in addition to the already increasing device temperature profiles resulting from the incorporation of wide bandgap technology into power systems. Joule heating effects can lead to a variety of reliability problems, but there are two failure modes which pose serious potential threats for devices in the future. In electrical conductors, one phenomenon associated with elevated temperatures and power densities is electromigration. Electromigration refers to the migration of conductor material away from its initial position and is typically associated with electrical resistance increases and shorting. The second potential failure mode is related to thermomechanical stresses resulting from differing coefficients of thermal expansion at localized hot spots in a device. One of the most common ways to make connections inside of power electronic devices is by wire bonding. Small current carrying components, such as wire bonds, in power electronic devices may be subjected to a combination of electromigratory and thermomechanical related stresses during operation. Thus, it is advantageous for studies to be conducted to understand the impact that the combined effects of electromigration and mechanical stress have on wire bond reliability. This work introduces a novel accelerated test methodology for divulging the impacts of these combined effects on wire bonded interconnects and introduces a framework for reliability analysis based on accelerated testing methodologies.

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Woo Pig Sooie and Go Hogs Go!

DEDICATION

This work is dedicated to my parents, Jay and Kat, and sister, Garland. Thank you for the tremendous amount of love and support you have given to me throughout my life. You have all shaped me into the person I am today. I love you all.

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1. INTRODUCTION

1.1. Power Electronic Devices

Global energy consumption is on the rise and there is no indication that it will stop rising any time soon. Power electronic devices are an integral part of energy generation, transmission, and storage in the modern world [1]. The continued development of numerous power electronic systems has assisted in meeting the demands of growing energy needs and assisted in the emergence of renewable energy options in recent years [2], [3].

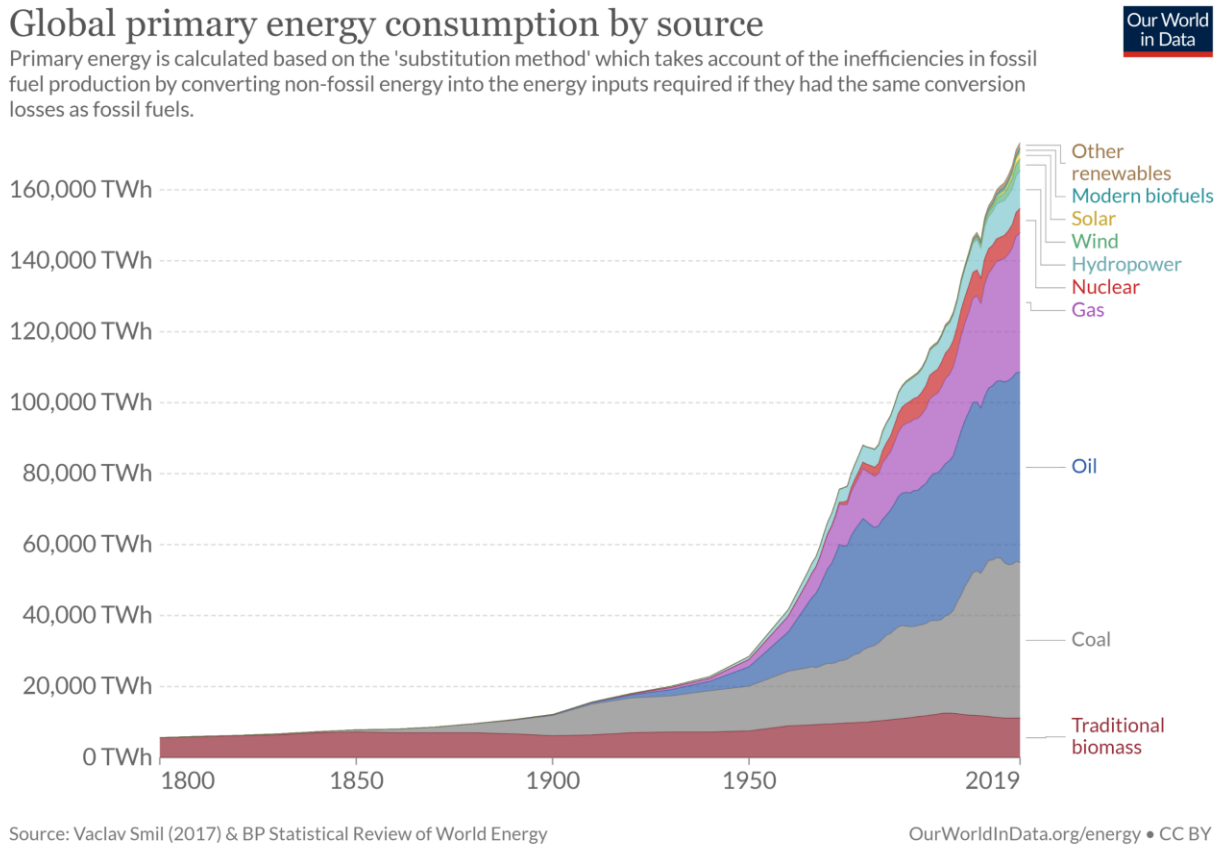

Figure 1: Global energy consumption over time. Reprinted from "Energy". Published online at OurWorldInData.org. Retrieved with permission from: https://ourworldindata.org/energy [4].

Recent developments of power electronic equipment have yielded new materials (such as the wide bandgap technologies of SiC and GaN chips for high power and high-speed applications), new system architectures, and improved operating efficiencies (which are exceeding 98.5%) [3],

[5]–[7]. The combination of all these technological advancements in addition to the introduction of reduced form factor restrictions (for the reduction of weight and manufacturing costs) has also, perhaps most notably, yielded an increase in device power density over time [1], [7]. Therefore, as the increase in global energy consumption has continued, so has device power density.

1.1.1. Operation

As mentioned before, power electronic devices are used in a variety of applications related to energy consumption in the modern world. Applications of these devices include, but are not limited to, industrial motor drives, power supplies, traction control systems, home appliances, and power conversion stations [1], [3], [8]. These applications require power electronic devices for the conversion of voltage levels or the rectification/inversion of electrical current from alternating to direct or vice versa. For example, without power electronics, we would be unable to efficiently invert the direct current produced by solar cells into alternating current for transmission across long distances or into power grids in cities.

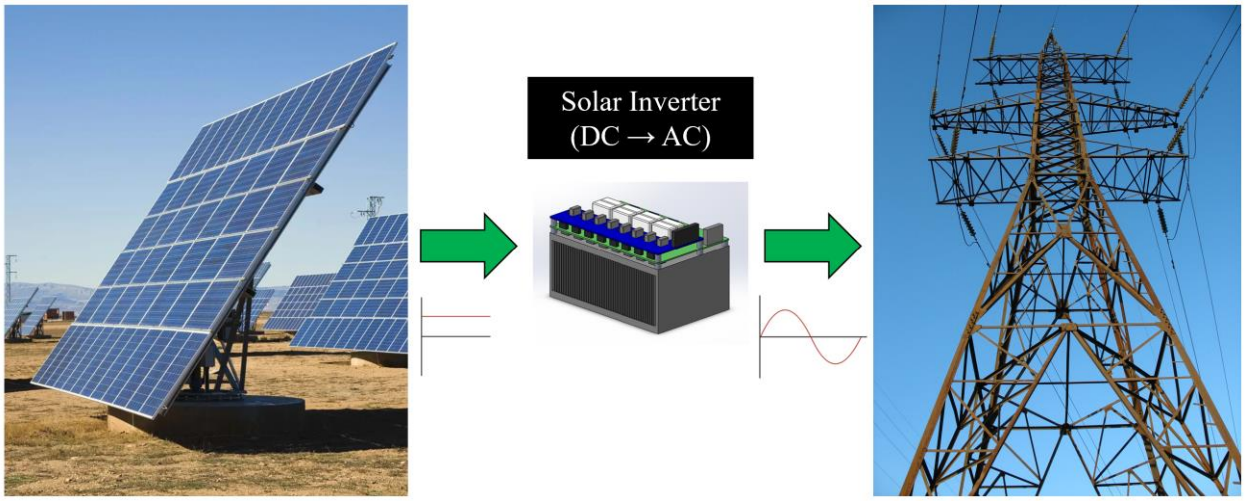

Figure 2: Example of power electronic device operation and functions. Solar inverter can be used to convert DC electricity to AC for transmission.

1.1.2. Failure Mechanisms

All categories of power modules are clearly critical to the utilization of electrical power in the world and, therefore, can be considered an Achilles heel in the energy consumption process if they cannot be relied upon to perform effectively during times of high energy demand [2]. There are numerous failure mechanisms associated with the normal operations of power electronic devices. The most common mechanisms are classified as overstress and wear-out failures and are summarized in Figure 3 [9]. Overstress failures are typically a result of fabrication defects, improper design considerations, or the sudden introduction of an unintended condition. Wear-out failures are degradation mechanisms which are system and device responses to the expected use condition cycles.

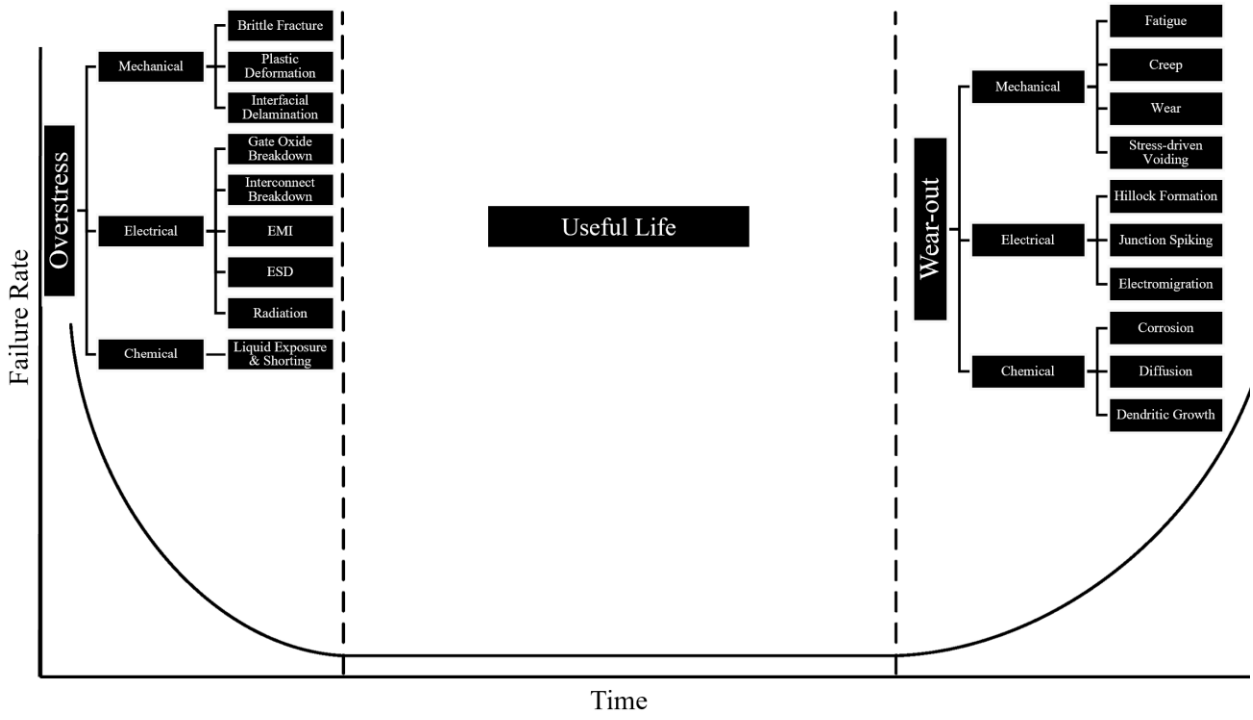

Figure 3: Bathtub curve for describing device failure rates over time (separated by overstress and wear-out failure mechanisms).

As power electronic device miniaturization continues, the likelihood of certain failure mechanisms affecting device lifetimes will change. Some mechanisms will become more

concerning with respect to reliability than they have in the past. The advent of wide bandgap technologies allows power devices to operate at higher temperatures than they have in the past [5]. It is well known that the failure rate of electrical components is directly related to conductor operating temperatures [10]. Critical components in power modules, such as MOSFETs (which have started using wide bandgap technologies in recent years), typically experience the highest temperatures in a power system and thus will begin to demonstrate shortened lifetimes as temperatures rise [11], [12]. In addition to anticipated heightened operating temperatures, device form factor reductions and heightened power requirements imply the existence of elevated current densities in devices. These effects of power electronic advancement indicate an increased potential for electromigration (EM) and thermomechanical (TM) stressing at localized hot spots in power electronic systems [13], [14].

1.1.2.1. Electromigration Failure

EM failures are classified as wear-out failure modes which occur under elevated conductor temperatures and current densities [15]. These failures manifest themselves in various ways under the same stress conditions for different materials which can include void nucleation, void growth, void migration, cracking, bambooing, grain structure realignment, metal migration, and intermetallic compound growth, all of which shorten conductor life [15]–[18]. The most well-known EM lifetime model, typically referred to as Black's equation, simplifies a lot of the complexity associated with EM failures and accounts for current density and conductor temperature in addition to experimentally derived model parameters (A and E_a).

$$MTTF = \frac{A}{j^n} e^{\left(\frac{E_a}{kT}\right)}$$

$$MTTF = \text{ mean time to electromigration failure } [hrs]$$
$$A = \text{geometry related constant}$$
$$j = \text{current density } \left[A \cdot cm^{-2}\right]$$
$$n = \text{current density related model parameter}$$
$$E_a = \text{activation energy } [eV]$$
$$k = Boltzmann's \text{ constant } \left[eV \cdot K^{-1}\right]$$
$$\left(= 8.617333262 \cdot 10^{-5}\right)$$
$$T = \text{conductor temperature } [K]$$

Figure 4: Summary of Black's equation and explanation of variables.

Void nucleation has been shown to occur in high temperature and current dense regions and will take a much longer time compared to the growth of existing voids, emphasizing the need for consistent fabrication techniques and materials to reduce the presence of voids prior to operation in future power devices [19], [20]. Metal and void migration are dependent on current density direction and temperatures [21]. Metal atoms migrate in the direction of current flow and tend to gather in regions of lower temperatures while voids will do the opposite, migrating at a velocity proportional to the local current density [22]–[24]. Atomic movement in EM tends to be much faster along grain boundaries because diffusion can happen much more quickly at these boundaries, explaining why grain size variation and realignment impact EM effects [25]. Additionally, as voids form and migrate, they begin to generate exponentially growing mechanical stresses within the conductor, inducing strains which cause deformations [26]–[28].

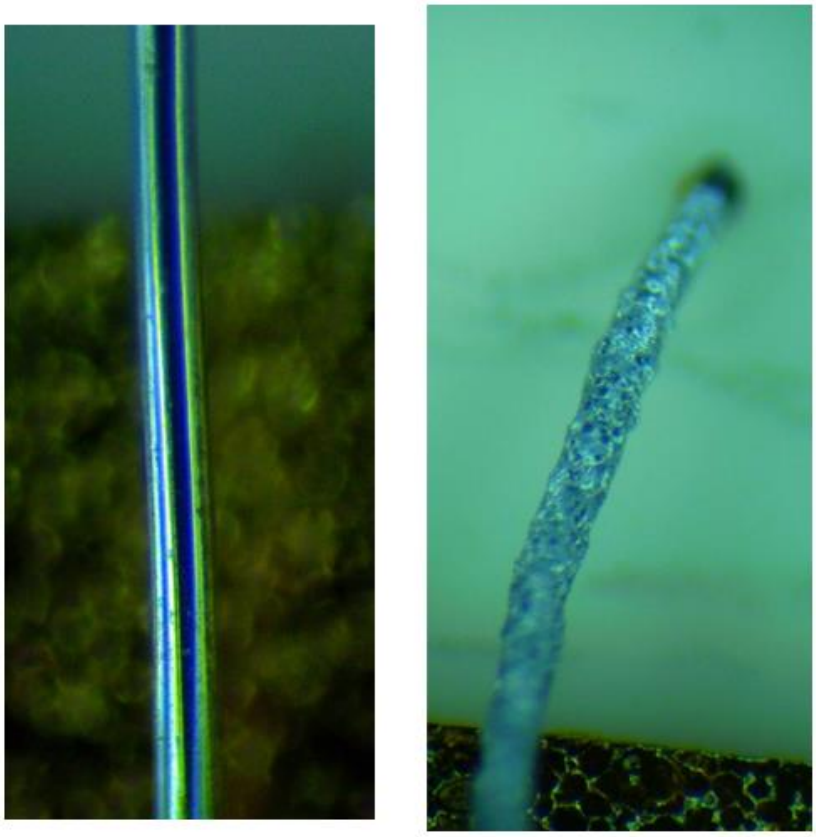

Figure 5: Images of aluminum wire bond before (left) and after (right) being subjected to EM conditions. The formation and migration of voids within the wire has changed the geometry of the wire and resulted in failure.

As these effects are generated over time under the stress conditions, they begin to compound upon themselves, accelerating failure. For example, geometry changes, such as void nucleation, void migration, and metal migration are dependent on the EM stress rates, which are varying as geometry is changed [29]. One easy way to understand this is by thinking about the effects of joule heating and current density as void nucleation and migration occur. As voids are formed and collect in certain regions of a conductor, the cross-sectional area of the conductor at that location is reduced, effectively increasing the local current density and joule heating there [30]. Therefore, regions in systems which experience joule heating and current density effects are easily identified as being particularly weak in terms of resilience to EM compared to other regions of the system [31].

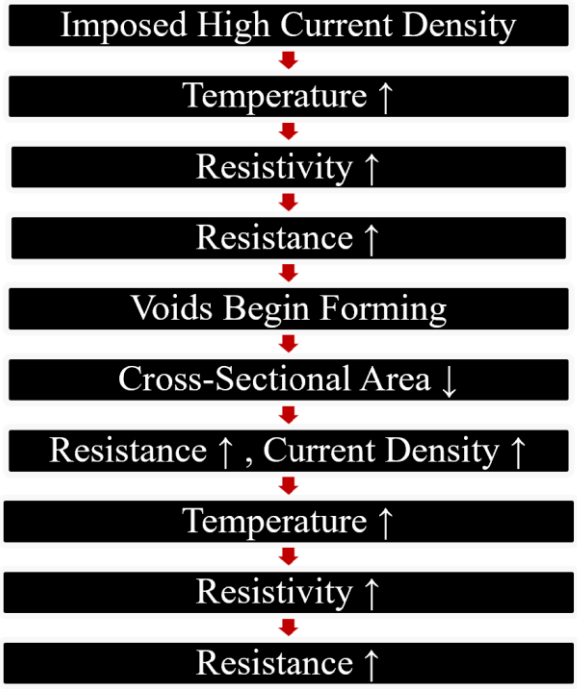

Figure 6: Flow diagram exemplifying the compounded acceleration of EM failures over time.

The potential for EM failures increases with increasing power density as it has been demonstrated that heightened power cycles induce increased damage growth rates, increasing concerns regarding system reliability [28]. EM is a limiting factor not only for device reliability but also, for operating frequencies [32]. As EM failures become more prevalent, operating frequencies will need to be optimized to reduce EM effects as they are linked to device operating temperatures. The maximum current density which can be tolerated by conductors is also shrinking with the corresponding form factor reductions [13]. For example, to maintain the reliability of an aluminum wire which is raised from 25 to 125 degrees Celsius, the maximum current density must be reduced by 90% [23]. Additionally, it has been shown that void nucleation in multi-line grids impacts current density at other lines in the system, further complicating the system reliability estimations for future power electronic systems [33]. This demonstrates the need for EM specific design layout requirements and failure characterizations to relieve reliability concerns and ensure optimized performance in future power deceive architectures [13], [34].

1.1.2.2. Thermomechanical Stress Failure

Thermomechanical stresses have been known to cause reliability problems in high-temperature electronic assemblies for quite some time. TM stresses are rooted in the material property known as the coefficient of thermal expansion (CTE), which describes a materials strain as a response to change in temperature. As materials in a power device expand and contract in response to operational power cycles, fatigue begins to structurally weaken the multi-material stack-ups which define the device [35]. After a certain number of these cycles, failure in the form of cracking, delamination, or shorting is unavoidable.

Table 1: Table of CTE values which demonstrates the variability between common power electronic device materials [9], [12], [36], [37].

Material	Coeff. Thermal Expansion – 10^{-6} * [C^{-1}]
Al - 99%	23.6
Cu - 99.9%	16.9
EMC Glass Filament	15
Alumina	8.1
Aluminum Nitride	4.5
Silicone Fiber Glass Filament	50
SiC	10.3
SAC 305	40
Au	15
Ag	20
Nylon	144
Graphite	2
Platinum	9.1
Silicon	2.5
Pb/Sn Eutectic Solder	29
Nickel	13.1
Zinc	31.2
Diamond, Natural	1.18
GaN	3.16

Some of the most influential warping in electronic assemblies comes from molding, or encapsulation, layers which typically have CTE values that are very different from the conductors which they protect [38]. Efforts have been made to mitigate some of the stressing caused by molding materials by varying filler sizes and shapes to reduce residual stresses and change their thermal properties, but even the best materials for thermal matching will generate some warpage

related stresses if they are attached to multiple different material types [39], [40]. Even during fabrication, fatigue during bonding processes is known to cause multiple out of plane deformations, resulting in a reduced fatigue life of substrates and interconnects [41]. TM stresses are therefore of interest in power devices, as they will impact the reliability of the system [42]. Because all system architectures are different, TM stresses can create any mechanical loading condition on components, such as compression, tension, shear, and so called "peeling" stresses, all of which can cause several different failure types [43], [44]. Aside from their obvious critical stress thresholds where overstress failures would present themselves and the previously described cyclic fatigue scenarios, stress migration of existing voids within conductor materials are also very real possibilities for failure. In conductors, tensile regions tend to nucleate voids while compressive stress regions will be areas that voids will tend to migrate to, causing a collection of regional voids over time in compressive regions, resulting in reduced cross-sectional areas and reduced conductor efficiencies [23]. As mentioned in the previous section, thermally and electrically driven void migration can also take place within conductor materials, demonstrating that regions of high thermal and electrical stress in power devices may be susceptible to a variety of void migration mechanisms which could result in significantly reduced lifetimes if allowed to act simultaneously.

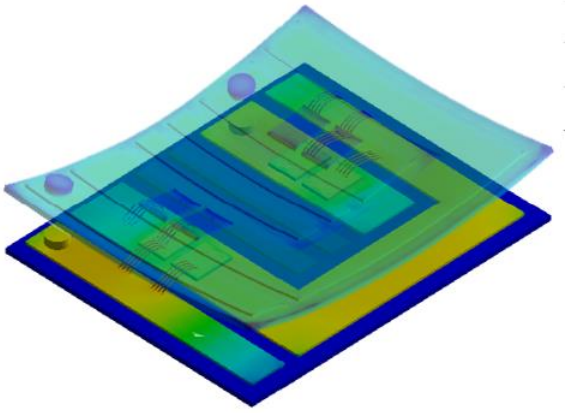

Figure 7: Image of simulated board deformation resulting from thermal stressing.

1.1.2.3. Combined Stress Failure

As the potential for increased TM and electrical stresses rises with miniaturization, their contributions to device failures will do the same. It has been demonstrated that void migration, metallization, and delamination all contribute to aging in electrical systems [45]. This emphasizes the need for the incorporation of multi-mechanism lifetime models into the design optimization process in future power electronic systems. The introduction of multi-stress models is not, on its own, a novel concept in electronics packaging. For example, some studies have demonstrated the use of modified or "effective" activation energy terms to better represent the combined influence of multiple stresses, while others have used Eyring models to incorporate different types of mechanisms into the same set of calculations for one total lifetime estimate [46], [47]. There are benefits and drawbacks to the use of different models. For example, Eyring models are typically used when failure mechanisms do not interact with each other. Specifically related to mechanical fatigue, it has been demonstrated that multi-failure analysis procedures are more reasonable compared to a dominating single-failure mode analysis techniques at electrical interfaces [48]. Specifically related to thermal analyses, time-at-temperature models have been shown to better represent material-dependent, thermally induced, processes compared to damage-cycle models, which do not necessarily account for the more arbitrary nature of real-world mission profiles for interface degradation in power modules [49]. Therefore, multi-stress models do improve reliability analysis in electronics, but the physics of interacting failures over intricate power cycles is complex, and no one model has been put forward which fully captures the interaction between EM and TM for all components in a power electronic system. So, it is paramount to better understand the interaction between these mechanisms at critical locations in power systems to increase the robustness of next-generation devices.

1.1.3. Interconnects

In power electronic devices, there are a multitude of strategies for interfacing or attaching two separate conductor materials, all of which are broadly (and aptly) described as interconnects [9], [12]. Interconnects can serve as avenues for heat dissipation, signal direction, or the supply of power, all of which also effect the reliability of the interconnect. Interconnects usually win the title of smallest individual parts within a power system, making them particularly sensitive to several electrical and mechanical failure mechanisms, classifying them as critical points in a system [45]. Some of the most notable interconnect methods are various solder ball arrays, solder layer attachments, and wire bonds.

Solder materials and wire bonds have their tradeoffs in terms of integrability into certain system or device layouts. For example, solder materials have enabled the miniaturization of power devices by creating opportunities for double sided cooling system layouts but also require reflow processes which can leave behind residual mechanical stresses within a system prior to even being used in operation. Some of the most common solder materials, such as SAC305, have low melting temperatures and thus may not be capable of being integrated into high density power systems. Alternatively, high-temperature solders, which can endure high temperature operation, are significantly more expensive and are therefore less desirable. Wire bonds, on the other hand, are usually made of materials which are more stable at high temperatures, such as aluminum, gold, and copper.

1.1.3.1. Wire Bonds in Power Devices

Wire bonding is one of the most common interconnect attachment methods used in electronic packaging [9], [12], [50]. Some of the most common categories of wire bonding include, but are not limited to, wedge bonding, ball bonding, and ribbon bonding, all of which have

tradeoffs related to their use in specific system configurations but are nonetheless advantageous because of their ability to be easily integrated into numerous different component geometries. When a system design requires wire bonding attachment processes, bond material, length, cross-sectional geometry, bond pad materials and geometry, and fabrication temperatures and speeds are all considered to optimize a designed system, device, or component.

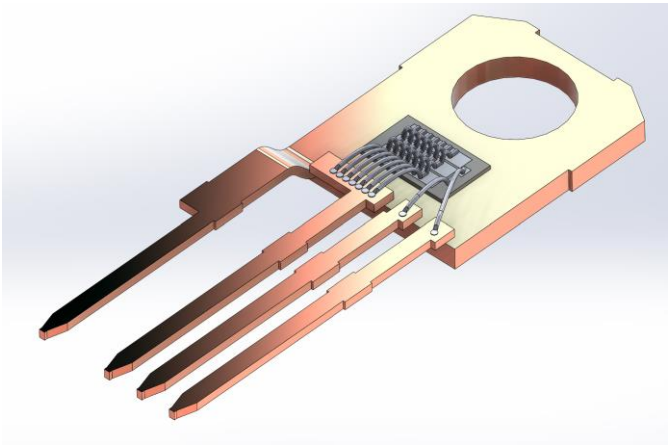

Figure 8: Image of CREE SiC MOSFET utilizing wedge bonds for drain-to-source power connection.

Ultrasonic bonding has become one of the most common practices in the power electronics industry due to its relatively reduced fabrication cost and low bonding temperatures [50]. Because ultrasonic wire bonds are so common in power devices, it is advantageous to examine their behavior under the combination of EM and mechanical stresses in anticipation of the potential for their interaction to impact power electronic device lifetimes in future system architectures.

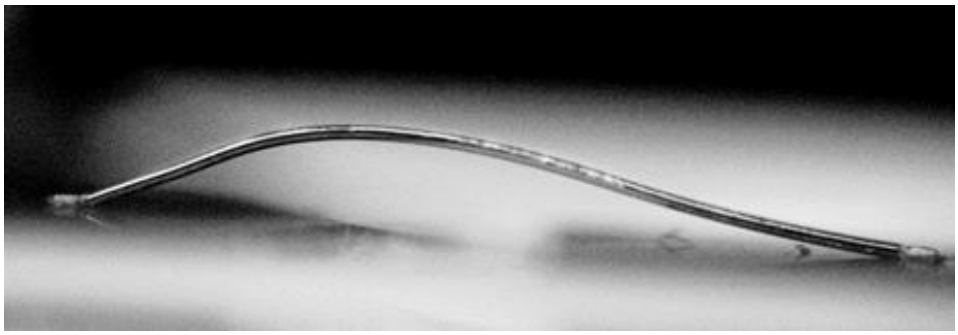

Figure 9: Example of standard 5 [mil] aluminum wire bond.

1.2. Thesis Overview

The probability that multiple interacting failure mechanisms will influence the lifetime of next-generation power electronic systems will continue to increase as power density increases. Because it has not been well explored in literature, this thesis demonstrates the specific analysis of the combined effects of EM and mechanical stresses on the lifetime of wire bonds because of the acknowledgement of the impacts that power electronic advancements will have on wire bond and system reliability. Elucidation of these effects can provide guidance for the development of more robust next-generation power electronic systems.

The lifetime effects of this combined stressing scenario will be experimentally derived in Chapter 2 through accelerated testing methods, which have been shown to be effective at extrapolating to use conditions for electrical conductors in single and multi-stress scenarios [51], [52]. Quantification of these effects will be accomplished by developing a multi-stress lifetime model based on experimental results and statistical analysis. A variety of multi-stress lifetime models have been demonstrated in several studies to outperform single failure mechanism models [46]–[49].

Finally, in Chapter 3, the implementation of the combined stressing model is demonstrated in the case study of a set of next-generation grid-tied solar inverters. The analysis of the systems is aligned with reliability analysis techniques which consider likely failure mechanisms during device operation and estimate lifetimes based on weak points in a system using models for those specific failure mechanisms [53], [54].

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2. EFFECT OF COMBINED ELECTROMIGRATION AND MECHANICAL STRESS ON ALUMINUM WIRE BOND LIFETIME

Co-Author: David Huitink

2.1. Abstract

In this study, 5 [mil] aluminum wire bonds are subjected to elevated ambient temperatures, current densities, and mechanical stresses using a novel accelerated testing mechanism. Failure of a wire bond in this study was a 10% increase in electrical resistance. Temperature coefficient of resistance experiments in this study identified the wire temperatures resulting from joule heating and thermomechanical stress evaluations were completed using ANSYS to extract relevant stresses occurring at each experimental condition. Collection of the failure data and analysis of the results indicate that mechanical stress interacts with current density and that the introduction of externally applied mechanical stress reduces the lifetime of a wire bond. Comparisons have been drawn between time to failure estimates for Black's equation for electromigration and a stress-modified model based on Black's equation which was developed based on the results of this study. The comparison indicates that Black's equation is insufficient when mechanical stresses interact with current density and that mechanical stress will need to be considered in the future when completing reliability evaluations for wired interconnects.

2.2. Introduction

Power electronic devices have and will continue to be miniaturized to meet the demands of globally increasing energy consumption [1]–[3]. As device sizes decrease, interconnect responses to electromigration (EM) and thermomigration (TM) behavior become more severe [4]. In power electronic systems, the EM and TM effects of joule heating and current crowing represent a system weakness which can cause losses in system efficiency or, in worst case scenarios, system

failure to deliver required power [5], [6]. Additionally, thermal expansion effects also introduce mechanical stressing on interconnects. As EM and TM are allowed to act on interconnects and systems in parallel with externally applied mechanical stressing, their collective damage exponentially grows [7]. Therefore, it is advantageous to quantify the collective impacts of current density, conductor temperature, and mechanical stresses in interconnects to enable accurate reliability estimation for next-generation power electronic devices.

Aluminum ultrasonic wire bonding is one of the most popular bonding methods used in power electronic devices because of its low working temperatures and costs [8]. Because it is expected that power device fabrication will continue to utilize wire bonding processes for the foreseeable future, this study aims to shed light on the combined failure mechanisms of current density, conductor temperature, and mechanical stresses and their collective impact on wire bond lifetime over a range of accelerated experimental conditions.

2.2.1. Electromigration

EM is a failure mechanism resulting in structural degradation of a conductor under electron flow and elevated temperatures [9]. Structural degradation of the conductor typically reveals itself as an increase in conductor electrical resistance or a reduction in efficiency. Common characteristics of EM failures include the nucleation and migration of voids, bambooing, grain structure realignment, and hillock or whisker formation at locations where migrated conductor material has been deposited [9], [10]. EM degradation manifests itself at locations in a conductor where temperature and current density crowd, increasing the localized electrical and thermal potential for atomic mobility [5]. EM is a failure typically classified as a wear-out failure, meaning that EM failures occur after long durations of time [11], [12]. By increasing current density and conductor temperatures, EM is accelerated, causing a reduced lifetime compared to more benign

conditions, which is corroborated by the fact that most failure mechanism degradation rates directly relate to component temperature [13].

As device sizes continue to shrink, the maximum tolerable current density for conductors follows suit [14]. Increasing power requirements and increasing operating temperature capabilities spell problems for wire bonded interconnects in next-generation power devices with respect to EM failures. Wire bonds connected to high-temperature junctions, such as SiC or GaN, will need to endure higher temperatures and current densities than they have been required to in the past, increasing the likelihood of EM failures at critical components in power systems [3], [15].

2.2.2. Thermomechanical Stress

Thermomechanical stresses occur because of temperature changes across or around a conductor. The coefficient of thermal expansion (CTE), a property which broadly describes a materials strain under a change in temperature, varies from material to material. Multi-material stack-ups, such as those seen in power electronic assemblies, will expand and contract as a response to temperature, over time resulting in thermal fatigue of the system [16]. In an electronic assembly, each layer or embedded component will deform at different rates, creating a cascade of thermomechanical stress concentrations throughout the system [6], [17]. These stress concentrations can severely influence the reliability of components at so called “hot spot” locations in a system, causing fatigue, delamination, voiding, or any combination of the three [9], [11], [18].

In wire bond interconnects, current density, cooling mechanisms, bond location, bond material, bond pad material, substrate material, and encapsulant material will all impact the resultant stresses inside of the wire [19], [20].

2.2.3. Combined Stress Failures

Multi-mode failures in components are described as two or more separate failure mechanisms occurring simultaneously and collectively causing failure, usually resulting in a reduced lifetime compared to any one failure mode acting alone. In the case of electrical conductors, Glavanovics et al. demonstrated that thermomechanical and electrical failures impact device failure in wire bonds by accelerating aging effects [6]. Yao et al. explained that increased duty cycles increase damage growth rate for both TM and EM [7].

In terms of modeling combined stress failures, several methods have been proposed with varying results, such as modified versions of Black's equation, Eyring models, Arrhenius models, and effective activation energy models to name a few [21]–[24]. In most cases, modified models or data-driven multi-stress models outperform models which do not consider all influencing failure mechanisms, leading to the need for such models to be developed and introduced as next-generation power electronic equipment is shrunk and multi-stress failures are anticipated to become more common.

2.2.4. Accelerated Testing

An accelerated test will subject a sample to excessive condition levels to produce failures in a short amount of time relative to the expected failure time under the intended use conditions. When failure modes are achieved in an accelerated fashion, the results can be extrapolated to the intended use conditions, providing an estimation of lifetime for a component or system under the specifically identified failure [11]. Accelerated testing data can also be used to observe the differences in life response of an electrical conductor under varying stresses [25]. Thus, an accelerated test which subjects a wire bond to multiple stresses can yield results which will indicate

possible interactions between the stress influences and be used to estimate accelerated and use condition lifetimes [26].

2.3. Materials and Methods

2.3.1. Test Condition Definition

To create an accelerated test that produces EM failures in a wire bond, the combination of current density and temperature of the bond must represent quantities significantly higher than those expected in a comparable power electronic bond. After analyses were performed for evaluating designs of a next-generation grid-tied solar inverter (as a part of one funding agreement for conducting this study), it was found that 5 [mil] aluminum wire bonds in the MOSFETs of the inverter design would endure maximums of ~8300 [A/cm^2] at ~93 [C] (the highest current density and temperature conditions of all wire bonds and other interconnects in the system). Therefore, the EM failure conditions used in this study represent stress levels well above those of a next-generation benchmark and conditions that will assist in evaluating wire bond performance in other similar failure mode scenarios in other next-generation power electronic systems.

As device miniaturization continues, the potential for multi-failure mode interactions at interconnect levels in power electronic systems will increase. Accordingly, this study looks to reveal some of the lifetime effects of the multi-stress interaction combination of EM and mechanical stresses in wire bonds. Having already established the baseline for accelerated EM conditions, the introduction of mechanical stress (in the form of an applied displacement) on wire bonds under the same accelerated EM conditions will provide the opportunity to draw comparisons between EM results and combined EM and mechanical stress results in terms of lifetime. DBC substrates, commonly used in power electronic modules for their high thermal conductivities and structural stability, can experience out of plane deformations up to 93 [μm] due to thermal

gradients of 350 [C] for a substrate floorplan of 35 by 15 [mm^2] [27]. Because this geometry is well aligned with common power module floorplans used today, it is reasonable to assume that modules of the same size or smaller will experience similar or smaller thermal expansion effects at operating and fabrication temperatures. These out of plane deformations also correspond to a DBC pad separations of up to 5 [μm]. Therefore, an accelerated test which subjects wire bonds to an applied linear displacement corresponding to DBC pad separation would need to impose a linear displacement greater than 5 [μm] to a wire bond sample.

To align this study well with common power electronic industry practices for wire bonding and ease of access to existing equipment for sample fabrication, 5 [mil] aluminum wire bonds have been selected as the test sample in this study.

Table 2: Experimental testing conditions.

Combined EM and Mechanical Stress Conditions		
EM Conditions*		
Current Density [A/cm²]	Ambient Temperature [C]	Applied Displacement [μm]
23684	100	0*
		20
		40
31578		60
		80
	125	100
39473		120
		140

To quantify the effects of the accelerated testing conditions in Table 2, the wire bond samples in this study were monitored for an increase in electrical resistance of 10%, which is a benchmark indicator in industry that an electrical component will need to be repaired or replaced because it represents reduction in system efficiency [28]. Thus, the time to 10% increase in resistance (TT10%IR) is used in this study for comparing the lifetime of bonds subjected to the experimental conditions.

$$10\% = 100\left(\frac{R_{TT10\%IR} - R_{initial}}{R_{initial}}\right) \qquad (1)$$

It also must be noted that at current densities as high as those being used in this study, joule heating effects will influence the prediction of wire bond temperatures. The "Evaluation of Thermal-Electric Properties" section of this article addresses these effects. Additionally, the application of elevated temperature and applied displacement to a wire bond inherently creates mechanical stresses within the bond. The relationship between temperature, displacement, and stress in a wire bond sample is addressed in the "Evaluation of Mechanical Stress Conditions" section of this article.

2.3.2. Experimental Setup

Two identical novel fixturing mechanisms were designed and built to study the combined effects of EM and mechanical stress on the lifetime of a wire bond. Simple in principle, the mechanisms allow for the supply of constant electrical current (by means of a Keysight E36312A or AimTTi MX180TP 375W low-noise power supply) across a series of wire bonds which are fixed in space at the first bond location and attached to a linear translation stage (Newport UMR3.5) at the second bond location so that a combination of electrical and mechanical stresses can occur in the wire bonds simultaneously. The sample fixturing stages have been outfitted with an adjustable locking structure so that the applied displacement condition is maintained for the duration of a data collection session. This entire assembly was attached to an oven rack and was brought to elevated ambient temperatures inside of an oven (Cascade TEK TFO-1).

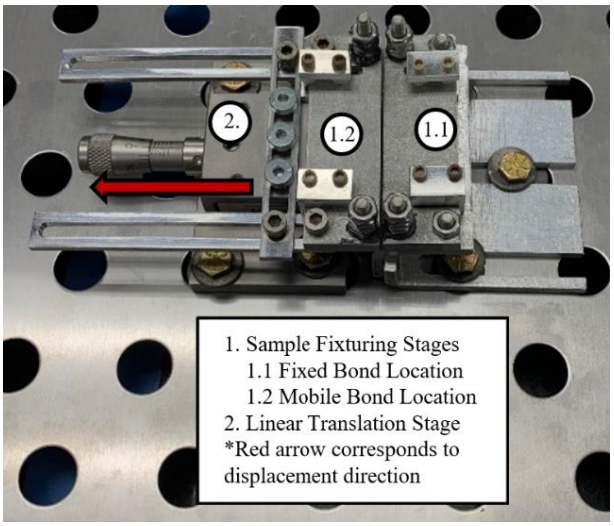

Figure 10: Labeled novel fixturing mechanism.

To determine the TT10%IR across a given wire bond, in situ resistance measurements were taken at a sample rate of 0.2 [S/s] using a DATAQ DI-4208-E high-resolution voltage measurement module. For a very low electrical resistance conductor, such as an aluminum wire bond, measuring electrical resistance in situ is easily done using a 4-point measurement technique, sometimes called Kelvin resistance measurement. So, the voltage measurement probes from the voltage measurement module were connected in parallel to the power supplies to create a Kelvin resistance measurement configuration.

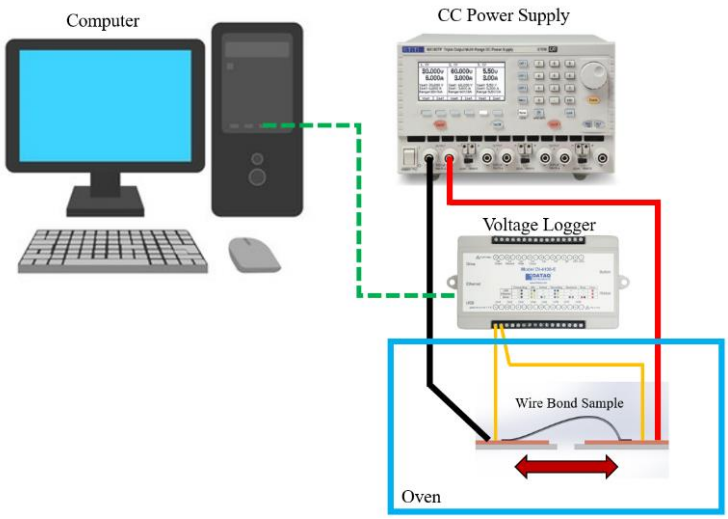

Figure 11: Basic experimental setup diagram.

Therefore, an applied electrical current up to 15 [A], ambient temperature up to 295 [C], and linear wire bond stretch up to 450 [μm] can be applied to a given wire bond sample with this setup and the change in resistance of the bond can be monitored over time, meeting all criteria needed to conduct experiments at the defined testing conditions.

2.3.3. Sample Preparation

To mimic the structure of common power electronic devices, wire bonds in this study were wedge-wedge bonded to direct bonded copper (DBC) pads on alumina cards by ultrasonic bonding using an Orthodyne Model 20 manual bonder. The first and second wire bond locations for each wire sample were bonded to their respective pad locations using a 250 [ms] bond time, 125 [g] of applied mass, and 160 and 170 [mW] of power, respectively. Prior to wire bonding, each bond pad was outfitted with a bent steel wire nail as a probing connection point using SAC305 solder paste for connecting to the previously described power supplies and data acquisition module. After connecting the probing points, each sample card was cleaned in a sonic bath for 2 minutes with acetone to remove oxidation layers and flux left behind during the reflow process. To address concerns related to possible EM effects in the DBC copper portions of the sample coupons, due to the large difference in electrically conductive cross-sectional area and copper's higher resistance to EM effects compared to aluminum, it is assumed that EM effects will manifest in the wire bonds much earlier than in the copper pads [26].

The sample cards described above fall into two categories within this study, one where the bond pads are connected by the alumina layer and a wire bond, and another where the pads are only connected via a wire bond. The first category of cards was used as the control group in this study, serving as the test vehicles for collecting data points on wire bonds that were only subjected to elevated current densities and ambient temperatures. This group of cards was labeled as the "EM

only" group and is referenced this way in the remainder of this study. The second category of cards was used as the treatment group, where the wire bonds were subjected to the same conditions as the EM only group with the addition of an applied mechanical stress using the previously described novel fixturing mechanisms. This treatment group has been labeled as the "Combined stressing" group and is noted this way for the remainder of this study. To bond the separated pads in the combined stressing group, the novel fixturing mechanism was also designed to be configured for fixing the pad cards during the bonding process.

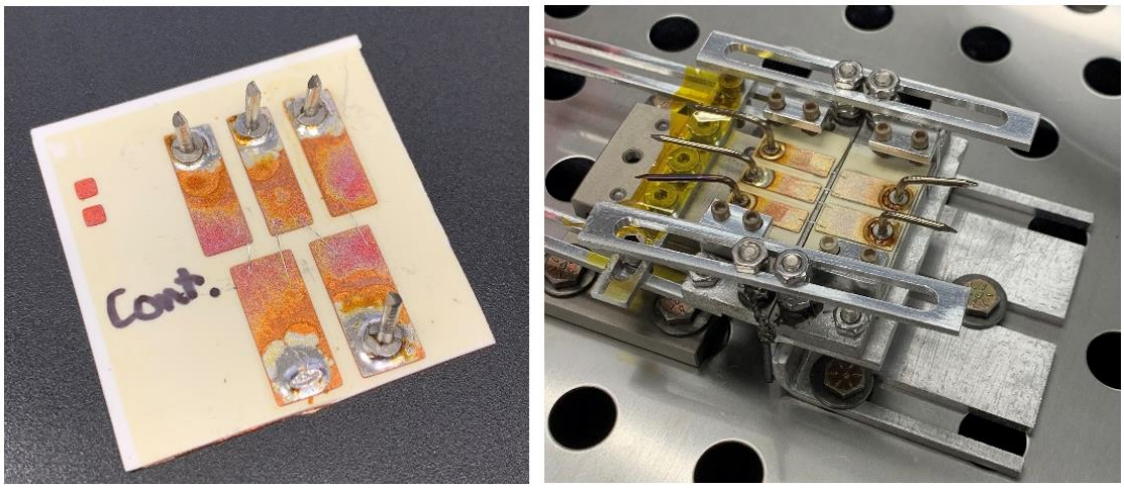

Figure 12: Examples of sample coupons for EM only conditions (left) and Combined stressing conditions (right).

2.3.4. Evaluation of Thermal-Electric Properties

Because an aluminum wire bond experiencing elevated current densities will dissipate heat, an effect known as self or joule heating, determination of the corresponding temperature rise within the bond must be quantified to correctly represent the temperature of the wire at the set experimental conditions. Fortunately, the electrical resistivity of a conductor typically has a positive linear relationship with the conductor's temperature, described by a term known as the temperature coefficient of resistance (abbreviated as TCR and usually represented by the Greek letter; α). Because the electrical resistance of a conductor is directly proportional to its electrical

resistivity, the resistance of the conductor has the same relationship with temperature as its resistivity. To find the TCR for the 5 [mil] aluminum wire bonds being used in this study, a series of 20 Kelvin resistance measurements were taken at 22-125 [C] across current densities ranging from 521-39,473 [A/cm^2] on a single wire bond sample. Measurements at 521 [A/cm^2] were taken using a GW Instek LCR-6002 while measurements at higher current densities used the combination of a Keysight E36312A low-noise power supply and DATAQ DI-4208-E high-resolution voltage measurement module. Ambient temperature was controlled by placing the wire bond sample and probing wires inside of a Cascade TEK TFO-1 forced air lab oven.

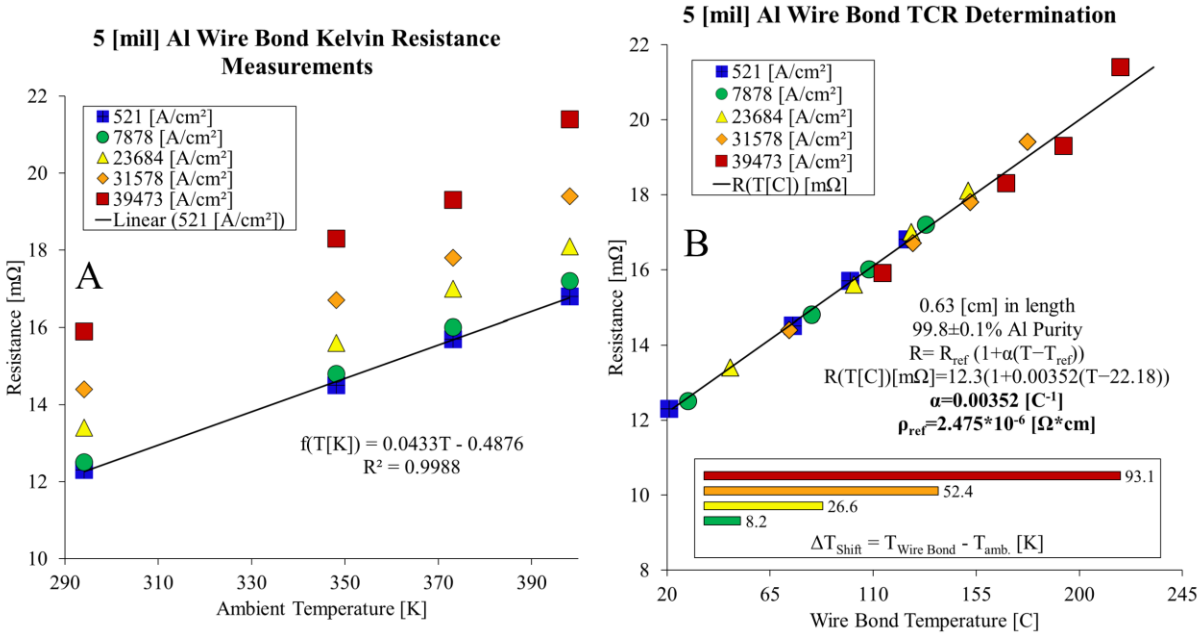

Figure 13: Kelvin resistance measurements for 5[mil] Al wire bond. A: Raw data measurements; B: Temperature shifted measurements for extraction of TCR.

At the 521 [A/cm^2] current density condition, joule heating effects were assumed to be negligible, and therefore the wire was assumed to be at the same temperature as the surrounding air. Using this assumption, the linear regression line in Figure 13A was used to define the relationship between the temperature and resistance of the wire bond. Using this equation, it was found that the TCR of the wire bond was $\alpha = 0.00352$ [C^{-1}]. A temperature shift was applied to the

ambient temperatures corresponding to the elevated current density conditions to fit the measured resistance values to the expected resistance values predicted using the TCR (see Figure 13B), allowing for estimation of the actual wire bond temperature at the experimental conditions (see Table 3).

Additionally, the reference electrical resistivity (resistivity at 22 [C]) of the wire bond was estimated to be $\rho_{ref} = 2.475 \cdot 10^{-6}$ [Ω·cm], as the measured resistance and wire diameter were known, and the length of the wire could be very closely approximated based on sample fabrication parameters.

Table 3: 5 [mil] Al wire bond temperature estimations at test conditions.

Current Density [A/cm²]	Ambient Temperature [C]	Wire Bond Temperature [C]	Dissipated Power [mW]
23684		126.6	153
31578	100	152.4	284.8
39473		193.1	482.5
23684		151.6	162.9
31578	125	177.4	310.4
39473		218.1	535

The estimated wire bond temperatures, TCR, and reference electrical resistivity enable proper analysis of results after the collection of TT10%IR data points and define the appropriate material properties and simulation conditions for gathering estimates of mechanical stresses in the following section.

2.3.5. Evaluation of Mechanical Stress Conditions

Quantifying the effects of applied displacement and thermal expansion in terms of stress is preferred for modeling lifetime effects because it is a metric which can be determined for any material or geometry, thereby making a stress term in a model more easily translated to multiple types of materials or geometries. To determine the stresses resulting from applied displacement and thermal expansion, ANSYS simulations were performed on a 3D modeled wire bond connected to DBC pads.

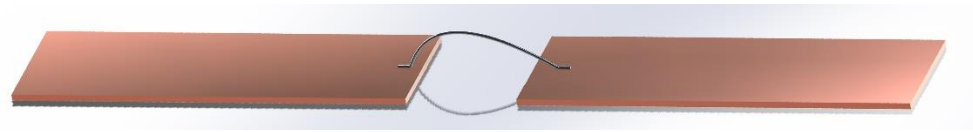

Figure 14: 3D model of 5 [mil] Al wire bond and DBC pads.

The ANSYS simulations consisted of a thermal-electric evaluation of the model under the accelerated testing conditions for EM only, which exported the resulting thermal profile into a transient structural simulation where each of the displacement conditions were applied to the model, resulting in the output of several stress values associated with the combined thermal gradients and applied displacement conditions. Material property data was imported to ANSYS from the previously described TCR results and *Physical Property Algorithms* by Stelzer [29].

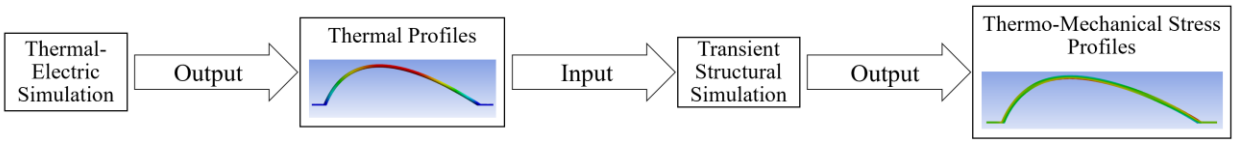

Figure 15: Block diagram describing steps taken to accomplish ANSYS simulations.

The thermal profiles from the thermal-electric portions of these simulations indicated that maximum temperatures and current densities in a wire bond subjected to the testing conditions in this study are endured by the center portion of the wire, known as the loop of the bond (see Figure 17). This indicated that EM driven failures, such as voiding, would initiate in the loop prior to appearing in the bonding locations and that voids would tend to migrate to the loop due to its

increased temperature. However, stress migration effects must also be considered to correctly represent the combined failure conditions in this study.

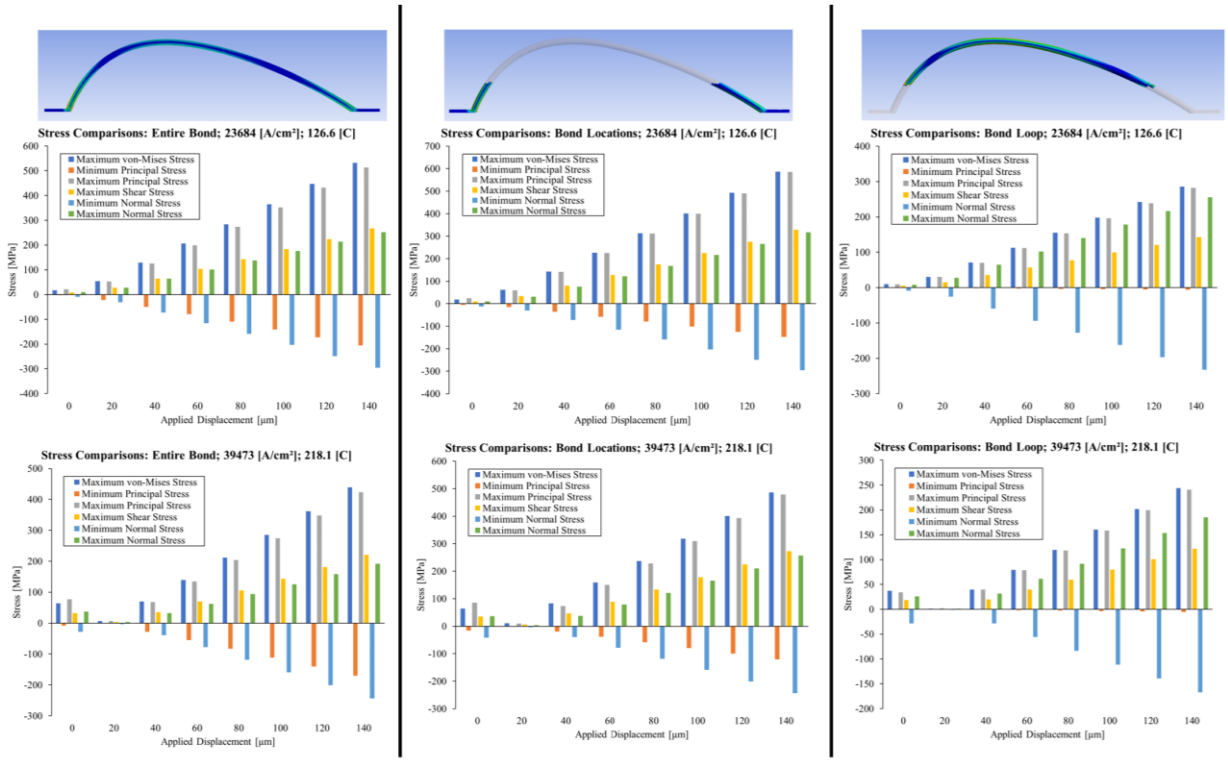

Figure 16: ANSYS thermal-electric and transient structural simulation results for the minimum and maximum stress conditions across the entire wire bond model (left); bond and heel locations of the model (center); and results across the loop portion of the model (right).

Figure 16 demonstrates the key results found by evaluating the thermal-electric and thermo-mechanical stress conditions. A wire bond will clearly endure a variety of stress conditions because of thermal expansion and applied displacement, but which stress condition is the most impactful in terms of accelerating EM failure? By analyzing the loop and bond locations separately in the simulation space, it became clear that as larger displacements are applied, both the loop and bond locations of the wire bond endure high levels of compressive and tensile stresses, in addition to less severe shear stresses. For the bond locations, significantly more shear stress was observed, indicating that the principal stresses were a better metric for describing the normal stress states at the bond locations. For the loop, shear stresses were much lower, indicating that the normal stresses

alone were a sufficient representation of the stress states in the loop. After comparing the principal stresses at the bond locations and the normal stresses at the loop locations, it became clear that the loop would endure the compressive and tensile stresses coinciding with the highest temperature regions, indicating that void nucleation would occur in tensile regions of the loop and that stress migration of voids in the bonds would be predominantly towards the compressed portion of the wire loop. Therefore, the results of the simulation efforts indicate that EM induced voiding is likely to occur at the loop of the bonds due to its heightened temperature and current density and tend to maintain the voids that are initiated there due to its compressive stress state. To justify this conclusion, Vinson et al. demonstrated loop voiding leading to total wire bond failure under the same EM only conditions [30].

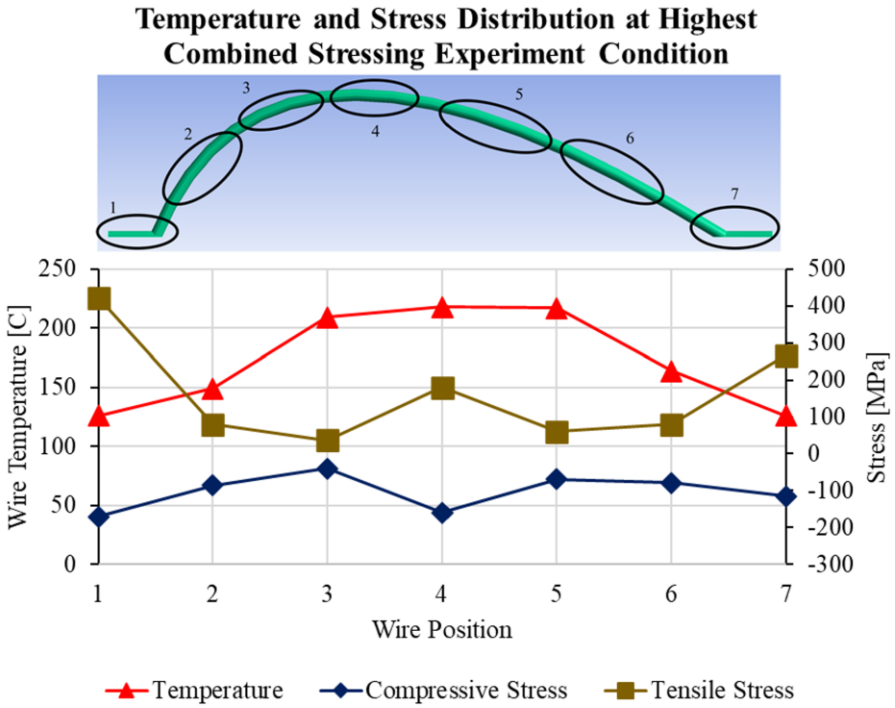

Figure 17: ANSYS temperature and normal stress profiles at highest experimentally stressed condition (125 [C] ambient, 39,473 [A/cm^2], 140 [μm] displacement).

From analysis of Figure 17, it is clear that tensile and compressive stresses increase at the top of the loop of the wire bond, indicating that a selection of one of the two stress value groups

will need to be done to relate the failure data to a corresponding stress state. To align this study with typical use condition stresses for power electronics, comparison of the dominant stresses at the accelerated and use conditions was done and can be seen in Figure 18 [27]. While tensile stress regions in a conductor represent locations where void nucleation occurs, the ultimate contribution to an increase in resistance due to voiding will occur in regions where voids will congregate, effectively reducing the cross-sectional area in that location, thus increasing local current densities and temperatures. Because nucleated voids will travel to compressive regions, the compressive region is an area where the effects of void growth will impact failure the most.

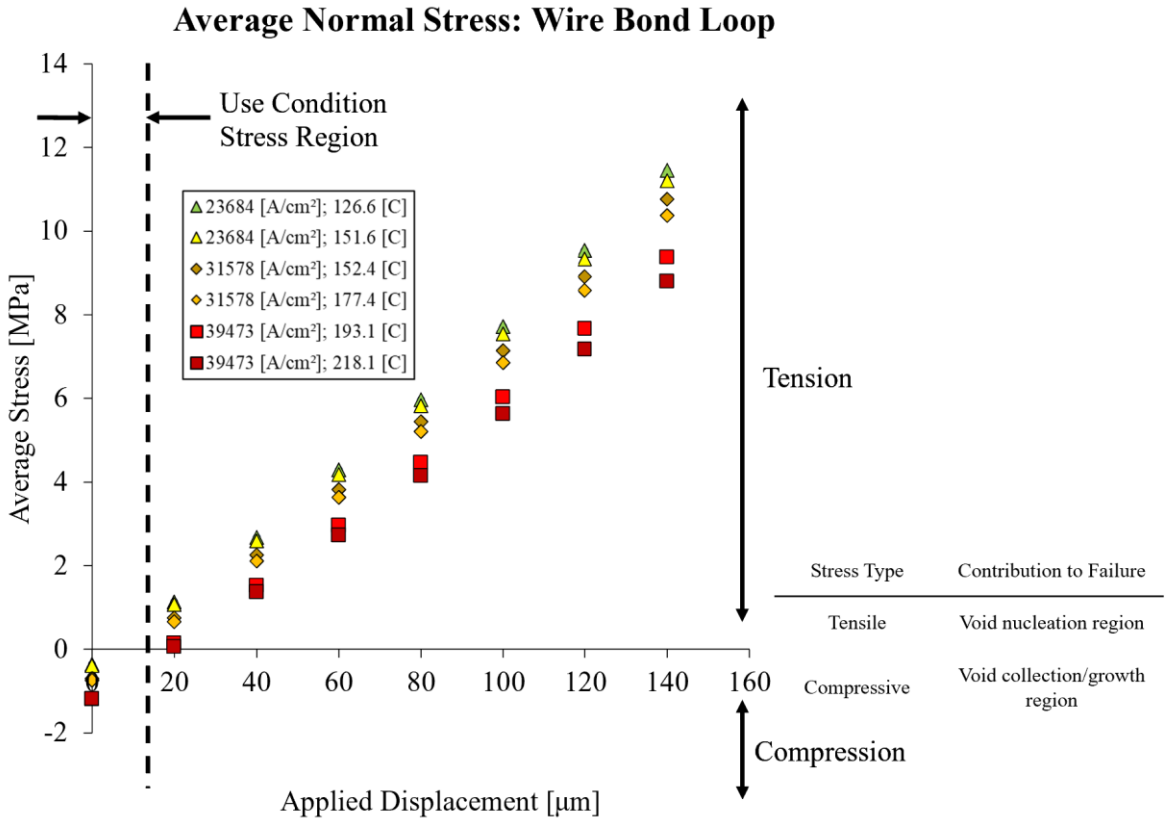

Figure 18: Average normal stresses present in a wire bond loop, annotated with use condition region.

By analyzing the results of these simulations, the extracted values for compressive normal stress in the loop of the wire bond gave estimates for the severity of stress states, provided insight

as to the potential failure locations existing at the various temperature and displacement conditions within the boundaries of the wire model, and provided stress values corresponding to the anticipated failure conditions. Figure 19 contains the collection of normal compressive stress values which have been used to differentiate each individual experimental condition in terms of stress.

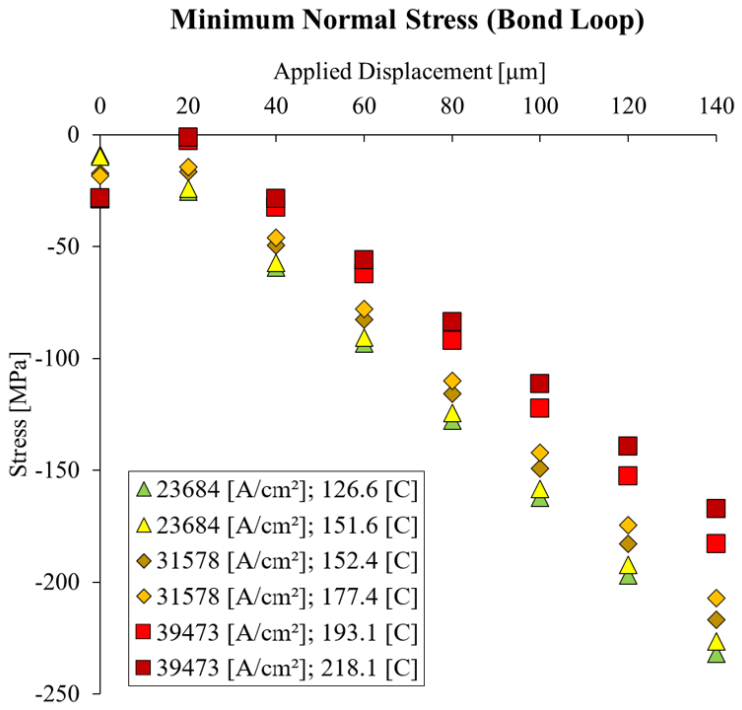

Figure 19: Minimum normal (compressive) stress results for loop portion of wire bond model used for estimating experimental testing conditions.

It must also be noted that for the EM only conditions, the compressive stressing in the wire loop occurs on the underside of the loop and on the top side of the loop in cases of combined stressing.

2.4. Results

2.4.1. Physical Observations

In situ resistance measurements combined with the previously described TCR experiments and ANSYS simulations resulted in the collection of 48 unique testing conditions made up of three

current density conditions, two ambient temperature conditions, and eight displacement conditions with four replications of each condition. This resulted in the overall collection of 192 individual TT10%IR measurements.

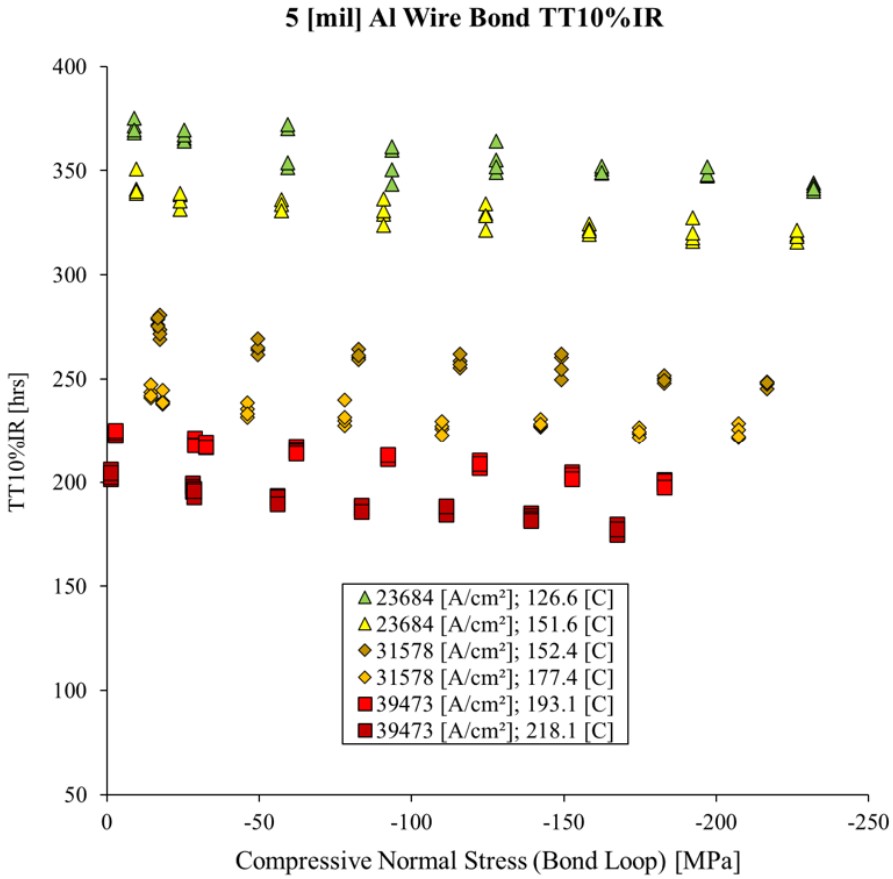

Figure 20: TT10%IR data for 5 [mil] Al wire bond under EM and compressive normal stresses, separated by current density and temperature.

The collection of data depicted in Figure 20 demonstrates the effect of current density, temperature, and compressive normal stress on the 10% increase in resistance lifetime of 5 [mil] aluminum wire bonds. The introduction of mechanical stress reduced the lifetime for all cases, as did temperature and current density.

2.4.2. Statistical Analysis

The results of the data collection were also analyzed statistically as a general full factorial design to identify potential effects of interaction on the TT10%IR and create a statistical model of the wire bond response to the three experimental testing conditions.

Table 4: Identification of impacting parameters on TT10%IR by ANOVA for a general full factorial design.

Analysis of Variance: 5 [mil] Al wire bond

Source	DF	Adj SS	Adj MS	F-Value	P-Value
Model	47	711877	15146	1214.03	0.0000
Linear	10	710597	71060	5695.68	0.0000
j [A/cm^2]	2	664981	332491	26650.3	0.0000
Temp. [C]	1	33246	33246	2664.77	0.0000
Stress [MPa]	7	12370	1767	141.64	0.0000
2-Way Interactions	23	1087	47	3.79	0.0000
*j [A/cm^2]*Temp. [C]*	2	457	229	18.32	0.0000
*j [A/cm^2]*Stress [MPa]*	14	492	35	2.82	0.0010
*Temp. [C]*Stress [MPa]*	7	137	20	1.57	0.1480
3-Way Interactions	14	194	14	1.11	0.3540
*j [A/cm^2]*Temp. [C]*Stress [MPa]*	14	194	14	1.11	0.3540
Error	144	1797	12		
Total	191	713674			

Prior to statistical analysis of the data, values for wire temperature and stress were standardized so that the number of test conditions matched the number of experimental conditions in each category correctly for factorial analysis. The results of statistical analysis indicate that each of the three experimental conditions, the interaction between current density and temperature (EM only conditions), and interaction between current density and normal compressive stress all significantly impact TT10%IR with a 95% confidence interval (P-values<0.05). Interaction between temperature and stress as well as the three-way interaction between all conditions did not significantly impact TT10%IR (P-values>0.05). Based on these results, it is safe to conclude that stress does impact the TT10%IR when EM only and combined stressing conditions are present, and that mechanical stress interacts with current density effects in 5 [mil] aluminum wire bonds.

Figure 21 contains the Weibull plot for all data points based on the factorial analysis. Refer to the last section of this article for the probability plots for each significant and interacting failure mode.

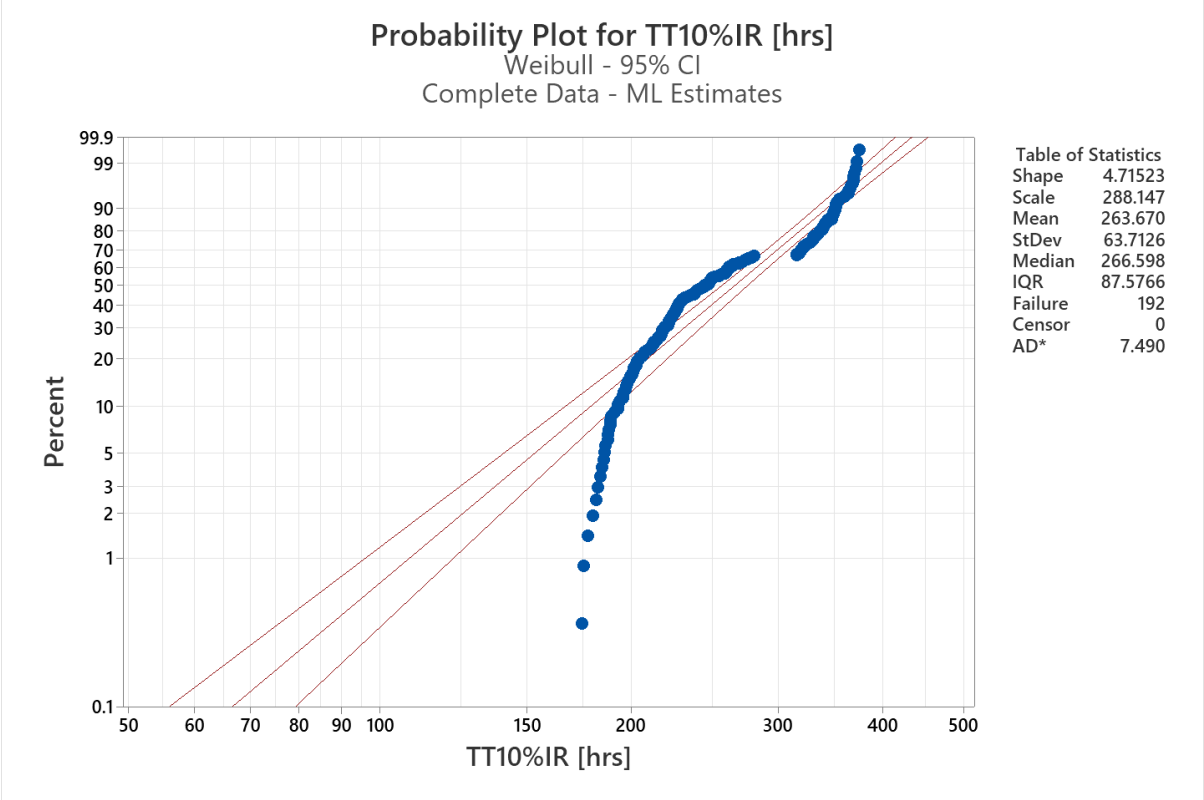

Figure 21: Probability plot for all data points for TT10%IR based on Weibull distribution with 95% confidence interval.

2.4.3. Combined Stressing Impacts

While the raw data and statistical analysis indicate that applied mechanical stressing impacts TT10%IR in this study, quantifying this impact is necessary to more wholistically represent the effect of constant stress on a wire bond which is already enduring EM conditions. To accomplish this, parameters for Black's equation for EM have been extracted for the EM only data points collected in this study.

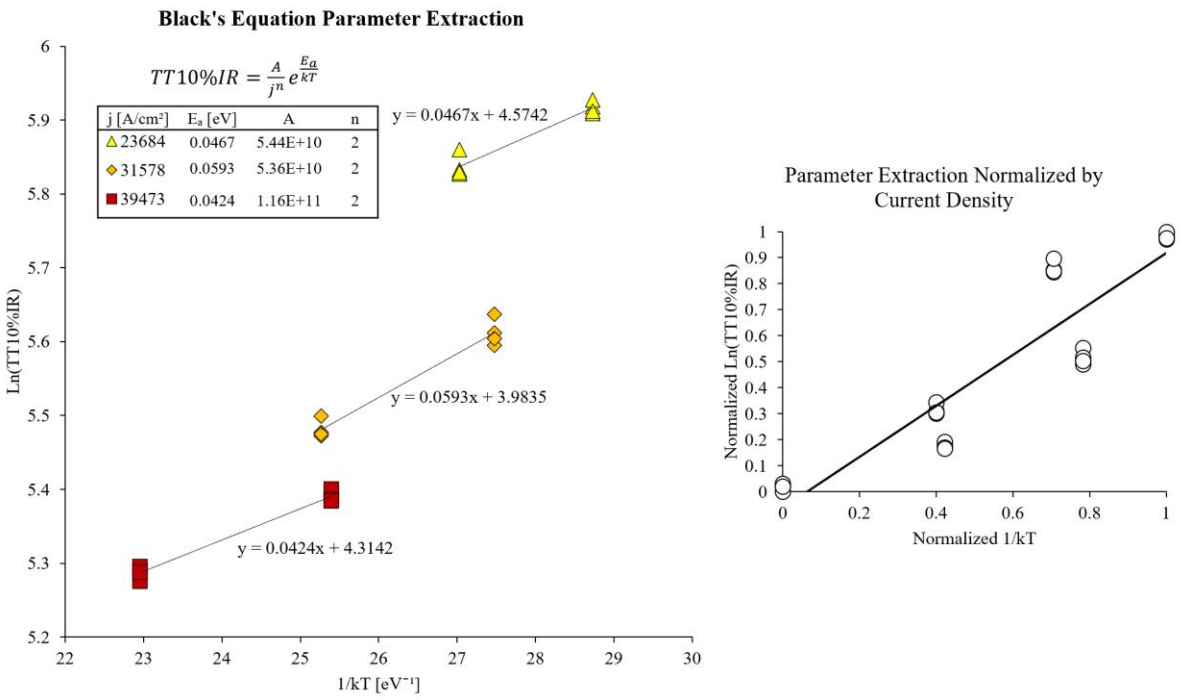

Figure 22: Extraction of parameters for Black's equation for EM only experimental group.

By using the extracted parameters in Figure 22, estimations for TT10%IR can be made for all 48 conditions tested in this study based on the corresponding current densities and wire temperatures for each test condition. Because Black's equation does not account for the reduction in lifetime resulting from mechanical stresses within a conductor, measured TT10%IR values for the combined stressing group in this study will differ from those predicted using the extracted parameters in Figure 22. The comparison between the Black's equation predicted and measured TT10%IR values is depicted in Figure 23.

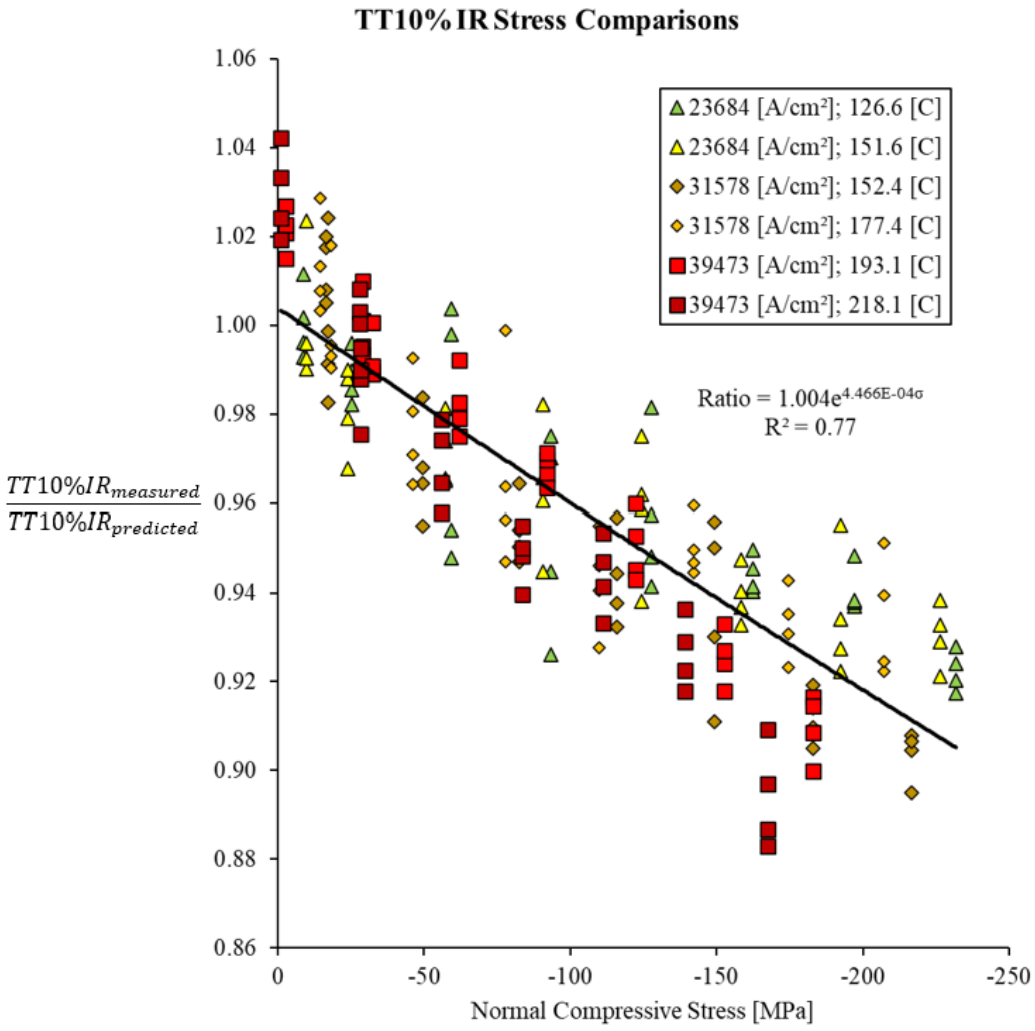

Figure 23: Ratio of measured and Black's eq. predicted TT10%IR values against stress values corresponding to applied displacement experimental conditions.

Figure 23 clearly indicates that the measured TT10%IR values decrease compared to their predicted values as stress is increased in the loop of the wire bond, demonstrating that Black's equation lacks the ability to account for stressing in a wire bond. To account for temperature, current density, and compressive normal stress in the loop of a 5 [mil] aluminum wire bond, a stress-modified model has been developed based on Black's equation and the experimental data. The corresponding comparison between measured and model estimated TT10%IR values is depicted in Figure 24.

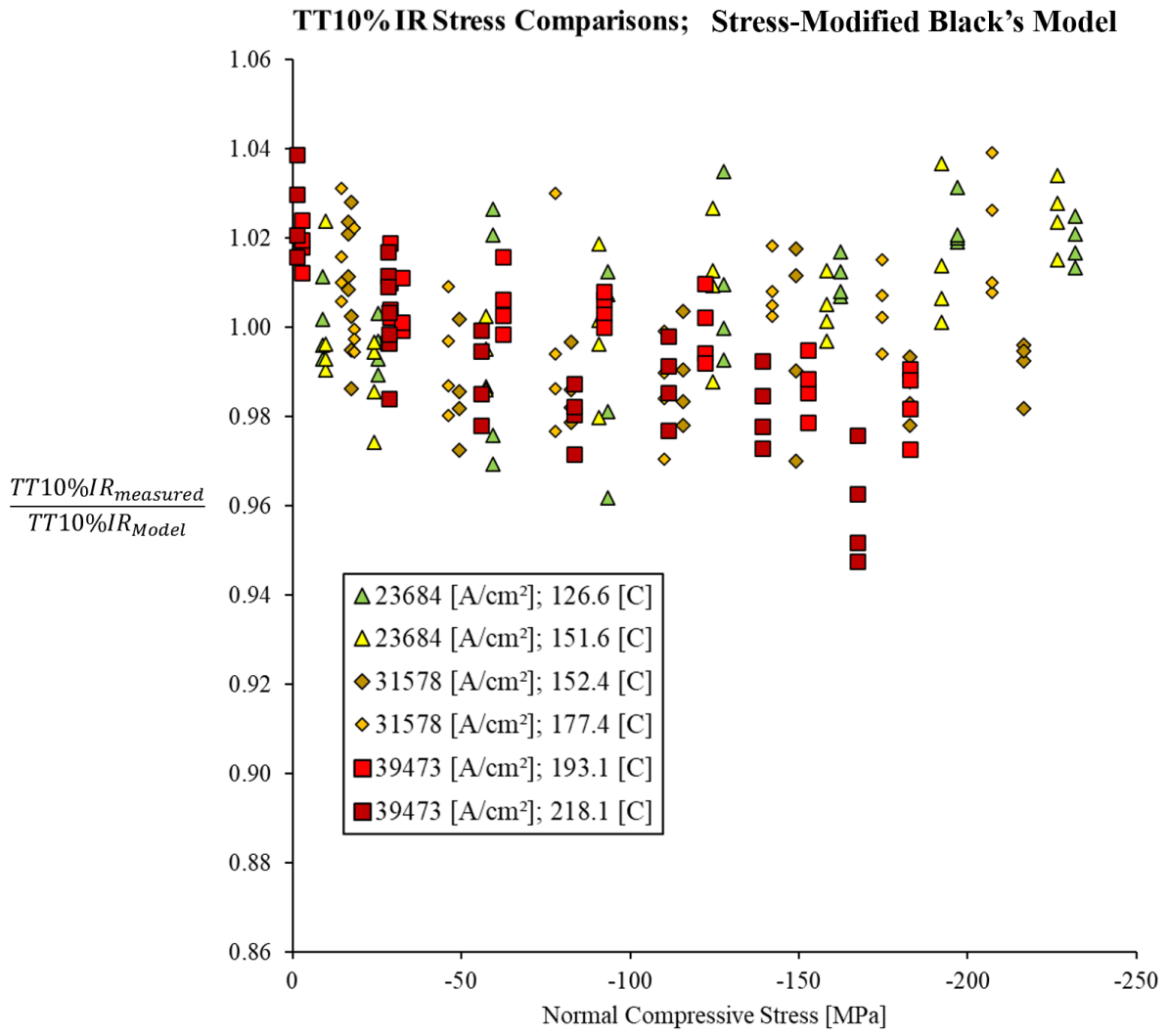

Figure 24: Ratio of measured and proposed stress-modified model predicted TT10%IR values against stress values corresponding to applied displacement experimental conditions

Figure 24 shows much better agreement between the stress-modified model predicted and experimentally measured values as increasing stress is applied to the wire bonds compared to estimates made using Black's equation. Table 5 contains the equation and parameters used for the proposed model.

Table 5: Black's equation, stress-modified Black's model parameters, and comparison of model performance.

Model Comparisons

$$TT10\%IR = \frac{A}{j^n} e^{\left(\frac{E_a}{kT} + \gamma\sigma\right)}$$

	Black's Equation			Stress-modified Black's Model
j [A/cm²]	23684	31578	39473	
A	5.44E+10	5.36E+10	1.16E+11	
n	2	2	2	
E_a *[eV]*	0.0467	0.0593	0.0424	
γ *[eV/MPa]*	0	0	0	4.47E-04
σ *[MPa]*	0	0	0	-245-0
Average measured/predicted TT10%IR		*0.96*		*1.00*

As can be seen in Table 5, the stress-modified Black's model developed in this study outperforms Black's equation when estimating TT10%IR while temperature, current density, and compressive stress are considered. Though 1.00 and 0.96 appear to be values that may not have a significant difference, in this analysis, a difference of 4% corresponds to an average difference in TT10%IR estimation of 15.8 hours compared to the measured value, meaning that Black's equation overestimates TT10%IR by 15.8 hours on average based on the collected data.

2.5. Discussion and Analysis

The results of this study exhibit that constant externally applied mechanical stress introduced to a 5 [mil] aluminum wire bond which is also is enduring EM conditions will reduce the lifetime of the wire bond when compared to EM conditions alone. The experimental conditions used in this study met the criteria for an accelerated test and the results demonstrated that the novel fixturing mechanism designed for this study is capable of producing data at a fidelity high enough to capture the effects of combined stress conditions on wire bond lifetime. The results of these experiments also indicate that compressive mechanical stressing in wire bonds interacts with current density.

Therefore, next-generation power devices which use wire bond connections as conductors for high current densities will need to be evaluated with mechanical stress in mind. Black's equation has been shown in this study to overestimate the TT10%IR when mechanical stress is considered. As device temperatures continue to increase and form factors continue to decrease, mechanical stressing of components due to CTE mismatches will continue to be an influential factor in lifetime estimation of wired interconnects.

Because wire bond geometries widely vary from one package to another, other wire configurations and stress application methods must be explored in future work to continue to establish a working relationship between mechanical stressing and current density. In this study, the loop of the wire bond was the point of analysis for identifying the correct temperatures, current densities, and stresses associated with failure. In a MOSFET, for example, the end of a bond which is connected to the die could be experiencing significantly higher temperatures and other influential degradation mechanisms than those in the loop of the bond, potentially indicating that analysis ought to be focused on the bond location as opposed to the loop of the bond [31].

2.6. Conclusions

In this study, a novel experimental testbed was developed and used to impose elevated current densities, temperatures, and constant mechanical stresses on 5 [mil] aluminum wire bonds to measure the TT10%IR for 48 different combinations of experimental conditions. It was shown through statistical analysis that compressive normal stresses interact with current density conditions and that TT10%IR was reduced as the three experimental condition levels increased. By extracting constants from EM only conditions for Black's equation and combining those factors with the combined stressing conditions, a stress-modified model based on Black's equation for determining the TT10%IR was developed for the three experimental parameters. The developed

model outperformed estimates made by Black's equation, demonstrating that Black's equation is insufficient when externally applied compressive stressing is imposed on a wire bond which is also subjected to EM conditions.

2.7. Acknowledgements

The authors would like to thank the Korea Electrotechnology Research Institute, the Defense Established Program to Stimulate Competitive Research, and the Office of Naval Research for funding and guidance to make this study possible. The authors would also like to the University of Arkansas College of Engineering and Mechanical Engineering department as well as the High Density Electronics Center for access to facilities, equipment, and resources needed for the creation of this study.

2.8. References

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2.9. Additional Statistical Plots

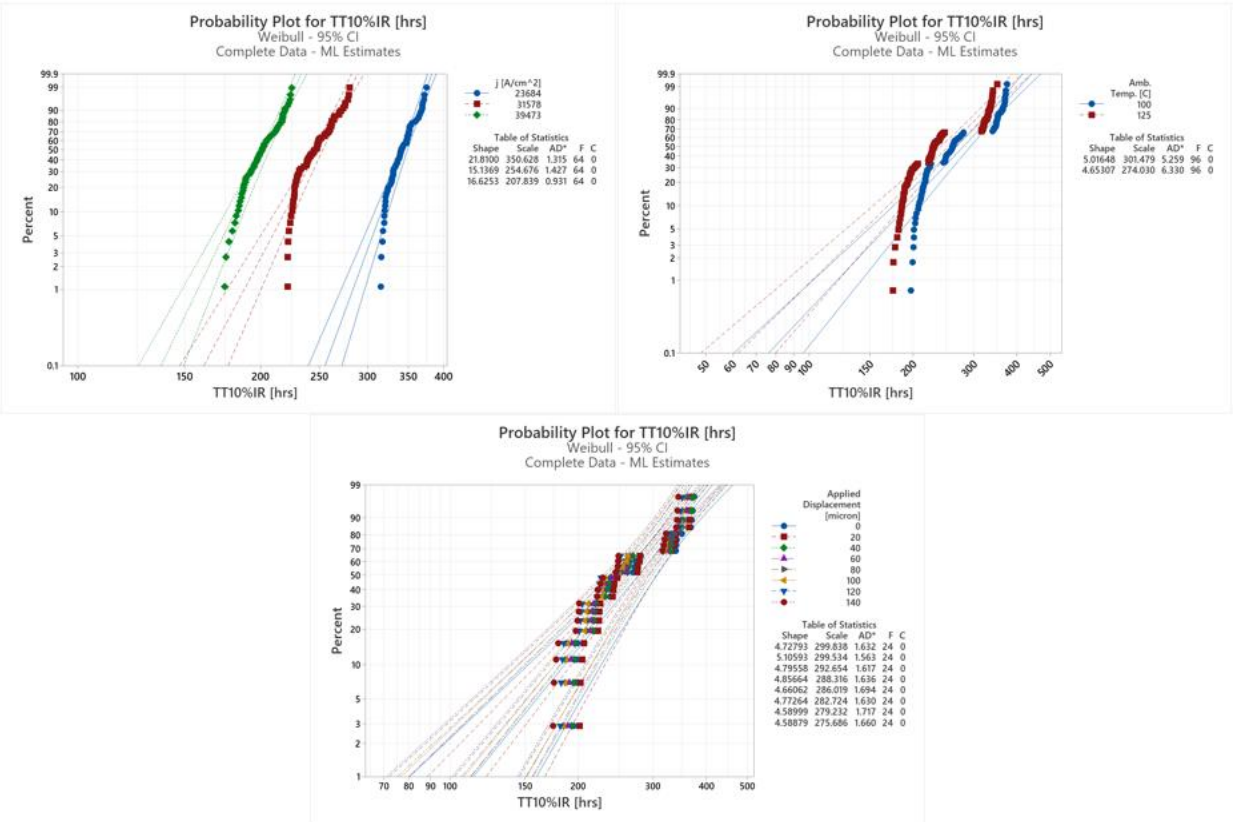


Figure 25: Weibull plots for individual experimental factors of current density (top left), ambient temperature (top right), and applied displacement (bottom).

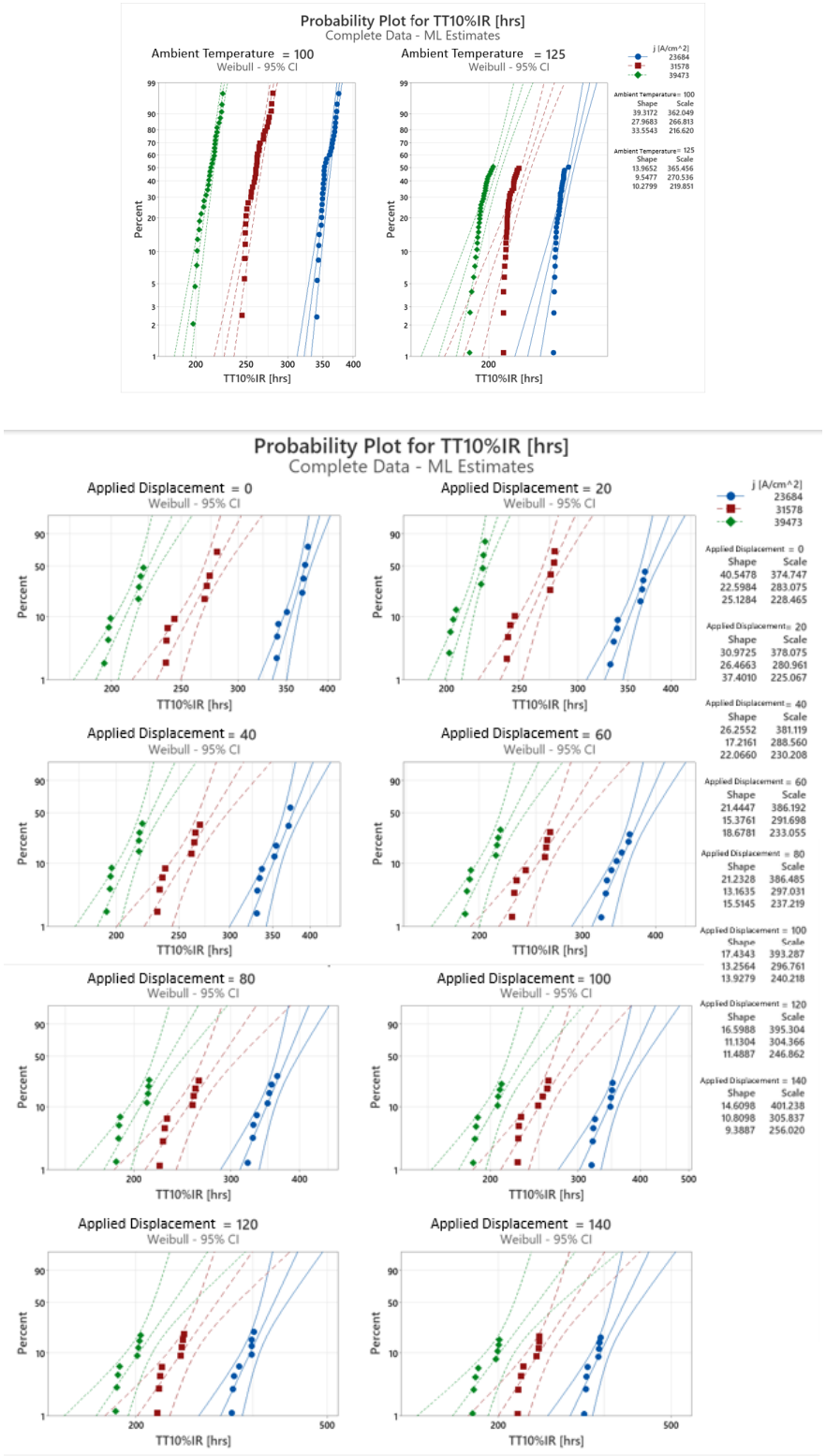


Figure 26: Weibull plots for current density and temperature interaction (top) and current density and applied displacement (bottom).

3. SOLAR INVERTER CASE STUDY

In this chapter, 30 and 50 [kW] grid-tied solar inverter designs developed by a team at the Korea Electrotechnology Research Institute (who funded a portion of this work) are evaluated based on the results achieved in Chapter 2. This analysis also resulted in the development of a rapid design analysis tool which can estimate the lifetime of a solar inverter based on anticipated combined electromigration and mechanical stressing use conditions without the need for computer-aided 3D modeling techniques. While the details related to the development of that tool will not be discussed in this body of work, the existence of the tool has been made known in the case that the reader would like to learn about the tool's functionality. Please contact the author or University of Arkansas graduate school for further information regarding this tool if desired.

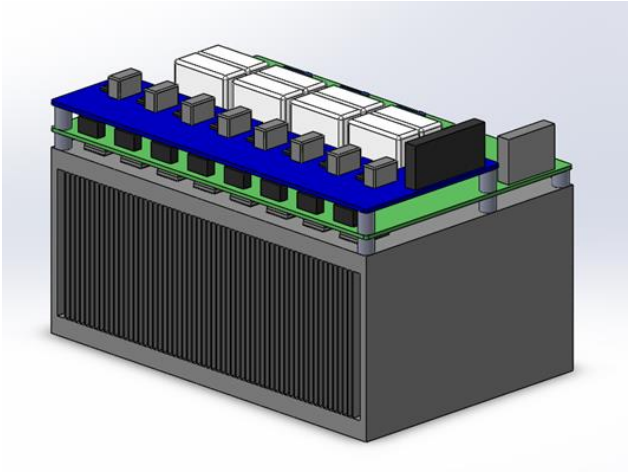


Figure 27: 30 [kW] grid-tied solar inverter CAD model.

3.1. Case Study

The case study of these inverter systems consisted of several parts which are summarized in Figure 28. By analyzing the systems in this fashion, elucidation of the lifetimes of the systems was accomplished.

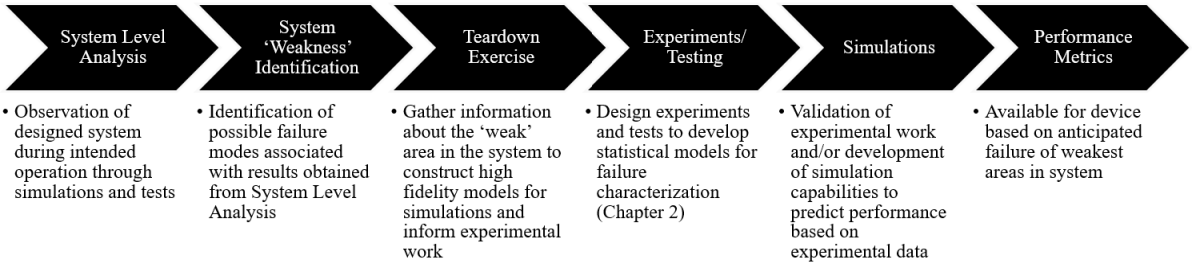


Figure 28: Flow diagram explaining solar inverter case study completion steps.

3.1.1. System Level Analysis & Weakness Identification

To analyze the solar inverter systems, detailed 3D modeling of their physical architecture was done. Thermal-electric simulations were then performed to evaluate their thermal performance under the maximum loading conditions that they would experience in their intended environments.

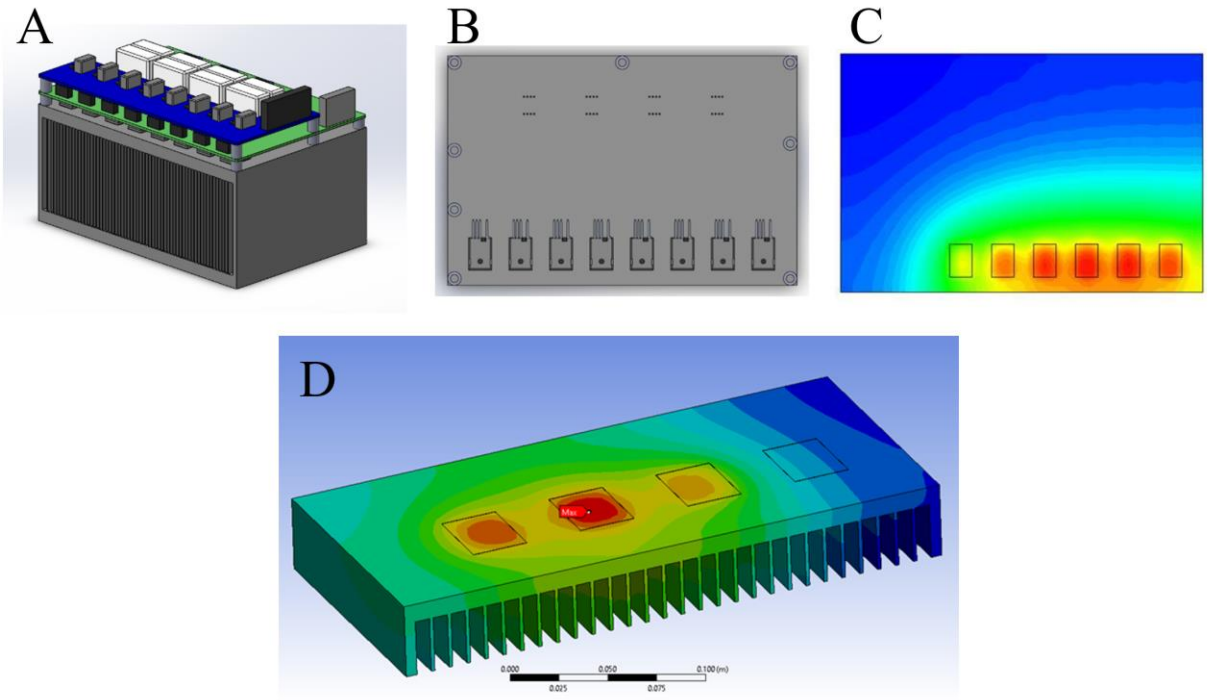


Figure 29: Images from CAD modeling and ANSYS simulations for determining hot spot locations in the inverter systems. A: CAD model of 30 [kW] system; B: Top view of MOSFETs in 30 [kW] system; C: Thermal profile for 30 [kW] system; D: Thermal profile for 50 [kW] system.

In these maximum loading scenarios, the switching components for inversion of power from DC to AC were identified as the critical components within the systems. These components

in the 30 [kW] inverter were CREE C3M00161120K MOSFETs. In the 50 [kW] system, Infineon FF08MR12W1MA1_B11A modules were used. In both cases, the chips utilized were made of Silicon Carbide (SiC) and connected using aluminum wire bonds. This analysis also indicated that thermal coupling would occur between the switching components, meaning that there was in fact a thermal gradient from component to component in the system. The following table summarizes the thermal results for the highest temperature components from this system level analysis.

Table 6: System level analysis thermal results for the 30 and 50 [kW] inverter systems.

Inverter Design [kW]	Maximum Junction Temperature [C]
30	88
50	94

The system level analysis thus indicated the need for a thorough examination of the switching components, as they were found to be operating under the highest thermal and electrical stresses in the systems.

3.1.2. Teardown Exercise

In the teardown analysis, the switching components and modules from the 30 and 50 [kW] systems were purchased and analyzed to facilitate high-fidelity modeling of the components themselves. These modeling activities were then used to extract temperature, current density, and mechanical stress states at the interconnect levels of the devices, enabling the use of the models developed in Chapter 2 for estimation of lifetime of the components and therefore the systems themselves.

In the case of the CREE MOSFETs, various iterations of sectioning, polishing, and grinding were used to remove the epoxy molding compound (EMC) housing from the component to reverse engineer a model of the device. In the case of the Infineon modules, the deconstruction

process was significantly more straightforward, as there was no EMC layering to remove in order to access the chip and wire bond locations.

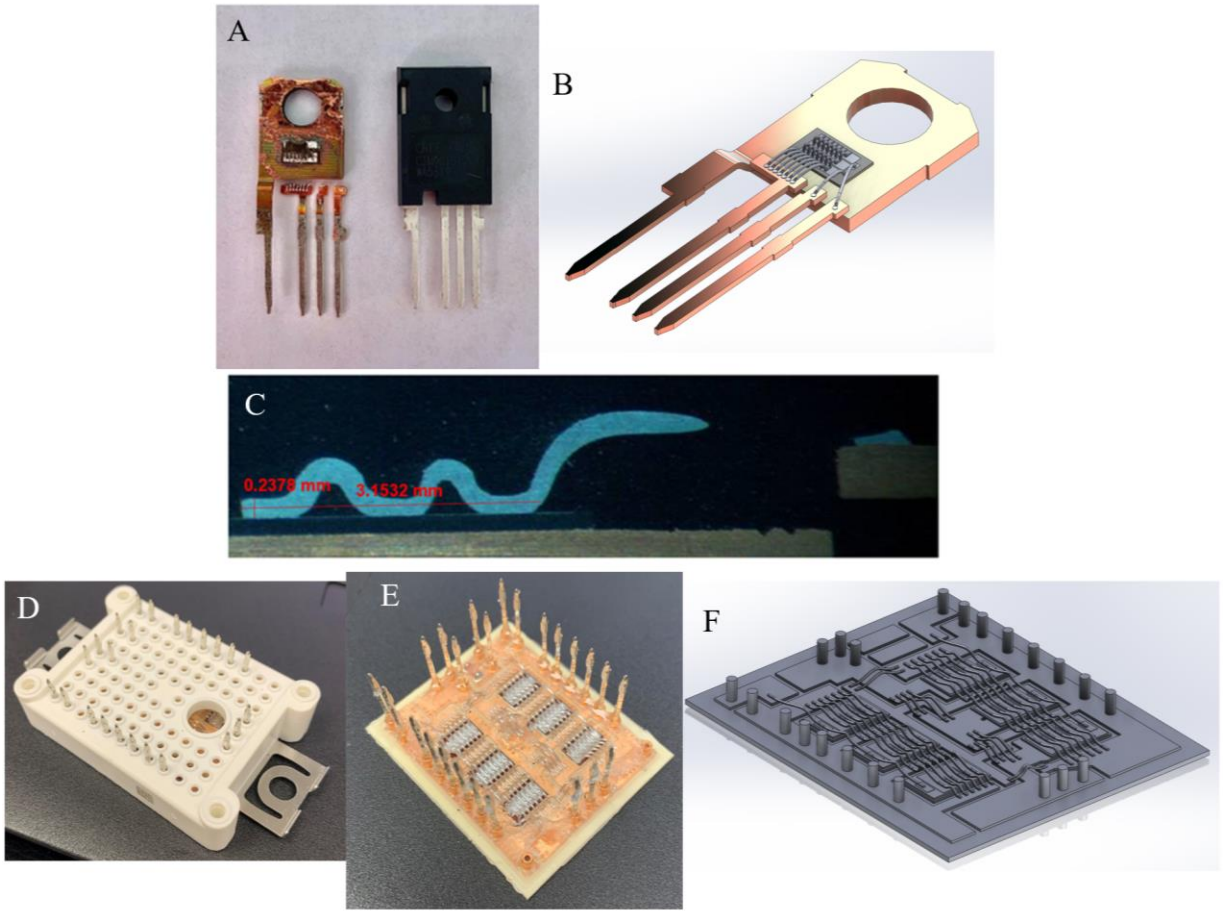
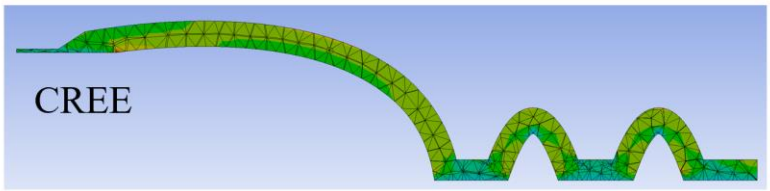


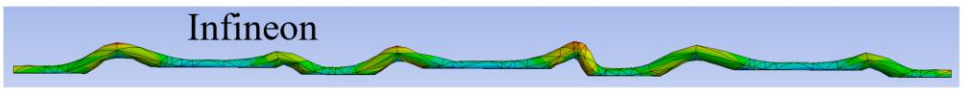
Figure 30: Images from teardown analyses for switching devices used in the 30 and 50 [kW] inverter designs. A: CREE MOSFET with and without EMC casing; B: CREE MOSFET CAD model; C: CREE MOSFET wire bonding cross-section; D & E: Infineon module with and without housing; F: Infineon module CAD model.

By analyzing the geometries of the CREE and Infineon modules, SOLIDWORKS models were created and ANSYS simulations were performed to extract more detailed thermal and mechanical stress information with respect to the wire bonds within each respective component. These analyses were again performed under maximum power load conditions.

Table 7: Summary of 30 and 50 [kW] switching components and respective wire bond analyses.

Inverter Design [kW]	30	50
Component	CREE	Infineon
Maximum Junction Temperature [C]	88	94
Maximum Wire Bond Temperature [C]	92	97
Maximum Wire Bond Current Density [A/cm^2]	7518	8276
Maximum Normal Compressive Stress [MPa]	-43.18	-93.06





3.1.3. Performance Metrics

The experiments and analysis performed in chapter two enabled the development of a lifetime model which incorporates the influences of EM and mechanical loading scenarios into one stress-modified lifetime model for aluminum wire bonds based on Black's equation. Because the analysis of the 30 and 50 [kW] inverters indicated that there was potential for wire bond failures under such conditions, the previously described model has been used to evaluate the lifetime of the inverter systems by using the parameters extracted from evaluation in section 3.1.2.

Solar inverters experience unique mission profiles during their lifetime, and therefore can be challenging to represent in terms of lifetime estimation. Factors such as cloud cover or even the collection of dust over time will impact the performance of solar cells, thereby impacting the mission profile of the solar inverters that they are attached to. Even for a perfect scenario where

solar cells always remain clean and there is not a cloud in the sky, diurnal cycles vary daily as our planet progresses through its annual trip around the sun. Fortunately, each of these factors will reduce the time spent at maximum operating capabilities for the solar inverter system. In a grid-tied scenario, the power loading scenario becomes even more complicated as the grid demands change on a daily, or even hourly basis.

If it is assumed that the most strenuous energy generation cycles are only endured for a few days or weeks annually during the portions of the year when the days are longest and other external conditions such as weather remain unchanged, it can be said that an inverter system will only spend short periods of time managing power loads at its maximum capabilities. If this assumption is used, lifetime estimates should be made based on the assumption that a solar inverter will endure those most strenuous conditions repeatedly until it reaches the failure criteria. Using this assumption, it can be said with certainty that the system will likely outlast those estimations. By anticipating early failure times in this way, it can almost be guaranteed that system inefficiencies and maintenance downtime can be predicted and managed with minimal time spent under maintenance, meaning that system down time can be minimized. In this body of work, this is the assumption that is being used to evaluate the lifetime of the devices. To summarize, it is thus being assumed that the 30 and 50 [kW] systems are expected to manage a diurnal cycle which, at their peak of operation, handle 30 and 50 [kW], respectively. This cycle is then repeated until the failure criteria of a 10% increase in electrical resistance at the wire bonds is met.

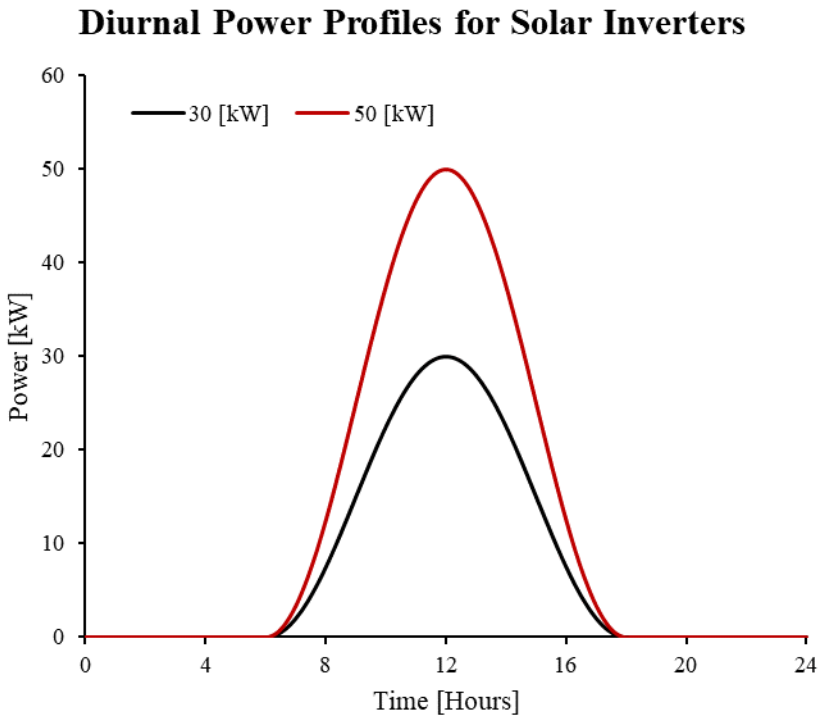


Figure 31: Diurnal power cycle profiles for 30 and 50 [kW] systems for "most strenuous" operating scenarios.

Because the models developed in Chapter 2 are not damage cumulative, further assumptions must be made to create an estimated lifetime based on the diurnal profiles. To make this simplification, the average values across the diurnal profiles have been taken to create a constant loading state which represents the time spent at the diurnal conditions. Using these averaged constant loading conditions, estimates for lifetime have been made.

To demonstrate the need for multi-stress model utilization in power electronics reliability, both Black's equation parameters and the stress-modified model developed in Chapter 2 have been used to independently estimate the time to failure in the solar inverter systems. This allows for the comparison of single and multi-stress analysis techniques and demonstrates that single stress models are insufficient for estimating time to failure.

Table 8: Comparison table for diurnal average stress estimations and lifetime estimation methods for the 30 and 50 [kW] inverter components.

Inverter Design [kW]	Component	Diurnal Cycle Avg. Wire Temperature [C]	Diurnal Cycle Avg. Current Density [A/cm^2]	Diurnal Cycle Avg. Normal Compressive Stress [MPa]	Black's Equation TT10%IR Estimation [Days]	Stress-modified Model TT10%IR Estimation [Days]	% Difference Between Model Results	Acceleration Factor (Use condition vs. Arrhenius Model)
30	CREE	56	4787	-26.28	562.00	557.66	0.8%	44.6
50	Infineon	60	5270	-57.56	454.13	444.37	2.2%	35.6

Table 8 summarizes the results obtained for lifetime analysis of the critical components in the 30 and 50 [kW] inverter systems. In both systems, accounting for mechanical stress reduced the estimated lifetime of the devices by five and ten days, respectively. These results thus demonstrate the potential for early-lifetime failures which could result in undesirable system downtime if unaccounted for. Therefore, the multi-stress model evaluation from Chapter 2 shows that the designed inverter systems should consider finding ways to reduce the impacts of thermo-mechanical stressing in future design iterations by implementing new cooling systems or optimizing switching component layouts to reduce co-heating effects between individual devices and lower the average junction temperatures so as to increase the expected lifetime of the devices. An example of this type of design change is depicted in Figure 32, where junction temperatures were reduced by 10 [C] on average between MOSFETs in the 30 [kW] system by alternating the spacing between the devices.

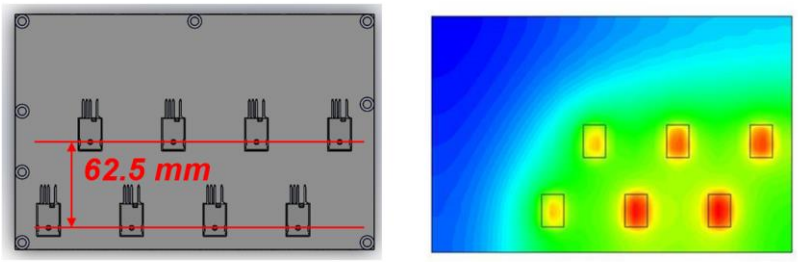


Figure 32: Demonstration of changing MOSFET positions in the 30 [kW] system to reduce the maximum junction temperatures and effects of co-heating between devices.

4. CONCLUSION

4.1. Summary of Results

In this thesis, a discussion of power electronics and their impact on the future is discussed. The critical aspects of robust and efficient power electronic systems are acknowledged, and their common failure mechanisms are described. Interconnect components at high stress locations in systems are identified as system weaknesses. Of the multitude of interconnect options, wire bonds are introduced and explored as an interconnect type which could be susceptible to failures in next-generation power electronic designs. With respect to wire bond utilization in future power electronic designs, the effects of electromigration (EM), thermomigration (TM), and thermomechanical stresses are explored and identified as a handful of key failure mechanisms which, if not accounted for appropriately, could cause significant reliability problems. Subsequently, the combined effects of those three failure mechanisms are experimentally explored as this interaction of failure mechanisms has not been well accounted for during the survey of existing literature. Based on the presented results, a model for the combined effects was developed and compared to Black's equation for EM and comparisons were drawn, demonstrating that combined stressing in wired interconnects will reduce the expected lifetime of the bond when a single failure mode model is used. Finally, the proposed multi-stress model is utilized to analyze a pair of grid-tied solar inverter designs as a case study and is compared to the same analysis using Black's equation. As expected, the multi-stress model indicated that the expected lifetimes of the inverter systems was shorter than the estimates made using Black's equation, further illustrating the impacts that multi-stress reliability models will have on improving lifetime analysis techniques in future power electronic systems.

4.2. Conclusions and Future Outlooks

The results of this work demonstrate the need for future power electronic interconnect reliability models to incorporate multi-stress analysis capabilities into design iterations to yield systems with increased robustness. Specifically, the combination of EM and mechanical stressing have been identified as a combinatorial pair which will influence lifetime estimations in power electronic device wire bonds now and in the future.

In the future, more studies directed at understanding the interaction between all types of externally applied mechanical stresses will prove to be advantageous, as wire bonds come in a variety of shapes and sizes and can be fabricated in multiple different ways. A single relationship for one wire scenario has been shown in this thesis, but it will not be able to account for these variabilities. Not only will other studies need to be completed in order to understand the interaction of EM and mechanical stresses, but studies related to the development and discovery of mitigation techniques for single and multi-stress cases will also prove to be useful. Some of these studies have been conducted already, but there is much potential for further work in this area. For example, it has been shown that alloying gallium with aluminum and copper can improve their performance against EM, but does alloying improve the resilience of an aluminum wire bond subjected to multiple stresses [1]? Another demonstrated mitigation technique involves electroless plating of copper with cobalt as a seeding layer, which improved EM performance [2]. Other studies have looked to use doping techniques to improve wire bond performance under EM conditions with good results [3]. Will doping and electroless plating have an improved effect under multiple stresses? Some studies have shown stabilization, strengthening, and improved electrical conductivities of aluminum conductors can be accomplished using spray coating or rotary swaging

techniques, but it has yet to be seen if these effects impact performance under multiple stresses [4], [5].

4.3. References

[1] S. Ravandi et al., "Gallium-Enhanced Aluminum and Copper Electromigration Performance for Flexible Electronics," ACS Applied Materials & Interfaces, vol. 13, no. 5, pp. 6960–6974, Feb. 2021, doi: 10.1021/acsami.0c22211.

[2] J. Tao, N. W. Cheung, and C. Hu, "Electromigration characteristics of copper interconnects," IEEE Electron Device Letters, vol. 14, no. 5, pp. 249–251, 1993, doi: 10.1109/55.215183.

[3] T.-H. Chuang, H.-J. Lin, H.-C. Wang, C.-H. Chuang, and C.-H. Tsai, "Mechanism of Electromigration in Ag-Alloy Bonding Wires with Different Pd and Au Content," Journal of Electronic Materials, vol. 44, no. 2, pp. 623–629, 2015, doi: 10.1007/s11664-014-3558-7.

[4] L. Celko, L. Klakurková, and J. vejcar, "Diffusion in Al-Ni and Al-NiCr Interfaces at Moderate Temperatures," Defect and Diffusion Forum, vol. 297–301, pp. 771–777, 2010.

[5] Y. Yang, J. Nie, Q. Mao, and Y. Zhao, "Improving the combination of electrical conductivity and tensile strength of Al 1070 by rotary swaging deformation," Results in Physics, vol. 13, p. 102236, 2019, doi: https://doi.org/10.1016/j.rinp.2019.102236.

5. APPENDIX

The following sections provide supplementary information for various portions of the first four chapters of this document related to executing various experimental, mathematical, and simulation procedures.

5.1. Appendix A: Combined EM and Stress Experiment Procedures

The following steps explain how fabricate samples and record time to 10% increase in resistance data for the aluminum wire bonds used in the study presented in Chapter 2.

1. Obtain DBC coupons with proper pad sizes and locations. For this study, the cards were ordered from a company named REMTEC.
2. Cut the DBC sheet into individual sample cards using a sectioning saw and clean with acetone to remove coolant fluid and particles. For this study, the sectioning saw in the Analytical Lab of the High Density Electronics Center at the University of Arkansas Engineering Research Center was used.
3. Attach bent steel wire nails to DBC bond pads using SAC305 solder paste and the manufacturer recommended reflow profile to create probing connection and power connection points.
4. Clean the sample cards in a sonic bath with acetone for two minutes.
5. Wire bond the DBC pad locations together to create a series network of four wire bonds for each sample coupon. For “EM only” samples, wire bonding can be done immediately after the cleaning process. For “Combined stressing” coupons, configure the novel fixturing mechanism for the bonding process by separating the fixturing mechanisms from the assembly and connect them using the sliding rails. After configuration, fix the sample cards to the mechanism and proceed to bond. For this study, the Orthodyne manual bonder

in the Assembly Lab of the High Density Electronics Center at the University of Arkansas Engineering Research Center was used.

6. Fix the samples to the oven rack. For “EM only” samples, fix them to the rack using high temperature tape. For “Combined stressing” samples, fix the mechanism to the adjustment stage and displace the desired amount. After applying displacement, fix the displacement using the sliding rails.
7. Place the samples inside of the oven and connect the power supply wires and voltage monitoring wires to the appropriate probe points on the samples.
8. Turn on the oven and set to the desired temperature.
9. Once the oven is at temperature, open the WinDAQ software application and configure the data acquisition module as desired with the appropriate channel settings and sample rate.
10. Begin recording the voltage values in the software, naming the file appropriately.
11. Set the power supply to constant current mode by keying in the desired constant current value and overshooting the applied voltage required for the resistance of the samples and supply lines.
12. Turn on power supply channel, allowing for the flow of constant electrical current.
13. Stop the experiment once the voltage reading indicate a 10% increase in resistance.

5.2. Appendix B: Al Wire Bond TCR Experiment Procedures

In this section, the procedures for determining the temperature coefficient of resistance for the wire bonds studied in Chapter 2 are outlined.

1. Create a single wire bond sample using the same process from Appendix A up to step 5.

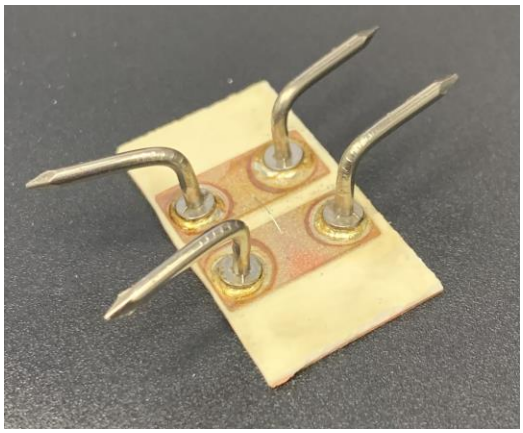


Figure 33: TCR wire bond experimental coupon.

2. Measure and record the resistance of the bond using a GW Instek LCR-6002 at room temperature, 75, 100, and 125 [C].
3. Connect the sample to a low-noise power supply and DATAQ voltage measurement module inside of a Cascade TEK oven. At current values of 1, 3, 4, and 5 Amps, measure and record the resistance at the same temperature conditions used in step 2. Wait 4 minutes for each condition to reach steady state before recording.
4. Use excel to create a linear trendline for the LCR measurements.
5. Extrapolate the trendline from step 4 outwards and apply a shift in temperature to the conditions from step 3 to match the measurements to the trendline.

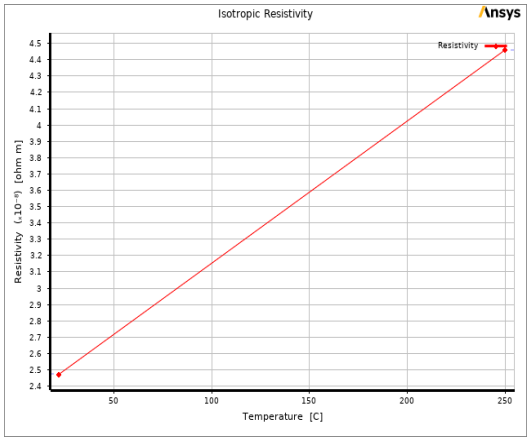
5.3. Appendix C: Al Wire Bond Mechanical Stress Analyses in ANSYS

The following steps detail the simulation procedures used to extract the relevant stress values associated with wire bond failure criteria in Chapter 2.

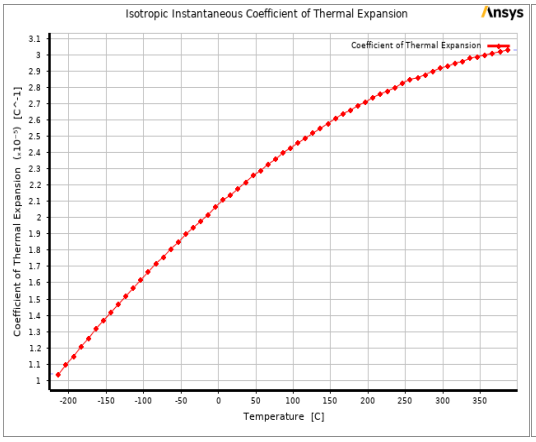
Steps for Simulation:

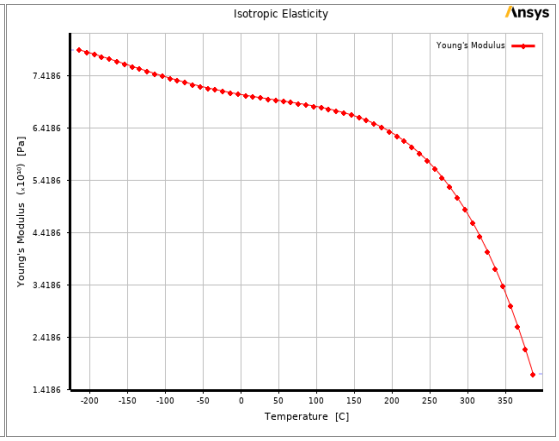
1. In ANSYS, create a custom material for the Aluminum wire bond based on TCR experiments and literature.

From TCR Experiments:



From Literature (ref [36], [37] in Ch. 1):





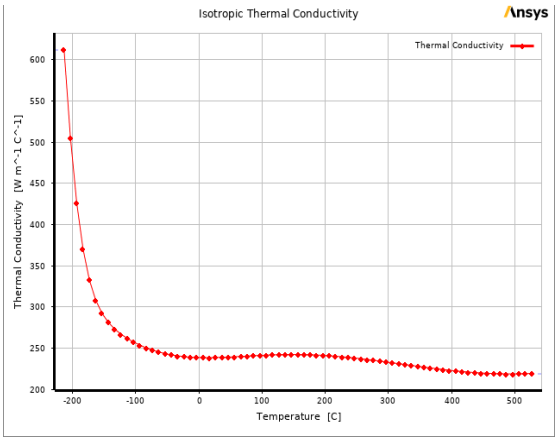


Figure 34: Experimental and literature-based material properties plots for ANSYS simulations.

2. 3D model a wedge-wedge wire bond in SOLIDWORKS, saving the file in .igs format.
3. Create an ANSYS project for thermal-electric analysis and transient structural analysis.

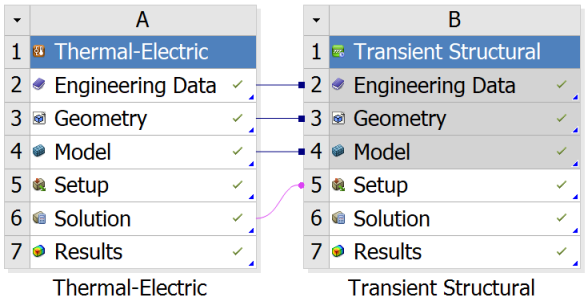


Figure 35: ANSYS project layout for thermal-electric and transient structural analysis.

4. Import the wedge-wedge wire bond .igs file into the thermal-electric analysis.
5. Update the model to generate a computer-controlled model mesh.
6. Edit the model and create a material assignment for the geometry from the custom material created in step 1.
7. Set the following initial and boundary conditions as well as the solution profiles in the thermal-electric and transient structural analyses.

Condition		Location on Model	Value
Thermal-Electric	Constant Temperature	Bottom surface of DBC pads	100 & 125 [C]
	Convection	All external faces (excluding bottom surface of DBC pads)	25 [W/m²K]
	Voltage	Bottom surface of DBC pad connected to First Bond location	0 [V]
	Current	Bottom surface of DBC pad connected to Second Bond location	3, 4, & 5 [A]
Transient Structural	Fixed Support	Bottom surface of DBC pad connected to First Bond location	NA
	Frictionless Support	Bottom surface of DBC pad connected to Second Bond location	NA
	X-direction Displacement	At heel of Second Bond location in x-direction	0-140 [µm]

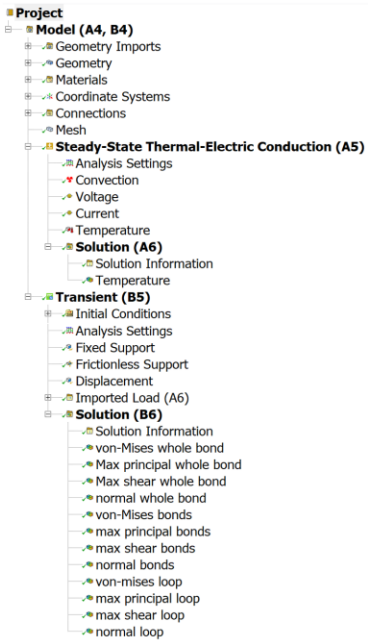


Figure 36: Assumptions and project flow for ANSYS thermal-electric and transient structural analysis.

8. Solve the simulation for each ambient temperature and current density condition to obtain temperature profiles and corresponding stress results. Record these values in excel by copying and pasting them from the tabulated results window.