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Reliability Enhancing Control Algorithms for Two-Stage Grid-Tied Inverters

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Reliability Enhancing Control Algorithms for Two-Stage Grid-Tied Inverters

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by

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ABSTRACT

In the photovoltaic (PV) generation system, two types of grid-tied inverter systems are usually deployed: the single-stage grid-tied inverter system and the two-stage grid-tied inverter system. In the single-stage grid-tied inverter system, the input of the inverter is directly connected to the PV arrays, while an additional dc-dc stage is inserted between the PV arrays and the dc-ac inverter in the two-stage design. The additional dc-dc stage could provide a stable dc-link voltage to the inverter, which also enables new design possibilities, including the multi-MPPT operation and solar-plus-storage application. Thus, the two-stage grid-tied inverter has been widely used in the PV generation system.

As the core component of the PV generation system, the reliability of the grid-tied inverter determines the overall robustness of the system. The two-stage grid-tied inverter system includes three parts: the dc-dc stage, dc-link capacitor, and dc-ac inverter. Thus, the reliability of the two-stage grid-tied inverter relies on the reliability of each part. The dc-dc stage is used to provide a stable dc-link voltage to the inverter. However, when the inverter stage provides constant power to the grid, the load of the dc-dc stage becomes the constant power load (CPL), which will deteriorate the stability of the dc-dc stage. The dc-link capacitor is used to attenuate the voltage ripple on the dc-link and balance the transient power mismatch between the dc-dc stage and the dc-ac stage. However, during the operation of the inverter system, the degradation of the capacitor will reduce the converter reliability, and even result in system failure. The inverter stage is connected to the grid through the output filter, and the LCL type filter has been commonly used due to its superior performance. The resonance of the LCL filter must be properly damped to enhance the inverter stability. However, the grid-side impedance will lead to the resonant frequency drifting of the LCL filter, which will worsen the stability margin of the inverter. Thus,

the control design of the two-stage grid-tied inverter system must consider those reliability challenges.

In this work, three control algorithms are proposed to solve the reliability challenges. For the dc-dc stage, an uncertainty and disturbance estimator (UDE) based robust voltage control scheme is proposed. The proposed voltage control scheme can actively estimate and compensate for the disturbance of the dc-dc stage. Both the disturbance rejection performance and the stability margin of the dc-dc stage, especially under the CPL, could be enhanced. For the dc-link capacitor, a high-frequency (HF) signal injection based capacitance estimation scheme is proposed. The proposed estimation scheme can monitor the actual dc-link capacitance in real-time. For the inverter stage, an adaptive extremum seeking control (AESC) based LCL filter resonant frequency estimation scheme is proposed. The AESC-based estimation scheme can estimate the resonant frequency of the LCL filter online. All the proposed reliability enhancing control algorithms could enhance the reliability of the two-stage grid-tied inverter system. Detailed theoretical analysis, simulation studies, and comprehensive experimental studies have been performed to validate the effectiveness.

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- University of Arkansas, USA

DEDICATION

This dissertation is dedicated to

my mother Dehui Yu, my father Gang Wu, and my sister Xiaojian Wu.

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[1] Y. Wu, M. H. Mahmud, Y. Zhao and H. A. Mantooth, "Uncertainty and Disturbance Estimator-Based Robust Tracking Control for Dual-Active- Bridge Converters," in IEEE Transactions on Transportation Electrification, vol. 6, no. 4, pp. 1791-1800, Dec. 2020. [Published, Chapter 2 consists of this paper].

[2] Y. Wu, M. H. Mahmud, R. S. Krishna Moorthy, M. Chinthavali and Y. Zhao, "Adaptive Extremum Seeking Control Based LCL Filter Resonant Frequency Online Estimation," in IEEE Transactions on Power Electronics, vol. 37, no. 1, pp. 59-64, Jan. 2022. [Published, Chapter 4 consists of this paper].

CHAPTER 1

INTRODUCTION

1.1 Background

The recent development in power electronic semiconductors enables the wide deployment of solar energy conversion systems. On one hand, the development of photovoltaic (PV) cells has notably reduced the cost of solar energy. In 2020, the cost of PV panels has reduced by about 85% compared with that in 2010, from $2.51/W to $0.38/W [1]. The cost reduction of PV panels has transferred solar energy from an expensive generation system to affordable clean energy. Table 1-1 summarizes some low-cost electricity goals of the U.S. Department of Energy (DOE) Solar Energy Technologies Office (SETO) for 2025 with a notable reduction in the levelized cost of energy (LCOE) of solar energy is expected. On the other hand, as the key component in the solar energy system that achieves the power conversion from PV modules to the grid, the design of the grid-tied inverter also benefits from the advancement of the wide bandgap (WBG) semiconductors, including silicon carbide (SiC) and gallium nitride (GaN) devices. The low switching loss of WBG devices allows for higher switching frequency, and thus, the power density of the converter can be improved. Meanwhile, compared to their silicon counterparts, the WBG devices can operate at higher temperature, which enhances the overall reliability of the inverter system [2].

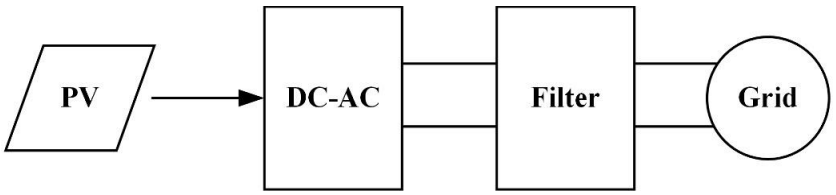
TABLE 1-1 U.S. DOE SETO 2025 Goals of Low-Cost Electricity [1]

Systems	LCOE Goal
Utility-scale PV system	$0.03/kWh
Commercial PV system	$0.08/kWh
Residential PV system	$0.10/kWh

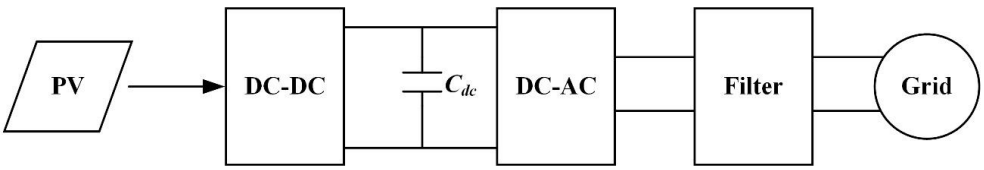
Utility-scale PV plus energy storage system	$1.36/$W_{DC}$

In grid-tied solar energy systems, single- and two-stage grid-tied inverters are the commonly used. Figure 1-1 (a) and (b) are the system-level architecture of the single-stage and two-stage grid-tied inverter systems, respectively. In the single-stage grid-tied inverter system, the PV modules are directly connected to the grid-tied inverter to achieve the dc-ac power conversion, where an output filter is inserted between the dc-ac stage and the grid to attenuate the switching ripples and harmonics. The two-stage grid-tied inverter system, however, contains an additional dc-dc stage. The dc-dc stage in the two-stage grid-tied inverter system provides a stiff dc-link voltage to the dc-ac stage, while the dc-link capacitor C_{dc} is used as the energy buffer to attenuate the voltage ripples and balance the transient power unbalance between the two stages. In order to maximize the output power of the PV module, both topologies are able to work in the maximum power point tracking (MPPT) mode [3]-[6]. Compared with the two-stage design, the single-stage grid-tied inverter system is simpler in the hardware design due to the elimination of the additional dc-dc stage. However, considering the intermittent nature of the solar energy and the MPPT operation, the input voltage of the single-stage grid-tied inverter system is not stable, and the control algorithm must be able to compensate for the uncertainties. Although the hardware cost of the two-stage design is higher, the input voltage of the dc-ac stage is stable due to the additional dc-dc stage. Thus, the control complexity of the dc-ac stage is much simpler in the two-stage design than that in the single-stage grid-tied inverter system. Besides, the single-stage grid-tied inverter cannot ensure the MPPT operation for each PV module if multiple PV modules are connected in series [3]. Those disadvantages of the single-stage grid-tied inverter could limit its application in the solar energy system. Nevertheless, the two-stage design can provide more degree-of-freedom

in the MPPT operation. By adopting a proper dc-dc topology, the two-stage grid-tied inverter system can support multi-MPPT operation, i.e., more energy can be harvested from PV modules. Moreover, the two-stage design also enables the solar-plus-storage applications [1], [2]. By adopting a bi-directional dc-dc converter in the two-stage grid-tied inverter system, a battery energy storage system (BESS) could be integrated with the PV modules and improve the system robustness and reliability. In 2019, about 2% of all PV utility-scale PV systems were integrated with BESS, and more than 30% of new utility-scale PV systems that are proposed in 2022 and 2023 will be paired with energy storage [1]. Thus, the two-stage grid-tied inverter system has been widely adopted in the PV system due to its advantages.



(a)



(b)

Figure 1-1. Different types of grid-tied inverter systems: (a) single-stage and (b) two-stage.

1.2 The state-of-the-art of two-stage grid-tied inverters

Besides the fact that the two-stage grid-tied inverter has been widely adopted in the PV generation system, there are also a large amount of research effort on the two-stage grid-tied inverter from both academia and industry to further enhance the performance of inverter systems.

Since the additional dc-dc stage in the two-stage grid-tied inverter system can provide a stable dc-link voltage to the dc-ac stage, the selection of the dc-link voltage enhances the degree-of-freedom of the controller design. In [7]-[9], the adaptive dc-link voltage strategy has been discussed. The dc-link voltage, i.e., the output voltage of the dc-dc stage, can be actively adjusted based on the required inverter output voltage, and thus, the switching loss in all power switches can be notably reduced. Feedforward control has been integrated with the adaptive dc-link voltage controller to enhance the dynamic response of the grid-tied inverter system. It should be noticed that although the additional dc-dc stage with a properly designed voltage controller can provide a stable dc-link voltage to the inverter, the high-frequency voltage ripples caused by the dc-ac stage still exist. Especially, when the grid-tied inverter is connected to the single-phase grid, voltage ripple on the dc-link with the double-line frequency will result in a series of odd order harmonics on the inverter output current, and thus, the output power quality will be distorted. In [10], a closed-form solution is proposed to calculate the amplitude of the ripple-caused harmonics. With the closed-form harmonics analysis, the selection of the dc-link capacitance can be guided by the required output power quality. Moreover, the impact of the dc-link capacitance on the dc-link voltage control stability has been analyzed in [11], where a small-signal model of the dc-link voltage control loop has been proposed, and a right-half-plane (RHP) has been observed if the inverter is operating at voltages lower than the maximum power point. With the proposed small-signal model, a minimum requirement of the dc-link capacitance can be provided to ensure the

stability of the PV generation system. In [4]-[6], the design method of the MPPT strategy of two-stage grid-tied inverter systems has been discussed. The low-voltage-ride-through (LVRT) problem of the two-stage grid-tied inverter has been discussed in [12], [13], and several control approaches have been proposed to increase the LVRT capability of the PV system.

Besides the research effort on the control of two-stage grid-tied inverter systems, various circuit topologies also have been discussed in the past decades. In [14], a three-level-stacked neutral point clamped (3L-SNPC) topology is proposed for the two-stage grid-tied inverter system. The proposed 3L-SNPC topology, as well as a new pulse-width-modulation (PWM) strategy, can enhance the converter efficiency, especially in the low-power region. The power loss of the two-stage inverter system has been analyzed, and a comparison of the single-stage and two-stage designs has been provided in [15]. In [16], a high step-up boost-integrated flyback converter is used as the dc-dc stage. The proposed dc-dc stage can work in the soft-switching condition, and thus, the switching loss can be notably reduced. Detailed analysis and comparison between different dc-dc topologies for the two-stage inverter system have been provided in [17], and a novel semi-isolated multi-input dc-dc topology has been proposed for the two-stage inverter system. All of those research efforts have enhanced the stability, efficiency, and output power quality of the two-stage grid-tied inverter system.

1.3 Challenges and problem definitions

As mentioned earlier, various research effort on the control and topology of the two-stage grid-tied inverter system have enhanced the stability, efficiency, and power quality of the PV system. However, challenges still remain in the reliability improvement of the two-stage grid-tied inverter system. It can be seen from Figure 1-1 that there are three major parts in the two-stage grid-tied

inverter system, i.e., the dc-dc stage, the dc-link capacitor, and the grid-tied dc-ac inverter. In this dissertation, three novel control algorithms are presented to enhance the reliability of the dc-dc stage, dc-link capacitor, and the grid-tied inverter stage, respectively. The two-stage grid-tied inverter investigated in this work contains a single-phase dual-active-bridge (DAB) dc-dc converter and a single-phase grid-tied inverter, and Figure 1-2 shows the schematic of the inverter system. The DAB converter is a bi-directional dc-dc converter with soft-switching capability. Due to the bi-directional power transmission capability, the DAB converter could be used in not only the conventional solar generation system but the solar-plus-storage applications. Besides, a standard H-bridge design could be adopted in the proposed two-stage grid-tied converter system to further enhance the modularity and flexibility.

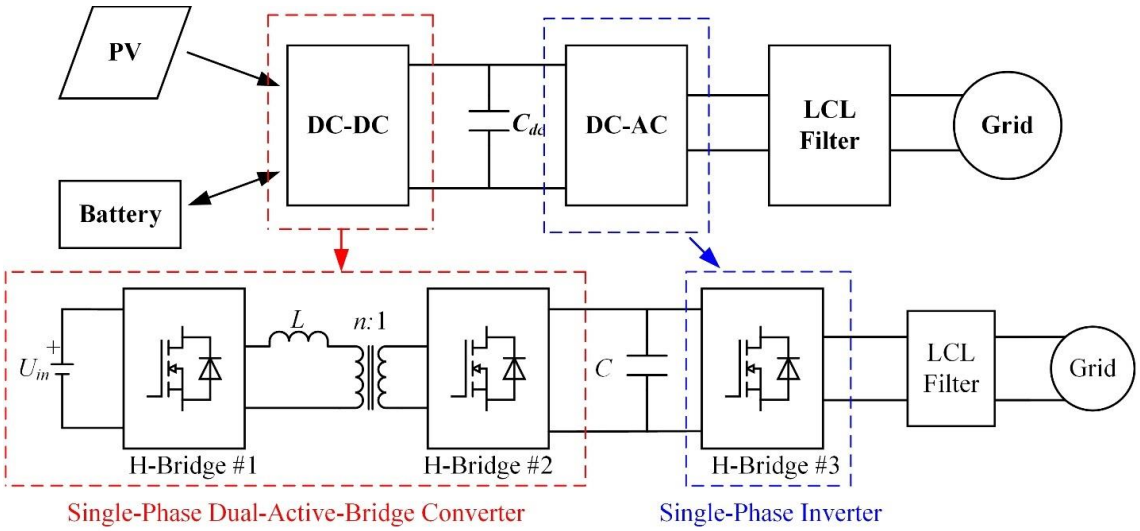


Figure 1-2. Schematic of the proposed two-stage grid-tied inverter system.

When the dc-ac stage provides constant power to the grid, the inverter stage will be a constant power load (CPL) to the dc-dc stage. However, the small-signal model of the CPL indicates a negative resistance, which deteriorates the stability of the dc-dc stage. As an example, Figure 1-3 shows the unstable dc-link voltage control due to the CPL. Due to the negative resistance

characteristic of the CPL, the voltage controller of the dc-dc stage is unstable. Thus, the design of the dc-dc converter voltage controller must consider the system stability under the CPL. Meanwhile, the voltage controller should also be able to provide a satisfactory command voltage tracking performance. Thus, the first reliability challenge of the two-stage grid-tied inverter is the robust voltage control of the dc-dc stage.

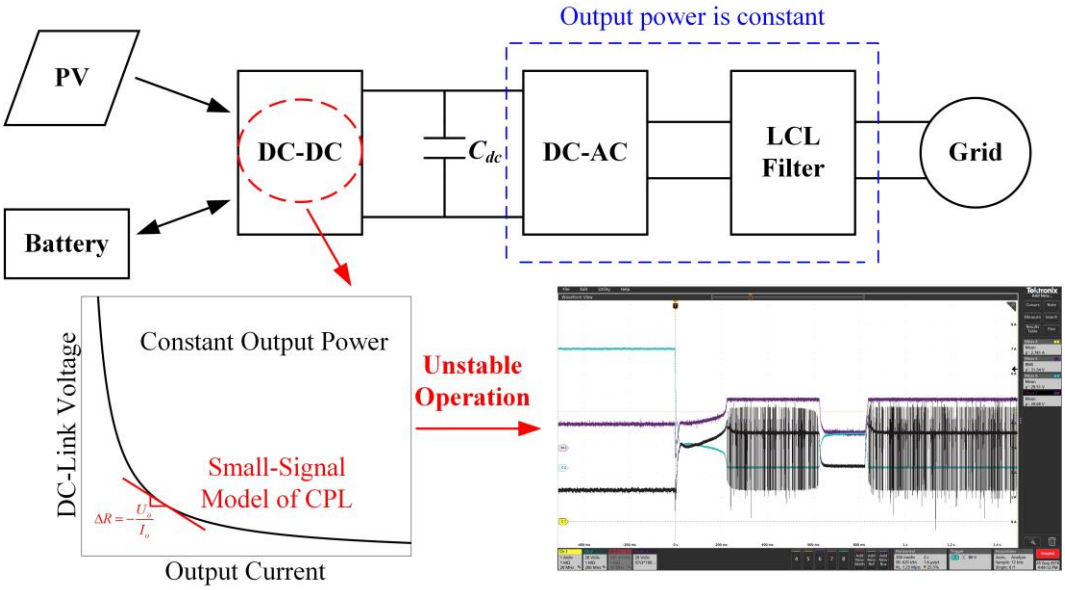


Figure 1-3. Unstable dc-dc converter due to the CPL.

As the energy buffer, the dc-link capacitor connects the dc-dc stage and the dc-ac stage, and it also determines the reliability of the whole converter system. Besides, the dc-link capacitor also impacts the voltage control performance of the dc-dc stage, since it plays a vital role in the small-signal model of the DAB converter [2]. However, during the operation of the grid-tied inverter system, the actual dc-link capacitance may vary from its nominal value due to the component tolerance, thermal stress, and also capacitor degradation. As an example, Figure 1-4 shows the capacitance degradation over the long-term operation of the inverter system. It can be seen that the end-of-life of the dc-link capacitor can be indicated by the actual capacitance. By monitoring the

actual dc-link capacitance, the health status of the dc-link capacitor could be known. Thus, the second need for reliability enhancement of the two-stage grid-tied inverter system is the online monitoring of the actual dc-link capacitance.

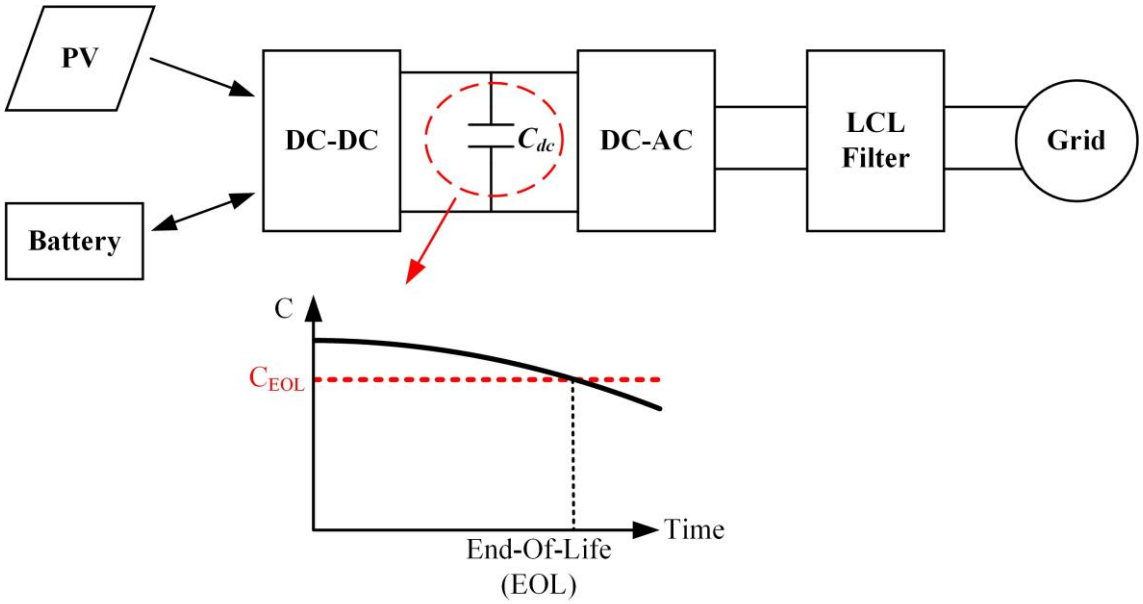


Figure 1-4. DC-link capacitance degradation.

When the dc-ac stage is connected to the grid, an output filter is necessary to attenuate the switching ripples and satisfy the grid code. In practice, the LCL-type filter is commonly adopted in grid-tied inverter applications. Compared with the L-type filter, the LCL filter can provide better switching ripple attenuation performance with reduced filter volume. However, the resonance of the LCL filter could deteriorate the stability of the inverter. Especially, the resonant frequency of the LCL filter is affected by the component tolerance, as well as the grid impedance. The drifting resonant frequency can increase the difficulties in the design of the damping scheme and further reduce the stability margin of the grid-tied inverter. Figure 1-5 shows that the actual resonant frequency of the LCL filter is impacted by the grid-side impedance, and the inverter controller cannot maintain the stability of the inverter system under the resonant frequency drifting. Thus,

the third reliability challenge of the two-stage grid-tied inverter is the online estimation of the actual resonant frequency of the LCL filter.

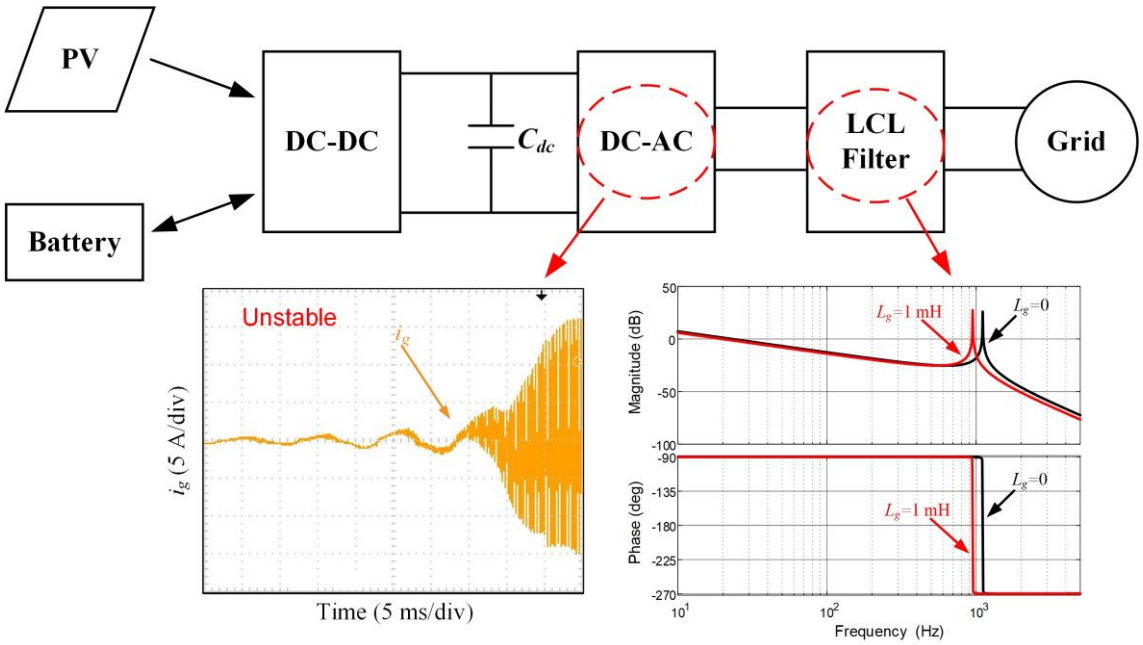


Figure 1-5. Unstable dc-ac stage due to the LCL filter resonant frequency drifting.

In this work, three control schemes to enhance the reliability of the grid-tied inverter system will be presented to solve the challenges that are discussed earlier. First, an uncertainty and disturbance estimator (UDE) based robust voltage control scheme is proposed for the DAB converter to improve the robustness of the dc-dc stage, especially under the CPL. Second, a high-frequency (HF) signal injection based dc-link capacitor estimation scheme is presented to provide the online estimate of the actual dc-link capacitance. Moreover, in order to estimate the actual resonant frequency of the LCL filter, an adaptive extremum seeking control (AESC) based LCL resonant frequency estimation scheme is also presented in this work. Rigorous theoretical analysis, simulations, and comprehensive experimental studies have been performed to validate the

effectiveness of the proposed schemes. With the proposed control strategies, the discussed challenges can be effectively solved and the overall reliability of the two-stage grid-tied inverter system will be notably enhanced.

1.4 Outline

This dissertation is organized as follows:

- Chapter 2 presents a UDE-based robust voltage control algorithm for the DAB converter. A linear output current based DAB model is proposed. Based on the linear DAB converter model, a UDE-based DAB converter voltage control scheme is presented. The proposed scheme can actively estimate and reject the converter uncertainty and disturbance, and thus, the voltage tracking performance and be enhanced. Besides, the CPL of the DAB converter has been analyzed in detail, and the proposed scheme can notably improve the DAB converter robustness and stability when feeding a CPL. Comprehensive experimental studies have been conducted to validate the effectiveness of the proposed voltage control algorithm.
- Chapter 3 describes the HF signal injection based dc-link capacitor estimation scheme. The proposed dc-link capacitor estimation scheme can provide an online estimate of the dc-link capacitor, which can be used for the component health monitoring. The deadtime of the DAB converter has been analyzed in detail, and a deadtime compensation scheme is proposed to further enhance the estimation accuracy. Both hardware-in-the-loop (HIL) and experimental studies have been performed to demonstrate and validate the effectiveness and performance of the proposed scheme.

- Chapter 4 presents an online estimation scheme for the LCL filter resonant frequency. By injecting an HF signal into the filter network, the proposed AESC-based estimation scheme can estimate the actual resonant frequency of the LCL filter, which will be impacted by the component tolerance and grid-side impedance. An adaptive law is proposed to actively adjust the magnitude of the injection signal, which can tradeoff the dynamic response and the steady-state inverter output power quality. The effectiveness of the proposed estimation scheme has been validated through experiments.
- Chapter 5 provides the conclusions and the future research recommendations for the work proposed in this dissertation.

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CHAPTER 2

UDE-BASED ROBUST VOLTAGE CONTROL FOR DAB CONVERTERS

2.1 Introduction

The DAB converter has been widely adopted in many industrial applications, including the DC microgrids, renewable energy systems, on-board chargers for electrical vehicles, more electric aircrafts (MEA) and etc., as it could achieve isolated bi-directional power transmission with soft-switching capability [1]-[7]. However, the system nonlinearities and external disturbances, e.g., the deadtime effect, on-state voltage drop of power devices, and load changes, will lead to tracking error in the DAB output voltage. Moreover, similar to other types of digital controlled converters [8], [9], there is at least one-step computation delay in the digital controlled DAB converter [10]. This time delay will lead to additional phase lag and deteriorate the system stability. Thus, it is still desirable to design a DAB controller to achieve the high-performance voltage tracking, which is robust against the system uncertainties and external disturbances.

Besides those uncertainties and disturbances of the DAB converter itself, the characteristics of the load can also pose significant challenges in the controller design. For example, when a DAB converter is used in a cascaded dc power conversion system, the load of the DAB converter could be other dc-dc or dc-ac converters rather than the passive loads [11]. In this configuration, the load of the DAB converter could be regarded as a constant-power load (CPL) as the second stage converter, when tightly regulated, providing a constant output power to its load regardless the input voltage. The characteristics of the two-stage inverter studied in this work is similar, where the load stage of the dc front-end can be viewed at CPL when the load power is tightly regulated. The small-signal model of the CPL exhibits negative incremental resistance [6], [11]-[16], which

significantly affect the stability of the converter. To address this issue due to CPLs, passive damping network could be introduced to the converter system to improve the system stability [14]. However, passive components can lead to additional power losses and reduce the efficiency. Active damping schemes also have been proposed to improve the stability with reduced power losses [11], [12]. Nevertheless, the conventional active damping scheme is achieved by emulating the passive components, which may conflict with other control objectives [14]. Thus, additional design effort for the high-performance DAB controller is still required to take into the account of the load characteristics.

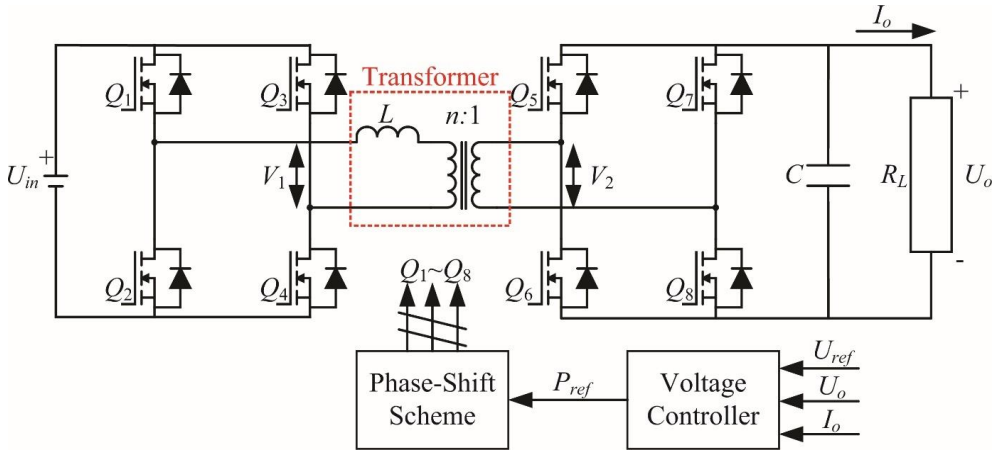
To attenuate the disturbances and uncertainties, various types of disturbance rejection control (DRC) has been proposed. Based on the design domains, the conventional DRC schemes could be classified into two categories: frequency-domain DRC and time-domain DRC [17]. Among the frequency-domain DRC schemes, the disturbance observer (DOB) has been widely adopted in the control systems, which utilizes a disturbance estimate filter to achieve the compensation of the disturbances, and the disturbance rejection performance could be easily realized by selecting proper disturbance estimate filter [17]-[19]. Meanwhile, DRC design could also be conducted in the time-domain, like the active disturbance rejection control [20]. Compared with the frequency-domain counterparts, the state-space based time-domain DRC schemes is more suitable for multiple-input multiple-output system. Recently, a mix-domain DRC scheme, uncertainty and disturbance estimator (UDE) based control, has been proposed to attenuate lumped disturbances and improve the disturbance rejection performance [21]-[23]. Compared with those single domain control schemes, UDE achieves the nominal feedback control and estimates the lumped disturbance through the use of system time-domain model and states measurements, then a

frequency-domain filter is used to make the control law causal and improve the system robustness to measurement noises.

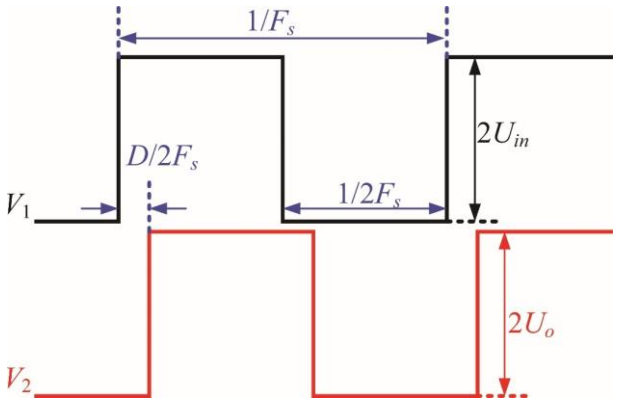
In this chapter, starting from the concept and preliminary study presented in [24], an UDE based voltage controller is proposed for the DAB converters to improve the system robustness while achieving the high accuracy tracking. First, the DAB converter circuit model and the model of the phase-shift modulation are integrated and re-modeled based on the converter output current to provide a generic linear model for the DAB controller design. Then a UDE based voltage controller is designed based on the proposed DAB model and the computation time delay also has been considered in the design. Rigorous stability analysis has been provided as the guidance of the parameter tuning. Besides, the output impedance of the UDE controlled DAB converter is also derived to show the stability boundary when the converter feeds a CPL. Comparative experimental studies have been conducted to show the effectiveness of the proposed schemes. The experimental results have proved that the proposed scheme can notably improve the voltage tracking performance even under significant parameter uncertainties. Meanwhile, the excellent disturbance rejection performance of the proposed scheme could also extend the stability boundary when feeding the CPL.

2.2 A Brief Review of DAB Converters and UDE Scheme

2.2.1 Review of the DAB Converter



(a)



(b)

Figure 2-1. (a) Schematic of the DAB converter and (b) single-phase-shift modulation scheme.

Figure 2-1(a) shows the schematic of the DAB converter with phase-shift control scheme, where U_{in} is the input dc power supply, Q_1-Q_8 are power devices, C is the output capacitor, R_L represents the load, L is the leakage inductance of the transformer, I_o is the output current, U_o is the output voltage, and U_{ref} is the reference voltage that U_o should track. In order to transfer the

power between the input and output ports, phase-shift modulation schemes are commonly used in the DAB converter [3]. Figure 2-1(b) shows the most widely used single-phase-shift (SPS) modulation scheme, where V_1 and V_2 are the voltages across the transformer primary and secondary windings respectively, output voltage duty-ratio is fixed as 50%, F_s is the switching frequency, D is phase-shift angle. The power transferred between the input and output ports when the SPS scheme is applied could be written as

$$P = \frac{nU_{in}U_o}{2F_sL} D(1-D) \tag{2-1}$$

It should be noticed that the waveforms shown in Figure 2-1(b) are the ideal output voltages of the DABs. The deadtime must be inserted in practice to avoid shooting through the two switches in the same phase leg, which will lead to distortions in the output voltages and change the power transmission characteristic of the DAB converter. Thus, in this work, both the nonlinearities due to the deadtime effect, as well as the uncertainties caused by the circuit parameters, are regarded as the system uncertainties. The voltage controller should effectively compensate the system uncertainties and improve the voltage tracking accuracy.

2.2.2 Review of UDE

Consider a linear system with uncertainty and disturbance

$$\frac{dx}{dt} = (A+\Delta A)x(t) + Bu(t) + f(t) \tag{2-2}$$

where $x(t)$ is the system state, $u(t)$ is the input of the system, A and B are the known state matrixes, ΔA represents the unknown dynamics of the system, and $f(t)$ is the external disturbance [21]. The effect of the uncertainty and disturbance could be represented as $u_d(t)= \Delta Ax(t)+f(t)$, and the control

objective of UDE is to eliminate $u_d(t)$ and ensure state variable $x(t)$ tracks its reference $x_m(t)$. The reference state $x_m(t)$ could be obtained through the reference model

$$\frac{dx_m}{dt} = A_m x_m(t) + B_m r(t) \tag{2-3}$$

where A_m and B_m are the reference system matrixes, which determine the closed-loop performance of the system, and $r(t)$ is the reference signal. In other words, when a high-performance controller is adopted to the system and the state $x(t)$ can tightly track its reference $x_m(t)$, the closed-loop system performance could be easily determined by selecting proper system matrixes A_m and B_m. In order to achieve the high accuracy tracking to the reference state $x_m(t)$, the tracking error could be defined as $e(t)= x_m(t)- x(t)$, and the converge rate of the tracking error could be defined through the following system

$$\frac{de}{dt} = A_m e(t) + Ke(t) \tag{2-4}$$

where K is the state-feedback gain and A_m+K should be Hurwitz. Combining the system model (2-2), desired closed-loop model (2-3), and the error convergence model (2-4), the control input should satisfy

$$u(t) = B^{+}\left[A_m x(t) - Ax(t) + B_m r(t) - Ke(t) - u_d(t)\right] \tag{2-5}$$

where B^{+} is the pseudoinverse of B.

However, it should be noticed that the uncertainty and disturbance is unknown in most of the practical applications. Thus, an estimate $u_{de}(t)$ is introduced in $u(t)$ to replace $u_d(t)$, which could be represented as

$$\begin{aligned} u_{de}(t) &= g_f(t) * u_d(t) \\ &= L^{-1}\left\{G_f(s)\left[sx(s) - Ax(s) - Bu(s)\right]\right\} \end{aligned} \tag{2-6}$$

where u_{de} is the estimate of u_d, g_f is the impulse response of a strictly proper filter $G_f(s)$, * represents the convolution operator, and L^{-1} is the inverse Laplace Transform operator. Thus, $u_{de}(t)$ could achieve the estimate of $u_d(t)$ within the bandwidth of $G_f(s)$. Besides, the introduction of the strictly proper stable function $G_f(s)$ could also make the term $G_f(s)sx(s)$ realizable.

2.3 UDE Based Robust Voltage Control for the DAB Converter

2.3.1 UDE Based Robust Voltage Control

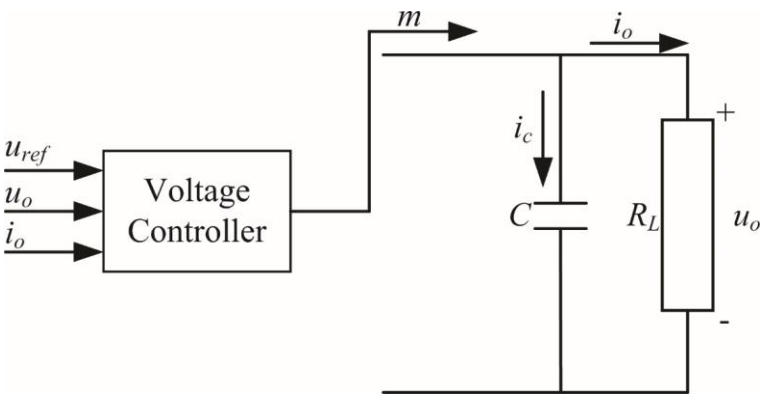


Figure 2-2. Output current model of the DAB converter.

Based on the power transmission characteristic of the SPS scheme (2-1), the relationship between the phase-shift angle D and the output power P is nonlinear, which increases the complexity when designing the controller. Moreover, when advanced phase-shift schemes are implemented, such as the dual- and triple-phase shift schemes, the power model can be more complicated [16]. To simplify the controller design and enhance the compatibility of the controller, an output current model of the DAB converter is shown in Figure 2-2, where u_{ref} is the reference

voltage that the output voltage u_o should track, m is the output current of the DAB converter, which consists of the output capacitor current, i.e., i_c, and the load current, i.e., i_o. Thus, the dynamic model of the DAB converter under the SPS scheme could be rewritten as

$$\begin{cases} m = \dfrac{nU_{in}}{2F_s L} D\left(1-D\right) \\ \dfrac{du_o}{dt} = \dfrac{m - i_o}{C} \end{cases} \tag{2-7}$$

$$D = \frac{1-\sqrt{1-8F_s L m_{ref} / \left(nU_{in}\right)}}{2} \tag{2-8}$$

The revised model of the DAB converter (2-7) decouples the selection of the phase-shift schemes and the design of the DAB controller. The voltage controller could be designed based on the current model (2-7), which is a linear system regardless the phase-shift scheme. The output of the voltage controller is the converter output current m, which is then generated through the phase-shift scheme. Different phase-shift schemes could be utilized to achieve the optimization [3], while retaining the same voltage controller and control performance, as the current model (2-7) will be the same. Thus, the proposed current-oriented controller design concept could simplify the controller design. In contrast, if the output of the controller is directly designed as the phase-shift angle, the design of the controller must consider the complicated nonlinear converter model if advanced phase-shift schemes are utilized. Also, the controller will lose the generality, as the controller need to be redesigned if a different phase-shift scheme is deployed [2]. It should be noted that (2-8) is only valid for the ideal case, i.e., external disturbances, system uncertainties, computation time delay, and deadtime effect are not existed. In practice, the phase-shift angle D

calculated through (2-8) often leads to tracking errors in the output current *m* and affect the voltage tracking accuracy, as such the voltage controller should compensate the system uncertainties and eliminate the tracking error in the output voltage.

Considering the non-ideal system characteristics, including the deadtime, parameters uncertainty, external disturbance, computation time delay, etc., the ideal current model of the DAB converter (7) could be rewritten into a transfer function as

$$su_o(s) = \frac{e^{-T_s s} m\left[1+\Delta_{Total}(s)\right] - i_o(s) + f(s)}{C} \tag{2-9}$$

where $e^{-T_s s}$ is the one-step computation time delay, $T_s = 1/F_s$ is the sampling period, Δ_{Total} represents the system uncertainty, and $f(s)$ is the external disturbance.

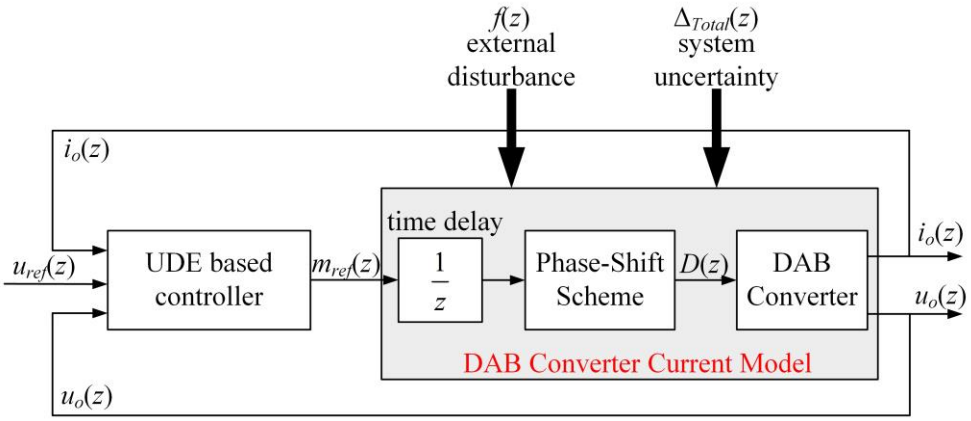


Figure 2-3. UDE controlled DAB converter.

Based on the UDE scheme reviewed in Section 2-2 and the DAB converter current model (2-9), define the reference system as

$$\frac{du_m}{dt} = -\alpha u_m(t) + \alpha u_{ref}(t) \tag{2-10}$$

where $\alpha>0$ is the bandwidth of the closed-loop DAB converter. The voltage tracking error is $e(t)=u_m(t)-u_o(t)$, whose dynamics satisfy

$$\frac{de}{dt} = -\alpha e(t) - ke(t) \tag{2-11}$$

Thus, the error convergence rate is determined by $\alpha+k$. Based on the UDE scheme and the system model (2-9), the control law can be written as

$$m_{ref}(t) = \underbrace{m_{fb}(t)}_{\text{state-feedback}} - \underbrace{f_e(t)}_{\substack{\text{disturbance} \\ \text{estimation}}} \tag{2-12}$$

where $m_{fb}(t)$ is the nominal state-feedback, which satisfies

$$m_{fb}(t) = \alpha C\left[u_{ref}(t) - u_o(t) + ke(t)\right] + i_o(t) \tag{2-13}$$

and $f_e(t)$ is the estimate of the disturbance $f(t)$, which could be written as

$$\begin{aligned} f_e(t) &= g_f(t) * f(t) \\ &= L^{-1}\left[G_f(s)\right] * \left[i_o(t) + C\frac{du_o}{dt} - m_{ref}(t - T_s)\right] \end{aligned} \tag{2-14}$$

The nominal state-feedback term (2-13) could achieve the desired tracking performance if the time delay $e^{-T_s s}$, system uncertainty $\Delta_{Total}(s)$, and disturbance $f(s)$ are not existed. The estimate of the disturbance $f_e(t)$ is used to attenuate the unideal system dynamics. Here, the disturbance

estimate filter is designed as $G_f(s) = \beta/(s+\beta)$, which could estimate the disturbance within the bandwidth β. In summary, there are three controller parameters that need to be designed: closed-loop bandwidth α, tracking error convergence rate k, and disturbance rejection bandwidth β. Figure 2-3 shows the block diagram of the UDE controlled DAB converter, where the proposed UDE controller measures the load current $i_o(z)$ and output voltage $u_o(z)$, and generates the current reference $m_{ref}(z)$. Then the phase-shift scheme block will calculate the phase-shift angle accordingly, however, the angle will be deployed to the converter in the next switching period due to the computation delay.

2.3.2 Stability Analysis

Theorem 2-1: Consider a DAB converter system (2-9) controlled by the UDE based voltage controller (2-12)-(2-14), and the controller is digitalized with sampling time T_s. The system is stable if

(1) roots of $1/(zG_s(z)+\alpha+k)$ are within the unit circle;

(2) external disturbance $f(z)$ is bounded and system uncertainty $\Delta_{Total}(z)$ is stable;

(3)

$$\left\| \frac{G_f(z)G_s(z)+\alpha+k}{zG_s(z)+\alpha+k} \Delta_{Total}(z) \right\|_\infty < 1 \tag{2-15}$$

where $z = e^{T_s s}$ and $G_f(z)$, $G_s(z)$, $f(z)$, and $\Delta_{Total}(z)$ are the Z-domain counterparts of the filter $G_f(s)$, derivative operator s, disturbance $f(s)$, and uncertainty $\Delta_{Total}(s)$ respectively.

Proof: The control law in (2-12)-(2-14) could be rewritten as

$$
\begin{aligned}
m_{ref}(z) &= m_{fb}(z) - f_e(z) \\
&= \alpha C\left[u_{ref}(t) - u_o(t) + ke(t)\right] + i_o(t) \\
&\quad - G_f(z)\left[i_o(t) + CG_s(z)u_o(z) - \frac{m_{ref}(z)}{z}\right] \\
&= \frac{z}{z - G_f(z)}\Big[\alpha C u_{ref}(z) - \alpha C u_o(z) + kCe(z) + i_o(z) \\
&\quad - G_f(z) i_o(z) - CG_f(z)G_s(z)u_o(z)\Big]
\end{aligned}
\tag{2-16}
$$

Combining (2-16) with the DAB converter model (2-9), the output voltage u_o could be written as

$$
\begin{aligned}
u_o(s) &= \frac{\frac{m_{ref}(z)}{z}\left[1 + \Delta_{Total}(z)\right] - i_o(z) + f(z)}{CG_s(z)} \\
&= \Big[\alpha C u_{ref}(z) - \alpha C u_o(z) + kCe(z) + i_o(z) - G_f(z) i_o(z) \\
&\quad - CG_f(z)G_s(z)u_o(z)\Big]\frac{1 + \Delta_{Total}(z)}{CG_s(z)\left[z - G_f(z)\right]} \\
&\quad - \frac{\left[i_o(z) - f(z)\right]\left[z - G_f(z)\right]}{CG_s(z)\left[z - G_f(z)\right]} \\
&= \frac{\left[1 + \Delta_{Total}(z)\right]\left[\alpha u_{ref}(z) + k u_m(z)\right] + \frac{\left[z - G_f(z)\right] f(z)}{C}}{zG_s(z) + \alpha + k + \Delta_{Total}(z)\left[G_f(z)G_s(z) + \alpha + k\right]} \\
&\quad + \frac{\Delta_{Total}(z)\left[1 - G_f(z)\right] + (1 - z)}{zG_s(z) + \alpha + k + \Delta_{Total}(z)\left[G_f(z)G_s(z) + \alpha + k\right]}\frac{i_o(z)}{C}
\end{aligned}
\tag{2-17}
$$

where $u_m(z)$ is the Z-domain counterpart of $u_m(s)$.

As the external disturbance $f(z)$ is bounded and the system uncertainty $\Delta_{Total}(z)$ is stable, the closed-loop system stability is determined by

$$\frac{1}{zG_s(z)+\alpha+k+\Delta_{Total}(z)\left[G_f(z)G_s(z)+\alpha+k\right]} = \frac{1}{zG_s(z)+\alpha+k}\frac{1}{1+\frac{G_f(z)G_s(z)+\alpha+k}{zG_s+\alpha+k}\Delta_{Total}(z)} \tag{2-18}$$

Thus, based on the small gain theorem [25] and (2-18), the closed-loop stability requires that $\frac{1}{zG_s(z)+\alpha+k}$ is stable and $\left\|\frac{G_f(z)G_s(z)+\alpha+k}{zG_s(z)+\alpha+k}\Delta_{Total}(z)\right\|_\infty < 1$.

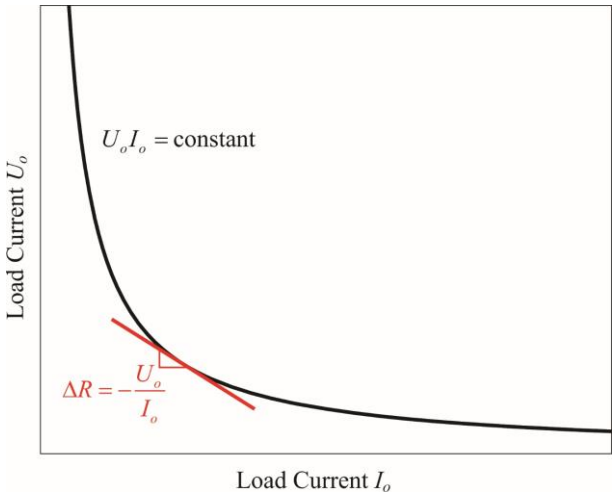
Based on (2-17), the voltage tracking error satisfies

$$\begin{aligned} e(z) &= u_m(z)-u_o(z) \\ &= \frac{G_s(z)(z-1)+\Delta_{Total}(z)G_s(z)\left[G_f(z)-1\right]}{zG_s(z)+\alpha+k+\Delta_{Total}(z)\left[G_f(z)G_s(z)+\alpha+k\right]}u_m(z) \\ &\quad -\frac{\left[z-G_f(z)\right]f(z)+\left\{\Delta_{Total}(z)\left[1-G_f(z)\right]-(1-z)\right\}i_o(z)}{C\left\{zG_s(z)+\alpha+k+\Delta_{Total}(z)\left[G_f(z)G_s(z)+\alpha+k\right]\right\}} \end{aligned} \tag{2-19}$$

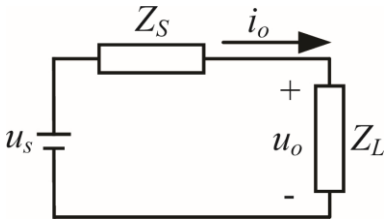
Remark 2-1: The tracking error (2-19) suggests that the uncertainty $\Delta_{Total}(z)$ and disturbance $f(z)$ could be effectively attenuated when $1-G_f(z)\approx 0$ and $z-G_f(z)\approx 0$ respectively. Especially, at low-frequency region ($\omega<F_s/10$), the disturbance rejection performance also could be represented by $\left|1-G_f(j\omega)\right|$, as $e^{T_s j\omega}\approx 1$. A high bandwidth $G_f(z)$ could reject the disturbance well. However, as the stability condition (2-15) shows, high bandwidth may result in instability when the amplitude of the system uncertainty $\Delta_{Total}(z)$ is large. Thus, the design of $G_f(z)$ needs to tradeoff between disturbance rejection performance and stability performance.

Remark 2-2: Besides the deadtime effect, one of the major sources for system uncertainty is the circuit parameters perturbation. Especially, the leakage inductance L and output capacitance C may deviate from their nominal values. Supposing L_d and C_d are the parameters error of the leakage inductance and output capacitor, while L_n and C_n are the nominal values used in the controller design. The actual circuit parameters satisfy $L=L_d+L_n$ and $C=C_d+C_n$. The system uncertainty caused by the leakage inductance and output capacitance perturbations are marked as Δ_L and Δ_C respectively. Based on (2-7) and (2-9), Δ_L could be written as $\Delta_L(z)=\dfrac{-L_d}{L_n+L_d}$. Similarly, the system uncertainty caused by the capacitance error could be represented as $\Delta_C(z)=\dfrac{C_d}{C_n}\left[1-\dfrac{i_o(z)}{CG_s(z)u_o(z)+i_o(z)}\right]$. The modeling of the uncertainties caused by the circuit parameters perturbation could be used in the robustness analysis.

2.3.3 Stability Under the CPL



(a)



(b)

Figure 2-4. (a) Negative incremental impedance of a CPL and (b) impedance model of the UDE controlled DAB converter.

When the DAB converter feeds a CPL, only the nominal stability condition given in Theorem 2-1 cannot ensure the stability. Figure 2-4(a) shows the voltage-current relationship of the CPL, and the incremental impedance of the CPL could be written as $\Delta R=-U_o/I_o$. Figure 2-4(b) is the equivalent impedance model of the UDE controlled DAB converter [14], where u_s is the ideal voltage source representing the converter output voltage under the no load situation, Z_S is the

output impedance of the converter, Z_L is the load, u_o is the output voltage, and i_o is the output current. Based on (2-17), the ideal voltage source is

$$u_s(s)=\frac{\left[1+\Delta_{Total}(z)\right]\left[\alpha u_{ref}(z)+ku_m(z)\right]+\frac{\left[z-G_f(z)\right]f(z)}{C}}{zG_s(z)+\alpha+k+\Delta_{Total}(z)\left[G_f(z)G_s(z)+\alpha+k\right]} \tag{2-20}$$

and the output impedance Z_S could be written as

$$\begin{aligned} Z_S(s)&=\frac{\Delta_{Total}(z)\left[1-G_f(z)\right]+(1-z)}{zG_s(z)+\alpha+k+\Delta_{Total}(z)\left[G_f(z)G_s(z)+\alpha+k\right]}\frac{1}{C}\\ &=\frac{1}{C\left[zG_s(z)+\alpha+k\right]}\frac{\Delta_{Total}(z)\left[G_f(z)-1\right]+(z-1)}{1+\frac{G_f(z)G_s(z)+\alpha+k}{zG_s(z)+\alpha+k}\Delta_{Total}(z)} \end{aligned} \tag{2-21}$$

Thus, the output voltage $u_o(z)$ could be written as

$$\begin{aligned} u_o(z)&=\frac{Z_L(z)}{Z_S(z)+Z_L(z)}u_s(z)\\ &=\frac{1}{1+\frac{Z_S(z)}{Z_L(z)}}u_s(z) \end{aligned} \tag{2-22}$$

It can be seen from (2-22) that the nominal stability condition given in Theorem 2-1 could ensure the stability of Z_S. However, when the load impedance $Z_L(z)$ is a negative constant, i.e., $Z_L(z)=-U_o/I_o$, a stable $Z_S(s)$ cannot ensure the system stability. Based on the small gain theorem [25], a sufficient condition for the system stability is

$$\left\| \frac{Z_S(z)}{Z_L(z)} \right\|_\infty < 1 \tag{2-23}$$

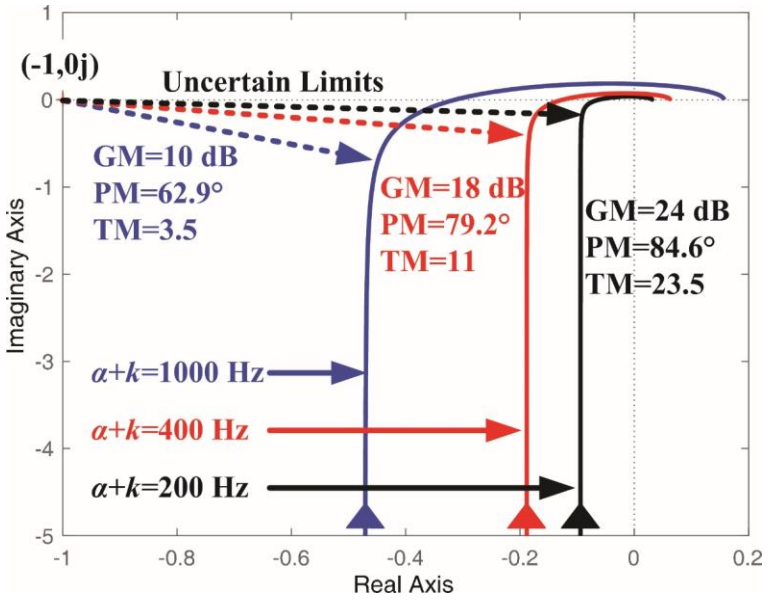
Although the stability condition (2-23) may lead to a more conservative requirement on $Z_S(z)$, a small value of $Z_S(z)$ is always desired as it could improve the tracking performance of the converter. Thus, the stability of the DAB converter when feeding CPL and a good tracking performance could be obtained by reducing the amplitude of the output impedance $Z_S(z)$. Based on (2-21), the introduction of $G_f(z)$ could effectively attenuate the system uncertainties and reduce the output impedance within its bandwidth.

2.3.4 Controller Design

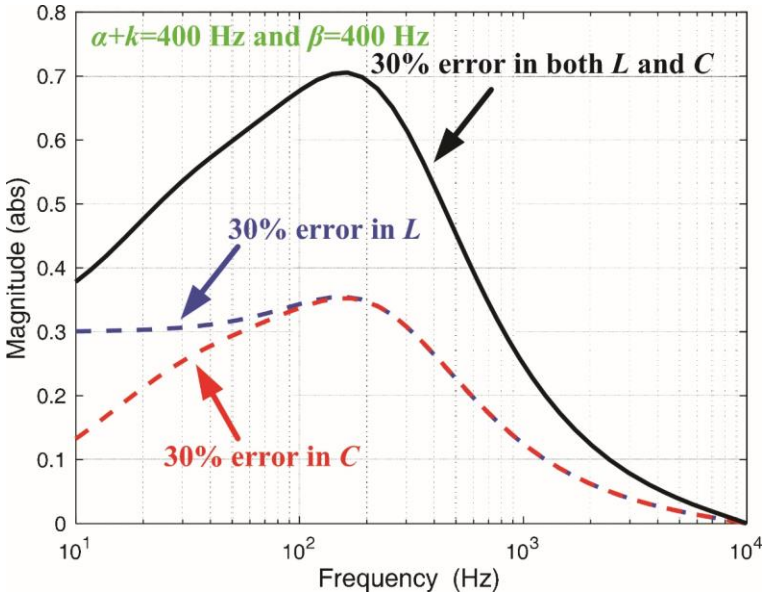
Based on the derived control law (2-12)-(2-14), there are three parameters needed to be designed: the closed-loop bandwidth α, the error convergence rate *k*, and the disturbance rejection bandwidth β. In order to maintain the system stability, the stability criteria given in Theorem 2-1 should be satisfied. Moreover, the output impedance of the UDE controlled DAB converter should also satisfy (2-23) when feeding a CPL. The detailed design process will be discussed in following.

First, the closed-loop bandwidth and error convergence rate could be designed based on the requirement that the roots of $1/\left(zG_s(z)+\alpha+k\right)$ are within the unit circle. Figure 2-5(a) shows the Nyquist plot of system $1/\left(zG_s(z)+\alpha+k\right)$, where GM is the gain margin in dB, PM is the phase margin in degrees, and TM is the time delay margin in steps. It can be seen that a good robustness and dynamic performance could be obtained when $\alpha+k$=400 Hz. Larger $\alpha+k$ could improve the dynamic response at the cost of worse robustness. Here, the closed-loop bandwidth α is selected as 100 Hz, and the error convergence rate *k* is designed as 300 Hz. Then the design of

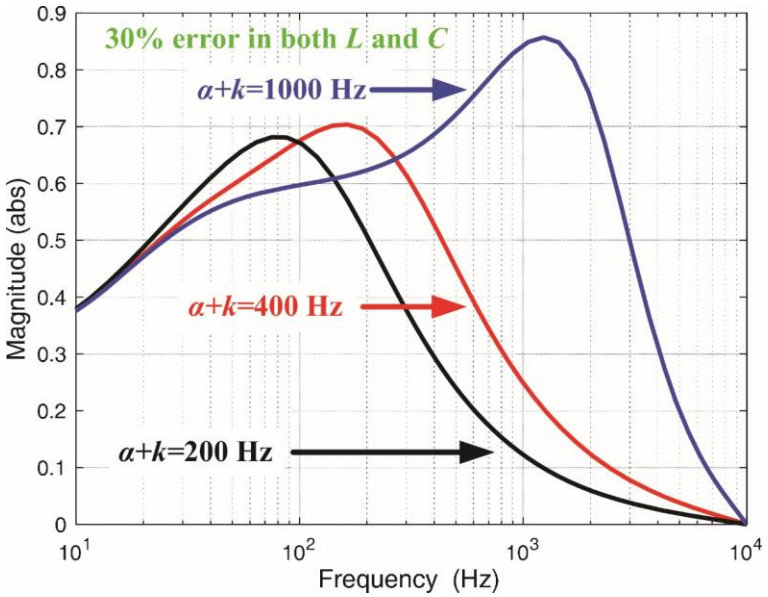
the disturbance estimate filter should satisfy (2-3). In this work, the disturbance rejection bandwidth is set as β=400 Hz to tradeoff between the system robustness and disturbance rejection performance. Figure 2-5(b) shows the frequency response of $\left|\frac{G_f(z)G_s(z)+\alpha+k}{zG_s(z)+\alpha+k}\Delta_{Total}(z)\right|$. It can be seen that a 400 Hz disturbance rejection bandwidth could maintain the system stability even under 30% circuit parameters error. Figure 2-5(c) shows the system stability performance under different closed-loop bandwidths and error convergence rates, when the disturbance rejection bandwidth β is fixed as 400 Hz and both L and C have 30% error. It can be seen that the system robustness is deteriorated when a high α+k is adopted, which matches the trend shown in Figure 2-5(a).


(-1,0j)
Uncertain Limits
GM=10 dB
PM=62.9°
TM=3.5
GM=18 dB
PM=79.2°
TM=11
GM=24 dB
PM=84.6°
TM=23.5
α+k=1000 Hz
α+k=400 Hz
α+k=200 Hz
Imaginary Axis
Real Axis

(a)


α+k=400 Hz and β=400 Hz
30% error in both L and C
30% error in L
30% error in C
Magnitude (abs)
Frequency (Hz)

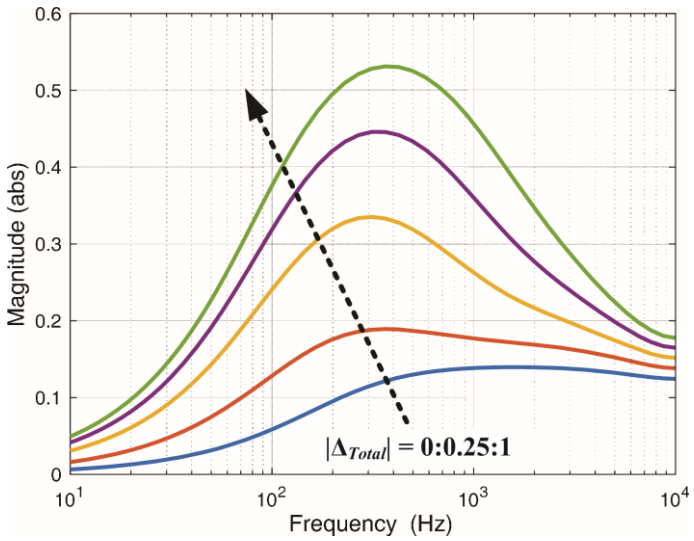
(b)



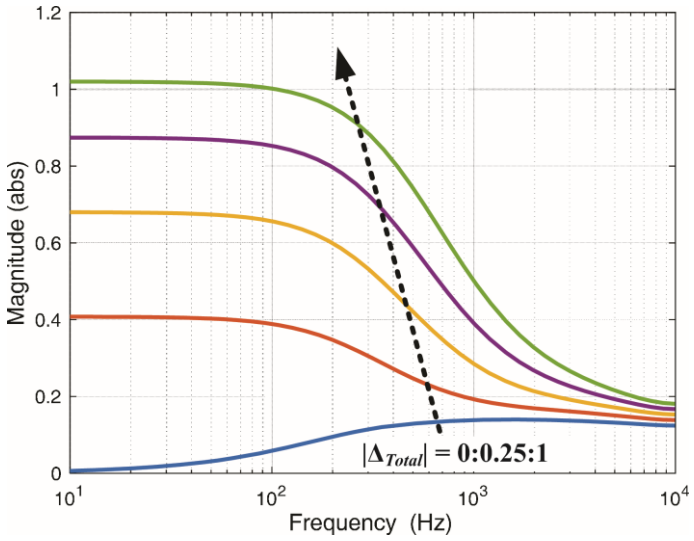
(c)

Figure 2-5. (a) Nyquist plot of $\frac{1}{zG_s(z)+\alpha+k}$, (b) and (c) frequency responses of $\left|\frac{G_f(z)G_s(z)+\alpha+k}{zG_s(z)+\alpha+k}\Delta_{Total}(z)\right|$: (b) under different parameter uncertainties and (c)under different closed-loop bandwidths and error convergence rates.

Considering the DAB converter feeding a CPL, the output impedance of the converter is shown in Figure 2-6. The system uncertainty $\Delta_{Total}(z)$ is regarded as a constant to show the effectiveness of the disturbance compensation. It can be seen that the introduction of $G_f(z)$ could notably reduce the amplitude of $Z_S(z)$ which means a larger stable margin is obtained when feeding a CPL. Based on Figure 2-6(a) and (2-23), the maximum negative resistance that the UDE controlled DAB converter could feed is Z_L=−0.54 Ω. In this work, a 120 W CPL is considered, and the maximum output voltage and current of the converter is 200 V and 10 A respectively. Thus, the maximum negative incremental resistance of the CPL is ΔR_{max}=−1.2 Ω and the UDE controlled converter could maintain the system stability.



(a)



(b)

Figure 2-6. Output impedance of the UDE controlled DAB converter. Bandwidth of (a) $G_f(z)$ = 400 Hz and (b) $G_f(z)$= 0.

2.4 Experimental Studies

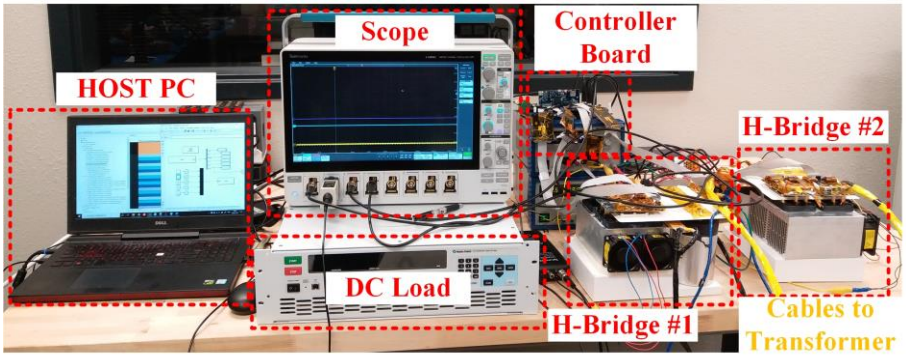


Figure 2-7. Experimental Setup.

TABLE 2-1 Key Parameters of the DAB Converter used in the Experimental Study

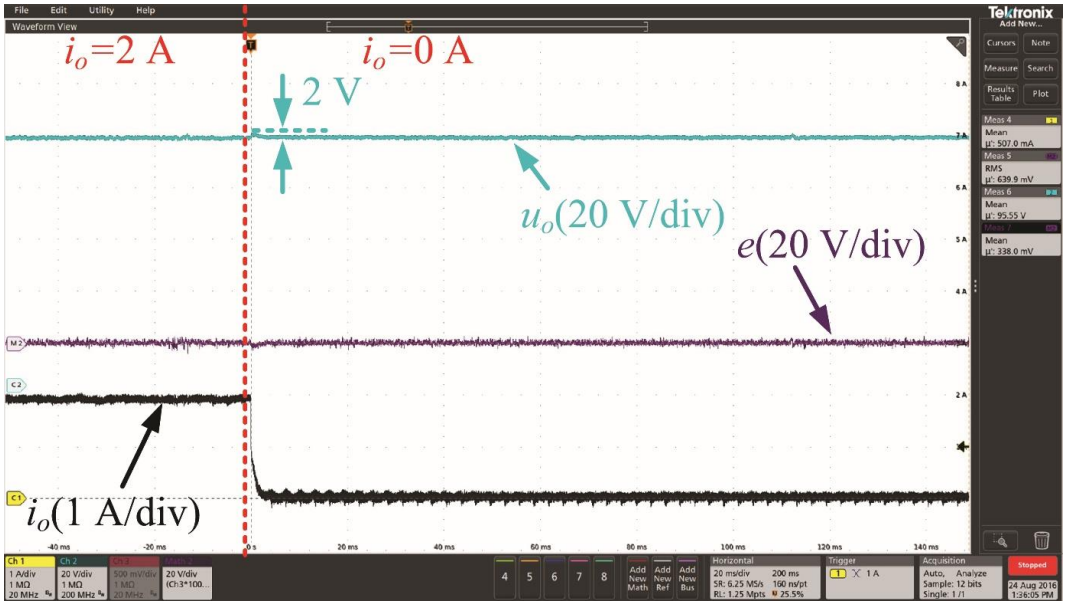
Parameter	Value	Parameter	Value
Input Voltage U_{in}	100 V	Turns Ratio n	1
Leakage Inductance L	80 μH	Closed-Loop Bandwidth α	100 Hz
Output Capacitor C	195 μF	Error Convergence Rate k	300 Hz
Power of CPL	120 W	Disturbance Rejection Bandwidth β	400 Hz

To verify the effectiveness of the proposed schemes, a series of comparative experiments are conducted. Table 2-1 summarized the converter and controller parameters. For comparison purpose, a proportional-integral (PI) controller is also tested. The PI controller is designed based on the DAB converter current model (2-7), and the controller structure is almost the same as the

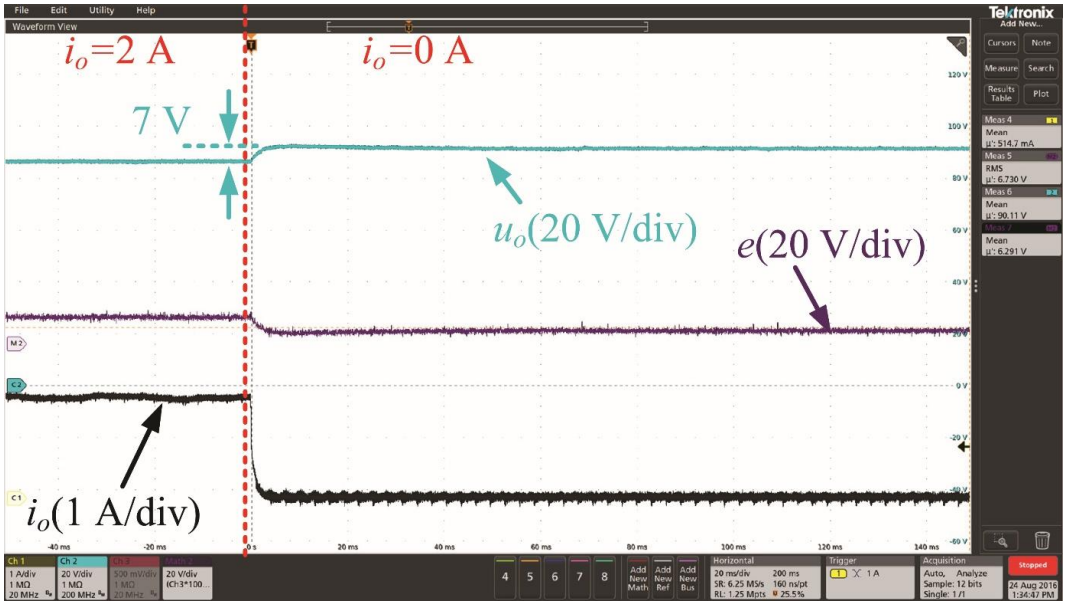
one shown in Figure 2-3 except that the UDE controller is replaced by the PI controller. Moreover, the output current feedforward compensation is also implemented with the PI controller to improve the dynamic response, and the control output of the PI controller could be written as

$$m_{ref|PI}(z)=\left(k_p+k_i\frac{T_s}{z-1}\right)\left[u_{ref}(z)-u_o(z)\right]+i_o(z) \tag{2-24}$$

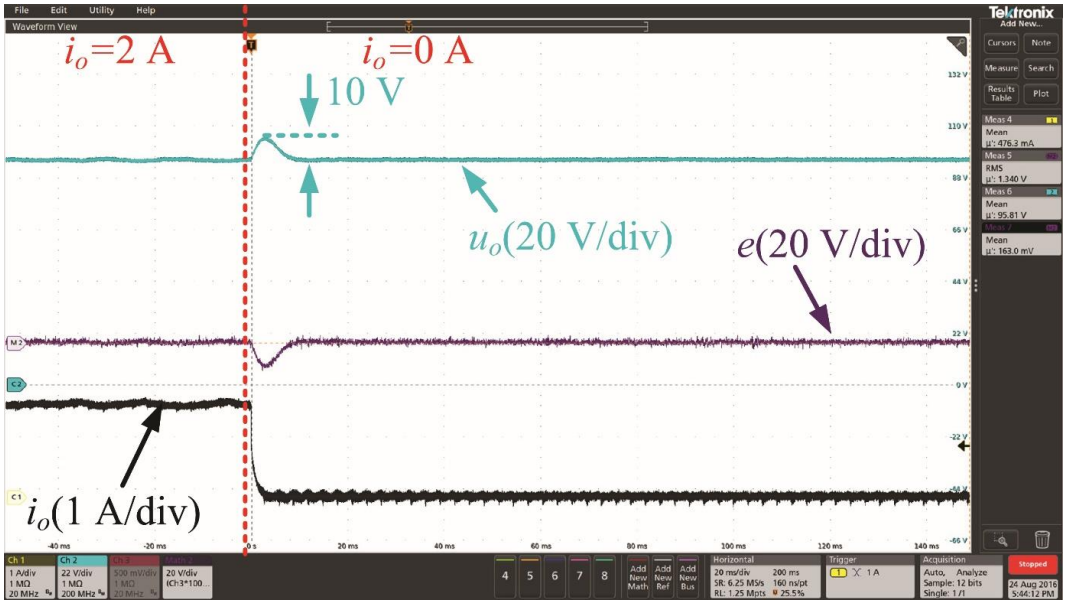
where k_p and k_i are the PI gains. In this work, the PI controller is designed as k_p =0.34 and k_i=216, and the closed-loop system bandwidth of the PI controlled DAB converter is also 400 Hz to ensure a fair comparison, which is the same as the disturbance rejection bandwidth of the UDE controller. Figure 2-7 shows the experiment setup. The deadtime of the converter is set as 2 μs.



(a)



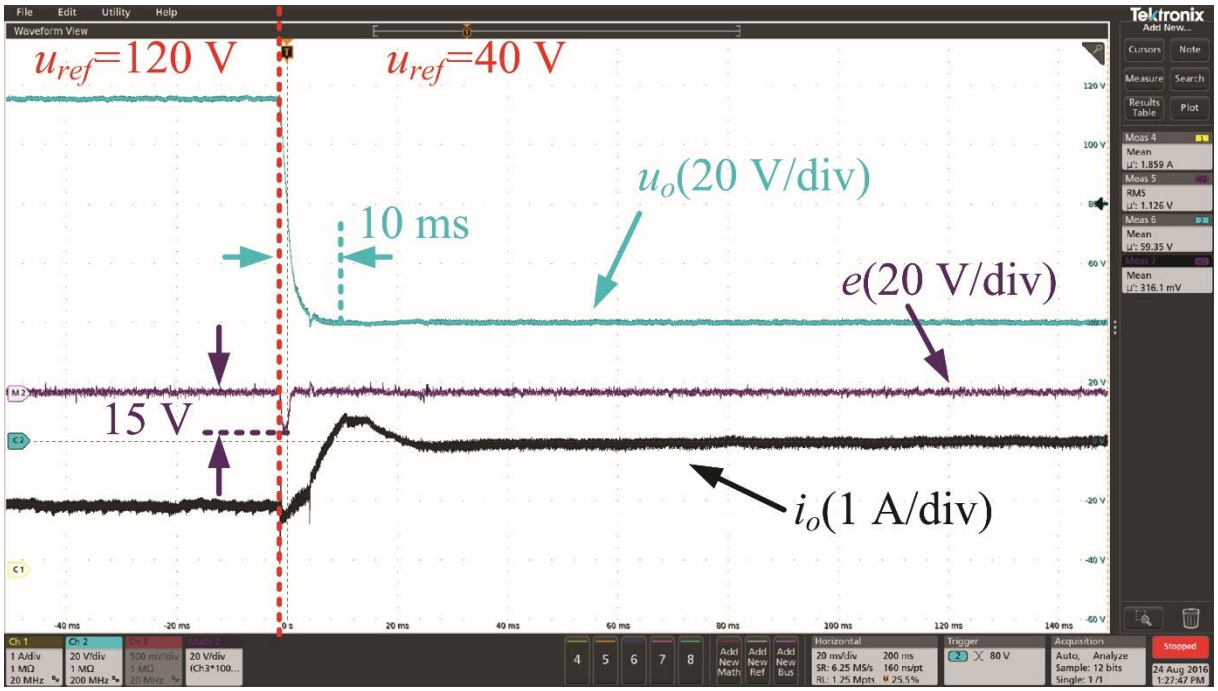
(b)



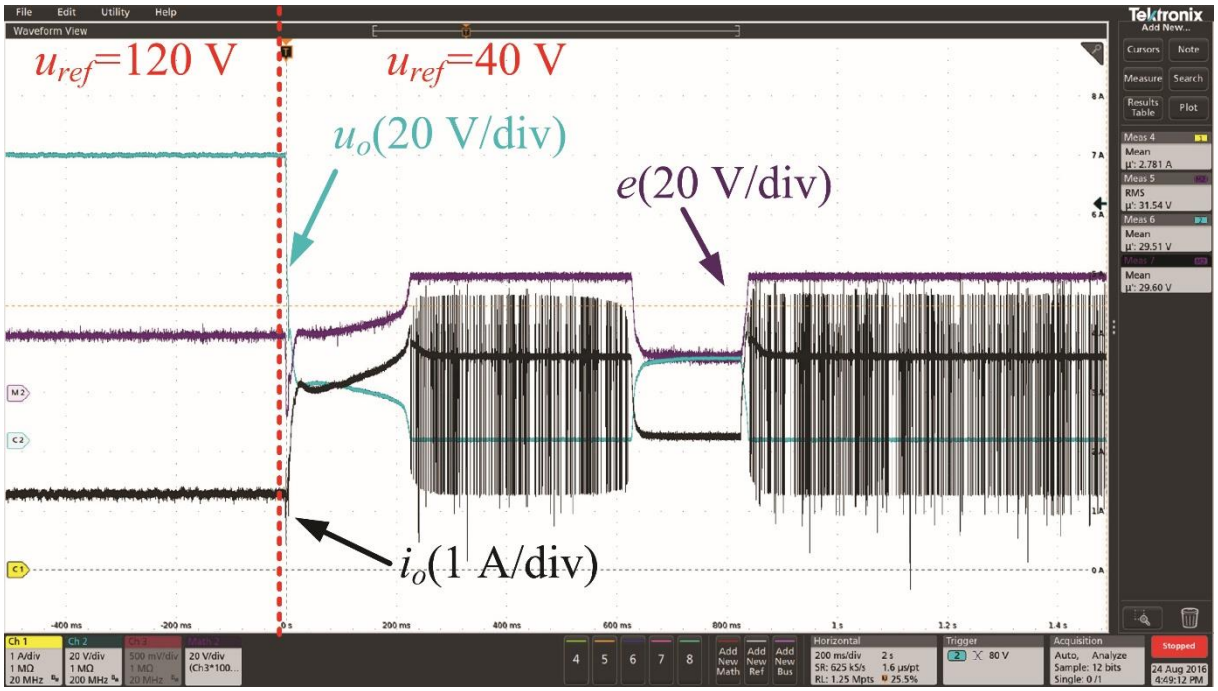
(c)

Figure 2-8. Transient responses of the DAB converter under load step change with different controllers: (a) UDE controller with 400 Hz bandwidth $G_f(z)$ (b) UDE controller with $G_f(z)$=0, and (c) PI controller.

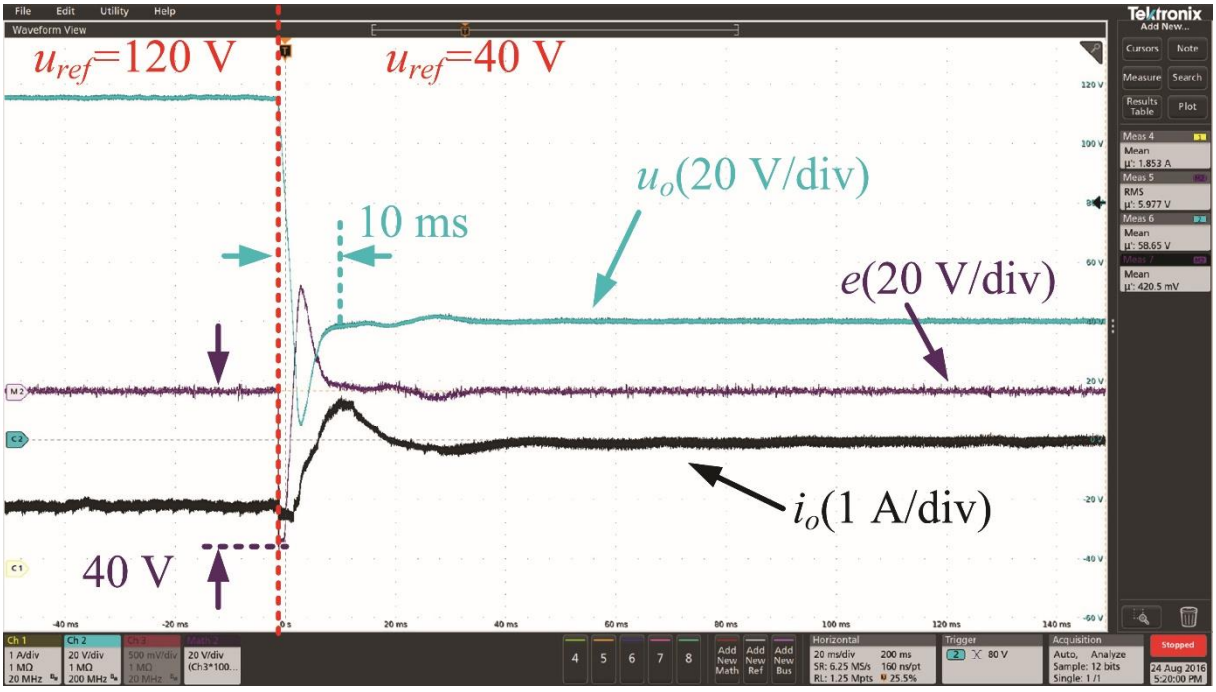
Figure 2-8 shows the dynamic responses of the DAB controller with different controllers, where the output current changes from 2 A to 0 A and the reference output voltage is u_{ref}=100 V. It can be seen that with the 400 Hz bandwidth disturbance compensation, the UDE controller could effectively attenuate the disturbance, and the tracking error is relatively small. Without the disturbance compensation, i.e., $G_f(z)$=0, it can be seen that the tracking error cannot converge to 0. Actually, both Figure 2-6 and (2-21) show that the system uncertainty will affect the converter output impedance, and $G_f(z)$ could notably attenuate the system uncertainty and reduce the output impedance within its bandwidth. Lower output impedance means that the output voltage is more robust when the load changes. Similar to the UDE controller, the PI controller could also achieve the zero steady-state voltage tracking, but the disturbance attenuation performance is worse than the UDE controller.


u_{ref}=120 V
u_{ref}=40 V
u_o(20 V/div)
10 ms
e(20 V/div)
15 V
i_o(1 A/div)

(a)


u_{ref}=120 V
u_{ref}=40 V
u_o(20 V/div)
e(20 V/div)
i_o(1 A/div)

(b)



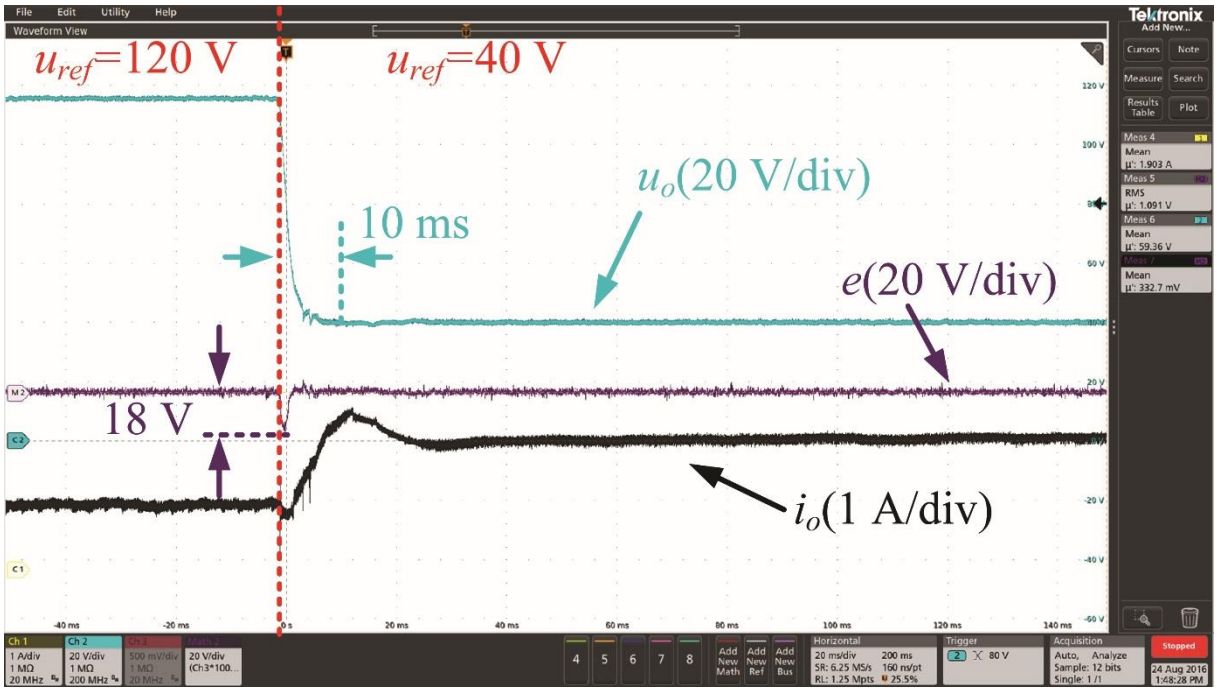
(c)

Figure 2-9. Transient responses of the DAB converter when feeding a 120 W CPL with different controllers and accurate parameters: (a) UDE controller with 400 Hz bandwidth $G_f(z)$ (b) UDE controller with $G_f(z)$=0, and (c) PI controller.

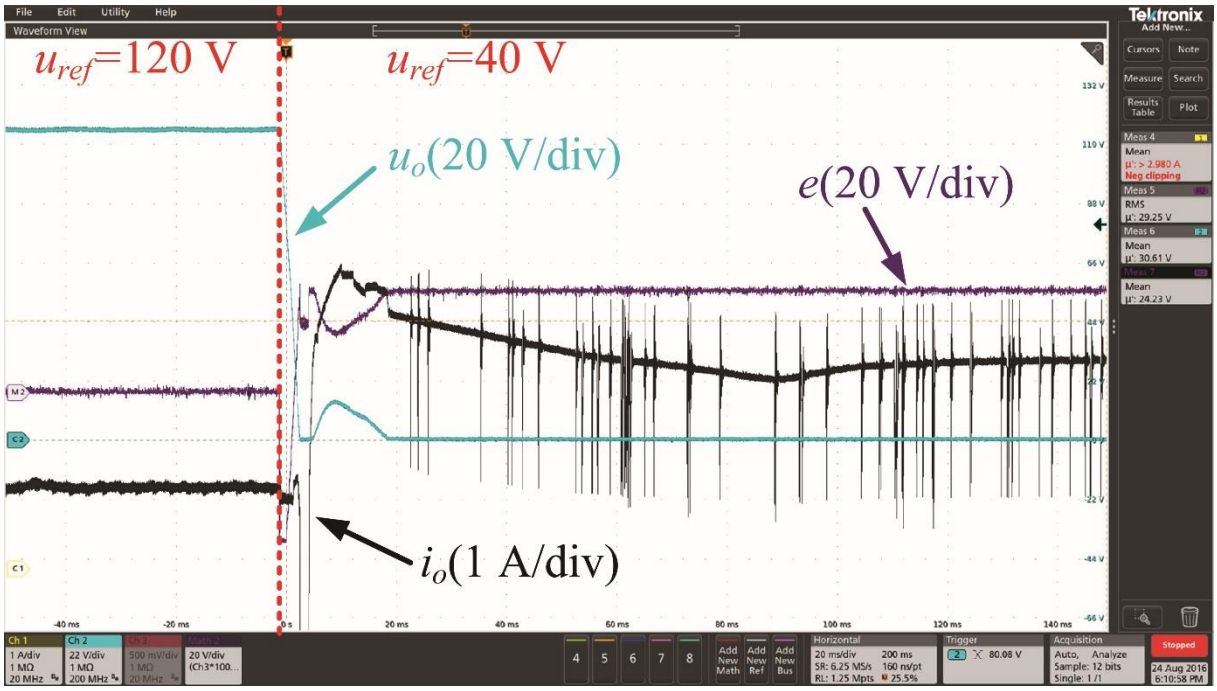
Figure 2-9 shows the DAB converter voltage responses when feeding a 120 W CPL. The CPL is emulated by using a programmable DC load. The reference voltage u_{ref} changes from 120 V to 40 V, and the UDE controller with disturbance compensation achieves the voltage tracking within 10 ms, which means the closed-loop performance of the UDE controlled DAB converter is matched with the designed reference system. The maximum tracking error during the transient response is also low. However, when the disturbance compensation is not enabled, i.e., $G_f(z)$=0, the system is unstable. Based on Figure 2-6, without disturbance compensation, the output impedance of the DAB converter is determined by the system uncertainty, especially in the low-frequency region. Based on the stability condition shown in (2-23), a low output impedance is always desired, as it could improve both the voltage tracking performance and system stability when feeding a CPL. Figure 2-9(c) shows that the PI controller could also maintain the system

stability and achieve the voltage tracking. However, the tracking overshoot of the PI controller is much higher than that of the UDE controller, which is almost not existed.

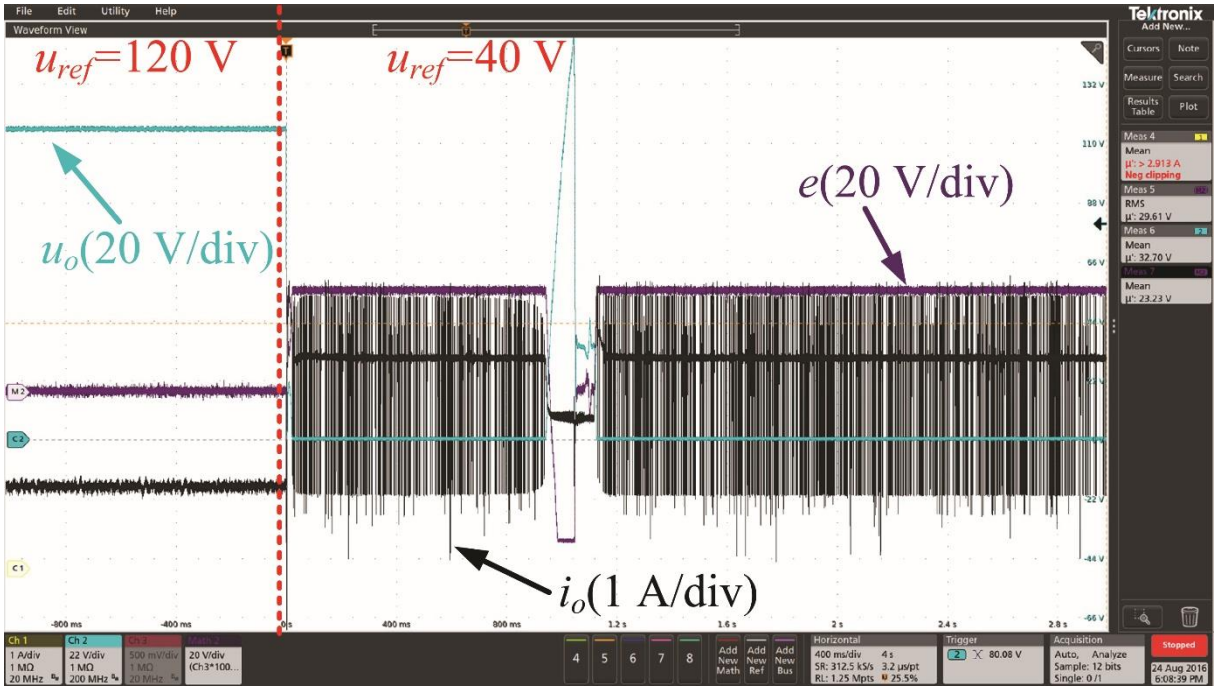
Figure 2-10 shows the system voltage responses when feeding the same CPL. However, the circuit parameters used in the controller design have 30% error, i.e., L=56 μH and C=136.5 μF rather than the values shown in Table 2-1 are used in the UDE and PI controllers design. It can be seen that the UDE controller with disturbance compensation maintains excellent tracking performance even under the high system uncertainty, and the closed-loop performance is still matched with the designed reference system. However, similar to the accurate parameters test, without $G_f(z)$, the UDE control law cannot maintain the system stability due to the large output impedance. Similarly, the PI controller is also unstable under the high system parameters uncertainty. In practical applications, not only the circuit parameters uncertainties, but also the deadtime uncertainty can affect the converter output performance.


u_{ref}=120 V
u_{ref}=40 V
u_o(20 V/div)
10 ms
e(20 V/div)
18 V
i_o(1 A/div)

(a)


u_{ref}=120 V
u_{ref}=40 V
u_o(20 V/div)
e(20 V/div)
i_o(1 A/div)

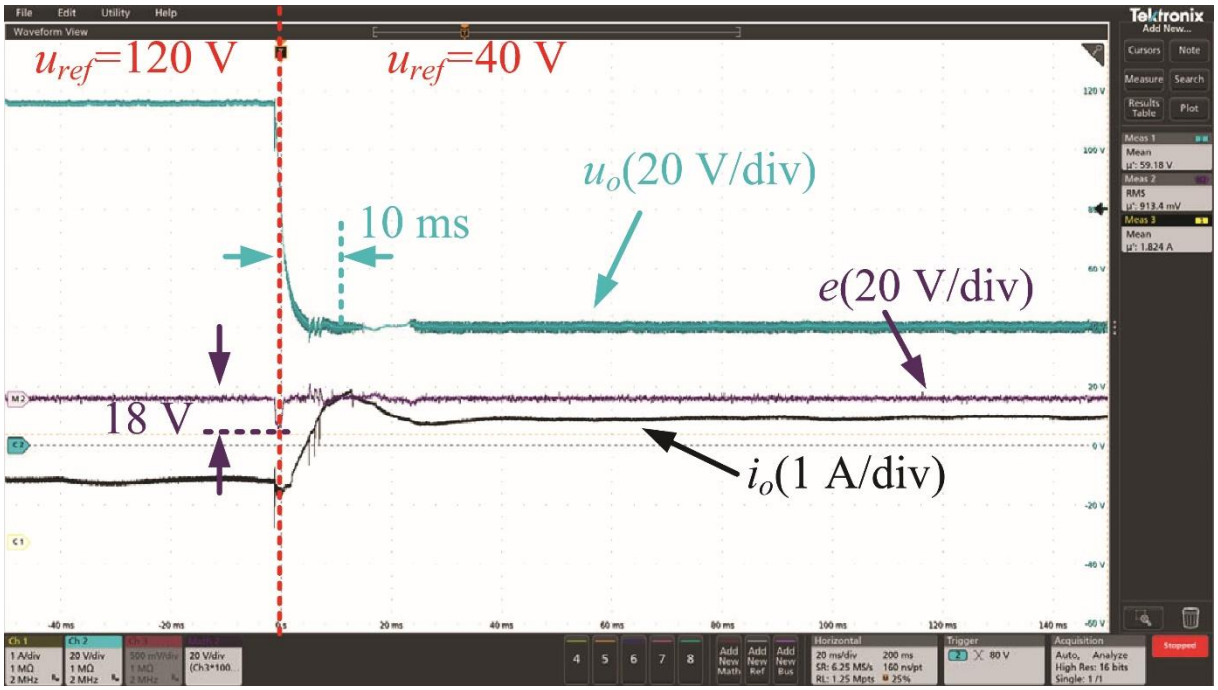
(b)



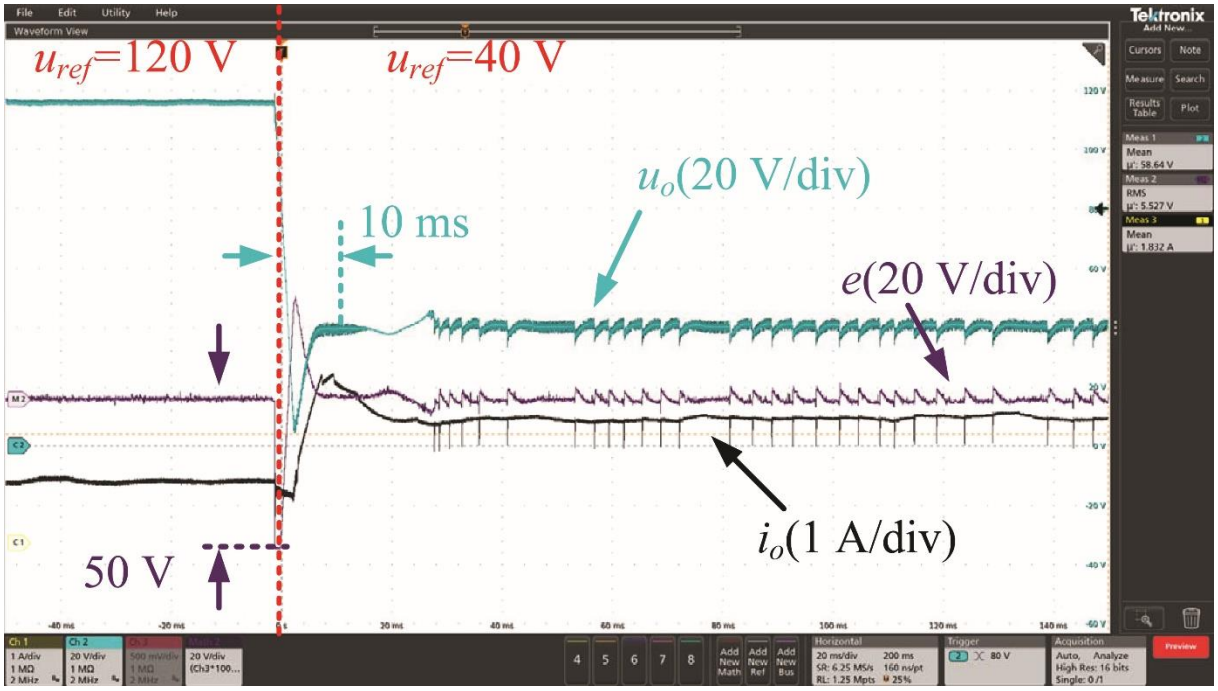
(c)

Figure 2-10. Transient responses of the DAB converter when feeding a 120 W CPL with different controllers and 30% error in L and C: (a) UDE controller with 400 Hz bandwidth $G_f(z)$ (b) UDE controller with $G_f(z)$=0, and (c) PI controller.

Figure 2-11 shows the system responses under the same 120 W CPL, but the converter deadtime has been doubled, i.e., 4 μs deadtime was used during the test. It can be seen that compared with the PI controller, the proposed UDE controller can still perform excellent tracking performance, while the PI controller almost reach the stability limitation due to the deadtime uncertainty and large overshoot as well as high voltage ripples occur in the voltage response. Thus, the proposed scheme could effectively improve the robustness and voltage tracking performance of the DAB converter.



(a)



(b)

Figure 2-11. Transient responses of the DAB converter when feeding a 120 W CPL with a doubled deadtime: (a) the proposed UDE controller and (b) PI controller.

2.5 Conclusion

In this chapter, a UDE based robust voltage control scheme is proposed for DAB converters to improve the output voltage tracking performance and system robustness against internal and external disturbances and uncertainties. To simplify the controller design and improve the controller compatibility, a universal DAB converter model is proposed based on the converter output current. Then the UDE based voltage controller is proposed using the proposed universal DAB model. The one-step delay caused by the computation in digital controller is considered, and the rigorous stability analysis is presented. To enhance the robustness to the load dynamics, especially when feeding the CPLs, the output impedance of the UDE controlled DAB converter is presented for the first time. Based on the stability requirements, the design of the UDE based voltage controller could be accomplished by selecting three parameters: the closed-loop bandwidth α, the error convergence rate k, and the disturbance rejection bandwidth β, which have strong physical significance. A series of comparative experiment studies have been conducted and the results are presented to validate the effectiveness of the proposed scheme.

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CHAPTER 3

HIGH-FREQUENCY SIGNAL INJECTION BASED OUTPUT CAPACITANCE ESTIMATION FOR DAB CONVERTERS

3.1 Introduction

DAB converters have been widely used in various applications due to their unique features, including bidirectional power transferring capability, high power density, and high efficiency [1]. In the DAB converters, the output capacitor is necessary to suppress the switching ripples, provide energy for transient operations, and balance the instantaneous power difference between the DAB converter and the load [2]. Thus, the design of the DAB converter must consider the selection of the dc-link capacitor. Moreover, the dc-link capacitor also plays an important role in the design of the DAB converter controller, since the capacitance is vital in the small-signal model of the DAB converter [3], [4]. Especially, for the two-stage grid-tied inverter system, the output capacitor of the DAB converter will also serve as the input dc-link capacitor for the grid-tied inverter, and thus, the overall system reliability and control performance will depend on the dc-link capacitor. However, in practice, the capacitance may vary from its nominal value due to component tolerance, thermal stress, and capacitor degradation [2], [5], [6]. Thus, the converter reliability and control performance will be deteriorated. With regard to this, it is important to estimate and monitor the actual output capacitance of the DAB converters in real-time, which can present the health status of the dc-link capacitor.

In order to estimate the dc-link capacitance and predict the reliability of the converter system, [7] has proposed a power-based dc-link capacitance estimation scheme for the interior permanent magnet synchronous motor drives. By measuring the input and output power of the traction

inverter, the capacitance of the inverter system could be estimated. However, the power-based estimation scheme requires that the traction inverter must generate a certain power on the motor, otherwise, the estimation accuracy will be impacted. A recursive-least-squares (RLS) based parameter estimation scheme has been proposed in [8] for dc-dc converters. By injecting a pseudo random binary sequence (PRBS) signal into the converter, the RLS scheme could estimate the circuit parameters based on the converter response. However, the computational complexity of the RLS scheme is high, which may limit the real-world application. An observer-based capacitance estimation scheme is proposed in [9] for a buck converter. However, the accuracy of the observer-based estimation scheme is not satisfactory, whose estimation error is about 5%, and thus, the estimated capacitance is not accurate enough for the remaining lifetime estimation for the dc-link capacitor [10]. In [11] and [12], the modeling of the film capacitor and the aluminum electrolytic capacitor has been discussed in detail, while an offline capacitance estimation is proposed. However, the offline estimation scheme cannot provide a real-time estimate of the dc-link capacitance. A support vector regression (SVR) based capacitance estimation scheme is proposed for a back-to-back converter in [13], while the high computation complexity of the SVR method may also limit its implementation in real time applications. In [14] and [15], the RLS-based capacitance estimation scheme has been implemented on a Buck converter.

In this chapter, an HF signal injection based capacitance estimation scheme has been proposed for the DAB converters, which can provide an accurate online estimate of the actual output capacitance. By injecting an HF signal into the DAB converter output current command, the output voltage and current of the DAB converter will be excited. After demodulating the excited voltage and current, the proposed estimation scheme could estimate the actual dc-link capacitance. The following of this chapter is organized as follows: First, the dynamic model of the DAB converter

is reviewed. Then proposed estimation scheme is presented. The deadtime effect has been analyzed and compensated to enhance the estimation accuracy. Both hardware-in-the-loop (HIL) studies and experimental studies have been performed to validate the effectiveness of the proposed scheme.

3.2 Modeling of the DAB Converter and DC-Link Capacitor

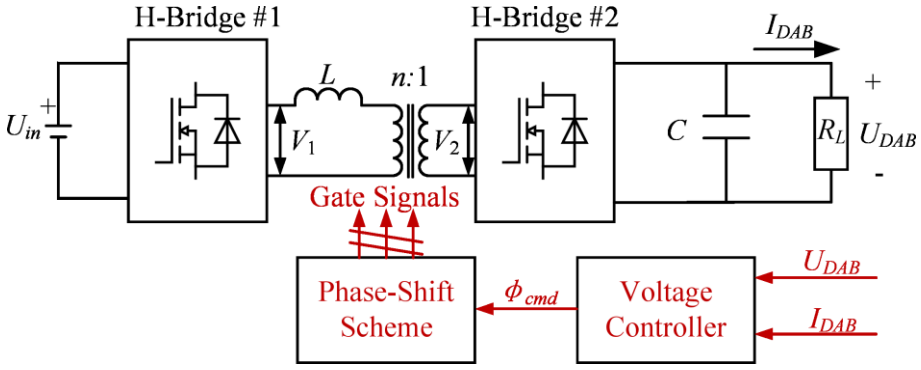
As discussed in Chapter 2, Figure 3-1(a) shows the schematic of a single-phase DAB converter, where U_{in} is the input voltage, V_1 is the output voltage of the first H-bridge converter, V_2 is the output voltage of the second H-bridge converter, L is the leakage inductance of the transformer, n is the turns ratio of the transformer, C is the output capacitor, U_{DAB} is the output voltage, and I_{DAB} is the load current. In this work, the single-phase-shift (SPS) modulation scheme is used to control the DAB converter due to its simplicity [1]. Figure 3-1 (b) shows the SPS modulation scheme, where F_s is the switching frequency of the DAB converter, T_s=1/F_s is the switching period, and ϕ_{cmd} is the phase-shift angle. The duty cycle for both H-bridge converters is fixed at 50%, and the phase-shift angle ϕ_{cmd} is applied between the output voltages V_1 and V_2. Under the SPS modulation scheme, the output current of the DAB converter can be written as

$$I_{cmd} = \frac{nU_{in}\phi_{cmd}\left(\pi - \phi_{cmd}\right)}{2\pi^2 F_s L} \tag{3-1}$$

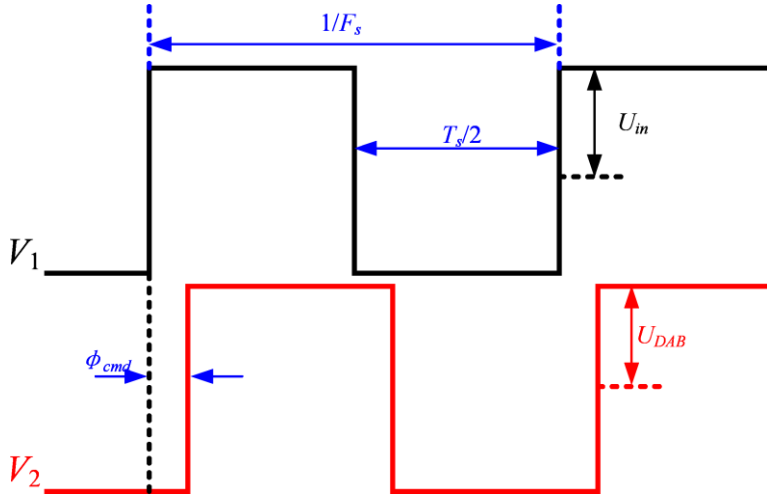
where I_{cmd} is the output current of the DAB converter. It should be noticed that the output current I_{cmd} contains two parts: load current I_{DAB} and the capacitor current I_c, i.e., $I_{cmd} = I_{DAB} + I_c$, as Figure 3-1(c) shows. Based on (1), for a certain output current I_{cmd}, the ideal phase-shift angle should satisfy [4]

$$\phi_{cmd} = \frac{\pi - \pi\sqrt{1 - 8F_s L I_{cmd} / (nU_{in})}}{2} \tag{3-2}$$

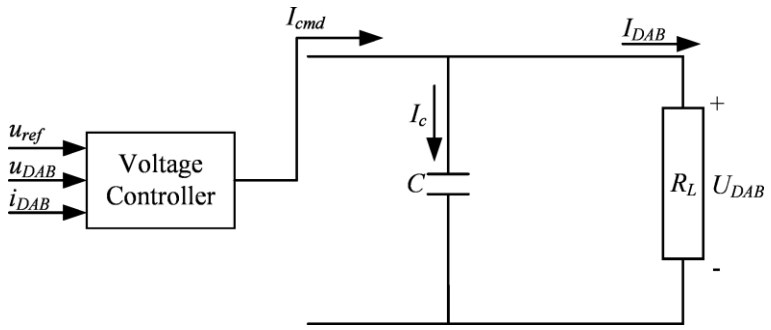
It can be seen from (3-1) and (3-2) that by adjusting the phase-shift angle, the output current of the DAB converter can be controlled. Especially, the capacitor current also satisfies $I_c = C\frac{dU_{DAB}}{dt}$, which means that the capacitor current can be used to estimate the dc-link capacitance.



(a)



(b)



(c)

Figure 3-1. (a) Single-phase DAB converter, (b) SPS modulation scheme, and (c) equivalent model of the DAB converter.

However, the characteristics of an actual capacitor must be considered in the design of the estimation scheme. In practice, capacitors contain parasitic inductance and resistance. Figure 3-2(a) shows the equivalent circuit of an actual capacitor *C*, where ESL is the equivalent-series-inductance, and ESR is the equivalent-series-resistance of the capacitor. Based on Figure 3-2(a), the dynamic model of an actual capacitor can be written as

$$C_{actual}(s) = \frac{1}{sC} + R_{ESR} + sL_{ESL} \tag{3-3}$$

Based on (3-3), the frequency response of the capacitor can be plotted in Figure 3-2(b). It can be seen from the figure that the ideal capacitance model, i.e., $\frac{1}{sC}$, can represent the actual capacitor when the frequency is lower than the self-resonant frequency of the capacitor. In practice, the controller bandwidth is much lower than the self-resonant frequency of the capacitor. Thus, the ideal capacitor model could be used in the design of the capacitance estimation scheme without significant accuracy loss.

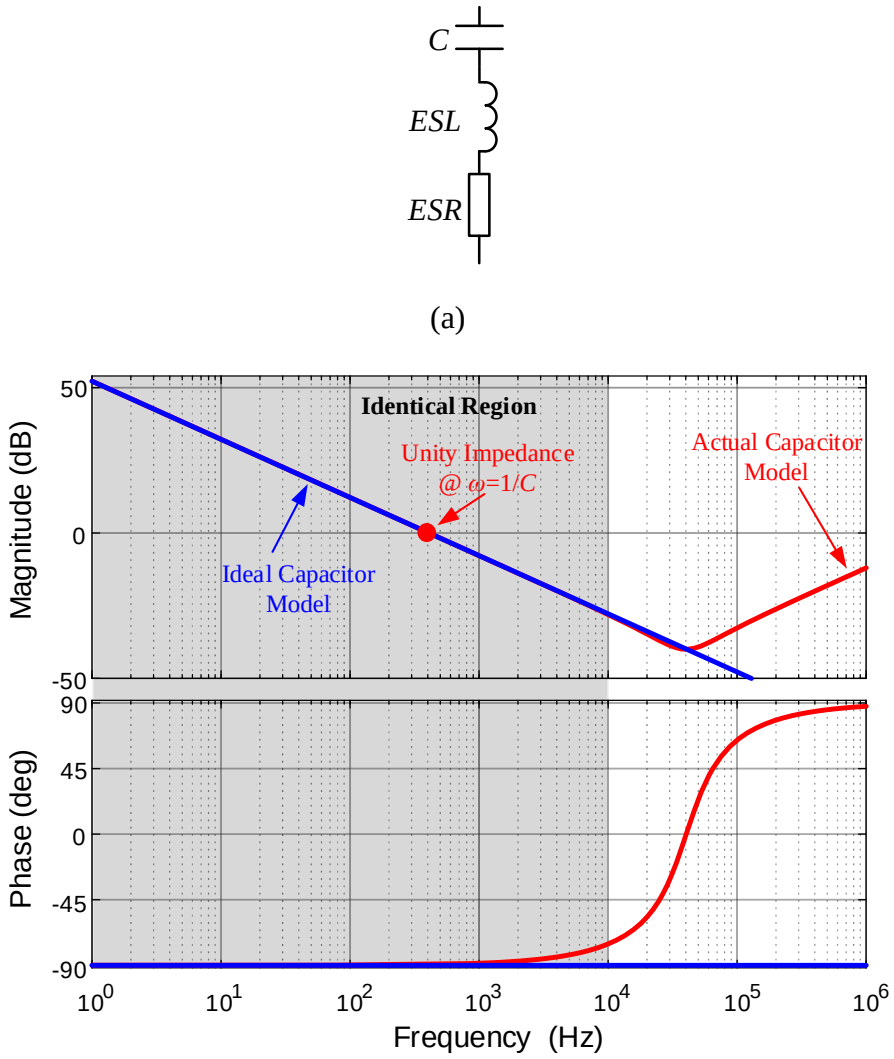


Figure 3-2. (a) Actual capacitor model and (b) frequency response of the actual capacitor and ideal capacitor.

3.3 High-Frequency Signal Injection Based Capacitance Estimation Scheme

3.3.1 Estimation Scheme

As mentioned earlier, the output current of the DAB converter I_{cmd} includes the capacitor current I_c and load current I_{DAB}. In practice, the capacitor current usually cannot be directly

measured due to hardware limitations. Instead, the capacitor current could be estimated based on the command current and the measurable load current. Thus, by injecting an HF signal into I_{cmd}, it is possible to extract the capacitance information based on the excited output voltage U_{DAB} and load current I_{DAB}.

Figure 3-3(a) shows the system diagram of the proposed scheme, where an HF signal $A\sin(\omega t)$ is injected into the DAB converter output current I_{cmd}, and I_{cmd0} is the output of the existing DAB converter controller to satisfy the power control requirement. With the HF injection signal, both the DAB converter output voltage U_{DAB} and the capacitor current I_c will be excited and the HF responses on the voltage and current can be used to estimate the dc-link capacitance. It can be seen that the proposed capacitance estimation scheme can be easily integrated with an existing DAB controller. Figure 3-3(b) shows the detailed diagram of the proposed scheme, where LPF is the low-pass filter, HPF is the high-pass filter, and the output of the proposed scheme is C^2, i.e., the square of the output capacitance. Thus, the proposed scheme could provide the online estimate of the actual dc-link capacitance.

Based on Figure 3-1, the DAB converter output current after the HF signal injection satisfies

$$I_{cmd,0} + A\sin(\omega t) = C\frac{dU_{DAB}}{dt} + I_{DAB} \tag{3-4}$$

With the injected signal, the converter output voltage will be excited. Supposing the frequency ω is much higher than the frequency of I_{cmd0}, then the HF voltage response can be written as

$$U_{DAB,\mathrm{hf}} = M\sin(\omega t + \phi_1) \tag{3-5}$$

where M and ϕ_1 are the amplitude and phase angle of the excited HF voltage response respectively. Similarly, based on (3-4) and (3-5), the HF DAB converter output current satisfies

$$\begin{aligned} A\sin(\omega t) - I_{DAB,hf} &= C\frac{dU_{DAB,hf}}{dt} \\ &= CM\omega\cos(\omega t + \phi_1) \end{aligned} \tag{3-6}$$

where $I_{DAB,hf}$ is the HF response of the load current. Supposing the HPF shown in Figure 3-2(b) is well-designed, which can effectively attenuate the low-frequency (LF) component and extract the HF response. Thus, based on (3-6) and Figure 3-3, the HF component of the current difference between I_{cmd} and I_{DAB}, i.e., $I_{diff,hf}$, can be written as

$$\begin{aligned} I_{diff,hf} &= A\sin(\omega t) - I_{DAB,hf} \\ &= CM\omega\cos(\omega t + \phi_1) \end{aligned} \tag{3-7}$$

It can be seen from (3-7) that the frequency of current $I_{diff,hf}$, is the same as the injection frequency. Meanwhile, the amplitude of $I_{diff,hf}$ contains the information of the actual dc-link capacitance. In order to extract the capacitance from the response current, the HF current difference $I_{diff,hf}$ is fed into two demodulation blocks. In the cosine branch, the demodulation result can be written as

$$I_{diff,hf} \times \cos(\omega t) = \underbrace{\frac{CM\omega\cos(\phi_1)}{2}}_{\text{LF component}} + \underbrace{\frac{CM\omega\cos(2\omega t + \phi_1)}{2}}_{\text{Double-Frequency Component}} \tag{3-8}$$

Similarly, the demodulation result in the sine branch can be written as

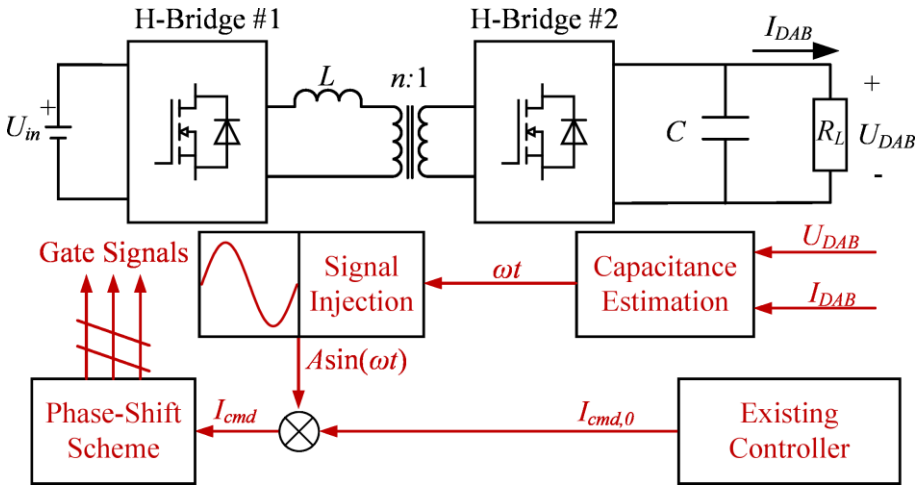
$$I_{diff,hf} \times \sin(\omega t) = \underbrace{\frac{CM\omega \sin(-\phi_1)}{2}}_{\text{LF component}} + \underbrace{\frac{CM\omega \sin(2\omega t + \phi_1)}{2}}_{\text{Double-Frequency Component}} \tag{3-9}$$

Supposing the LPF is also properly designed, which can effectively attenuate the double-frequency component and extract the LF component from the demodulation results. Thus, the outputs of the LPFs can be written as

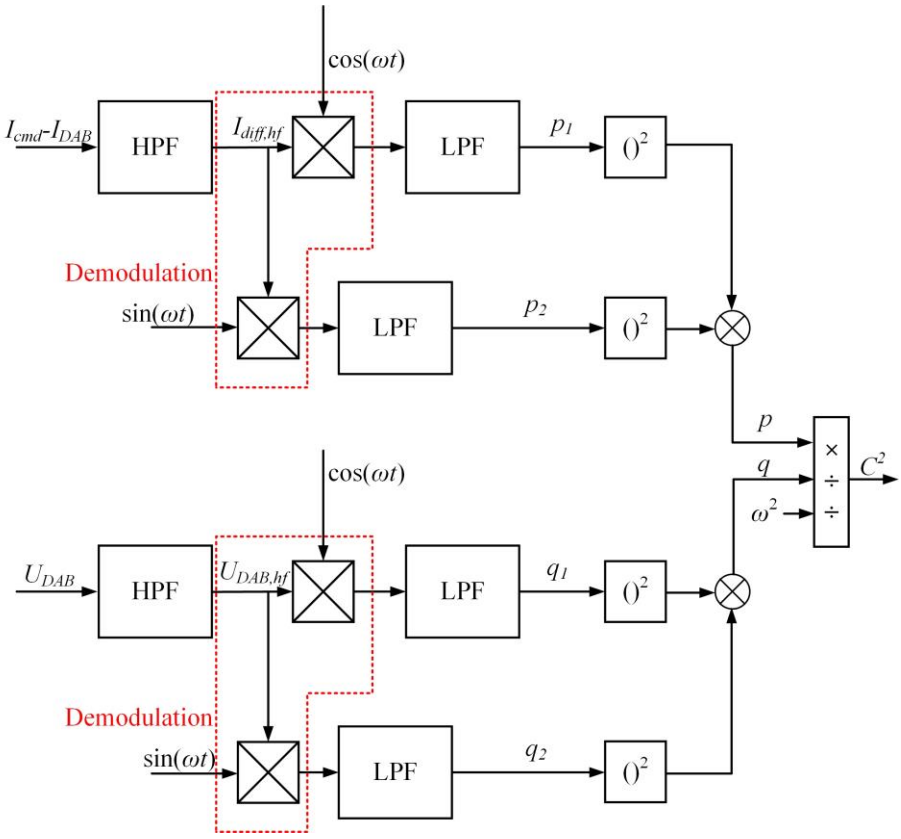
$$\begin{cases} p_1 = 0.5CM\omega \cos(\phi_1) \\ p_2 = -0.5CM\omega \sin(\phi_1) \end{cases} \tag{3-10}$$

and the signal p can be written as

$$\begin{aligned} p &= p_1^2 + p_2^2 \\ &= 0.25C^2M^2\omega^2 \end{aligned} \tag{3-11}$$



(a)



(b)

Figure 3-3. (a) system diagram of the proposed scheme, and (b) detailed diagram of the proposed scheme.

It can be seen from (3-11) that the signal p contains the output capacitance information. However, the amplitude of the HF voltage response, i.e., M, is still unknown. Thus, a similar demodulation operation can be applied on the DAB converter output voltage to extract the amplitude of the HF voltage response. The demodulation results of the DAB converter HF response voltage can be written as

$$U_{DAB,hf} \times \cos(\omega t) = \underbrace{\frac{M\cos(\phi_1)}{2}}_{\text{LF component}} + \underbrace{\frac{M\cos(2\omega t+\phi_1)}{2}}_{\text{Double-Frequency Component}} \tag{3-12}$$

and

$$U_{DAB,hf} \times \sin(\omega t) = \underbrace{\frac{M \sin(-\phi_1)}{2}}_{\text{LF component}} + \underbrace{\frac{M \sin(2\omega t + \phi_1)}{2}}_{\text{Double-Frequency Component}} \tag{3-13}$$

To extract the LF components from the demodulation results, LPFs are utilized, and the results can be written as

$$\begin{cases} q_1 = 0.5M \sin(\phi_1) \\ q_2 = 0.5M \cos(\phi_1) \end{cases} \tag{3-14}$$

where q_1 and q_2 are the LPF outputs of the cosine branch and sine branch respectively. The final output of the UDAB demodulation can be written as

$$q = 0.25M^2 \tag{3-15}$$

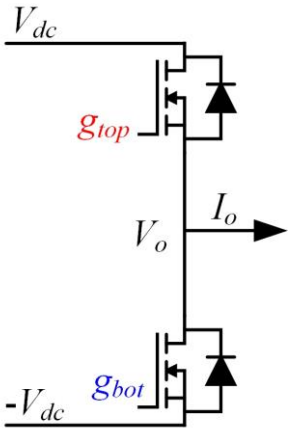
Based on (3-11) and (3-15), the online estimate of the actual output capacitance can be written as

$$C = \sqrt{\frac{p}{q\omega^2}} \tag{3-16}$$

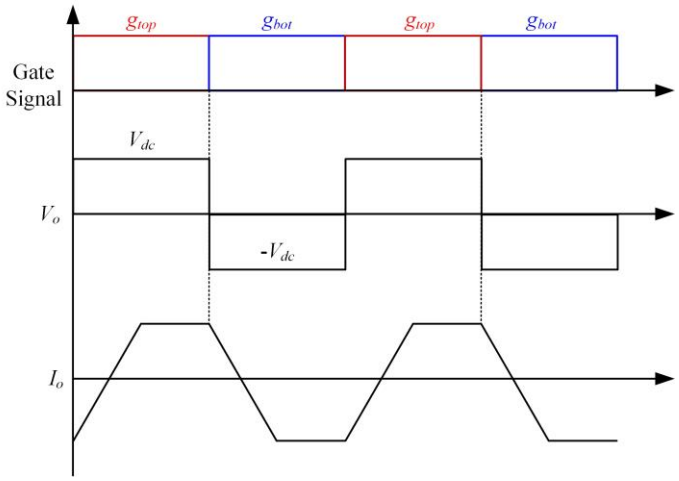
3.3.2 Deadtime Effect

In practice, a blanking time is usually inserted into the gate signals for the top switch and bottom switch in a half-bridge configuration to avoid the shoot-through failure. Figure 3-4 shows the ideal gate signals for the half-bridge. It can be seen that the gate signals are completely complimentary and the current flows through the MOSFETs all the time. Figure 3-5 shows the actual gate signals for the half-bridge considering the deadtime. During the deadtime, the current

will flow through the diodes as both the top MOSFET and bottom MOSFET are turned off. Thus, the output voltage of the half-bridge during the deadtime depends on the current direction. If the half-bridge is working in the ZVS mode, i.e., the load current flowing through the bode diode or external anti-parallel diode of the MOSFET before it is turned on, the output voltage of the half-bridge will be the same as that in the case without deadtime. Nevertheless, if the half-bridge is working in the non-ZVS mode, then the output voltage of the half-bridge will be distorted due to the deadtime. Actually, it can be seen from Figure 3-5 that there is a phase-shift between the ideal output voltage and the actual output voltage of the half-bridge if the half-bridge is working in the non-ZVS mode. The additional phase-shift caused by deadtime will impact the accuracy of the equivalent output current model of the DAB converter shown in (3-1).

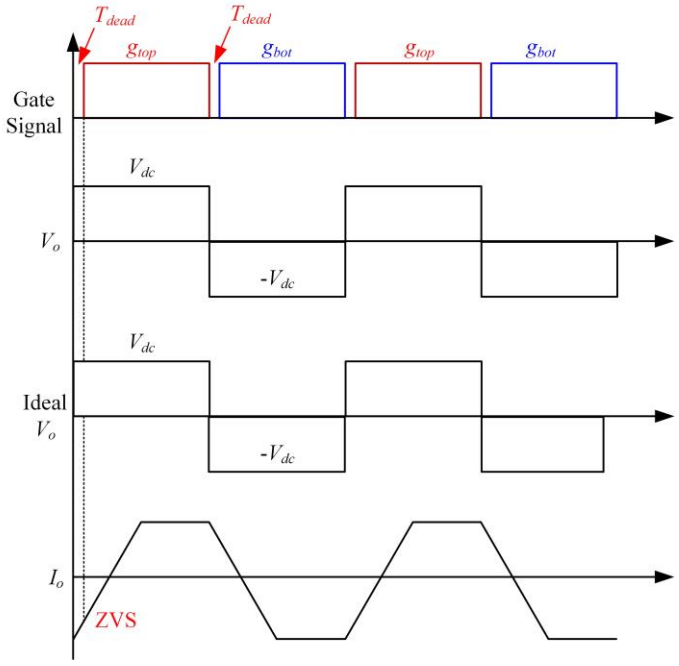


(a)

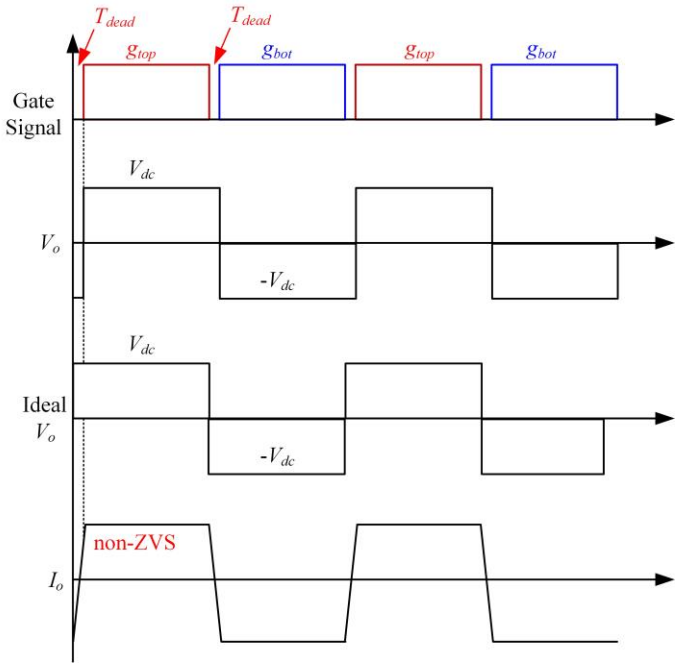


(b)

Figure 3-4. (a) Schematic of a half-bridge and (b) ideal gate signals, output voltage, and output current of the half-bridge.



(a)



(b)

Figure 3-5. Gate signals, output voltage, and output current of the half-bridge under (a) ZVS condition and (b) non-ZVS condition.

In the proposed capacitance estimation scheme, the HF current is injected to the DAB converter through phase-shift control. In other words, the HF current is generated by actively adjusting the phase-shift angle. However, the deadtime effect will deteriorate the accuracy of the HF signal injection as the actual phase-shift angle is no longer the same as the desired phase-shift angle. In other words, although the ideal HF injected signal is $A\sin(\omega t)$, the actual HF component of the DAB converter output current might be different from $A\sin(\omega t)$ due to the deadtime, and the accuracy of the capacitance estimation will be deteriorated. As discussed earlier, the phase-shift caused by deadtime is zero if the half-bridge is working in the ZVS mode. In the non-ZVS mode, the phase-shift angle distortion caused by deadtime can be calculated as

$$\phi_{deadtime} = 2\pi T_{dead} F_{sw} \tag{3-17}$$

Thus, if the working condition of the primary side H-bridge is the same as that of the secondary side H-bridge, i.e., both sides are working in the ZVS mode or non-ZVS mode, the deadtime will not impact the estimation performance. However, if the working conditions of the primary side and secondary side are not the same, the distorted phase-shift angle caused by deadtime must be compensated.

Since the phase-shift distortion caused by the deadtime depends on the ZVS condition of the DAB converter, thus, a working condition based deadtime compensation scheme can be designed as

$$\phi_{comp} = \begin{cases} 2\pi T_{dead} F_{sw}, & \text{Primary-side non-ZVS and Secondary-side ZVS} \\ 0, & \text{Primary-side and Secondary-side have the same working condition} \\ -2\pi T_{dead} F_{sw}, & \text{Primary-side ZVS and Secondary-side non-ZVS} \end{cases} \tag{3-18}$$

Figure 3-6 shows the deadtime compensation diagram. Based on the DAB converter input voltage, output voltage, and original phase-shift command, the deadtime compensation scheme could estimate the soft-switching conditions of both the primary-side and secondary-side. Supposing the ratio between the input voltage and output voltage is M_V, i.e.,

$$M_V = \frac{nU_{DAB}}{U_{in}} \tag{3-19}$$

For the primary-side, the ZVS condition is [1]

$$\frac{\phi_{cmd}}{\pi} > \frac{M_V - 1}{2M_V} \tag{3-20}$$

Similarly, the ZVS condition for the secondary-side can be written as

$$\frac{\phi_{cmd}}{\pi} > \frac{1 - M_V}{2} \tag{3-21}$$

As an example, Figure 3-7 shows the ZVS region of both the primary-side and secondary-side under different voltage ratio and phase-shift angle.

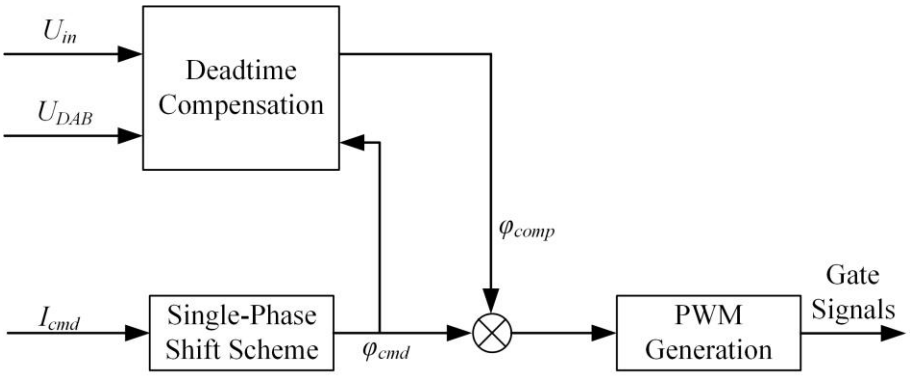


Figure 3-6. Proposed deadtime compensation scheme.

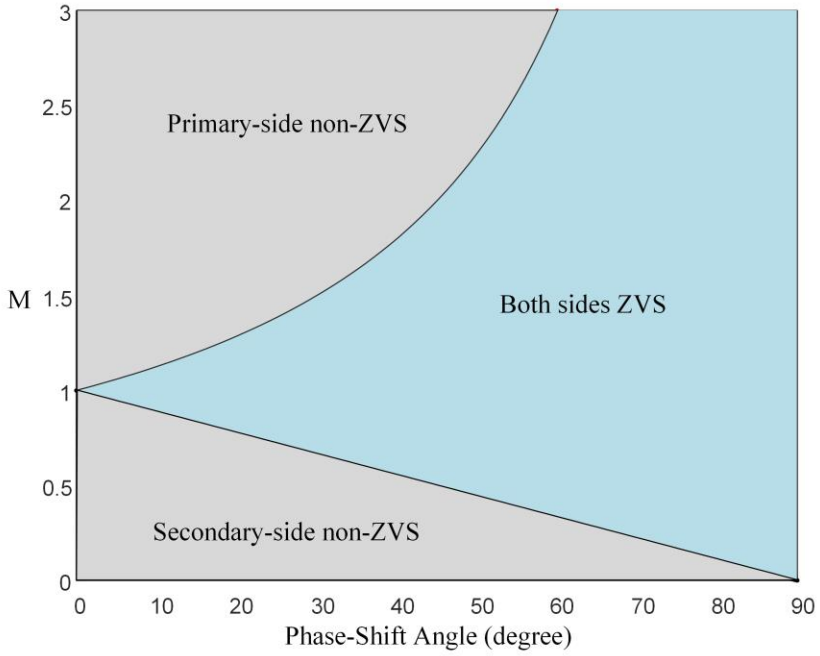


Figure 3-7. ZVS region of the DAB converter.

Thus, based on the ZVS conditions (3-20) and (3-21), and the deadtime compensation scheme (3-18), the deadtime effect of the DAB converter could be mitigated and the capacitance estimation accuracy could be enhanced.

3.4 HIL and Experimental Studies

TABLE 3-1 HIL Simulation Parameters

Parameter	Value	Parameter	Value
Input Voltage U_{in}	400 V	Output Voltage U_{DAB}	200 V
Load Current	100 A	Output Capacitor C	600 μF
Amplitude of Injection Signal	5 A	Frequency of Injection Signal	500 Hz
Switching Frequency	10 kHz	Controller Sampling Frequency	10 kHz

In order to validate the effectiveness of the proposed scheme, HIL simulation studies have been conducted on a Typhoon HIL402 HIL simulator. The converter and controller parameters are listed in Table 3-1. The proposed scheme is implemented on the TI TMS320F28335 DSP in the HIL simulation. The bandwidths of the HPF and LPF are set as 100 Hz and 10 Hz respectively. Figure 3-8 shows the HIL simulation result. It can be seen that the proposed scheme can provide an accurate online estimation of the DAB converter output capacitance within 80 ms.

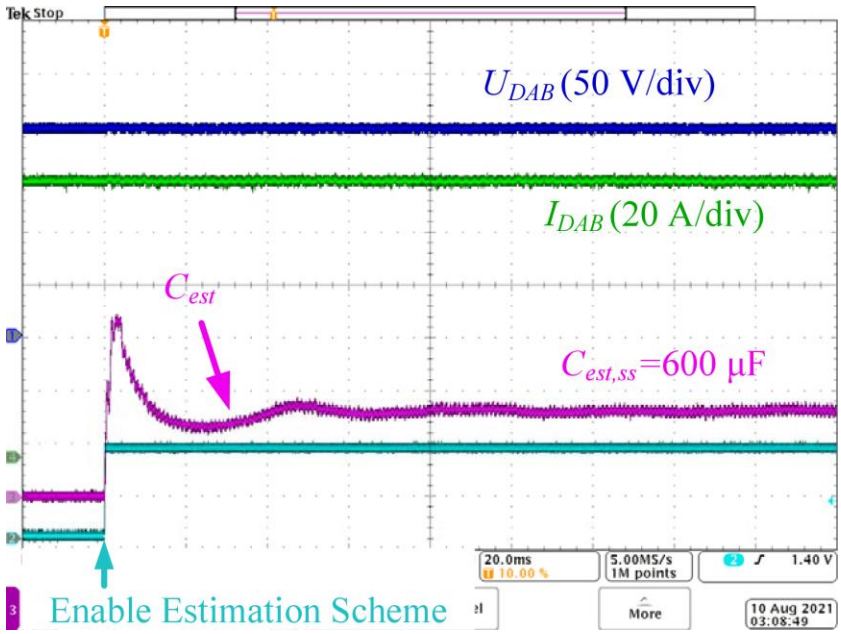


Figure 3-8. HIL simulation result.

TABLE 3-2 Experiment Parameters

Parameter	Value	Parameter	Value
Input Voltage U_{in}	100 V	Output Voltage U_{DAB}	50 V
Load Current	10 A	Output Capacitor C	390 μF
Amplitude of Injection Signal	1 A	Frequency of Injection Signal	500 Hz
Switching Frequency	20 kHz	Controller Sampling Frequency	20 kHz

Besides, a single-phase DAB converter prototype has been built to further demonstrate the performance of the proposed estimation scheme, and Figure 3-9 shows the experimental setup. Table 3-2 summarizes the converter and controller parameters that are used in the experiment. The proposed scheme is implemented on the TI TMS320F28379 DSP in the experiment. The deadtime

of the DAB converter is set as 2 μs and the proposed deadtime compensation scheme is implemented to enhance the estimation accuracy. The bandwidths of the HPF and LPF are set as 100 Hz and 10 Hz respectively. Figure 3-10 shows the experimental result. Similar to the results of the HIL simulation, the proposed scheme can provide an accurate estimate of the dc-link capacitance, and the estimation error is only about 2%. Meanwhile, the voltage ripple caused by the HF injection is also acceptable, which is only about 5% of the nominal output voltage. Both the HIL test and experiment test have demonstrated the effectiveness of the proposed scheme, and an accurate dc-link capacitance can be obtained through the proposed method.

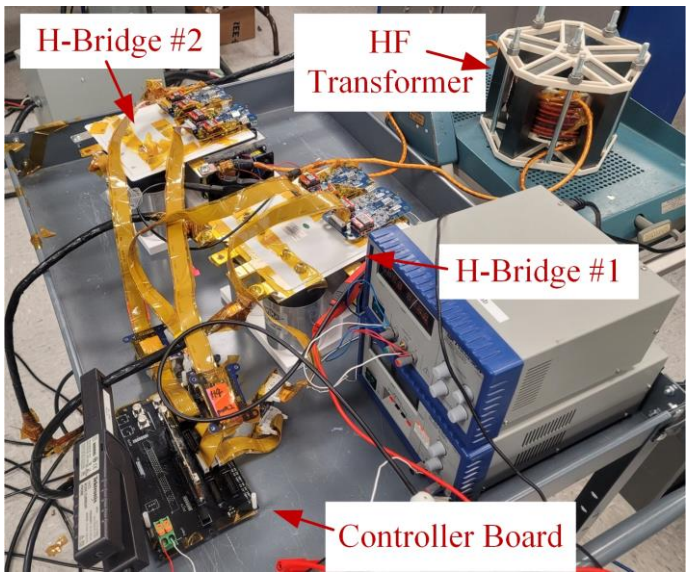


Figure 3-9. Experimental setup.

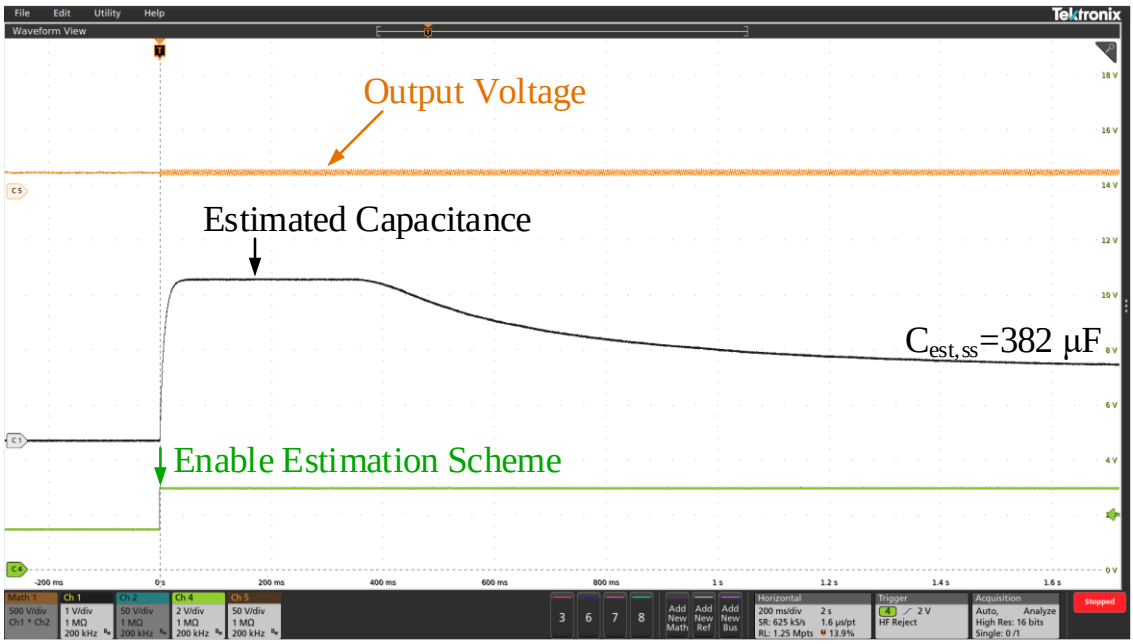


Figure 3-10. Experimental result.

3.5 Conclusions

In this chapter, an HF signal injection based capacitance estimation scheme has been proposed for DAB converters. By injecting an HF signal into the converter output current, the converter output voltage, as well as the load current, will be excited. Then the proposed estimation scheme will extract the HF responses from the excited output voltage and load currents. Through a properly designed demodulation process, the proposed scheme could provide an accurate online estimate of the DAB converter output capacitance based on the extracted HF responses. The deadtime effect of the DAB converter has been discussed. The deadtime of the DAB converter may lead to an additional phase-shift angle at certain working conditions, which will result in the inaccuracy of the DAB converter output current model and lead to the capacitance estimation error. A simple working condition based deadtime compensation scheme is proposed for the DAB converter, and the estimation accuracy can be further enhanced. A single-phase DAB converter has been built as

the test bench. Both the HIL simulation and experimental studies have been performed, and the results demonstrate the effectiveness of the proposed scheme.

3.6 References

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CHAPTER 4

AESC-BASED RESONANT FREQUENCY ESTIMATION OF LCL FILTERS

4.1 Introduction

Compared with the L-type filter, the LCL filter can provide better switching ripple attenuation with reduced filter volume, and thus, the LCL filter has been widely used in grid-tied inverter systems. However, the resonance of the LCL filter deteriorates the stability of the inverter system [1]. Moreover, the grid impedance variation can lead to the drift of the resonant frequency, which can turn the notch-filter-based active damping schemes ineffective and worsen the system robustness and stability [1], [2]. Thus, it is important to know the resonant frequency of the LCL filter online, which can benefit the design of adaptive active damping schemes and provide information of grid-side impedance [1]-[5].

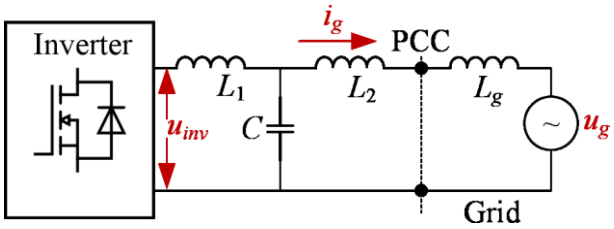
In [1], the resonance of the LCL filter is excited by tuning the controller first, and then the estimation of the resonant frequency can be achieved by using the discrete Fourier transform (DFT). Based on the estimated resonant frequency, the notch-filter-based active damping scheme can be adaptive [1] and the grid impedance can also be calculated [3]. In [6], the parameters of the LCL filter are estimated by a recursive prediction error (RPE) algorithm, while a binary sequence is injected into the inverter output voltage to excite the resonance of the filter. The recursive least square (RLS) scheme is combined with the RPE scheme to estimate the parameters of the LCL filter in [7], while the pseudorandom binary sequence is used as the excitation signal. However, both the DFT scheme and recursive algorithms suffer from the heavy computation burden, which may even affect the normal operation of the inverter controller.

In this chapter, an ESC based estimation scheme is proposed to estimate the resonant frequency of the LCL filter in real-time. The ESC scheme is a model-free optimization algorithm and has been adopted in various industrial applications [8]-[11]. In other words, the ESC algorithm can find the setpoint that extremizes the system output without known plant dynamics. Although the estimation of the LCL filter resonant frequency is not a conventional optimization problem, the online searching for the actual resonant frequency can follow the concept of the ESC scheme. By injecting an HF signal into the inverter output voltage, the proposed ESC based estimation scheme can seek the frequency that can maximize the excited response, which is the resonant frequency of the LCL filter [9]. However, in the conventional ESC scheme, the amplitude of the injection signal is constant. Considering the impedance characteristics of the LCL filter, i.e., the amplitude response of the LCL filter reaches its peak value at the resonant frequency, the selection of the injection signal amplitude must tradeoff between the dynamic response and inverter output current quality. A low amplitude injection scheme can maintain a satisfactory inverter output current quality while the dynamics of the estimation scheme would be slow. Nevertheless, a high amplitude injection signal may reduce the settling time while the inverter output current will be distorted. Thus, an adaptive ESC scheme is proposed to further enhance the estimation scheme both the dynamic performance as well as the inverter output current quality. Compared with the conventional ESC scheme, where a constant amplitude signal is injected, the proposed AESC scheme can actively adjust the amplitude of the injection signal, which can address the tradeoff between the scheme dynamic response and the inverter output current quality. The stability analysis of the AESC scheme is given, and experimental studies have been conducted to validate the effectiveness of the proposed scheme. Compared with the DFT scheme and recursive

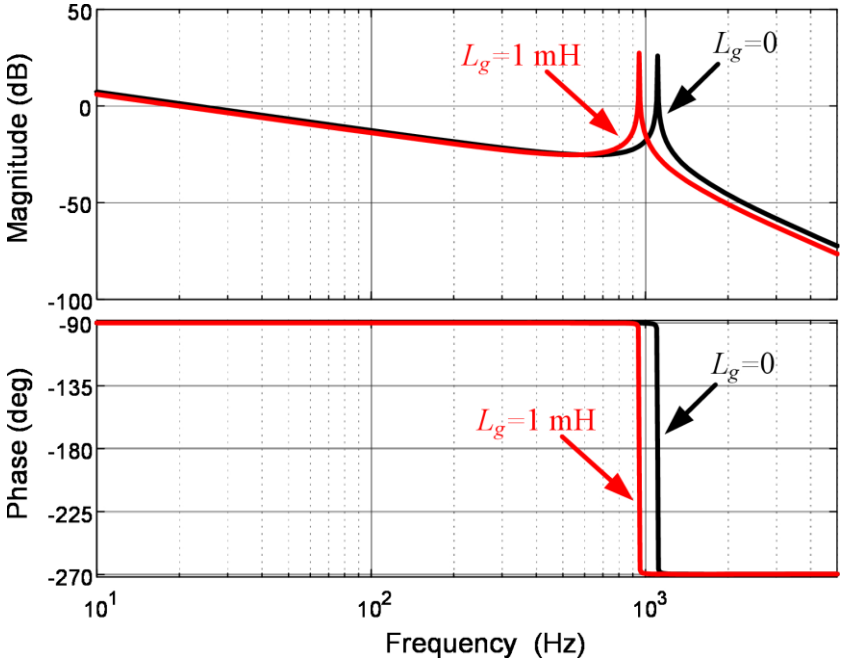
estimation schemes, the AESC scheme has much lower computational complexity, which can benefit the real-time realization and allow the implementation on low-cost microcontrollers.

4.2 Review of LCL Type Grid-Tied Inverter and ESC Scheme

4.2.1 Review of LCL Type Grid-Tied Inverter



(a)



(b)

Figure 4-1. (a) Grid-tied inverter with an LCL filter and (b) typical frequency response of the LCL filter.

Figure 4-1 shows a generic diagram of a single-phase LCL-type grid-tied inverter, where the inverter is connected to the point of common coupling (PCC) through the LCL filter, L_g is the grid-side impedance, u_{in} is the output voltage of the inverter, and u_g is the grid voltage. In this work, the grid impedance is considered as inductive. Besides, the number of resonances is supposed as one, i.e., there is only one resonant frequency in the grid-tied inverter system. The inverter-side current, capacitor current, and grid-side current of the grid-tied inverter can be written as

$$\begin{cases} i_L = \dfrac{\left(1+L_2Cs^2+L_gCs^2\right)u_{in}-u_g}{s\left[L_1\left(L_2+L_g\right)Cs^2+L_1+L_2+L_g\right]} \\ i_C = \dfrac{Cs\left(L_2su_{in}+L_gsu_{in}+L_1su_g\right)}{s\left[L_1\left(L_2+L_g\right)Cs^2+L_1+L_2+L_g\right]} \\ i_g = \dfrac{u_{in}-\left(1+L_1Cs^2\right)u_g}{s\left[L_1\left(L_2+L_g\right)Cs^2+L_1+L_2+L_g\right]} \end{cases} \tag{4-1}$$

It can be seen from (4-1) that the transfer function of those currents includes a resonant term, i.e, $\dfrac{1}{L_1\left(L_2+L_g\right)Cs^2+L_1+L_2+L_g}$. The resonant term will result in the resonance of the inverter output current, and the resonant frequency of the LCL filter is $\omega_{re}=\sqrt{\left(L_1+L_2+L_g\right)/L_1\left(L_2+L_g\right)C}$. In practice, the resonant of the LCL filter must be damped to enhance the stability and robustness of the grid-tied inverter system. However, it can be seen that the grid-side impedance, as well as the LCL parameters uncertainty, can lead to the resonant frequency drift. As an example, Figure 4-1(b) shows the frequency response of an LCL filter under different grid-side impedance, where L_1=5 mH, L_2=2.9 mH, and C=15 μF, and the resonant frequency is reduced from 1107 Hz to 960 Hz when the L_g is increased from 0 to 1 mH.

4.2.2 Review of ESC Scheme

Figure 4-2 shows a typical block diagram of the ESC scheme, where x is the system operating point and $f(x)$ is the cost function that should be minimized. An HF signal, $\sin(\omega t)$, is injected into the system, and the response of the cost function is sampled and multiplied with the injected signal to achieve the demodulation. The demodulation operation could transform the HF response as a low-frequency signal. Based on the demodulated signal, the integrator is used to seek the optimum operating point x_{op} that can minimize the cost function. In practice, additional filters might be required to extract the HF system response excited by the injection signal [8]. The implementation of the ESC scheme as the resonant frequency estimator will be further introduced in the following sections.

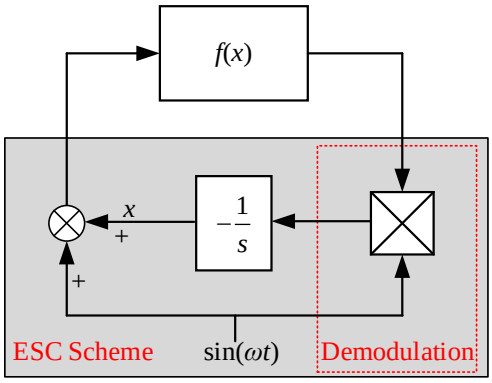


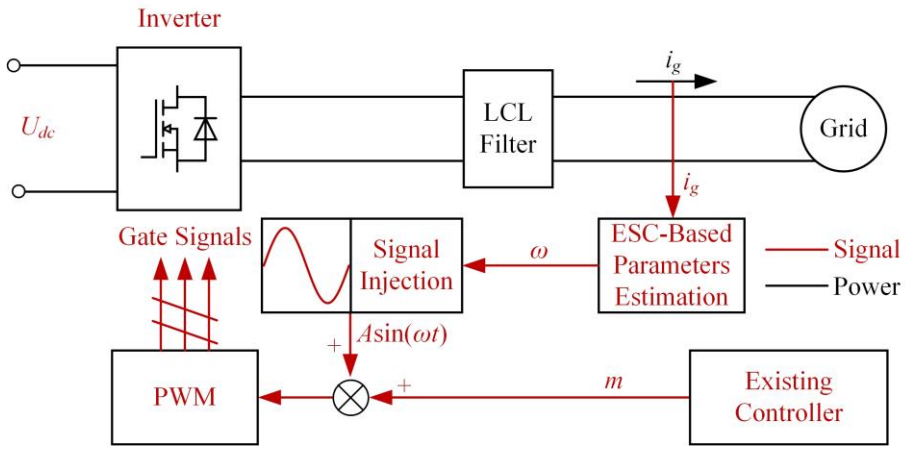
Figure 4-2. Typical control diagram of the ESC scheme.

4.3 ESC Based Resonant Frequency Estimation

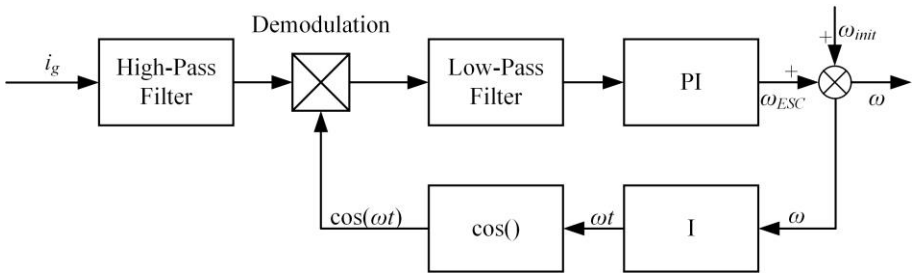
4.3.1 Design of ESC Based Resonant Frequency Estimation Scheme

Figure 4-3 shows the ESC based resonant frequency estimation scheme, where m is the modulation index, which is generated by the existing controller to achieve the nominal control,

$Asin(\omega t)$ is the injection signal, A is the amplitude of the injected signal, PI and I are the proportional-integral controller and integrator respectively, ω_{init} is the initial output of the ESC scheme, and ω is the online estimation of the resonant frequency. As Figure 4-3(a) shows, the proposed scheme can be easily integrated with an existing inverter controller and provide the online estimation of the resonant frequency. The grid-side current is measured for the ESC scheme, which usually is a necessary sampled variable for the existing controller, and thus, no additional sensors are required.



(a)



(b)

Figure 4-3. ESC based resonant frequency estimation scheme: (a) inverter system diagram and (b) ESC scheme.

Compared with the conventional ESC scheme shown in Figure 4-2, an additional high-pass filter is added to extract the system response under the HF excitation. Besides, the high-pass filter could also attenuate the fundament current, which may impact the estimation accuracy. Based on (4-1), the grid-side current response under the HF injected signal can be written as

$$i_{g,hf}(\omega) = A\left|G_{LCL}\right|_{\omega} \sin\left(\omega t + \phi\right) \tag{4-2}$$

where $G_{LCL}(s) = \dfrac{\left(1+L_2Cs^2\right)u_{in} - u_g}{s\left(L_1L_2Cs^2 + L_1 + L_2\right)}$ is the transfer function of the LCL filter, $\left|G_{LCL}\right|_{\omega}$ and ϕ are the amplitude gain and phase shift of $G_{LCL}(s)$ at frequency ω. As mentioned earlier, a properly designed high-pass filter can extract $i_{g,hf}$ from the grid-side current measurement. In order to demodulate the high-frequency signal, $i_{g,hf}$ is multiplied with signal $\cos\left(\omega t\right)$, and the demodulated signal can be written as

$$A\left|G_{LCL}\right|_{\omega}\sin\left(\omega t+\phi\right)\cos\left(\omega t\right)=B\sin\left(\phi\right)+B\sin\left(2\omega t+\phi\right) \tag{4-3}$$

where $B=A\left|G_{LCL}\right|_{\omega}/2$. It should be noticed that the demodulated signal contains a constant term $B\sin\left(\phi\right)$ and a double-frequency term $B\sin\left(2\omega t+\phi\right)$. Then the low-pass filter can attenuate the double-frequency term and only the constant term can be amplified by the PI controller. Since the LCL filter has a –180° phase shift at the resonant frequency, i.e., $\phi=-180°\big|_{\omega=\omega_{re}}$, the demodulated signal after the low-pass filter should be 0 when the estimated resonant frequency matches with the actual resonant frequency. Thus, the estimation of the resonant frequency is equivalent to seeking the optimum operation point ω that can enforce $B\sin\left(\phi\right)$ to be 0, and the ESC scheme can be utilized as a resonant frequency estimator. Compared with the conventional ESC scheme shown in Figure 4-2, the integrator is replaced by the PI controller to accelerate the dynamic response. Compared with the DFT and RPE schemes, the computation of the ESC scheme has been notably simplified. For example, in the RPE scheme, the complicated matrix computation is necessary to update the estimation, which can lead to a massive computational time, while the complicated matrix computation is totally avoided in the proposed scheme.

It should be noticed that the tuning of the PI controller must consider the frequency response of the LCL filter, which is given in Figure 4-1. It can be seen that the phase angle of the LCL filter satisfies (4-4) if the stray resistance of the LCL filter is ignored.

$$\begin{cases} \phi = -90^{\circ}, \omega < \omega_{re} \\ \phi = -180^{\circ}, \omega = \omega_{re} \\ \phi = -270^{\circ}, \omega > \omega_{re} \end{cases} \quad (4\text{-}4)$$

As mentioned earlier, the output of the low-pass filter, i.e., the input of the PI controller, is the constant term of the demodulated signal, which is $B\sin(\phi)$. Thus, when the estimated resonant frequency is lower than the actual resonant frequency, the input of the PI controller is negative. Similarly, when the estimated resonant frequency is higher than the actual resonant frequency, the input of PI is positive. Thus, in order to achieve the tracking of the actual resonant frequency, the PI controller must satisfy $k_p < 0$ and $k_i < 0$, where k_p and k_i are the proportional gain and integral gain of the PI controller respectively, and (4-5) shows the output of the PI controller, i.e., ω_{ESC}, at different frequency regions.

$$\begin{cases} \omega_{ESC} > 0, \omega < \omega_{re} \\ \omega_{ESC} = 0, \omega = \omega_{re} \\ \omega_{ESC} < 0^{\circ}, \omega > \omega_{re} \end{cases} \quad (4\text{-}5)$$

4.3.2 Simulation and Hardware-in-the-Loop Studies

In order to validate the performance of the proposed ESC based estimation scheme, comprehensive simulation and hardware-in-the-loop (HIL) studies have been conducted. In both simulation and HIL studies, the PI controller is designed as $k_p = -200$ and $k_i = -2$. The amplitude of the injection signal is $A = 0.05$. The sampling frequency of the proposed scheme is 10 kHz. The bandwidths of the low-pass filter and high-pass filter are set as 30 Hz and 120 Hz respectively. Figure 4-4 shows the simulation results of the proposed scheme. It can be seen that

the proposed scheme can provide an accurate estimation of the actual resonant frequency of the LCL filter within 0.3 s.

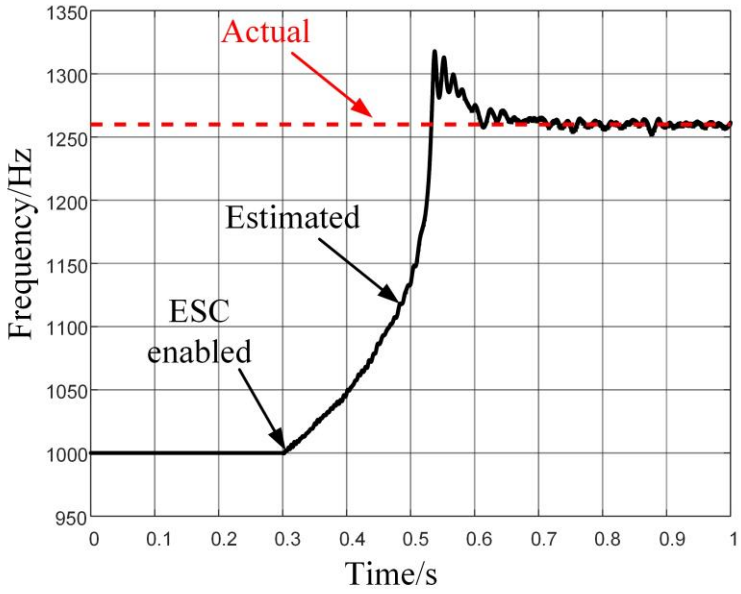
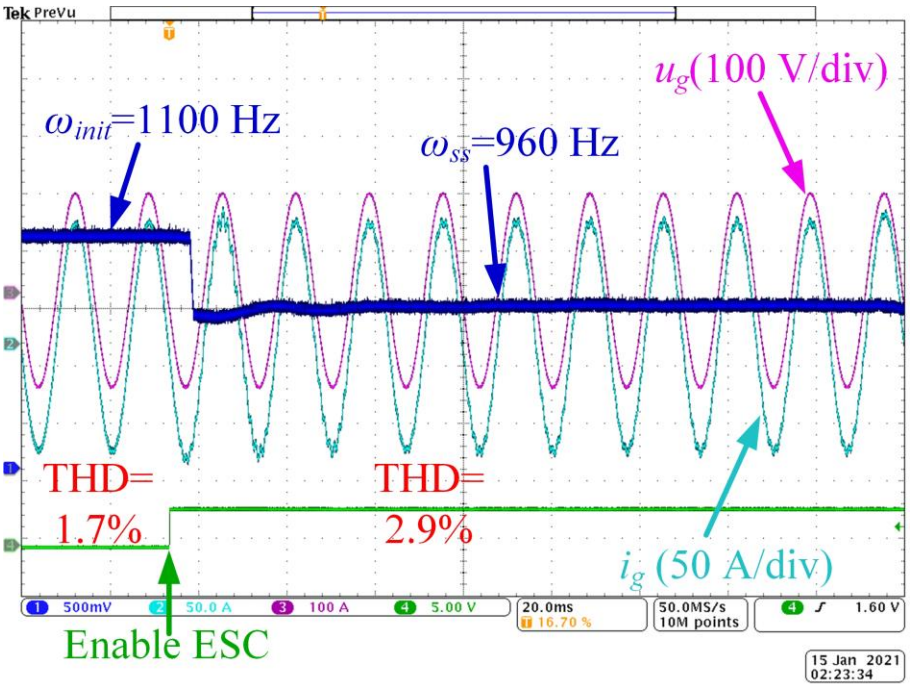


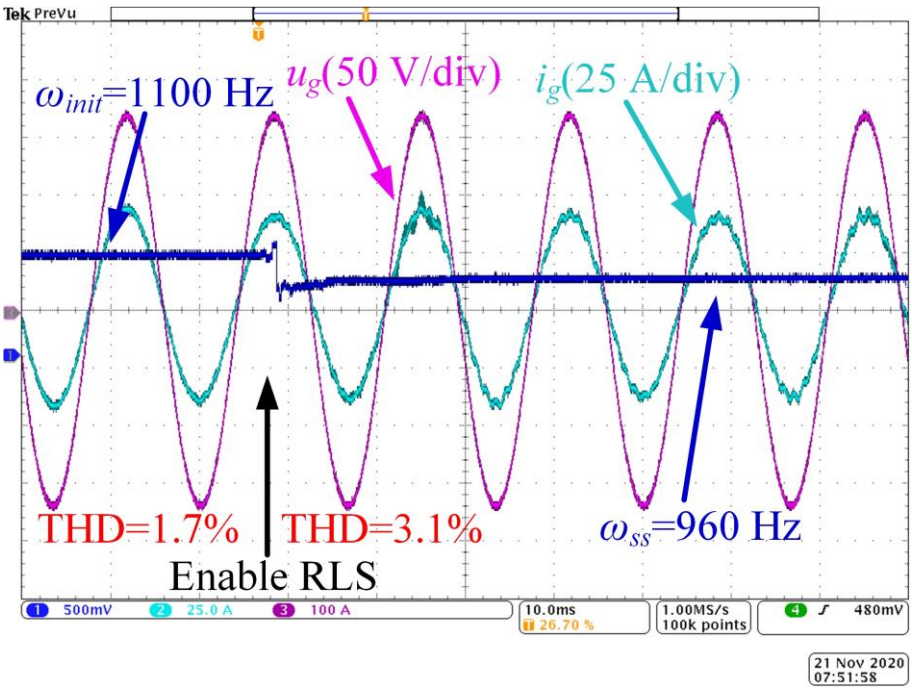
Figure 4-4. Simulation of the proposed ESC based estimation scheme.

Besides, in order to further validate the effectiveness of the proposed scheme, HIL tests have been conducted. Figure 4-5 shows the HIL results, where the proposed scheme is implemented on the TI TMS320F28335 DSP and a Typhoon HIL402 simulator is used as the test bench. In the HIL test, the LCL parameters are L_1=5 mH, L_2=2.9 mH, and C=15 μF. The actual resonant frequency is 960 Hz in the HIL test since the 1 mH L_g is also added into the system. The initial frequency of the proposed scheme is set as 1100 Hz, which is the same as that of the LCL filter without grid-side impedance. During the HIL test, the RLS scheme is also tested for comparison. The execution time of the proposed scheme on the selected DSP is only 28.3 μs, while the RLS scheme needs 79.4 μs to finish the update of the estimation. Besides, the proposed scheme has less current distortion compared with that in the RLS scheme. Thus, the proposed scheme can provide an

accurate estimation of the LCL filter resonant frequency with notably reduced computation complexity.



(a)



(b)

Figure 4-5. Estimation of the LCL filter actual resonant frequency: (a) proposed scheme and (b) RLS scheme.

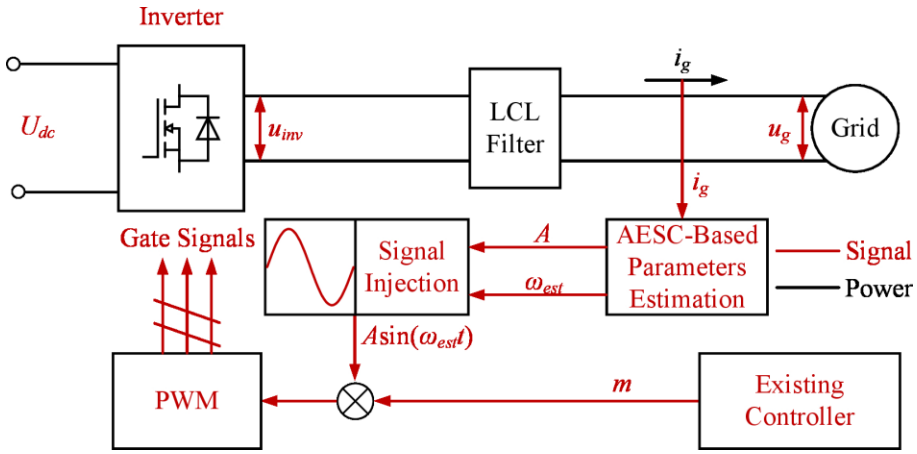
4.4 AESC Based LCL Filter Resonant Frequency Estimation

4.4.1 AESC based Estimation Scheme

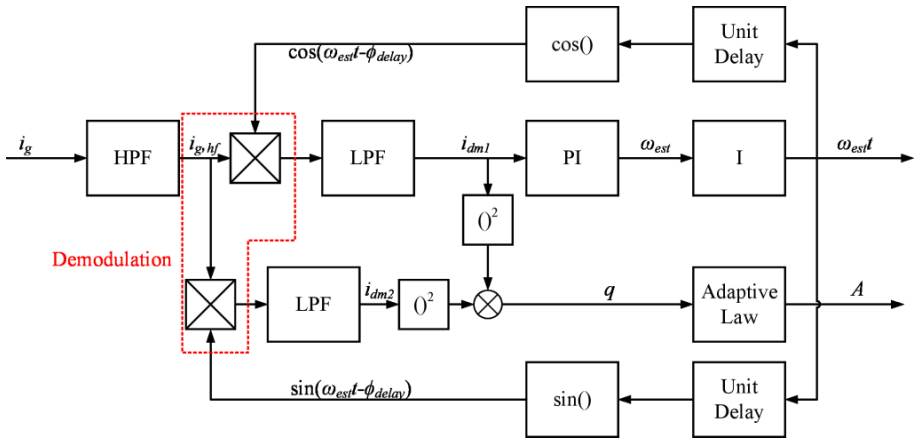
In the design of the ESC based LCL filter resonant frequency estimation scheme, the selection of the amplitude of the injection signal is critical, which determines the dynamic response of the estimation scheme and can impact the steady-state inverter output current quality. A low amplitude injection signal can improve the steady-state power quality, while the convergence time of the estimation scheme will be longer. Nevertheless, a high amplitude injection signal could enhance the dynamic response of the estimation scheme at the cost of the inverter output current quality. Thus, a satisfactory tradeoff between the dynamic response of the estimation scheme and the steady-state inverter output power quality can be achieved by actively adjusting the amplitude of the injection signal. Based on the previously discussed ESC based estimation scheme, an adaptive ESC (AESC) based LCL filter resonant frequency estimation is proposed here.

Figure 4-6(a) shows the inverter-level system diagram, where the AESC based estimation scheme is integrated with an existing controller, i_g is grid-side current, A is the amplitude of the injection signal, ω_{est} is the estimated resonant frequency of the LCL filter, and m is the output of the existing controller. The AESC scheme samples grid-side current i_g and provides the estimation of the resonant frequency ω_{est} as well as the amplitude of the injection signal A. Then the signal injection block injects an HF signal $A\sin(\omega_{est}t)$ into the inverter output voltage to excite the LCL filter. Figure 4-6(b) shows the detailed diagram of the proposed scheme, where HPF is the high-pass filter, $i_{g,hf}$ is the HF response of the grid-side current excited by the injection signal, LPF is the low-pass filter, i_{dm1} and i_{dm2} are the outputs of the low-pass filters respectively, q is the input

of the adaptive law, PI is the proportional-integral controller, I is the integrator, and the unit delay blocks are used to cancel the one-step delay caused by the digital control.



(a)



(b)

Figure 4-6. AESC based resonant frequency estimation scheme: (a) inverter-level system diagram and (b) detailed diagram of AESC.

With the signal injection, the grid-side current can be written as

$$i_g(t) = I_{fund}\sin\left(\omega_{fund}t + \phi_{fund}\right) + B\sin\left(\omega_{est}t + \phi_1 - \phi_{delay}\right) \tag{4-6}$$

where ω_{fund} is the grid fundamental frequency, ϕ_{fund} is the phase angle of the fundamental current, I_{fund} is the amplitude of the fundamental grid-side current, B is the amplitude of the HF response of the grid-side current that is excited by the injection signal, ϕ_1 is the phase angle of the LCL filter at frequency ω_{est}, and ϕ_{delay} is the phase delay caused by the digital control. Assuming the HPF can eliminate the fundamental component, and the extracted HF response of i_g can be written as

$$i_{g,hf}(t) = C\sin\left(\omega_{est} + \phi_1 + \phi_2 - \phi_{delay}\right) \tag{4-7}$$

where C is the amplitude of the extracted signal, and ϕ_2 is the phase angle of the HPF at frequency ω_{est}. It should be noted that a properly designed HPF should provide high attenuation performance at the fundamental frequency and introduce low amplitude and phase angle distortions at frequency ω_{est}, i.e., $C \approx B$ and $\phi_2 \approx 0$. Besides the signal injection, the estimated resonant frequency is also used to demodulate the HF grid-side current. In the cosine demodulation branch, the demodulated signal is

$$\cos\left(\omega_{est}t - \phi_{delay}\right) \times i_{g,hf} = \frac{C}{2} \times \left[\underbrace{\sin\left(\phi_1 + \phi_2\right)}_{\text{constant}} + \underbrace{\sin\left(2\omega_{est} + \phi_1 + \phi_2 - 2\phi_{delay}\right)}_{\text{double-frequency}} \right] \tag{4-8}$$

Similarly, the demodulated signal in the sine branch is

$$\sin\left(\omega_{est}t-\phi_{delay}\right)\times i_{g,hf}=\frac{C}{2}\times\left[\underbrace{\cos\left(\phi_1+\phi_2\right)}_{\text{constant}}-\underbrace{\cos\left(2\omega_{est}+\phi_1+\phi_2-2\phi_{delay}\right)}_{\text{double-frequency}}\right] \tag{4-9}$$

It can be seen that both demodulated signals consist of low-frequency components and double-frequency components. Especially, the low-frequency components, i.e., $\cos\left(\phi_1+\phi_2\right)$ and $\sin\left(\phi_1+\phi_2\right)$ contain the phase angle of the LCL filter. Thus, the LPFs are used to remove the double-frequency components and extract the low-frequency components. Supposing a properly designed LPF can totally remove the double-frequency components, the outputs of the low-pass filters can be written as

$$\begin{cases} i_{dm1}=\dfrac{C}{2}\sin\left(\phi_1+\phi_2\right) \\ i_{dm2}=\dfrac{C}{2}\cos\left(\phi_1+\phi_2\right) \end{cases} \tag{4-10}$$

As mentioned earlier, a properly designed HPF should satisfy $\phi_2 \approx 0$. Based on the frequency response of the LCL filter given in Figure 4-1(b), signal i_{dm1} satisfies

$$\begin{cases} i_{dm1}<0,\ \omega_{est}<\omega_r \\ i_{dm1}=0,\ \omega_{est}=\omega_r \\ i_{dm1}>0,\ \omega_{est}>\omega_r \end{cases} \tag{4-11}$$

Thus, a PI controller is used to seek the estimated frequency that can lead to $i_{dm1} = 0$, where the estimated frequency is the same as the resonant frequency of the LCL filter.

It should be noticed that under a constant amplitude of injection signal, i.e., *A* is a constant, the amplitudes of HF responses, i.e., *B* and *C*, vary at different ω_{est} . In other words, the amplitude response of the LCL filter, which is given in Figure 4-1(b), determines the ratio *B/A*. It can be seen that at the resonant frequency, the ratio *B/A* is much larger than that at different frequencies. Small amplitude of injection signal is preferred to improve the inverter output power quality with a slow dynamic response. In contrast, a large amplitude *A* can improve the dynamic response of the proposed scheme at the cost of steady-state current quality. To address the tradeoff between the power quality of the inverter and the dynamic response of the proposed scheme, an adaptive law is adopted to actively adjust the amplitude of the injection signal. Based on Figure 4-6 and (4-6), the input of the adaptive law satisfies

$$\begin{aligned} q &= i_{dm1}^2 + i_{dm2}^2 \\ &= \frac{C^2}{4} \end{aligned} \tag{4-12}$$

which means *q* can represent the amplitude of the HF response of the i_g. Thus, a simple adaptive law is adopted as

$$A = \frac{J}{2\sqrt{q} + \lambda} \tag{4-13}$$

where $J > 0$ is a constant that limits the maximum amplitude of the injection signal, and $\lambda > 0$ is a constant that can avoid dividing zero. With the adaptive law (4-13), the AESC scheme can decrease

the amplitude of the injection signal when ω_{est} approaches ω_r, and thus, the inverter output current quality can be improved. Meanwhile, a large amplitude of the injection signal will be used when ω_{est} is far from the resonant frequency, which can enhance the dynamic response of the proposed scheme. Figure 4-7 shows the concept of the adaptive amplitude. It can be seen from the figure that the proposed adaptive law can actively adjust the amplitude of the injection signal at different frequency regions, and thus, a satisfactory tradeoff between the steady-state inverter output power quality and the dynamic response can be achieved.

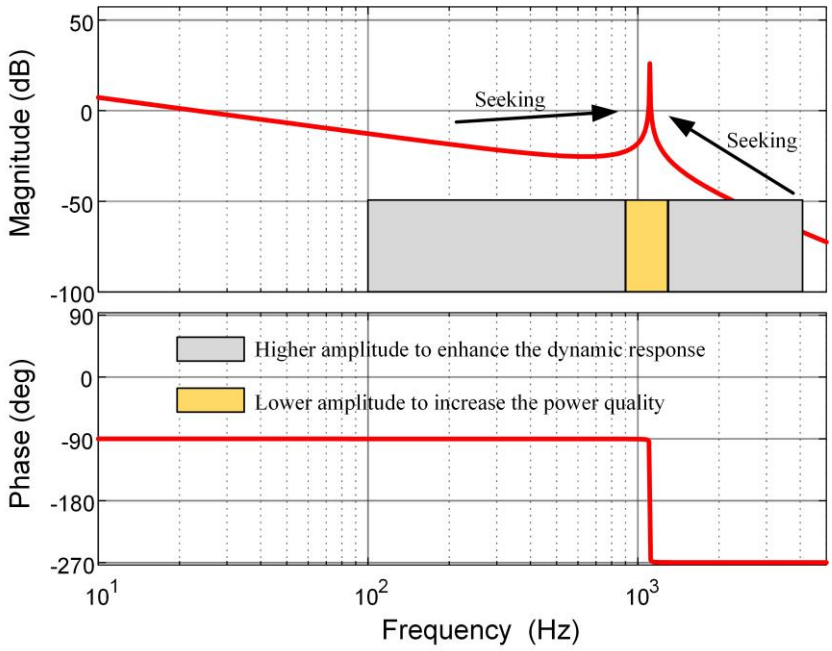


Figure 4-7. Adaptive amplitude of the injection signal.

Remark 1: With the estimated resonant frequency of the LCL filter, i.e., ω_{est}, it is possible to calculate the grid impedance. According to [3], assuming LCL filter parameters are known, and the grid impedance is inductive, i.e., the grid impedance can be represented by L_g shown in Figure

4-1(a). The resonant frequency of the LCL filter without grid impedance can be calculated as $\omega_{r,LCL}=\sqrt{\frac{L_1+L_2}{L_1L_2C}}$ .In the steady-state, define $\Delta=\omega_{est}^2-\omega_{r,LCL}^2$ to represent the difference of resonant frequency caused by the grid impedance. Then the grid impedance can be calculated as $L_g=L_2\left(\frac{1}{1+L_2C\Delta}-1\right)$.

4.4.2 AESC Design and Stability Analysis

As mentioned earlier, the HPF eliminates the fundamental component from the grid-side current, while the LPFs remove the double-frequency components from the demodulated signals. Here, a second-order HPF is used to reduce the complexity, whose transfer function can be written as

$$HPF\left(s\right)=\frac{s^2}{\left(s+\alpha\right)^2} \tag{4-14}$$

where α is the bandwidth of the HPF. It can be seen from (4-10) that the accuracy of the estimation scheme depends on the phase angle of the HPF at the estimated frequency, i.e., ϕ_2 . Meanwhile, the bandwidth of the HPF also determines the attenuation of the fundamental grid-side current. In this work, the bandwidth of the high-pass filter is set as 1.5 times of the fundamental frequency, i.e., α=1.5ω_{fund} , which can provide about 10 dB attenuation performance.

The LPFs need to remove the double-frequency components from the demodulated signals. However, as the LPFs and the PI controller are inside of the feedback loop, the stability of the

proposed scheme should be analyzed. Supposing second-order LPFs are adopted, which can be written as

$$LPF(s) = \frac{\beta^2}{(s+\beta)^2} \tag{4-15}$$

where β is the bandwidth of the LPF. The PI controller can be written as

$$PI(s) = k_p + \frac{k_i}{s} \tag{4-16}$$

where k_p and k_i are the gains of the PI controller. To simplify the controller design, the ratio between k_i and k_p is set as β, i.e., $k_i = \beta k_p$. Based on Figure 4-6(b), the estimated resonant frequency satisfies

$$\frac{d\omega_{est}}{dt} = k_p \frac{di_{dm1}}{dt} + k_i i_{dm1} \tag{4-17}$$

Define the estimation error e as $e = \omega_r - \omega_{est}$, and a Lyapunov function V can be defined as

$$V = \frac{1}{2}e^2 \tag{4-18}$$

Supposing the actual resonant frequency ω_r is slow time-varying. The derivative of V can be calculated as

$$\begin{aligned}\frac{dV}{dt} &= e\frac{de}{dt} \\ &= -e\frac{d\omega_{est}}{dt} \\ &= -e\left(k_p\frac{di_{dm1}}{dt} + k_i i_{dm1}\right)\end{aligned} \tag{4-19}$$

Define an intermediate variable *p* that satisfies

$$p = \frac{1}{\beta}\left(\frac{di_{dm1}}{dt} + \beta i_{dm1}\right) \tag{4-20}$$

Actually, the intermediate variable *p* can be regarded as the output of a virtual first-order LPF $\beta/(s+\beta)$, and the input of the virtual LPF is the same as that of the LPF shown in Figure 4-6(b). With the variable *p*, equation (4-19) can be rewritten as

$$\frac{dV}{dt} = -e\left(k_p\frac{di_{dm1}}{dt} + k_i i_{dm1}\right) = -e\beta k_p p \tag{4-21}$$

The intermediate variable *p* also satisfies (4-11) by replacing i_{dm1} with *p* if the virtual LPF can effectively attenuate the double-frequency components. Thus, based on the Lyapunov criterion, the proposed scheme is stable if $k_p<0$.

According to the above stability analysis, it can be seen that the design of the LPF filter bandwidth should be low enough to reject the double-frequency component. In practice, the resonant frequency ωr usually is much high than the fundamental frequency ω_{fund}. In this work, the bandwidth β is set the same as the fundamental frequency, i.e., $\beta=\omega_{fund}$. Figure 4-8 shows the frequency responses of the designed HPF and LPF.

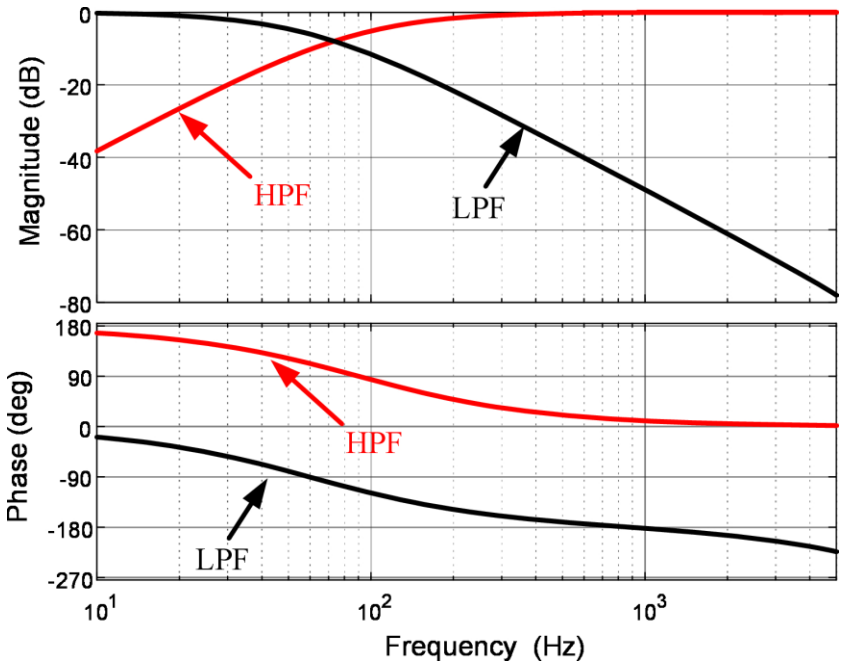


Figure 4-8. Frequency responses of the designed HPF and LPF.

4.4.3 Accuracy and implementation discussions

4.4.3.1 Harmonics

It can be seen from the previous analysis that the AESC scheme could ensure the zero steady-state error of the resonant frequency estimation. However, the actual implementation of the proposed scheme must consider the harmonic currents. Considering the grid-side current contains harmonics, the grid-side current in (4-6) can be rewritten as

$$\begin{aligned} i_g(t) = I_{fund}\sin\left(\omega_{fund}t+\phi_{fund}\right) + B\sin\left(\omega_{est}t+\phi_1-\phi_{delay}\right) \\ + \sum_{n=3,5,7...} I_n \sin\left(n\omega_{fund}t+\phi_n\right) \end{aligned} \tag{4-22}$$

where n is the order of harmonics, I_n is the amplitude of the n^{th}-order harmonic, and ϕ_n is the phase angle of harmonic current. It should be noticed that the HPF may not be able to eliminate the

harmonics since the frequency of harmonic might be within the bandwidth of HPF. Thus, the high-frequency response of the grid-side current, which is given in (4-7), should be rewritten as

$$i_{g,hf}(t) = C\sin\left(\omega_{est} + \phi_1 + \phi_2 - \phi_{delay}\right) + \sum_{n=3,5,7...} D_n \sin\left(n\omega_{fund}t + \phi_{HPF,n}\right) \tag{4-23}$$

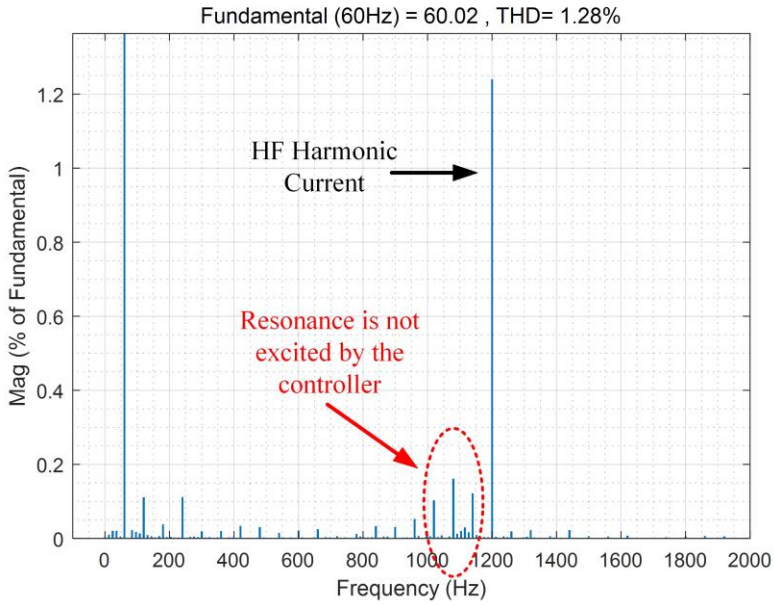
where D_n is the amplitude of the n^{th}-order harmonic current after the HPF, and $\phi_{HPF,n}$ is the phase angle of the n^{th}-order harmonic current after the HPF. In the cosine demodulation branch, the demodulated signal can be rewritten as

$$\begin{aligned}
&\cos\left(\omega_{est}t - \phi_{delay}\right) \times i_{g,hf} \\
&= \frac{C}{2} \times \left[\underbrace{\sin\left(\phi_1 + \phi_2\right)}_{\text{constant}} + \underbrace{\sin\left(2\omega_{est} + \phi_1 + \phi_2 - 2\phi_{delay}\right)}_{\text{double-frequency}} \right] + \\
&\underbrace{\sum_{n=3,5,7...} \frac{D_n}{2} \left[\begin{array}{l} \sin\left(n\omega_{fund}t + \phi_{HPF,n} - \omega_{est}t + \phi_{delay}\right) + \\ \sin\left(\omega_{est}t - \phi_{delay} + n\omega_{fund}t + \phi_{HPF,n}\right) \end{array} \right]}_{\text{harmonics after demodulation}}
\end{aligned} \tag{4-24}$$

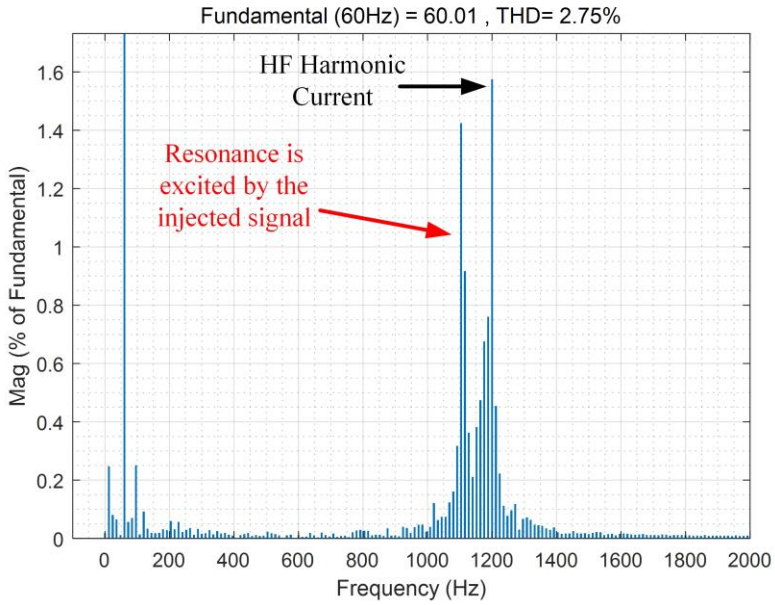
Similarly, the sine demodulation branch satisfies

$$\begin{aligned}
&\sin\left(\omega_{est}t - \phi_{delay}\right) \times i_{g,hf} \\
&= \frac{C}{2} \times \left[\underbrace{\cos\left(\phi_1 + \phi_2\right)}_{\text{constant}} - \underbrace{\cos\left(2\omega_{est} + \phi_1 + \phi_2 - 2\phi_{delay}\right)}_{\text{double-frequency}} \right] + \\
&\underbrace{\sum_{n=3,5,7...} \frac{D_n}{2} \left[\begin{array}{l} \cos\left(\omega_{est}t - \phi_{delay} - n\omega_{fund}t - \phi_{HPF,n}\right) - \\ \cos\left(\omega_{est}t - \phi_{delay} + n\omega_{fund}t + \phi_{HPF,n}\right) \end{array} \right]}_{\text{harmonics after demodulation}}
\end{aligned} \tag{4-25}$$

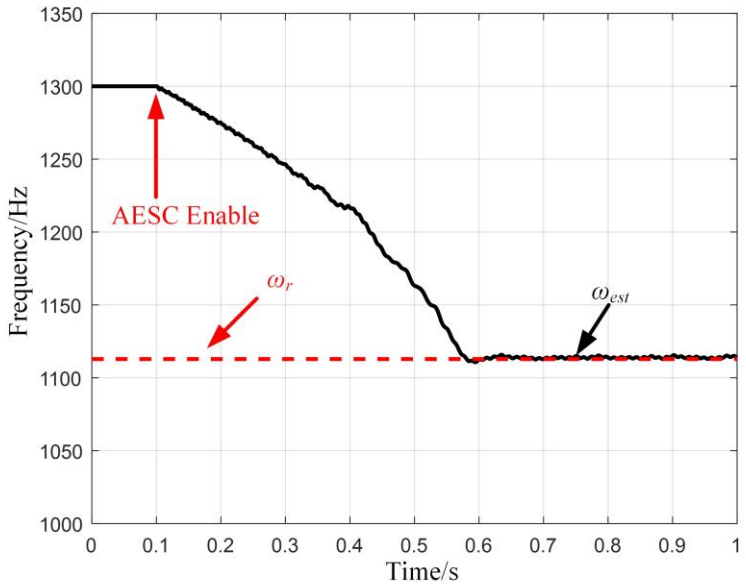
It should be noticed that with a properly designed controller, the resonant frequency of the LCL filter should be away from the harmonic frequencies, otherwise the harmonics will excite the resonance and notably deteriorate the output power quality. Especially, when the frequency of a certain order harmonic is in the vicinity of the resonant frequency, the amplitude of this harmonic should be effectively attenuated, otherwise, the resonance of the LCL filter will be excited by the controller. In other words, the amplitude of the excited high-frequency response should be much higher than that of the harmonics whose frequencies are close to the resonant frequency, i.e., $C \square D_j|_{\omega_{est} \approx \omega_r, j\omega_{fund} \approx \omega_r}$. On the other hand, the low-pass filter can also attenuate the harmonics after demodulation if ω_{est}-$n\omega_{fund}$ is not within the bandwidth of LPF. For example, the frequency of the 7th-order harmonic is 420 Hz. Supposing the resonant frequency of the LCL filter is 1200 Hz, the demodulated signal of the 7th-order harmonic contains two frequency components: 780 Hz and 1620 Hz. Thus, the LPF can effectively reject the harmonics and the proposed scheme can still provide satisfactory estimation results even under a highly distorted grid. Figure 4-9 shows the simulated results when the harmonic frequencies overlap the resonance frequency. In the simulation, the actual resonant frequency of the LCL filter is 1110 Hz. It can be seen from Figure 4-9(a) that before the AESC scheme is enabled, there is an HF harmonic current, whose frequency is 1200 Hz and is close to the actual resonant frequency of the LCL filter. The inverter controller is well-tuned and the resonance of the LCL filter is not excited by the controller. Figure 4-9(b) shows the current spectrum after the AESC scheme is enabled. It can be seen that the injected HF single $A\sin(\omega_{est}t)$ can excite the resonance of the LCL filter, which means that $C \square D_j|_{\omega_{est} \approx \omega_r, j\omega_{fund} \approx \omega_r}$. Figure 4-9(c) shows the estimated resonant frequency of the LCL filter, and the results show that the proposed scheme can still provide satisfactory estimation performance even the harmonic frequencies overlap the resonant frequency.


Fundamental (60Hz) = 60.02 , THD= 1.28%
HF Harmonic Current
Resonance is not excited by the controller
Mag (% of Fundamental)
Frequency (Hz)
0
0.2
0.4
0.6
0.8
1
1.2
0
200
400
600
800
1000
1200
1400
1600
1800
2000

(a)


Fundamental (60Hz) = 60.01 , THD= 2.75%
HF Harmonic Current
Resonance is excited by the injected signal
Mag (% of Fundamental)
Frequency (Hz)
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
0
200
400
600
800
1000
1200
1400
1600
1800
2000

(b)



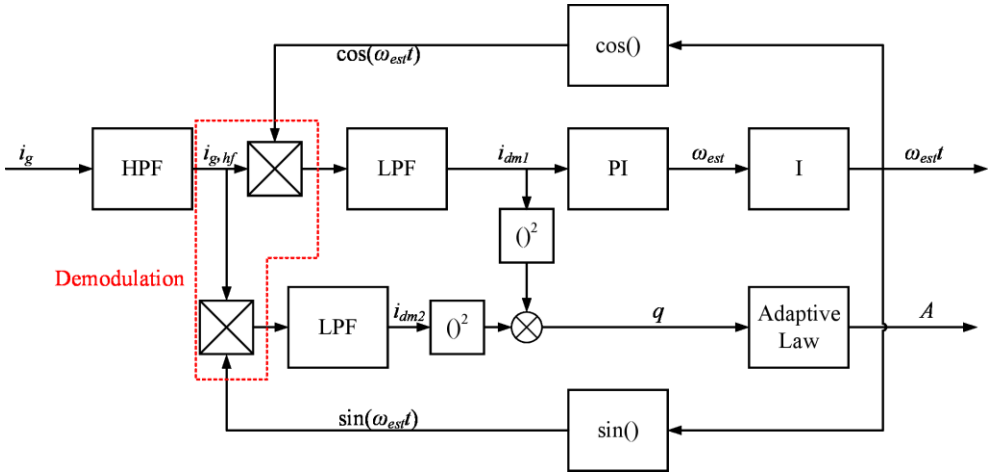
(c)

Figure 4-9. Simulated results when the harmonic frequencies overlap the resonant frequency: (a) frequency spectrum of the grid-side current before the AESC scheme is enabled, (b) frequency spectrum of the grid-side current after the AESC scheme is enabled, and (c) estimated resonant frequency.

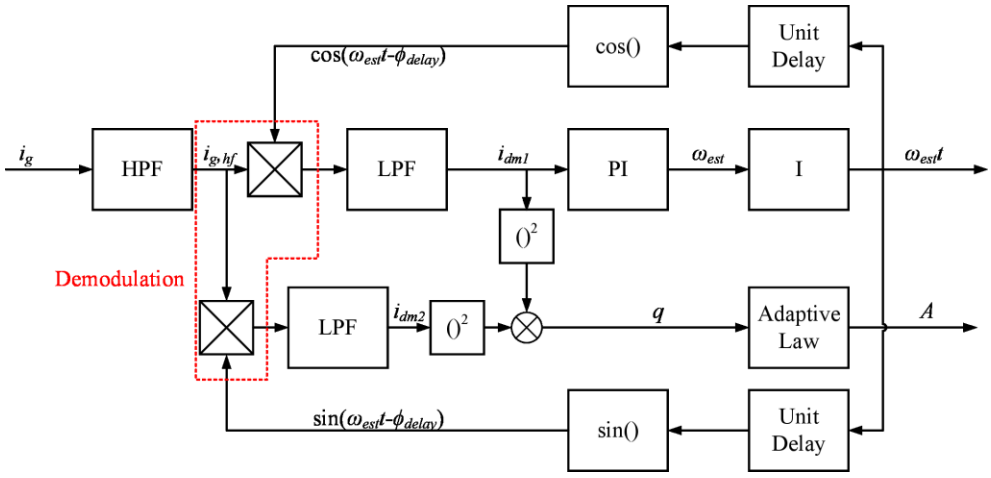
4.4.3.2 Control delay

In the digital control, there is a one-step delay between the injection signal and the high-frequency output from the inverter due to the digital control, which can be written as $G_{delay} = e^{-sT_s}$, where T_s is the sampling time of the digital control. The one-step delay will result in an additional phase delay on the filter output and deteriorate the accuracy of the estimation scheme. Thus, it is important to compensate for the control delay in the signal demodulation processing. Figure 4-10(a) shows the AESC scheme without the delay compensation. Figure 4-10(b) presents the AESC scheme with the explicit delay compensation, which is also given in Figure 4-6(b). It can be seen that the high-frequency signal used in the demodulation has been delayed for one step to compensate for the delay caused by the digital control. With the compensation, the delay effect can

be significantly mitigated, and the estimation accuracy can be further improved. Figure 4-11 shows the simulation results of AESC with and without delay compensation. It can be seen from the simulation results that the delay caused by digital control can lead to about 10 Hz steady-state error, while the delay compensation can eliminate the steady-state error.

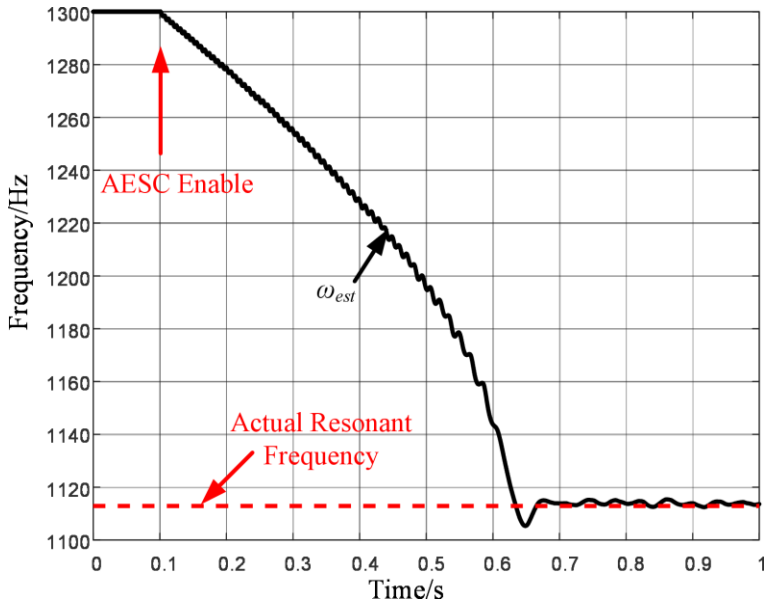


(a)

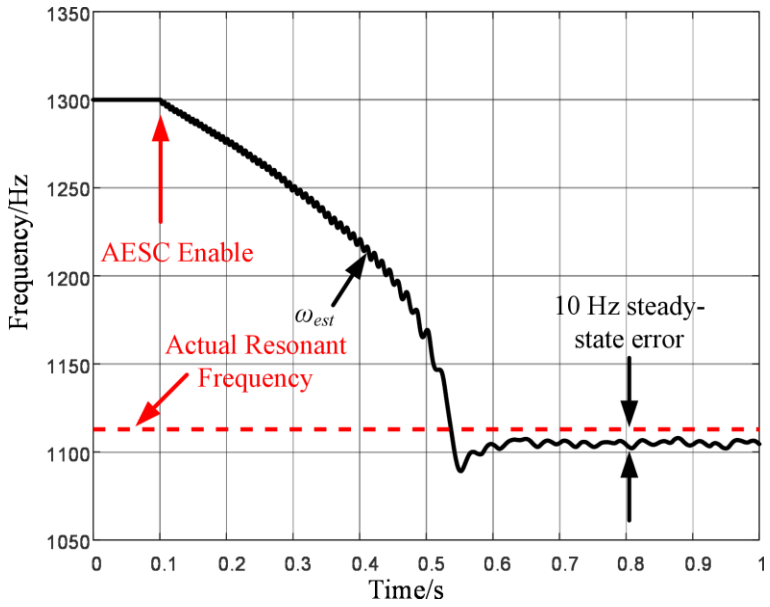


(b)

Figure 4-10. Diagram of AESC (a) without delay compensation and (b) with explicit delay compensation.



(a)



(b)

Figure 4-11. Simulation results of AESC scheme: (a) with delay compensation and (b) without delay compensation.

4.4.3.3 Multiple inverters

When multiple inverters are connected to the same point of common coupling (PCC), the proposed scheme can still be implemented in the inverters to estimate the actual resonant frequency of the LCL filter if the PCC voltage can be well regulated by the grid. In order to validate the estimation performance of the proposed scheme, simulation studies have been conducted. In the simulation, two grid-tied inverters with different LCL parameters are paralleled to provide power to the grid, and the AESC scheme is implemented on both inverters to estimate the resonant frequency respectively. Figure 4-12 shows the simulation results, where ω_{r1} and ω_{r2} are the resonant frequencies for the first and second inverters respectively, ω_{est1} and ω_{est2} are the estimated resonant frequencies. The simulation results suggest that the proposed scheme can provide satisfactory estimation performance when multiple inverters are paralleled.

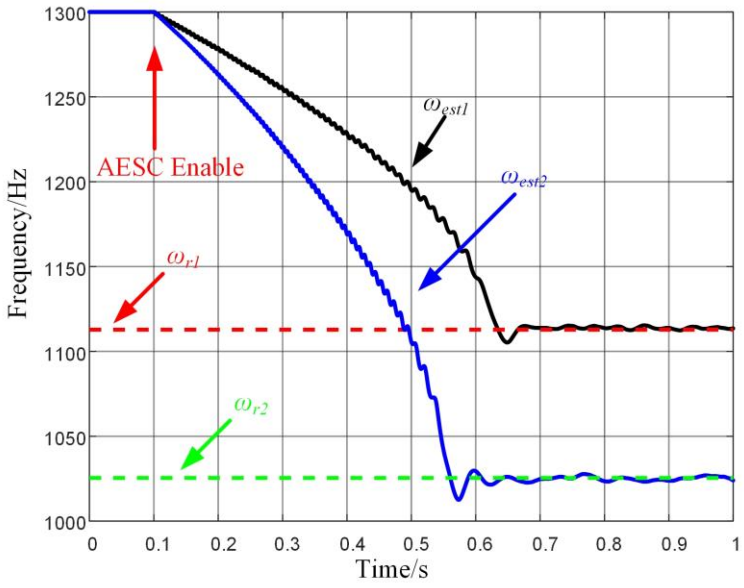


Figure 4-12. Estimated resonant frequency when two grid-tied inverters are paralleled.

4.4.3.4 Computational complexity

Compared with the recursive estimation schemes [6], [7], [12], the complicated matrix computation is avoided in the proposed AESC based estimation scheme. Based on Figure 4-6(b), Table 4-1 summarized the operation and the complexity of the proposed scheme, where the complexity is presented by using the big O notation [12].

TABLE 4-1. Summary of the Proposed Scheme

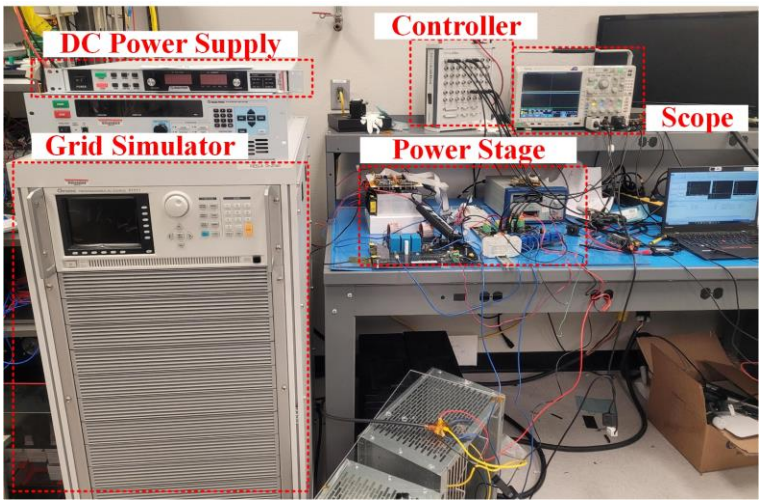
Operation	Complexity
N^{th}-order HPF	O(N)
Demodulation	O(1)
N^{th}-order LPF	O(N)
Square Operation: $()^2$	O(1)
PI and I	O(1)
Adaptive Law	O(1)
Unit Delay	O(1)
cos() and sin()	O(1)

It can be seen from Table 4-1 that except for the LPF and HPF, the complexity of all the other blocks shown in Figure 4-6(b) is in the order of O(1). Considering the order of the LPF and HPF is N, the overall computational complexity of the proposed scheme is in the order of O(N). The complexity of the RLS scheme is $O(N^2)$ [12], where N is the number of parameters to be estimated. Thus, the proposed scheme has much lower complexity compared with the recursive estimation

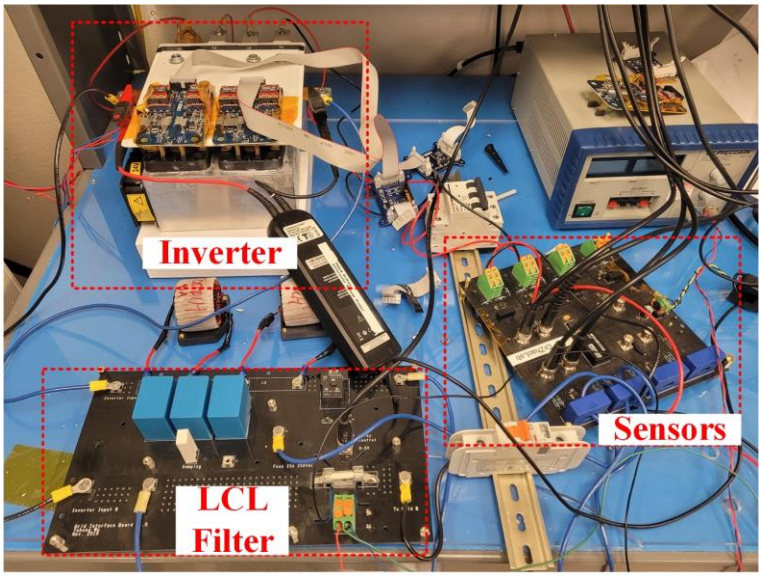
schemes. As an example, in this work, the order of filters is set as N = 2, while the number of parameters to be estimated in [6] and [7] is N = 5.

4.5 Experimental Studies

To validate the effectiveness of the proposed AESC scheme, experimental studies have been conducted. Figure 4-13 shows the experiment setup, where a grid simulator is used to simulate the grid, a single-phase inverter with an LCL filter is used as the grid-tied inverter, and the controller is implemented on a dSPACE MicroLabBox. The dc power supply is used to provide the dc power to the single-phase inverter, and the output port of the inverter is connected to the LCL filter, which is mounted on a standalone circuit board with additional protection units. The grid-side voltage and current are measured through a sensor board, and the outputs of the sensor board are fed back to the analog input ports of the dSPACE MicroLabBox. The parameters of the AESC scheme are set as α=90 Hz, β=60 Hz, J=0.5, λ=0.1, and k_p=100. It should be noticed that the parameters of LCL may not equal the nominal values in practice. Thus, the characterization of the LCL filter has been conducted before experiments. During the characterization, the grid-tied inverter outputs current to the grid through the LCL filter, and the amplitude of the grid-side current is the same as the one used in the experiments. Then based on [3], the actual resonant frequency of the LCL filter can be measured through fast Fourier transform (FFT). Figure 4-14 shows the characterization results of the LCL filter, and the measured resonant frequency of the LCL filter is 1200 Hz.

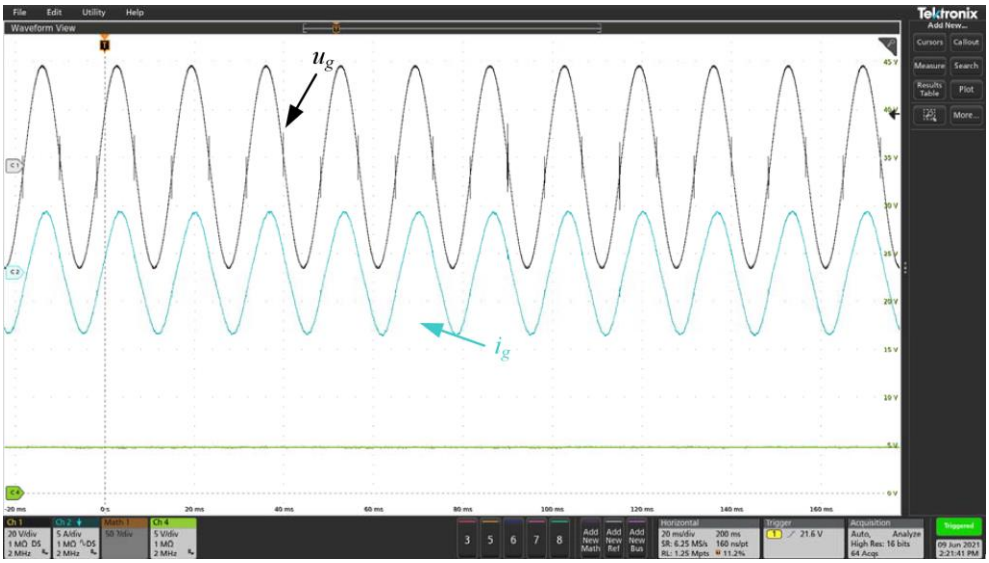


(a)

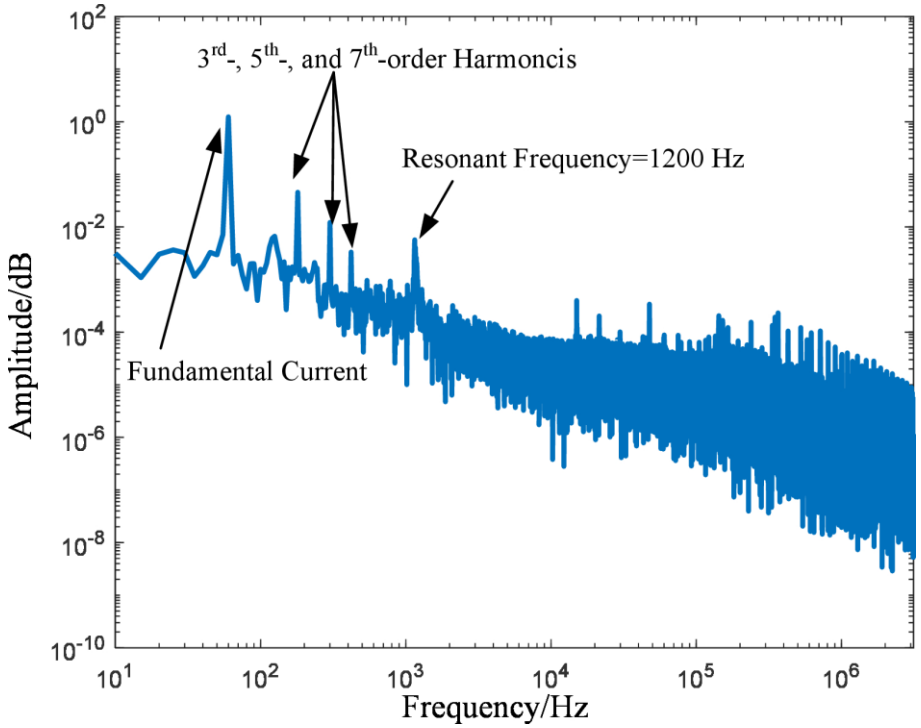


(b)

Figure 4-13. (a) Experiment setup and (b) details of the grid-tied inverter under test.



(a)

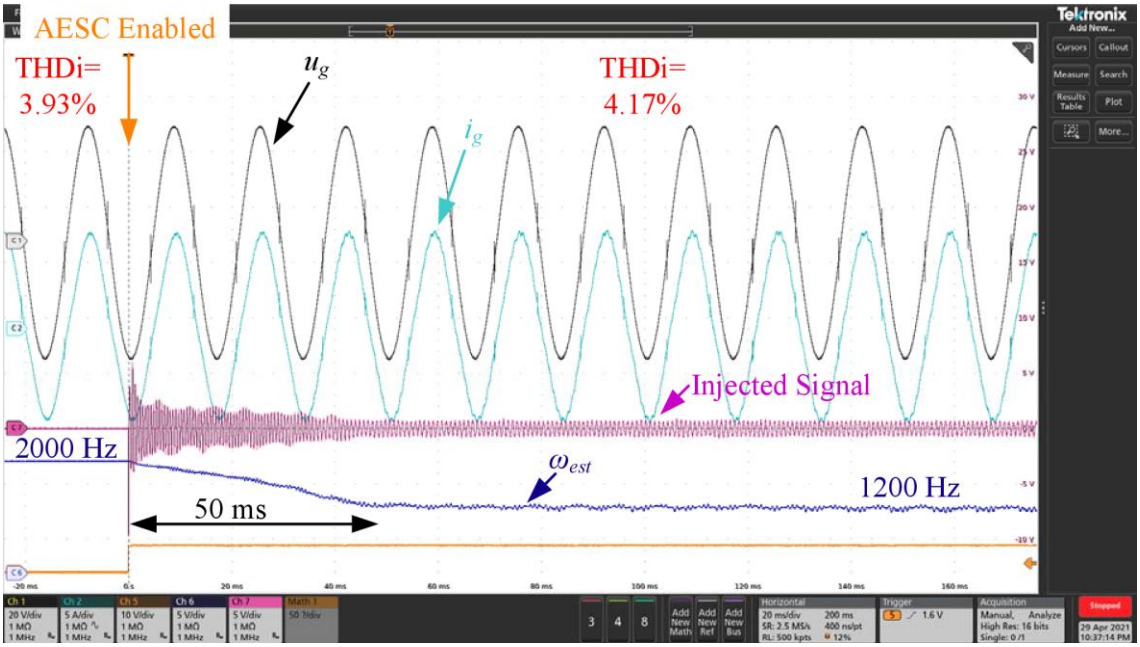


(b)

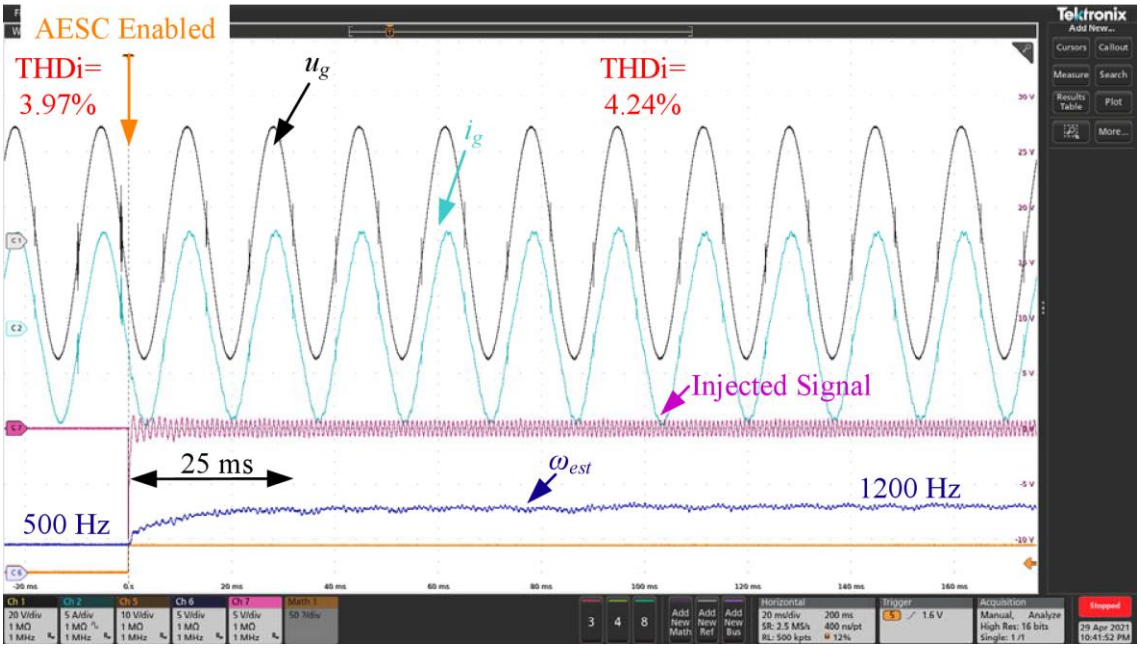
Figure 4-14. Characterization of the LCL filter (a) output of the grid-tied inverter and (b) FFT results of the grid-side current.

Figure 4-15 shows the experiment results. The initial value of the estimated resonant frequency $\omega_{est,init}$ is set higher and lower than ω_r in Figure 4-15(a) and (b) respectively to validate the convergence performance from both directions. The proposed scheme can achieve convergence within 3 fundamental cycles, i.e., 50 ms, in both tests. Moreover, the adaptive law can actively adjust the amplitude of the injection signal to tradeoff between dynamic response and steady-state current quality. Besides, Figure 4-16 shows the estimation performance of the proposed scheme under the weak grid condition, where an additional 1 mH inductor is added between PCC and grid simulator to represent the grid impedance L_g. Due to the grid impedance, the resonant frequency of the LCL filter reduces to 900 Hz, and the proposed scheme can still provide an accurate estimation of the actual resonant frequency. Figure 4-17 shows the estimation performance under a highly distorted grid. Similar to the results given in Figure 4-15, the proposed scheme can provide a satisfactory estimation result even under highly distorted grid voltage and current.

To compare the computational complexity of the proposed scheme with recursive estimation schemes presented in [6] and [7], the proposed scheme and RLS scheme have been implemented in both the MicroLabBox and a TI DSP TMS320F28335. The code for MicroLabBox is generated and downloaded into MicroLabBox by using Simulink Coder. The code for the TI DSP is also generated by MATLAB/Simulink and downloaded to the DSP by using Code Composer Studio. The measurement of the execution time follows the guides that are provided by dSPACE and MATLAB respectively [10], [11]. In the MicroLabBox, the execution time of the proposed scheme is 1.1 μs, while the RLS scheme needs 2.2 μs. Similarly, the proposed scheme costs 18.5 μs in the TI DSP while the RLS scheme costs 68.3 μs, which means that the proposed scheme has much less computational complexity and is more suitable for real-time applications.

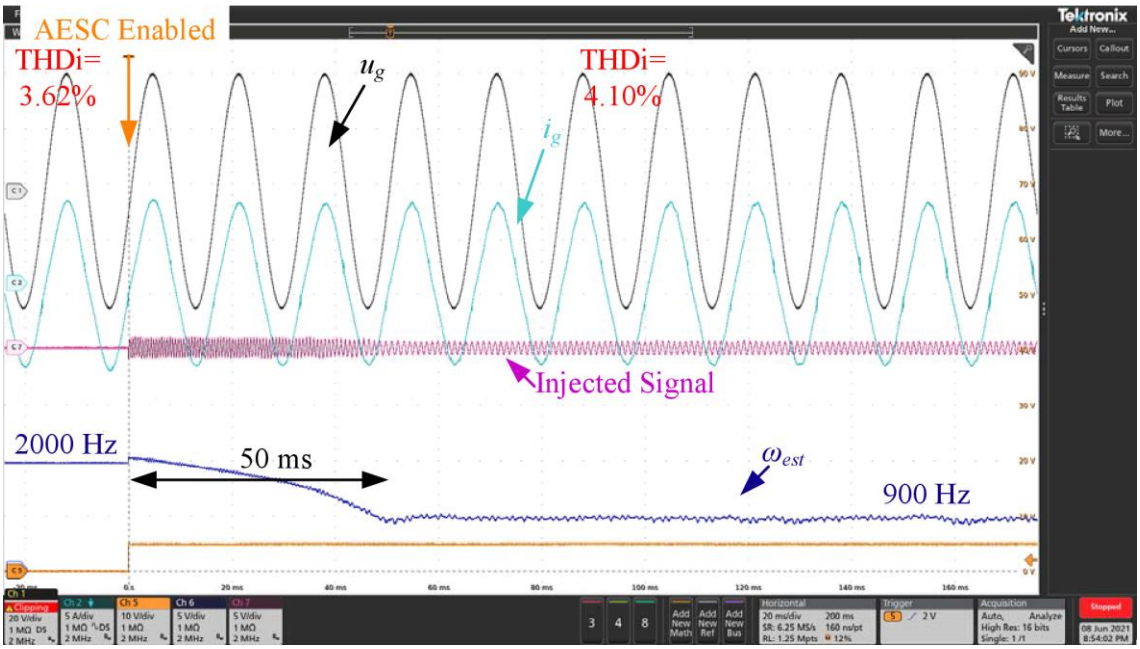


(a)

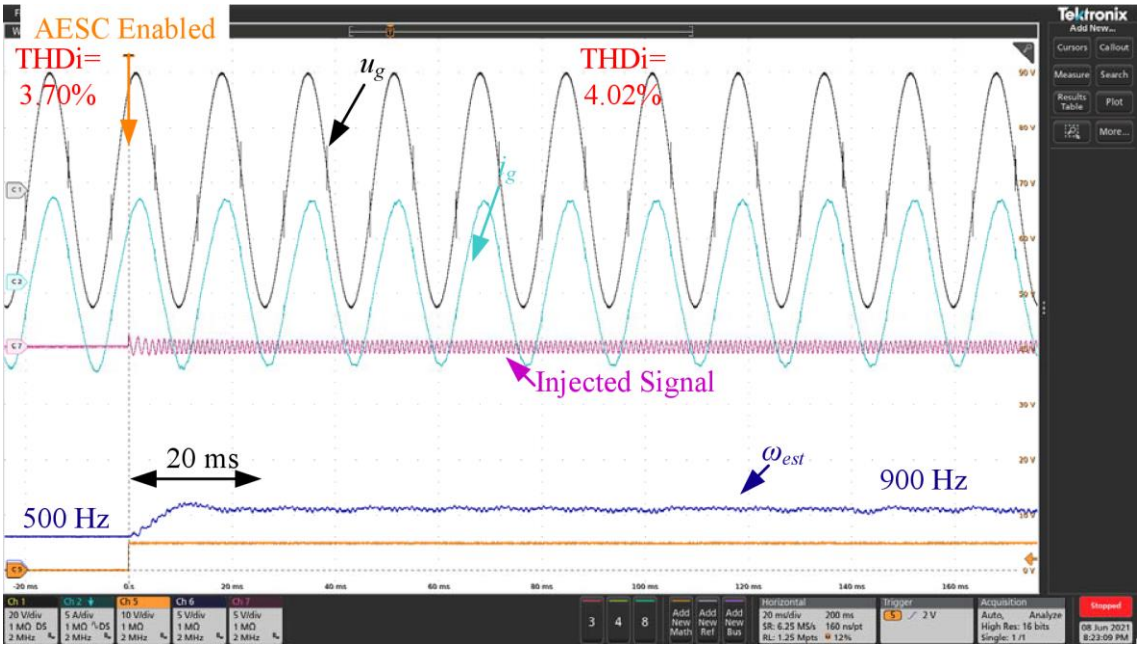


(b)

Figure 4-15. Performance of proposed scheme with differential initial conditions: (a) $\omega_r<\omega_{est,init}$ and (b) $\omega_>\omega_{est,init}$.



(a)



(b)

Figure 4-16. Performance of proposed scheme under weak grid with differential initial conditions: (a) $\omega_r<\omega_{est,init}$ and (b) $\omega>\omega_{est,init}$.

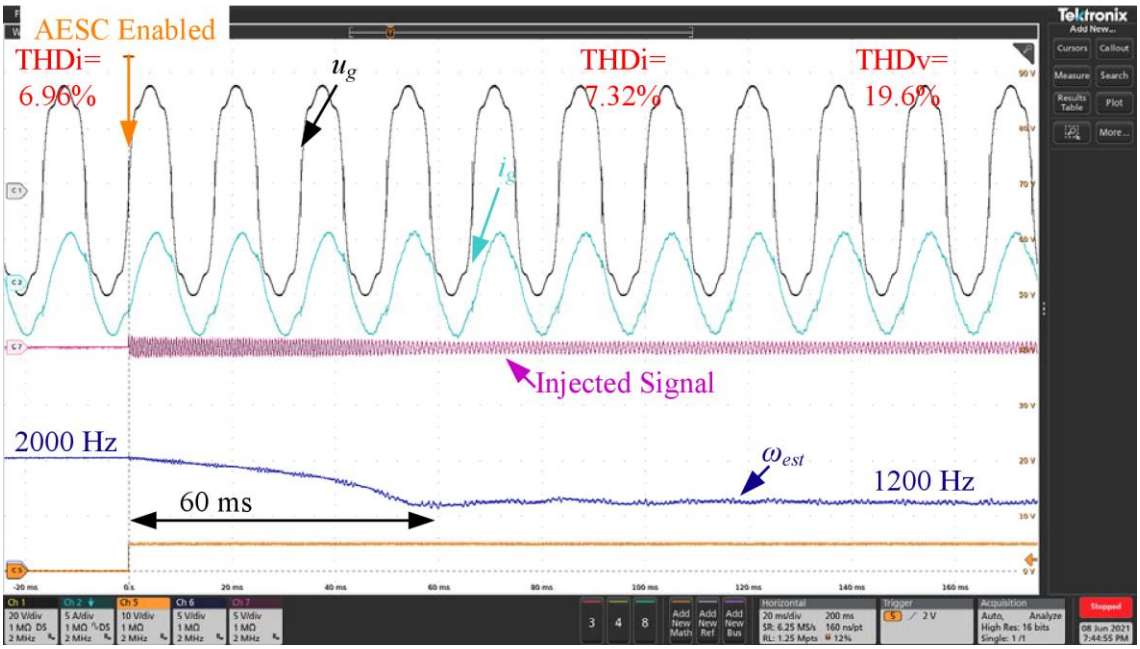


Figure 4-17. Performance of proposed scheme under highly distorted grid.

4.6 Conclusions

In this chapter, an ESC based LCL filter resonant frequency estimation scheme is firstly proposed. By injecting an HF signal into the LCL filter, the proposed scheme can provide an online estimation of the actual resonant frequency. Compared with the conventional recursive based estimation scheme, the proposed ESC based estimation scheme can provide an accurate estimate with much reduced computational complexity. In practice, the selection of the amplitude of the injection signal is important. A high amplitude injection signal can enhance the convergence speed of the estimation scheme. However, the steady-state inverter output power quality will be deteriorated. On the other hand, a low amplitude injection signal can maintain a high steady-state inverter output current quality at the cost of dynamic performance. In order to tradeoff between the dynamic response and the steady-state power quality, based on the proposed ESC based

estimation scheme, an AESC based LCL filter estimation scheme is presented. In the AESC scheme, the amplitude of the injection signal is adaptive. When the estimated resonant frequency is away from the actual resonant frequency, the adaptive law can actively enlarge the amplitude of the injection signal to improve the convergence rate. When the estimated resonant frequency is close to the actual resonant frequency, the adaptive law can automatically reduce the amplitude of the injection signal to improve the steady-state inverter output power quality. Thus, both the dynamic performance and the steady-state power quality are satisfactory. The stability, accuracy, and the design of the proposed scheme have been discussed in detail. Comprehensive simulation and experiment studies have been performed to validate the effectiveness of the proposed scheme.

4.7 References

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CHAPTER 5

CONCLUSIONS AND FUTURE RESEARCH WORK

In this chapter, the objectives of this dissertation are reviewed, and the conclusions of the research are illustrated. Moreover, the potential future research work on this topic is presented and discussed.

5.1 Conclusions of This Dissertation

This dissertation has developed three reliability enhancing control schemes for the two-stage grid-tied inverter. The two-stage grid-tied inverter system has been widely adopted in the PV generation systems, however, there are reliability challenges remaining, which are,

- DC-dc stage voltage tracking and stability under CPL.
- DC-link capacitor degradation.
- LCL filter resonant frequency drifting.

All these challenges will deteriorate the robustness and reliability of the two-stage grid-tied inverter system. The proposed control schemes could solve the reliability challenges, and the effectiveness of the proposed solutions has been comprehensively verified through theoretical analysis, simulation, and experiments. Based on the aforementioned challenges and proposed solutions, the following detailed conclusions for each challenge can be summarized:

In chapter 2, a UDE based voltage control scheme has been proposed for the DAB dc-dc converter. The proposed control scheme could notably enhance the disturbance rejection performance of the voltage control. Besides, the UDE based voltage control scheme could also enlarge the converter stable margin under the CPL. Rigorous stability analysis and comprehensive experimental studies have validated the effectiveness of the proposed voltage control scheme.

In chapter 3, an HF signal injection based dc-link capacitance estimation scheme for the DAB converter has been presented. By injecting an HF signal into the dc-dc converter output current, the proposed scheme could provide the online estimate of the actual dc-link capacitance based on the HF response. The deadtime effect has been analyzed, which may lead to the phase-shift angle distortion and result in estimation inaccuracy. Then a deadtime compensation scheme is proposed and integrated with the capacitance estimation scheme to further enhance the estimation accuracy. Both HIL and experimental studies have demonstrated the performance of the proposed estimation scheme.

In chapter 4, an HF signal injection based LCL filter resonant frequency estimation scheme is presented. Starting from the concept of the ESC scheme, and ESC based LCL filter resonant frequency estimation scheme is firstly presented. The proposed estimation scheme can provide the online estimate of the LCL filter actual resonant frequency, which can be impacted by the component tolerance and the grid-side impedance. Besides, an adaptive law is proposed and integrated with the ESC based estimation scheme. The proposed AESC based estimation scheme could actively adjust the amplitude of the HF injection signal, and a satisfactory tradeoff between the dynamic response of the estimation scheme and the steady-state inverter output power quality can be achieved. Comprehensive experimental studies have been performed to validate the functionality of the proposed scheme.

Thus, the proposed reliability enhancing control algorithms could effectively solve the reliability challenges and notably improve the reliability of the two-stage grid-tied inverter system.

5.2 Future Work

In this dissertation, three control schemes are proposed to solve three reliability challenges of the two-stage grid-tied inverter system. Based on the presented work, future research efforts could

be performed to further enhance the reliability performance. The possible future works are listed as follows:

- The proposed UDE based voltage control scheme for the DAB converter requires two feedback signals: output voltage and load current. The load current feedback relies on the current sensor, which will increase the hardware cost and may limit the implementation of the proposed scheme in low-cost applications. Thus, one of the future works could focus on the development of the current-sensorless UDE based voltage controller for the DAB converter to further reduce the hardware cost. A current observer could be implemented to replace the actual current sensor and provide the load current to the proposed UDE based voltage controller.
- The developed dc-link estimation algorithm focuses on the estimation of the dc-link capacitor between the dc-dc stage and the dc-ac stage, i.e., the output capacitor of the DAB converter. However, the input capacitor of the DAB converter also suffers from the capacitance degradation. Thus, one of the future works could be the development of the capacitance estimation scheme that can estimate both the input capacitor and the output capacitor of the DAB converter.
- The proposed LCL filter resonant frequency scheme could provide the online estimate of the actual resonant frequency. Thus, one of the future works could be the design of the active damping scheme based on the proposed resonant frequency estimator. Based on the online estimate of the actual resonant frequency, the active damping scheme could further enlarge the stable margin of the grid-tied inverter system.