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Etching of Silicon Wafer in Preparation of Graphene Transfer

Floyd T. Lancaster III
University of Arkansas, Fayetteville

Etching of Silicon Wafer in Preparation of Graphene Transfer

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Floyd T. Lancaster III
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Paul M. Thibado, Ph.D.
Thesis Director

Tacy Joffe-Minor, Ph.D.
Committee Member

Stephen R. Skinner, Ed.D.
Committee Member

Abstract

Following the research done on graphene looking at its unique properties it has been found that graphene can be used as a varying capacitor. What has been observed is that graphene acts almost like a torrential ocean constantly fluctuating. What we use is a silicon wafer with multiple etched layers to create a stable platform on which to capture this energy. In this paper we will discuss the general setup and step-by-step procedures required to create a functioning variable capacitor out of graphene, gold, and Silicon dioxide (SiO2) substrate. Electron Beam Lithography (EBL) is used to create the initial design after which the sample undergoes an etching process in order to adjust the tips to the proper height so that the graphene does not make contact while also balancing the etch time so that the trenches, which will carry the current, aren't destroyed during the process.

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Introduction

For this thesis, my research followed the work of Dr. Millicent Gikunda under the supervision of Dr. Paul Thibado. My goal was to understand the research and techniques described by Dr. Gikunda and to apply them for further research and development. The particular paper I followed was “Array of Graphene Variable Capacitors on 100 mm Silicon Wafers for Vibration-Based Applications” . Specifically, I looked into recreating a viable sample that could be used as a potential energy source. As described by Dr. Thibado and his research team in the paper “Fluctuation-induced current from freestanding graphene”, it was found that a thin sheet of graphene fluctuates in a wave like fashion which when laid upon the design described can act as a variable capacitor as the electrons in the graphene pushed-pulled on the electrons of the corresponding tips. The design of the sample is that of a well and trench arrangement where a tip is formed inside the well and acts as the point of influence when graphene is suspended above it as shown in the Figure 1.

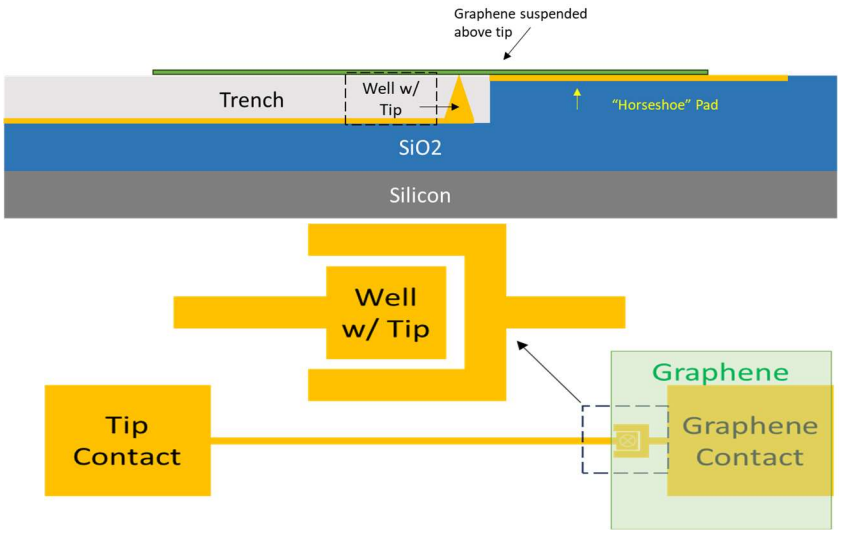


Figure 1: (a) Side view of Sample, top and (b) Top view of Sample, bottom

More details as to how this structure is fully developed is shown in the Fabrication section. For my part, I focused on the development of the samples up to what is called “Layer 2”. This nomenclature comes from the chip designed by the previous researchers and how the software program K-Layout, shown in Figure 2, defined each of the layers of the chip’s development. For quick reference Layer 1 is where the Trench, Well, and Tip is developed. Layer 2 is the creation of the graphene contact pad and the “horseshoe” shape that surrounds the well. Layer 4 is actually the first process of creating the samples by which the alignment marks are created. These alignment marks are crucial to the development as a whole. The Layers 1 and 3 are not used by us, but were a part of the initial design when created by the K-Layout software. Below is an image from the software to show the chips desired outcome when finished with all layers, but without graphene.

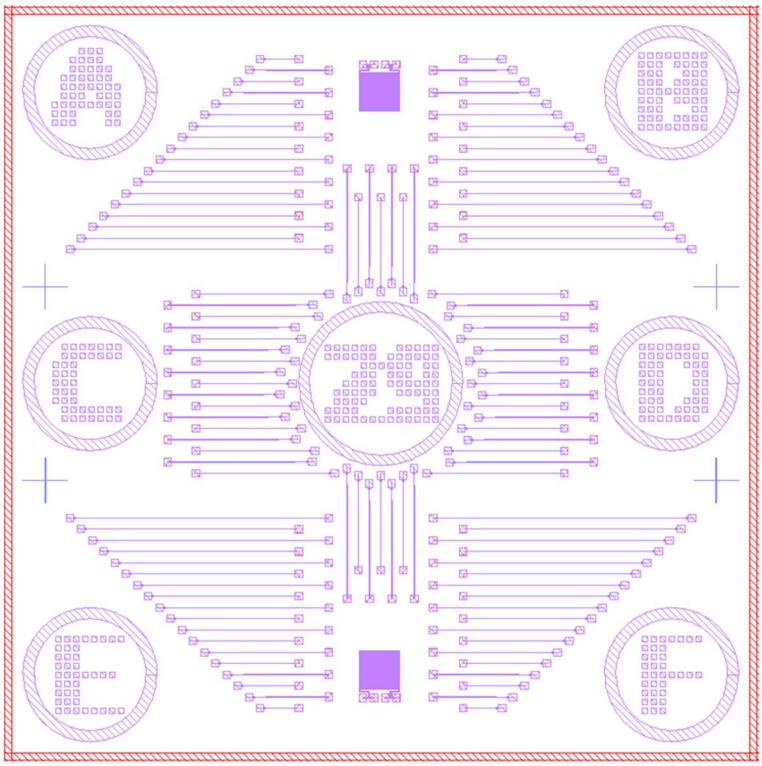


Figure 2: K-Layout of Sample

Note that the trenches are of different lengths, this “slanted” look outlined in red in Figure 3 is the intended location of the graphene transfer.

Figure 3: Close up view of trench ends for graphene placement.

This helps in creating different potentials from the graphene suspended above. I worked specifically on only developing Layers 1, 2, & 4 for only one corner at a time as the process is both time consuming and also allows for adjustments between each sample trial. By only focusing on one corner at a time, a complete trial run could be completed on a single sample chip and if it failed, then there were three more corners to attempt. This was also done to conserve wafers so that there was less waste in the long run.

Consideration of Materials

When finding the proper wafer, several considerations were made. The wafer that was ultimately selected by Dr. Thibado was University Wafer ID: 2570. The wafer is 100mm at its widest with both a primary and secondary flat side which are parallel to each other and perpendicular to the primary cutting path. It is an n-type wafer with Miller indices of (100). The Miller index is a system created by William Hallowes Miller for defining the planes of a crystalline structure and notating proper cutting planes. For this wafer having an index of (100), this means that proper cuts can be made along the x-axis slicing through the yz-plane. The design of this lattice structure allowed breaking points, meaning that once a cut is made into the lattice, the sample would break along a single plane allowing square samples from an otherwise rounded wafer. The primary crystal was a single crystal of silicon coated with an amorphous silicon dioxide layer.

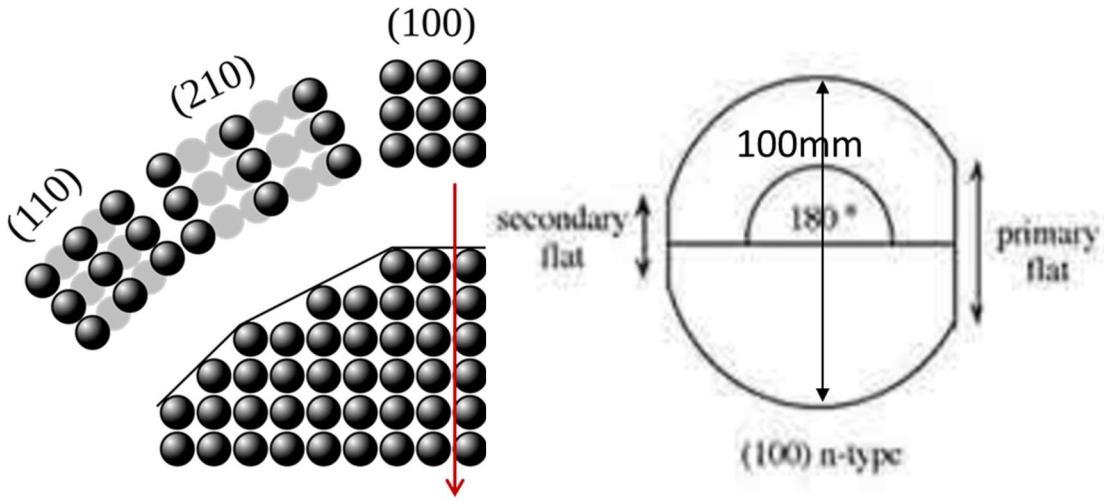


Figure 4: (a) surface density of atoms for a monoatomic simple cubic crystal, left (b) schematic of SiO_2 wafer shape and orientation (Dang)

This cutting process is better known as cleaving. Cleaving is a low-energy fracture that propagates along well-defined low-index crystallographic planes known as cleavage planes. If

we were to look at a 3D representation of the Si lattice structure it would look more hexagonal from one angle, yet square from another.

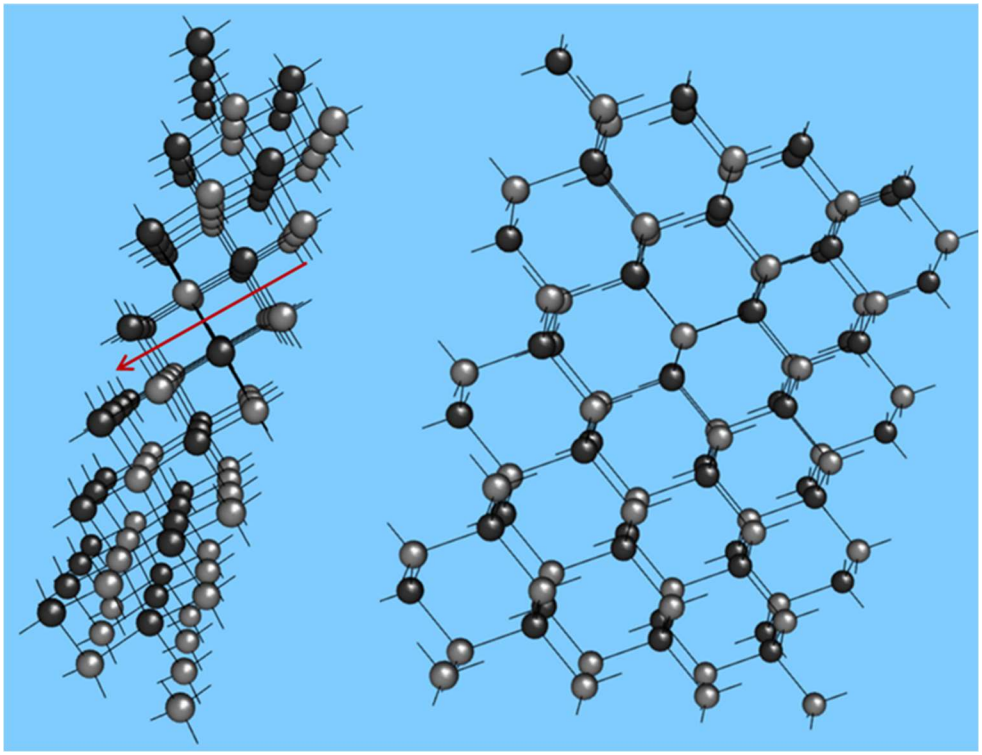
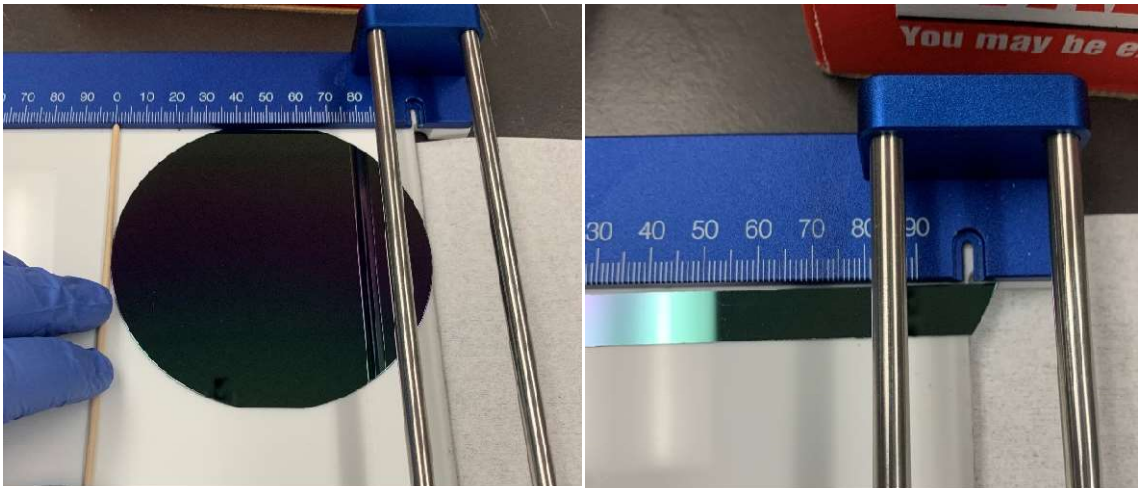


Figure 5: Silicon Lattice from top and side view (Demidov & Drozdov)

The red arrows on the previous Figures 4 and 5, indicate the planes along which cleavage occurs. The exact process of cleaving the samples is discussed in the Fabrication section. The use of amorphous SiO_2 on the surface allowed us to etch the sample using buffered-oxide etching post electron-beam lithography to develop the desired well-trench-tip structures we desired.

Fabrication

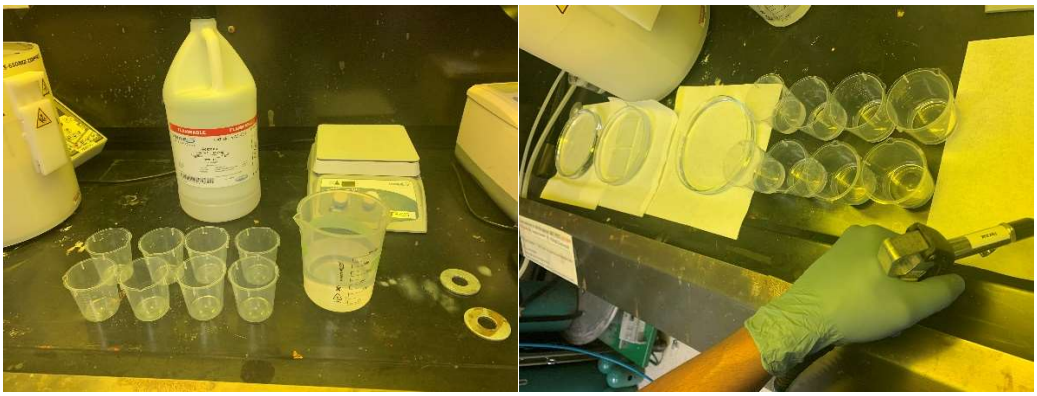
The initial step is to cut a sample chip from the larger wafer. Great care is taken when handling any part of the wafer as any slight defect created from the cutting/cleavage stage will be present throughout the rest of the process. The individual chips are initially cut 1cm by 1cm to allow for easier manipulating of the sample/chip and gives a greater room for error in handling the sample. The cutting process is performed using a cutting board with a diamond tip cutter. The wafer is lined up so that the longer flat side of the wafer is flush to the guide rail of the cutting board which also allows for a more accurate measurement of the initial cut. Once a "slice", or initial cut from the wafer, is made that slice is then lined up against the guide rail of the cutting board as shown in the figures below.



Figures 6: Cleaving of SiO_2 wafer

From the slice an additional cut is made to remove the curved section of the slice as it is unusable and "squares" the rest of the slice to make easier to measure and cleave. The diamond cutter does not actually cut all of the way through the sample, instead it cuts through the SiO_2 and creates a cleavage plane in the silicon from which gently applied pressure allows us to break off the desired chip.

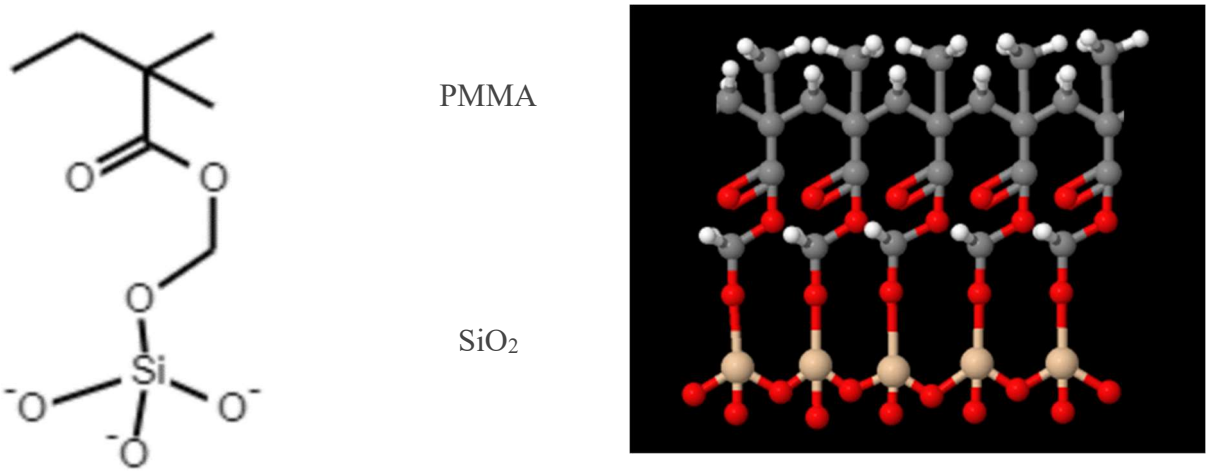
Once the chip has been cleaved from the sample it is likely dirty from microscopic debris and will need to be cleaned. Rather than simply using an air gun which may scratch the surface further by pushing the debris, the sample are placed in acetone which allows the debris to be more gently removed and also allows for any other possible contaminants to be removed.



Figures 7: Cleaning setup for wafer preparation

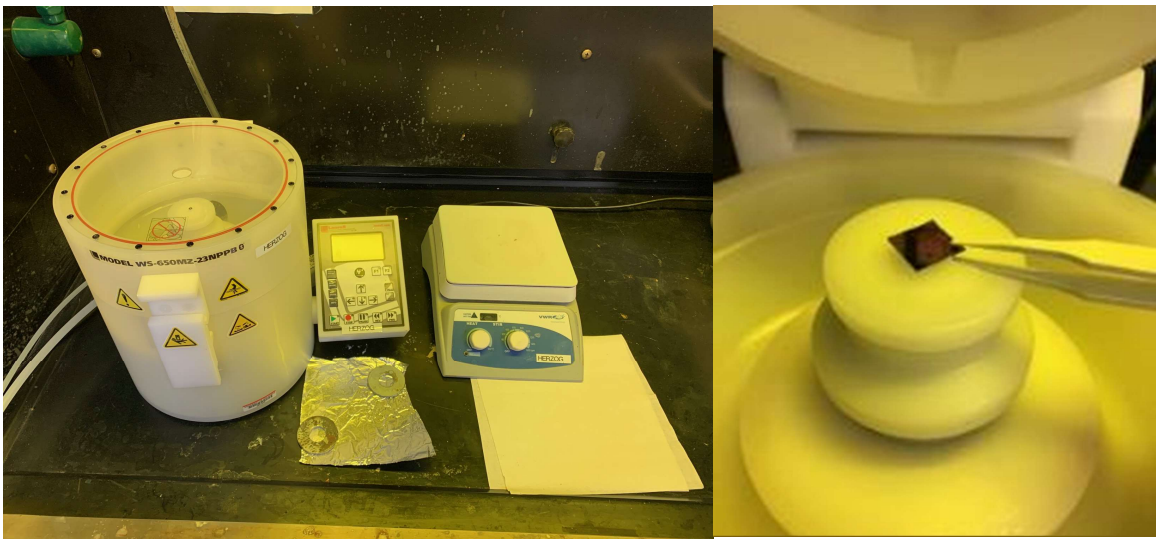
After it is soaked in acetone it is given an isopropyl alcohol rinse to remove any remaining acetone and then immediately dried using a nitrogen air gun. If organic contamination is suspected then it is sent into an oxygen plasma cleaner, though this was rarely the case.

Once the sample is deemed clean, it is then prepped for Layer 4, the alignment marks. The alignment marks are vital as they are the guidance marks for the EBL software which uses them write later layers, ergo a poor alignment mark means that the sample can be worthless. In preparation for the EBL the chip is spin coated using PMMA: Poly(methyl methacrylate). The PMMA bonds to the SiO2 as shown in Figure 8.



Figures 8: Chemical structure of bonding between PMMA and SiO2 Wafer

The spin coating process allows for the PMMA to spread across the sample so that there is an even distribution of the PMMA. This is an important step as too much PMMA can prevent a successful write, and too little can allow damage the SiO_2 layer during etching.



Figures 9: (a) Setup of hot plate and spin coater, left

(b) placement of sample onto vacuum of spin coater, right

The sample is initially heated on a hot plate (Figure 9a) to 180˚C for five minutes. This ensures that there is no moisture remaining on the chip. After the chip is baked, it is allowed to cool for one minute, and from there it is placed into the spin coater as shown in Figure 9b and held in

place by a vacuum produced by the spin coater. A dropper is used to place the PMMA onto the chip such that the PMMA is covering the entire sample. At this point the spin cycle begins and the sample is spun at 1500rpm for one minute. The film/PMMA thickness is approximated by

$$h_f \propto \frac{1}{\sqrt{\omega}}$$

Where h_f is the film thickness and ω is the angular velocity of the spinner. Once the sample chip is removed from the spin coater the sample is again placed onto the hot plate for another 5min. to allow the PMMA to fully dry and is again allowed to cool for one minute.

Now that the sample is coated in PMMA it is ready for EBL. This step is actually performed by a specialist in another lab group as it is a complex process. Electron-beam lithography differs from photo-lithography in that where photo-lithography requires a mask and the areas exposed to the light are scribed, EBL uses a stream of electrons and exposes only certain areas of the sample to disrupt the bonds of the PMMA/SiO_2. The EBL machine used actually moves the sample inside rather than moving the beam. The sample is placed onto a cassette and loaded into the machine. From there the specialist can program the EBL to write a particular pattern into the PMMA.

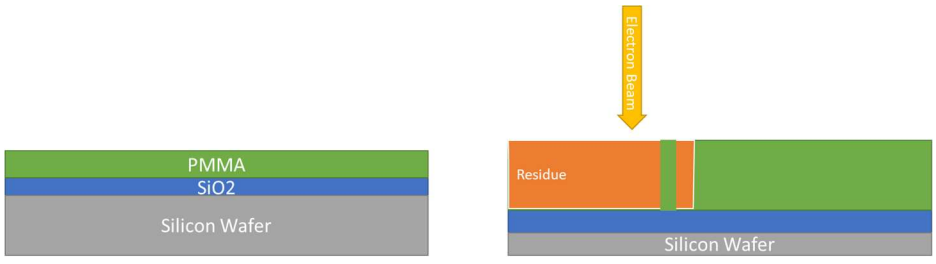


Figure 10: (a) side view of sample before EBL, left (b) side view of sample during/after EBL

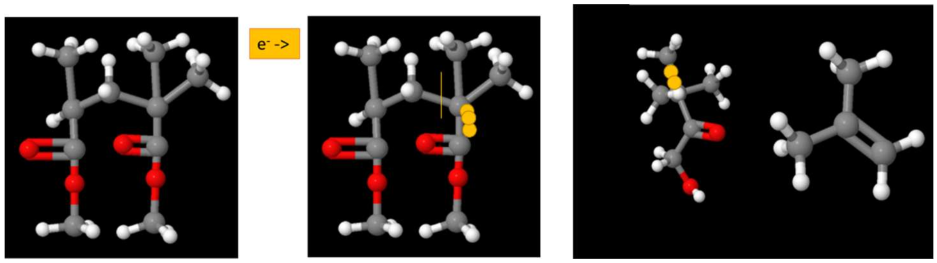


Figure 11: (a) atomic structure before EBL, left (b) atomic structure as EBL takes place, middle (c) atomic structure after EBL, right

As shown in Figure 11, the EBL breaks the bonds at the points indicated in yellow on the figures. This residue of unwanted molecules needs to be removed so that the chip can processed further. We develop the chip by “washing” away this residue using a combination of Methyl isobutyl ketone (MIBK) and isopropanol (IPA) at a ratio of 1:3 respectively for one minute, then it is rinsed with isopropanol for 10 seconds.

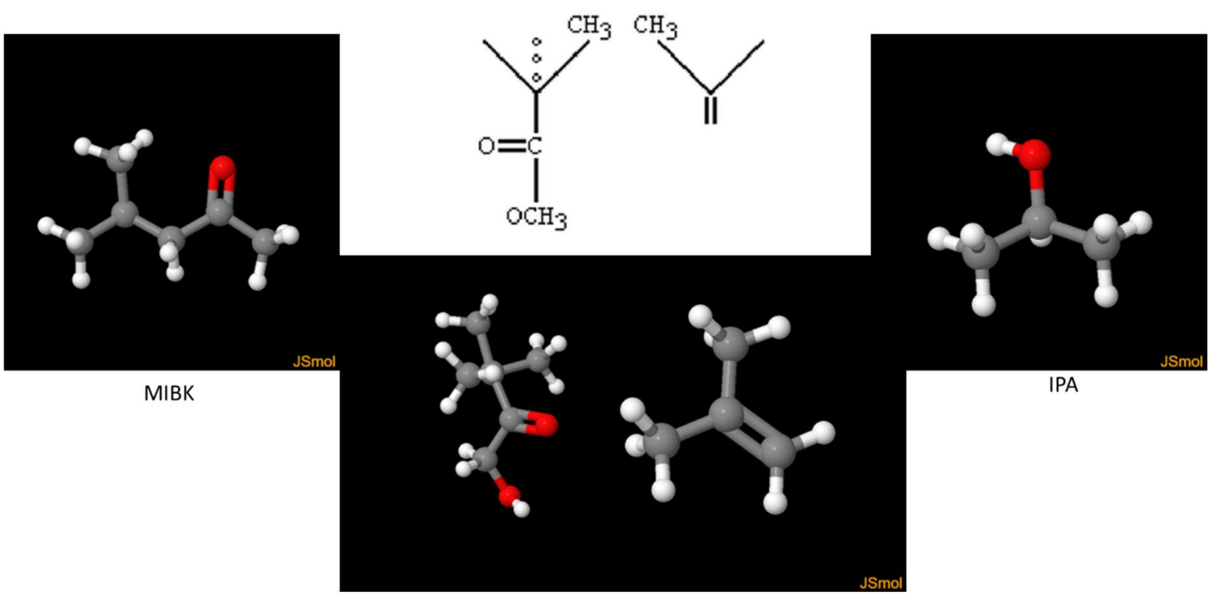


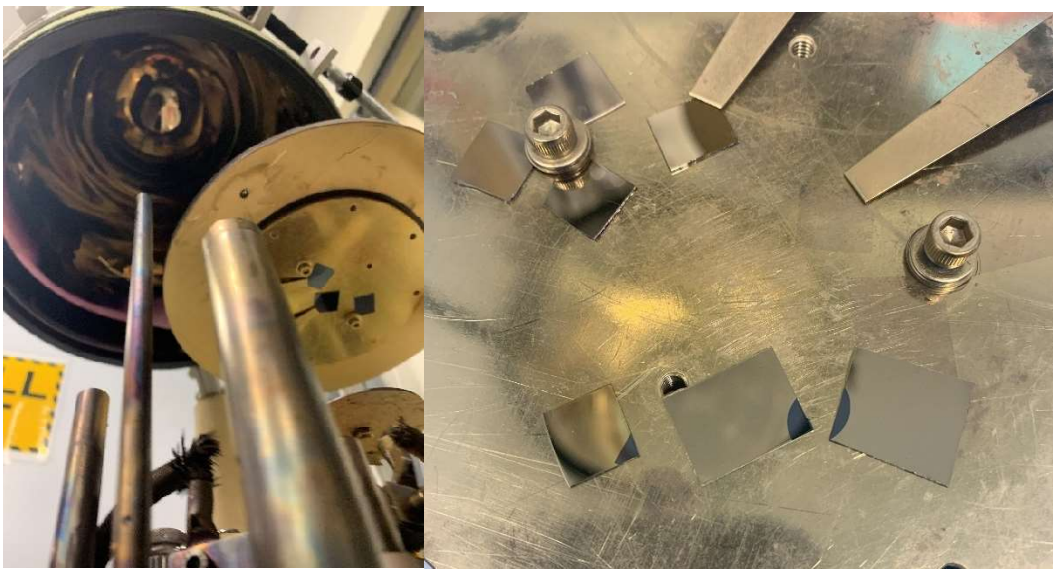
Figure 12: Molecular size comparison of MIBK and IPA compared to the residue remaining from EBL

The MIBK and IPA essentially push the impurities out of the written areas rather than actually interacting with the debris leaving the silicon layer exposed. The next image, Figure 13,

is a real example of what the sample will look like after having Layer-4 written and post development. It is a stitched picture taken at 5X magnification under the microscope. Now that the pattern has been written onto the chip, it becomes necessary to prevent it from disappearing. We do this by using gold deposition. Note: the markings are 0.6mm each way.

Figure 13: Deposition of Au and Cr

During gold deposition 5nm of chromium is placed followed by 50nm of gold. The chromium acts as a binder between the gold and the SiO_2 layers through the process of metallization, otherwise the gold would not stick to the chip. The process of deposition is done by mounting the sample to a holding plate inside the deposition machine shown in Figure 15a. Here the inside pressure is reduced to ~$5x10^{-6}$atm with aid of liquid nitrogen. Once the sample is set and the proper vacuum is reached, a sample of the metal to be deposited is electrically heated to the point of vaporization. It is this vapor which coats the sample; however, it is not a direct deposition in that the entire sample is coated with the metal(s) used as shown in Figure 14b.



Figures 14: (a) Samples in evaporator, left (b) samples after Au and Cr deposition, right

Since the sample is completely coated, the excess metal needs to be removed so that the sample can be processed further. We do this by using acetone to remove the PMMA that the metal has bonded to by soaking it overnight in acetone. This process is called Liftoff. After the sample has had a chance to soak, we use either an acetone squirt bottle or a syringe to push or "lift" the gold off of the sample depending on how well the acetone was able to soak through the PMMA. Figure 15 shows a loosened gold layer on the sample that is lifted off by acetone.

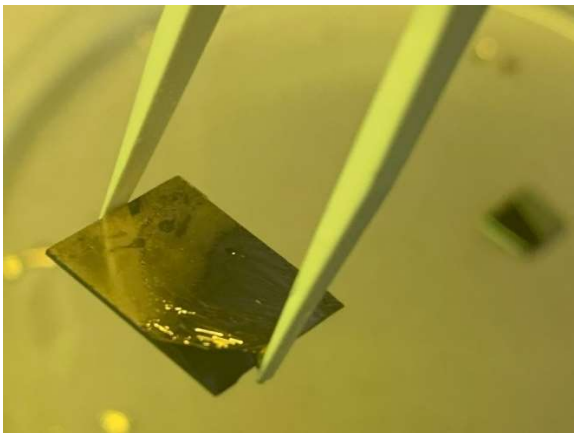


Figure 15: Au layer being removed by acetone

Once all of the excess metal is removed the sample is rinsed with IPA and again dried using nitrogen. The resulting chip now has four permanent crosshairs for aligning the coming layers, one of these post deposition marks is shown by Figure 16.

Figure 16: Marks after Au deposition with measurements

Now that the chip has alignment marks it is again coated with PMMA and sent for Layer 1 to be written. Layer 1 is the creation of the contact points, trench, well, and tips. The chip is sent to the EBL for the writing, however after development there are several steps to be taken prior to deposition. Once developed, the chip is then imaged optically to check for defects using a desktop microscope. If it appears to be a good write then the sample is submersed in buffered-oxide etch (BOE) for 10.5 minutes. This step is etching the SiO_2 where the PMMA residue is removed during development. While the contact points and trenches are fairly straight forward, it is the development of the well tip that is important. Too high and the tip will touch the graphene causing a short, and too low and there will be an open circuit. The etching process isotopically

creates the tip inside the 5µm by 5µm well which was initially a square “hat” created during exposure. It is easier to see this by using the K-Layout schematic.

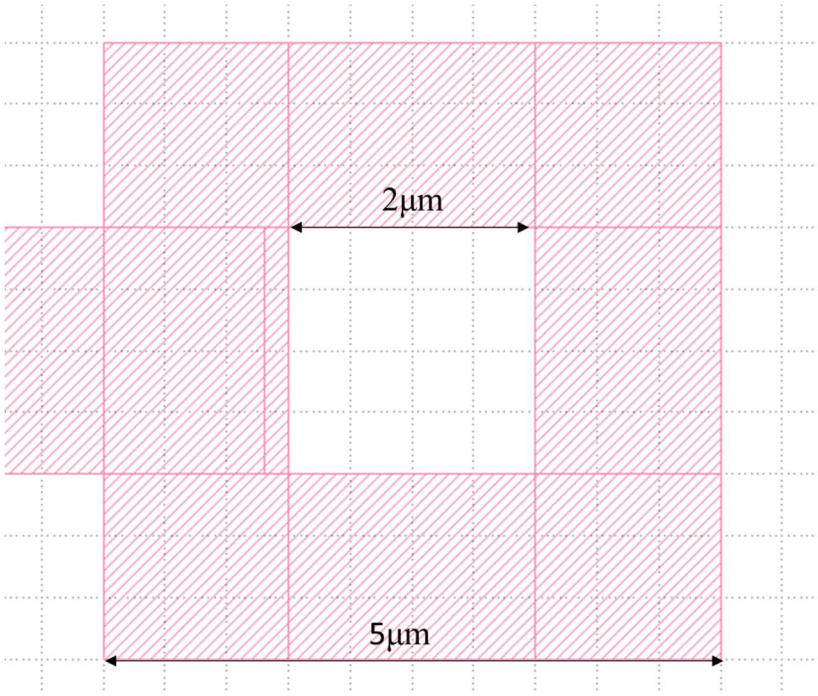


Figure 17: K-Layout top view of etching

The blank 2µm area in Figure 17 is where the tip will present itself once the etching has been completed (Refer to Figure 19a for optical view). Typically, the tip is 1.5µm from the surface once the etch is complete. Once the chip is finished with the BOE it is then dipped into a two-stage deionized water bath, the first stage is immediately after the BOE to rinse off the acid and the second allows the chip to stay submersed for another minute to ensure neutralization of any lingering acid. The setup is displayed by Figure 18.

Figure 18: Setup for etching

After the etch is completed, it is necessary to look at the tip to ensure that it is where it needs to be. This is done initially with an optical microscope where we look to see if a tip has formed and to also check the other structures for defects.

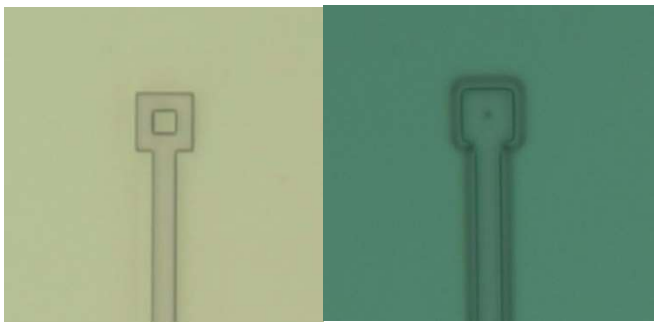
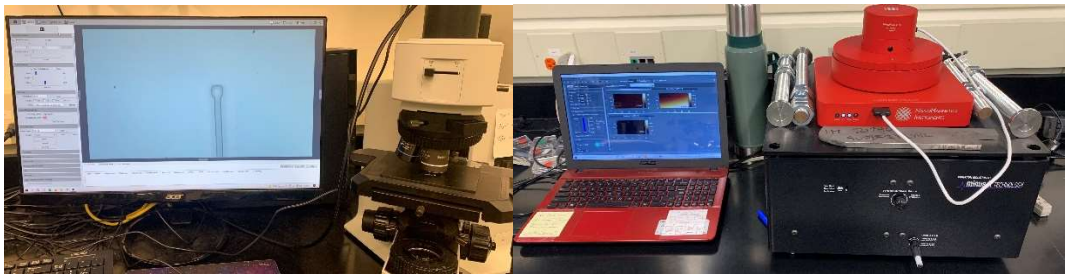


Figure 19: (a) tip pre-etch, left (b) tip post-etch, right

Once it is confirmed that a tip is present (Figure 19b) atomic force microscopy (AFM) is then used to check the tip height to ensure a viable tip is present. Multiple tips are checked during this process for comparison. Knowing PMMA thickness is prevalent during this process as the AFM will read from the "surface", or where the PMMA is, to the well bottom and again to the top of the tip. The equipment setup for this process can be found in Figure 20. As stated, the desired tip height should be no closer than 1.5μm from the surface of the SiO_2 meaning we have to include the PMMA thickness into calculations.



Figures 20: (a) optical view of tip, left (b) AFM setup

If the tips are at the desired height the next step is for preparation of Layer 2. This layer adds in the contact pads and “horseshoe” structure upon which the graphene is meant to be placed. This is done by first writing the pattern and then deposit gold/chromium again followed by liftoff and then reimaged with both the optical microscope and AFM to ensure proper tip height. If successful the sample is then ready for graphene transfer. Figure 21 shows the chip once layer 2 has been written in preparation for graphene transfer.

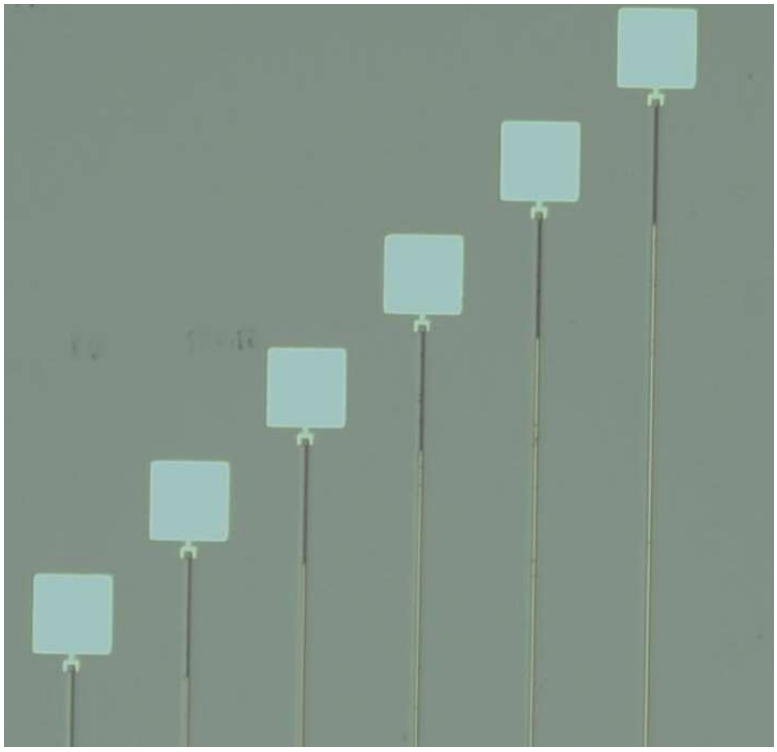
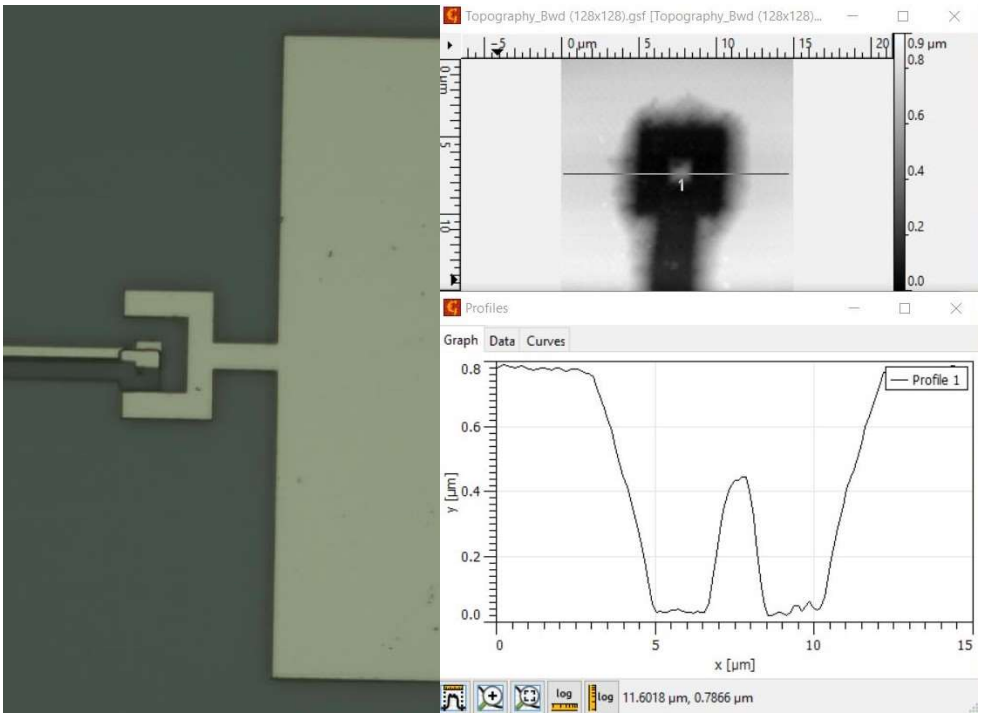


Figure 21: Final result of tips with layer two

Results

While I did have two samples make it to Layer 2 and of those one to graphene transfer, which was not discussed as the sample was given to a student who was more practiced at transfer, none of them of them ended up being viable test samples as variable capacitors as hoped. One sample became shorted during transfer, the graphene had folded into the tips and was unusable. The other was a mechanical failure from the EBL and unfortunately affected myself as well as many others. Other set backs came from a lack of practice, leaping before I looked. I was fortunate enough to succeed in getting two samples to Layer 2 and became knowledgeable in the use of various equipment and techniques required to complete the process. Below are some images from the microscopes show casing some success and failure.



Figures 22: (a) optical view of mechanical error resulting in mechanical failure, left (b) AFM results of the same tips, right

The picture on the left is from the mechanical failure and the image on the right was the AFM image of the same sample prior to Layer 2.

Condensed Step-by-Step:

1. Cleave sample
    a. Clean sample in acetone 10 minutes.
        i. Rinse with IPA
        ii. Dry with nitrogen gun.
2. Spin-coat
    a. 5 minutes bake
    b. 1 minute cool
    c. Spin
    d. 5 minutes bake
    e. 1 minute cool
3. Layer 4: the alignment marks are written
    a. Exposure via EBL
    b. Develop post EBL
4. Gold deposition
    a. Liftoff
5. Spin-coat following previous method
6. Layer 2: Well, Trench, Tip Exposure
    a. Develop
    b. Check visually with microscope
7. BOE for 10.5 minutes
    a. Double bathe using unionized water
        i. Quick dip into first bath, 1minute rest in second bath
8. AFM
    a. Using both optical microscopy and atomic force microscopy, check tip height
9. Layer 2 Exposure
10. Gold Deposition
    a. Liftoff
11. Optical Microscopy Inspection

If the steps go properly, then the sample is ready for further testing.

References

1 Gikunda, M., Harerimana, F., Mangum, J. M., Rahman, S., Thompson, J., Harris, C. B., Churchill, H., & Thibado, P. (2022). Array of Graphene Variable Capacitors on 100 mm Silicon Wafers for Vibration-Based Applications. *Membranes*, *12*(5), 533. https://doi.org/10.3390/membranes12050533

2 Thibado, P. M., Kumar, P., Singh, S., Ruiz-Garcia, M., Lasanta, A., & Bonilla, L. L. (2020, October 2). *Fluctuation-induced current from freestanding graphene*. Physical Review E. https://journals.aps.org/pre/abstract/10.1103/PhysRevE.102.042101

Figure 4 by Dang, C. (n.d.). *File:cristal densite surface.svg*. Wikimedia Commons. https://commons.wikimedia.org/w/index.php?curid=5923268

Figure 5 by Demidov, E., & Drozdov, Y. (2011, October). *3D Solid State Crystal Models*. 3D crystal models. https://www.ibiblio.org/e-notes/Cryst/Cryst.htm