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Advanced CMOS Process for Submicron Silicon Carbide (SiC) Device

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Abstract

Silicon carbide (SiC) is a wide semiconductor material with superior material properties compared to other rival materials. Due to its fewer dislocation defects than gallium nitride and its ability to form native oxides, this material possesses an advantage among wide band gap materials. Despite having several superior properties its low voltage application is less explored. CMOS is extremely important in low voltage areas and silicon is the dominant player in it for the last 50 years where scaling has contributed a major role in this flourishment. The channel length of silicon devices has reached 3 nm whereas SiC is still in the micrometer (2 μm/ 1.2 μm) range. So, SiC technology is still in its infancy which can be compared with silicon technology in the mid-1980s range. When the SiC devices would enter into the sub-micron and deep submicron range, proper device design in those ranges is necessary to rip the benefit of scaling.

In this thesis, the SiC CMOS process available from different institutes and foundries is discussed first to understand the current state of the art. Later, low-voltage conventional SiC NMOS devices in the submicron range (2 μm to 600 nm) are simulated and their key parameters and performances are analyzed. In the submicron range, one major issue in MOSFET scaling is hot carrier effects. Thus to minimize this effect, a low-doped drain (LDD) region is introduced in the conventional SiC design having a channel length of 800 nm and 600 nm. In comparison with conventional designs, LDD designs have shown better saturation current behavior, reduced threshold roll-off, reduced hot electron current density, minimized gate leakage, reduced body hole current, enhanced voltage handling capability, reduced electric field, and improved subthreshold behavior in SiC. In the end, spacer technology, dopants, doping methods, and LDD realization technique in SiC are discussed.

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Chapter 1. Introduction

1.1 Silicon Carbide as a Material

Silicon carbide (SiC) was discovered in 1824 by Jacob Berzelius, a scientist, famous for his discovery of silicon in Sweden [1]. During the experiment in his lab, he assumed a chemical bond between silicon and Carbon. Later in 1891, near Pittsburgh, Edward Goodrich Acheson, an American chemist, mixed silica and coke in a furnace and found one of the hardest and crystalline materials that can substitute diamond [1]. He named the material 'carborundum' as it was a compound of carbon and silicon and gave the proper formula as SiC. Two years later, in 1893, Henry Moissan found SiC as one of the rarest minerals on the earth in meteorite form and patented it as a highly effective abrasive [2]. According to his name, mineralogists termed it SiC moissanite [1]. To date, SiC is one of the best and most used abrasives in the world which has a hardness of 9.5/10 (on the Mohs scale), almost comparable to diamond where the diamond is the hardest material on earth having a hardness of 10. Not only as an abrasive, but SiC was also a part of many technological inventions such as light emitting diode (LED) in 1907, body armors, telescopes, and electronic elements, all of which share a form of SiC [1].

SiC has grabbed attention as a wide band gap material (WBG) due to its superior material properties compared to other rival materials used in the electronics industry. Depending on the sequence of silicon and carbon atom, SiC can have more than 250 polytypes out of which 6H-SiC, 4H-SiC, and 3C-SiC are the most popular [3]. Among these three, 4H-SiC is mostly used in the commercial perspective (as high power, high-frequency, and high-temperature device) due to its higher mobility, higher bandgap, isotropic nature, and availability of large wafer size.

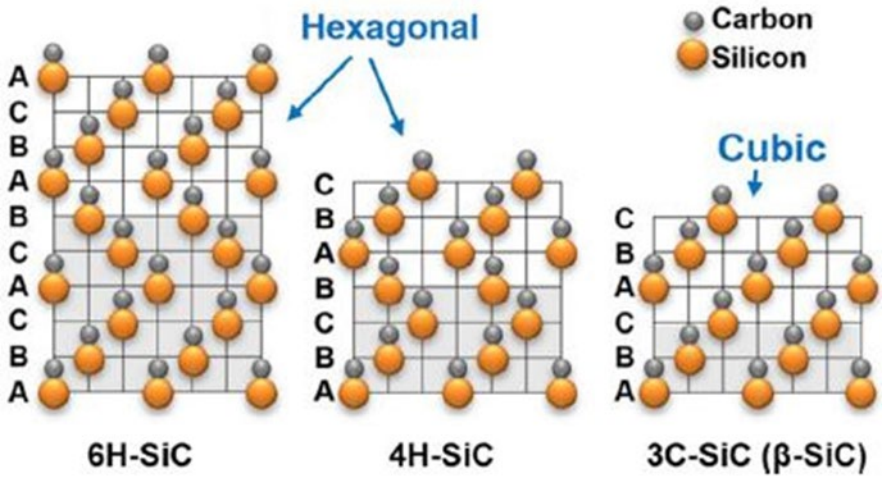


Figure 1.1 The stacking sequence of 6H-SiC, 4H-SiC, and 3C-SiC [4]

Some material properties of SiC and other important semiconductors are summarized in Table 1.1 [3]. From Table 1.1, compared to Si, it can be seen that 4H-SiC has a three times wider bandgap (E_g), three times higher thermal conductivity (λ), two times higher saturation velocity (V_{sat}), ten times higher critical e-field (E_c). SiC has a unique advantage i.e. its native oxide (SiO_2) can be thermally grown similar to silicon technology. Another major advantage of SiC MOSFET is as temperature increases from room temperature (25 °C) to 135 °C, its on-resistance increases by only 20% compared to Si MOSFET which increases by 250% [3].

Table 1.1 Material properties of SiC and other semiconductors [3]

Material	**E_g [eV]**	**n_i [cm^{-3}]**	**ϵ_r**	**μ_n [$cmV^{-1}s^{-1}$]**	**E_c [MV/cm]**	**V_{sat} [10^7 cm/s]**	**λ [$Wcm^{-1}K^{-1}$]**
Si	1.12	$1.5*10^{10}$	11.8	1350	0.3	1.0	1.5
Ge	0.66	$2.4*10^{13}$	16	3900	0.1	0.5	0.6
GaAs	1.4	$1.8*10^{6}$	12.8	8500	0.4	2.0	0.5
GaN	3.39	$1.9*10^{-10}$	9.0	900	3.3	2.5	1.3
3C-SiC	2.2	6.9	9.6	900	1.2	2.0	4.5
6H-SiC	3.0	$2.3*10^{-6}$	10	370^a, 50^c	2.4	2.0	4.5
4H-SiC	3.26	$8.2*10^{-9}$	9.7	720^a, 650^c	3.0	2.0	4.5
Diamond	5.45	$1.6*10^{-27}$	5.5	1900	5.6	2.7	20

1.2 Importance of SiC CMOS

A Complementary Metal Oxide Semiconductor (CMOS) is named as it uses two complementary transistors (PMOS and NMOS) in its circuits. In comparison to NMOS technology, although CMOS technology is more complex in terms of device physics and fabrication issues, it is still the most dominant integrated circuit (IC) technology. Unlike an NMOS inverter, in a CMOS inverter, only one transistor (either PMOS or NMOS) turns on at a time. That means when a CMOS inverter is not switching from one state to another state (high to low), a high impedance path exists from supply to ground. As a result, almost no current path exists and thus no dc power is dissipated. Another important feature of CMOS is when the inverter changes its state, the output (V_{out}) swings fully (from V_{dd} to 0 or 0 to V_{dd}), which is referred to as rail to rail. The third advantage of CMOS is when V_{out} swings from rail to rail, it gives excellent noise margins. The fourth advantage of CMOS is as CMOS devices dissipate less power, so the inherent heat generation is less which signifies a more reliable device. Usually, the packaging cost represents 25-75% of total chip manufacturing costs [5]. Since CMOS needs very low power so cheaper packaging technology can be used. Another major advantage is CMOS technology can give a 'static ratioless' logic design. It is termed 'static' because the gates are triggered by a data signal and do not need any external clock signal. Compared to NMOS which depends on the balance of the current ratio between transistors, CMOS design is termed as 'ratio less' because it does not depend on the geometric ratio of p and n-type transistors. A significant problem with NMOS is that its current ratio should be maintained when there is a change in temperature, power supply, and fabrication process. On the other hand, CMOS can give a temperature-independent logic level [6]. Silicon is still the dominant material in CMOS technology mainly due to its maturity of technology, wide research (more than 40 to 50 years),

and low-cost wafers [7]. Although wide band gap technology like SiC is less mature than silicon technology, it is worth pushing the research due to several advantages. The first advantage is the demand for harsh environment electronics [8]. Harsh environment electronics signifies a system that can withstand harsh environments such as high- temperature, high pressure, high radiation, and corrosive gas environments. Such harsh environments can be found in space exploration, turbine engine, nuclear reactor, automobile sector, and so on. The plot in Figure 1.2 signifies the importance of SiC devices.

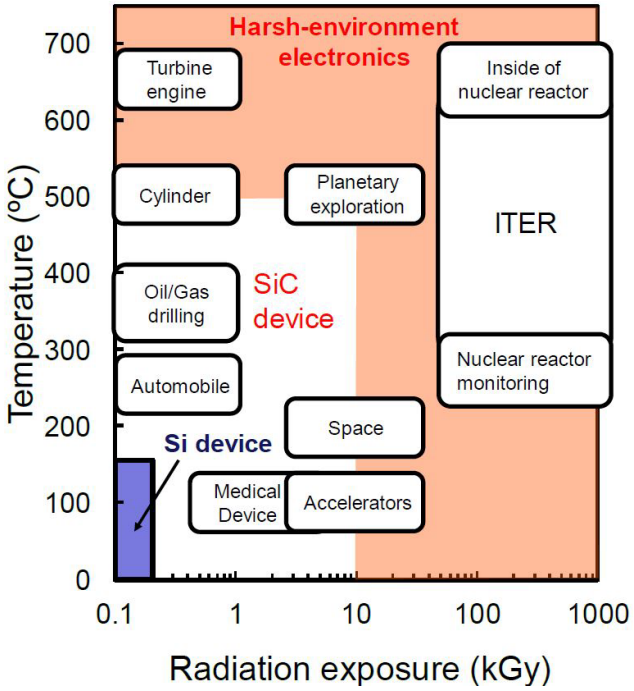


Figure 1.2. Demand for harsh environment electronics [8]

From Figure 1.2 it is clear that silicon technology cannot work at high temperatures. This is mainly because of the abundance of intrinsic carrier density in silicon devices at high temperatures. When the temperature crosses 300 °C, the number of the intrinsic carrier can exceed dopant carriers which signifies a reliability issue. At prolonged temperatures, silicon devices can be degraded or fail to operate and when temperatures cross 600 °C, it is impossible

to design any system with silicon technology [9]. Apart from that, at high temperatures, the control circuit has to reside in a cool area or needs an extra exhaust and cooling system. The cooling system can be air cooling or liquid cooling which adds extra cost and space to a system. In space aircraft, these extra overheads can pose a serious threat and reliability issues. Another significant advantage of SiC is its high-voltage transmission capability. The thickness of its drift region can be reduced by 10 times compared to the silicon device. As a result, SiC devices can be made smaller. Due to the small size of its drift region, the on-resistance decreases. The third advantage of SiC is circuit efficiency. The wide band gap and high breakdown voltage capability of SiC enable faster switching that improves system efficiency. Furthermore, due to the 100 times lower resistance and lower leakage current when the devices stay on and off, the energy losses are minimum compared to silicon devices. This is a significant advantage in hybrid electric vehicles where minimizing energy loss is important and complex cooling systems and heavy heat sinks are undesired. Among the WBG materials, gallium nitride GaN is a competitor of SiC, but SiC bulk crystal has fewer dislocation defects (order of magnitude lower) than GaN. So, SiC is more advanced in important technology areas such as making reliable ohmic contacts, and impurity doping, which are inevitable in CMOS technology. Apart from that, the ability to form native oxide (SiO_2) makes SiC a reliable producer of MOSFET devices [9].

1.3 Importance of Technology Scaling

In the early 1970 scientists from IBM, Intel, and elsewhere decided that due to the production simplicity and low power consumption, MOSFET will facilitate the future growth of complex integrated circuits. This trend was recognized by Gordon Moore in 1965 at Intel. He stated that the number of transistors in an IC will be doubled every 24 months which became the driving force of the IC industry for the last 50 years or more. Due to this fact, the price of semiconductor

memory devices has dropped to 100 million times and the trend continues. This price drop has become the driving force behind new inventions of semiconductor devices. This is possible due to 'miniaturization' which means transistors and interconnects become smaller. Thus more circuits can be fabricated in a small wafer area which in turn reduces the cost, increases the speed, reduces the power consumption, and makes devices smaller and portable. Historically, a new technology node or new generation means a reduction of metal line width. Examples of some technology generation are 180 nm, 130 nm, 60 nm, 65 nm, and 45 nm technology nodes. At each new generation/ node feature size becomes 70% of the previous node. Eventually, 70% of the previous line width means almost 50% of area reduction (0.7 * 0.7 = 0.49), so cost is reduced significantly [10]. On the other hand, historically it has been found that speed increases by around 30% more than its previous nodes in all generations [11].

Table 1.2 Scaling of MOS technology [11]

MOSFET Technology (Gate length)	**Production Year**	**MOSFET Technology (Gate length)**	**Production Year**
10 µm (2D technology)	1971	65 nm	2005
6 µm	1974	45 nm	2007
3 µm	1977	32 nm	2009
1.5 µm	1981	22 nm (3D technology)	2012
0.8 µm	1987	14 nm	2014
0.6 µm	1990	10 nm	2016
350 nm	1993	7 nm	2018
250 nm	1996	5 nm	2020
180 nm	1999	3 nm	2021
130 nm	2001	2 nm	2024 (future trend)
90 nm	2003		

It can be said that scaling has been the most effective technique for the success of the Very Large Scale Integration (VLSI) industry [12]. This semiconductor scaling has been

governed by Robert H. Dennard. In 1980, Dr. Dennard formulated some rules which are known as Dennard's law [13]. Silicon-based devices have been scaled by his classical scaling rules up to 2011. These rules are termed 'constant field scaling' and 'constant voltage scaling'. The details of 'constant field scaling' and 'constant voltage scaling' is mentioned in Table 1.3. In both approaches, device engineers take a device from a current generation and scale it horizontally (gate length) and vertically (junction depth, depletion width, gate oxide thickness) by the same factor. The main aim of this scaling is to get a scaled device that has the same transistor proportions.

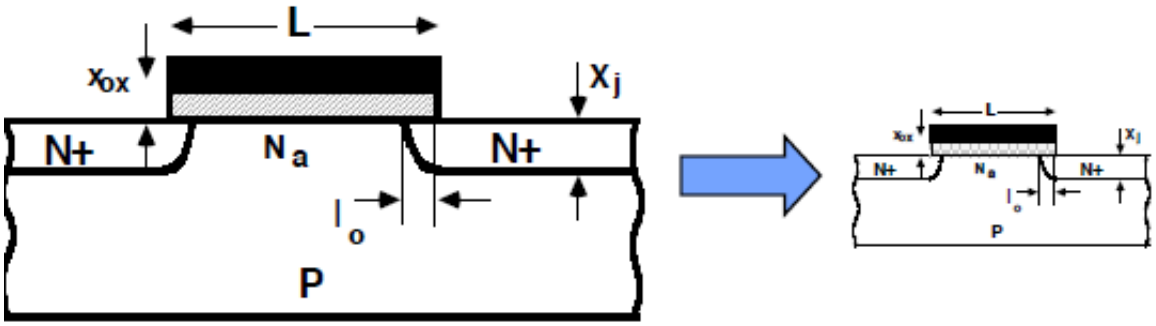


Figure 1.3 Principle of MOSFET IC scaling [14]

When the voltage and all dimensions of a MOSFET are decreased by a factor 'α' and charge densities and doping are increased by the same factor 'α', the e-field remains constant. As a result, the circuit speed is increased by 'α', and density increases by 'α^2'. This is known as constant field scaling. In the case of constant voltage scaling, all MOSFET dimensions are decreased by a factor 'α' except the power supply and terminal voltage. As MOSFET's dimensions are scaled but the voltage is not scaled, this process can lead to some serious issues such as oxide breakdown, electrical stress, and electro-migration. On the other hand, in the case of constant field scaling, the terminal voltages and power supply gets scaled which leads to

another type of problem. The reduction of voltage is not preferred because peripheral circuits and interfaces require a fixed voltage. As a result, multiple power supply is required which is not feasible in many cases. This is why constant voltage scaling is chosen in most cases.

Table 1.3 Constant field and constant voltage scaling [15]

Parameter	**Symbol**	**Constant Field Scaling**	**Constant Voltage Scaling**
Gate length	L	$\frac{1}{\alpha}$	$\frac{1}{\alpha}$
Gate width	W	$\frac{1}{\alpha}$	$\frac{1}{\alpha}$
E-field	ϵ	1	$\frac{1}{\alpha}$
Oxide thickness	t_{ox}	$\frac{1}{\alpha}$	$\frac{1}{\alpha}$
Substrate doping	N_a	α^2	α^2
Gate capacitance	C_g	$\frac{1}{\alpha}$	$\frac{1}{\alpha}$
Oxide capacitance	C_{ox}	α	α
Transit time	t_r	$\frac{1}{\alpha^2}$	$\frac{1}{\alpha^2}$
Frequency	f_r	α	α^2
Voltage	V	$\frac{1}{\alpha}$	1
Current	I	$\frac{1}{\alpha}$	α
Power	P	$\frac{1}{\alpha^2}$	α
Power delay	$P\Delta t$	$\frac{1}{\alpha^3}$	$\frac{1}{\alpha}$

The main purpose of scaling is to maximize current driving capability, mobility, and turn-off speed and at the same time, minimize output conductance. However, some of these properties are contradictory and depends on certain device application. Apart from that, the scaling theory proposed by Dennard has a lot of limitations such as it does not consider short-channel effects and the turn-off behavior of a transistor.

1.4 Challenges in MOSFET Scaling

Although dimension scaling has a lot of advantages as mentioned in the previous section, a drastic reduction of dimension does not always give an expected result unless the following issues are taken care of. The main reason for this is depletion widths of the drain and source become comparable to the channel length of a MOSFET. One common observation is, due to the short channel length of the MOSFET, the drain current which is supposed to be constant in the saturation region, keeps increasing.

Threshold voltage: When a MOSFET is shrunk, the power supply voltage (V_{dd}) has to decrease to keep the e-field and power dissipation within certain limits. On the other hand, threshold voltage (V_{th}) cannot be decreased much because the higher portion of leakage current constitutes the majority of power dissipation. Therefore, V_{th} scaling needs to slow down to decrease off-state current (I_{OFF}) [16]. On the other hand, circuit designers always want V_{th} to be invariant with biasing conditions and transistor dimensions.

High electric fields: The supply voltage (V_{dd}) of a MOSFET cannot be reduced proportionally to the channel length. Thus, the electric field increases across the oxide (SiO_2) layer. Due to higher e-field, carrier mobility decreases, and scattering increases. When the e-field increases significantly, it causes a breakdown in the oxide, increases leakage current, and eventually, the device is damaged.

Gate oxide tunneling: As MOSFET is scaled down, the ratio between electron thermal voltage (kT/q) and operating voltage reduces. This leads to a higher leakage current originating from the thermal diffusion of electrons [17]. Oxide thickness should be reduced in proportion to scaling, but when the oxide thickness is reduced too much, quantum tunneling occurs. This leads to an exponential increase in gate current which is unwanted [17].

Parasitic resistance and capacitance: The parasitic resistance and capacitance reduce unfavorably with transistor scaling [17]. Thus, the effects of parasitic elements reduce the performance gain obtained from transistor scaling which can lead to reduced drain current.

The randomness of dopant distribution: In smaller devices, it is not possible to place dopant atoms at accurate positions, which leads to the random orientation of the dopant atoms.

Source to drain tunneling: The channel length of a MOSFET means the distance between the source and drain. When the channel length becomes small enough, it is easier for the electrons to tunnel through the barrier even without gate bias. When this happens, the purpose of a transistor is not served i.e. it cannot act as a switch [18].

Heat dissipation and interconnect delays: When a MOSFET cannot dissipate heat properly to the resistive parts, hot spots can occur. This leads to an overheating of material, and eventually, the device comes to a failure. Due to scaling, the interconnect wire width is reduced which increases the resistance, thus delay is increased. [17].

Hot carrier effect: The carriers are termed 'hot' because when the carriers attain high energy, their effective temperature becomes greater than the lattice temperature. Due to this energy imbalance, carriers cannot release their energy to lattice atoms quickly. This is a significant problem of MOSFET operating in linear and saturation regions. In the Si device, the barrier height between Si-SiO_2 layers is 3.1 eV, whereas, for 4H-SiC, the barrier height between SiC-SiO_2 is 2.7 eV. That signifies that the chances of electrons crossing the barrier height for SiC devices are higher compared to Si devices.

1.5 Thesis Goals

It has been clear that scaling is the future for any technology and that is why the silicon industry is flourished in the last 50 years. In 2022, Samsung unveiled 3 nm GAA technology in

silicon devices [19]. Also, they are focusing to bring 2 nm in 2025 and 1.4 nm in 2027. On the other hand, SiC is still in the micrometer (2 μm/ 1.2 μm) range (discussed in chapter 2 of this thesis). So, SiC technology is still in its infancy which can be compared with silicon technology in the mid-1980s range. In the future, the SiC devices are expected to become more scaled i.e. they will enter into the sub-micron and then deep submicron range. Proper device design in those ranges can be necessary to rip the benefit of scaling. In parallel, the challenges of MOSFET scaling should be taken care of. Although SiC is popular in many areas such as in power electronics, high-temperature circuits, harsh environment sensing, and so on, research on low voltage areas is less explored or yet to be explored. Low voltage CMOS technology is of immense importance keeping complex circuit technology, reproducibility and cost in mind. In this thesis, a low-voltage SiC NMOS device in the submicron range (2 μm to 600 nm) is simulated and its key parameters and performance are analyzed. At the same time, hot carrier analysis is done and a new structure (using silicon topology) is proposed in SiC to mitigate hot carrier effects. In the end, the realization of this structure in terms of the CMOS process is proposed.

In Chapter 2 of this thesis, different SiC CMOS processes from foundries and other institutes are discussed to understand the current state of the art of SiC CMOS processes and their main differences. In addition, hot carrier effects on MOSFETs are discussed.

Chapter 3 provides a brief description of the tools used to simulate conventional 4H-SiC NMOSFET. Then, conventional devices are designed, characterized and results are discussed.

Chapter 4 provides simulations of the Low Doped Drain (LDD) structure in 4H-SiC to mitigate hot carrier issues. Then, LDD devices are characterized and results are discussed. The advantages and disadvantages of LDD are analyzed in the end.

Chapter 5 discusses prospective spacer technology, dopant species, and doping methods. Furthermore, a non self-alignment, and self-alignment technique to implement LDD structure in 4H-SiC CMOS is discussed.

Chapter 6 provides conclusions which include the summary, future work, and major roadblocks to implementing LDD design in the current CMOS process.

Chapter 2. Background and Literature Review

CMOS devices are used in many IC applications such as digital logic, memory devices, sensors, OPAMPs, and microprocessors. They are available for digital and mixed analog applications. The main aspect of any CMOS process is, a single substrate is capable of handling two complementary transistors (p-type/ PMOS and n-type/ NMOS). To understand a CMOS process, it is important to look into a standard silicon CMOS process first because the SiC CMOS process has evolved from the Si CMOS process. Then, the major differences between Si and SiC CMOS process will be highlighted. Gradually, SiC CMOS processes available from different manufacturers/institutes will be discussed to understand the current state of the art.

2.1 CMOS Process Overview

The fabrication of the silicon CMOS process consists of a sequence of steps. In a single well process, it can consist of six masks: n-well, polysilicon, n+ diffusion, p+ diffusion, contacts, and a metal layer [20]. It can start with a p-type substrate, on top of which an n-well is made by the group - V dopant atoms. The wafer is oxidized at a high temperature to form oxide (SiO_2) on the surface, and photoresist (organic material) is deposited on top of it. The oxide is patterned to form an n-well by an n-well mask and the photoresist is exposed through the n-well mask. This is called photolithography where the UV lights can only pass through where the well exists. Upon exposure to UV light, the photoresist (positive photoresist) gets softened and is removed to expose the oxide. The oxide is etched where it is not protected with photoresist. The remaining photoresist is stripped with piranha (mixture of H_2O_2 and H_2SO_4) etching. Then, a thin oxide (SiO_2) is grown on the surface of the wafer and placed in a chamber with Silane gas (SiH_4) and heated to grow a polysilicon layer by CVD process. The wafer is then patterned with a photoresist and poly mask. The n+ region is introduced in the p-substrate and n-well through an

n+ diffusion mask after growing an oxide layer. Although ion implantation is used in recent times to implant n+, they are still known as diffusion. In the silicon CMOS process, source and drain junctions are automatically formed adjacent to the gate which is known as self-alignment. Then, the protective oxide is stripped off. For p-diffusion, the same process is repeated. A thick field oxide is grown to insulate the wafer and patterned with a contact mask. Then, a metal is sputtered over the contact cuts for making ohmic contact. Finally, metal is patterned with a metal mask. A plasma etch is used to remove metal everywhere except the contact area. Although the main structure and concept are the same for SiC CMOS, there are some major differences. In SiC, ion implantation is done at more than 500 °C and at such high temperature, no photoresist mask can exist. Thus, a metal mask or oxide mask is used. After the ion implantation process, high-temperature annealing (more than 1500 °C) is required for SiC to activate the dopants. At such high temperatures, polysilicon cannot exist because its melting point is around 1440 °C. Also, at such a high temperature, the quality of SiO_2 /oxide posed a question mark. For this purpose, self-alignment is not preferred by scientists in the SiC CMOS process.

The following sections are highlighting the differences between the SiC CMOS processes of different foundries and Institutes. Refer to Figure 2.1 for a cross-section processing diagram of the silicon CMOS process.

2.1.1 Cree CMOS

European patent (EP 0894339 B1) or US patent (US 6344663 B1) is a great source to review Cree's silicon carbide CMOS fabrication process in detail [21], [22]. Cree's CMOS process starts with a 6H-SiC p-type substrate of doping concentration 1e16 to 1e18. The preferred doping concentration of the p- epitaxial layer was 1e15 to 1e17. The well region was formed with a doping concentration of 1e15 to 1e17 by implanting nitrogen at 650 °C with energy 380 keV.

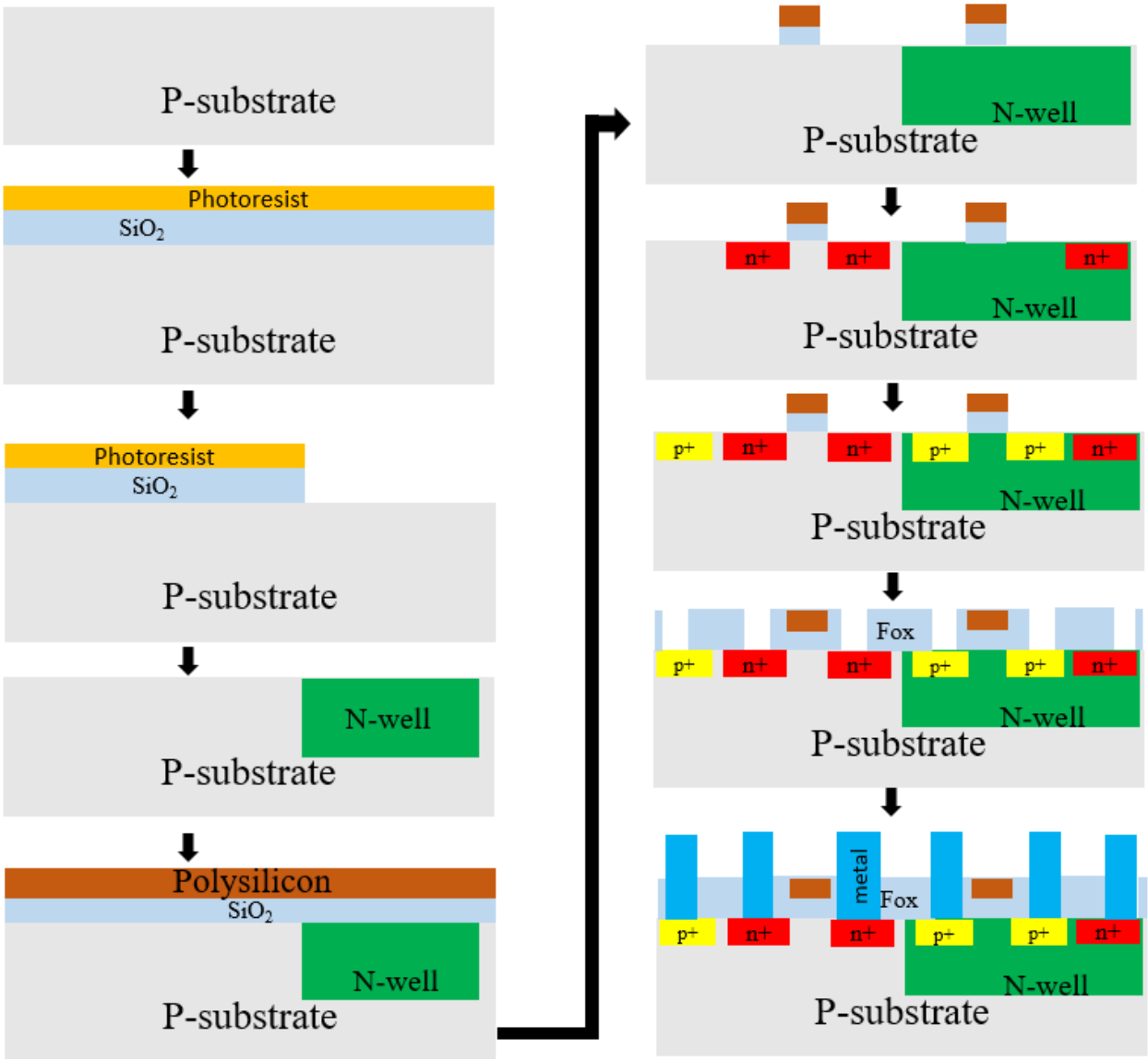


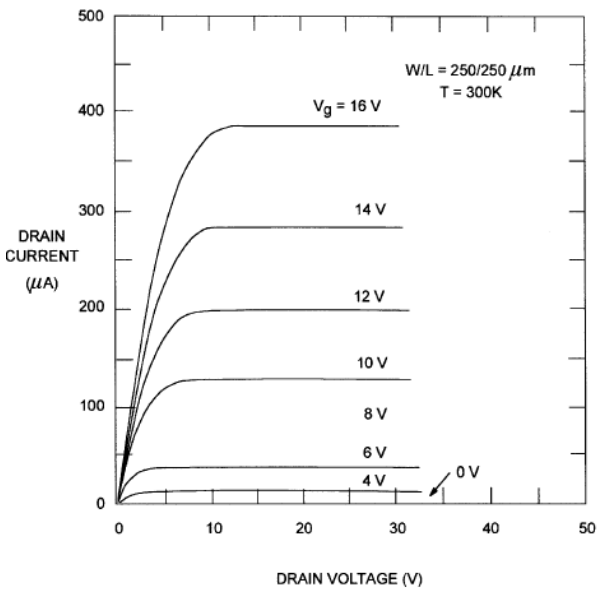
Figure 2.1 Basic CMOS Process (silicon) [20]

However, the temperature can vary from room temperature (RT) to 1300 °C and energy can vary from 250 keV to 1 MeV. The NMOS source (n+), drain (n+), and PMOS channel stop (n+) region were doped with nitrogen ion at 650 °C with a doping concentration of 1e17 to 1e20. This was done by multiple-step implantation where the energy range varied from 135 keV to 200 keV.

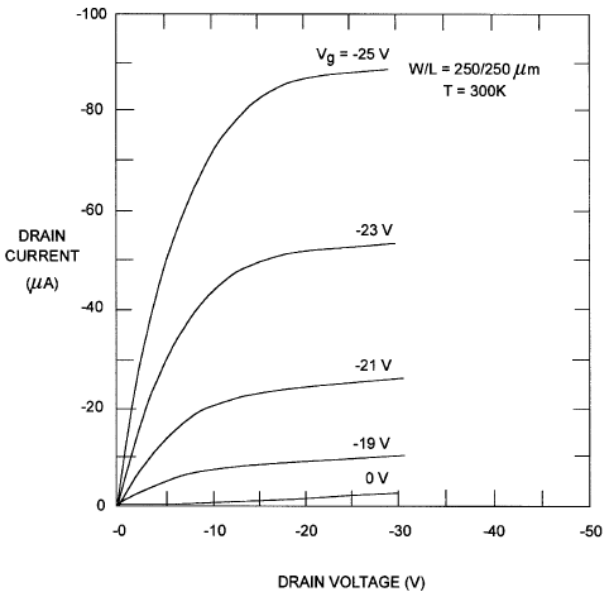
The wafer was then annealed at 1550 °C to activate the dopants. Next, PMOS source (p+), drain (p+), and NMOS channel stop (p+) implants were done with carrier concentrations

1e17 to 1e20. This was done by aluminum ion at an implanted temperature of about 1200 °C, but temperatures ranging up to 1300 °C can be used. Aluminum was used during multiple energy implants (energy up to 135 keV) to get an appropriate well depth. Ion implantation energy was chosen such that the depletion region of the source and the drain should not exceed the substrate region. Then the wafer was thermally annealed at 1550 °C to remove surface damage and the resulting oxides were stripped. The gate dielectric (SiO_2) was deposited and then placed in an oxidized ambient for several hours before the deposition of gate metal. This process is called re-oxidization and this is one of the key steps in Cree's CMOS process [23]. Re-oxidization helps to densify the oxide by oxidizing impurities such as residual carbon and dangling silicon bonds. Re-oxidization also improves the oxide layer to become C/ SiC free; increases the dielectric strength of SiO_2 (11-12 MV/cm) and increases breakdown voltage [23]. According to Cree, as most MOSFETs face reliability issues in their oxides, a dense oxide layer is important as it strengthens the gate overlap region. Reoxidation is significant in another sense. 'Self-alignment' which is common in silicon devices, is not common in SiC. The source and drain are implanted before the gate by the ion implantation process. As a result, the surface of SiC becomes poor due to heavy implantation. So, when dielectric strength is not strong, it increases the oxide failure in the gate overlap region. According to them, the poor dielectric strength is the result of impurity segregation, rough SiC-SiO_2 interface, or non-stoichiometric growth. They mentioned that deposited oxide acts better than thermally grown oxide. When oxide is thermally grown it is important to consider the face. If the oxidation is in the carbon (C) face then the temperature requirement is less (900 °C - 1300 °C) than silicon (Si) face (1000 °C – 1400 °C) because C oxidizes faster than Si. The best result they got for oxidation was at around 1050 °C – 1100 °C. Similarly, in the case of re-oxidization, their preferred temperature is 950 °C in the presence of

water (H_2O). On the other hand, in PMOS, usually, aluminum was used as a dopant and this aluminum creates a gate leakage path at a higher temperature. This problem was solved by the re-oxidization process. Molybdenum (preferable) or aluminum was used as gate material and nickel was used to create simultaneous ohmic contact in NMOS and PMOS. The contacts were annealed at 825 °C for 2 minutes. The interconnect metallization was formed by molybdenum. Then contact pads were formed with a platinum layer and a gold layer. Finally. The entire device was covered by a protective layer of SiO_2 or Si_3N_4. An operational amplifier was demonstrated in a 6H-SiC circuit with epilayer doping concentration of 6e15 to 6e16 and thickness of 3-5 µm. 15V power supply or V_{DD} was used. The carrier concentrations of n+ and p+ were 1e19 cm^{-3} and 1e18 cm^{-3} and the depths were 0.35 µm and 0.25 µm respectively. The gate widths were 25 to 200 µm and gate lengths were 2 to 8 µm. The threshold voltage of NMOS was 2.5 volts and that of PMOS was -15 to -17 volts. The open loop operational gain of the amplifier was 10^4 or 80 dB.



(a)



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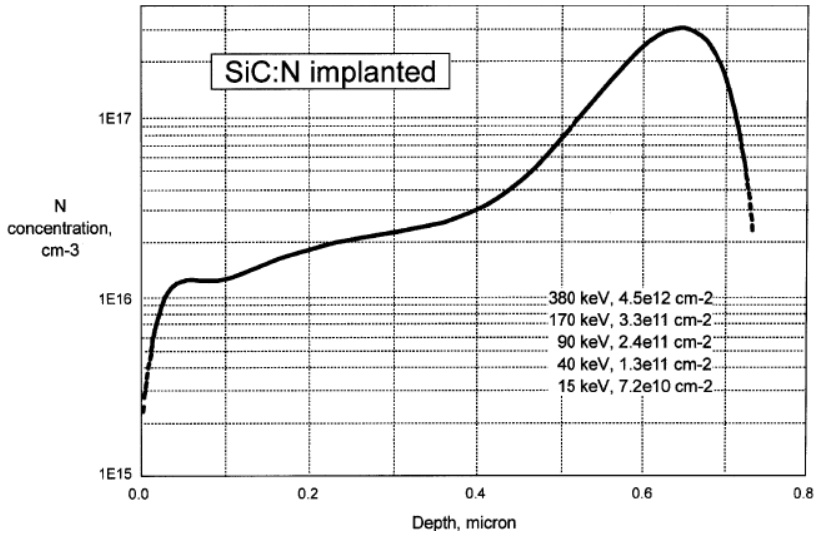
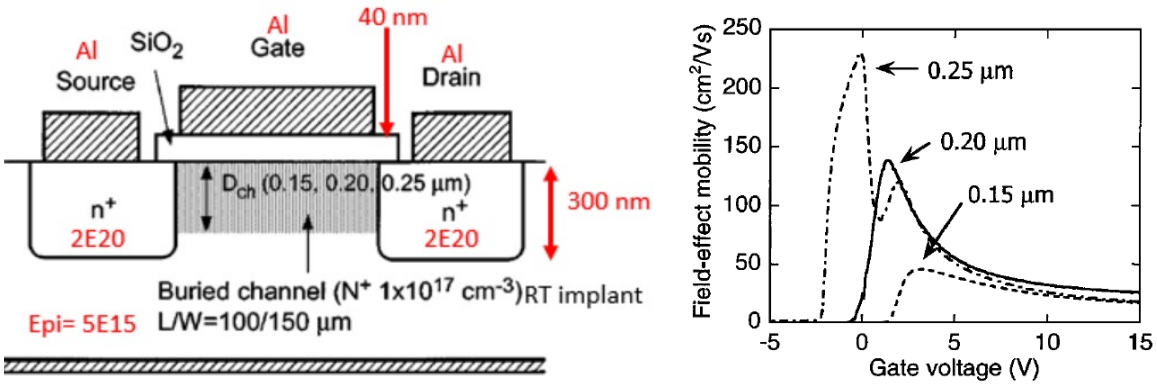


(c)

Figure 2.2 Cree CMOS (a) NMOS I-V characteristics, (b) PMOS I-V, (c) Doping profile of n-well showing nitrogen concentration [22]

2.1.2 Hitachi CMOS

Hitachi Ltd. demonstrated buried channel (BC) MOSFET where their main focus was on channel mobility [24], [25]. It is believed that at the SiO_2/ SiC surface, a high density of traps exists. As a result, the channel mobility is extremely low in 4H-SiC MOSFET. Hence, their main focus was shifting the channel from the surface to the body of MOSFET. As a result, they got higher electron mobility (140 cm^2/ Vs) compared to standard inversion channel mobility which is 25 - 35 cm^2/ Vs [26]. In their structure, the MOSFET's channel length and widths were 100 to 150 μm [24]. The buried channel was formed by nitrogen ion (N^+) at room temperature implantation at a depth of 0.2 μm followed by annealing at 1500 °C. This is almost similar to Cree's process. Another noticeable point in their process is that they also mentioned the importance of wet re-oxidation (after gate oxide is grown by dry oxidation step) which significantly improves channel mobility.



(a) (b)

Figure 2.3 (a) Schematic cross-section, (b) Field effect mobility of Hitachi's 4H-SiC BC MOSFET [24]

Apart from BC MOSFET, Hitachi focused their research on radiation resistance technology with SiC after the incident in Fukushima. They have demonstrated CMOS technology and radiation performance of op-amp. In their MOSFET, gate length and width were 100 µm and 200 µm. In terms of the circuit, where they have demonstrated op-amp, the length (L_g) of NMOS and PMOS was 10 µm and 20 µm [27]. In one of their recent work, they fabricated a trans-impedance amplifier (TIA) to measure gamma irradiation resistance [28]. They have used 8 nm thin gate oxide to reduce threshold voltage (V_{th}). The length and width of NMOS and PMOS were 5 µm and 400 µm respectively. They have also reduced leakage current (42% less than conventional) during higher gamma radiation by their structure, but their main focus was making a heat and high radiation resistance technology [29].

2.1.3 NASA & CWRU JFET

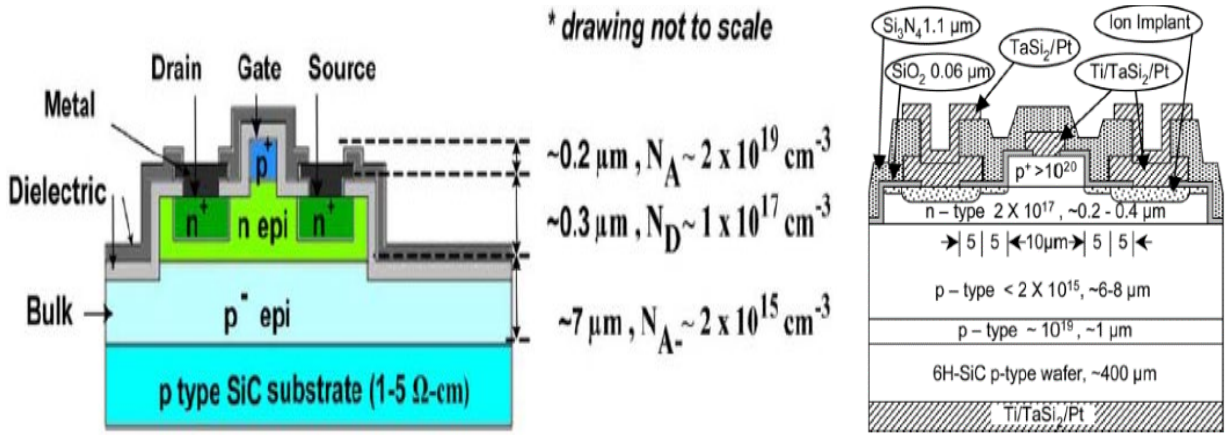
As mentioned in the first chapter that SiC is famous for its high-temperature application and that is one of the selling points of this material. NASA has demonstrated ICs that are capable of operating at higher temperatures up to 1000 °C for a prolonged period [30]. As their main

target was space exploration and extremely high temperatures (such as on Venus), making a reliable device was important. For that reason, they explored JFET instead of MOSFET as JFET is an oxide-free device, and maintaining the quality of oxide at very high temperatures is difficult. The feature size of their JFET was 24 μm / 6 μm [30]. In another type of work, they focused not only on the extremely high temperature but also on the lower temperature (from -190 °C to +812 °C). Such temperature can be seen in arctic conditions where an aircraft engine consisting of SiC circuits can perform at a lower temperature such as -55 °C [31].

A similar kind of structure which is developed by NASA Glenn Research Center is fabricated by researchers from Case Western Reserve University (CWRU). Their W/L ratio of JFET was 100 μm / 10 μm [32]. Unlike MOSFET, one thing that is noticeable in this structure was the existence of three epi-layers (7 μm, 0.3 μm, 0.2 μm). The doping level of the gate epi layer was two magnitudes higher than the channel (10^{19} compared to 10^{17}). This higher doping ensures the formation of a depletion layer in the n-epi layer when a reverse bias is applied to the gate terminal. Figure 2.4 shows the cross-section of 6H-SiC JFET.

The threshold voltage of this device is -4V which ensures complete pinch-off (depletion width becomes 0.324 μm) of the channel and signifies the operation of JFET. Another significant step is, the gate is mesa etched (compared to MOSFET where the polysilicon gate is deposited) which ensures a defect-free gate and does not require activation at high temperatures [33].

Perhaps one of the significant differences which are embedded in this structure is the presence of a shallow low-doped region (in the 0.3 μm layer by phosphorus atom @130 keV at room temperature implant). This also can be done by nitrogen atom @70 keV. In both cases, the dose of ion implantation is 7e12 cm^{-2}. The main reason for this shallow low doped region is to reduce the e-field between the gate and source/ drain. This shallow low doped region also



(a) (b)

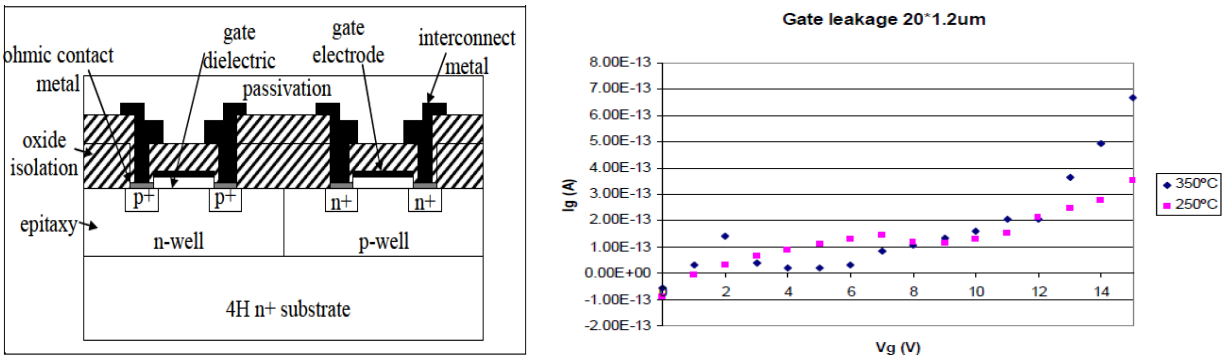
Figure 2.4 (a) Schematic cross-section of CWRU 6H-SiC JFET [32], (b) Simplified cross-section of NASA 6H-JFET [33]

helped to reduce parasitic resistance [33]. On the other hand, like silicon scaling, CWRU researchers have mentioned the importance of channel length and feature size reduction to improve the performance of the JFET device [34]. However, JFET is a normally-on device, so despite providing lower on-resistance, the higher leakage of this device makes it less popular than MOSFET.

2.1.4 Raytheon CMOS

Raytheon Systems Limited has demonstrated 1.2 µm 4H-SiC technology called high-temperature silicon carbide (HiTSiC®) for logic and mixed-signal ICs, however, this technology was discontinued in 2018 [35]. Their technology was mainly developed to operate at 15V at high temperatures up to 400 °C - 450 °C [36], however, they have observed excessive gate leakage (shown in Figure 2.5 (b) when the temperature crosses 350 °C [37]. They have demonstrated an inverter, NAND gate, and ring oscillator [37] in their process. Using this 1.2 µm Raytheon process, Dr. Mantooth's group from the University of Arkansas has demonstrated a comparator, current, and voltage references, gate driver, and 8-bit digital-to-analog converter (DAC) [38]–

[41]. Raytheon's main aim was to develop a process that can work in high temperatures and prolonged hours (7500 hours). For that reason, they have mentioned the use of a carbon cap during the annealing process after ion implantation and threshold implant [36]. The channel length of their designed transistors was between 20 μm to 1 μm where a short channel effect was observed with gate lengths below 1.2 μm. To overcome the short channel effects they tried high well doping which degraded the channel mobility of the device [42]. Nickel was used as an ohmic contact in both the p+ and n+ regions. Aluminum (1.02e17 cm^{-3}) and nitrogen (1.5e17 cm^{-3}) was used as p-channel and n-channel dopant respectively which is common in the previously mentioned CMOS processes. They pointed out that minimization of ion implantation energy can result in a good quality device. Also, they pointed out that a 4-degree off-axis along <1120> direction is better than on-axis orientation along {0001} planes or 8 degrees off-axis towards {0001} or <1120> planes [43]. Another important observation of their structure is that they have used the full depth of the epitaxial layer to fabricate different devices. As an example, when they use a p-type substrate and they need n-conductivity in the p-type substrate, they used very high implant energy (as high as 2 MeV). This is to ensure that the n-conductivity region extends the full depth of the epitaxial layer and touches the p-type substrate (vice versa is also true). By doing this, they ensured p-type epitaxial layer becomes discontinuous in the lateral direction [43]. This serves the purpose of isolation. Apart from this, they have demonstrated BiCMOS technology which consists of CMOS and bipolar transistor (npn / pnp) in a single IC [43].

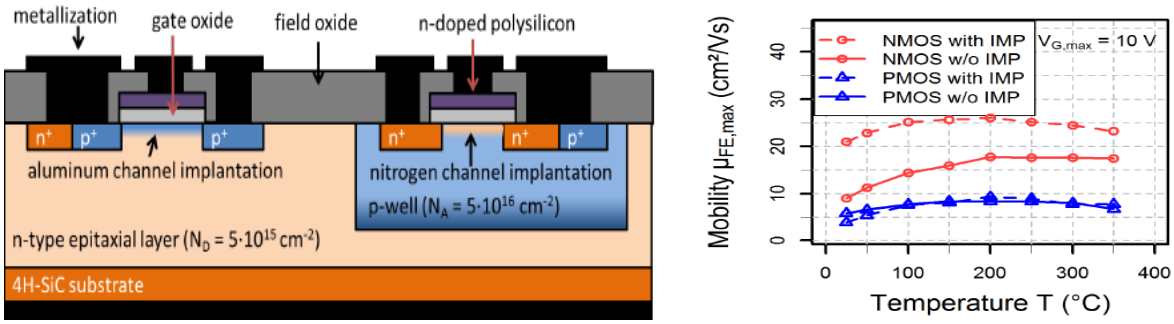


(a) (b)

Figure 2.5 (a) Raytheon's CMOS process architecture, (b) Gate current vs. gate voltage for 20*1.2 µm NMOS [37]

2.1.5 Fraunhofer CMOS

Fraunhofer Institute for Integrated System and Devices Technology (IISB) reported 6 µm SiC CMOS technology where they used 1-2 µm n-type epilayer (1e18 cm^{-3}) as a buffer layer and then again 8 µm n-type epilayer (5e14 cm^{-3}) as a top layer [35]. They have used well-known silicon topologies to define their CMOS circuit [44]. N and P are used as dopants for the well and source and drain. The annealing temperature (1700 °C) is almost the same as what is being used in earlier mentioned processes. 50 nm thick gate oxide and 400 nm thick field oxide was used. 500 nm polysilicon layer was used as a gate. 80 / 300 nm Ti / Al stack was used as an ohmic contact in the p+ and 50 nm Ni / Al was used as an ohmic contact in the n+ region [35]. They have investigated ohmic contacts with some other materials also such as Ni/Ti/Al/W and checked the formation of silicides at different temperatures [45]. Their metallization was done with 50 nm/ 700 nm/ 20 nm using Ti/Al/Ti stack which helped to reduce their thermal budget. This 6 µm technology was built to operate at 20V supply voltage [35].



(a) (b)

Figure 2.6 (a) Fraunhofer's CMOS process architecture [46], (b) Field effect mobility of NMOS and PMOS with and without channel implant [46]

In some research work that was published using Fraunhofer's devices, the importance of channel implants was pointed out (2e13 cm^{-2} with Al @35keV for PMOS). This channel implant helped them to shift the threshold voltage from –5V to -3.6V [47]. For NMOS, nitrogen was used as a channel implant (5e13 cm^{-2} @20keV) [46] (as shown in Figure 2.6 (b)). In one research, the propagation delay of SiC devices was compared with silicon technology where they showed propagation delay was 17 times longer than Si devices at a p-well doping concentration of 1e15 cm^{-3}. The speed of the device was limited due to the lower mobility of pMOS at room temperature and higher temperatures (300 °C). The delay was seen to be 32 times when the well doping concentration is increased to 8e15 cm^{-3} [48].

Recently, Fraunhofer offered early access to its 2 µm SiC CMOS technology in a twin well technology [49]. Their circuits are capable of working at high temperatures of up to 600 °C. They have also worked on process modules capable of working at high voltages and harsh environments. They have mentioned using one poly and two metal (Pt) layers [49] and the oxides are capable of handling 20V. Fraunhofer only uses thermal oxidation for their oxide growth and annealing, but they did not mention wet re-oxidation in their process.

2.1.6 Purdue CMOS

Dr. Kornegay himself and his research group demonstrated significant process development in SiC devices. Researchers under him demonstrated a 6H-SiC CMOS process where a lightly doped epilayer (5e15 cm^{-3}) was used on a heavily doped n+ substrate [50]. After cleaning, they oxidized the wafer at 1200 °C in an O_2 environment for 30 minutes. One of the key differences in this process is the use of a hard mask. They used Ti / Au mask (20 nm / 1 μm) and used six-step implantation with Boron (B) at 650 °C to form a p-well. The total dose to form p-well was 2.5e14 cm^{-3} (20 keV/4.5e12, 45 keV/7.5e12, 85keV/1.1e13, 140keV/1.7e13, 230 keV/3e13, 380keV/1.8e14) [50]. B was used as p-channel implant (25keV/ 8e12, 60keV/1.8e13) at 650 °C and N is used as n-channel implant at 650 °C (260KeV / 6e12). The surface was covered by Ti (20 nm) and Au (470 nm) mask and then pMOS source and drain implant were done by Al with dose 2.2e15/cm^2 (45 keV/2.2e14, 90 keV/3.4e14, 160keV/5.4e14, 270keV/1.1e15). Again, Ti (20 nm) and Au (470 nm) was used as nMOS mask and N was used as an implant with dose 1.05e16/cm^2 (40 keV/2.5e15, 90 keV/3e15, 160keV/5e15). 1550 °C temperature was used in the Ar environment for annealing. Wet oxidation was used at 1150 °C for 1 hour to grow gate oxide followed by 30 minutes of Ar anneal.

The polysilicon gate was deposited by LPCVD in the presence of silane gas for 30 minutes. Then polysilicon was doped with boron followed by dopant dive in at 900 °C for 50 minutes in nitrogen and oxygen flow. 50 nm Al and 20 nm Ni were grown by a thermal evaporator and used as p-type contact and n-type contact respectively. The isolation of the device was done by 200 nm Si_3N_4 grown by RTA at 850 °C for 5 minutes. Refer to Table 2.1 for process parameters used in Purdue CMOS.

Table 2.1 Process parameters used in Purdue CMOS [50]

Parameter	**NMOS**	**PMOS**
Gate Oxide thickness	285 °A	
Interface state density	$4.2 * 10^{11}$ $eV^{-1}cm^{-2}$	
Fixed charge density	$1.0 * 10^{12}$ cm^{-2}	
Substrate concentration	$1.3 * 10^{17}$ cm^{-3}	$5 * 10^{15}$ cm^{-3}
Long channel V_T	2.6 V	-6.7 V
Channel mobility	8 cm^2/Vs	5.87 cm^2/Vs
Source/ drain junction depth	3000 °A	3500 °A
S/D sheet resistivity	3.1 kΩ/sq.	120 kΩ/sq
Specific contact resistivty	$1.65 * 10^{-4}$ Ωcm^{-2}	$2.9 * 10^{-2}$ Ωcm^{-2}

In their research, they used e-beam to pattern their submicron channel lengths. The rest of their fabrication was processed by optical lithography. The channel length of their CMOS was 0.8 μm [50]. As their study was based on sub-micron devices, they mentioned the importance of hot carrier effects in devices having thin gate oxide. However, the reliability of the device was unexplored [50]. They also mentioned the importance of low doped drain (LDD) in sub-micrometer MOSFET which requires more in-depth study. Dr. Kornegay's group has demonstrated an 11-bit ring oscillator, NANO, NOR, ExNOR, and Ex-OR gates.

Table 2.2 shows the summary in terms of the gate length of the SiC CMOS processes.

Table 2.2 SiC processes

Inventors	**MOSFET Technology (Gate length)**	**Production Year**	**References**
Cree CMOS	2 to 8 μm	2002	[21], [22]
Hitachi CMOS	100 μm	2001	[24]
NASA JFET	6 μm	2018	[30]
CWRU JFET	10 μm	2014	[32]
Raytheon CMOS	1.2 μm	2014	[37]
Fraunhofer CMOS	2 μm	Early Access	[49]
Purdue CMOS	0.8 μm	1998	[50]

As this thesis is focused on SiC advanced CMOS process in the submicron range, and in that range, one of the prominent issues is hot carrier effects. The next section will discuss the basics of hot carrier effects in MOSFET and its mitigation processes. Among many solutions, one prospective solution will be considered and discussed thoroughly.

2.2 Hot Carrier Effects in MOSFET

When device dimensions are decreased but supply voltage remains constant, the lateral electric field in the MOS device increases. When the electric field (E_M) becomes too strong then carriers become energetic, thus they are termed as 'hot'. Carriers are of two types in MOSFETs – electrons and holes. So, two types of effects are possible - hot electron effects and hot hole effects. Hot electron effects are more serious than hot hole effects because of electrons' high mobility compared to holes. For this reason, hot electron effects are more serious in NMOSFETs as the carriers are electrons, and the channel is formed by them. From the operation perspective, when a MOSFET goes into the saturation region, the electric field (E_M) becomes high near the drain. The calculation of E_M is complex [5] as it depends on the two-dimensional Poisson equation. However, the calculation of E_M can be written as

$$E_M = \frac{V_d - V_{dsat}}{m} \qquad \text{Equation 2.1}$$

$$where\ m = 0.22\, t_{ox}^{\frac{1}{3}} r_J^{\frac{1}{3}}\ \ for\ t_{ox} \geq 15\ nm;$$

$$or\ m = 1.7 * 10^{-2} * t_{ox}^{\frac{1}{3}} r_J^{\frac{1}{3}} L^{\frac{1}{5}}\ \ for\ t_{ox} < 15\ nm\ and\ L < 0.5\ \mu m$$

From Equation 2.1, it can be seen that r_J, t_{ox}, and L is inversely proportional to E_M. Thus, as the device dimension shrinks, E_M increases. This high E_M energizes electrons by supplying more kinetic energy. Thus they become 'hot'. This hot electron causes several effects in the

MOSFETs. Due to the high e-field, when electrons gain sufficient energy, they can lose their energy by creating other carriers. This process is known as impact ionization. The total number of carriers generated by impact ionization is equivalent to the reciprocal of e-field ($1/E_M$). When

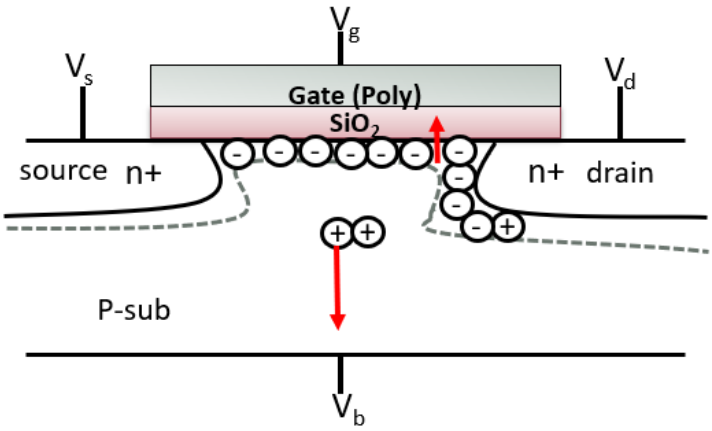


Figure 2.7 Hot carrier (electrons and holes) generation [50]

the generation of carriers reaches an extreme, it can lead to avalanche breakdown [5]. The first effect that can be seen due to the hot carrier is the generation of substrate current. Generally, electrons are attracted towards the drain (due to positive bias) and add drain current whereas the holes enter the substrate and create parasitic substrate current. These holes sometimes when absorbed by the source, can lead to a voltage drop and becomes a major reason for snapback breakdown. Excess amounts of substrate current can induce latch-up in CMOS circuits. The second effect that can be seen by hot carriers is gate leakage. Some of the carriers can move towards the gate electrode and produce gate leakage current (usually, in the pA (10^{-12}) or fA (10^{-15}) range), which is undesired. Sometimes, hot carriers cannot reach the gate electrode as they are absorbed by oxide vacancies or traps. As a result, negative charge density is created in the oxide layer, and thus threshold voltage (V_{th}) deviates (V_{th} increases for nMOS device). This situation sometimes leads to a permanent V_{th} shift. The third effect, visible from the hot electron is device

degradation. From the Shockley equation [51], the amount of drain current in the cut-off, linear, and saturation regions can be mentioned as follows:

$$I_{ds} = 0 \; when \; V_{gs} < V_{th} \; i.e. at \; cutoff \quad \text{Equation 2.2}$$

$$I_{ds} = \beta \left(V_{GT} - \frac{V_{ds}}{2} \right) V_{ds} \; when \; V_{ds} < V_{dsat} \; i.e. at \; linear \quad \text{Equation 2.3}$$

$$I_{ds} = \frac{\beta}{2} V_{GT}^2 \text{ when } V_{ds} > V_{dsat} \; i.e. at \; saturation \quad \text{Equation 2.4}$$

Where $V_{GT} = V_{gs} - V_{th}$, $\beta = \mu C_{ox} W/L$, $C_{ox} = \epsilon_{ox} / t_{ox}$ which is also termed as capacitance per unit area of the gate oxide.

As V_{th} increases, V_{GT} will decrease, so the saturation current (I_{ds}) decreases. Again, when substrate leakage increases, transconductance (g_m) decreases. On the other hand, due to the accumulation of trapped charges in oxide, device performance becomes unacceptable after a certain period. When a large amount of substrate current accumulates, the device lifetime gets shortened (depending on the 10% degradation rule on g_m) [5].

The next section discusses the mitigation processes of hot carrier effects.

2.2.1 Mitigate Hot Carrier Effects

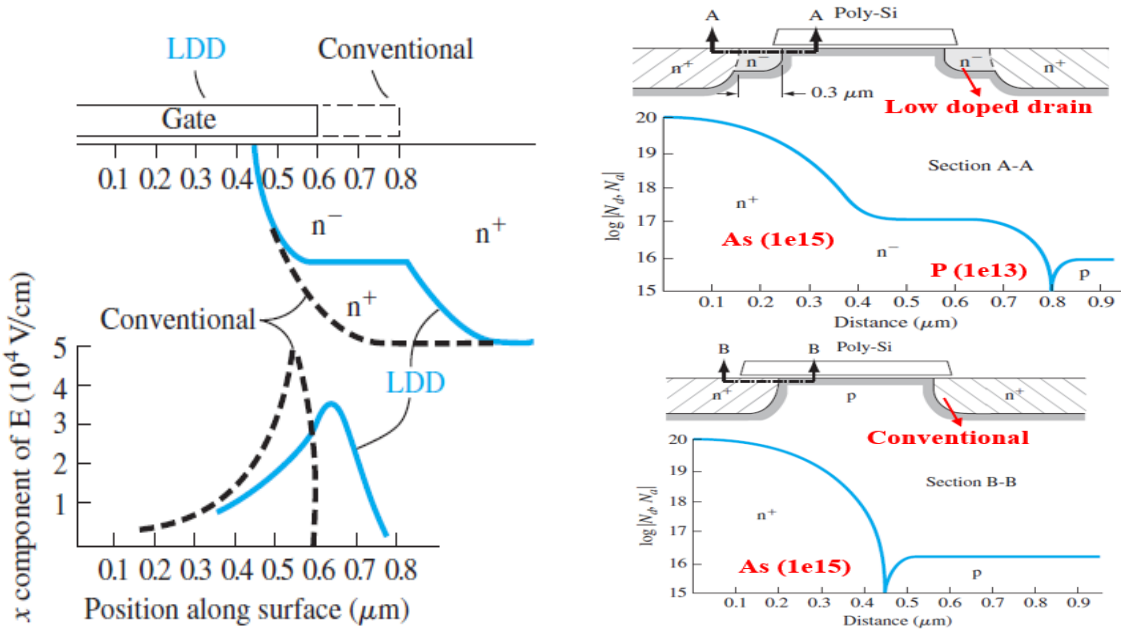
Several techniques can be applied to mitigate hot carrier effects [5]. They are:

- The voltage applied across the device can be reduced, however, this solution is out of the scope of any designer or fabricator. So, this is not a possible solution.
- The stress time of the device can be decreased, however, this is not a possible solution like the previous one because this option belongs to a user.

- Appropriate drain design techniques like Double diffused drain (DDD) and Low doped drain (LDD). However, among these two, DDD is less effective in short-channel devices due to its higher overlap capacitance and deep source and drain junctions [5].
- The density of trapping oxide can be reduced which means deploying another oxide than SiO_2 which is out of the scope of this research.

2.2.2 Low-Doped Drain

Lightly doped drain or (LDD) has been used extensively in silicon devices (Twin tub IV (L_{eff}= 1 µm), twin tub V (L_{eff}= 0.75 µm), twin tub VI (L_{eff}= 0.4 µm)) when the channel lengths are less than 2 µm. The purpose of this design is that it can absorb some of the electric fields to the drain, so E_M reduces.



(a) (b)

Figure 2.8 (a) E-field at Si-SiO_2 interface, (b) Doping profile LDD vs. conventional structure [52]

LDD structure is accompanied by a conventional structure where two doped regions are used (the lightly doped region and the heavily doped region as shown in Figure 2.8 (b), whereas conventional drain structure consists of only one region i.e. high doped region as shown in Figure 2.8 (a). From Figure 2.8 (a), it can be seen that in the LDD structure, the electric field intensity is reduced and also the peak position is shifted towards the drain. Figure 2.8 (b) shows the doping profile of conventional and LDD structures. In the LDD structure, the n+ region is doped with arsenic (As) with a dose of 1e15 cm^{-3}, called highly doped, and the low doped region is doped with phosphorus with a dose of 1e13 cm^{-3}. In the conventional structure, only As is used with a dose of 1e15 cm^{-3}. Research says that for a silicon 5V device, the LDD structure can reduce substrate leakage as high as 90% [53].

Although short-channel topologies are well used for silicon devices in the submicron ranges, they are still not popular in SiC devices. As discussed in Table 2.2, one of the main reasons is perhaps the long channel length which is still in the micron range for SiC devices. Also, Figure 2.8 discusses hot carrier effects and their mitigation process in silicon devices. How the LDD design will behave in SiC, is still unknown. Among all the CMOS processes mentioned previously, only Dr. Kornegay's group has demonstrated work in the submicron range on 6H-SiC wafers. They have used e-beam lithography to baseline the CMOS process and fabricated submicron devices and circuits [50]. They used e-beam to define channel area and used optical lithography for other areas. However, in e-beam lithography, the throughput is very low as patterns are serially written. As the self-alignment gate process is not popular for SiC, the overlapping area of the polysilicon gate on the source and drain is very important to get accurate speed. For this reason, they have taken the help of an e-beam to accurately align the poly gate over the source and drain. The gate lengths of NMOS and PMOS devices were 0.8 μm and 0.5

μm. They used Medici software to investigate the importance of punch-through implantation for their p-channel device. However, they could not demonstrate any CMOS circuits because of the malfunction of their NMOS. They mentioned the importance of LDD in NMOS and also mentioned that the use of LDD can reduce the current drive of NMOS. However detailed hot carrier analysis in NMOS is missing in their work

The hot carrier analysis on SiC NMOS has been found in a small scope in this paper [54]. They claimed to report hot carrier analysis for the first time in SiC and mentioned that a high density of defect exists in gate dielectrics, interface, and in the channel, so detection of hot carrier is difficult. Although they confirmed that hot carrier effects exist in SiC MOSFETs, its mitigation process is not shown. So, it is, therefore, very important to analyze the hot carrier effects in SiC MOSFETs with the help of simulation tools and also their mitigation process. These will be discussed in the next chapter.

Chapter 3. Conventional NMOSFET Device Simulation and Characterization

3.1 Tools Overview

Technology Computer-Aided Design (TCAD) software from Synopsys (called Sentaurus TCAD workbench) is used to design an NMOS device and analyze it (refer to Figure 3.1). Synopsys is an industry-leading software that helps to develop and optimize semiconductor processes. This tool helps engineers to tackle challenges upfront and reduce development costs. TCAD simulations are extremely important for today's IC industry as it helps to explore concepts and technologies that are not yet present in reality. TCAD helps to understand the inner working of the device and improves current existing technology [55].

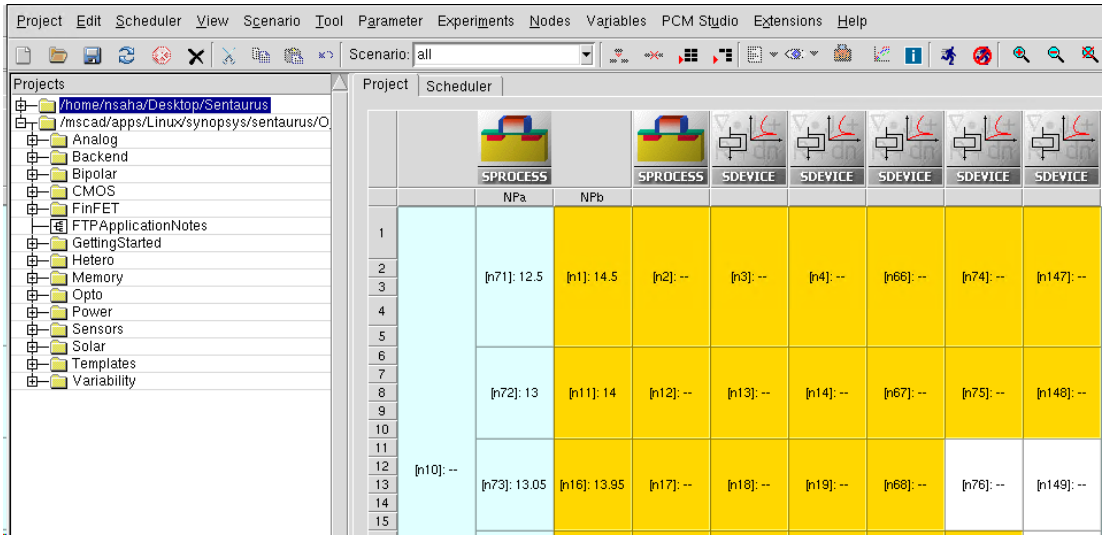


Figure 3.1 Sentaurus workbench used for process and device simulation

Sentaurus process-based simulation called 'Sprocess' was used to fabricate the NMOS device [56]. This was a virtual fabrication of the device followed by a meshing of the device required for device simulation. After that, electrical characteristics were studied by 'Sdevice' [57]. Finally, figures and plots were generated by 'Svisual'. Advanced physical models such as

Schottky Reed Hall, Auger, Lucky electron, Overstraeten- de Man, Okuto-Crowell, etc. were used to understand the device behavior.

3.2 Device Simulation

Lateral N-MOSFETs (x/y = 5 µm / 20 µm) or (W/L=5/20) with different channel lengths (2 µm, 1 µm, 0.8 µm, 0.6 µm) were designed using SProcess (refer to Figure 3.2). Seven masks were used during the virtual fabrication process. They were: 'Pwell' for the well region, 'PPlus' for body contact, 'NPlus' for the source and drain region, 'Gox' for gate oxide, 'Poly' for polysilicon, 'Fox' for field oxide, and 'Ct' for contacts.

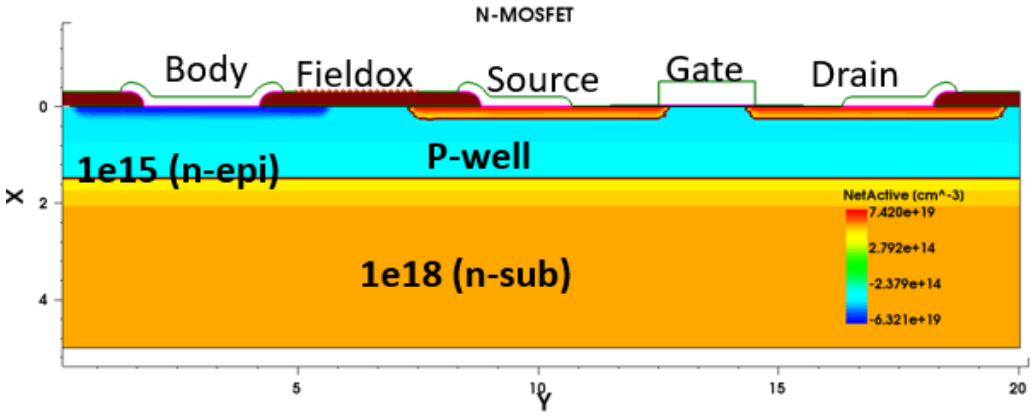
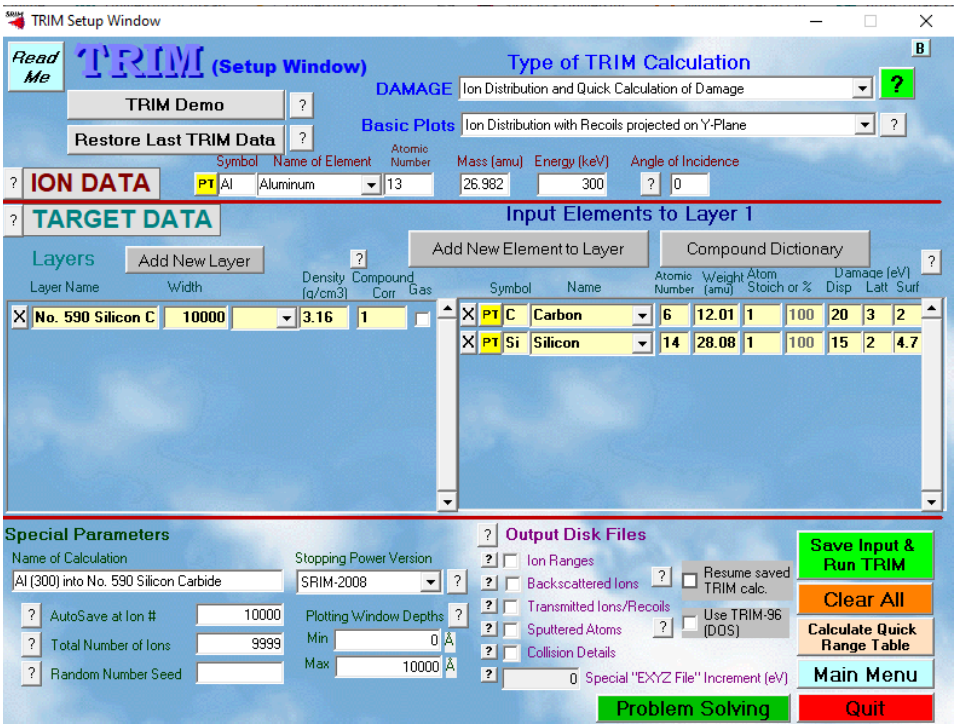


Figure 3.2 Conventional NMOSFET device simulatation in Sentaurus

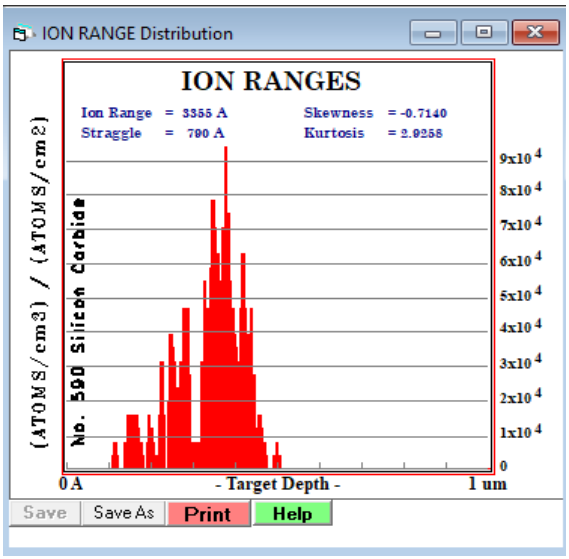
A highly doped n-type 4H-SiC substrate (1e18 cm^{-3}) was chosen to start the fabrication. There were two reasons for choosing an n-type over a p-type substrate. The N-type wafer is usually cheaper than the p-type and for a lateral device n-type is better suited than the p-type substrate because the carrier is electrons [58]. A 2 µm n-type epilayer (1e15 cm^{-3}) was grown on top of the substrate. As this structure will be combined with PMOS to form a CMOS structure, so twin well approach was considered. For that reason, aluminum was used to form a P-well with a doping concentration of 4e16 cm^{-3}. As higher temperature helps to reduce the damage of SiC

[58], so implantation was done at an elevated temperature of 500 °C. The source and drain were formed by multiple implantation steps taking aluminum as a dopant. The peak doping concentration of the source and drain regions was 7e19 cm^{-3}. 1600 °C temperature for 5 seconds was considered to activate the dopants followed by thermal annealing at 1750 °C. 20 nm gate oxide (SiO_2) was deposited to overlap source and drain followed by field oxide deposition. 50 nm polysilicon was deposited and aluminum was considered to form contacts.

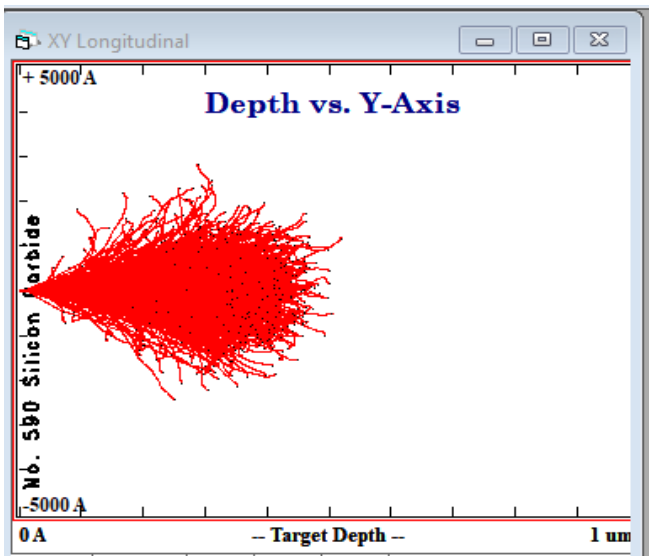
Although in some devices (like bipolar junction transistor (BJT)) ion implantation is not preferable, especially where a lower defect region is required (like the base of BJT), in CMOS, ion implantation is still a preferred method. The ion implantation profile was created with the help of software called Stopping and Range of Ions in Matter (SRIM). Figure 3.3 depicts the aluminum (Al) (atomic number = 13) dopant in silicon carbide. In Figure 3.3(a), an energy of 300 keV is chosen to implant Al. The total number of ions chosen is '9999', a random number to get an idea of the depth of implant and ion distribution. If the number of ions is more, it takes a longer time to finish the simulation. Figure 3.3(b) shows the ion range distribution of aluminum in SiC. Figure 3.3(c) shows a depth of 555 nm can be reached with the energy (300 keV) and angle (0°).



(a)



(b)



(c)

Figure 3.3 (a) SRIM workbench used for ion implantation, (b) Ion range distribution, (c) Implantation depth analysis by SRIM

3.3 Device Characterization

To understand the e-field behavior across different channel length devices, four NMOSFETs were simulated having channel lengths of 2 µm, 1 µm, 0.8 µm, and 0.6 µm. The difference among them was only in the channel lengths; the position of gate oxide and poly were fixed in all of these devices. The channel length (drawn vs. effective) of conventional NMOS is shown in Table 3.1. The effective channel length was found consistent across all four devices. The effective channel length of a MOSFET signifies the length of a channel between the source and drain which means the diffusion lengths are deducted from the drawn channel length.

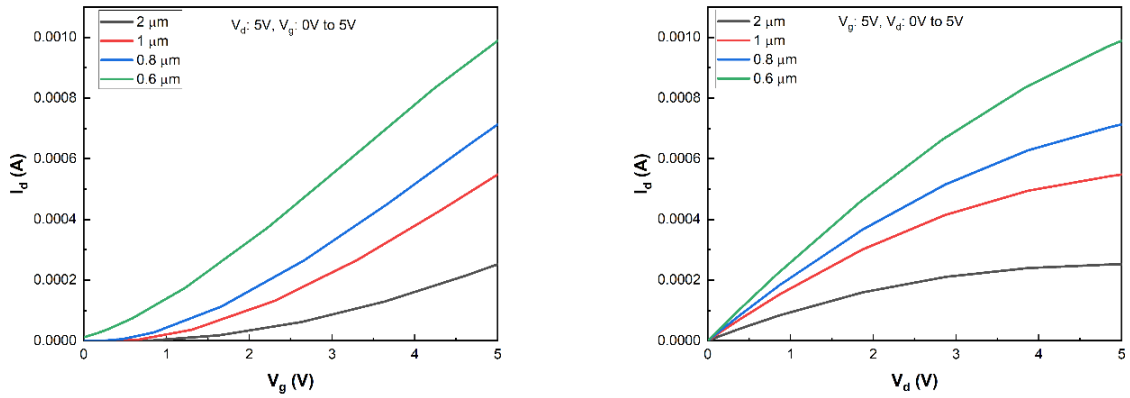
Table 3.1 The channel length of NMOSFET.

Drawn channel length (L_{drawn}) (µm)	**Effective channel length (L_{eff}) (µm)**
2	1.6
1	0.6
0.8	0.4
0.6	0.2

Figure 3.4 (a) shows the plot of drain current vs. gate voltage (I_dV_g) where 5V drain voltage (V_d) was given and gate voltage (V_g) was varied from 0V to 5V. The substrate and source terminal was connected with ground or 0V. Figure 3.4 (b), shows the plot of drain current vs. drain voltage (I_dV_d) where 5V gate voltage (V_g) was given and drain voltage (V_d) was varied from 0V to 5V. The substrate and source terminal was connected with ground or 0V. From Figure 3.4 (b) it can be seen that when the channel length was below 1 µm, the drain current was not entered into the saturation region. This signifies that the short-channel effect is prominent in channel lengths below 1 µm.

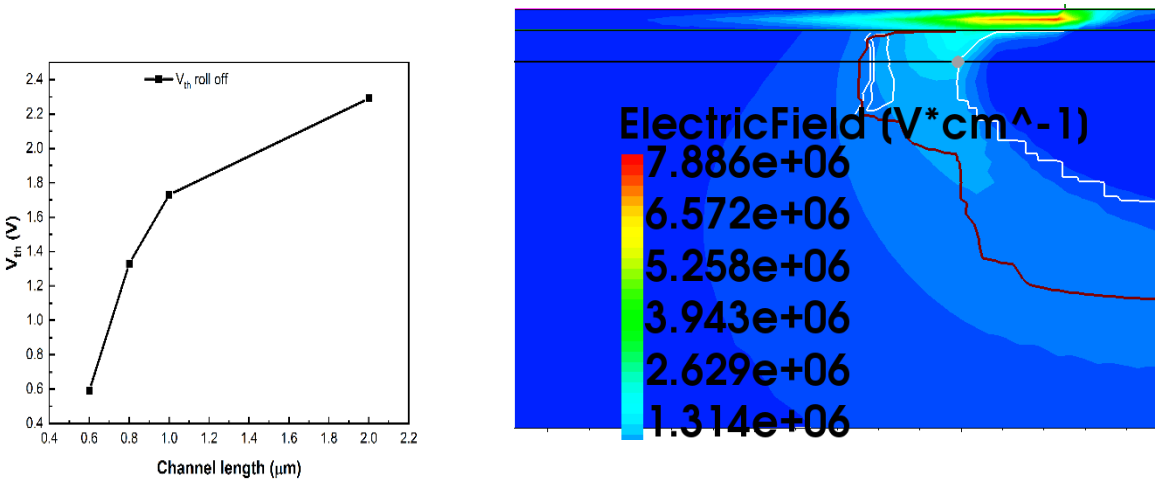
The threshold voltage signifies a minimum gate voltage required to create a conducting path between the source and drain. The threshold voltage was noted down from the simulation deck of these four devices. They are 2.29 V, 1.73 V, 1.33 V, and 0.59 V respectively for 2 µm, 1

µm, 0.8 µm, and 0.6 µm devices. They are plotted in Figure 3.5 (a) and it can be seen that V_{th} changes drastically below 1 µm as the device is scaled down. This signifies a short-channel effect.



(a) (b)

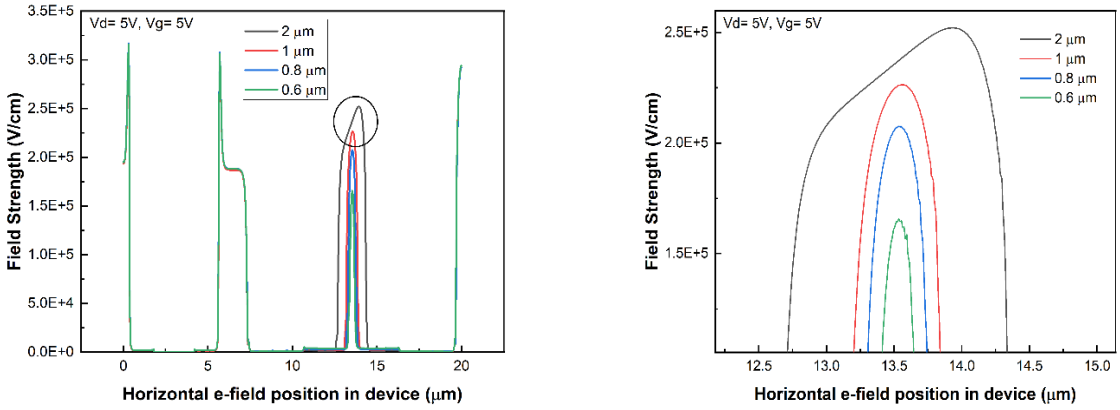
Figure 3.4 (a) Drain current (I_d) vs. Gate voltage (V_g), (b) Drain current (I_d) vs. Drain voltage (V_d) at different channel lengths



(a) (b)

Figure 3.5 (a) Threshold voltage (V_{th}) vs. Channel length (µm), (b) Cutline to check e-field across 2 µm device

Cutline was drawn along the x-axis horizontally (x1 = 0.03, y1 = - 0.003, x2 = 0.03, y2 = 20) to see the electric field position across the device. A sample cutline to a 2 µm device is shown in Figure 3.5 (b).



(a) (b)

Figure 3.6 (a) Horizontal e-field strength vs. e-field position, (b) Zoomed area of e-field

From Figure 3.6, it is clear that as the device is scaled down, the e-field intensity is decreasing. These changes in the e-field occurred near the drain region of NMOS, whereas in the other areas, the e-field is less affected. To understand the behavior of the e-field, it is compared with the silicon device (Figure 3.7).

Comparing Figure 3.7 with 3.6, it can be observed that in Figure 3.7, the e-field intensity increased when the device was scaled for a silicon device. It means that the behavior of the e-field in SiC devices is exactly the opposite compared to Si. To understand further the reason for the e-field reduction in SiC devices, Equation 2.1 of this thesis was used.

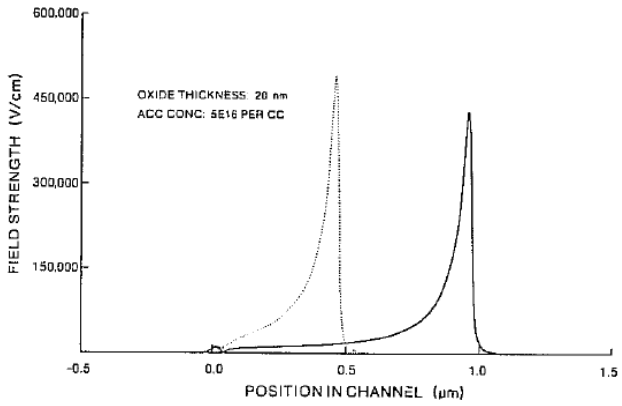
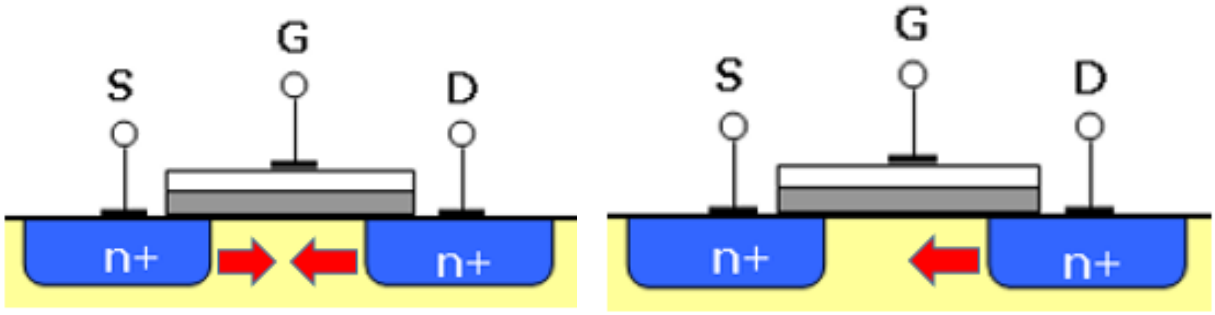


Figure 3.7 Horizontal e-field strength vs. channel length for Si device (1 μm, 0.5 μm) [59]

According to Equation 2.1, 'm' is a constant that depends on the thickness of gate oxide and source and junction depth. That means constant 'm' depends on the vertical scaling of a device which is not done in this thesis. This thesis only considered horizontal scaling. That is why 'm' is said to be a constant in this discussion. The other term, V_{dsat} depends inversely proportional to the channel length. So, in this case, Equation 2.1 would be

$$E_M = (V_d - V_{dsat}) \qquad \text{Equation 3.1}$$

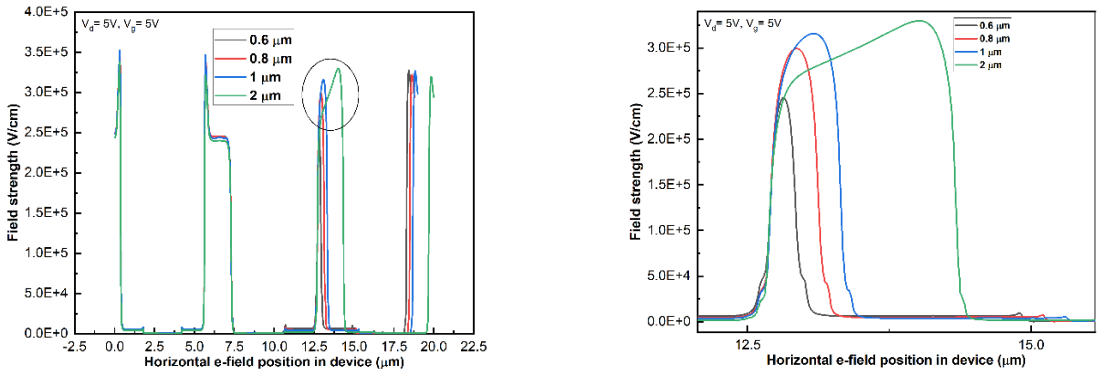
That means when a device is scaled down, E_M decreases.



(a) (b)

Figure 3.8 Channel preparation (a) First approach, (b) Second approach

Now, to understand the shifting of the e-field (as shown in Figure 3.7), two types of design variation were done as shown in Figure 3.8 where S signifies source, G signifies gate, and D signifies drain of MOSFET. In the first approach (Figure (3.8 (a)), both the right side of the source and the left side of the drain were moved towards each other when the channel length was decreased from 2 µm to 0.6 µm. In the second approach (Figure (3.8 (b)), the right side of the source terminal was kept fixed, and the left side of the drain terminal was shifted towards the left or towards the source to prepare the channel when the channel length was decreased from 2 µm to 0.6 µm. A cutline was drawn and the e-field was monitored and shown in Figure 3.9.

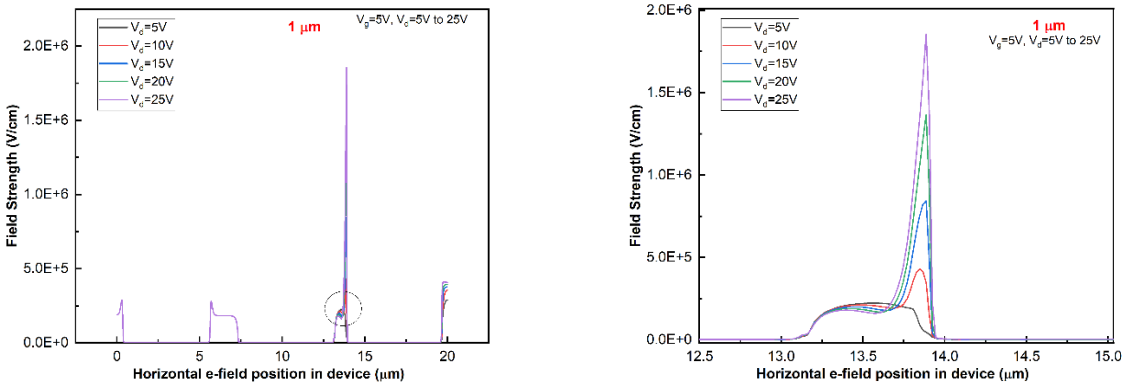


(a) (b)

Figure 3.9 (a) Horizontal e-field strength vs. e-field position, (b) Zoomed area of e-field

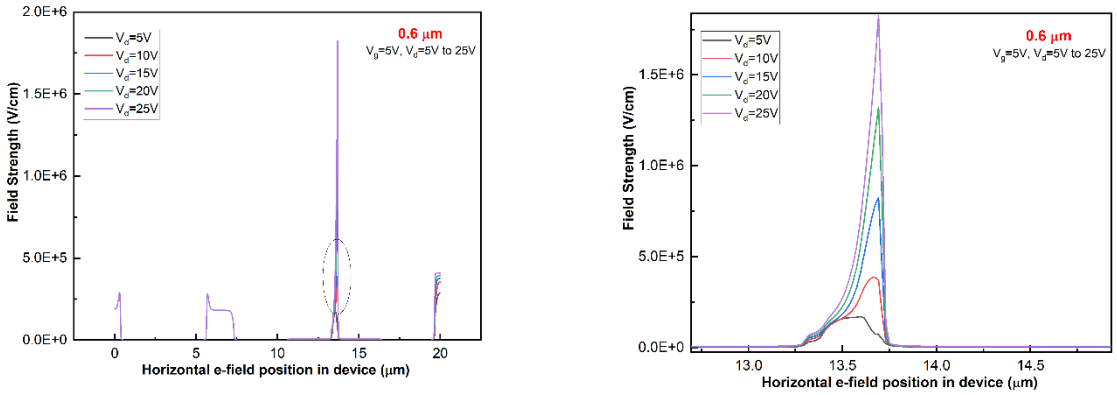
From Figure 3.9 (b) it has been observed that the right side of the e-field was moving with the position of the drain as the channel length was decreased from 2 µm to 0.6 µm. From Figure 3.6 (b) and Figure 3.9 (b), it is clear that the position of the e-field depends on the position of the drain. The intensity of the e-field decreases as the channel length decreases. Another important observation was the position of the maximum e-field that was highest at the point in the channel where the drain terminal starts. This observation matches with Figure 2.8 (a) of the last chapter.

Now, a 1 µm device was taken and V_g was kept fixed at 5V and V_d increased from 5V to 25V (refer to Figure 3.10).



(a) (b)

Figure 3.10 (a) 1 µm horizontal e-field strength vs. e-field position, (b) Zoomed area of e-field



(a) (b)

Figure 3.11 (a) 0.6 µm horizontal e-field strength vs. e-field position, (b) Zoomed area of e-field

Similarly, a 0.6 µm device was taken and V_g was kept fixed at 5V and V_d increased from 5V to 25V and the horizontal e-field was checked (shown in Figure 3.11). Figure 3.11 shows the same

trend as Figure 3.10. To compare the e-field position and intensity in terms of the device channel length, a plot is shown in Figure 3.12, which clearly shows that the e-filed position is shifting towards the left and also e-field intensity increases as the drain voltage (V_d) increased from 5V to 25V keeping gate voltage (V_g) fixed at 5V.

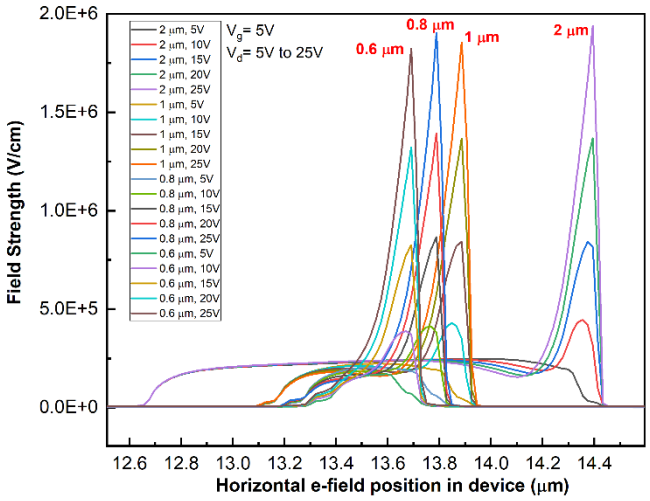


Figure 3.12 Comparison of e-field between 2 µm, 1 µm, 0.8 µm, and 0.6 µm channel length

Next, a model called the 'Classical Lucky electron injection model' was turned on to understand the hot electron current density and e-field [60]. Table 3.2 is shown in this regard.

Table 3.2 Comparison between e-field and hot electron density of 2 µm, 1 µm, 0.8 µm, and 0.6 µm channel length NMOSFET device

Voltage (V_g=5V)	**Maximum e-field (2 µm) (V/cm)**	**Hot electron current density (2 µm) (A/cm^2)**	**Maximum e-field (1 µm) (V/cm)**	**Hot electron current density (1 µm) (A/cm^2)**	**Maximum e-field (0.8 µm) (V/cm)**	**Hot electron current density (0.8 µm) (A/cm^2)**	**Maximum e-field (0.6 µm) (V/cm)**	**Hot electron current density (0.6 µm) (A/cm^2)**
V_d=5V	1.9 e6	1.95 e-22	1.5 e6	1.3 e-15	1.5 e6	5.2 e-13	1.4 e6	1.4 e-10
V_d=10V	3.1 e6	4.8 e-8	3.07 e6	2.2 e-7	2.9 e6	2.6 e-7	2.8 e6	9.1 e-7
V_d=15V	5.6 e6	3.8 e-6	5.6 e6	6.7 e-6	5.5 e6	2.4 e-5	5.3 e6	7.1 e-5
V_d=20V	7.8 e7	8.3 e-6	8.1 e6	1.9 e-5	8.02 e6	5.01 e-5	7.7 e6	1.2 e-4
V_d=25V	1.01 e7	7.4 e-6	1.06 e7	2.2 e-5	1.05 e7	5.4 e-5	1.02 e7	1.3 e-4

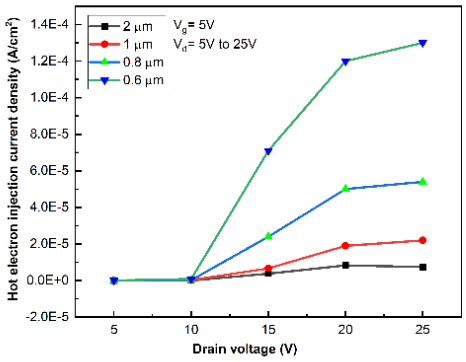


Figure 3.13 Hot electron injection current density (A/cm^2) vs. drain voltage V_g = 5V, V_d = 5V to 25V

From Table 3.2 it can be seen that as V_d was increased from 5V to 25V, the corresponding e-field increased. This trend was common to all four devices. If V_d was fixed at a certain voltage, the maximum e-field remains almost the same for all devices irrespective of channel lengths. However, the interesting point was the amount of hot electron current density that was produced across the devices. When V_d = 5V and the channel was shrunk from 1 µm to 0.8 µm, 400 times hot electron current density was increased. When the channel was shrunk from 0.8 µm to 0.6 µm, 270 times increased. When V_d was changed to 20V, hot electron current density was increasing 2.2 times when the device was shrunk from 2 µm to 1 µm and 2.6 times when shrunk to 0.6 µm. An almost similar increasing trend was visible when V_d changed to 25V. Figure 3.13 shows the hot electron injection density as a function of drain voltage. When the gate voltage was fixed at a certain voltage (5V) and the drain voltage increased from 5V to 25V, the amount of hot electron injection current density was increasing as the channel length was scaled down after the drain voltage crosses 10V. The reason for the generation of hot electrons can be understood from the following equations.

Two types of electric fields are present: lateral electric field and vertical electric field. The e-field equation can be written as:

$$E_{lateral} = \frac{V_{ds}}{L}, where\ L\ is\ the\ channel\ length \quad \text{Equation 3.2}$$

$$E_{vertical} = \frac{V_{gs}}{t_{ox}}, where\ t_{ox}\ is\ the\ thickness\ of\ gate\ oxide \quad \text{Equation 3.3}$$

Due to constant field scaling, $L = \frac{L'}{S}$

Where S is the scaling factor that is greater than 1.

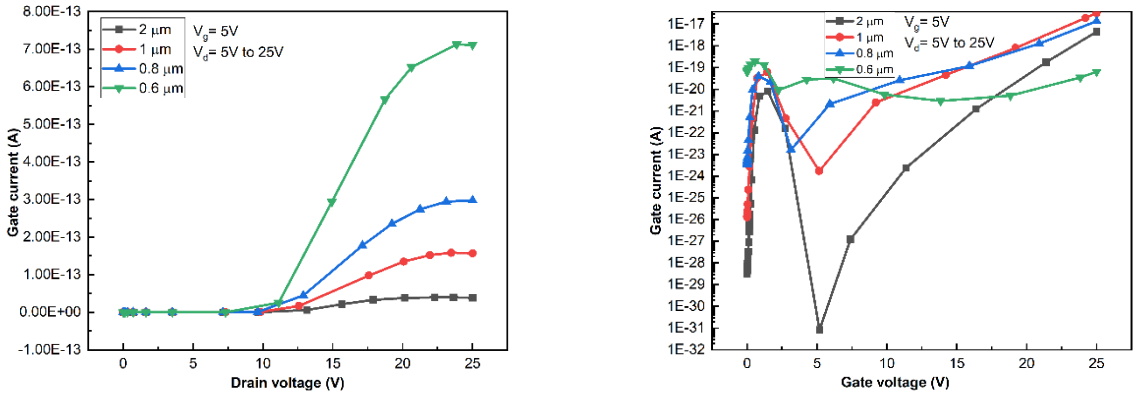
$$Thus, \qquad E_{lateral} = S\frac{V_{ds}}{L'}, \quad \text{Equation 3.4}$$

$$Drift\ velocity, V_{drift} = \mu E_{lateral} \quad \text{Equation 3.5}$$

When a transistor operates in saturation region i.e. when $V_{ds} > V_{dsat}$, pinch-off occurs, and the channel shifts toward the source. When it operates in the saturation region, on one side, V_{ds} is increasing, whereas on the other side, L is decreasing due to the pinch-off. Due to the scaling also, L is decreasing. So, from Equation 3.4, the lateral electric field ($E_{lateral}$) is increasing. Thus, from Equation 3.5, V_{drift} is increasing which means electrons are moving with a very high velocity and their kinetic energy is increasing. This is how hot electrons are generated.

As the increasing trend of hot electrons was observed while the device was shrunk from 2 μm to 0.6 μm, the effect of hot electrons on the device was examined. In Chapter 2, it has been mentioned that the effect of hot electrons can be seen in terms of gate leakage. For that reason, gate leakage has been monitored by keeping V_g fixed at 5V, and V_d was varied from 5V to 25V. In Figure 3.14 (a) it can be seen that when the channel length was reduced from 1 μm to 0.8 μm at V_d = 20V, gate leakage increased more than 2 times (Figure 3.14 a). Similarly, when the device was shrunk from 1 μm to 0.6 μm at V_d = 20V, gate leakage increased 7 times (Figure 3.14

(a). Figure 3.14 (b)) shows gate leakage variation when the drain voltage was fixed at 5V and the gate voltage increased from 5V to 25V. The gate current (I_g) was increased almost exponentially after 10V.



(a) (b)

Figure 3.14 (a) Gate current (I_g) vs. drain voltage (V_d) at V_g = 5V, V_d = 5V to 25V, (b) Gate current (I_g) vs. gate voltage (V_g) at V_d = 5V, V_g = 5V to 25V

Figure 3.15 shows the variation in the total current density of the devices as a function of drain voltage. At any particular drain voltage, the total current density of the devices are increasing when the dimensions are decreased. As mentioned in the previous chapter when the device goes into saturation region and drain voltage increases, the electrons become energetic and attracted towards the gate terminal leaving holes behind. The holes are then attracted toward the substrate and constitute a substrate current. As a result, substrate current is another phenomenon of hot carrier effects.

Now, the maximum amount of substrate current (for 2 µm, 1 µm, 0.8 µm, 0.6 µm devices) was plotted against a varying drain voltage (5V, 10V, 15V, 20V, and 25V) keeping gate voltage fixed at 5V, but no clear trend was observed.

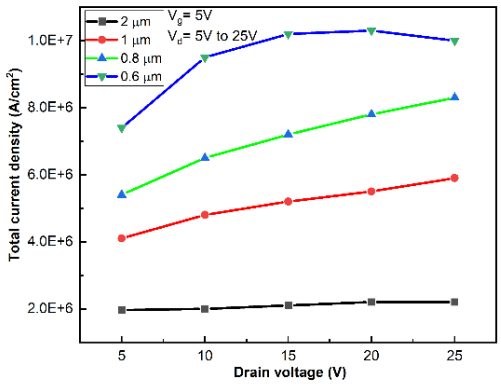


Figure 3.15 Total current density of 2 µm, 1 µm, 0.8 µm, and 0.6 µm devices at V_g = 5V, V_d = 25V

According to the research paper [54], the conventional method to observe hot carrier effects is not reliable for 4H-SiC. So, these graphs are not shown in this thesis. The maximum substrate current was found in the range of 10^{-22} to 10^{-24} Ampere for 0.8 µm and 0.6 µm device when V_d reaches 25V.

As Avalanche generation or impact ionization is the key process to generate electron-hole pairs, which in turn create substrate current, so avalanche process was observed in the devices. The keywords ('eAvalanche' and 'hAvalanche') were used to turn on Avalanche mode in Sentaurus. The default 'Overstraeten- de Man model' was used to understand the electron impact ionization process which calculates based on the electron temperature and the 'Okuto-Crowell' model was used for holes [57].

In Figure 3.16, the Avalanche process is shown in a 1 µm device. When V_d was fixed at a certain voltage and V_g increased, the avalanche region was spreading but the value of impact ionization was constant (4.38 e-3 /cm^3s). That signifies the device did not reach saturation region. The Avalanche direction was moving from the drain to the source terminal (refer to Figure 3.16).

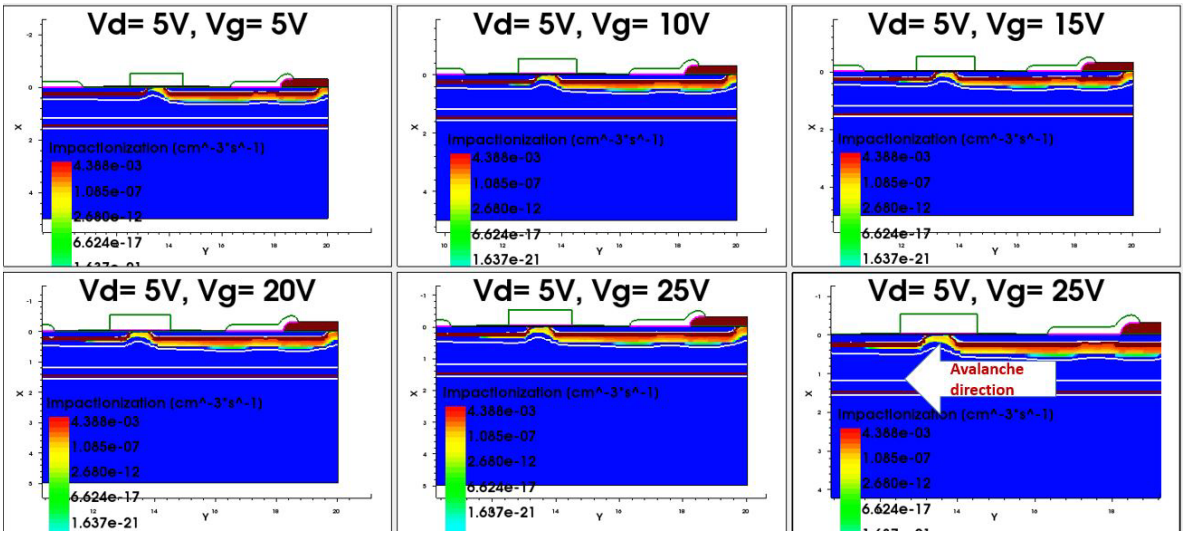


Figure 3.16 Avalanche direction of 1 μm device at V_d =5V, V_g = 5V to 25V

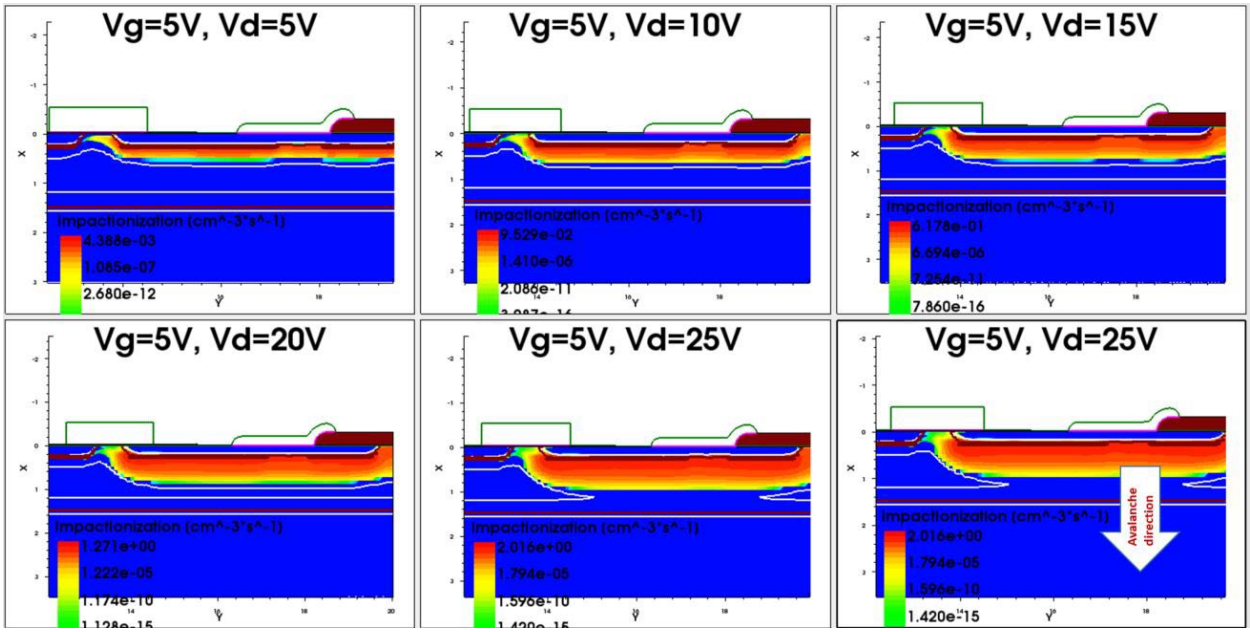


Figure 3.17 Impact ionization of 1 μm device at V_g =5V, V_d = 5V to 25V

However, when V_g was fixed at 5V, and V_d was increased from 5V to 25V, the avalanche direction was from the drain to the body (Figure 3.17).

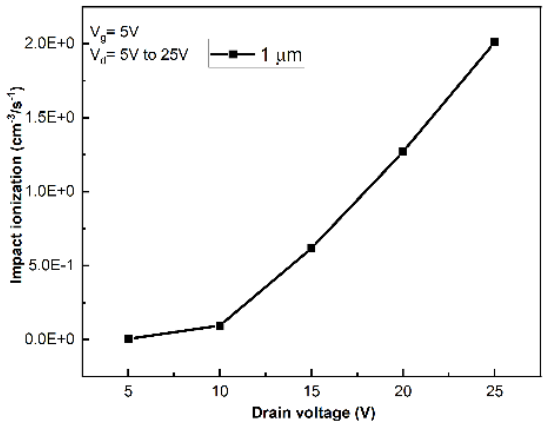


Figure 3.18 Impact ionization vs. drain voltage of 1 µm device at V_g =5V, V_d = 5V to 25V

From Figure 3.18 it has been clear that as the drain voltage increases, the avalanche process started increasing. The avalanche process increases rapidly when the drain voltage crosses 10V. This can be confirmed by Figure 3.17, where due to the impact ionization, the red zone (current density) was spreading as V_d increased from 5V to 25V.

Chapter 4. Low-Doped Drain NMOSFET Device Simulation and Characterization

4.1 Device Simulation with Low-Doped Drain

As mentioned in Chapter 2, Low doped drain (LDD) has been used to reduce hot carrier effects in silicon devices. But whether LDD is beneficial for SiC or not, is still unknown. To understand the viability of LDD design in SiC, two NMOSFETs were simulated with different channel lengths (0.8 µm, 0.6 µm) with LDD design. Now a question may come why LDD structure was chosen to implement in SiC for channel lengths 0.6 µm and 0.8 µm? The answer is hidden in the evolution of technologies for silicon devices. The effective channel lengths of Si devices are matched with SiC devices. For silicon devices, especially in Twin tub IV (L_{eff} = 1 µm), twin tub V (L_{eff} = 0.75 µm), and twin tub VI (L_{eff} = 0.4 µm)) technologies, LDD was used [5]. In this research, the effective channel length of 4H-SiC LDD devices was 0.6 µm and 0.4 µm respectively for 0.8 µm and 0.6 µm devices. Thus, 0.8 µm and 0.6 µm channel lengths were chosen to implement the LDD structure in SiC.

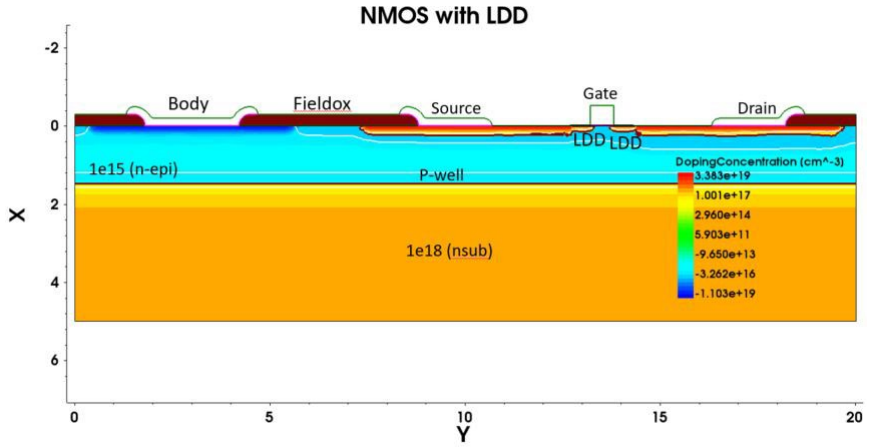
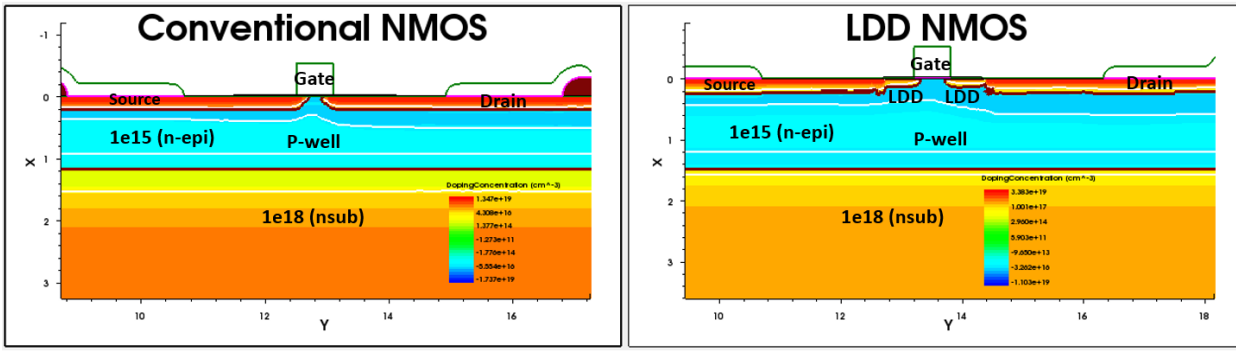


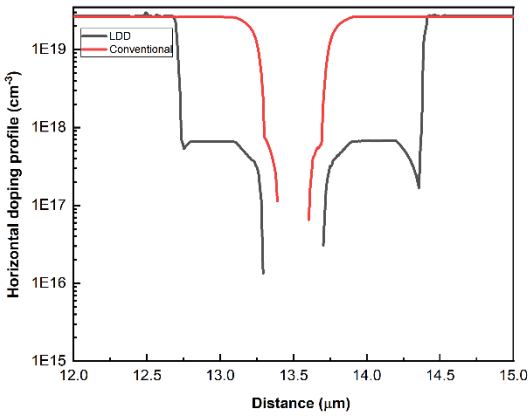
Figure 4.1 NMOSFET (0.6 µm channel length) with LDD region

To simulate the LDD region in NMOSFET, phosphorus was chosen and ion implantation was used @25 keV at a temperature of 500 °C. The maximum depth of the LDD region was

found 138 nm and the length of LDD was 500 nm. Figure 4.2 (a) shows the conventional and LDD NMOSFET, and Figure 4.2 (b) comparison between their doping profiles near the drain region.



(a)



(b)

Figure 4.2 (a) NMOS LDD structure and NMOS conventional structure, (b) Comparison of doping profile between LDD and conventional NMOSFET (0.6 μm channel length)

The junction depth of LDD was kept lowered compared to the junction depth of conventional source and drain design. This is because shallow junction minimizes the short channel effect and helps to reduce V_{th} roll-off. Also, shallow junction reduces drain-induced barrier lowering

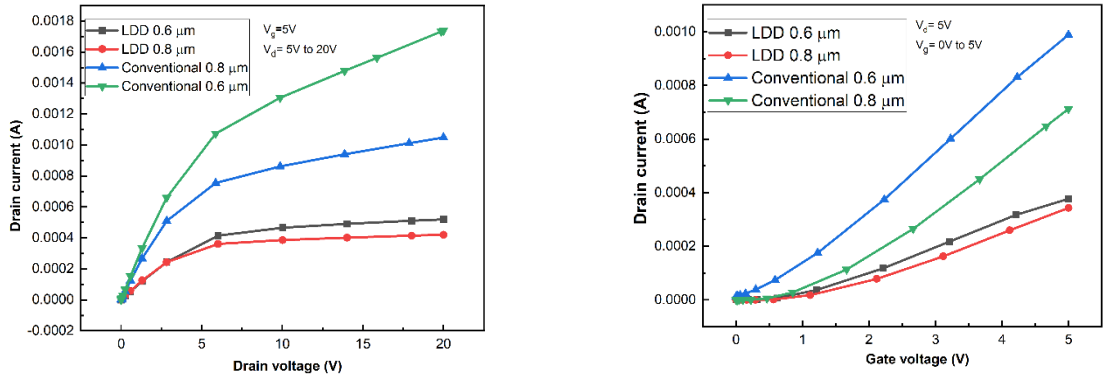
(DIBL) [5]. However, there are some disadvantages of shallow junctions such as parasitic resistance increases (discussed in the next sections) and difficulties in forming reliable contact.

4.2 Device Characterization

The drawn channel length and effective channel length of LDD NMOSFET are mentioned in Table 4.1.

Table 4.1 The channel length of LDD NMOSFET.

Drawn channel length (L_{drawn}) (µm)	**Effective channel length (L_{eff}) (µm)**
0.8	0.6
0.6	0.4



(a) (b)

Figure 4.3 (a) Comparison between I_dV_d of LDD and conventional NMOSFET, (b) Comparison between I_dV_g of LDD and conventional NMOSFET

Figure 4.3 (a) shows the comparison of I_dV_d between LDD (0.6 µm, 0.8 µm) and conventional (0.6 µm, 0.8 µm) design. The drain voltage up to 20V was varied. From Figure 4.3 (a) a clear improvement in the saturation current was visible. The improvement in the saturation current was visible for both 0.6 µm and 0.8 µm LDD devices. Thus, it is confirmed that with LDD design, the short channel effect of NMOSFET can be minimized. Figure (4.3 (b)) shows

the I_dV_g characteristics of LDD and conventional NMOSFET. Figure 4.4 shows the V_{th} roll-off behavior between conventional and LDD where it can be seen that V_{th} roll-off is less in LDD NMOSFET.

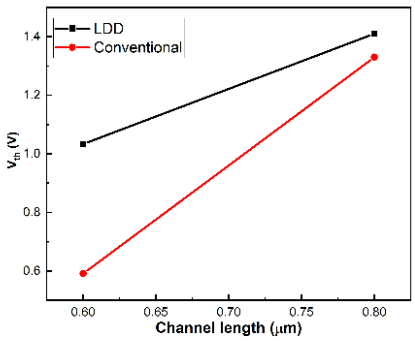
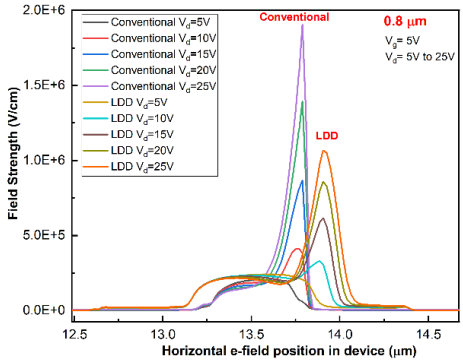
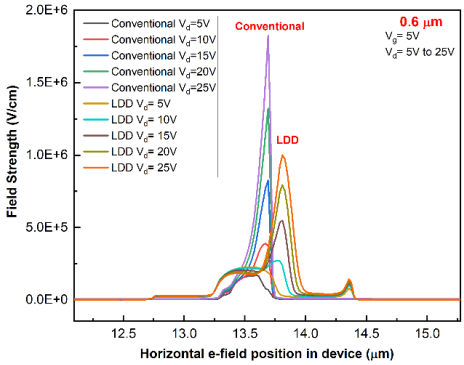


Figure 4.4 V_{th} roll-off comparison for LDD and conventional NMOSFET

Next, the e-field behavior of LDD-NMOSFET and conventional NMOSFET was observed. For LDD, as the changes were implemented only in the channel region, so horizontal e-field in the drain region was focused to observe the changes.





(a) (b)

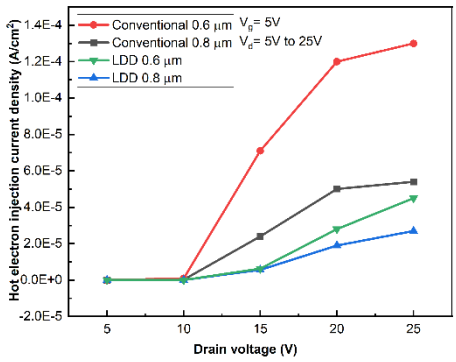
Figure 4.5 (a) Comparison of e-field between conventional and LDD NMOSFET (0.8 μm), (b) Comparison of e-field between conventional and LDD NMOSFET (0.6 μm)

Figure 4.5 (a, b) shows the e-field behavior of LDD and conventional NMOSFET where it can be seen that field intensity was decreased almost two times (at 15V, 20V, and 25V) for both 0.6 µm and 0.8 µm channel length LDD compared to conventional NMOSFET.

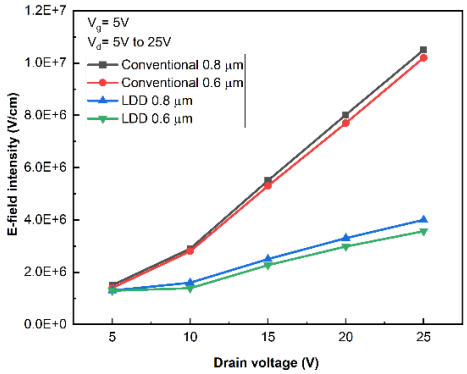
Next, in the simulation again 'Classical Lucky electron injection model' was turned on to understand the hot electron current density and e-field [60] in the LDD NMOSFET structure. Table 4.2 gives the maximum hot electron current density and e-field for conventional and LDD NMOSFET. Figure 4.6 (a, b) shows the comparative analysis of e-field intensity and hot electron injection density between LDD and conventional NMOSFET. This data has been expressed in terms of graphs for better understanding. From Table 4.2, when the channel length = 0.6 µm and drain voltage = 10V, hot electron injection density was almost 112 times lower for LDD NMOSFET compared to the conventional design. The e-field was 2 times lower in LDD NMOSFET when the drain voltage was 10V. The critical e-field of SiC is 3 MV/cm i.e. when the channel length was 0.6 µm, the conventional design MOSFET can absorb only 10V of drain voltage, whereas, the LDD design can absorb (20V - 25V) (refer to Figure 4.6 (b)). This signifies that the breakdown voltage of LDD is much higher than conventional NMOSFET which in turn means that the stability of the LDD device is better than conventional design.

Table 4.2 Comparison between e-field and hot electron density of LDD NMOSFET vs. conventional NMOSFET of channel length 0.8 µm and 0.6 µm

Voltage (V_g=5V)	**Conventional max-e-field (0.8 µm) (V/cm)**	**Conventional hot electron current density (0.8 µm) (A/cm^2)**	**Conventional max-e-field (0.6 µm) (V/cm)**	**Conventional hot electron current density (0.6 µm) (A/cm^2)**	**LDD max-e-field (0.8 µm) (V/cm)**	**LDD hot electron current density (0.8 µm) (A/cm^2)**	**LDD max e-field(0.6 µm) (V/cm)**	**LDD hot electron current density (0.6 µm) (A/cm^2)**
V_d=5V	1.5 e6	5.2 e-13	1.4 e6	1.4 e-10	1.3 e6	3.2 e-17	1.29 e6	3.1 e-16
V_d=10V	2.9 e6	2.6 e-7	2.8 e6	9.1 e-7	1.6 e6	4.5 e-8	1.39 e6	8.1 e-9
V_d=15V	5.5 e6	2.4 e-5	5.3 e6	7.1 e-5	2.5 e6	5.6 e-6	2.27 e6	6.3 e-6
V_d=20V	8.02 e6	5.01 e-5	7.7 e6	1.2 e-4	3.3 e6	1.9 e-5	2.98 e6	2.8 e-5
V_d=25V	1.05 e7	5.4 e-5	1.02 e7	1.3 e-4	4.0 e6	2.7 e-5	3.57 e6	4.5 e-5



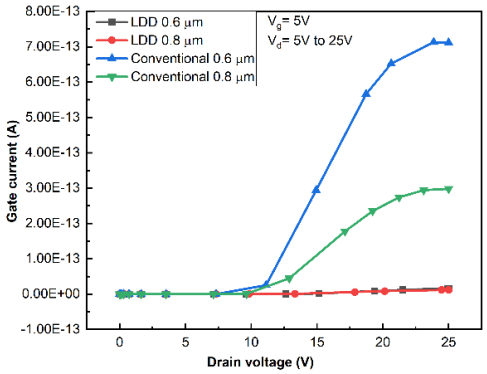
(a)



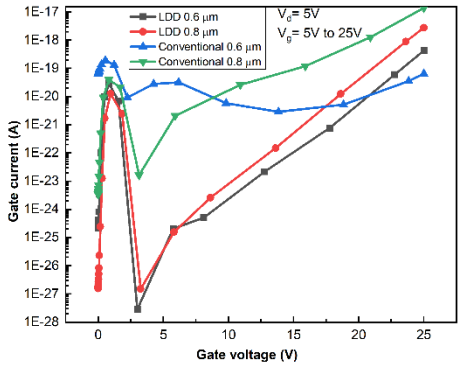
(b)

Figure 4.6 Comparative analysis of (a) hot electron injection density, (b) e-field intensity between conventional and LDD NMOSFET (0.8 µm, 0.6 µm)

To understand the improvement of gate leakage in the LDD structure, gate current was plotted against drain voltage (Figure 4.7 (a)). For channel lengths 0.6 µm and 0.8 µm, the LDD structure reduced the gate leakage to a significant amount compared to conventional NMOSFET at $V_d \geq$ 10V. LDD designs show zero gate leakage whereas conventional devices show leaky behavior.



(a)



(b)

Figure 4.7 (a) Comparative analysis of gate leakage vs. drain voltage between conventional and LDD NMOSFET (0.8 µm, 0.6 µm), (b) Comparative analysis of gate leakage vs. gate voltage between conventional and LDD NMOSFET (0.8 µm, 0.6 µm)

Figure 4.7 (b) shows the gate leakage variation with gate voltage. When the gate voltage was increased up to 25V by keeping V_d = 5V, gate leakage for LDD NMOSFET was following the same pattern as conventional NMOSFET. However, the LDD designs were showing less gate leakage compared to conventional NMOSFET.

According to Stanley Wolf [5], the substrate current (Isub) depends on the effective channel length (Leff) of MOSFET. Figure 4.8 shows a lesser substrate current in long-channel Si devices. In this thesis, the effective channel lengths of LDD NMOSFETs are slightly higher than conventional NMOSFETS (shown in Table 3.1 and Table 4.1). Thus, a lesser substrate current is expected from LDD NMOSFET than from conventional design. At V_d = 25V, and V_g = 5V, the LDD NMOSFETs (0.8 μm and 0.6 μm) were showing a substrate current of 10^{-28}A to 10^{-27}A, compared to conventional NMOSFETs (0.8 μm and 0.6 μm) which showed a substrate current of 10^{-24}A to 10^{-22}A. However, from 5V to 25V, the graphs of substrate current did not show a clear trend, so they are not presented in this thesis. Now, the substrate current is divided into hole current and electron current. Although the electron current did not show a good trend, the hole current showed a good trend as shown in Figure 4.9.

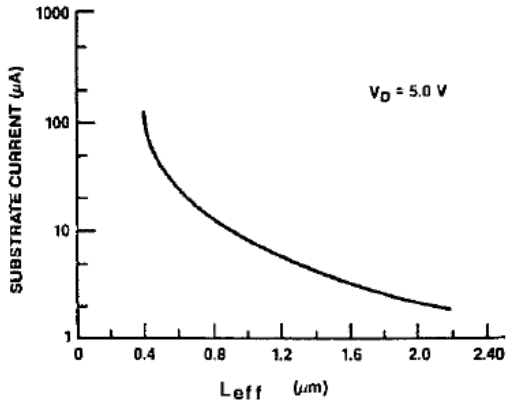


Figure 4.8 Maximum substrate current vs. L_{eff} for Si MOSFETs with t_{ox} = 25 nm [59]

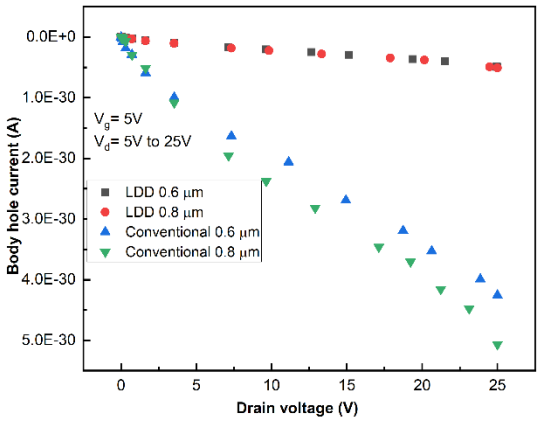


Figure 4.9 Body hole current vs. drain voltage between conventional and LDD NMOSFET (0.8 µm, 0.6 µm)

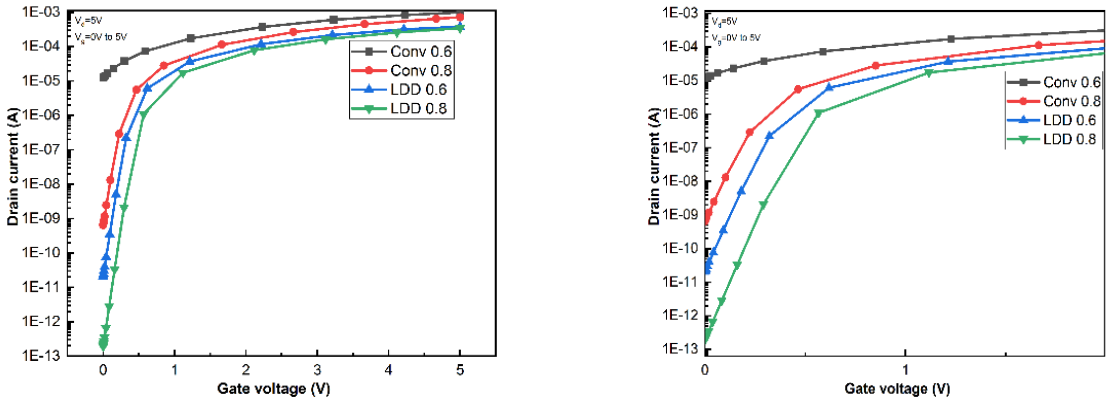
From Figure 4.9 it can be seen that the LDD NMOSFETs show a lesser body hole current compared to conventional NMOSFETs.

One of the important device characteristics in the subthreshold region is the subthreshold slope or subthreshold swing (S_t). This characteristic indicates how effectively a MOSFET can be turned off below V_{th}. Ideally, no current is expected below a turned-on voltage or V_{th}. When the gate voltage (V_{gs}) is zero, the drain current (I_d) should be zero, but practically, there is always some current which is known as I_{off} current. From Figure 4.10 (a) it has been observed that when the gate voltage is zero, the amount of drain current was higher for the conventional device than for LDD. This signifies the off current for the conventional devices is higher compared to LDD devices. The formula (Equation 4.1) of subthreshold swing (S_t) is used to calculate the subthreshold swing of conventional and LDD NMOSFETs. Figure (4.10 (b)) shows that when the channel length was 0.6 µm, the slope of the LDD device was more than conventional NMOSFET. That signifies that the power loss of the conventional device will be more than LDD NMOSFET when the device operates below the threshold voltage.

$$S_t = ln10\left(\frac{dlnI_d}{dV_{gs}}\right)^{-1}$$ Equation 4.1

Table 4.3 Comparison between subthreshold characteristics of conventional and LDD NMOSFET

Device	**V_{th} (V)**	$\frac{I_{on}}{I_{off}}$	**Subthreshold swing (S_t) (mV/decade)**
LDD 0.6	1.033	1.25 e6	7.67
LDD 0.8	1.41	1.1 e8	7.68
Conv 0.6	0.59	5.67	6.97
Conv 0.8	1.33	1.01 e5	7.29



(a) (b)

Figure 4.10 (a) Comparative analysis of subthreshold characteristics of conventional and LDD NMOSFET (0.8 µm, 0.6 µm), (b) Magnified region below the threshold voltage

From Table 4.3 it can be seen that the $\frac{I_{on}}{I_{off}}$ ratio for LDD devices is very high which signifies that the leakage is smaller compared to conventional devices. One point noted here is for a channel length of 0.6 µm, a conventional device shows a high leakage current. The subthreshold slope of all of these devices are almost comparable, however, conventional devices show lower S_t values which mean small V_{gs} are required to turn off these devices compared to LDD devices [59].

4.3 Advantages and Disadvantages of the Proposed Solution

The comparison of device parameters between conventional and LDD NMOSFET is shown in Table 4.4. It can be noted that transconductance for an LDD device is smaller compared to the conventional design and smaller transconductance means it requires more amount of voltage across its gate to produce current. This can be confirmed by the I_dV_g graph shown in Figure 4.3(b).

Table 4.4 Comparison of device parameters between LDD and NMOSFET

Channel length	**Transconductance (g_m)**		**Threshold (V_{th})**	
	LDD	**Conventional**	**LDD**	**Conventional**
0.6	9.16 e-5	2.0 e-4	1.03	0.59
0.8	8.51 e-5	1.6 e-4	1.41	1.33

On the other hand, from Table 4.3 it is noted that the performance of the LDD device in terms of the subthreshold characteristics is better than the conventional design NMOSFET. The hot electron current density produced at LDD devices is much lower than in a conventional design and the e-field intensity is also lower in LDD devices (Figure 4.6). Figure 4.6 (b) shows that LDD devices are capable of absorbing more voltages (20V - 25V) compared to conventional devices that can handle up to 10V before reaching the critical e-field of SiC (3 MV/cm).

To overcome the hot electron effects in a device, the electric field must be reduced. For an LDD device, the doping in the LDD region is reduced which means the depletion width (W_d) is increased. It can be seen from Equation 4.2 below.

$$Depletion\ width, W_d = \sqrt{\frac{2\epsilon}{q}\left[\frac{1}{N_A}+\frac{1}{N_D}\right]V_b}, \qquad \text{Equation 4.2}$$

$$V_b = V_t \ln\left[\frac{N_A N_D}{n_i^2}\right] \text{ where } V_t \text{ is the threshold voltage,} \quad \text{Equation 4.3}$$

$$Breakdown\ voltage, V_{br} = \frac{1}{2} W_d E_{cr} \quad \text{Equation 4.4}$$

where N_A, N_D are acceptor and donor atoms concentration, n_i is the intrinsic carrier concentration, V_b is the barrier potential, ϵ is the electrical permittivity, E_{cr} is the critical electric field. From Equation 4.4, it can be seen that when W_d is increasing, breakdown voltage (V_{br}) is increasing. Again, from basic electrostatics, it was known that, $E = \frac{V_b}{W_d}$, where V_b is the barrier potential. This signifies that when depletion width (W_d) increases, and the electric field (E) decreases.

Figure 4.7 confirms that the gate leakage for the LDD device is smaller compared to the conventional design NMOSFET. The LDD devices have shown zero gate leakage compared to conventional devices that show higher leakage currents. From Figure 4.3 it can be noted that the current drive capability of conventional devices is higher than LDD devices. The most obvious reason is that adding two LDD (n-) regions in between the source and drain signifies the addition of two lower-doped regions along the current path. That means a higher resistance is existing along the current path. The resistance of this LDD (n-) region depends on the length of LDD (L_n^-) and the doping concentration of the (n-) region. The variation of both of these determines the effectiveness of LDD in an NMOSFET. If the doping concentration is too high means the LDD region will be an extension of the n+ region and sufficient reduction of the e-field cannot be achieved [59]. If the doping is too low, means there will be hardly any difference in LDD compared to conventional NMOSFET because a high e-field will stay in the n+ region. On the other hand if L_n^- is high then the R_n^- value will be high. Research suggests that hot electron

protection will be maximum if the maximum e-field lies under the gate [59]. Here in 0.8 μm and 0.6 μm LDD devices, the maximum e-field is located under the gate.

Chapter 5. Proposed Advanced CMOS Process

The benefits of LDD NMOSFET over conventional NMOSFET are well understood and also its associated disadvantages are clear from previous chapters. To implement LDD in the SiC CMOS process, first, the associated changes need to be discussed. These changes consist of a spacer structure, extra masks for LDD, doping methods, and dopant species.

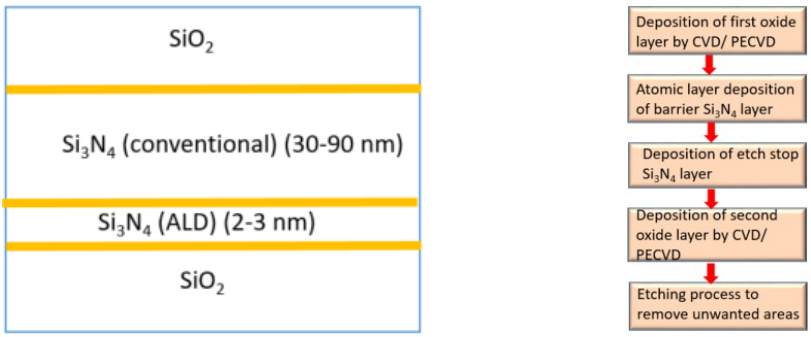
5.1 Proposed Spacer structure

Spacers consist of dielectric layers which are formed after the formation of the gate. In silicon technology, a spacer is an integral part of scaling. After gate formation, the photoresist is applied on top of the gate, patterned, and etched undesired portions of the dielectric layer. The remaining portions of the dielectric layer which includes the vertical sidewall of the gate, and small horizontal portions adjacent to vertical portions, become spacer [61]. In previous chapters, where the simulations or virtual fabrications were done, a spacer was not required because ion implantation can be done in a selective region very easily and precisely. However, in lab fabrication, the situation will be different. Especially for silicon devices, spacers are used to protect the LDD region. Spacers provide some other benefits as well. Spacers are used as a mask during source and drain implantation, help to insulate gate structure from source and drain, control the parasitic resistance, and can help to lower leakage in MOSFET [62].

(a) (b)

Figure 5.1 (a) Gate without spacer, (b) Gate with spacer [63]

Figure 5.1 shows the gate structure with and without a spacer. In spacers, as most of the portions are vertical so single layer spacers suffer non-uniformity problems and overhang issues [62]. When the dimensions are low, these issues affect the performance of a transistor. A composite spacer formed by oxide-nitride-oxide (ONO) can be a solution to this problem. As this thesis is focused on the submicron range, the ONO structure can be beneficial. Also, Si_3N_4 which is part of an ONO spacer is extensively used in SiC D-MOSFET [64]. Research suggests that Cree and Purdue University have used Si_3N_4 in their CMOS process. In the ONO structure, a silicon nitride (Si_3N_4) layer is sandwiched between two SiO_2 layers. silicon nitride is divided into two portions where the upper portion is prepared by a conventional deposition process such as CVD/ PECVD (30 - 90 nm), followed by atomic layer deposition (ALD) of a silicon nitride layer (2 - 3 nm). The purpose of each layer is mentioned in Table 5.1.



(a) (b)

Figure 5.2 (a) ONO spacer structure, (b) Proposed method of ONO spacer [62]

Table 5.1 Purpose of each layer [62]

Layer	Purpose
SiO_2	Isolate Si_3N_4 from the SiC surface. It can reduce stress at Si_3N_4/ SiC surface.
Si_3N_4	Helps to control the spacer width due to its high selectivity compared to SiO_2.
ALD	Helps SiO_2 from being nitridize.

As SiO_2 is a dielectric, the reason for using another dielectric (silicon nitride) (as shown in the ONO structure) can create a question in mind. In this structure, the silicon nitride (Si_3N_4) layer is proposed to use along with the SiO_2 layer because silicon nitride has a higher dielectric constant (7 - 7.5) than SiO_2 (3.8 - 3.9). Also, silicon nitride has solid microstructures without microchannels compared to SiO_2 [62] which helps to stop the diffusion of oxygen at higher temperatures (1000°C) [61]. Compared to SiO_2, silicon nitride has a high concentration of electrons and hole traps (~10^{19}) and these traps are deep and have high energy (1.4 – 1.6 eV). Thus in comparison to SiO_2, charges get trapped into the nitride layer more and thus help to reduce leakage. On the other side, during the growth of silicon nitride, ammonium precursor is used. Ammonium precursors nitridize oxide layers and convert them to oxynitride (Si_2ON_2) which generates stress in the corner of gate oxide [62]. The equation can be mentioned as:

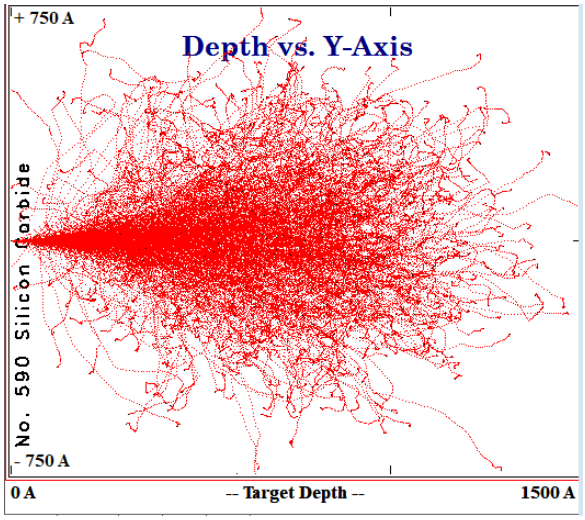
$$2SiO_2 + 2NH_3 = Si_2ON_2 + 3H_2O$$

This stress is a feature size stress and leads to the deactivation of acceptors and donors in channel regions which degrades the drive current. To reduce the stress, the ALD nitride layer is used because the ALD process does not need any ammonium precursor. However, the ALD process is time-consuming and expensive. So a thin ALD layer (2-3 nm) is proposed instead of a total Si_3N_4 layer grown by ALD.

5.2 Proposed Doping Methods and Dopants for LDD

The reason for using the ion implantation process to grow LDD is described in this section. Ion implantation has been used extensively to grow LDD regions in silicon devices. As the diffusion process does not work well with SiC due to the lower diffusivity of dopants, an ion implantation process is proposed. Nitrogen (N) and phosphorus (P) are commonly used as n-type dopants for SiC. The atomic weight of N is 14 and P is 30. Due to the lighter weight, N can go

deep during ion implantation even at very low energy. Now, the lowest implantation energy that can be achieved by any ion implanter is 30 keV [59]. SRIM suggests that at 30 keV, nitrogen gives a depth of around 150 nm in SiC, whereas phosphorus gives a depth of 100 nm. That means phosphorus can be used to make a shallow region. The straggle (R_p) of nitrogen shows 267 A (Figure 5.3 (b)) whereas phosphorus shows 156 A. This signifies that nitrogen ions are penetrating far, compared to phosphorus. Now, it is difficult to create an amorphous layer for atoms having lower atomic weight. Thus crystalline defects that are formed by nitrogen need very high-temperature annealing [59] compared to phosphorus due to its higher atomic weight. Additionally, compared to nitrogen, phosphorus shows high mobility and lower sheet resistance [65]. On the other hand, two other n-type dopants (As, Sb) could also be used in TCAD simulation, but they possess a lower activation rate despite having higher carrier mobility compared to N and P [65].



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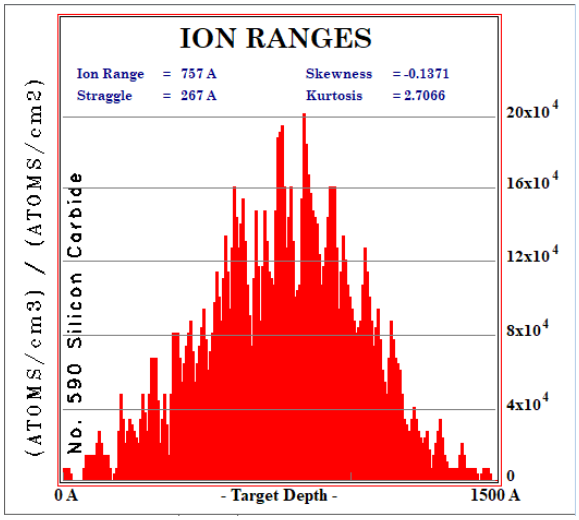

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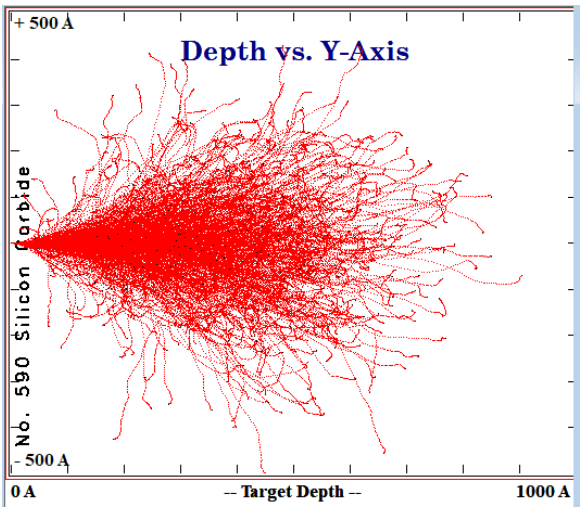

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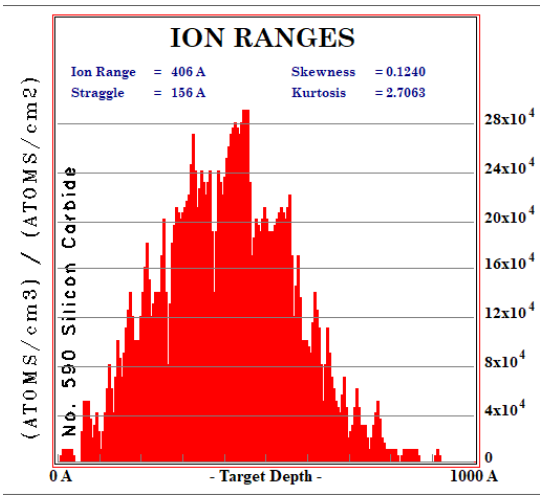


(d)

Figure 5.3 (a) Depth of nitrogen at 30 keV in SiC, (b) Ion range of nitrogen, (c) Depth of phosphorus at 30 keV in SiC, (d) Ion range of phosphorus

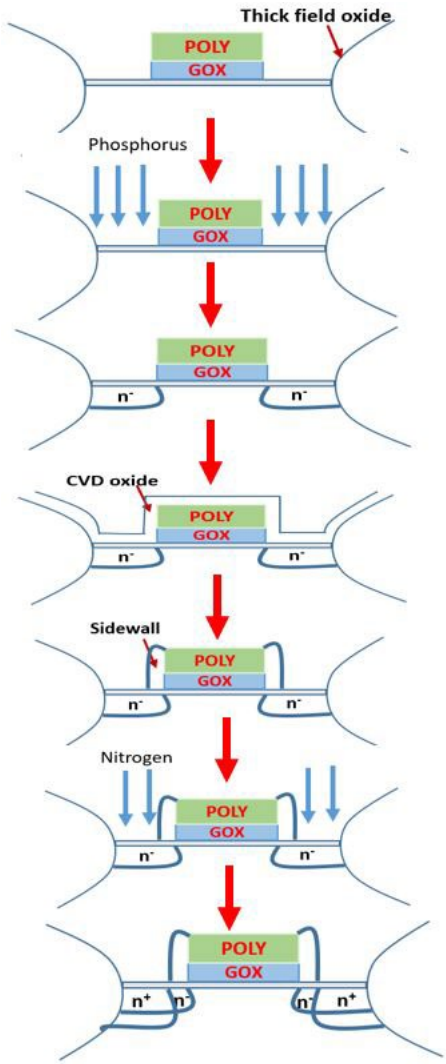
5.3 Realization of LDD structure

5.3.1 LDD in Silicon

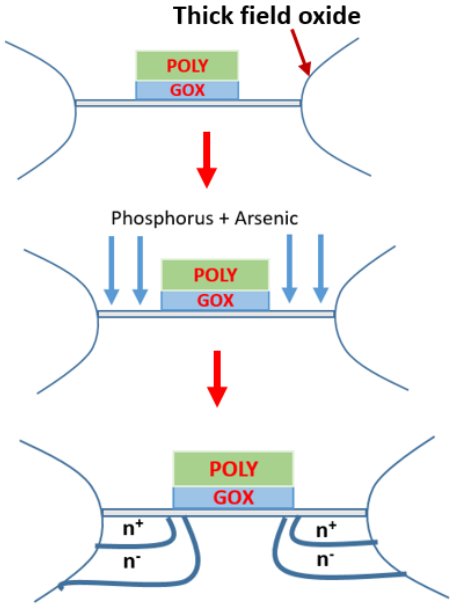
The LDD structure has been realized in many ways in silicon devices. Figure 5.4 shows two ways to implement LDD in silicon. In process 1, after polysilicon is patterned, phosphorus is implanted at a low dose to introduce an n- region. This process is followed by growing a CVD oxide layer and then anisotropic etching, which ensures only the vertical portion of the sidewall is retained and the horizontal portion is stripped off. Then the second implantation is done with a high dose of nitrogen to ensure a deeper n+ region.

In process 2, double implantation is done with phosphorus and arsenic. Due to heavy mass, arsenic ion creates a shallow n+ region. Phosphorus has a large straggle compared to arsenic which ensures deep implantation and lateral projection. Among these two processes, the first method gives better control over the LDD length because it is controlled by the width of the spacer. However, the second process is less complex compared to the first process due to the use

of two ions at the same time during implantation. In the silicon carbide platform, the second process can be implemented easily compared to the first because the second process has less dependency on the gate.



(a)



(b)

Figure 5.4 LDD realization in Si (a) First Process, (b) Second Process

5.3.2 LDD in SiC

The above LDD realization technique applies to Si devices, but the tricky question is how it can be implemented in SiC since it has not been applied yet in SiC. Using the epitaxial process, self-alignment is possible by creating a groove. This method was demonstrated by General Electric Company [66]. However, using the epitaxial process, LDD design may not be possible because LDD needs to reside at the same level as the source/ drain which is difficult to grow in epitaxy.

A non-self-alignment technique to realize LDD in SiC is proposed in Figure 5.5. A thin oxide layer is to be grown on the surface and patterned first and then an LDD implant can be done. After that, a thick SiO_2 layer will be grown on the surface. The thickness of SiO_2 should vary depending on the ion implantation energy. Thick oxides are capable of absorbing higher energy implants, so a thick oxide layer is proposed on the top surface. Following that, the oxide will be patterned and a high-energy implant will be done to create a source and drain region. Then gate oxide and polysilicon will be grown/ deposited and patterned. In this process, higher-temperature annealing is possible. Unlike silicon, lateral diffusion is less effective in SiC. Thus, an LDD implant seems to be possible using an extra mask because the implant species will stay near the implanted position due to less diffusivity of dopants in SiC. Another point is, the bond length/ interatomic distance between Si and C atom is less in SiC, so a shallow implant is easier in SiC compared to silicon. However, the critical step in this process is the alignment of the gate. If the gate is not overlapped between the source and drain then the channel won't form which means a current won't flow in the MOSFET. On the other hand, high overlapping means capacitance will increase which will generate a delay in the transistor.

A self-alignment gate technique using ion implantation has been demonstrated by a researcher from Dr. Kornegay's group at Purdue University [67]. Nitrogen has been used as a dopant on 6H-SiC. The thermal annealing process was tried at a lower temperature (900 °C – 1200 °C) for a long duration (up to 64 hours). The researcher mentioned that the success of annealing depends not only on temperature but on time also. Thus, lower temperatures but long hours can be the key to success in this self-alignment process. However, the selection of appropriate dopants is equally important in this process where the ionization energy of an ion plays a key role. Nitrogen has lower ionization energy in 4H-SiC (50 - 92 meV) compared to 6H-SiC (85 – 140 meV) [58]. As this thesis is focused on 4H-SiC, so activation will be better if nitrogen will be used in 4H-SiC compared to 6H-SiC.

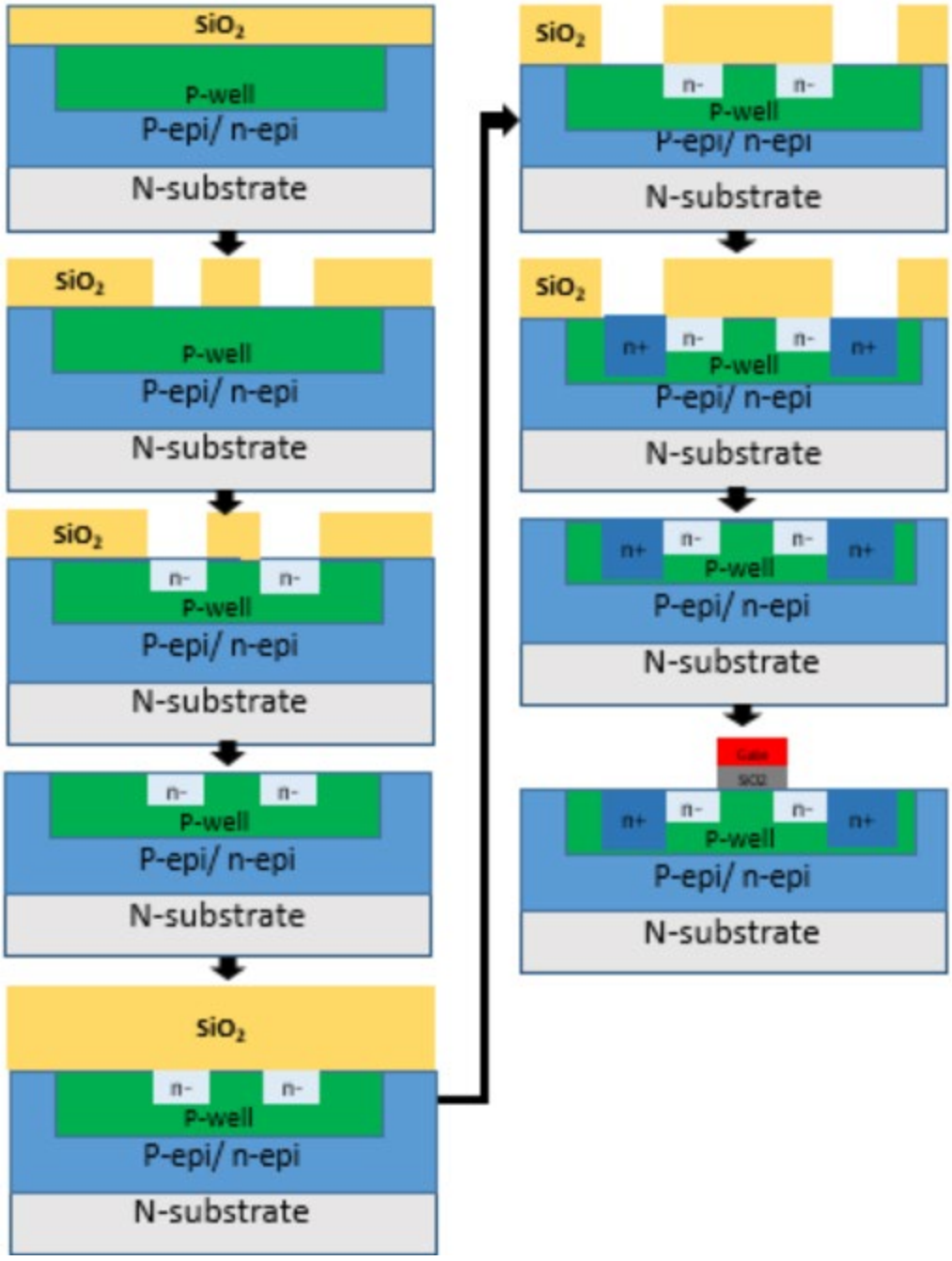


Figure 5.5 Proposed non-self-alignment technique to realize LDD in SiC

Chapter 6. Conclusions

6.1 Summary

Although wide research is available on silicon devices in the submicron region, little has been known about the behavior of silicon carbide in the submicron region. The main purpose of this thesis is to acknowledge the current state of the SiC CMOS process, understand the behavior of SiC devices in the submicron region, and see if silicon topology can be applied to its research progress or not. The minimum channel length that has been reached in this thesis is 0.6 μm. Devices less than 0.6 μm could not be produced due to the convergence issue in the simulation deck. A clear comparison between the LDD NMOSFET and conventional NMOSFET has been established in the SiC platform. The behavior of electric fields in the conventional device and LDD device is discussed. Implementing an LDD region in the channel helped to reduce the electric field to a great extent (almost half) which in turn increases device reliability. LDD devices are capable of handling more voltages (20 – 25V) compared to conventional designs (10V) before reaching the critical electric field of 4H-SiC. The short channel effects such as threshold roll-off are improved compared to a conventional device. Hot electron density and impact ionization process in both conventional and LDD devices are discussed. Hot electron effects are less in LDD devices compared to conventional design MOSFETs. The subthreshold characteristics and gate leakage behavior have shown a clear improvement for the LDD device compared to the conventional MOSFETs. Body hole current is also less for LDD designs compared to conventional designs. At the end of this thesis, a realization of LDD in SiC has been discussed.

6.2 Future Work

In terms of research direction, the optimization of the LDD such as its doping concentration, junction depth, and length may give superior device performance. This thesis is mainly focused on reducing the lateral scaling of a device, but complete scaling which consists of both lateral and vertical dimension reduction can give a more enhanced benefit of device scaling. The device degradation behavior of conventional and LDD devices can be another aspect to look at. Moreover, the device behavior shown in this thesis is at room temperature, but as SiC is famous to operate at higher temperatures so the behavior of LDD at higher temperatures is worth trying. LDD in PMOS may not be necessary for SiC. This is because, in silicon, the hole mobility is 480 cm^2/Vs compared to the electron mobility of 1350 cm^2/Vs. Whereas, for 4H-SiC, the hole mobility is 120 cm^2/Vs compared to the electron mobility of 950 cm^2/Vs [58]. This means that the hole mobility is 2.8 times lower than electron mobility for silicon, but almost 8 times lower for 4H-SiC. Perhaps self-alignment gate technology in SiC is the most important technological barrier at this moment that researchers should focus on to further advance SiC research.

6.3 Major Roadblocks

The hot electron effect is a cumulative effect which means during the times of fabrication it cannot be seen. When the device will be in use day after day, the hot electron effects will be accumulated, so it becomes a reliability issue for the device. Another important aspect associated with this issue is scaling. As the devices are going smaller and smaller, hot electron degradations are becoming larger and larger. To cater to this issue, low doped drain or LDD design can help to reduce the e-field of the device, and eventually, the hot electron effects are minimized. LDD design works well with silicon devices where self-align gate technology is used. That means the gate is grown before the source and drain which means the gate is automatically aligned with the

source and drain. This self-alignment ensures that the gate overhangs the source and drain so that the channel always exists. Again, this self-alignment process reduces the capacitance by ensuring there is no extra overlapping between the gate-to-source and gate-to-drain terminal. Reduction of capacitance means a faster device. This is very significant in the submicron region because overlap capacitance can play a critical part where the channel length or the device size is very small. In SiC, the source and drain are grown first and then the gate is grown. Although some researchers have tried to implement self-alignment in SiC, it is still not widely used. Thus in SiC, clearly the major roadblock is the absence of a self-alignment technique. Although without a self-alignment technique, LDD can be implemented, it requires very high alignment precision and higher instrument capability. Another major roadblock is the use of high annealing temperatures after ion implantation. When a temperature of 1500 °C or more is in use to diffuse dopants, polysilicon or oxide cannot sustain that temperature. This in turn signifies the difficulty of growing gate region first. Hence, it can be said that the use of higher annealing temperatures is a barrier to SiC research progress. This thesis shows the virtual fabrication of LDD, but the real fabrication of LDD can be complex and challenging.

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Appendix A: Description of Research for Popular Publication

No publications resulted from this work.

Appendix B: Executive Summary of Newly Created Intellectual Property

No intellectual property resulted from this work

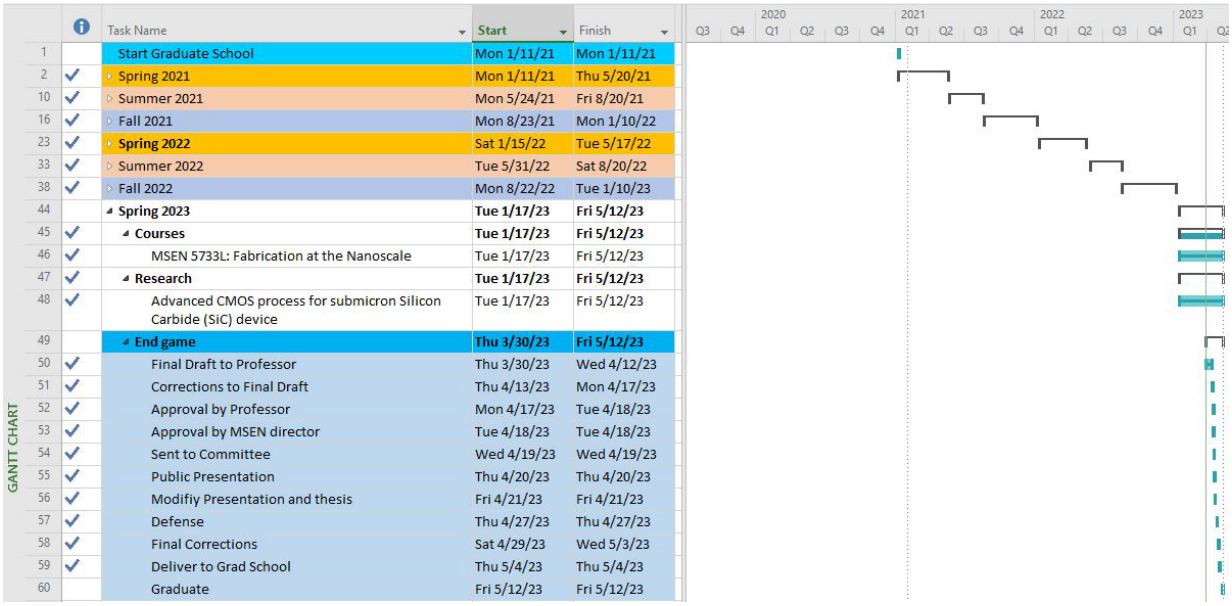
Appendix C: Potential Patent and Commercialization Aspects of Listed Intellectual Property Item

No intellectual property resulted from this work

Appendix D: Broader Impact of Research

Silicon carbide ICs have a huge impact on the market starting from space aviation, electrical vehicles (EVs), nuclear sectors, turbine engines, and so on. Many countries have started to phase out combustion engines and adopt EVs for a cleaner and more sustainable future. SiC ICs will play a huge role in that perspective. Many famous car companies such as GM, Nissan, and Volkswagen have already declared to go all-electric in the future. GM already declared to electrify all vehicles by 2035, whereas Nissan will do it by 2030. BMW and Volkswagen expect their EV sales will be around 50% by 2030. Recently, Land Rover and Jaguar have started to implement SiC in their vehicles. SiC ICs have reduced the inverter battery size to almost 50% and system power efficiency increased up to 99%. Companies such as Microchip planned to invest $880 million, STMicroelectronics planned to invest $4 billion, and Wolfspeed planned $1 billion to expand their research capabilities in SiC. In low voltage areas such as in CMOS, SiC can play a critical role provided its full capability is unleashed by the researchers. SiC IC can work in harsh environments such as in space exploration, solar systems, rocket ships, etc due to its beautiful material properties. In such harsh environments and high temperatures, silicon IC cannot withstand. In power electronics, SiC is already implanted in photovoltaic (PV) arrays and power grids with the capability of reducing 50% energy loss. The market size of SiC was valued at $2.96 billion in 2021 and is expected to increase at a compound annual growth rate (CAGR) of 23% from 2022 to 2030 [68].

Appendix E: Microsoft Project for MS MATE Degree Plan



GANTT CHART

		Task Name	Start	Finish
1		Start Graduate School	Mon 1/11/21	Mon 1/11/21
2	✓	Spring 2021	Mon 1/11/21	Thu 5/20/21
10	✓	Summer 2021	Mon 5/24/21	Fri 8/20/21
16	✓	Fall 2021	Mon 8/23/21	Mon 1/10/22
23	✓	**Spring 2022**	Sat 1/15/22	Tue 5/17/22
33	✓	Summer 2022	Tue 5/31/22	Sat 8/20/22
38	✓	Fall 2022	Mon 8/22/22	Tue 1/10/23
44		**Spring 2023**	**Tue 1/17/23**	**Fri 5/12/23**
45	✓	**Courses**	**Tue 1/17/23**	**Fri 5/12/23**
46	✓	MSEN 5733L: Fabrication at the Nanoscale	Tue 1/17/23	Fri 5/12/23
47	✓	**Research**	**Tue 1/17/23**	**Fri 5/12/23**
48	✓	Advanced CMOS process for submicron Silicon Carbide (SiC) device	Tue 1/17/23	Fri 5/12/23
49		**End game**	**Thu 3/30/23**	**Fri 5/12/23**
50	✓	Final Draft to Professor	Thu 3/30/23	Wed 4/12/23
51	✓	Corrections to Final Draft	Thu 4/13/23	Mon 4/17/23
52	✓	Approval by Professor	Mon 4/17/23	Tue 4/18/23
53	✓	Approval by MSEN director	Tue 4/18/23	Tue 4/18/23
54	✓	Sent to Committee	Wed 4/19/23	Wed 4/19/23
55	✓	Public Presentation	Thu 4/20/23	Thu 4/20/23
56	✓	Modifiy Presentation and thesis	Fri 4/21/23	Fri 4/21/23
57	✓	Defense	Thu 4/27/23	Thu 4/27/23
58	✓	Final Corrections	Sat 4/29/23	Wed 5/3/23
59	✓	Deliver to Grad School	Thu 5/4/23	Thu 5/4/23
60		Graduate	Fri 5/12/23	Fri 5/12/23

Appendix F: Identification of All Software Used in Research and Thesis Generation

Computer #1:

Model Number: Dell Latitude 5320
Service Tag: BW9LCS3
Location: Personal laptop
Owner: Niloy Saha

Software #1:

Name: Microsoft Office 365
Purchased by: University of Arkansas Site License

Software #2:

Name: Microsoft project professional 2016
Purchased by: University of Arkansas Site License

Software #3:

Name: Zotero
Purchased by: Free download available from Zotero.org

Software #4:

Name: Grammarly
Purchased by: Free of charge

Computer #2:

Model No: Dell Core i7
Service Tag: eleg-c210Ma18w1.uark.edu
Location: CSRC 210.18
Owner: Dr. H. Alan Mantooth

Software #1:

Name: VMware Workstation 16 pro
Purchased by: Dr. H. Alan Mantooth

Software #2:

Name: Scientific Linux 6.5
Purchased by: Electrical Engineering Department, University of Arkansas

Software #3:

Name: Sentaurus Workbench vO-2018.06
Purchased by: Dr. H. Alan Mantooth

Software #4:

Name: Sentaurus Workbench vQ-2019.12
Purchased by: Dr. H. Alan Mantooth

Software #5:

Name: SRIM
Purchased by: Free of charge

Appendix G: All Publications Published, Submitted, and Planned

Planned

2023

[1] Hui Wang, Kevin Chen, **Niloy Saha**, Anthony Di Mauro, Tanner Rice, Pengyu Lai, Zhong Chen, H. Alan Mantooth, "Highly Linear Temperature Sensor Based on Silicon Carbide Schottky Barrier Diode for **Harsh** Environments".

[2] SiC CMOS review paper (author's list not yet decided)

Conference Presentations

2022

[1] **Niloy Saha**, Pengyu Lai, Kevin Chen, Tanner Rice, Hui Wang, Anthony De Mauro, Dr. Zhong Chen, Dr. H. Alan Mantooth, "Study of Spacer Technology for Sub-micron SiC Low Voltage MOSFET", Annual MSEN/MEPH IAB and Academy meetings, Fayetteville, AR (2022).

Appendix H: Simulation Deck

Conventional NMOSFET

Part 1**: Structure creation with SProcess**

```
pdbSet Compute Max.Anneal.T 1800<C>
math coord.ucs
# interface refinement
# refinebox interface.materials= { SiliconCarbide }
pdbSet Grid Adaptive 1
# Using Advanced Calibration models
# Multi-threading to speed up the simulation
math numThreads= 4
# Calibrated set-up for Implantation of Dopants in 4H-SiC to increase the accuracy
AdvancedCalibration 4H-SiC
# Line definition
line x location= 0.0      spacing= 0.01<um>  tag= Top
line x location= 0.2      spacing= 0.02<um>
line x location= 0.5      spacing= 0.1<um>
line x location= 2.0      spacing= 0.2<um>  tag= Bottom_epi
line x location= 5.0     spacing= 0.5<um>  tag= Bottom
line y location= 0.0      spacing= 0.1<um>  tag= Left
line y location= 6.0      spacing= 0.1<um>
line y location= 20.0     spacing= 0.1<um>  tag= Right
mgoals accuracy= 1.0e-5 resolution= 0.2
# Mask definition
mask name= PW left= 0 right= 20
mask name= NW left= 7 right= 17
mask name= PP left= 0.5 right= 5.5
mask name= NP segments= "7.5 @NPa@ @NPb@ 19.5"
mask name= GOX left= 11.5 right= 15.5 negative
mask name= POLY left= 12.5 right= 14.5 negative
mask name= FOX segments= "0 1.5 4.5 8.5 18.5 20" negative
mask name= CT segments= "1.5 4.5 8.5 10.5 16.5 18.5" negative
# SiC substrate init -- P-type 1e18
region SiliconCarbide xlo= Bottom_epi xhi= Bottom ylo= Left yhi= Right substrate
init concentration= 1.0e+18<cm-3> field= Nitrogen
# Deposit N-epi
deposit SiliconCarbide anisotropic thickness= 2 species= Nitrogen concentration= 1.0e+15<cm-
3>
# Saving structure
struct tdr= n@node@_1_epi
refinebox SiliconCarbide min= {0.0 0.0} max= {1 20} xrefine= "0.01 0.02 0.02" yrefine= "0.1
0.1 0.1"
# P-well implantation
```

```
photo mask= PW thickness= 5.0
implant Aluminum dose=4.9e12<cm-2> energy=300<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=5000 info=1 cascades
implant Aluminum dose=1.e11<cm-2> energy=36<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=5000 info=1 cascades
# Remove PhotoResist
strip photo
# Diffuse to active dopants
diffuse temperature= 1600<C> time= 5.0<s>
# Saving structure
struct tdr= n@node@_2_PW
# N-Well implantation
#photo mask= NW thickness= 5.0
#implant Nitrogen energy=810 dose=2.0e13 tilt=7 rot=0 sentaurus.mc particles=1000 info=2
#implant Nitrogen energy=380 dose=2.0e11 tilt=7 rot=0 sentaurus.mc particles=1000 info=2
#implant Nitrogen energy=270 dose=1.5e11 tilt=7 rot=0 sentaurus.mc particles=1000 info=2
#implant Nitrogen energy=180 dose=1.0e11 tilt=7 rot=0 sentaurus.mc particles=1000 info=2
#implant Nitrogen energy=80 dose=1.0e11 tilt=7 rot=0 sentaurus.mc particles=1000 info=2
#implant Nitrogen energy=20 dose=1.0e11 tilt=7 rot=0 sentaurus.mc particles=1000 info=2
# Remove PhotoResist
#strip photo
# Diffuse to active dopants
#diffuse temperature= 1600<C> time= 5.0<s>
# Saving structure
#struct tdr= n@node@_3_NW
# P+ implantation
photo mask= PP thickness= 5.0
implant Aluminum dose=7.8e14<cm-2> energy=36<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
implant Aluminum dose=2.0e13<cm-2> energy=18<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
implant Aluminum dose=2.0e14<cm-2> energy=9<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
# Remove PhotoResist
strip photo
# Diffuse to active dopants
diffuse temperature= 1600<C> time= 5.0<s>
# Saving structure
struct tdr= n@node@_4_PP
# N+ implantation
photo mask= NP thickness= 5.0
implant Phosphorus dose=5.8e14<cm-2> energy=36<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
implant Phosphorus dose=2.8e14<cm-2> energy=30<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
```

```
implant Phosphorus dose=2.0e13<cm-2> energy=18<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
implant Phosphorus dose=2.0e14<cm-2> energy=9<keV> tilt=0<degree> rotation=0<degree>
sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
# Diffuse to active dopants
diffuse temperature= 1600<C> time= 5.0<s>
# Remove PhotoResist
strip photo
```

Part 2: **Meshing for NMOS**

```
init tdr= n@node|NMOS_process10@_9_CT
pdbSet InfoDefault 1
## Clear all the lines and refineboxes defined earlier for the process simulation
## ------------------------------------------------------------------------
refinebox clear
refinebox clear.interface.mats
refinebox !keep.lines
line clear

## Device Simulation Mesh Settings
pdbSet Grid SnMesh DelaunayType boxmethod
pdbSet Grid AdaptiveField Refine.Abs.Error     1e37
pdbSet Grid AdaptiveField Refine.Rel.Error     1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0

# Contact Definition (electrode definition)
contact name= "body" point x=-0.1 y=3 Aluminum replace
contact name= "source" point x=-0.1 y=10 Aluminum replace
contact name= "drain" point x=-0.1 y=17 Aluminum replace
contact name= "gate" point x= -0.2 y= 13.5 PolySilicon replace
## contact name= "substrate" bottom
## Refine mesh for simulation
refinebox clear
refinebox clear.interface.mats
refinebox !keep.lines
line clear
refinebox SiliconCarbide min= {0 0} max= {5 20} refine.max.edge= "0.1 0.1 0.1"
refine.min.edge= "0.05 0.05 0.05" def.max.asinhdiff= 0.5 adaptive add
refinebox SiliconCarbide min= {0 0} max= {0.3 20} xrefine= {0.02 0.02 0.02} yrefine= {0.02
0.02 0.02} min.normal.size= 0.001 normal.growth.ratio= 1.5 add
refine.max.edge= {0.02 0.02} refine.fields= {NetActive} def.max.asinhdiff= 0.5 adaptive
SiliconCarbide;
grid remesh
# Saving structure
struct tdr= n@node@_final
```

Part 3: **NMOS transfer curve I_d -V_d with Avalanche Breakdown**

```
# Input/Output files
File {
        Grid= "n@node|NMOSmesh10@_final_fps.tdr"
        Plot= "@tdrdat@"
        Current= "@plot@"
        Output= "@log@"
        *Parameter= "@parameter@"
}
# Electrical contact definitions
Electrode {
        { Name="drain"     Voltage= 0.0 }
        { Name="source"    Voltage= 0.0 }
        { Name="gate"      Voltage= 0.1 }
        { Name="body"              Voltage= 0.0 }
}
## Physics models
Physics {
        Temperature = 300
        AreaFactor  = 10
        Recombination (
         SRH(DopingDependence)
         Auger
eAvalanche(CarrierTempDrive) hAvalanche(Okuto)
)
        Mobility (
         DopingDependence
         #HighFieldSaturation
         #Enormal(Lombardi InterfaceCharge)
         IncompleteIonization
        )
        IncompleteIonization (
         *Split (
                 *Doping = "NitrogenActiveConcentration"
                 *Weights = (0.5 0.5)
         *)
        )
        EffectiveIntrinsicDensity ( Slotboom NoFermi )
        #eBarrierTunneling "NLM" (BarrierLowering)
}
Physics(MaterialInterface="Oxide/SiliconCarbide") {Traps(Conc=2.e12 FixedCharge)}

Plot {
        NonLocal
```

```
        eDensity hDensity
        eCurrent hCurrent
        TotalCurrent
        ElectricField
        eQuasiFermi hQuasiFermi
        egradQuasiFermi hgradQuasiFermi
        Potential Doping SpaceCharge
        SRH Auger
        AvalancheGeneration
        eAvalanche hAvalanche
        eMobility hMobility
        DonorConcentration AcceptorConcentration
        Doping
        eVelocity hVelocity
        #BarrierTunneling
        ConductionBandEnergy ValenceBandEnergy BandGap
        eQuasiFermi hQuasiFermi
}

Math {

        Digits= 7
        Extrapolate
        Method = Blocked
        SubMethod = Pardiso
        ErrEff(electron)= 1e4
        ErrEff(hole)= 1e4
        RHSmin= 1e-5
        RHSmax= 1e15
        RHSFactor= 1e10
        Notdamped= 50
        Iterations= 20
        ExitOnFailure
        eMobilityAveraging= ElementEdge
        hMobilityAveraging= ElementEdge

        ExtendedPrecision(128)
        ## BM_ExtendedPrecision
        #TensorGridAniso(aniso)
        ComputeGradQuasiFermiAtContacts= UseQuasiFermi

        ## NumberofThreads= 4
        NumberofThreads= maximum
        -CheckUndefinedModels
}
```

```
Solve {
        *- Initial Solution
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson }
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson Electron }
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson Electron Hole }

        # Curve Vg=5, Vg sweep
        Quasistationary(
        InitialStep= 1e-6 MinStep= 1e-8 MaxStep=0.2
        Increment= 2.0 Decrement= 2.0
        Goal { Name="gate" Voltage= @Vg7@ }
        ){ Coupled { Poisson Electron Hole }  }
        Save (FilePrefix="Vg5")
        # Curve Vg=5, Vd sweep
        Load(FilePrefix="Vg5")
        NewCurrentPrefix="IdVd_Vg5_"
        Quasistationary(
        InitialStep= 1e-6 MinStep= 1e-8 MaxStep= 0.2
        Increment= 2.5 Decrement= 2.0
        Goal { Name="drain" Voltage= @Vdvary7@ }
        ){ Coupled { Poisson Electron Hole }
        }
}
```

Part 4: NMOS transfer curve I_d –V_g with hot electron injection and gate leakage

```
# Input/Ouput files
File {
        Grid= "n@node|NMOSmesh10@_final_fps.tdr"
        Plot= "@tdrdat@"
        Current= "@plot@"
        Output= "@log@"
        *Parameter= "@parameter@"
}

# Electrical contact definitions
Electrode {
        { Name="drain"     Voltage= 0.0 }
        { Name="source"    Voltage= 0.0 }
        { Name="gate"      Voltage= 0.0 }
#{ Name="gate"      Voltage= -1.0 }
        { Name="body"              Voltage= 0.0 }
}

## Physics models
Physics {
```

```
        Temperature = 300
        AreaFactor  = 1
        Recombination (
         SRH(DopingDependence)
         Auger )
        Mobility (
         DopingDependence
         #HighFieldSaturation
         #Enormal(Lombardi InterfaceCharge)
         IncompleteIonization
        )
        IncompleteIonization (
         *Split (
                 *Doping = "NitrogenActiveConcentration"
                 *Weights = (0.5 0.5)
         *)
        )
        EffectiveIntrinsicDensity ( Slotboom NoFermi )
        #eBarrierTunneling "NLM" (BarrierLowering)
        }
##Physics(MaterialInterface="Oxide/SiliconCarbide") {Traps(Conc=2.e12 FixedCharge)}
Physics(MaterialInterface="Oxide/SiliconCarbide")
{
Traps(Conc=2.e12 FixedCharge)
GateCurrent(GateName="gate" Lucky Fiegna)
}

Plot {
        NonLocal
        eDensity hDensity
        eCurrent hCurrent
        TotalCurrent
        ElectricField
        eQuasiFermi hQuasiFermi
        egradQuasiFermi hgradQuasiFermi
        Potential Doping SpaceCharge
        SRH Auger
        AvalancheGeneration
        eAvalanche hAvalanche
        eMobility hMobility
        DonorConcentration AcceptorConcentration
        Doping
        eVelocity hVelocity
        #BarrierTunneling
        ConductionBandEnergy ValenceBandEnergy BandGap
        eQuasiFermi hQuasiFermi
```

```
        HotElectronInj
}

Math {
        Digits= 7
        Extrapolate
        Method = Blocked
        SubMethod = Pardiso
        ErrEff(electron)= 1E-2
        ErrEff(hole)= 1E-2
        RHSmin= 1E-15
        RHSmax= 1e15
        RHSFactor= 1e10
        Notdamped= 50
        Iterations= 20
        ExitOnFailure
        eMobilityAveraging= ElementEdge
        hMobilityAveraging= ElementEdge
         ExtendedPrecision(128)
        ## BM_ExtendedPrecision
        #TensorGridAniso(aniso)
        ComputeGradQuasiFermiAtContacts= UseQuasiFermi
        ## NumberofThreads= 4
        NumberofThreads= maximum
-CheckUndefinedModels
}
Solve {
        *- Initial Solution
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson }
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson Electron }
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson Electron Hole }

        *- Vd sweep
        Quasistationary(
        InitialStep= 1e-6 MinStep= 1e-8 MaxStep=0.2
        Increment= 2.0 Decrement= 2.0
        Goal { Name="drain" Voltage= @Vdlow3@ }
        ){ Coupled { Poisson Electron Hole }  }
        NewCurrentFile="IdVg_"
        *- Vg sweep
        Quasistationary(
        InitialStep= 1e-6 MinStep= 1e-8 MaxStep= 0.2
        Increment= 2.5 Decrement= 2.0
        Goal { Name="gate" Voltage= @Vgvary3@ }
        ){ Coupled { Poisson Electron Hole }
        }}
```

LDD NMOSFET

Part 1: **Structure creation with SProcess**

```
pdbSet Compute Max.Anneal.T 1800<C>
math coord.ucs

pdbSet Grid Adaptive 1

# Using Advanced Calibration models
# Multi-threading to speed up the simulation
math numThreads= 4
# Calibrated set-up for Implantation of Dopants in 4H-SiC to increase the accuracy
AdvancedCalibration 4H-SiC

# Line definition
line x location= 0.0      spacing= 0.01<um>  tag= Top
line x location= 0.2      spacing= 0.02<um>
line x location= 0.5      spacing= 0.1<um>
line x location= 2.0      spacing= 0.2<um>  tag= Bottom_epi
line x location= 5.0     spacing= 0.5<um>  tag= Bottom

line y location= 0.0      spacing= 0.1<um>  tag= Left
line y location= 6.0      spacing= 0.1<um>
line y location= 20.0     spacing= 0.1<um>  tag= Right
mgoals accuracy= 1.0e-5 resolution= 0.2
# Mask definition
mask name= PW left= 0 right= 20
mask name= NW left= 7 right= 17
mask name= PP left= 0.5 right= 5.5
mask name= NM segments= "12.7 13.2 13.8 14.3"
mask name= NP segments= "7.5 12.7 14.4 19.5"
mask name= GOX left= 12.7 right= 14.3 negative
mask name= POLY left= 13.2 right= 13.8 negative
mask name= FOX segments= "0 1.5 4.5 8.5 18.5 20" negative
mask name= CT segments= "1.5 4.5 8.5 10.5 16.5 18.5" negative

# SiC substrate init -- P-type 1e18
region SiliconCarbide xlo= Bottom_epi xhi= Bottom ylo= Left yhi= Right substrate
init concentration= 1.0e+18<cm-3> field= Nitrogen

# Deposit N-epi
deposit SiliconCarbide anisotropic thickness= 2 species= Nitrogen concentration= 1.0e+15<cm-
        3>
# Saving structure
struct tdr= n@node@_1100_epi
```

```
refinebox SiliconCarbide min= {0.0 0.0} max= {1 20} xrefine= "0.01 0.02 0.02" yrefine= "0.1
        0.1 0.1"
# P-well implantation
photo mask= PW thickness= 5.0
implant Aluminum dose=4.9e12<cm-2> energy=300<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=5000 info=1 cascades
implant Aluminum dose=1.e11<cm-2> energy=36<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=5000 info=1 cascades
# Remove PhotoResist
strip photo
# Diffuse to active dopants
diffuse temperature= 1600<C> time= 5.0<s>
# Saving structure
struct tdr= n@node@_1101_PW
# P+ implantation
photo mask= PP thickness= 5.0
implant Aluminum dose=7.8e14<cm-2> energy=36<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
implant Aluminum dose=2.0e13<cm-2> energy=18<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
implant Aluminum dose=2.0e14<cm-2> energy=9<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
# Remove PhotoResist
strip photo
# Diffuse to active dopants
diffuse temperature= 1600<C> time= 5.0<s>
# Saving structure
struct tdr= n@node@_1102_PP

# N- implantation
photo mask= NM thickness= 5.0
implant Phosphorus dose=1e13<cm-2> energy=25<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
#Diffuse to active dopants
diffuse temperature= 1600<C> time= 5.0<s>
# Remove PhotoResist
strip photo
# High Temperature Annealing
diffuse time= 20<min> temperature= 1750<C> init= 1.0<min>
# Saving structure
struct tdr= n@node@_1103_NM
init tdr= n@node|NMOSprocess_modify30@_1103_NM
# N+ implantation
photo mask= NP thickness= 5.0
implant Phosphorus dose=7.8e14<cm-2> energy=32<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
```

```
implant Phosphorus dose=2.0e13<cm-2> energy=18<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades
implant Phosphorus dose=2.0e14<cm-2> energy=10<keV> tilt=0<degree> rotation=0<degree>
        sentaurus.mc particles=1000 info=1 temperature= 500<C> cascades

strip photo
# Diffuse to active dopants
diffuse temperature= 1600<C> time= 3.0<s>

# Remove PhotoResist
strip photo

# High Temperature Annealing
diffuse time= 30<min> temperature= 1750<C> init= 1.0<min>

# Saving structure
struct tdr= n@node@_1104_NP

init tdr= n@node|NMOS_Process2mymodif31@_1104_NP

# Gate oxidation
deposit Oxide thickness= 0.02 isotropic mask= GOX region.name= "gateoxide"

# Diffuse to active dopants
diffuse temperature= 1600<C> time= 5.0<s>
# Remove PhotoResist
strip photo
# Saving structure
struct tdr= n@node@_1105_GOX
# Gate oxidation
deposit Oxide thickness= 0.3 isotropic mask= FOX region.name= "Fieldoxide"
# Diffuse to active dopants
diffuse temperature= 1600<C> time= 5.0<s>
# Remove PhotoResist
strip photo
# Saving structure
struct tdr= n@node@_1106_FOX
# Poly deposition
deposit PolySilicon anisotropic mask= POLY thickness= 0.5
# Remove PhotoResist
strip photo
# Saving structure
struct tdr= n@node@_1107_GPO
# Metalization
deposit Aluminum isotropic mask= CT thickness= 0.2
# Diffuse to active dopants
```

```
#diffuse temperature= 1600<C> time= 5.0<s>
# Remove PhotoResist
strip photo
# Saving structure
struct tdr= n@node@_1108_CT
```

Part 2: **Meshing for LDD NMOS**

```
init tdr= n@node|NMOS_Process3mymodif32@_1108_CT

pdbSet InfoDefault 1
## Clear all the lines and refineboxes defined earlier for the process simulation
## ------------------------------------------------------------------------------
refinebox clear
refinebox clear.interface.mats
refinebox !keep.lines
line clear

## Device Simulation Mesh Settings
pdbSet Grid SnMesh DelaunayType boxmethod
pdbSet Grid AdaptiveField Refine.Abs.Error     1e37
pdbSet Grid AdaptiveField Refine.Rel.Error     1e10
pdbSet Grid AdaptiveField Refine.Target.Length 100.0

# Contact Definition (electrode definition)
contact name= "body" point x=-0.1 y=3 Aluminum replace
contact name= "source" point x=-0.1 y=10 Aluminum replace
contact name= "drain" point x=-0.1 y=17 Aluminum replace
contact name= "gate" point x= -0.2 y= 13.5 PolySilicon replace
## contact name= "substrate" bottom

## Refine mesh for simulation
refinebox clear
refinebox clear.interface.mats
refinebox !keep.lines
line clear
refinebox SiliconCarbide min= {0 0} max= {5 20} refine.max.edge= "0.1 0.1 0.1"
        refine.min.edge= "0.05 0.05 0.05" def.max.asinhdiff= 0.5 adaptive add
refinebox SiliconCarbide min= {0 0} max= {0.3 20} xrefine= {0.02 0.02 0.02} yrefine= {0.02
        0.02 0.02} min.normal.size= 0.001 normal.growth.ratio= 1.5 add
grid remesh

# Saving structure
struct tdr= n@node@_final
```

Part 3: **LDD NMOS transfer curve I_d –V_g**

```
# Input/Output files
File {
        Grid= "n@node|NMOSmesh33@_final_fps.tdr"
        Plot= "@tdrdat@"
        Current= "@plot@"
        Output= "@log@"
        *Parameter= "@parameter@"
}

# Electrical contact definitions
Electrode {
        { Name="drain"     Voltage= 0.0 }
        { Name="source"   Voltage= 0.0 }
        { Name="gate"      Voltage= 0.0 }
        { Name="body"     Voltage= 0.0 }
}

## Physics models
Physics {
        Temperature = 300
        AreaFactor  = 1
        Recombination (
         SRH(DopingDependence)
         Auger )
        Mobility (
         DopingDependence
         #HighFieldSaturation
         #Enormal(Lombardi InterfaceCharge)
         IncompleteIonization
        )
        IncompleteIonization (
         *Split (
                 *Doping = "NitrogenActiveConcentration"
                 *Weights = (0.5 0.5)
         *)
        )
        EffectiveIntrinsicDensity ( Slotboom NoFermi )
        #eBarrierTunneling "NLM" (BarrierLowering)
}
Physics(MaterialInterface="Oxide/SiliconCarbide")
{
Traps(Conc=2.e12 FixedCharge)
GateCurrent(GateName="gate" Lucky Fiegna)
}
```

```
Plot {
        NonLocal
        eDensity hDensity
        eCurrent hCurrent
        TotalCurrent
        ElectricField
        eQuasiFermi hQuasiFermi
        egradQuasiFermi hgradQuasiFermi
        Potential Doping SpaceCharge
        SRH Auger
        AvalancheGeneration
        eAvalanche hAvalanche
        eMobility hMobility
        DonorConcentration AcceptorConcentration
        Doping
        eVelocity hVelocity
        #BarrierTunneling
        ConductionBandEnergy ValenceBandEnergy BandGap
        eQuasiFermi hQuasiFermi
        HotElectronInj
}
Math {
        Digits= 7
        Extrapolate
        Method = Blocked
        SubMethod = Pardiso
        ErrEff(electron)= 1E-2
        ErrEff(hole)= 1E-2
        RHSmin= 1E-15
        RHSmax= 1e15
        RHSFactor= 1e10
        Notdamped= 50
        Iterations= 20
        ExitOnFailure
        eMobilityAveraging= ElementEdge
        hMobilityAveraging= ElementEdge

        ExtendedPrecision(128)
        ## BM_ExtendedPrecision
        #TensorGridAniso(aniso)
        ComputeGradQuasiFermiAtContacts= UseQuasiFermi
         ## NumberofThreads= 4
        NumberofThreads= maximum
-CheckUndefinedModels
}
```

```
Solve {
        *- Initial Solution
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson }
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson Electron }
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson Electron Hole }

        *- Vd sweep
        Quasistationary(
        InitialStep= 1e-6 MinStep= 1e-8 MaxStep=0.2
        Increment= 2.0 Decrement= 2.0
        Goal { Name="drain" Voltage= @Vd33@ }
        ){ Coupled { Poisson Electron Hole }  }
        NewCurrentFile="IdVg_"
        *- Vg sweep
        Quasistationary(
        InitialStep= 1e-6 MinStep= 1e-8 MaxStep= 0.2
        Increment= 2.5 Decrement= 2.0
        Goal { Name="gate" Voltage= @Vgvary33@ }
        ){ Coupled { Poisson Electron Hole}
        }
        }
```

Part 3: **LDD NMOS transfer curve I_d –V_d**

```
# Input/Output files
File {
        Grid= "n@node|NMOSmesh33@_final_fps.tdr"
        Plot= "@tdrdat@"
        Current= "@plot@"
        Output= "@log@"
        *Parameter= "@parameter@"
}
# Electrical contact definitions
Electrode {
        { Name="drain"     Voltage= 0.0 }
        { Name="source"    Voltage= 0.0 }
        { Name="gate"      Voltage= 0.1 }
        { Name="body"              Voltage= 0.0 }
}
## Physics models
Physics {
        Temperature = 300
        AreaFactor  = 1
        Recombination (
         SRH(DopingDependence)
         Auger )
```

```
        Mobility (
         DopingDependence
         #HighFieldSaturation
         #Enormal(Lombardi InterfaceCharge)
         IncompleteIonization
        )
        IncompleteIonization ( )
        EffectiveIntrinsicDensity ( Slotboom NoFermi )}
##Physics(MaterialInterface="Oxide/SiliconCarbide") {Traps(Conc=2.e12 FixedCharge)}
Physics(MaterialInterface="Oxide/SiliconCarbide")
{
Traps(Conc=2.e12 FixedCharge)
GateCurrent(GateName="gate" Lucky Fiegna)
}
Plot {
        NonLocal
        eDensity hDensity
        eCurrent hCurrent
        TotalCurrent
        ElectricField
        eQuasiFermi hQuasiFermi
        egradQuasiFermi hgradQuasiFermi
        Potential Doping SpaceCharge
        SRH Auger
        AvalancheGeneration
        eAvalanche hAvalanche
        eMobility hMobility
        DonorConcentration AcceptorConcentration
        Doping
        eVelocity hVelocity
        #BarrierTunneling
        ConductionBandEnergy ValenceBandEnergy BandGap
        eQuasiFermi hQuasiFermi
        HotElectronInj}
Math {
        Digits= 7
        Extrapolate
        Method = Blocked
        SubMethod = Pardiso
        ErrEff(electron)= 1e4
        ErrEff(hole)= 1e4
        RHSmin= 1e-5
        RHSmax= 1e15
        RHSFactor= 1e10
        Notdamped= 50
        Iterations= 20
```

```
        ExitOnFailure
        eMobilityAveraging= ElementEdge
        hMobilityAveraging= ElementEdge

        ExtendedPrecision(128)
        ## BM_ExtendedPrecision
        #TensorGridAniso(aniso)
        ComputeGradQuasiFermiAtContacts= UseQuasiFermi

        ## NumberofThreads= 4
        NumberofThreads= maximum
        -CheckUndefinedModels
}
Solve {
        *- Initial Solution
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson }
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson Electron }
        Coupled(Iterations=1000 LineSearchDamping=1e-2){ Poisson Electron Hole }

         # Curve Vg=5, Vg sweep
        Quasistationary(
        InitialStep= 1e-6 MinStep= 1e-8 MaxStep=0.2
        Increment= 2.0 Decrement= 2.0
        Goal { Name="gate" Voltage= @Vg34@ }
        ){ Coupled { Poisson Electron Hole }  }
        Save (FilePrefix="Vg")
        # Curve Vg=5, Vd sweep
        Load(FilePrefix="Vg")
        NewCurrentPrefix="IdVd_Vg_"
        Quasistationary(
        InitialStep= 1e-6 MinStep= 1e-8 MaxStep= 0.2
        Increment= 2.5 Decrement= 2.0
        Goal { Name="drain" Voltage= @Vdvary34@ }
        ){ Coupled { Poisson Electron Hole }
        }
}
```