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Analysis of an Isolated Bidirectional Ćuk Converter

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Analysis of an Isolated Bidirectional Ćuk Converter

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ABSTRACT

The objective of this thesis is to perform an analysis of the isolated bidirectional Ćuk dc-dc converter topology and demonstrate the advantages and operation of this configuration through simulations using MATLAB/Simulink^{TM} and measurements collected from a 1.5-kW prototype tested at the Engineering Research Center (ENRC) laboratory of the University of Arkansas.

The idea of integrating an active-clamp snubber circuit on each side of the converter, proposed by Dr. Sudip Mazumder from the University of Illinois, Chicago, limits the additional voltage stresses on the components due to the energy from the transformer's leakage inductance. This is studied in this thesis to achieve zero voltage switching (ZVS) turn-ON functionality of all active devices, reducing the losses and size of passive components. In addition, this work evaluates three separate control parameters that are utilized for power transfer, ZVS region, and the circulating current of the converter. These three variables are the duty cycle of S_{P1}, namely d_1; the duty cycle of S_{S1}, namely d_2; and the phase-shift ratio, by the symbol $\Delta_\emptyset$.

The theoretical analysis is validated through simulations using MATLAB/Simulink^{TM} and through a 1.5-kW prototype converter. In addition to the analysis of the results, conclusions and suggestions for future work are presented to enhance the system's quality.

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CHAPTER 1

INTRODUCTION

1.1   Motivations for this Research Work

The sustainability of life on Earth is critically dependent on the environment. The current world faces difficulties to improve energy efficiency and reduce greenhouse effects, caused by the carbon dioxide emitted from typical internal combustion engines used in most vehicles, methane emitted from a variety of anthropogenic and natural resources such as agricultural activities, coal mining, and certain industrial processes, etc. [1]. Renewable energy is considered to be the most effective option for managing these environmental challenges because it can supply energy free of air pollution and greenhouse gas emissions by generating pretty much zero of these gases [2].

The spread of most renewable energy sources is partially dependent on the advancement of power electronic systems, which offer reliability, efficiency, and reduced cost. In the last few decades, typical bidirectional dc-dc converters such as the buck, boost, and dual active bridge (DAB) have become the focus of research in power electronics. A bidirectional dc-dc converter steps down or steps up dc voltage from one side to the other while being driven by a gate-signal generator and related controller. It is a key component in numerous modern applications, including those for servers, energy storage, automobiles, and renewable energy systems. For instance, Fig. 1.1 illustrates an example of a general topology of energy conversion from solar energy, which is a renewable energy source, consisting of series-connected 60-kW boost converter (DC/DC) and inverter (DC/AC) that will deliver the desired output voltage or current, which it will be in this case to the power grid. Several renewable energy sources provide electrical energy in the dc form, which is then transmitted in ac form for usage in domestic,
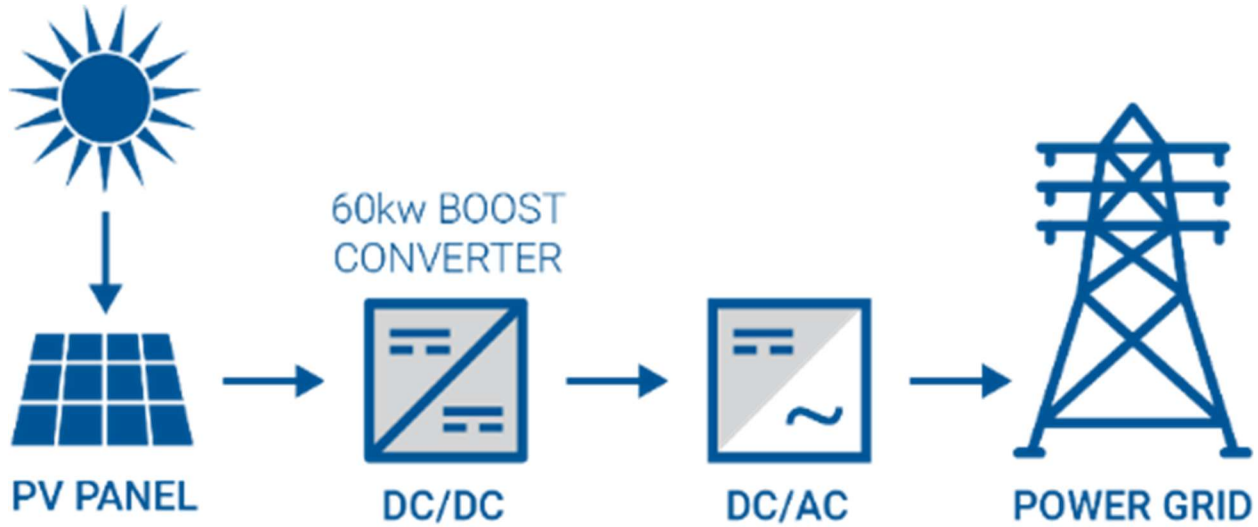
Fig. 1.1: Solar DC/DC and DC/AC power conversion [3].

commercial, and industrial applications. However, many applications and gadgets need dc power to function, so power conversion is once again more necessary.

With reference to Fig. 1.1, the dc-dc converter is an important subsystem in a renewable energy system. Converters must be developed in a compact manner, so the power electronic converter topology is very significant. The dc-dc converter topologies are designed to compensate for the mismatch in power supply availability and variations in current and voltage levels that the load demands. The dc-dc converter is used to alter the input dc voltage from one level to another.

The bidirectional dc-dc converter block in MATLAB/Simulink$^{\text{TM}}$ allows to model different topologies of converters, such as non-isolated converters with two switching devices, isolated converters with six switching devices, or DAB converters with eight switching devices [4]. In the next paragraphs, these topologies are explained and their configurations are presented. In particular, this thesis' work focuses on the analysis of the isolated bidirectional Ćuk dc-dc converter which will be expanded upon in more detail in the next chapter.

A non-isolated bidirectional dc-dc converter lacks an electrical isolation barrier provided by a transformer. This type of converter is the typical non-isolated half-bridge topology, as illustrated in Fig. 1.2 consisting of an inductor, two capacitors, and two switches that are of the same device type. This converter consists of a combination of a step-up and step-down converter connected in anti-parallel where the operation of the circuit can be explained by two modes. Switch S_1 operates with the proper duty cycle during the forward step-down process, while switch S_2 is always OFF while its anti-parallel diode is conducting. As an alternative, S_1 is always OFF and S_2 is in operation throughout the backward step-up process. If the switch in the OFF state is a MOSFET, synchronous rectification (SR) used to increase efficiency is possible [5].

An isolated bidirectional dc-dc converter does have an electrical isolation barrier provided by a transformer separating the input and output voltages. This converter has four additional switches, which makes a total of six switching devices that form a full bridge located on the input side of the converter and the other two switches are on the output side of the converter. Some passive components such as capacitors and inductors are also included in the system to eliminate switching noise and regulate the output voltage. The isolated bidirectional dc-dc converter's schematic circuit, which places the full bridge on the converter's input side, is displayed in Fig. 1.3.
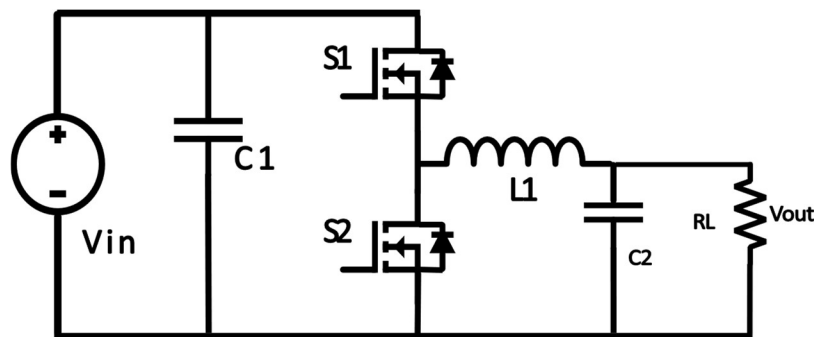
Fig. 1.2: Non-isolated bidirectional dc-dc converter (half-bridge).
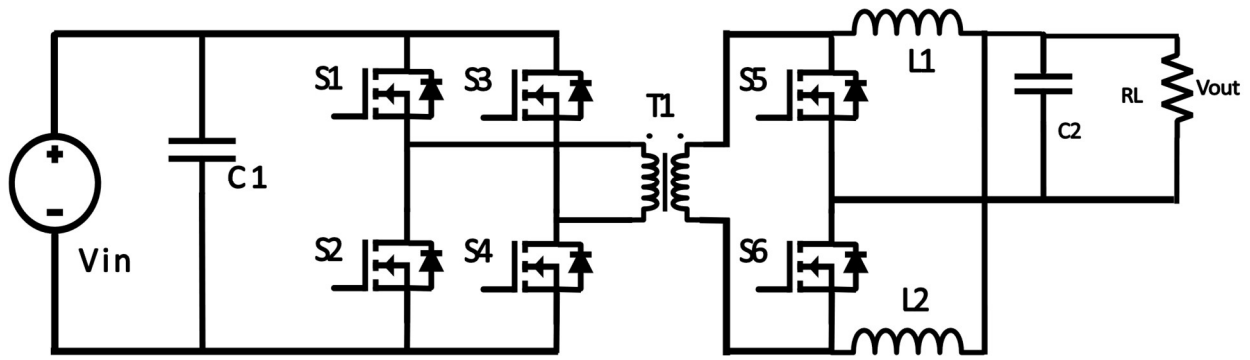
Fig. 1.3: Isolated bidirectional dc-dc converter (full bridge on the input side).

The DAB is a bidirectional, controllable, dc-dc converter suitable for medium and high-power applications comprised of eight semiconductor devices or two full bridges, a high-frequency transformer (HFT), and some passive components such as transfer inductors and dc-link capacitors as shown in Fig. 1.4. It is also known as a full bridge with a controllable rectifier due to its configuration. The isolated bidirectional DAB-based dc-dc converter has a number of benefits over conventional ones, including electrical isolation, excellent reliability, and bidirectional power transmission [6]. Nevertheless, because the DAB employs so many switches and additional filtering components, a number of innovative converter topologies have been invented to identify the best electrical connections for power processing elements, such as switches, storage components, and transformers in order to achieve the highest efficiency and best performance.
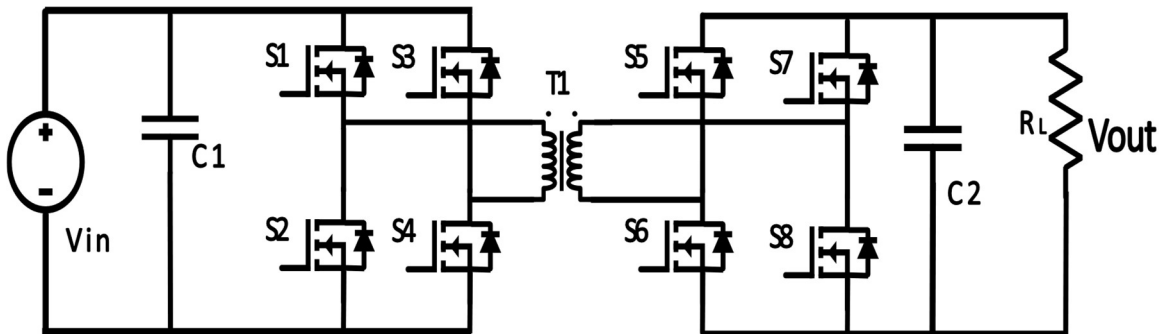
Fig. 1.4: Dual active bridge dc-dc converter (two full bridges).

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In contrast to the DAB, the isolated bidirectional Ćuk dc-dc converter can be implemented with just two active switches. Some passive components such as $L_1, C_{a1}, C_{b1},$ and L_2 are also added to this topology. As illustrated in Fig. 1.5, this converter combines the functions of buck and boost converters so that the input side behaves like a boost and the output side like a buck in a disconnected inverting fashion.

Due to its wide operating range and special characteristic of continuous current flow at both terminals, the isolated bidirectional Ćuk dc-dc converter is a great solution for integrating renewable energy sources as a voltage regulator in hybrid solar-wind technology, where the input voltage depends on the sun irradiance and wind velocity. The Ćuk converter modifies the output voltage in response to inputs that vary with the strength of the sun and wind. In addition, the Ćuk converter can be utilized in battery management systems of electric vehicles. Overall, the Ćuk converter is used when an output voltage that is smaller or larger than the input voltage is required—mostly at high output voltage levels with negative polarity and low-standby currents.

Furthermore, the output voltage polarity can be freely chosen due to the transformer's isolation of the converter denoted by T1. Even with a 1:1 ac transformer, this output voltage can be greater or less than the input voltage. However, the turns ratio of the transformer can be adjusted to reduce device stress on the input side.
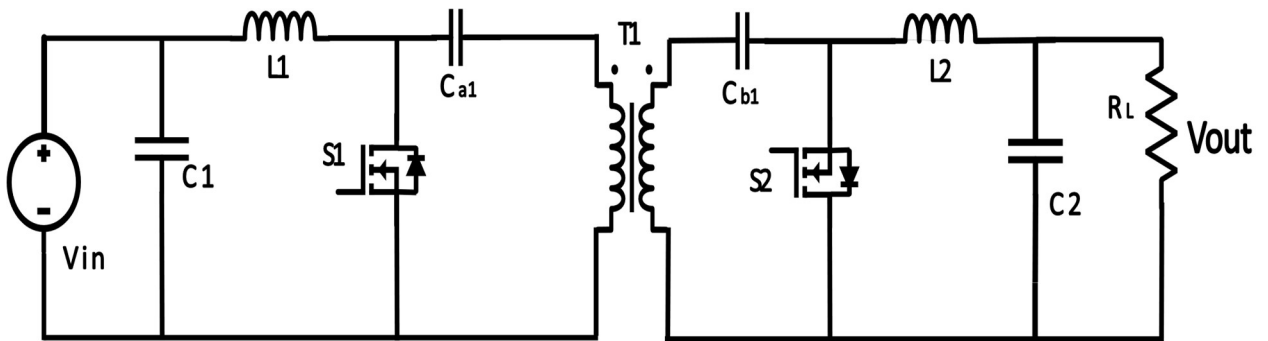
Fig. 1.5: Conventional isolated bidirectional Ćuk dc-dc converter.

Table 1.1: Characteristics of the Different Type of Converters

Converter Topology	Non-isolated (Half-Bridge)	Isolated (Full-bridge)	DAB	Isolated Ćuk
No. of Switches	2	6	8	2
No. of Diodes	2	6	8	2
No. of Capacitors	2	2	2	4
No. of Inductors	1	2	0	2
Isolation	No	Yes	Yes	Yes

Table 1.1 summarizes the characteristics of the various dc-dc converter topologies that were previously presented. In a typical (non-isolated) dc-dc converter, current can flow directly from input to output, decreasing cost, size, and complexity. However, galvanic isolation or simply known as isolation is frequently needed in applications to electrically separate the input and output sides of the device. In this case, a transformer is utilized to transfer current and voltage across the gap between the input and output sides of an isolated dc-dc converter. Other advantages of isolation include separating noise-sensitive circuit components from the sources of that noise, meeting safety standards, etc. [7]. Due to the number of components and its several advantages, the Ćuk converter is selected as the topology to be studied in this thesis.

1.2 Objectives and Organization of Thesis

From an analysis of Table 1.1, the main objective of this thesis is to perform an analysis of the isolated bidirectional Ćuk converter topology and demonstrate experimentally the advantages of this configuration in a 1.5-kW rated power scaled-down prototype. Equipment available at the National Center for Reliable Electric Power Transmission (NCREPT) and the Engineering Research Center (ENRC) laboratory at the University of Arkansas will be used to test this prototype.

The structure of this thesis is as follows: Chapter 2 addresses the theoretical aspects of

the isolated bidirectional Ćuk converter topology providing the necessary insights to understand its functioning. Chapter 3 provides the design equations that determine the system parameters and simulations based on MATLAB/Simulink^{TM} to enable the development of control algorithms. The experimental results of the scaled-down prototype and comparison analysis of the calculation, simulation, and experimental results are given in Chapter 4. Finally, conclusions and recommendations for future work are identified in Chapter 5.

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CHAPTER 2

ISOLATED BIDIRECTIONAL ĆUK DC-DC CONVERTERS

2.1   Introduction

This chapter overviews the basic topologies of the conventional non-isolated and isolated bidirectional Ćuk converters and their principles of operation. In particular, the functionality and modes of operation of the isolated bidirectional Ćuk converter with an active-clamp topology are explained. Chapter 2 also addresses the theoretical analysis of the converter, which is the first stage of any design.

The structure of this chapter is organized as follows: Section 2.2 addresses an overview of the conventional non-isolated bidirectional Ćuk converter. Section 2.3 presents the topology of the conventional isolated bidirectional Ćuk converter as well as the isolated bidirectional Ćuk converter with an active-clamp to accomplish soft-switching turn-ON. Section 2.4 discusses the functionality and modes of operation of this converter. Section 2.5 analyzes the system through three characteristics that are relevant to the control parameters; namely the power transfer, circulating current, and ZVS operation. Section 2.6 provides a summary of the accomplishments of this entire chapter and describes the goals for the following chapter.

2.2   Ćuk Converter Overview

In 1977, Prof. Slobodan Ćuk developed the switching dc-dc converter called the Ćuk switched-mode dc-dc voltage converter [1], [2]. This configuration, illustrated in Fig. 2.1, makes use of the fewest possible inductive and capacitive storage and switching components in order to completely imitate the ideal dc-dc converter with theoretically pure input and output dc currents. Two inductors, two capacitors, one diode, and one switching transistor comprise the non-isolated Ćuk converter. Replacing the diode with another transistor makes the converter bidirectional,

while also adding a transformer and replacing the series capacitor with two series capacitors makes the converter an isolated bidirectional Ćuk converter, as previously presented in Fig. 1.5.

The original non-isolated Ćuk converter was designed to overcome the main disadvantages of the buck-boost converter illustrated in Fig. 2.2, such as significant ripple in the output current and Electromagnetic Interference (EMI) issues caused by the discontinuous input current and the charging current of the output capacitor. The Ćuk converter is also capable of both stepping up and stepping down the output voltage and, therefore, the current. Hence, the output voltage can be either higher or lower than the input voltage depending on the application and operating conditions controlled by the duty ratio of the switching transistor. The Ćuk converter has other advantages, such as having reduced voltage ripple on the input and output sides due to the usage of two inductors, and having higher efficiency, reduced EMI, smaller size and weight, etc. [3].
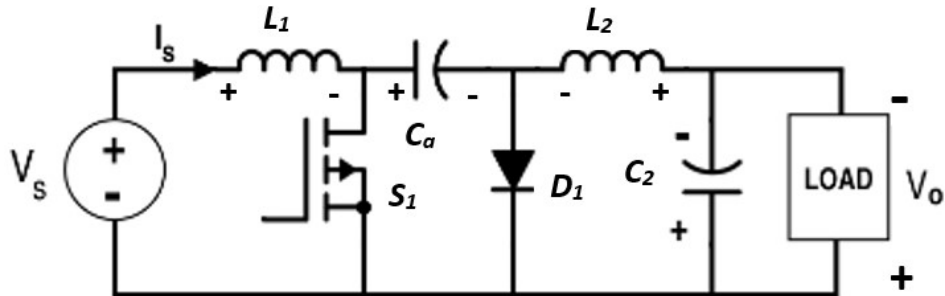
Fig. 2.1: Non-isolated Ćuk converter.
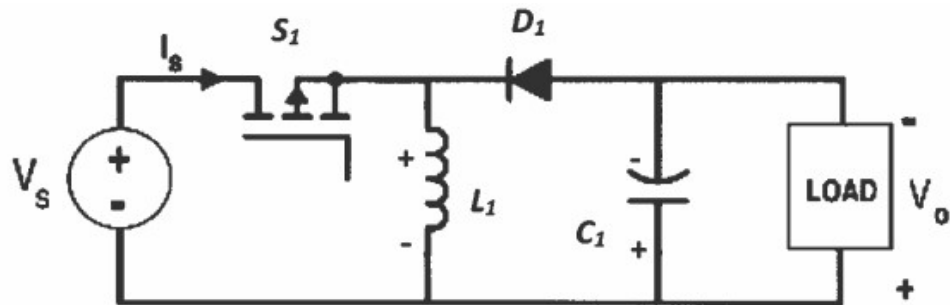
Fig. 2.2: Buck-boost converter.

Similar to the basic buck-boost converter, the Ćuk converter also results in a negative output voltage, meaning the output voltage with respect to the same input ground has a negative value. The energy flows from the input to the output through the coupling capacitor C_a, which is another variation in how this converter works. Comparatively to other dc-dc converters, the Ćuk converter demands a more complex controller in terms of control design.

Due to complexity and the lack of a rational strategy for achieving the appropriate magnetics design that provides "zero-ripple" terminal currents, only a small percentage of users are able to quickly adapt the Ćuk converter and its variants to their applications [4].

Before a detailed analysis of the isolated topology, which has more components added to the conventional non-isolated bidirectional Ćuk converter, it is significantly important to understand first the basic topology and its operation. The variations of the topology of the original Ćuk converter are covered in detail through this chapter. During the analysis of Fig. 2.1, the blocking capacitor C_a must be large enough so that its voltage can be assumed constant under steady-state conditions. The presence of the inductors L_1 and L_2 in series with the input and output ports (source and load), respectively, ensures the currents in both input and output are non-pulsating currents, which implies the input current should be smooth and the output capacitor C_2 is small. Assuming that the components or L_1, C_a, C_2, and L_2 do not hold any charge, there are two cases under steady-state conditions of the equivalent circuit of a Ćuk converter that can be analyzed:

a) **Switch-ON interval:** When the switch S_1 is turned ON, the diode D_1 is reverse-biased by the voltage across the capacitor C_a. The inductor L_1 rises flowing through the switch and back to the source. At the same time, the stored energy in the capacitor C_a from the previous cycle is fed to the load and increases the energy stored in L_2. The key point is

that this current also flows through the switch. Fig. 2.3 displays how the circuit behaves when the switch S_1 is closed.

b) **Switch-OFF interval:** During this OFF interval, the current through the inductor L_2 and L_1 flows through the diode (that is forward biased). In the process, current i_{L1} charges capacitor C_a and current i_{L2} charges the output capacitor C_2 and supplies the load. Fig. 2.4 shows the equivalent circuit when the switch is turned OFF.

2.3   Isolated Ćuk Converter Topology

Following three essential procedures, the crucial electrical isolation feature, frequently required in practice, can be introduced easily and optimally [2]. First, the coupling capacitor C_a is separated into two series or blocking capacitors C_a and C_b, each one being a mirror image of the other, as shown in Fig. 2.5(a). Next, there is an unknown dc voltage at the connection point
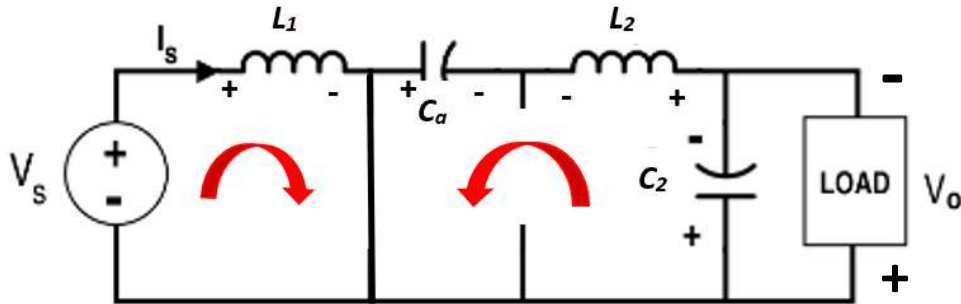
Fig. 2.3: Switch-ON interval.
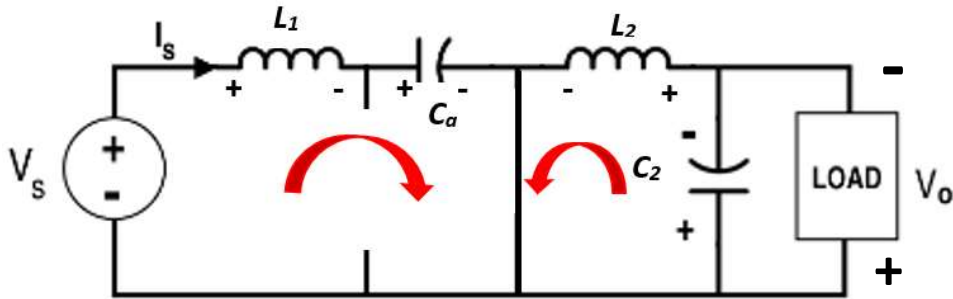
Fig. 2.4: Switch-OFF interval.

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between these two capacitors. By adding an inductor between this point and ground, this

uncertain voltage can then be set to zero, as seen in Fig. 2.5(b). Finally, in order to achieve the

needed electrical isolation between input and output, the additional inductance is simply divided

into two equal transformer windings, and the transformer is denoted by T1 as illustrated in Fig.

2.5(c). The transformer turns ratio is arbitrarily assumed unity.

When compared to other widely-used isolated switching architectures, the electrical

isolation obtained in this manner not only has some exceptional qualities but also entirely

preserves the general characteristics of the basic converter. The two inductors of the basic Ćuk

converter can be integrated into a single magnetic circuit with two windings, primary and

secondary, respectively; this approach is the so-called "integrated magnetics" [2].
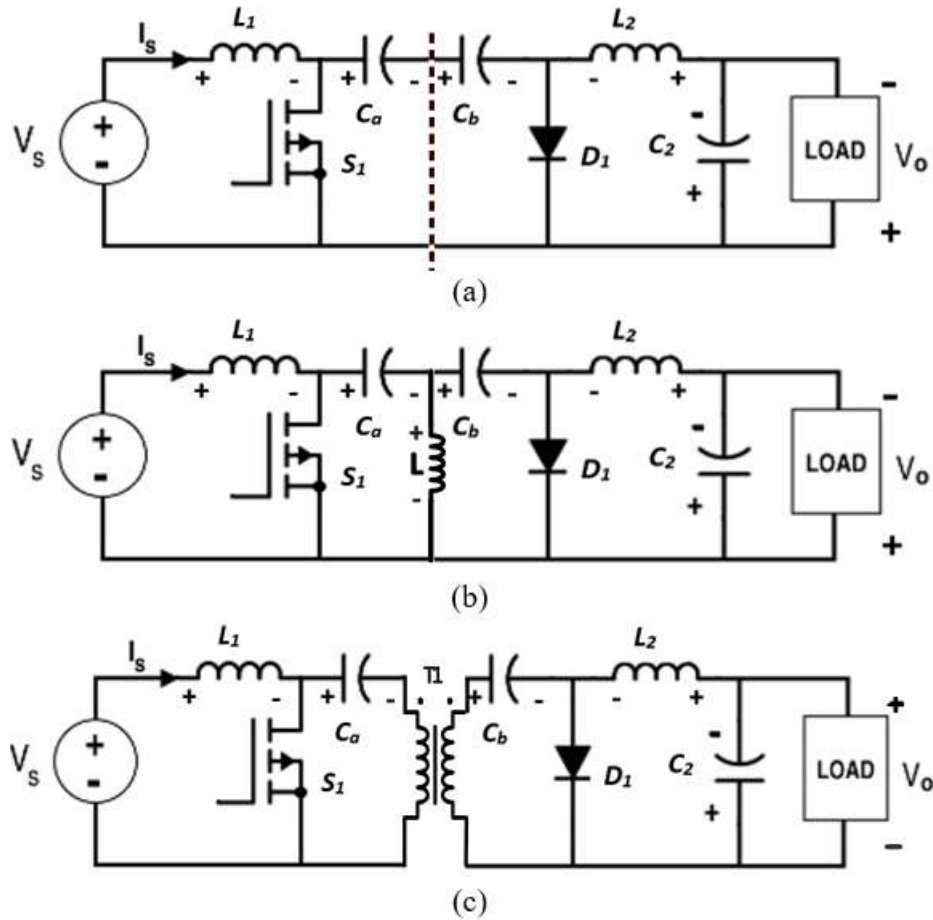
Fig. 2.5: Steps to have dc isolation in the original Ćuk converter.

The inductor coupling adds a concurrent inductive energy transfer to the initial capacitive energy transfer that existed between the input and output ports. Therefore, it may naturally be assumed that using this coupling mechanism results in less ripple currents at both the input and output; this is actually, the case.

Now, the conventional isolated bidirectional Ćuk dc-dc converter circuit shown in Fig. 1.5, which is also presented in this chapter as Fig. 2.6, can be analyzed. The left switch S_1 is controlled by a pulse width modulation (PWM) signal, just like in the original Ćuk converter in the forward mode, whereas the right switch S_2 is OFF, making it function like a standard diode. In contrast, S_2 is controlled by the PWM signal in the reverse mode, while S_1 is turned OFF to function as a diode [5]. The output voltage polarity can be chosen freely since the converter is isolated by the transformer. This output voltage can have a higher or lower magnitude than the input voltage even with a 1:1 transformer, with the turns ratio of this transformer can be determined to lessen device stresses on the input side [2].

Just two active switches are required in an isolated bidirectional Ćuk dc-dc converter; however, these switches are hard-switched resulting in larger losses. This sort of converters typically uses a lossy snubber circuit to reduce the drain-to-source voltage across the devices by dissipating the energy stored in the leakage inductance of a common high-frequency transformer
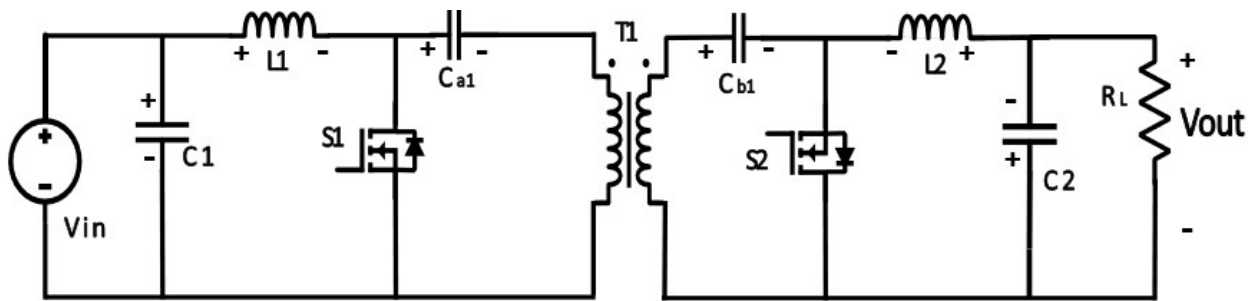
Fig. 2.6: Conventional isolated bidirectional Ćuk dc-dc converter.

(HFT). As a result, the converter suffers additional losses which minimize its application, so a lossless snubber solution should be implemented [6], [7]. To achieve this, however, a number of passive components are required, but it is well known that they increase the system's losses and reduce efficiency.

Dr. Sudip Mazumder and his doctoral student, Shantanu Gupta from the University of Illinois at Chicago, proposed the idea of incorporating an active-clamp snubber circuit in each side of the converter, consisting of a capacitor, a series resonant inductor, and an auxiliary switch to limit the voltage stresses on the components and transfer energy from the leakage inductance of the transformer to the clamp capacitor [6], [7]. Potentially, the efficiency increases could be around 8 % by eliminating turn-on losses. The active-clamp circuit helps the switching devices to operate at higher switching frequencies and enables zero voltage switching (ZVS) turn-ON of the main switches, reducing the losses and sizes of passive components. Fig. 2.7 illustrates the proposed topology for the isolated bidirectional Ćuk dc-dc converter which will be analyzed throughout this work.

2.4   Functionality of the Isolated Ćuk Converter

With reference to Fig. 2.7, the primary-side circuit consists of the input source represented by voltage V_{in}, input capacitor C_1, input inductor L_1, primary series resonant inductor L_{R1}, primary soft-switching or auxiliary capacitor C_{T1}, main primary switch S_{P1},
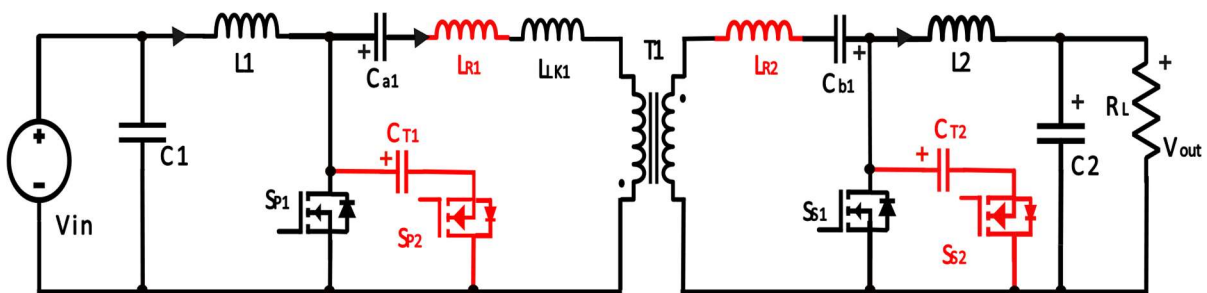
Fig. 2.7: Proposed isolated bidirectional Ćuk converter with an active-clamp.

auxiliary primary switch S_{P2}, primary blocking capacitor C_{a1}, and leakage inductance referred to the primary side, L_{LK1}. The secondary blocking capacitor C_{b1}, secondary series resonant inductor L_{R2}, secondary soft-switching or auxiliary capacitor C_{T2}, main secondary switch S_{S1}, auxiliary secondary switch S_{S2}, output inductor L_2, output capacitor C_2, and resistive load R_L form the secondary-side circuit. The middle part of the system that connects both sides is the isolating transformer T1 and the two active-clamp circuits in this topology are needed for bidirectional operation. The power flow is defined as positive (forward mode) when power is transferred from V_{in} to V_{out}, and S_{S1} operates in synchronous rectification (SR) mode, whereas the power flow is defined as reverse power flow (backward mode) when power is transferred from V_{out} to V_{in}, and S_{P1} operates in SR mode. The switches' conduction losses are decreased under SR operation.

The converter's ZVS functioning is dependent on the transformer's magnetizing inductance, even though the active-clamp circuit serves as a snubber circuit to decrease the impact of the transformer leakage inductance. The lower the leakage inductance, the higher the auxiliary and blocking capacitors are required to avoid resonance between them. Therefore, a high-switching frequency operation is critical for achieving ZVS [6], [7].

The modulation techniques of this converter will be based on three control parameters: the duty cycle of S_{P1}, d_1; duty cycle of S_{S1}, d_2; and the phase-shift ratio $\Delta_\emptyset$. The phase-shift ratio is the ratio between the time periods when both main switches are inactive in the switching interval, that is:

$$\Delta_\emptyset = \frac{t_{SP1,OFF}}{t_{SS1,OFF}}. \tag{2.1}$$

This produces a broad ZVS range and increased efficiency for a wide voltage gain. The duty cycles of the two main switches S_{P1} and S_{S1} work in a complementary mode in the conventional modulation. However, the modulation proposed in [6] and [7] suggests that the

duty cycles of these switches and the phase-shift ratio are independently controlled, allowing other degrees of freedom. A variety of optimization strategies are presented to lower the circulating current for a given output power when maintaining ZVS operation to lower conduction losses. The authors of [6] and [7] proposed that d_1 and d_2 should be optimized to accomplish the minimal circulating current while keeping a constant $\Delta_\emptyset$ [6], [7].

2.4.1　Modes of operation

Using the active-clamp circuits and the equivalent series inductor L_{eq}, which is the sum of the series resonant inductors L_{R1} and L_{R2} as well as the leakage inductances of the transformer L_{LK1} and L_{LK2}, the proposed Ćuk converter provides ZVS turn-ON of all switches. The main MOSFET switch's body diode turns ON before the gate goes high due to the active-clamp circuit's producing a negative drain-to-source current, i_{ds}, through the main switch which enables ZVS turn-ON, whereas the constant voltages from the auxiliary and blocking capacitors over a switching cycle are applied to the equivalent series inductor L_{eq}, causing circulating current and power transfer. The inductor current i_{Leq} must be linear throughout the main modes in order for the converter to operate linearly; this is made possible by eliminating LC resonances.

Only the forward power flow of the converter topology, from the turn-OFF of S_{P1} to the turn-ON of S_{S1}, is considered in this thesis [6], [7].

In switch-mode power conversion circuits, the "volt-seconds balance" refers to the fact that the integral of the voltage waveforms applied to L_1, L_2, and L_{eq} must be zero over one complete switching cycle under steady-state conditions. The following average voltage equations can then be obtained:

$$V_{CT1} = \frac{V_{in}}{d'_1} \tag{2.2}$$

$$V_{CT2} = \frac{V_{out}}{d'_2} \tag{2.3}$$

$$V_{Ca1} + V_{Cb1} = V_{in} + V_{out} \tag{2.4}$$

where V_{CT1} and V_{CT2} are the steady-state average voltages across the capacitors C_{T1} and C_{T2}; V_{in} and V_{out} are steady-state average input and output voltages, respectively; d'_1 and d'_2 are the duty cycles of the primary-side auxiliary switch (S_{P2}) and secondary-side auxiliary switch (S_{S2}). These duty cycles $d'_1 = 1 - d_1$ and $d'_2 = 1 - d_2$ are complementary of the main switches. The V_{Ca1} and V_{Cb} are respectively steady-state average voltages across capacitors C_{a1} and C_{b1} over a switching period.

The duration of the phase-shift between the primary and secondary gate signals is $\Delta_\emptyset T_{sw}$.

Per Fig. 2.8 to Fig. 2.23, the current flowing into the switch S_{P1} branch is defined as $i_1(t)$ and the one flowing through switch S_{S1} branch is defined as $i_2(t)$. These currents can be determined per KCL with reference to Fig. 2.8 as follows:

$$i_1(t) = i_{L1}(t) - i_{Leq}(t) \tag{2.5}$$

$$i_2(t) = i_{L2}(t) + i_{Leq}(t). \tag{2.6}$$

where $i_{L1}(t)$ and $i_{L2}(t)$ are the instantaneous currents through the input and output inductors, respectively, and $i_{Leq}(t)$ is the instantaneous current through the equivalent inductor L_{eq}. Furthermore, $v_1(t)$ and $v_2(t)$ are the voltages across the main switches S_{P1} and S_{S1}.

Eight (8) forward modes describe the operation of the converter: four (4) main operating modes (M$_1$, M$_2$, M$_3$, and M$_4$) and four (4) transition modes (T$_1$, T$_2$, T$_3$, and T$_4$) as depicted in Fig. 2.8 to Fig. 2.23 [6], [7]. Each mode for forward operation of the proposed Ćuk converter is analyzed below [6], [7].

Main operating mode M₁

At time t_0, main switch S_{P1} is OFF (see transition mode T₄) and current $i_1(t)$ is flowing

through the body diode of the auxiliary switch S_{P2} because $i_{P2}(t)$ is negative, and auxiliary

switch S_{S2} is already conducting. Switch S_{P2} is turning ON at ZVS before current $i_1(t)$ becomes

positive. The drain-to-source current of S_{P2}, $i_{P2}(t)$ is equal to $-i_1(t)$. Fig. 2.8 illustrates the

current paths of the main operating mode M₁ through the interval $t_0 < t < t_1$. The voltage

across the inductor L_{eq} is given by $[V_{CT} + V_{CT} - V_{Ca1} - V_{Cb1}]$ since the switches S_{P2} and S_{S2}

are active. The current $i_{Leq}(t)$ increasing linearly is then defined as follows:

$$i_{Leq}(t) = \frac{V_{CT1} + V_{CT2} - V_{Ca1} - V_{Cb1}}{Leq} (t - t_0) + i_{Leq}(t_0). \qquad (2.7)$$

At time t_1, main operating mode M₁ ends by turning OFF auxiliary switch S_{S2}. This

mode's duration, T_{M1}, is calculated as follows [6]:

$$T_{M1} = t_1 - t_0 = \Delta_\emptyset\, T_{sw} - (T_{T1} + T_{T4})/2 \qquad (2.8)$$

where T_{T1} and T_{T4} are the durations of the transition modes T_1 and T_4, respectively. Fig. 2.9

presents the current $i_{Leq}(t)$ during this main operating mode M₁.

Fig. 2.8: Main operating mode 1 [t₀ -t₁]: M₁.

Fig. 2.9: Current through the equivalent inductance L_{eq} during interval t_0 -t_1.

Transition mode T_1

This transition mode shown in Fig. 2.10 lasts during interval $t_1 < t < t_2$. At time t_1, auxiliary switch S_{S2} is turned OFF, so current $i_2(t)$ is transferred from S_{S2} to main switch S_{S1}. As a result, the output capacitance of S_{S1} ($C_{oss,S1}$) discharges and the output capacitance of S_{S2} ($C_{oss,S2}$) charges. In order for ZVS turn-ON of S_{S1}, $C_{oss,S1}$ must be completely discharged prior to applying its gate voltage. The end of this mode is signaled by the clamping of $v_2(t)$ by the body diode of S_{S1} as a result of the current $i_2(t)$. The duration of this transition mode T₁ is given by:

$$T_{T1} = t_2 - t_1 = \frac{(C_{oss,S1} + C_{oss,S2})V_{CT2}}{i_2(t_1)}$$

(2.9)

$$i_2(t_1) = (I_{L2} + \Delta I_{L2}) + i_{Leq}(t_1)$$

(2.10)

where $i_{Leq}(t_1)$ is given by (2.7). Fig. 2.11 displays the current $i_2(t_1)$ during this transition mode T₁.

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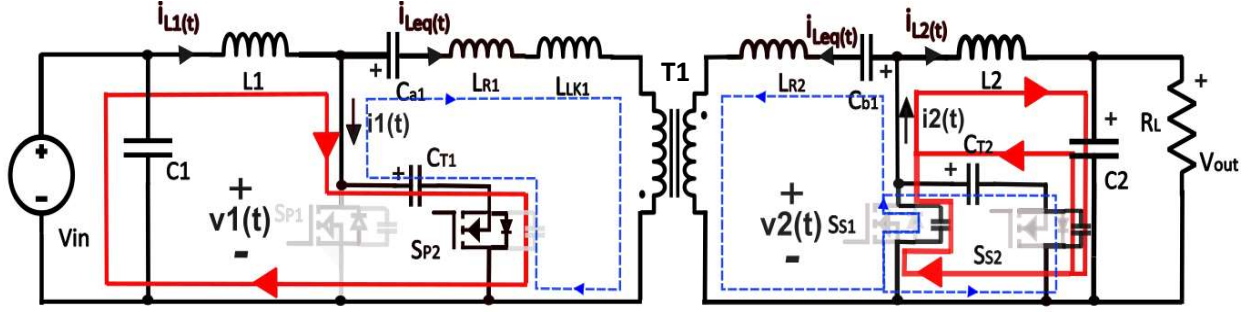
Fig. 2.10: Transition mode 1 [t_1 -t_2]: T_1.

Fig. 2.11: Current $i_2(t)$ flowing out of the node voltage $v_2(t)$ during interval t_1 -t_2.

Main operating mode M₂

At time t_2, main switch S_{S1} is turning ON at ZVS when current flowing through its body diode of S_{S1} becomes positive ($i_{S1}(t) = $ -$i_2(t)$) and auxiliary switch S_{P2} is already conducting. Fig. 2.12 illustrates the current paths of the main operating mode M₂ during interval $t_2 < t < t_3$. The voltage across the inductor L_{eq} is now [$V_{CT1} - V_{Ca1} - V_{Cb1}$], which depending on the value of V_{CT1}, might be positive or negative, as auxiliary switch S_{P2} is also active. The current $i_{Leq}(t)$ is defined by [6]:

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$$i_{Leq}(t) = \frac{V_{CT1} - V_{Ca1} - V_{Cb1}}{Leq} (t - t_2) + i_{Leq}(t_2). \tag{2.11}$$

At time t_3, main operating mode M2 ends by turning OFF auxiliary switch S_{P2}. This mode's duration, T$_{M2}$, is calculated as follows [6]:

$$T_{M2} = t_3 - t_2 = (d'_1 - \Delta_\emptyset) T_{sw} - (T_{T2} + T_{T1})/2 \tag{2.12}$$

where T_{T2} and T_{T1} are the lengths of the transition modes T_2 and T_1, respectively. Fig. 2.13 presents the current $i_{Leq}(t)$ during this main operating mode M2.

Fig. 2.12: Main operating mode 2 [t2 -t3]: M2.

Fig. 2.13: Current through the equivalent inductance L_{eq} during interval t2 -t3.

Transition mode T₂

This transition mode shown in Fig. 2.14 lasts during the interval $t_3 < t < t_4$. At time t_3, auxiliary switch S_{P2} is turned OFF, so current $i_1(t)$ is transferred from S_{P2} to main switch S_{P1}. As a result, the output capacitance of S_{P1} ($C_{oss,P1}$) and the output capacitance of S_{P2} ($C_{oss,P2}$) are discharged and charged, respectively. In order for ZVS turn-ON of S_{P1}, $C_{oss,P1}$ must be completely discharged prior to applying its gate voltage. The end of this mode is signaled by the clamping of $v_1(t)$ by the body diode of S_{P1} as a result of the current $i_1(t)$. The duration of this transition mode T₂, and the current $i_1(t_3)$ are given by:

$$T_{T2} = t_4 - t_3 = \frac{(C_{oss,P1} + C_{oss,P2})V_{CT1}}{i_1(t_3)} \tag{2.13}$$

$$i_1(t_3) = (I_{L1} + \Delta I_{L1}) - i_{Leq}(t_3) \tag{2.14}$$

where $i_{Leq}(t_3)$ is given by (2.11). Fig. 2.15 displays the current $i_1(t_3)$ during this transition mode T₂.
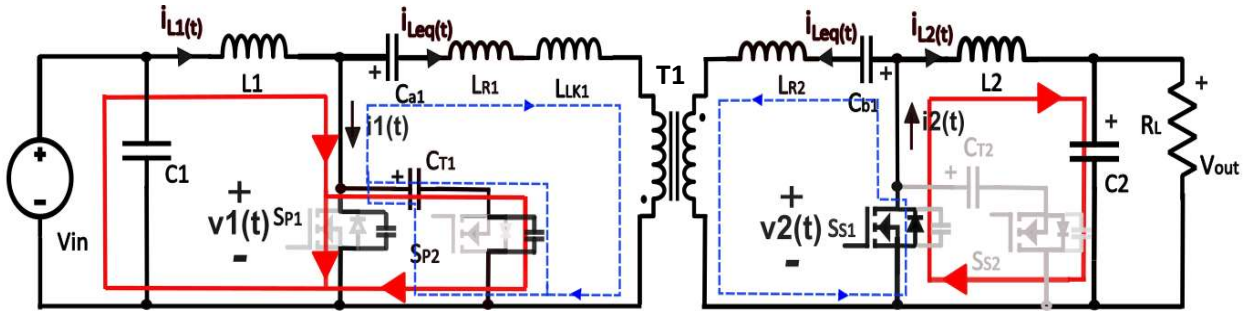
Fig. 2.14: Transition mode 2 [t₃ -t₄]: T₂.
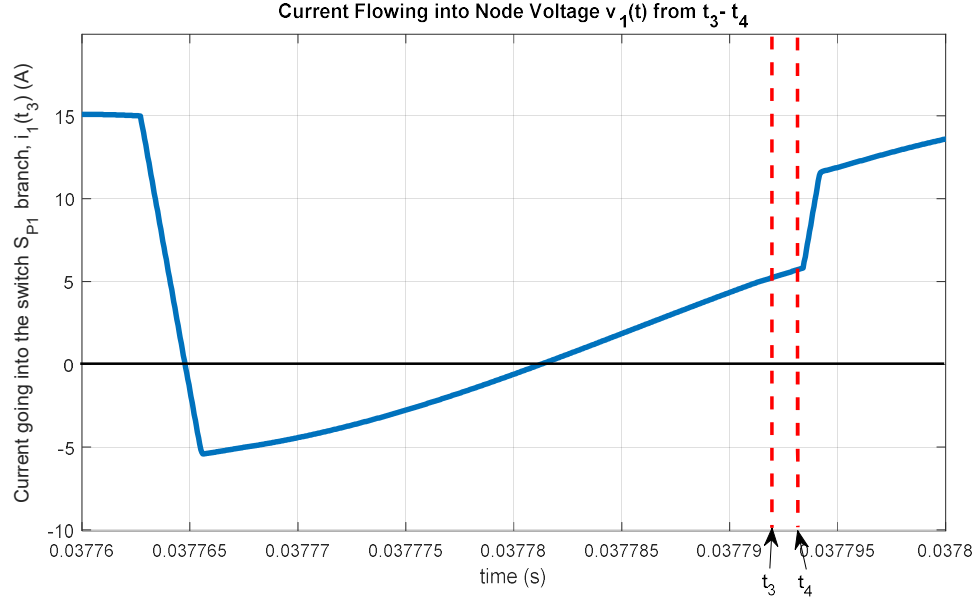
Fig. 2.15: Current $i_1(t)$ flowing into the node voltage $v_1(t)$ during interval t_3 -t_4.

Main operating mode M$_3$

At time t_4, main switch S_{P1} is turning ON at ZVS when current flowing through its body diode of S_{P1} becomes positive ($i_{P1}(t) = i_1(t)$), and main switch S_{S1} is already conducting. Fig. 2.16 illustrates the current paths of this main operating mode M$_3$ during interval $t_4 < t < t_5$. The voltage across the inductor L_{eq} is equal to $[-V_{Ca1} - V_{Cb1}]$, as switches S_{P1} and S_{S1} are ON. The current $i_{Leq}(t)$ decreasing linearly is defined by:

$$i_{Leq}(t) = \frac{-V_{Ca1} - V_{Cb1}}{Leq} (t - t_4) + i_{Leq}(t_4).$$

(2.15)

At time t_5, mode M$_3$ ends by turning OFF S_{S1}. This mode's duration, T$_{M3}$, is obtained as follows [6]:

$$T_{M3} = t_5 - t_4 = (d_1 - d'_2 + \Delta_\emptyset) T_{sw} - (T_{T3} + T_{T2})/2$$

(2.16)

where T_{T3} and T_{T2} are the lengths of the transition modes T_3 and T_2, respectively. Fig. 2.17 presents the current $i_{Leq}(t)$ during this main operating mode M$_3$.
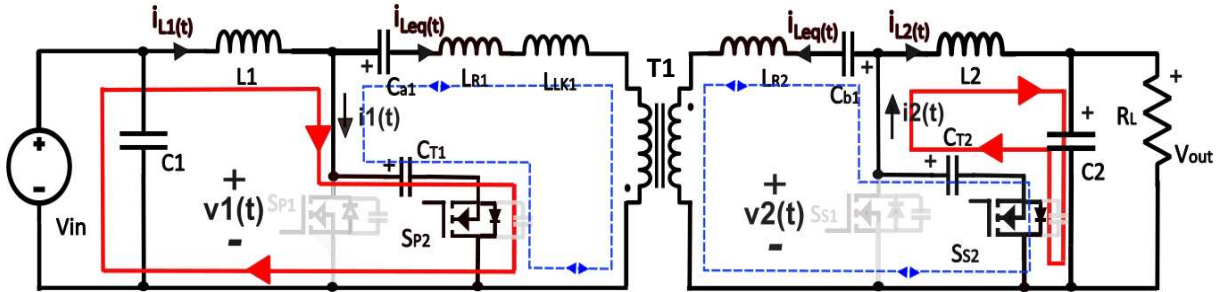
23
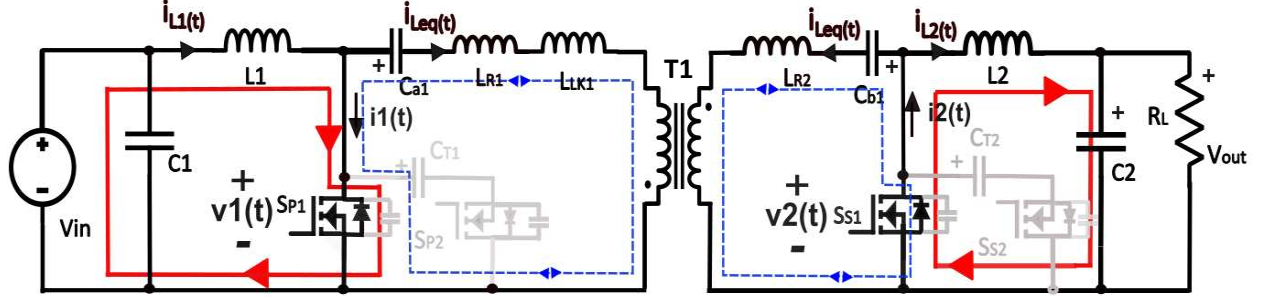
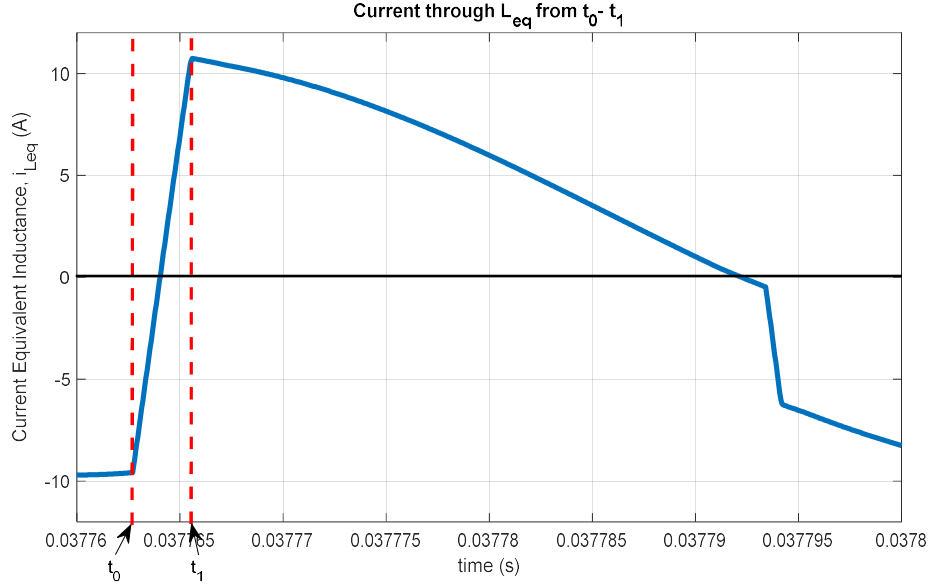Fig. 2.16: Main operating mode 3 [t_4 -t_5]: M_3.
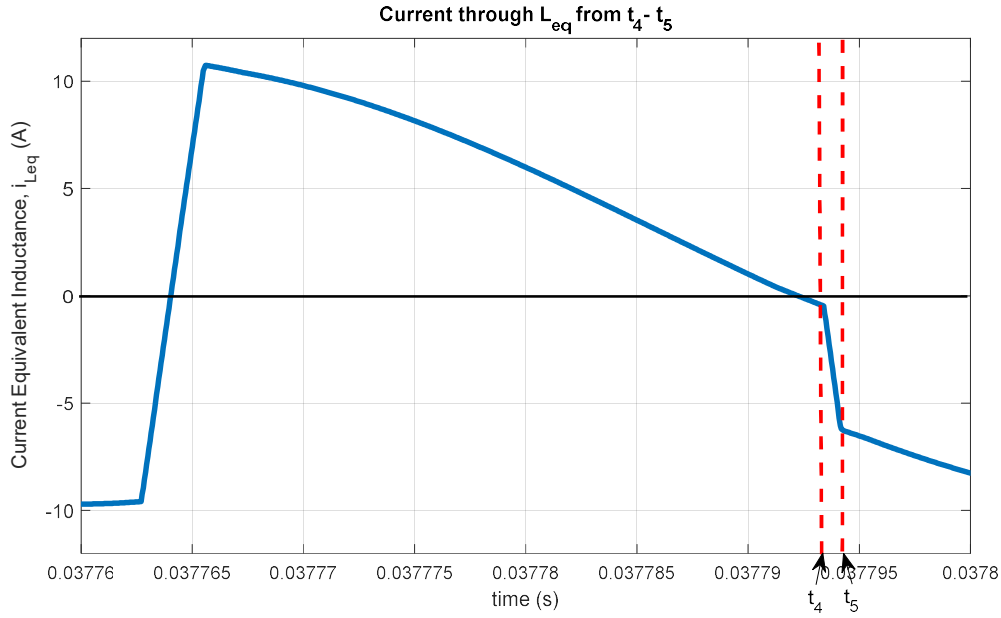
Fig. 2.17: Current through the equivalent inductance L_{eq} during interval t_4 -t_5.

Transition mode T_3

This transition mode shown in Fig. 2.18 lasts during interval $t_5 < t < t_6$. At time t_5, main switch S_{S1} is turned OFF, so current $i_{Leq}(t)$ forces the current $i_2(t)$ to become negative. As a result, the output capacitance of S_{S1} discharges ($C_{oss,S1}$) and the output capacitance of auxiliary switch S_{S2} ($C_{oss,S2}$) charges. In order for ZVS turn-ON of S_{S2}, $C_{oss,S2}$ must be completely discharged prior to applying its gate voltage. The end of this mode is signaled by the clamping of voltage $v_2(t)$ by the body diode of

S_{S2} as a result of the current $i_2(t)$. The duration of this transition mode T$_3$, and the current $i_2(t_5)$ are calculated by (2.17) and (2.18):

$$T_{T3} = t_6 - t_5 = \frac{(C_{oss,S1} + C_{oss,S2})V_{CT2}}{-i_2(t_5)} \tag{2.17}$$

$$i_2(t_5) = (I_{L2} + \Delta I_{L2}) - i_{Leq}(t_5) \tag{2.18}$$

where $i_{Leq}(t_5)$ is given by (2.15). Fig. 2.19 displays the current $i_2(t_5)$ during this transition mode T$_3$.
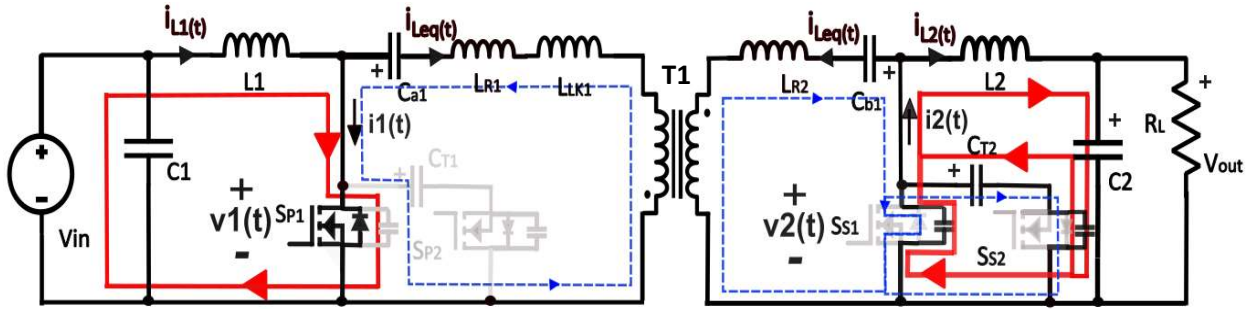
Fig. 2.18: Transition mode 3 [t$_5$ -t$_6$]: T$_3$.
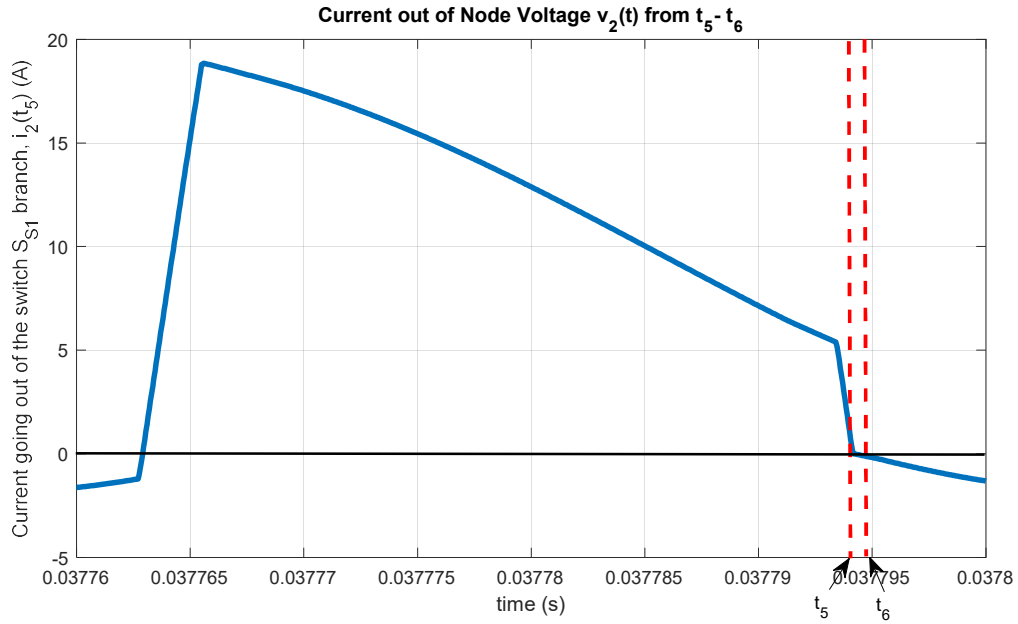
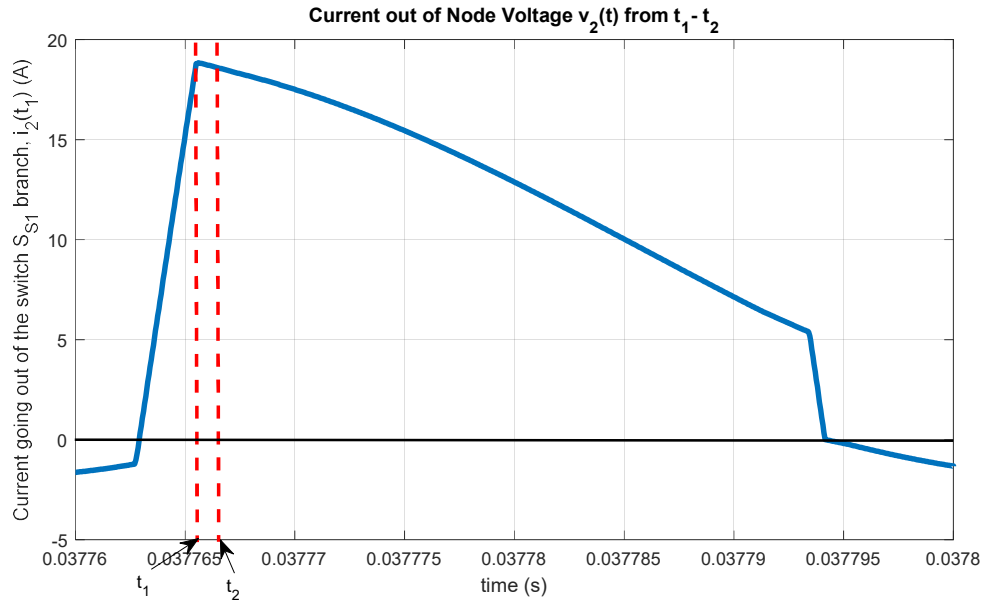Fig. 2.19: Current $i_2(t)$ flowing out of the node voltage $v_2(t)$ during interval t$_5$ -t$_6$.

Main operating mode M₄

At time t_6, auxiliary switch S_{S2} is turning ON at ZVS when current flowing through its body diode of S_{S2} becomes positive $(i_{S2}(t) = i_2(t))$, and main switch S_{P1} is already conducting. Fig. 2.20 illustrates the current paths of this main operating mode M₄ during the interval $t_6 < t < t_7$. The voltage across the inductor L_{eq} is equal to $[V_{CT2} - V_{Ca1} - V_{Cb1}]$ since the switches S_{P1} and S_{S2} are active. The current $i_{Leq}(t)$ is then given by:

$$i_{Leq}(t) = \frac{V_{CT2} - V_{Ca1} - V_{Cb1}}{Leq}(t - t_6) + i_{Leq}(t_6). \tag{2.19}$$

At time t_7, mode M₄ ends by turning OFF main switch S_{P1}. This mode's duration, T_{M4}, is calculated as follows:

$$T_{M4} = t_7 - t_6 = (d'_2 - \Delta_\emptyset) T_{sw} - (T_{T4} + T_{T3})/2 \tag{2.20}$$

where T_{T4} and T_{T3} are the durations of the transition modes T_4 and T_3, respectively. Fig. 2.21 presents the current $i_{Leq}(t)$ during this main operating mode M₄.

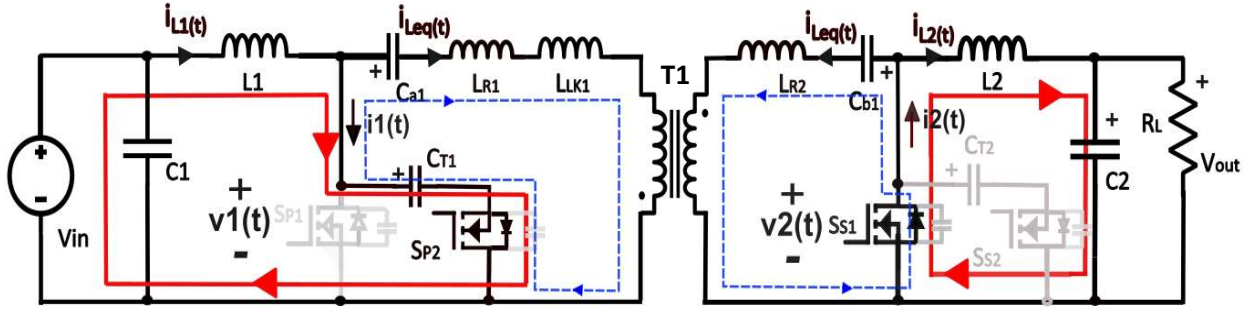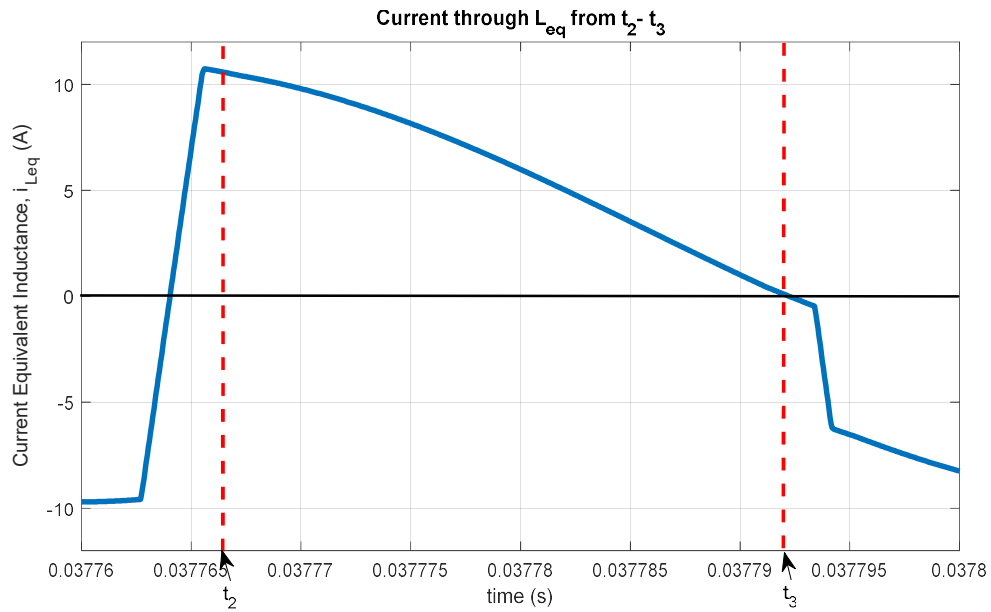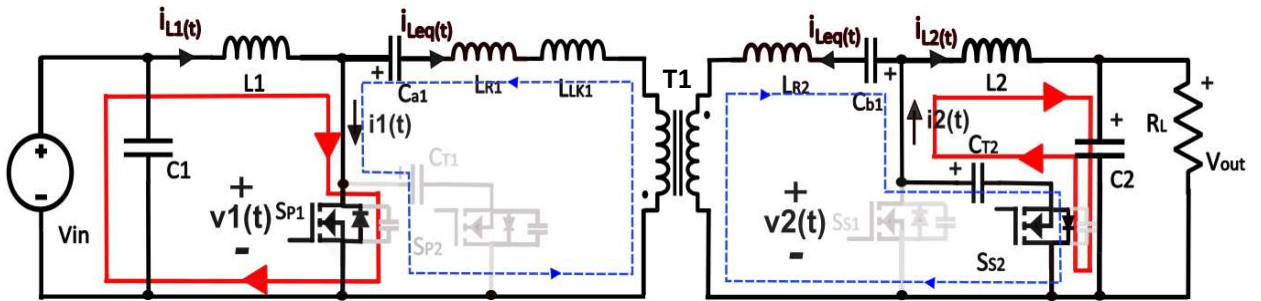Fig. 2.20: Main operating mode 4 [t₆ -t₇]: M₄.
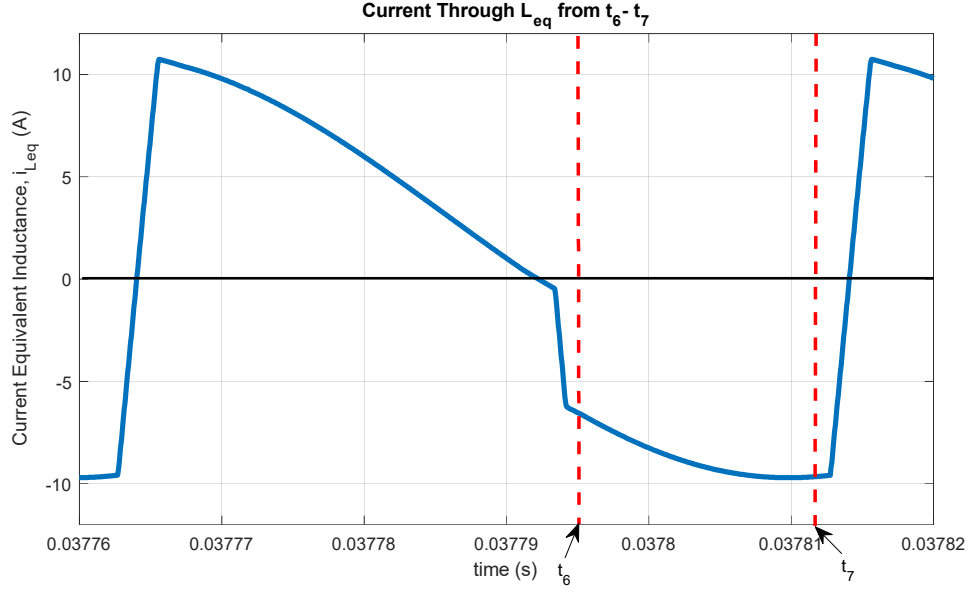
Fig. 2.21: Current through the equivalent inductance L_{eq} during interval t_6 -t_7.

Transition mode T₄

This transition mode shown in Fig. 2.22 occurs within the interval $t_7 < t < t_0 + T_{sw}$. At time t_7, main switch S_{P1} is turned OFF, so current $i_1(t)$ is transferred from S_{P1} to auxiliary switch S_{P2}. As a result, the output capacitance of S_{P2} ($C_{oss,P2}$) and the output capacitance of S_{P1} ($C_{oss,P1}$) are discharged and charged, respectively. In order for ZVS turn-ON of S_{P2}, $C_{oss,P2}$ must be completely discharged prior to applying its gate voltage. The end of this mode is signaled by the clamping of $v_1(t)$ by S_{P2}'s body diode as a result of the current $i_1(t)$. The duration of this transition mode T₄ and the current $i_1(t_7)$ are given by:

$$T_{T4} = t_0 + T_{sw} - t_7 = \frac{(C_{oss,P1} + C_{oss,P2})V_{CT1}}{-i_1(t_7)}$$

(2.21)

$$i_1(t_7) = (I_{L1} + \Delta I_{L1}) - i_{Leq}(t_7)$$

(2.22)

where $i_{Leq}(t_7)$ is given by (2.19). Fig. 2.23 displays the current $i_1(t_7)$ during this transition mode T₄.

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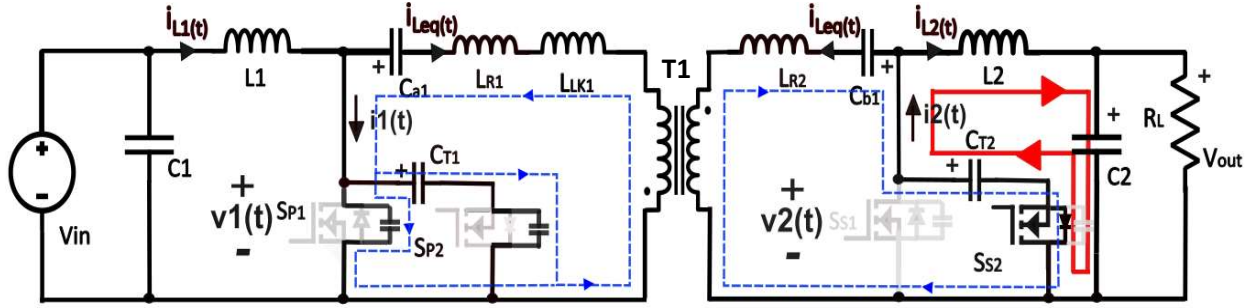
Fig. 2.22: Transition mode 4 [t_7 -t_0]: T_4.
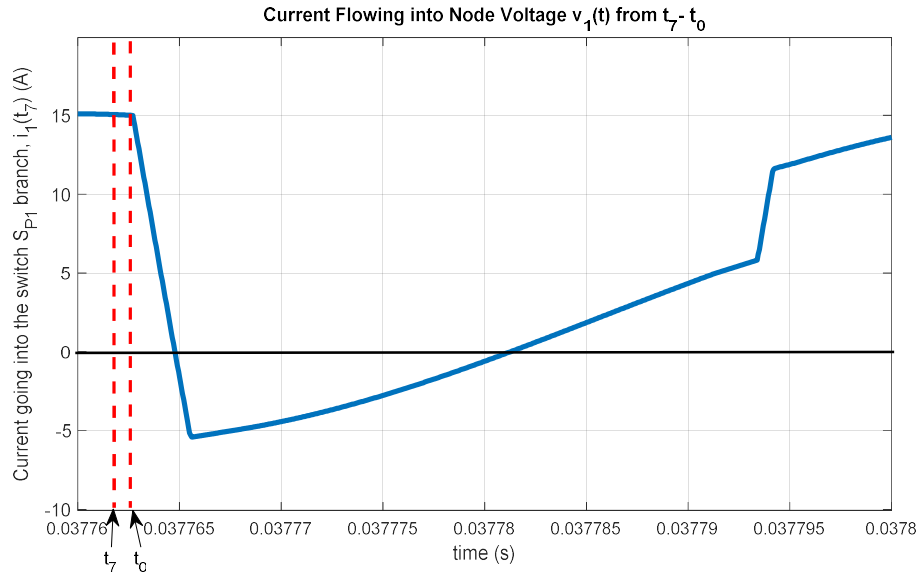
Fig. 2.23: Current $i_1(t)$ flowing into the node voltage $v_1(t)$ during interval t_7 -t_0.

2.5   System Analysis

A simplified model of the Ćuk converter as a primary referred circuit is considered to carry out a simple analysis of the power transfer, circulating current, and ZVS due to the need for series inductor current states. This model is depicted in Fig. 2.24.

The transition modes (T_1, T_2, T_3, and T_4) are active for very brief periods of time when compared to the main operating modes (M_1, M_2, M_3, and M_4). Therefore, the transition modes can be disregarded in power flow and circulating current analyses, which are crucial aspects of this topology.
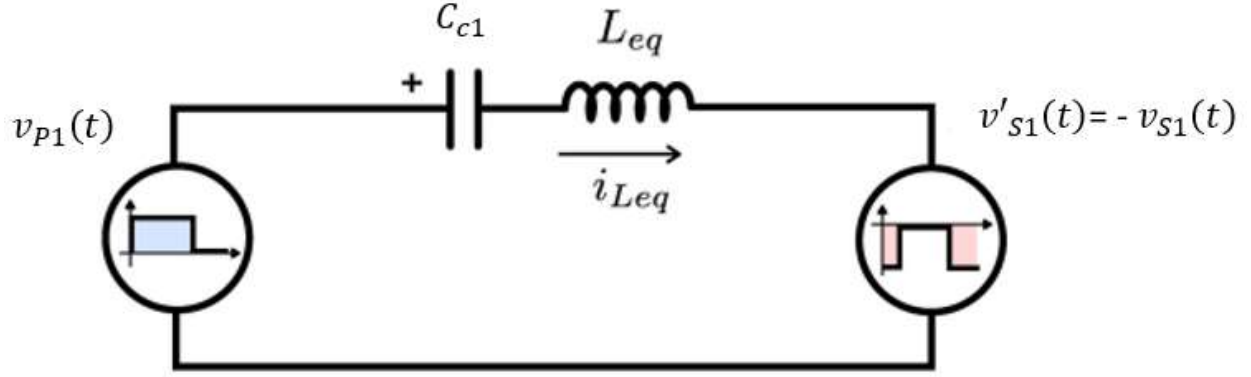
Fig. 2.24: Simplified primary-referred circuit of the isolated Ćuk converter [6], [7].

The node voltage $v_{S1}(t)$ referred to the primary side is represented by $v'_{S1}(t)$. The capacitor C_{c1} is the equivalent of C_{a1} and C_{b1} that are connected in series. The magnetizing inductance L_m is disregarded in the circuit because $L_m \gg L_{eq}$ [6], [7]. Components L_{eq} and C_{c1} are subjected to node voltages $v_{P1}(t)$ and $v'_{S1}(t)$. Volatges V_{in} and $-V_{out}$, the corresponding DC components of $v_{P1}(t)$ and $v'_{S1}(t)$, respectively, are blocked by C_{c1}.

2.5.1 Power transfer

The output power of this simplified converter is given by:

$$P_{out} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v'_{S1,ac}(t)\, i_{Leq}(t)\, dt \tag{2.23}$$

where $v'_{S1,ac}(t)$ is the ac equivalent of the dc node voltage $v'_{S1}(t)$ and $i_{Leq}(t)$ is the current through the equivalent inductor. The powers transferred within each main mode are obtained from (2.23) and given as follows [6], [7]:

$$P_1 = \frac{V_{CT1}V_{CT2}d_1d_2T_{sw}}{2L_{eq}}\Delta_\emptyset(d'_1 - \Delta_\emptyset) \tag{2.24}$$

$$P_2 = \frac{V_{CT1}V_{CT2}d_1d'_2T_{sw}}{2L_{eq}}\Delta_\emptyset(d'_1 - \Delta_\emptyset) \tag{2.25}$$

$$P_3 = \frac{V_{CT1}V_{CT2}d'_1d'_2T_{sw}}{2L_{eq}}(d'_2 - \Delta_\emptyset)(d_2 - d_1 + \Delta_\emptyset) \qquad (2.26)$$

$$P_4 = \frac{V_{CT1}V_{CT2}d'_1d_2T_{sw}}{2L_{eq}}(d'_2 - \Delta_\emptyset)(d_2 - d_1 + \Delta_\emptyset). \qquad (2.27)$$

Calculating the total power transferred under steady state over a switching cycle involves replacing the capacitor voltages from (2.2) and (2.3) into the power equations given above and yielding:

$$P_{out} = \frac{V_{in}V_{out}T_{sw}}{2L_{eq}}\left(2\Delta_\emptyset + (d_1 + d_2 - 1) - \frac{\Delta^2_\emptyset}{d'_1d'_2}\right). \qquad (2.28)$$

Equation (2.28) demonstrates that the power transferred depends on the three control parameters on which this converter's modulation techniques are based.

2.5.2 Circulating current

As previously mentioned, the ZVS turn-ON of all switches requires a circulating current through L_{eq}. To ensure ZVS, the circulating current should be limited to decrease conduction losses, so one may quantify this current by taking the mean square of $i_{Leq}(t)$ over a switching cycle. In addition, conduction losses are proportional to $I^2_{L,RMS}$ and also present due to the parasitic resistive components in $i_{Leq}(t)$. This mean square of $i_{Leq}(t)$ can be computed in each main operating mode as follows [6], [7]:

$$I^2_{L,RMS} = \frac{1}{T_{sw}}\sum_{i=1}^{4}\int_{t_{i-1}}^{t_i}i^2_{Leq}(t)\,dt \qquad (2.29)$$

and

$$i_{Leq}(t) = m_i(t - t_{i-1}) + i_{Leq}(t_{i-1}) \qquad (2.30)$$

where i is the index of the main operating modes, m_i is the slope of the current, and $i_{Leq}(t_{i-1})$ is the initial condition of the current at the start of the ith mode [6], [7]. Table 2.1 summarizes the calculations of the slopes and initial conditions of the current.

The total mean square current over a switching cycle is given by:

$$I^2{}_{L,RMS} = \left(\frac{T_{sw}}{L_{eq}}\right)^2 \left\{ \begin{array}{l} \dfrac{V_{out}(12V_{in}\Delta^2{}_\emptyset + V_{out})}{12} + \dfrac{V_{in}d_1{}^2(V_{in} + 4V_{out})}{12} \\[3mm] + \dfrac{V_{in}d'_2{}^2(4V_{in} + V_{out})}{12} - \dfrac{V_{out}d'_2(V_{out} + 6V_{in}\Delta_\emptyset)}{6} \\[3mm] - \dfrac{V_{in}V_{out}\Delta_\emptyset{}^3)}{3d'_2 - 3d_1d'_2} - \dfrac{V_{in}V_{out}d_1(3d'_2 - 6\Delta_\emptyset + 1)}{6} \end{array} \right\}. \tag{2.31}$$

Table 2.1: Series Inductor Current for Each Main Operating Mode [6], [7]

Main Mode	Slope of $i_{Leq}(t)$ for the ith mode	Initial current at the start of the ith mode
M_1	$m_1 = (V_{CT1}d_1 + V_{CT2}d_2)/L_{eq}$	$i_{Leq}(t_0) = (-0.5d_1d'_1V_{CT1} - 0.5d_2d'_2V_{CT2} + (d'_2 - \Delta_\emptyset)d_2V_{CT2})T_{sw}/L_{eq}$
M_2	$m_2 = (V_{CT1}d_1 - V_{CT2}d'_2)/L_{eq}$	$i_{Leq}(t_1) = (-0.5d_1d'_1V_{CT1} + \Delta_\emptyset d_1V_{CT1} + 0.5d_2d'_2V_{CT2})T_{sw}/L_{eq}$
M_3	$m_3 = (-V_{CT1}d'_1 - V_{CT2}d'_2)/L_{eq}$	$i_{Leq}(t_2) = (0.5d_1d'_1V_{CT1} + 0.5d_2d'_2V_{CT2} - (d'_1 - \Delta_\emptyset)d'_2V_{CT2})T_{sw}/L_{eq}$
M_4	$m_4 = (-V_{CT1}d'_1 + V_{CT2}d_2)/L_{eq}$	$i_{Leq}(t_3) = (0.5d_1d'_1V_{CT1} - (d_1 - d'_2 + \Delta_\emptyset)d'_1V_{CT} - 0.5d_2d'_2V_{CT2})T_{sw}/L_{eq}$

2.5.3 ZVS operation

The output capacitance (C_{oss}) of the ZVS turn-ON switch must be fully discharged and the C_{oss} of the ZVS turn-OFF switch must be fully charged within the deadband t_{db} [8], [9]. The C_{oss} and t_{db} between the gates of the complementary switches are considered constants. To gain complete ZVS turn-ON of the switches, the deadband t_{db} between the complementary switches needs to be longer than the switching transition duration. The switch's minimum allowable threshold current, $i_{ZVS,min}$, which allows the switches to charge and discharge their output capacitances within t_{db}, is calculated as follows [6], [7]:

$$i_{ZVS,min} = \frac{2C_{oss}V_{DS}}{t_{db}} \tag{2.32}$$

where V_{DS} represents the voltage across the switch that is turning OFF.

In Table 2.2, where $i_{Leq}(t_i)$ at the time of transition is taken from Table 2.1, the criteria on the current $i_{Leq}(t)$ that must be met to ensure that there is sufficient current flowing through the switches at the point of transition for ZVS to turn ON are provided.

From an analysis of Table 2.2, the ZVS turn-ON of S_{P1} and S_{S2} switches requires proper selection of the control parameters d_1, d_2, and $\Delta_\emptyset$, whereas the conditions for the other two

Table 2.2: Conditions of $i_{Leq}(t)$ to Ensure ZVS Turn-ON

ZVS on the switches	Conditions of $i_{Leq}(t)$
ZVS on S_{P1}	$i_{Leq}(t_2) > (I_{in} - \Delta I_{in}) + 2C_{oss}V_{CT1}/t_{db}$
ZVS on S_{P2}	$i_{Leq}(t_0) < (I_{in} + \Delta I_{in}) - 2C_{oss}V_{CT1}/t_{db}$
ZVS on S_{S1}	$i_{Leq}(t_1) > -(I_{out} + \Delta I_{out}) + 2C_{oss}V_{CT2}/t_{db}$
ZVS on S_{S2}	$i_{Leq}(t_3) < -(I_{out} - \Delta I_{out}) - 2C_{oss}V_{CT2}/t_{db}$

switches are generally easily satisfied. Equations (2.33) and (2.34) provide the conditions for ZVS turn-ON of S_{P1} and S_{S2} switches, respectively [6], [7]:

$$d_{1,ZVS(P1)} > \frac{\left(\frac{G}{L_{eq}}\left(1 - \frac{\Delta^2{}_{\emptyset}}{d'_1 d'_2}\right)\right) + \frac{4C_{oss}}{d'_1 t_{db} T_{sw}}}{\left(\frac{G+1}{L_{eq}} + \frac{1}{L_1}\right)} \tag{2.33}$$

$$d_{2,ZVS(S2)} > \frac{\left(\frac{1}{L_{eq}}\left(1 - \frac{\Delta^2{}_{\emptyset}}{d'_1 d'_2}\right)\right) + \frac{4C_{oss}}{d'_2 t_{db} T_{sw}}}{\left(\frac{G+1}{L_{eq}} + \frac{G}{L_2}\right)} \tag{2.34}$$

where G is the converter gain V_{out}/V_{in}. The ZVS boundary conditions of (2.33) decreases while (2.34) increases when G increases.

2.6   Concluding Remarks

In Chapter 2, the theoretical aspects of the isolated bidirectional Ćuk dc-dc converter topology are explored, providing readers the knowledge needed to comprehend the converter's forward mode of operation. The reader can thus better understand simulation and experimental results through the various modes of operation.

Chapter 3 intends to assist readers in beginning their own designs by guiding them to establish the system parameters and run simulations using MATLAB/Simulink™. In this chapter, a quantitative analysis is performed to interpret the operation of the converter by collecting and evaluating measurable and verifiable data through simulations.

2.7   References

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CHAPTER 3

DESIGN AND SIMULATIONS OF ISOLATED BIDIRECTIONAL ĆUK CONVERTER

3.1 Introduction

The previous chapter presented the theoretical analysis of the isolated bidirectional Ćuk dc-dc converter topology. Chapter 3 focuses on the design and simulations of the Ćuk dc-dc converter utilizing MATLAB/Simulink^{TM}. The main objective of this chapter is to explain the process for designing and developing the circuit model to run simulations validating the knowledge gained in Chapter 2. The main specifications of this converter are an input voltage of 300 V, output voltage of 213 V, rated output power of 1.5 kW, and switching frequency of 20 kHz.

The structure of this chapter is organized as follows: Section 3.2 addresses an overview of the selection of the hardware components and control parameters. Section 3.3 presents the procedure used for designing the Ćuk-based dc-dc prototype. Section 3.4 discusses the components used in the circuit and the implementation of the control algorithm in MATLAB/Simulink^{TM}. Moreover, a quantitative analysis is carried out to verify the proper function of the converter by gathering and evaluating measurable data using the simulation results. Then, Section 3.5 provides a summary of the accomplishments of this entire chapter and describes the goals of the following chapter.

3.2 Determining System Parameters

3.2.1 Hardware design

It is evident that active and passive components are necessary for power transfer, minimizing circulating current, and achieving ZVS conditions. Thus, proper selection of the

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active and passive components depending on the control parameter range is important. In particular:

MOSFET selection: The maximum voltage across the auxiliary capacitors C_{T1} and C_{T2} determines the voltage ratings of the main and auxiliary switches on the primary and secondary sides since these are clamped by these auxiliary capacitors. Equations (2.2) and (2.3) determine the value of the maximum voltage across the primary and secondary main and auxiliary switches of the converter, respectively. Ideally, the maximum voltage across the switch is given by the sum of the input and output voltages. From the turn-OFF currents through the switches S_{P1}, S_{P2}, S_{S1}, and S_{S2} at the end of the main operating modes M_1 and M_2, the absolute peak currents through these switches can be determined as follows:

$$I_{P1,max} = I_{P2,max} = \left|(I_{in} + \Delta I_{in}) - i_{Leq,max}(t_0)\right| \qquad (3.1)$$

$$I_{S1,max} = I_{S2,max} = \left|(I_{out} + \Delta I_{out}) + i_{Leq,max}(t_1)\right|. \qquad (3.2)$$

where I_{in} and I_{out} are the mean input and output current values, respectively; ΔI_{in} and ΔI_{out} are neglected because the input and output inductors are coupled in an Integrated Magnetic (IM) structure to achieve zero inductor current ripple; and $i_{Leq,max}(t_0)$ and $i_{Leq,max}(t_1)$ are calculated using KCL in the circuit.

Equivalent series inductance, L_{eq}: Due to the fact that both power transfer and circulating current are inversely proportional to L_{eq}, this inductance is crucial for the ZVS turn-ON of the switches, where (2.28) and (2.31) play a crucial role. For ZVS under turn-ON conditions, the designer must choose an inductance that can handle the smallest amount of load required. According to [1] and [2], increasing L_{eq} decreases the output power and mean square circulating current per Watt. Equation (3.3) represents the minimum condition for L_{eq} and is obtained as:

$$L_{eq} > \frac{V_{in}V_{out}T_{sw}}{2P_{min}}\left(2\Delta_\emptyset + d_{1,ZVS} + d_{2,ZVS} - 1 - \frac{\Delta^2_\emptyset}{d'_{1,ZVS}d'_{2,ZVS}}\right) \qquad (3.3)$$

where P_{min} is the minimum required output load and $d_{1,ZVS}$ and $d_{2,ZVS}$ are the expressions for the ZVS boundary turn-ON of S_{P1} and S_{S2} switches given in (2.33) and (2.34) for a constant phase-shift $\Delta_\emptyset$.

Input and output inductors, L_1 and L_2: The ripple requirements are considered while selecting these inductors when designing a typical Ćuk converter. ZVS boundary limitations, however, show that larger inductor current ripple over the inductors is preferable to help with ZVS operation [1], [2]. However, for our purpose, the input and output inductors are connected in an Integrated magnetics (IM) structure to accomplish zero inductor current ripple.

Auxiliary capacitors, C_{T1} and C_{T2}: Both capacitors are selected to ensure that the circuit formed by the auxiliary and blocking capacitors and L_{eq} has a resonance period significantly longer than the main operating modes M₂ and M₄, respectively. The following conditions can be applied to choose the value of the auxiliary capacitors C_{T1} and C_{T2}:

$$(1 - d_{1,max} - \Delta_\emptyset)T_{sw} \ll 2\pi\sqrt{L_{eq}\left(C_{T1}||C_{a1}||C_{b1}\right)} \qquad (3.4)$$

$$(1 - d_{2,max} - \Delta_\emptyset)T_{sw} \ll 2\pi\sqrt{L_{eq}\left(C_{T2}||C_{a1}||C_{b1}\right)} \qquad (3.5)$$

where $d_{1,max}$ and $d_{2,max}$ are the maximum duty cycles limited by the capacitor and switch voltage ratings [1], [2].

3.2.2 Control parameters

As mentioned in Chapter 2, the modulation techniques of the analyzed Ćuk converter are based on three control parameters: d_1, d_2, and $\Delta_\emptyset$. Depending on the required purpose, one can

choose the parameters for a certain operation. The objective of this study is to lower the circulating current by optimizing the duty cycles d_1 and d_2 for a constant phase-shift ratio [1], [2].

Phase-shift ratio, $\Delta_\emptyset$: The circulating current is caused by the phase difference produced by the two duty cycles, which helps in achieving ZVS turn-ON of the switches. Following the ideas in [1] and [2], a small fixed phase-shift ratio of 0.09 is selected.

Duty cycles, d_1 and d_2: The minimum duty cycles are limited by the ZVS boundary given in (2.33) and (2.34) while the maximum duty cycles are restrained by the voltage rating of the switches and the auxiliary capacitors given by (2.2) and (2.3).

Assuming a constant $\Delta_\emptyset$ of 0.09 [6], Fig. 3.1 presents a 3-D plot of power transferred to the output as a function of the control parameters (d_1 and d_2). The data point on Fig. 3.1 represents the values of $x = d_1$ and $y = d_2$ for an output power of $z = 1511.86$ W used for the design carried out in this thesis.
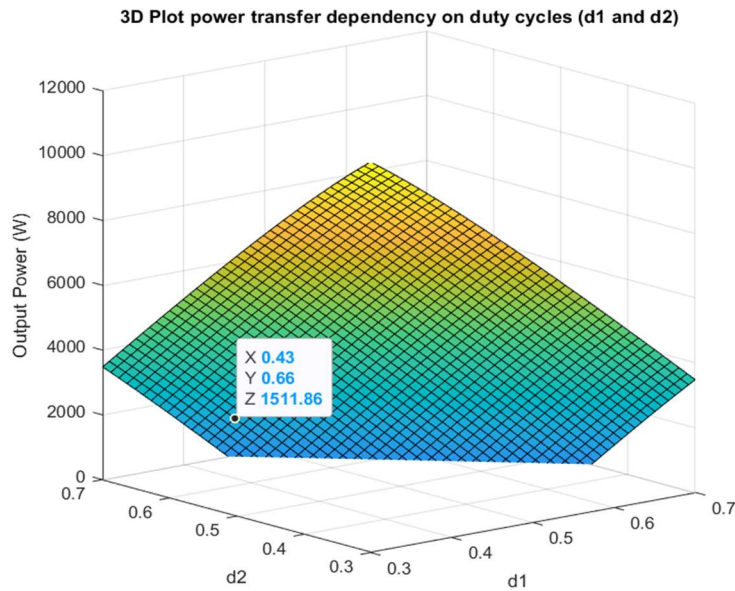
Fig. 3.1: Three-dimensional plot showing power transfer dependency on duty cycles (d_1 and d_2) for $V_{in} = 300$ V, $V_{out} = 213$ V, $L_{eq} = 69$ µH and $\Delta_\emptyset = 0.09$.

To further grasp the connection between the circulating current and the control parameters, Fig. 3.2 shows the mean square current of the series inductor normalized by power transferred and dependency on the duty cycle of main switch S_{P1}, d_1 and duty cycle of main switch S_{S1}, d_2 for a constant phase-shift ratio Δ_ϕ of 0.09. By optimizing the three control parameters, it is possible to determine the minimum current for the required output power from the convex shape of the plot. The data point on Fig. 3.2 represents the approximation values of $x = d_1 = 0.43$, $y = d_2 = 0.66$ and $z = 0.2725$ A^2/W used to get an idea of the conduction losses for the design. The value of z is very close to its minimum value of 0.249 A^2/W corresponding to $d_1 = 0.3$ and $d_2 = 0.7$.
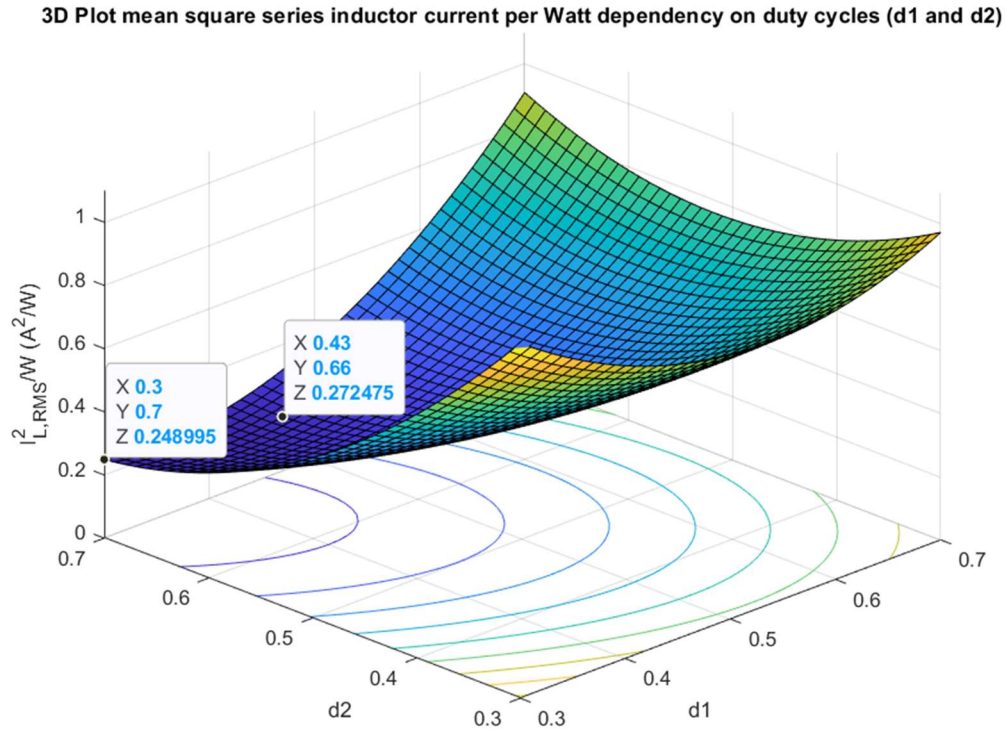
Fig. 3.2: Three-dimensional plot of the mean square series inductor current per Watt dependency on duty cycles (d_1 and d_2) for V_{in}= 300 V, V_{out}= 213 V, L_{eq}= 69 µH and Δ_ϕ= 0.09.

3.3 Design Process of the Isolated Ćuk DC-DC Prototype

The specifications of the design considered in this thesis are:

$$V_{in} = 300 \ V$$

$$V_{out} = 213 \ V$$

$$P_{rated} = 1.5 \ kW$$

$$T_{sw} = 50 \ \mu s$$

$$n = 1$$

The following equations are used to determine the design parameters of the isolated Ćuk

dc-dc converter:

$$D = \frac{V_{out}/n}{V_{in} + V_{out}/n} \cong 0.43 = d_1 \tag{3.6}$$

$$R_L = \frac{V_{out}^2}{P_{rated}} = \frac{213^2}{1500} \cong 30 \ \Omega \tag{3.7}$$

Typical values of Δv_{ripple} are 1%, 2%, 5%, 10%, etc. The application determines the

specific ripple values. Selecting $\Delta v_{Ca1} = 5 \ \%$ and $\Delta v_{Cb1} = 5 \ \%$ yield:

$$C_{a1} = \frac{V_{out} \ n \ DT_{sw}}{2 \ R_L \ \Delta v_{Ca1}} = 15.265 \ \mu F \tag{3.8}$$

$$C_{b1} = \frac{V_{out} \ DT_{sw}}{2 \ R_L \ \Delta v_{Cb1}} = 15.265 \ \mu F \tag{3.9}$$

Selecting $\Delta v_{C2} = 1 \ \%$ and having $L_2 = 620 \ \mu H$, yields:

$$C_2 = \frac{V_{out} \ (1 - D)T_{sw}^2}{8 \ L_2 \ R_L \ \Delta v_{C2}} = 3 \ \mu F \tag{3.10}$$

Common discrete values for capacitors such as those in [3] lead the designer to select the

closest values available in the market to the calculated ones considering voltage and current

handling capacities. As a result, capacitors C_{a1}, C_{b1}, and C_2 are selected to be 15 μF, 15 μF, and 3 μF, respectively.

One can theoretically achieve zero current ripple in both the input and output currents of the dc-dc Ćuk converter by using the IM topology presented in [4], which integrates the transformer, input, and output inductors into a single magnetic structure. The transformer for this prototype was designed by doctoral student David Porras and built by myself for a related project.

Table 3.1 shows the specified and calculated data of the system at rated conditions of 1.5-kW, 300 V_{dc} at the input and 213 V_{dc} at the output.

Table 3.1: Parameters of the Designed Prototype

Parameters	Value	Unit
Input voltage (Vin)*	300	V
Output voltage ($Vout$)*	213	V
Output power ($Pout$)*	1.5	kW
Switching frequency (f_{sw})*	20	kHz
Voltage ripple across C_{a1} and C_{b1} (Δv_{Ca1}, Δv_{Cb1})*	5	%
Voltage ripple across C_2 (Δv_{C2})*	1	%
Turns ratio (1:n)*	1	
Input and output inductors (L_1 and L_2)*	620	μH
Load resistance (R_L) [#]	30	Ω
Duty cycle ($D = d_1$) [#]	0.43	
Series capacitors (C_{a1} and C_{b1}) [#]	15	μF
Output Capacitor (C_2) [#]	3	μF

* Input Data, [#] Calculated Data

Table 3.2 presents the remaining component values used in the converter. SiC MOSFET devices with lower rated voltage could have been used, but these ones were selected for a related project having higher voltage ratings. The gain G is calculated as follows:

$$G = \frac{V_{out,rated}}{V_{in,rated}} = 0.71 \tag{3.11}$$

Table 3.2: Other Component Values for the Designed Prototype

Component Specifications	Value	Unit
Input Capacitor (C_1)	3	μF
Primary auxiliary capacitor (C_{T1})	7.5	μF
Secondary auxiliary capacitor (C_{T2})	2.2	μF
Series resonant inductors (L_{R1} and L_{R2})	31	μH
Leakage inductors (L_{LK1} and L_{LK2})	3.6	μH
Equivalent series inductor (L_{eq})	69	μH
MOSFETs ($S_{P1}, S_{P2}, S_{S1}, S_{S2}$)	C2M0045170D	1.7 kV
Hitachi CC cores for L_{R1} and L_{R2}	F3CC0010	
Hitachi CC cores for IM	AMCC-320	
Gain (G)	0.71	
$\Delta_\emptyset$	0.09	

This application could have used 900 V or 1200 V SiC MOSFETs since the theoretical peak voltage across the switches when OFF is 513 V (300 V + 213 V). However, the author of this thesis is leveraging a prototype built for a related project.

3.4 MATLAB/Simulink™ Simulations

3.4.1 Implementation of the circuit schematic

Simulations are performed using the circuit model presented in Fig. 2.7 with all the parameters listed in Tables 3.1 and 3.2.

Figure 3.3 shows the schematic of the implemented isolated bidirectional Ćuk dc-dc converter using MATLAB/Simulink™. Input and output capacitors are represented as C_1 and C_2, respectively, and the IM structure as block IM whose schematic is given in [3]. The 1.7-kV discrete SiC power MOSFETs are used for main switches S_{P1} and S_{S1} as well as the auxiliary switches S_{P2} and S_{S2} that were added to operate the converter under soft-switching conditions. Other components are the blocking capacitors C_{a1} and C_{b1}, series resonant inductors L_{R1} and L_{R2}, and capacitors C_{T1} and C_{T2}. All the inductors and capacitors have an equivalent series resistance (ESR) of 10 mΩ to make them non-ideal as the simulation results are going to be
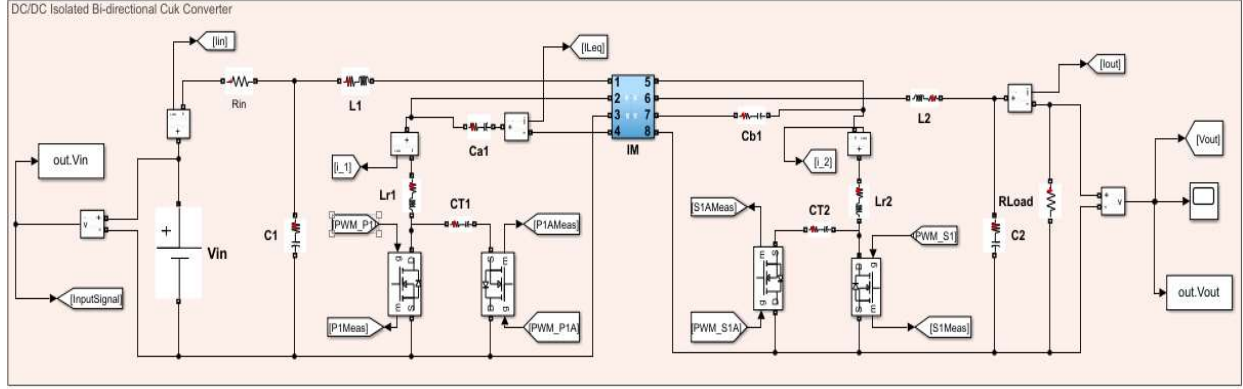
Fig. 3.3: Simulation model in Simulink.

compared with the experimental results in the built prototype.

3.4.2   Implementation of the system control algorithm

As already mentioned, the circuit control algorithm schematic presented in Fig. 3.4 is based on these three control parameters: the duty cycle of S_{P1}, d_1; duty cycle of S_{S1}, d_2; and the phase-shift ratio $\Delta_\emptyset$. To ensure the ZVS of all switches, deadband times or ON delays are added to the algorithm to help with the phase-shift time. Only one duty cycle ($D = d_1 = 0.43$) is used for simplicity in the controller since it is the duty cycle of the main switch S_{P1} that determines 213 V_{dc} at the output with an input voltage of 300 V.

For the controller in Fig. 3.4, a PWM generator with phase delay block is needed. This block has three inputs: D, f_{sw}, and delay. The values of D and f_{sw} given in Table 3.1 are 0.43 and 20 kHz, respectively. The delay variable time (t_{delay}) is the delay time between the time periods when main switch S_{P1} is turned OFF and auxiliary switch S_{S2} is turned ON, which is set to 2.8 μs. The outputs of the block are the PWM and shifted PWM signals for the primary and secondary switches, respectively. After these signals, ON delays or deadband times (t_{db}) are needed for ZVS operation, which are the times used between the gate signals of the main and auxiliary switches when they are turned OFF. These ON delay are set to (2.2, 1.7, 1.2, and 1.7)
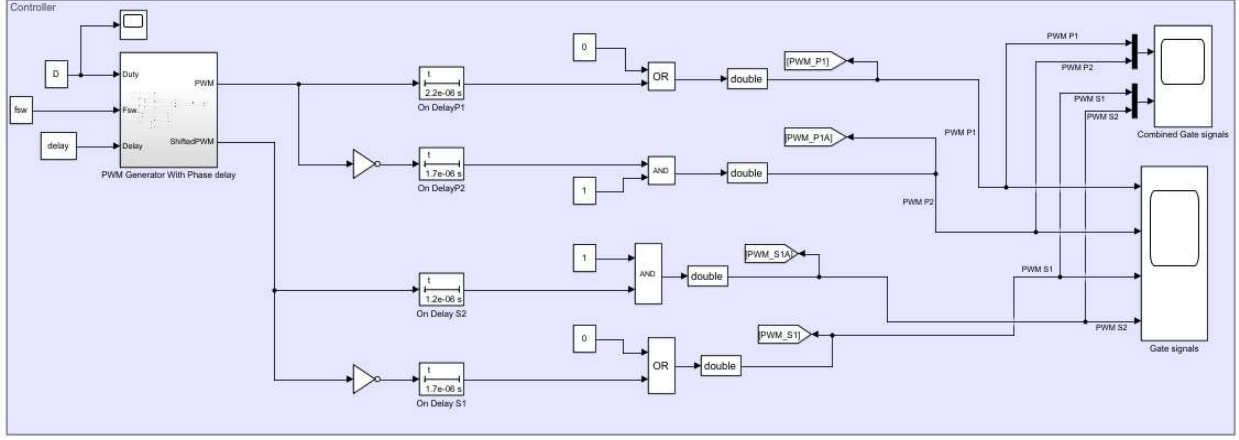
Fig. 3.4: Control algorithm schematic in Simulink.

μs for switches S_{P1}, S_{P2}, S_{S2}, and S_{S1}, respectively. Some logical operators are needed for the logic of the controller to function. Two NOT gates or inverters are needed to invert the signals of switches S_{P2} and S_{S1}. Two OR gates are used as the operator for signals of main switches S_{P1} and S_{S1}. The two inputs of the OR gate for S_{P1} are zero and the PWM signal delayed by the deadband time t_{db} of S_{P1}, while the two inputs of the OR gate for S_{S1} are zero and the shifted PWM signal also delayed by the t_{db} of S_{S1}. Two AND gates are used as the operator for signals of the auxiliary switches S_{P2} and S_{S2}. The inputs of the AND gate for S_{P2} are the PWM signal delayed by the t_{db} of S_{P2} and one, while the inputs of the AND gate for S_{S2} are the phase-shifted PWM signal delayed by t_{db} of S_{S2} and one. The outputs for all four gates are the double precision data type conversion block, which converts the input to double precision data type and scale the output. These outputs are also connected to scopes for analyzing the PWM signal of each switch.

The phase-shift time is calculated as the phase-shift ratio $\Delta_\emptyset$ times the switching period T_{sw} as follows:

$$t_{\Delta_\phi} = \Delta_\phi \, T_{sw} = 4.5 \, \mu s \qquad (3.12)$$

The phase-shift time for the simulation is calculated when both main switches S_{P1} and S_{S1} are OFF. This interval of time is calculated as the sum of the t_{delay} when both switches S_{P1} and auxiliary switch S_{S2} are OFF and t_{db} when both main switch S_{S2} and S_{S1} are also OFF and is given by:

$$t_{\Delta\phi} = t_{delay} + t_{db,\,S_{S1}-S_{S2}\,OFF} = (2.8 + 1.7)\,\mu s = 4.5\,\mu s \qquad (3.13)$$

3.4.3 Simulation Results

Simulations were run for the following operating conditions: input voltage of 300 V, output voltage of 213 V, rated output power of 1.5 kW, switching frequency of 20 kHz, voltage ripple across C_{a1} and C_{b1} of 5%, and voltage ripple across C_2 of 1%.

Fig. 3.5 provides the maximum voltages across the main and auxiliary switches (i.e., S_{P1}, S_{P2}, S_{S1}, and S_{S2}). The maximum voltages obtained from the simulation are (494.6, 489.9, 510.3, 503.1) V for switches S_{P1}, S_{P2}, S_{S1}, and S_{S2}, respectively. The maximum voltages across the primary side switches S_{P1} and S_{P2} are clamped by the auxiliary capacitor C_{T1} while the maximum voltages across the secondary switches S_{S1} and S_{S2} are clamped by C_{T2}. The theoretical value without any active clamp circuit should be 513 V (300 V + 213 V). The simulated values illustrate the effectiveness of the active clamp circuits.

Fig. 3.6 presents the instantaneous currents that are relevant to the analysis of the system. These currents are the ones flowing through main switch S_{P1}, $i_1(t)$; main switch S_{S1}, $i_2(t)$; and L_{eq}, $i_{Leq}(t)$. The peak values are (15.1, 18.9, and 10.7) A, respectively. The theoretical peak currents $I_{P1,max}$ and $I_{S1,max}$ calculated using (3.1) and (3.2) are 14.6 A (5 A - (-9.6 A) and 17.6 A (7.04 A + 10.6 A), respectively. The values from the simulations are fairly close to the theoretical values.
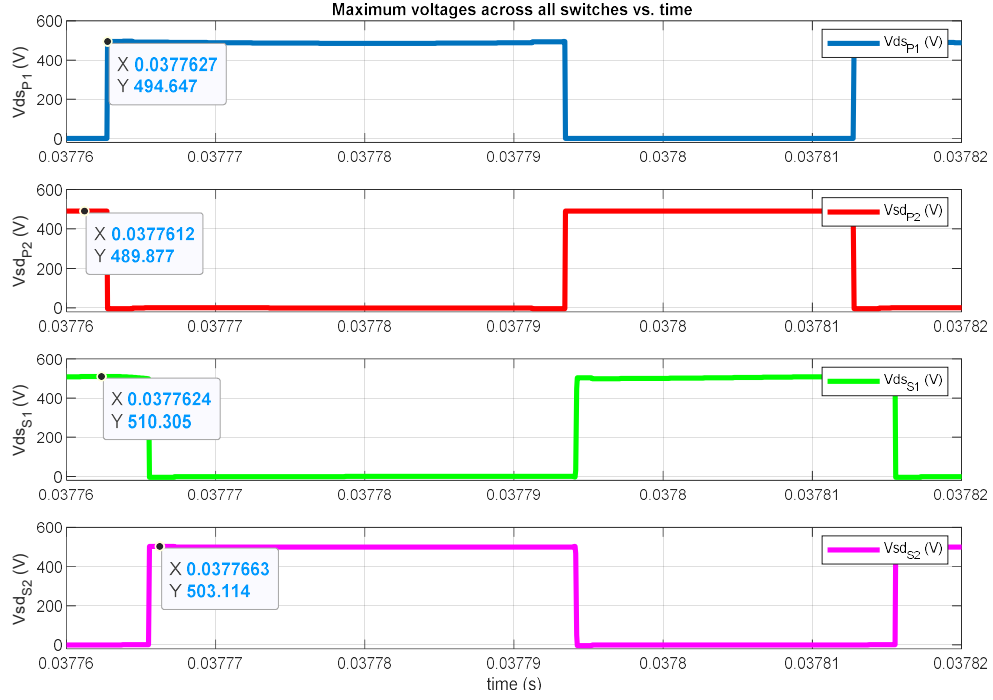
Fig. 3.5: Maximum voltages across switches S_{P1} (top), S_{P2} (second), , S_{S1} (third), and S_{S2} (bottom).
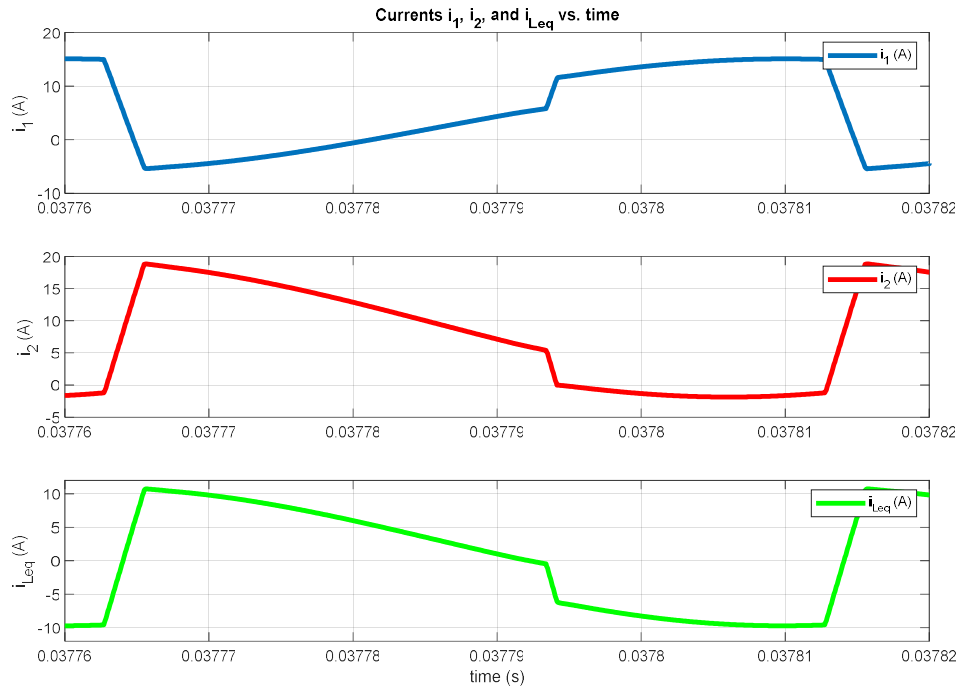
Fig. 3.6: Currents i_1 (top), i_2 (middle), and i_{Leq} (bottom) vs. time.

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Fig. 3.7 uses the cursor measurement tool to display the phase-shift time measurement $t_{\Delta\phi}$ used for the shifted PWM between the time periods when both main switches S_{P1} (top waveform) and S_{S1} (third waveform) are inactive during a switching period, T_{sw}. This value is 4.426 μs which compares with the theoretical value of 4.5 μs.

Fig. 3.8 presents the delay time t_{delay} to ensure soft-switching in all switches between the time difference when main switch S_{P1} turns OFF (top waveform) and auxiliary S_{S2} turns OFF (bottom waveform). This value is 2.812 μs which compares with the theoretical value of 2.8 μs.

Fig. 3.9 illustrates the deadband time t_{db} of 1.614 μs used between the gate signals of the main S_{S1} (third waveform) and auxiliary S_{S2} (bottom waveform) switches when they are inactive.

Table 3.3 depicts the mean values of the input voltage (i.e., 300 V) and output voltage (i.e., 212.9 V). Their input and output current mean values were (5.46 and 7.10) A, respectively. The theoretical values of the mean input and output currents I_{in} and I_{out}, respectively, are 5 A (1500 W/300 V) and 7.04 A (1500 W/213 V), respectively. The simulated and theoretical values compared fairly well. The input and output powers can be calculated theoretically using the current and voltage values obtained from the simulation.

Table 3.3: Signal statistics of the input and output currents and voltages.

Trace Selection: Vin		Trace Selection: Iin		Trace Selection: Vout		Trace Selection: Iout	
Signal Statistics		**Signal Statistics**		**Signal Statistics**		**Signal Statistics**	
Value	Time	Value	Time	Value	Time	Value	Time
Max 3.000e+02	0.000e+00	Max 2.135e+01	7.948e-04	Max 2.962e+02	1.342e-03	Max 9.874e+00	1.342e-03
Min 3.000e+02	0.000e+00	Min -2.183e+00	1.830e-03	Min -1.326e+02	1.236e-04	Min -4.421e+00	1.236e-04
Peak to Peak 0.000e+00		Peak to Peak 2.353e+01		Peak to Peak 4.289e+02		Peak to Peak 1.430e+01	
Mean 3.000e+02		Mean 5.455e+00		Mean 2.129e+02		Mean 7.098e+00	
Median 3.000e+02		Median 5.350e+00		Median 2.152e+02		Median 7.172e+00	
RMS 3.000e+02		RMS 5.677e+00		RMS 2.147e+02		RMS 7.157e+00	

Fig. 3.7: Gate signals for S_{P1} (top), auxiliary S_{P2} (second), S_{S1}(third), and auxiliary S_{S2} (bottom).
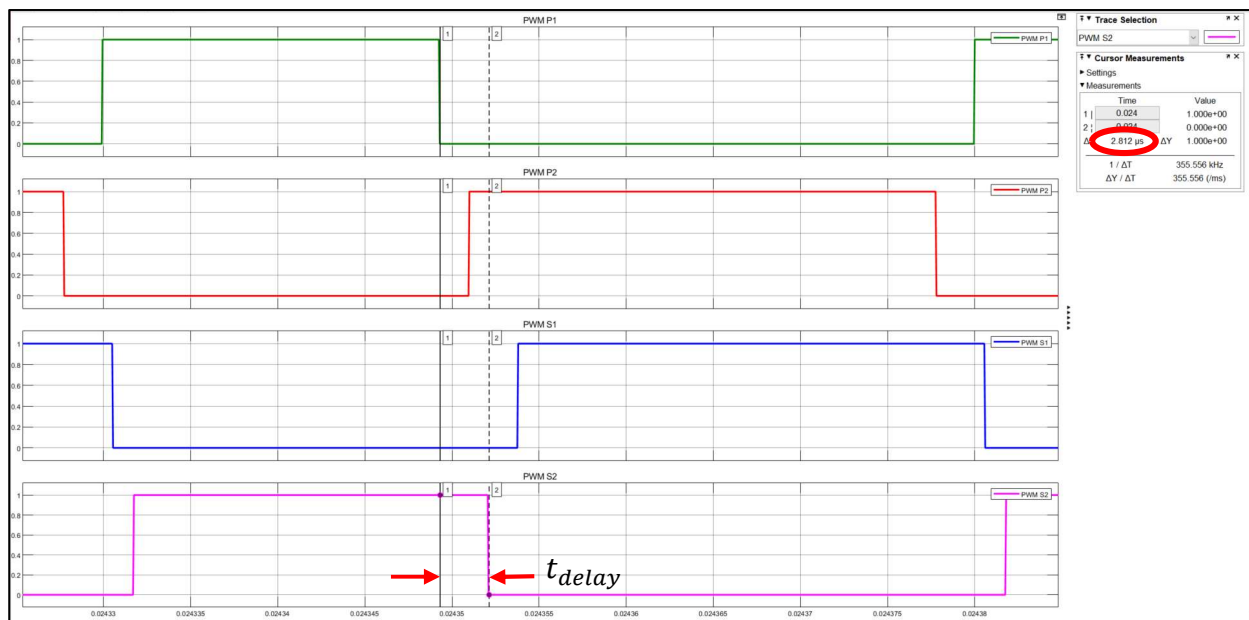
Fig. 3.8: Delay time between the time difference when S_{P1} turns OFF (top) and S_{S2} turns OFF (bottom).
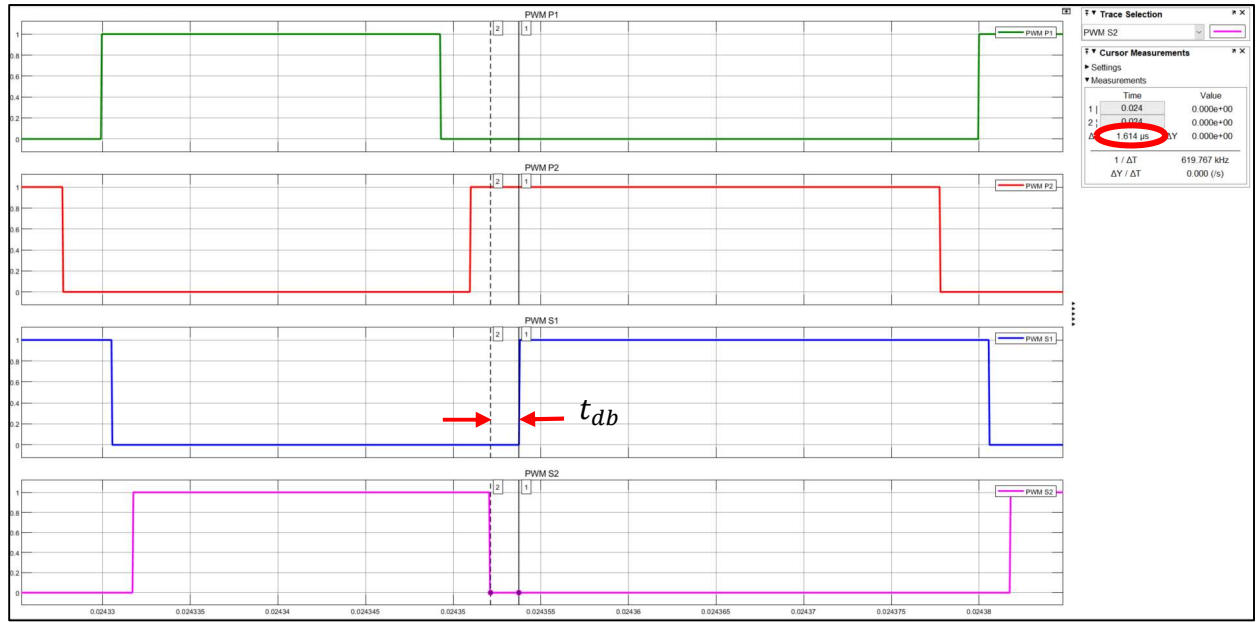
Fig. 3.9: Deadband time between the time periods when both S_{S1} (third) and S_{S2} (bottom) are OFF.

3.5   Concluding Remarks

Chapter 3 provided the design and simulations of the isolated bidirectional Ćuk dc-dc converter, assisting readers in beginning their own designs by demonstrating how to set up the system parameters and carry out simulations with MATLAB/Simulink[TM]. The reader can perform a quantitative analysis of the converter operation and compare with the theoretical analysis given in Chapter 2.

Chapter 4 aims to demonstrate the setup of the prototype and experimental results to validate the operation of the Ćuk converter throughout measurable data that could be compared with data collected through simulations as well as the theoretical analysis from previous chapters.

3.6   References

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CHAPTER 4

EXPERIMENTAL RESULTS OF THE ISOLATED ĆUK DC-DC PROTOTYPE

4.1 Introduction

Chapter 3 provided the design and simulation data to better understand the theoretical analysis of the isolated Ćuk converter presented in Chapter 2. Chapter 4 experimentally validates the stages of theoretical understanding and simulation analyses through a built 1.5 kW prototype of using the testing facilities at the ENRC laboratory complex.

The structure of Chapter 4 is as follows: Section 4.2 addresses the equipment needed for testing. Section 4.3 presents the physical implementation of the prototype and its testing. Section 4.4 discusses an analysis of the three design stages: theoretical understanding, simulations, and prototyping. Section 4.5 provides a summary of the accomplishments of this entire chapter and describes the goal of the following chapter.

4.2 Testing

Fig. 4.1 illustrates the test bench used to obtain the experimental data. Probes and communication cables are routed to a table in the test area to ease the operations of collecting waveforms/measurements and reprogramming the controller. Fig. 4.2 shows the built prototype of the Ćuk-based dc-dc converter prototype. Table 4.1 provides all the equipment and instrumentation used for the experimental results.

Table 4.1: Test Equipment and Instrumentation

Name	Make	Model
Power Resistive Load	ZENITHSUN	DSR3 500W10RJ
Oscilloscope	Tektronix	5 Series – MSO58
DC Power Supply	Electronic Measurements Inc.	-
DSP Control Board	Built by Roderick Gomez	-
Voltage Sensor Board	Built by David Porras	-
Differential Voltage Probes	Tektronix	THDP0100
Current Meter	IDEAL	61-747
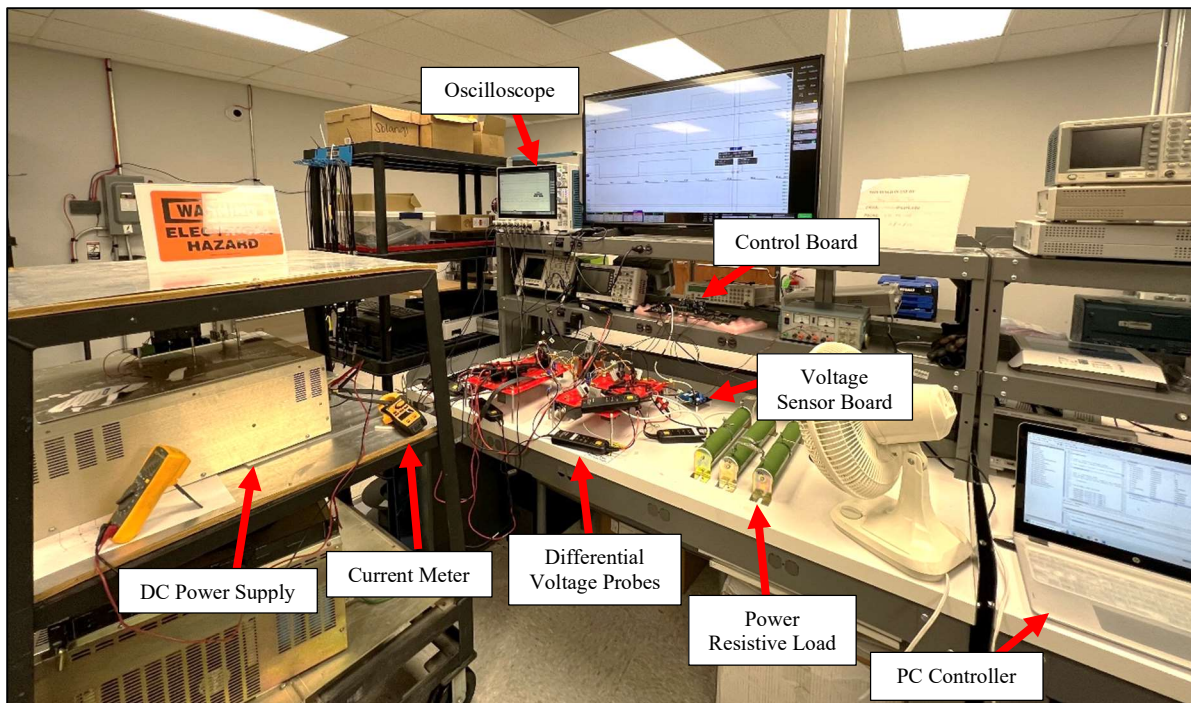
Fig. 4.1: Test equipment setup.
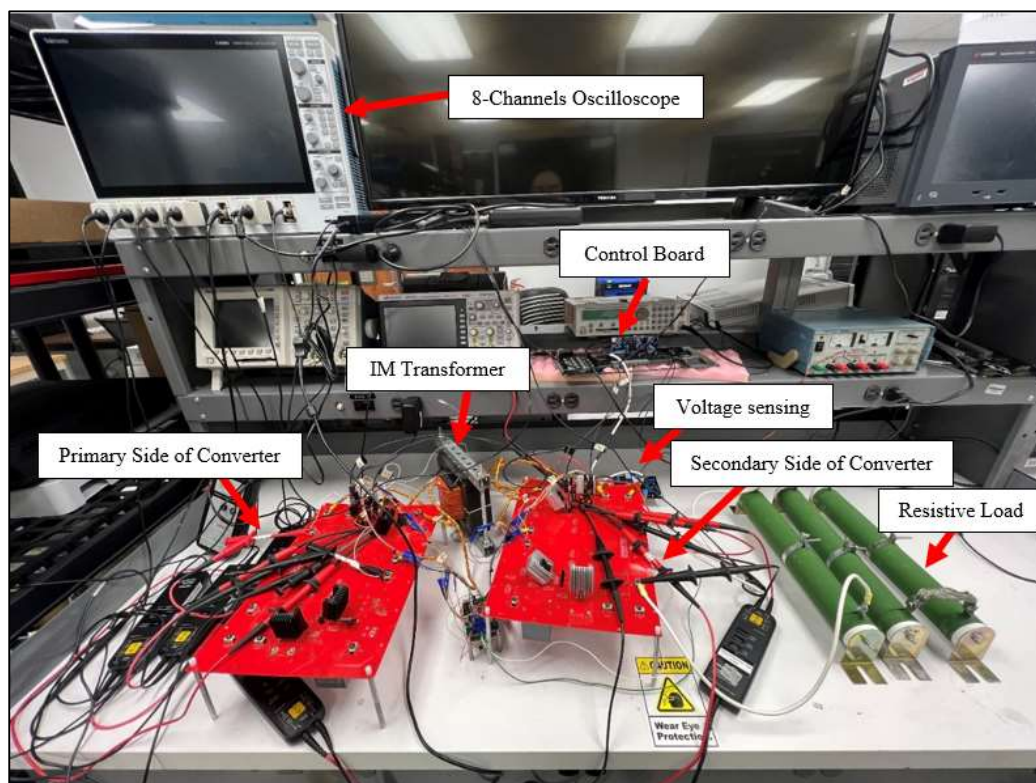
Fig. 4.2: Implemented 1.5-kW prototype.

After designing the converter in Chapter 3 and procuring all the components, the Printed Circuit Boards (PCBs) were populated and each component tested to validate its functioning. At the same time, the IM structure was built. Then, connections were made between the terminals of the IM structure and the PCB. A DC power supply was used to provide the input voltage of 300 V_{dc}.

Furthermore, the gate drivers were connected from the PCB to its source board, which was connected to the voltage sensor board. A voltage supply provided the 12 V for the voltage sensors. The DSP control board designed by doctoral student Roderick Gomez provided the optical PWM channels that were connected to the gate drivers and the analog input channel for the voltage sensors. A TMS320F28379D control card attached to the DSP control board was used for the controller implementation and was connected to the PC controller using Code Composer Studio version 10.2.0. All the desired signals were obtained using differential voltage probes and dc current meters and all were connected to an 8-channels oscilloscope. Three resistors rated 10 Ω at 500 W were connected in series to make a total resistance of 30 Ω rated at 1.5 kW; that is, the resistive load connected to the output of the converter.

4.3   Prototype Implementation and Testing

4.3.1   Controller subsystem

It is necessary to develop and implement various control algorithms in a microcontroller or a DSP in order to operate the isolated Ćuk-based dc-dc converter prototype. A DSP card, along with the measuring circuits and protections, is used to implement the control stage. Executing control algorithms and carrying out other functions related to security and communication with a PC fall under the scope of the TMS320F28379D DSP control card. Short-circuiting protection for the converter's module, which involves the gate driver circuits, is also

considered [1]. The low-cost commercial integrated circuit (IC) IXDN609SICT-ND from IXYS

Integrated Circuits Division is used to opto-isolate the gate drivers utilized in this design. It

offers protection against desaturation, undervoltage, overvoltage, and the potential to generate an

open-collector fault signal that might be applied to trigger a controlled shutdown of the converter

in the event of a failure [1].

Fig. 4.3 (a) illustrates the gate driver of the 1.7-kV discrete SiC MOSFETs designed by

doctoral student Fei Diao, and (b) shows the DSP control card from Texas Instruments. Figs. 4.4

and 4.5 presents the PCB designs made by doctoral student David Porras. The author of this

thesis built and tested each of the components in the prototype. Overall, the design of various

components of the prototype was a team effort from the University of Arkansas (UA) research

group.
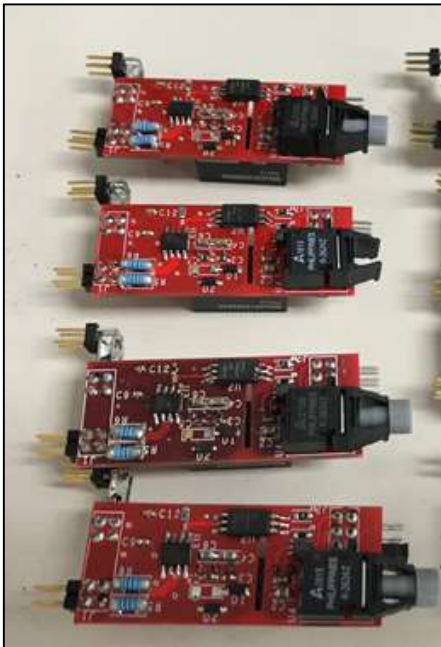
(a)   (b)

Fig. 4.3: (a) Gate driver of the 1.7-kV discrete SiC MOSFETs, and (b) DSP control card [2].
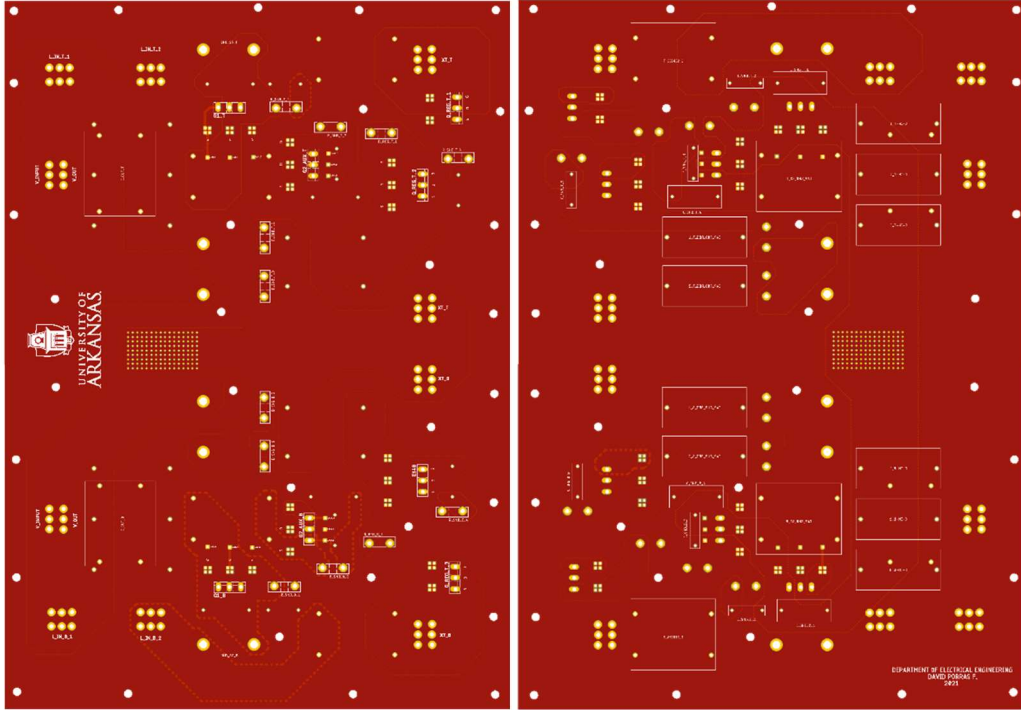
(a)   (b)

Fig. 4.4: Power stage for the isolated bidirectional Ćuk dc-dc converter:
(a) Primary, and (b) Secondary sides.
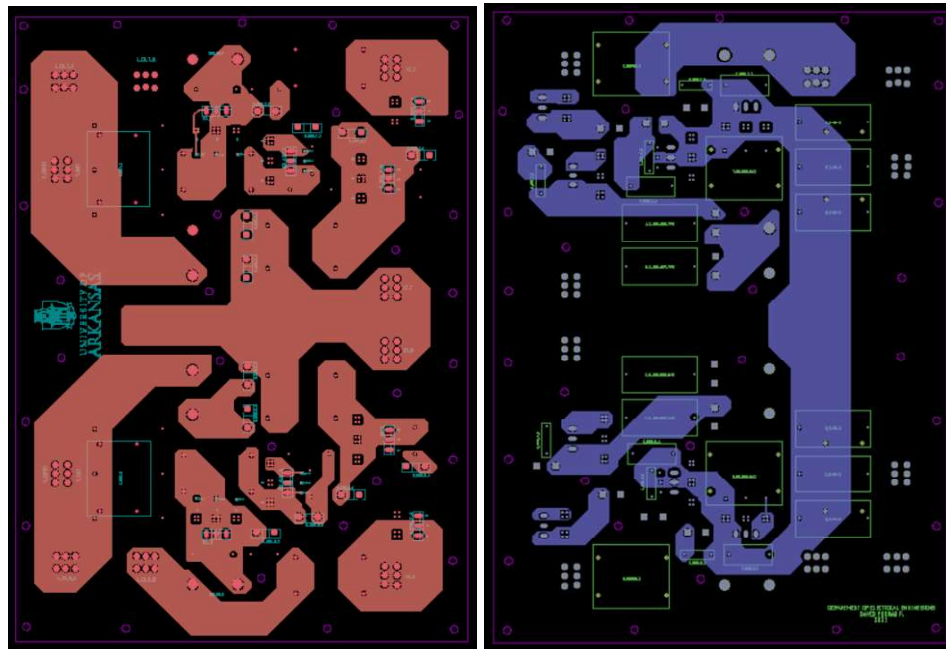
(a)   (b)

Fig. 4.5: Power stage Gerber view: (a) Top, and (b) Bottom layers.

4.3.2 Testing plan

The assembled 1.5-kW prototype was operated at different voltage and power levels to ensure correct and normal operation under different conditions.

The first test is a low input voltage (200 V), low output power (672 W) designed to evaluate the basic operation of the system and its connections to the source and load. As determined in Chapter 3, the duty cycle D is set to 0.43 to achieve 213 V at the output.

The operation sequence should be as follows: set load (R value) to 30 Ω → enable the PWM signals (controller active verification) → increase the input dc voltage in 20 V increments from 0 V → continue increasing the dc voltage until 200 V is reached. After the relevant data are captured, the operation sequence should be: decrease the input voltage to 0 V in decrements of 20 V→ disable the PWM signals.

Table 4.2 shows the operational conditions of the converter: V_{in} and V_{out} are the dc input and output voltages, respectively, P_{out} is the output power, and I_{in} and I_{out} are the input and output currents, respectively. Additional attention is placed on the voltage across the switching devices during the test to ensure the active-clamp circuit limits the voltage stress and ZVS turn-ON is enabled.

Table 4.2: Operational conditions for P_{out} = 672 W and V_{in} = 200 V_{dc}

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Rload (Ω)	Pout (W)
200	3.7	142	4.7	30	672

Fig. 4.6 illustrates the operation of the main switches S_{P1} and S_{S1}. The top waveforms are the drain-to source and gate to-source voltages of main switch S_{P1} combined, the second waveforms are the drain-to source and gate to-source voltages of main switch S_{S1} combined, the third waveform is the input voltage, the fourth waveform is the output voltage and the bottom

Fig. 4.6: ZVS turn-ON of the main devices S_{P1} (top), S_{S1} (second), input voltage (third), output voltage (fourth), and output current (bottom) at $V_{in} = 200$ V.

waveform is the output current. The output voltage is around 142 V when the input voltage is around 200 V.

ZVS turn-ON occurs because the switch voltage is 0 V when the switch current becomes positive. The maximum voltages of S_{P1} and S_{S1} are 334 V and 337.3 V, respectively; the mean values for the input and output voltages are 200.9 V and 142.1 V, respectively; and the mean output current is 4.72 A.

Once the basic operation of the system at low voltage is verified, the goal of the second test is to check that the converter can work at the rated power and voltage of 1.5 kW and 300 V, respectively. The output voltage is given by the duty cycle D of 0.43 calculated in Chapter 3. The operational sequence should be the same one as that of the first test. The operational conditions of the converter are presented in Table 4.3.

Table 4.3: Operational conditions for P_{out} =1.5 kW and V_{in} = 300 V_{dc}

Vin (V)	Iin (A)	Vout (V)	Iout (A)	Rload (Ω)	Pout (kW)
300	5.4	213	7.1	30	1.5

Fig. 4.7 illustrates the operation of the main switches S_{P1} and S_{S1} where the output

voltage is around 213 V for an input voltage of around 300 V corresponding to gain G of 0.71.

The top waveforms are the drain-to source and gate to-source voltages of main switch

S_{P1} combined, the second waveforms are the drain-to source and gate to-source voltages of main

switch S_{S1} combined, the third waveform is the input voltage, the fourth waveform is the output

voltage and the bottom waveform is the output current.

The maximum voltages of S_{P1} and S_{S1} are 494.8 V and 498.7 V, respectively; the mean

values for the input and output voltages are 300.8 V and 214.3 V, respectively; and the mean

output current is 7.10 A. These values agree with those that are theoretically obtained.

The second set of waveforms shows that the main switch S_{S1} operates at ZVS at turn-ON.

However, this is not the case for main switch S_{P1}. Approximately 6 V is present across the gate

voltage of main switch S_{P1} as shown in Fig. 4.8, so ZVS at turn-ON is not ideal. The voltage

$V_{ds,P1}$ is at around 250 V when $V_{gs,P1}$ is around 6 V and $i_1(t)$ is around 5.8 A. However, this is not

large enough to affect the overall system. This is attributed, in part, to the gain of 0.71 being

used, which causes the relatively small equivalent inductor, L_{eq}, to discharge faster than it

should. Due to the restricted amount of power that is delivered by the load, the gain is set to 0.71

because it satisfies the voltage requirements. Thus, increasing the t_{db} of S_{P1} could be a way of

assuring ZVS of main switch S_{P1} and solving this issue, but the fall and rise edges of the PWMs

are linked; if the fall time is increased, then the rise time is also, and the other switches may start

losing ZVS turn-ON. As a result, trade-offs between parameters should be considered to obtain

the best design.

Fig. 4.7: ZVS turn-ON of the main devices S_{P1} (top), S_{S1} (second), input voltage (third), output voltage (fourth), and output current (bottom) at V_{in} = 300 V and G = 0.71.
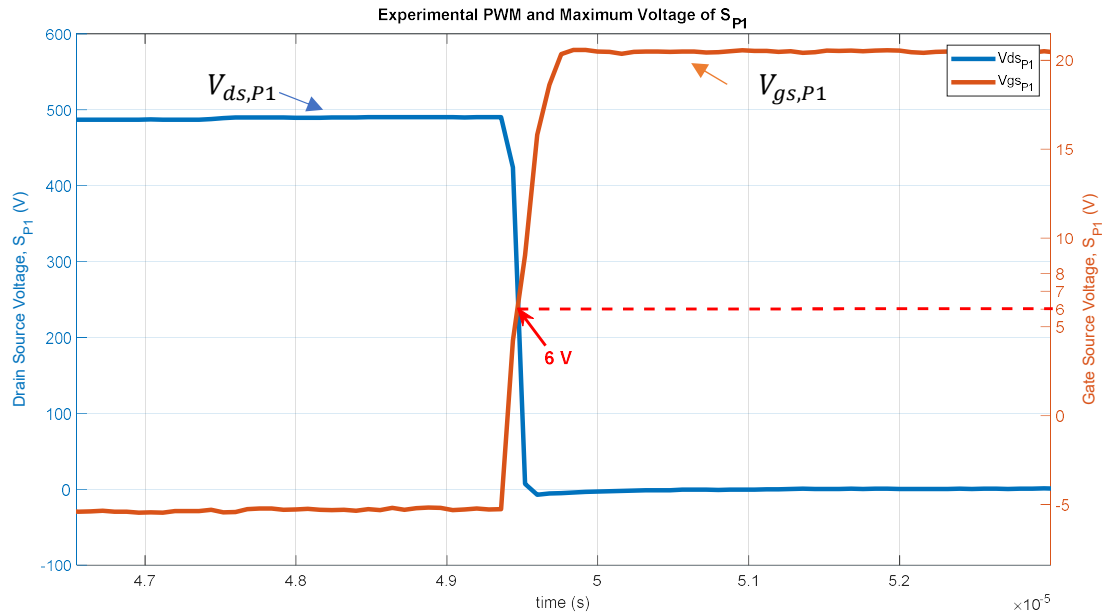
Fig. 4.8: Zoomed-in view of the experimental voltages $V_{ds,P1}$ (left) and $V_{gs,P1}$ (right).

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The second test at rated power is repeated to obtain measurements for the auxiliary switches S_{P2} and S_{S2}, and main switches S_{P1} and S_{S1} to ensure all devices are operating under soft-switching when the gate signal is turned ON. In Figs. 4.9 to 4.12, the ZVS operation of each active switch in the built prototype at rated power is shown and outlined by dashed lines.

When the drain-to-source voltage, V_{ds}, drops to 0 V prior to the application of the gate-to-source voltage, V_{ds}, the switches will experience ZVS turn-ON.

Channels 1, 3, and 5 display the maximum voltage measurements of the drain-to-source switches that are being tested. Channels 2, 4, and 6 are used for the gate-to-source voltages and channels 7 and 8 display the mean input and output voltages, respectively.

Fig. 4.9 shows the gate-to-source voltages as well as the drain-to-source voltages across switches S_{P1}, S_{P2}, and S_{S1}. Both voltages are combined together for each switch to observe if the ZVS turn-ON of the gate signal is accomplished. The top waveforms are the drain-to source and gate to-source voltages of switch S_{P1} combined, the second waveforms are the drain-to source and gate to-source voltages of switch S_{P2} combined, the third waveforms are the drain-to source and gate to-source voltages of switch S_{S1} combined, and the bottom waveforms are the input and output voltages. The maximum voltages of S_{P1}, S_{P2}, and S_{S1} are 500.3 V, 488.5 V, and 511.8 V, respectively, and the mean values for the input and output voltages are 300.4 V and 213.4 V, respectively. These values agree fairly well with theoretical values.

Fig. 4.10 presents the gate-to-source voltages as well as the drain-to-source voltages across switches S_{P1}, S_{S1}, and S_{S2}. The top waveforms are the drain-to source and gate to-source voltages of switch S_{P1} combined, the second waveforms are the drain-to source and gate to-source voltages of switch S_{S1} combined, the third waveforms are the drain-to source and gate to-source voltages of switch S_{S2} combined, and the bottom waveforms are the input and output

voltages. The maximum voltages of S_{P1}, S_{S1}, and S_{S2} are 501.3 V, 513.5 V, and 486.6 V, respectively, and the mean values for the input and output voltages are 300.4 V and 214 V, respectively. Once again, these values agree fairly well with theoretical values.

Fig. 4.11 illustrates the gate-to-source voltages as well as the drain-to-source voltages across switches S_{P2}, S_{S1}, and S_{S2}. The top waveforms are the drain-to source and gate to-source voltages of switch S_{P2} combined, the second waveforms are the drain-to source and gate to-source voltages of switch S_{S1} combined, the third waveforms are the drain-to source and gate to-source voltages of switch S_{S2} combined, and the bottom waveforms are the input and output voltages. The maximum voltages of S_{P2}, S_{S1}, and S_{S2} are 499 V, 513.3 V, and 487.1 V, respectively, and the mean values for the input and output voltages are 300.8 V and 214.3 V, respectively.

Fig. 4.12 displays the gate-to-source voltages as well as the drain-to-source voltages across switches S_{P1}, S_{P2}, and S_{S2}. The top waveforms are the drain-to source and gate to-source voltages of switch S_{P1} combined, the second waveforms are the drain-to source and gate to-source voltages of switch S_{P2} combined, the third waveforms are the drain-to source and gate to-source voltages of switch S_{S2} combined, and the bottom waveforms are the input and output voltages. The maximum voltages of S_{P1}, S_{P2}, and S_{S2} are 507.8 V, 499 V, and 487.6 V, respectively, and the mean values for the input and output voltages are 300.8 V and 214.3 V, respectively.

In general, ZVS turn-ON is accomplished for all switches except S_{P1} which operates under quasi- ZVS. This could be related to (a) a synchronization between switch S_{P1} and its auxiliary switch S_{P2} which is responsible for reducing the current through S_{P1} to zero, and (b) the quantization error in the DSP since 32-bit is used for the measurements brought inside the DSP.
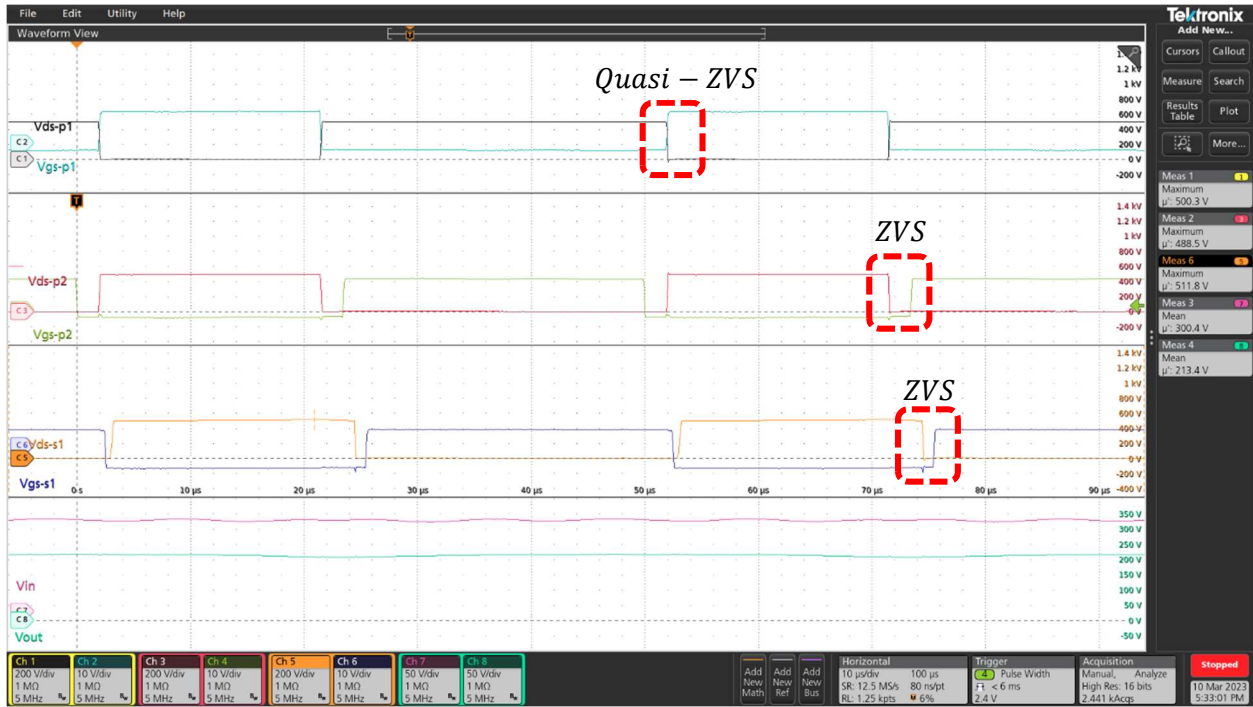
Fig. 4.9: ZVS turn-ON of devices S_{P1} (top), S_{P2} (second), S_{S1} (third), and input and output voltages (bottom) at rated power.
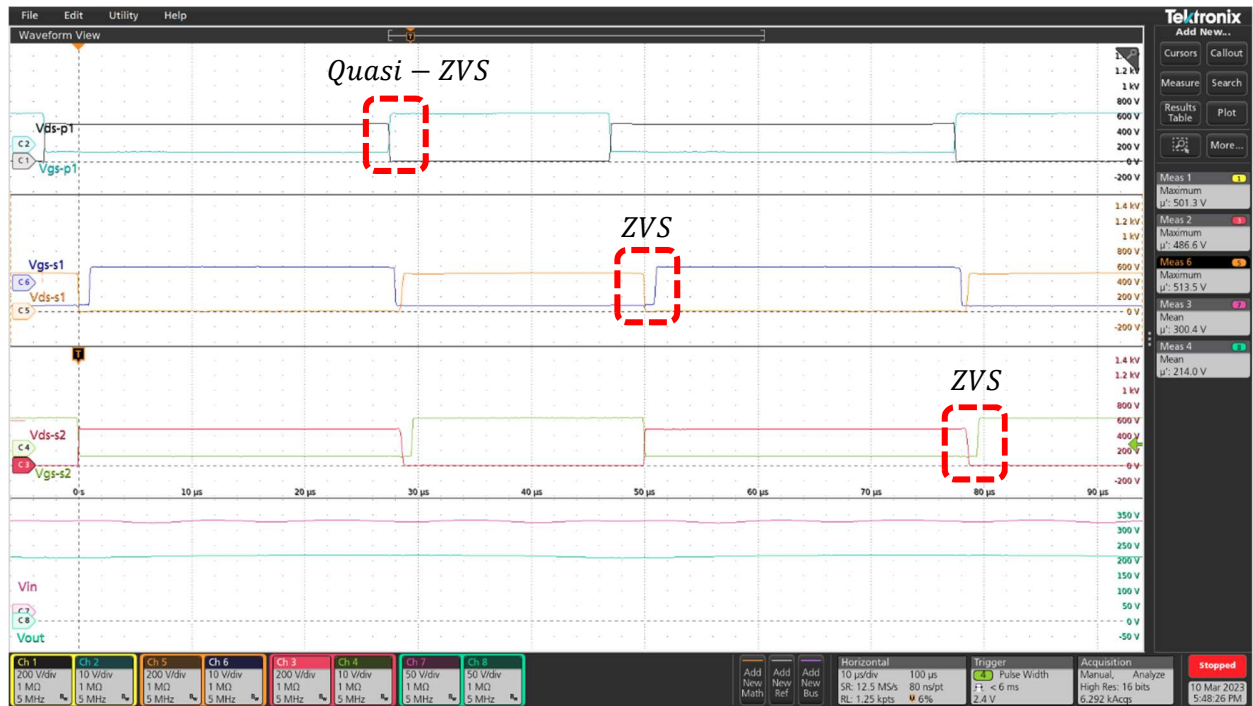
Fig. 4.10: ZVS turn-ON of devices S_{P1} (top), S_{S1} (second), S_{S2} (third), and input and output voltages (bottom) at rated power.
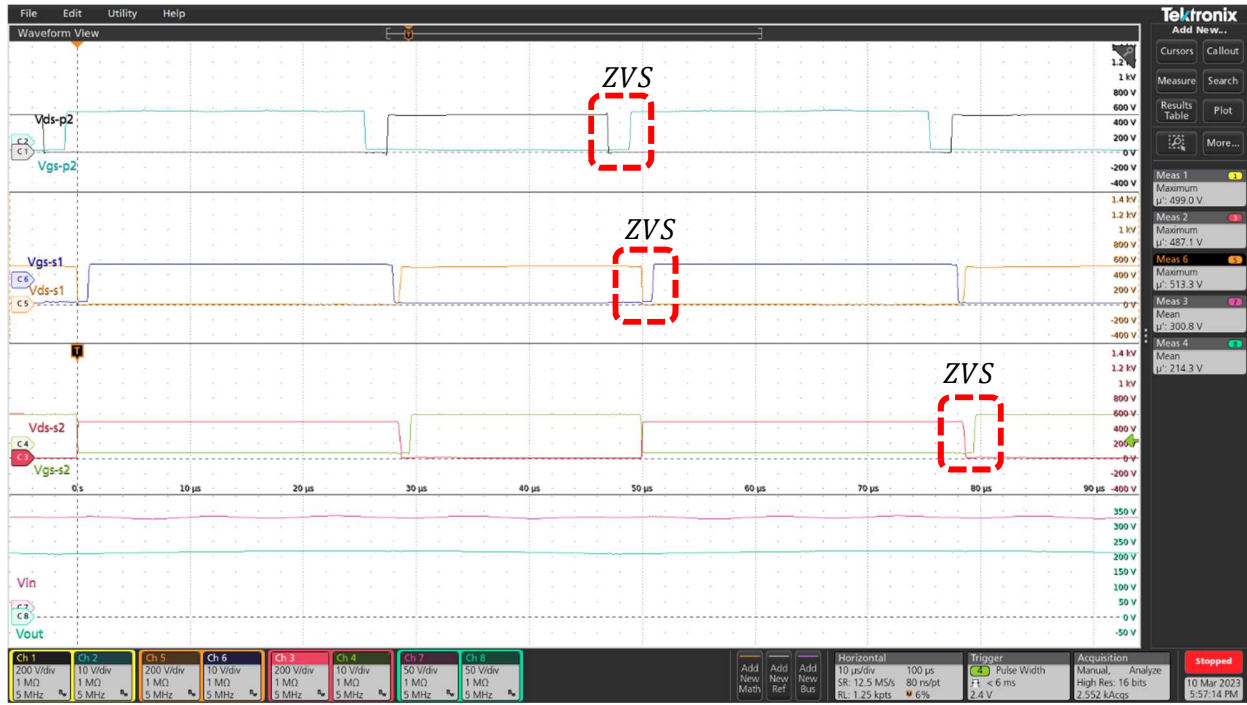
Fig. 4.11: ZVS turn-ON of devices S_{P2} (top), S_{S1} (second), S_{S2} (third), and input and output voltages (bottom) at rated power.
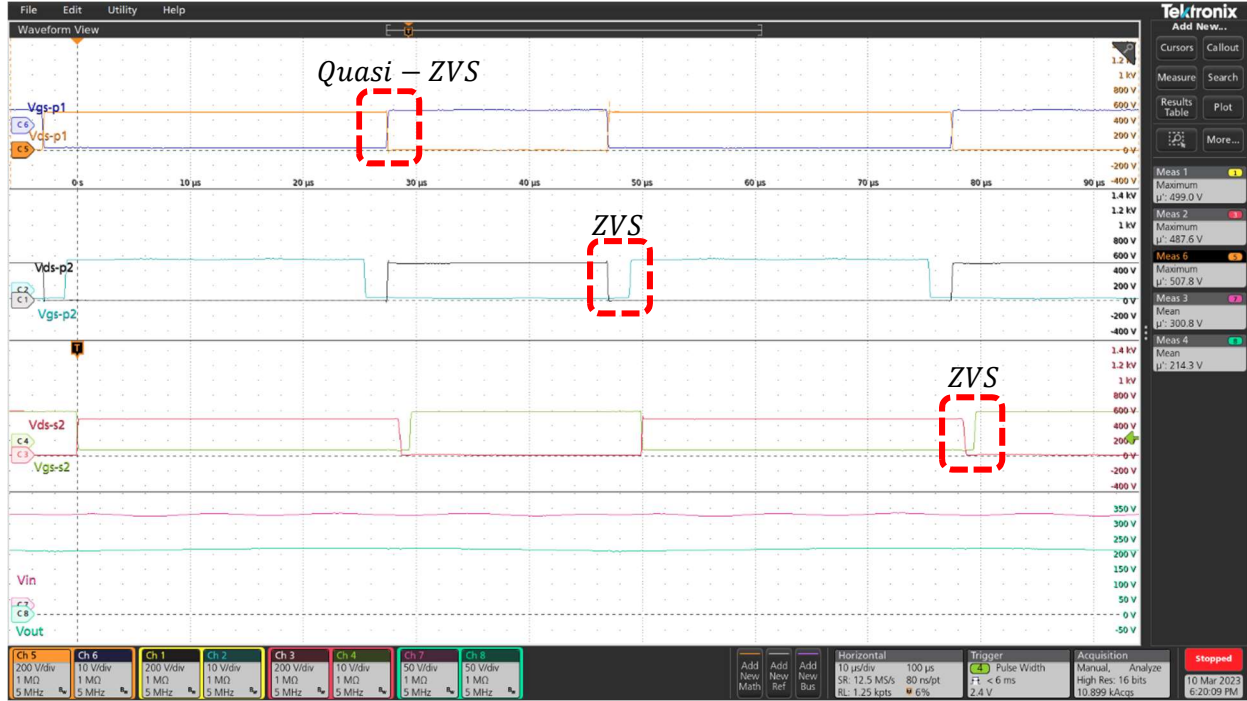
Fig. 4.12: ZVS turn-ON of devices S_{P1} (top), S_{P2} (second), S_{S2} (third), and input and output voltages (bottom) at rated power.

Table 4.4 presents the power efficiency of the system measured at the two tests.

Table 4.4: Experimental Power Efficiency

Measurements	Test 1	Test 2
Vin (V)	200.9	300.8
Iin (A)	3.7	5.4
Vout (V)	142.1	214.3
Iout (A)	4.7	7.1
Efficiency (%)	89.8	93.7

The efficiency of the system increases when the input voltage increases; Test 1 is about 45 % of rated power and Test 2 is approximately at rated power of 1.5 kW. It is well known that the efficiency decreases from this peak (that does not normally occur at rated power) towards lower power and rated power.

4.4 Loss Analysis of Theoretical, Simulation, and Experimental Results

4.4.1 Theoretical losses

The theoretical power losses in a MOSFET can be divided into two key components, conduction and switching losses, which are addressed below.

4.4.1.1 Conduction losses

Power is dissipated when current flows through the resistive component of the switch. Due to parasitic resistances, these losses are a direct function of the converter's duty cycle $D = d_1$ and are conveniently represented as [3]:

$$P_{cond} = I^2_{rms} R_{on} \tag{4.1}$$

where I_{rms} is the rms value of the MOSFET on-state current and R_{on} is the on-state resistance. The conduction loss for the case of a MOSFET utilized in a converter is given by:

$$P_{cond} = (\sqrt{D} \cdot I_o)^2 R_{on} \tag{4.2}$$

where D is the duty cycle in continuous conduction mode, I_o is the output current, and R_{on} is the on-state resistance.

4.4.1.2 Switching losses

Switching losses result from the switch intrinsic capacitor's storing and releasing energy during the turn-ON and OFF transitions. They are proportional to the switching frequency and the value of the parasitic capacitance. The following equation represents the switching losses:

$$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw} \tag{4.3}$$

where E_{on} and E_{off} is the turn-ON and turn-OFF energy losses in the power MOSFET, respectively, and the f_{sw} is the switching frequency. E_{on} is neglected in the calculation because of ZVS turn-ON across the switches.

In addition, there are other losses in the system to the MOSFET losses.

4.4.1.3 Magnetic losses

The total losses of the high-frequency transformer (HFT) are core and copper losses given respectively by:

$$P_{fe} = V_{fe} k_i f_{sw}{}^\alpha B_{max}{}^\beta \tag{4.4}$$

$$P_{cu} = \frac{\rho_{cu} N_p}{A_{litz}} \left[\frac{(l_{p1} + l_{p2})}{S_p} I_p{}^2 + \frac{l_s}{n S_s} I_s{}^2 \right] \tag{4.5}$$

where V_{fe} is the core volume, k_i is the Improved General Steinmetz Equation (IGSE) constant for a square wave, f_{sw} is the switching frequency, α and β are the core Steinmetz coefficients, B_{max} is the peak value of the triangular flux density, ρ_{cu} is the copper resistivity, N_p is the

primary turns, A_{litz} is the is the area of the Litz wire, l_{p1} and l_{p2} are the mean length per turn of

the primary and secondary windings, S_p and S_s are the primary and secondary numbers of

strands, I_p and I_s are the rms values of i_p and i_s, respectively, and n is the turns ratio.

The filter inductor losses are given by:

$$P_{fe} = V_{fe} k_i f_{sw}{}^{\alpha} B_{max}{}^{\beta} \tag{4.6}$$

$$P_{cu} = \frac{\rho_{cu} N}{A_{litz}} \left[\frac{(l_{p1} + l_{p2})}{S} I_{rms}{}^2 \right] \tag{4.7}$$

The core losses calculation are extracted from the IGSE, and the copper losses calculation

consider the selected Litz wire.

Using the datasheet of the 1.7-kV C2M0045170D SiC power MOSFET selected and

Application Note by Infineon [4], the losses per device for the worst-case scenario of a $T_j =$

150 °C are as follows:

$P_{cond} = (\sqrt{D} \cdot I_o)^2 R_{on} = 0.43 \cdot 7.1^2 \cdot 72 \cdot 10^3 = 1.56$ W per device.

$P_{sw} = (E_{on} + E_{off}) \cdot f_{sw} = E_{off} \cdot f_{sw} \cdot \frac{V_{dc}}{V_d} \cdot \frac{I_{dc}}{I_d} = 1.1 \cdot 10^{-3} \cdot 20 \cdot 10^3 \cdot \frac{51}{1200} \cdot \frac{14.6}{50} =$

2.75 W per device.

$P_{T,MOSFET} = P_{cond} + P_{sw} = 4\ (1.56 + 2.75) = 17.24\ W.$

The total power losses, P_T, across the used four power MOSFETs are 17.24 W. The R_{on}

and E_{off} to calculate the conduction and switching losses are taken from the MOSFET

datasheet.

The magnetic losses are the following:

The HFT total losses for a 300 V_{dc} excitation and 7.45 Arms are $P_{T,HFT} = 19.21\ W$.

The inductor total losses for input current of 5.17 A_{peak} and 3.66 A_{rms} and output current

of 7.07 A_{peak} and 5 A_{rms} are $P_{T,L} = 36.1\ W$.

The total magnetic and MOSFET losses for the system are approximately 72.55 W given a theoretical efficiency at 1.5-kW rated power of 95.4 %. Fig. 4.13 displays the projected loss distribution of the 1.5-kW converter.

4.4.2   Performance analysis

Table 4.5 presents a comparison of the power loss and efficiency for the theoretical, simulation, and experimental results.

Table 4.5: Comparison of Power Loss and Efficiency

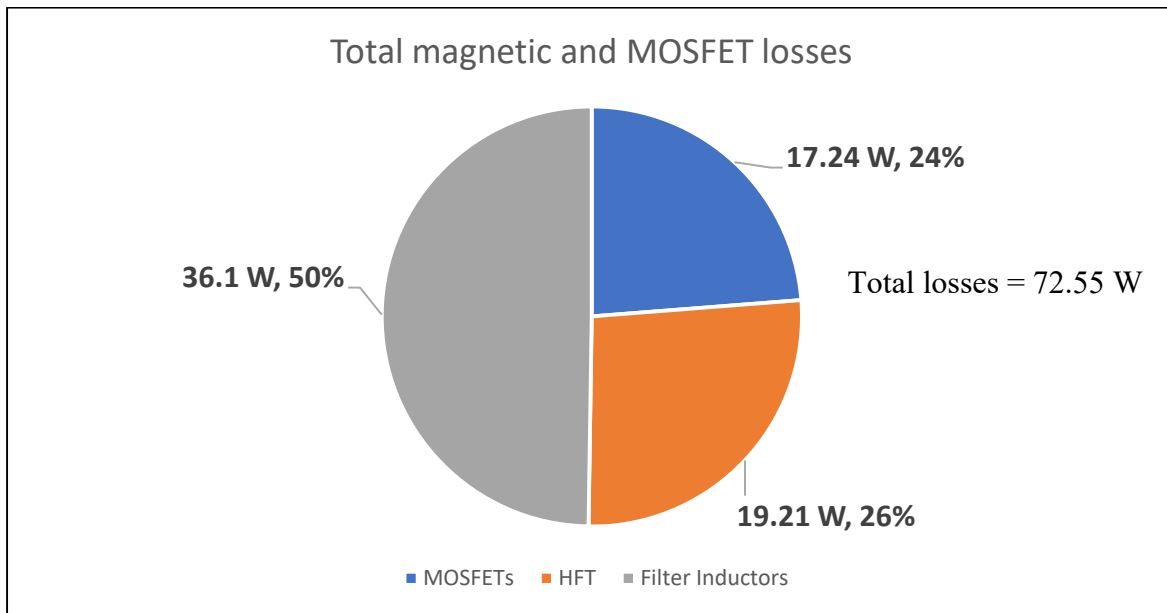| Measurements	Theoretical	Simulation	Experimental
Pin (W)	1572.55	1638	1624.32
Pout (W)	1500	1511.59	1521.53
Power loss (W)	72.55	126.41	102.79
Efficiency (%)	95.4	92.3	93.7

Fig. 4.13: Theoretical losses of the system.

The theoretical data using the datasheets of the components result in less power losses (72.55 W) given a better efficiency (95.4 %) than the power losses in the simulation (126.41 W) and experimental (102.79 W) data as expected since this approach typical values from the datasheets.

Mathematics and knowledge provide the foundation of the theoretical analysis. The values of the components are gathered from their datasheet, where linear behavior is commonly assumed. As a result, the theoretical efficiency typically tends to be higher than the experimental efficiency. Comparatively, experimental efficiency is based on experiments of a built prototype where there may be additional sources of error (e.g., actual values of the components) that cause the system to have more losses. Results from experiments accurately reflect the behavior of the system being tested when specific measuring errors are accounted for. Usually, simulations use the theoretical model of a system to simulate the behavior of that system. However, the simulation efficiency was close enough to the experimental one due to the component values utilized in the circuit model being similar to the actual values.

4.5   Concluding Remarks

In Chapter 4, the setup of the prototype was presented with all the test equipment used for testing. It also presented the controller implementation and testing plan to obtain the experimental results to verify the operation of the Ćuk converter through measurable data that was collected through various testing at the ENRC laboratory. A comparison of the results from the theoretical, simulation, and experimental analyses was done to validate the three stages of any design.

Chapter 5 will present the conclusions and accomplishments of the work done throughout this thesis and some recommendations for future work to improve the quality of the system

presented.

4.6   References

[1]   G. Oggier, D. Simatupang, R. Gomez, and J. Balda, "Next-Generation Modular Flexible Low-Cost SiC-Based High-Frequency-Link Transformer," University of Arkansas, Fayetteville, Arkansas, Jan. 10, 2020.

[2]   Texas Instruments, "Delfino™ TMS320F28379D controlCARD R1.3," User's Guide datasheet, Mar. 2017 [Revised Jun. 2022].

[3]   Narendra Mehta, "GaN FET module performance advantage over silicon". In: Application Note, Texas Instruments (2015).

[4]   Dušan Graovac, Marco Pürschel, and Andreas Kiep, "MOSFET Power Losses Calculation Using the DataSheet Parameters," Infineon, Application Note, v.1.1, Jul 2006.

CHAPTER 5

CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

5.1   Conclusions

This thesis presented an analysis of an isolated bidirectional Ćuk dc-dc converter which has certain advantages over other topologies due to the numbers of active and passive components, and almost ripple-free input and output currents.

The main objective of this thesis was accomplished through the following:

- A theoretical analysis of the converter operation.

- An analysis through simulations using MATLAB/Simulink$^{\text{TM}}$.

- An evaluation of measurements obtained from a 1.5-kW prototype at the ENRC laboratory.

The theoretical background is significant when analyzing any system. Hence, Chapter 2 addressed the theoretical understanding of the isolated bidirectional Ćuk dc-dc converter to comprehend the converter operation. Analyzing the operation of the Ćuk converter enabled understanding that there are three control parameters used as the modulation technique. These are the duty cycle of S_{P1}, d_1; duty cycle of S_{S1}, d_2; and the phase-shift ratio, $\Delta_\emptyset$. Following the ideas in [1] and [2], these three parameters were determined to operate the system as per Fig. 2.25.

The knowledge gained in Chapter 2 was validated through simulations in Chapter 3 verifying that the active-clamp effectively achieves ZVS turn-ON of the switches.

Finally, the goal of the 1.5-kW prototype with an input voltage of 300 V_{dc} accomplishing an output voltage of 213 V_{dc} was to demonstrate the operation of the Ćuk converter illustrated in Chapter 3. The experimental results showed the ZVS turn-ON capability of all the active

switches. These results were found to be in consensus with the theoretical analysis and simulation results. In addition, loss and efficiency performance analyses were carried out at the system level. The largest losses were in the simulations where 126.41 W is lost due to the passive and active components' losses in the system.

5.2   Recommendations for Future Work

The recommendations for potential future work are the following:

- Further testing with higher input power can be done to raise the overall efficiency of the converter. A power resistive load with higher power rating can be replaced at the output to increase the output power of the system.

- The design of the PCB could be improved to avoid unnecessary vias that are not being used, keeping traces short and direct.

- The cores for the IM could be selected to be another type of core material for better edging; and therefore, less core losses.

- The control algorithm developed for the prototype should be implemented and tested for better accuracy of deadband times to improve the desired phase-shift.

- Equivalent control algorithm for a closed-loop configuration can be investigated to provide more accurate monitoring and regulation of the output.

5.3   References

[1]   S. Gupta and S. K. Mazumder, "A Novel Modulation Scheme for Isolated PWM Active-Clamp Ćuk DC/DC Converter," *IEEE Trans. Power Electron.*, vol. 37, no. 12, pp. 14966-14980, Dec. 2022, doi: 10.1109/TPEL.2022.3189672.

[2]   S. Gupta and S. K. Mazumder, "Analysis of Resonant PWM Active-clamp Ćuk DC/DC Converter," *IEEE Trans. Power Electron.*, APEC 2023, doi: 978-1-6654-7539-6/23/$31.00.

MATLAB Code

```matlab
%% DC-DC Isolated Bi-directional Cuk converter parameters
% Simulink file: DC_DC_cuk.slx

clear
format shortEng
clc

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%  Design Parameters
Tsim = 50e-3;         % simulation time
Tstep = 5e-08;        % step size of simulation

Vin= 300;             % input voltage in V
%Vout = 213;
D = 0.43;             % Duty cycle
Vout = Vin*(D/(1-D));   %mean output voltage
Pout = 1.5e3;         % Output power in W
fsw = 20e3;           % switching frequency in Hz
Tsw = 1/fsw;          % switching period in s
tr = 1;               % transformer ratio
f_g = 60;             % grid frequency
w = 2*pi*f_g;         %angular frequency
delay = 2.8e-6;

Vc_rpp1 = 0.017;        % maximum voltage ripple on series capacitors Ca1
Vc_rpp2 = 0.024;        % maximum voltage ripple on series capacitors Cb1
Vout_rpp = 0.0032;      % maximum output voltage ripple %

Vc_rp1 = Vin*Vc_rpp1;         % voltage ripple on series capacitors Ca1
Vc_rp2 = Vout*Vc_rpp2;         % voltage ripple on series capacitors Cb1
Vout_rp = Vout*Vout_rpp;            % output voltage ripple

% Component values
C1 = 3e-6;            % input capacitor in F
C2 = C1;              % output capacitor in F
L1 = 620e-6;          % input inductor in H
L2 = L1;              % output inductor in H
Lr1 = 31e-6;          % primary series inductor in H
Lr2 = Lr1;            % secondary series inductor in H
CT1 = 7.5e-6;         % primary soft switching or aux capacitor in F
CT2 = 2.2e-6;         % secondary soft switching or aux capacitor in F
Leq = 69e-6;          % sum of Lr1+Lr2+Llk1 in H
Ca1 = 15e-6;           % primary blocking or series capacitor in F
Cb1 = Ca1;            % secondary blocking or series capacitor in F
Rload = 30;           % resistive load in ohms

%switches parameters
ton_fed_P1 = 2e-6;        %on delay
Rds_on1 = 40e-3;     %Rds on mosfet
```

```matlab
Rds_on2 = Rds_on1;
Rds_on3 = Rds_on1;
Rds_on4 = Rds_on1;

%Coupling inductors
Lp = L1;
Ls = Lp;
Llk = 3.5e-6; %leakage inductance of the XT

R1 = 1e-3;   %winding resistance


%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
% 3D Plot showing power transfer and mean square series inductor current per Watt
dependency on duty cycles d1 and d2 for
% specific voltages with gain =1, Leq = 66 uH and Phase shift ratio of 0.05

phase = 0.09;
d1 = 0.3:0.01:0.7;
d2 = 1-d1;
%d1' == 1-d1;      %auxiliary primary duty
%d2' == 1-d2;      %auxiliary secondary duty
n = length(d1);
m = length(d2);
for j= 1:n
    for k = 1:m
        Pout(j,k) = (((Vin*Vout*Tsw)/(2*Leq))*(2*phase+(d1(j)+d2(k)-1)-
((phase^2)/((1-d1(j))*(1-d2(k))))));     %Output power in W

        a (j,k)= (Vout*(12*Vin*phase^2+Vout))/12;
        b (j,k)= (Vin*((d1(j))^2)*(Vin+4*Vout))/12;
        c (j,k)= (Vin*((1-d2(k))^2)*(4*Vin+Vout))/12;
        d (j,k)= (Vout*(1-d2(k))*(Vout+6*Vin*phase))/6;
        e (j,k)= (Vin*Vout*(phase^3))/(3*(1-d2(k))-3*(d1(j))*(1-d2(k)));
        f (j,k)= (Vin*Vout*(d1(j))*(3*(1-d2(k))-(6*phase)+1))/6;
        I_mean_sq (j,k) = ((Tsw/Leq)^2)*(a(j,k)+b(j,k)+c(j,k)-d(j,k)-e(j,k)-f(j,k));
%currrent mean squared per Watt in A^2/W

    end
end

x = (d1);
y = (d2);
z = (Pout);

figure(1)
clf
s = surf(x,y,z);
hold on

grid on
xlabel('d1');
ylabel('d2');
zlabel('Output Power (W)');
zlim([0, 12000]);
```

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```matlab
title('3D Plot power transfer dependency on duty cycles (d1 and d2)')
colorbar

z = (I_mean_sq)/Pout(j,k);
hold off
figure (2)
clf
s1 = surf(x,y,z);
hold on
contour(x,y,z);
grid on
xlabel('d1');
ylabel('d2');
zlabel('I^2_L_,_R_M_S/W (A^2/W)');
zlim([0, 1.1]);
title('3D Plot mean square series inductor current per Watt dependency on duty cycles
(d1 and d2)')
colorbar
hold off

%%
figure(3)
data = load('300Vin_data.mat');
%i_leq(t) at t0-t1
plot(data.out.t, data.out.iLeq, 'LineWidth',3)
ylim([-12, 12]);
ylabel('Current Equivalent Inductance, i_L_e_q (A)')
grid on
hold on
xlim([0.03776, 0.03782]);
xlabel('time (s)')
title('Current Through L_e_q from t_0- t_1')
%%
figure(4)
data = load('300Vin_data.mat');
%i_2(t1) at t1-t2
plot(data.out.t, data.out.i_2, 'LineWidth',3)
ylim([-5, 20]);
ylabel('Current going out of the switch S_S_1 branch, i_2(t_1) (A)')
grid on
hold on
xlim([0.03776, 0.0378]);
xlabel('time (s)')
title('Current out of Node Voltage v_2(t) from t_1- t_2')
%%
figure(5)
data = load('300Vin_data.mat');
%i_1(t3) at t3-t4
plot(data.out.t, data.out.i_1, 'LineWidth',3)
ylim([-10, 20]);
ylabel('Current going into the switch S_P_1 branch, i_1(t_3) (A)')
grid on
hold on
xlim([0.03776, 0.0378]);
xlabel('time (s)')
```

```matlab
title('Current Flowing into Node Voltage v_1(t) from t_3- t_4')

%%
figure(6)
data = load('300Vin_data.mat');
subplot(3,1,1);
y1 = data.out.i_1;
plot(data.out.t, y1, 'LineWidth',3)
xlim([0.03776, 0.03782]);
ylim([-10, 20]);
grid on
ylabel('i_1 (A)')
legend('i_1 (A)')
title('Currents i_1, i_2, and i_L_e_q vs. time')

subplot(3,1,2);
y2 = data.out.i_2;
plot(data.out.t, y2, 'Color', 'red','LineWidth',3)
xlim([0.03776, 0.03782]);
ylim([-5, 20]);
grid on
ylabel('i_2 (A)')
legend('i_2 (A)')

subplot(3,1,3);
y3 = data.out.iLeq;
plot(data.out.t, y3, 'Color', 'green','LineWidth',3)
xlim([0.03776, 0.03782]);
ylim([-12, 12]);
grid on
xlabel('time (s)')
ylabel('i_L_e_q (A)')
legend('i_L_e_q (A)')

%%
figure(7)
data = load('300Vin_data.mat');
subplot(4,1,1);
y1 = data.out.VDS_P1;
plot(data.out.t, y1, 'LineWidth',3)
xlim([0.03776, 0.03782]);
ylim([-20, 600]);
grid on
ylabel('Vds_P_1 (V)')
legend('Vds_P_1 (V)')
title('Maximum voltages across all switches vs. time')

subplot(4,1,2);
y2 = data.out.VDS_P2;
plot(data.out.t, y2, 'Color', 'red','LineWidth',3)
xlim([0.03776, 0.03782]);
ylim([-20, 600]);
grid on
ylabel('Vsd_P_2 (V)')
legend('Vsd_P_2 (V)')
```

```matlab
subplot(4,1,3);
y3 = data.out.VDS_S1;
plot(data.out.t, y3, 'Color', 'green','LineWidth',3)
xlim([0.03776, 0.03782]);
ylim([-20, 600]);
grid on
ylabel('Vds_S_1 (V)')
legend('Vds_S_1 (V)')

subplot(4,1,4);
y4 = data.out.VDS_S2;
plot(data.out.t, y4, 'Color', 'magenta','LineWidth',3)
xlim([0.03776, 0.03782]);
ylim([-20, 600]);
grid on
ylabel('Vsd_S_2 (V)')
legend('Vsd_S_2 (V)')
xlabel('time (s)')
%%
figure(8)
%VDS_P1 from oscilloscope
CH1 = load('test300v_000_ch1.mat');
yyaxis left
VDS_P1 = CH1.data;
t = CH1.time;
plot(t, VDS_P1, 'LineWidth',3)
ylabel('Drain Source Voltage, S_P_1 (V)')
ylim([-100, 600]);

%VGS_P1 from oscilloscope
CH2 = load('test300v_000_ch2.mat');
yyaxis right
PWM_P1 = CH2.data;
t = CH2.time;
plot(t, PWM_P1, 'LineWidth',3)
yticks([-5 0 5 6 7 8 10 15 20 25]);
ylabel('Gate Source Voltage, S_P_1 (V)')
legend('Vds_P_1' , 'Vgs_P_1')
xlabel('time (s)')
title('Experimental PWM and Maximum Voltage of S_P_1')
grid on
hold on

%%
figure(9)
%VDS_P1 from oscilloscope
CH3 = load('test300v_000_ch3.mat');
yyaxis left
VDS_S1 = CH3.data;
t = CH3.time;
plot(t, VDS_S1, 'LineWidth',3)
%xlim([0.018, 0.01808]);
ylabel('Drain Source Voltage, S_S_1 (V)')
ylim([-100, 600]);
```

```matlab
%VGS_P1 from oscilloscope
CH4 = load('test300v_000_ch4.mat');
yyaxis right
PWM_S1 = CH4.data;
t = CH4.time;
plot(t, PWM_S1, 'LineWidth',3)
yticks([-5 0 5 10 15 20 25]);
ylabel('Gate Source Voltage, S_S_1 (V)')
legend('Vds_S_1' , 'Vgs_S_1')
xlabel('time (s)')
title('Experimental PWM and Maximum Voltage of S_S_1')
grid on
hold on
```