Fabrication of Vertical Silicon Nanowires through Metal Assisted Deposition

Matthew Garett Young
University of Arkansas, Fayetteville

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FABRICATION OF VERTICAL SILICON NANOWIRES THROUGH METAL ASSISTED DEPOSITION
FABRICATION OF VERTICAL SILICON NANOWIRES THROUGH METAL ASSISTED DEPOSITION

A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science in Microelectronics-Photonics

By

Matthew Garett Young
Arkansas Tech University
Bachelor of Science in Electrical Engineering, 2009

May 2012
University of Arkansas
Abstract

Controlled and ordered growth of Si nanowires through a low temperature fabrication method compatible with CMOS processing lines is a highly desirable replacement to future electronic fabrication technologies as well as a candidate for a low cost route to inexpensive photovoltaics. This stems from the fact that traditional CMOS based electronics are hitting physical barriers that are slowing the Moore’s Law trend as well as the demand for an inexpensive solar cell technology that can obtain grid parity. A fractional factorial growth study is presented that compares the growth of Au and Al catalyzed Si nanowires at temperatures ranging from 150 to 400°C. Dense and prolific growth of Si nanowires on <111> and <100> Si substrates as well as glass substrates was obtained using a Au catalyst at temperatures of 400°C. An overview is given that considers all growth experiments and includes TEM analysis of individual Si nanowires grown on Si substrates showing nanowires to be both crystalline and amorphous in nature. Optical transmission data of bulk Si nanowire films on glass substrates showed that the collective optical properties were highly desirable as transmission was minimized over the 300 to 1400 nm wavelength range at different transmission angles. Collectively, a growth platform is presented from which further material study will yield advanced Si nanowire based devices, satisfying a demand by the ITRS and the scientific community at large for electronics that can continue the Moore’s law trend and inexpensive photovoltaics capable of meeting the consumer demand for grid parity.
This thesis is approved for recommendation to the Graduate Council.

Thesis Director:

___________________________________
Dr. Hameed Naseem

Thesis Committee:

___________________________________
Dr. Shui-Qing (Fisher) Yu

___________________________________
Dr. Jiali Li

___________________________________
Prof. Ken Vickers

The following signatories attest that all software used in this thesis was legally licensed for use by Mr. Matthew Garrett Young for research purposes and publication.

___________________________________
Mr. Matthew Garrett Young, Student

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Dedication

I could list a number of individuals to which this thesis is dedicated and maybe that is proper to do, but I feel as though this scientific work should be dedicated to anyone who works to make the world a better place. We all have to live here, so we should do so in harmony.
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Chapter 1: Introduction and Review of Literature

The first chapter of this thesis introduces the reader to the societal problems that silicon nanowires may help to solve. A literature review of the most relevant fabrication methods is given. The structure and layout of the thesis is given as well as the motivation for this research.

1.1 State of Energy Conversion and Integrated Circuits

Two major engineering problems that society is currently faced with is the need for alternative energy sources to power the activities of the human race, and the need for advanced circuitry to further develop technological progress. The backbone of the modern world is constructed of electronic circuitry as it is this circuitry that allows this thesis to be composed, powers the financial transactions and economic trade of the world, enables new technological applications that can aid society in preventing disease and extending life, and ultimately ties us all together so that information can be spread and knowledge can proliferate through time. It is information that is the key to the modern world and it is communication that allows this information to grow. Communication cannot be supported without the development of faster and more powerful electronics. And, to power all of this, society needs abundant amounts of energy, such as that comes from the sun.

A pivotal document that is updated on a bi-annual basis that discusses the state of the electronics industry is that of the International Technology Roadmap for Semiconductors (ITRS) [1]. As of the 2011 issue, the document calls for the implementation of semiconducting nanowires in the long term (2019-2026 timeframe) as alternative to traditional complementary metal oxide semiconductor (CMOS) materials for continued scaling of electronics via Moore’s Law. This is
due to the semi-ballistic transport that semiconductor nanowires have been characterized to have that can sustain drive currents in metal oxide semiconductor field effect transistors (MOSFET) devices [1]. A particular aspect that must be met is the low temperature processing of devices in order to maintain material properties through the fabrication of a packaged device [1]. This is an area that silicon nanowires can actively meet, especially since silicon nanowires can be grown at low temperatures and the majority of the world’s processing lines are based upon Si. An additional area where Si nanowires are thought to become relevant into the future is the application of interconnects in electronic packaging [1]. Again, it is the low temperature processing and electronic properties that are sought-after and that Si nanowires possess for the continued advancement of the areas that are called upon by the ITRS.

Another area of technological process that requires a solution that Si nanowires can provide is that of energy conversion. The radiation that strikes the livable surface of the earth in one day alone could power the daily activities of humans for a year! [2] Significant cost barriers have prohibited the wide spread implementation of photovoltaic devices mainly due to the material cost of the finished device. One way to reduce such a cost is by reducing the amount of material the photovoltaic device utilizes, but without giving up the quantum efficiency that ultimately governs how light is converted to electrical energy. Si nanowires offer an excellent platform from which to do this as they require less material, can be deposited from gas phase (removing wafer dependence) and can be grown on multiple substrate types (including inexpensive plastics and flexible materials) which is another large cost associated with solar cell production. Si nanowire based solar cells also have a built-in anti-reflection scheme that eliminates several
processing steps for simpler fabrication, thus making them an even more attractive candidate over conventional technologies.

To continue to expand human knowledge and drive innovation, new electronic technologies need to be researched to solve problems that face society. Two major problems have been introduced, that of continued scaling in the semiconductor industry and the quest for alternative energy. Si nanowires are an attractive platform for helping to solve both problems and thus continue the pace of information transfer that drives the human element.

This thesis is concerned with exploring the possibility of fabricating Si nanowires as a device platform through a low temperature fabrication method using plasma enhanced chemical vapor deposition (PECVD). The analysis of the fabrication of Si nanowires by PECVD is needed in order to gain control over Si nanowire fabrication for accurate and optimal implementation into working devices. This method is compatible with the low temperature needs sought after by ITRS for maintaining material properties in a packaged device as well as the needs for a low cost solution to current solar energy harvesting applications.

1.2 Fabrication of Silicon Nanowires by PECVD

Silicon nanowires have been synthesized by many different methods including chemical methods, high temperature furnaces, and top down etching. While these methods have been proven to be essential to the study of the underlying physics of silicon nanowires, few methods, if any, have been developed that allow for scalable and technologically compatible fabrication. Here, the history of the use of PECVD to grow silicon nanowires is given, showing relevant
benchmarks in using the process to grow nanowires. It is shown that PECVD is a strong candidate for a low temperature scalable production of silicon nanowires.

The first case of silicon nanowire nucleation via plasma enhanced chemical vapor deposition (PECVD) was performed by Hofmann et. al. in 2003 [3]. This work involved the growth of nanowires at temperatures below 400°C using a Au catalyst and SiH₄ as a source gas on oxide coated Si substrates. Silicon nanowires that were grown were found to have a crystalline core with a 2-nm thick oxide coating and were thin so that confinement was noticed [3]. This work was the seminal paper in proving that silicon nanowires could be grown using a low temperature method such as PECVD. No research was performed on silicon nanowires grown by PECVD until 3 years later when Colli et. al. published a paper comparing properties of silicon nanowires that were grown using different fabrication methods [4]. This work showed that the morphology of nanowires was process dependent, although no conclusions were formed around which method had the most advantages for good quality silicon nanowire growth. PECVD was shown to produce higher quality nanowires than CVD grown wires owing to plasma enhancement, but parasitic deposition of a-Si:H was also noted as a potential barrier to PECVD grown wires. This parasitic deposition is inherent to the PECVD process as uncatalyzed deposition material can actually act to blanket a metal catalyst such that no nanowire growth ever occurs.

The next instance of silicon nanowire growth via PECVD involved the use of low temperature alternative catalysts such as Al and In [5]. The reasoning behind the investigation of alternative metal catalysts rested in the idea that Au catalyst which had been previously investigated in PECVD growth might lead to high trapping densities within Si, rendering the as-grown
nanowires useless for electronic application. Iacopi et. al. showed that In could be used as a low melting point catalyst for growth of silicon nanowires for semiconductor applications, but Al proved to yield little or no results for wire growth [5]. This was attributed to the fact that when a metal such as Al is used, the growth process of the wire is not limited by the amount of gaseous source, but rather is limited by the solid phase diffusion of the gas phase into the solid metal. This places an obstacle in the way of creating a fabrication method that is compatible with the semiconductor industry. Al would be an ideal candidate from which to grow silicon nanowires as it is a p-type dopant in Si and would not introduce significant mid-gap states that would deplete electronic charge.

Another paper that sought to show that a catalyst was not necessary due to plasma enhancement was that of Griffiths et. al. [6]. This paper showed that Ga and In were both viable candidates for silicon nanowire growth, but it was not due to the catalyst aspect of the metals, but rather the low melting temperatures of Ga and In. The plasma acted to dissociate gas molecules before they diffused into a metal particle. As such, the catalyst effect of a metal cracking the gas molecule was not necessary because the plasma took care of this process. This placed some freedom in the PECVD growth process because it broadened the spectrum of metal catalysts that could be used in fabrication. So long as a method is available to produce a liquid phase of a metal on a substrate, then it is likely possible to grow silicon nanowires with that metal particle.

Further work with the fabrication of silicon nanowires via PECVD came from Alet et. al. in 2008, when they successfully grew silicon nanowires after decomposing indium tin oxide (ITO) films into indium droplets using a plasma [7]. The highlight of this work was achieving lower
temperature growth than what had been achieved with prior PECVD fabrication. In was chosen as the choice metal because its melting temperature is 156.6 °C. Previous research showed that liquid catalyst particles were a requirement for silicon nanowire fabrication so the researchers decided In would provide the lowest temperature method through which to synthesize silicon nanowires. The researchers chose to decompose ITO into In droplets because In has a high chemical reactivity at atmospheric conditions. Decomposing an ITO film into In droplets is an in-situ method to creating In under vacuum. A hydrogen plasma was used to first decompose the ITO, and then a silane plasma was used to grow silicon nanowires [7]. In many ways this research was proof that PECVD could be used as a method to generate devices in-situ, as the ITO was used as a transparent conducting oxide even after the silicon nanowires were grown on top of it. More research into the low temperature synthesis of silicon nanowires focused upon Ga as a metal since its melting point is 29.8 °C [8], which coincides with the Si-Ga eutectic temperature. In addition to the possibility of the low growth temperature, Ga is viewed as benign in Si and could be used as a p-type dopant much like Al. This removes the fear of trapping states due to metal contaminants that Au introduces into silicon. Despite seeking the low growth temperature that Ga might achieve, the researchers produced wires at 600 °C [8]. However, interesting growth physics was noted as the nucleation along the length of the wires was obtained due to the migration of Ga during the growth process [8]. Though Ga could prove to be an effective metal to grow silicon nanowires at low temperatures, it remains an expensive metal which makes it a less attractive growth candidate. Another attractive material candidate, Sn, was used as a growth catalyst by Rathi et. al., whereby Sn was evaporated onto a Si substrate and H₂ diluted SiH₄ was used to grow silicon nanowires at temperatures around 300 to 400 °C [9]. The importance of this silicon nanowire growth was that the Sn seem to disappear during growth due
to the H$_2$ plasma, which might lead to metal-free growth of silicon nanowires [9]. Another attempt at In catalyzed silicon nanowires was made by Convertino et. al., however nanowires were obtained at 330 and 500°C [10]. The authors did point out that silicon nanowires grow at a temperature much higher than that of the In-Si eutectic from experimentation [10].

Silicon nanowires have successfully been synthesized using a variety of metal catalysts including Au, Sn, In, and Ga by PECVD. The lowest temperature growth occured with In at 250°C [7]. Silicon nanowires grown using different catalysts showed differences in physical composition including c-Si cores with oxide coatings [4], c-Si cores with twinning in the crystal lattice [7], and a-Si coating a c-Si core [11]. Developing good control over the morphology of wires during growth is a key to the implementation of PECVD as a fabrication method for silicon nanowires which has yet to be achieved within the scientific community.

Silicon nanowire growth through PECVD is a relatively new fabrication method as compared to other methods. It is promising as a bottom up nanoscale fabrication method owing to its possibility to grow nanowires at low temperatures. Low temperature growth would enable inexpensive plastics to be used as a device substrate. A comprehensive study is necessary such that the differences in nanowires grown with different catalysts can be analyzed for the electronic and optical properties of the silicon nanowires.

Using PECVD to grow silicon nanowires is not the only method used to synthesize silicon nanowires. Other fabrication processes have been developed using different tools and this work is briefly surveyed in the next section.
1.3 Other Methods of Fabrication

If one attempts to organize the growth of silicon nanowires by all available methods, one would become quickly overwhelmed. A distinct pattern would be noticed, however, in that methods can generally be divided into two categories. The categories are top down fabrication and bottom up fabrication. An example of bottom up fabrication is the growth using PECVD that was described in Section 1.2, nanowires nucleating from processes that tend to cause the nanowires to grow on a substrate. Top down methods refer to steps that are used to remove some material, as in etching, to sculpt out silicon nanowires from a solid material. A few relevant examples of each of these is given below and advantages to PECVD growth are given.

Top-down methods usually utilize etching to remove substrate material such that a nanowire or nanostructure is left that has been sculpted from the substrate. Standard lithography has been used to pattern a substrate and then deep reactive ion etching (DRIE) was used to form the nanowires [12]. Though this method seemed advantageous because it was simple, DRIE was limited by the size of the patterning in the lithography step. This often resulted in the use of e-beam lithography to pattern a substrate, but e-beam lithography requires a large amount of throughput on the order of days for 1 cm$^2$ sample depending upon dose, beam current, and sample area. Another top down approach uses block-copolymers to act as an etching template for nanorod creation [13]. Block co-polymers are material that form nanoscale voids when mixed in different compositions. These voids in the co-polymer were used as openings through which an etchant attacked the underlying substrate and produced nanorod structures. Though this method could be scaled, it suffered from poor resolution of as-grown wires and wires were produced in random locations. Long vertical wires produced by this method suffer from
throughput issues as longer wires require longer etching time. Yet another method of creating silicon nanowires through a top down approach was that of metal assisted etching where a Si substrate was introduced to a liquid solution that contained metal catalyst salts [14]. This process worked by chemically depositing metals onto the Si substrate followed by the etchant chemical, often HF, selectively etching the areas not covered by the metal particle deposition. This formed arrays of vertically oriented nanowires, but the chemical process was not easily adaptable to large scale manufacturing as the wire properties were sensitive to slight variations in chemical processing. With sophisticated lithography tools, controlled creation of silicon nanowires could achieved through top-down methods. Generally speaking, the etching away of substrate material represents a loss in a fabrication method and as such these processes are not attractive for device creation.

Other bottom up methods exist that had been used to controllably fabricate vertical silicon nanowires. Such methods included CVD, evaporation, molecular beam epitaxy (MBE), and chemical techniques. Chemical vapor deposition is the sister process to PECVD and is identical except that high temperatures are used to crack gaseous molecules for deposition. There is no plasma in the process so the catalytic properties of the metal catalyst used must be sufficient to grow high quality silicon nanowires. Good control over nanowire geometry had been achieved using CVD with diameters ranging from the micrometer scale down to tens of nanometers [15]. The lack of plasma in the process meant that it relied upon only thermal energy and thus much higher temperatures were needed than PECVD. MBE has been used to create high quality single crystalline silicon nanowires at slow growth rates [16]. The wires created were short, only reaching to 200 nm, and the Gibbs-Thomson effect placed a lower limit on the diameter of the
nanostructures, thus preventing thin nanowires with large aspect ratios from being grown. The slow rate of growth in addition to the physical mechanism limiting the growth of the nanowires made MBE an unattractive candidate for scalable growth of silicon nanowires. A method where bulk production of silicon nanowires was achieved was that of evaporation of Si bearing powders such as SiO powder [17]. The nanowires achieved using this method were created by evaporating a powder in one end of a furnace and placing a metal coated substrate at an opposing end. A gaseous flux was used to carry evaporated Si to a heated substrate in a thermal gradient, typically in excess of 1000 °C and a chemical reaction at the substrate surface broke the SiO into Si and SiO₂ providing the metal catalyst with diffusive Si molecules. This method produced long wires, but it was hard to gain control over the wire diameters and the high temperatures made the process limited to specific substrates.

Though other methods of fabricating silicon nanowires exist, PECVD remains a good candidate as it possess most of the advantages of other methods while maintaining few of its own disadvantages, mainly owing to parasitic deposition of a-Si burying catalyst particles. The research involved in the fabrication of silicon nanowires is still relatively new and other methods may yet to be developed. PECVD was chosen as the concentration in this thesis because it is viewed as a low temperature method that has the ability to gain excellent control of nanowire growth. The low thermal energy needed enables cost savings when looking to wide scale implementation and also opens the door for incorporation of electronic devices on varying types of substrates such as plastics, metal foils, and adhesives.
1.4 Summary and Motivation

The strongest motivator for the work in this thesis is the conceptualized photovoltaic device pictured in Figure 1-1. As shown in the figure, the solar cell is comprised of a p-i-n stack featuring the p-type Si nanowires interpenetrating the intrinsic a-Si:H layer.

![Conceptual depiction of proposed photovoltaic topology.](image)

Figure 1-1. Conceptual depiction of proposed photovoltaic topology.

This design is an advancement of a typical p-i-n solar cell, where a p-type, intrinsic, n-type a-Si:H stack is used to collect light and produce charge. An Al contact on the back of the cell will interface with the n-type a-Si:H layer to extract charge and a second Al contact will interface with the ZnO:Al to extract charge from the front of the cell. The ZnO:Al is a transparent conducting oxide and can provide ample conducting for charge to be extracted while allowing light to pass through the bottom side of the device. The overall cell thickness would be on the order of 1 µm with the ZnO:Al being 50 nm thick, the p-type a-Si:H being 100 nm thick, the intrinsic a-Si:H being 500 nm thick, the n-type a-Si:H being 100 nm thick, and the back contact being 250 nm thick. Of course, these thicknesses may be altered in order to produce an
optimally operating solar cell. Light enters from beneath the cell, through the glass substrate and ZnO:Al penetrating the p-i-n stack. Any remnant light not trapped by the SiNW will be reflected from the back contact into the p-i-n stack for a second chance to be trapped in the forest of p-type SiNW. Al contacts allowed for charge to be extracted through the back n-type a-Si:H layer and the front ZnO:Al layer. Additionally, the charge separating field created by the p-type/intrinsic interface will be enhanced due to a dramatic increase in surface area owing to the surface of the Si nanowires. Another feature of this device is its capability to be fabricated in-situ, mitigating oxidation effects and particle impurities. Since the design will be made using PECVD the manufacturing aspects such as a scalability and throughput will be flexible contributing to a lower cost end product. Since the overall amount of Si used in this device will be less than 1 µm in thickness, the overall material cost will be substantially less than the thick crystalline Si solar cells that dominate the current consumer market. The device of Figure 1-1 is a steadfast competitor to replace current marketable technologies as a photovoltaic product that can reach grid parity at low cost.

A brief survey of silicon nanowire growth both through PECVD and other fabrication methods has been given. The rest of this thesis concentrates on experimentation using PECVD to grow both Au catalyzed and Al catalyzed silicon nanowires. First, the reader is provided an explanation on popular theories concerning why growth occurs using PECVD with relevant applications of PECVD grown nanowires highlighted. Chapter 3 discusses the experimental methods and equipment used to conduct the experiments in this thesis. Chapter 4 contains the presentation of results from the experimental work included in this thesis as well as relevant discussions concerning properties of the as grown silicon nanowires. Chapter 5 concludes the
thesis and contains an examination of future areas of work that will support development of optimized, high quality electronic devices. Chapter 5 also provides information regarding future areas of work that have been enabled by this thesis.
Chapter 2: Theoretical Aspects of Silicon Nanowires

This section discusses the relevant theory of nanowire fabrication and theoretical aspects of nanowire devices. First, a brief look at growth physics is introduced followed by a discussion of the role of the plasma in the growth of nanowires. This chapter also includes a survey of theory governing the implementation of nanowire devices ranging from electronics such as transistors to energy conversion uses such as photovoltaics.

2.1 Theory of Nanowire Growth

The physics behind the growth of silicon nanowires via a metal catalyst differs depending upon the metal used and the substrate used. This difference is largely a result of the temperature at which processing occurs, as this determines whether a solid phase diffusion takes place or a liquid phase diffusion process. This section explains the mechanism by which silicon nanowires are thought to grow. The Vapor Liquid Solid (VLS) method is first discussed, followed by a discussion of the Vapor Solid Solid (VSS) method. A new section is then developed that discusses specifically the role of the metal catalyst in the growth process. This is followed by examining the growth process amongst the addition of a plasma environment.

2.1.1 Growth Mechanisms

Vapor-liquid-solid growth refers to a growth process by which a vapor phase is diffused into a liquid phase of a material system, such that a solid phase of single material or a multiple material system forms. This growth process is dependent upon the surface interactions of all of the phases of the material systems present during the process. This process can be described in a
pure physical form using a thermodynamic formulation, but a more tutorial like approach is taken here.

The formulation of this growth process begins with the schematic process that is shown in Figure 2-1.

Figure 2-1. Schematic depiction of three initial phases of silicon nanowire nucleation using PECVD. (a) shows the formation of the liquid eutectic droplet with the surface energies $SE_{lv}$, $SE_{sv}$, and $SE_{ls}$ shown that determine its shape. (b) shows the initial phases of growth, specifically the precipitation and formation of c-Si between the Au/substrate interface. (c) depicts the growth as the wire continues to grow with some Au being consumed.

The process begins with a solid film in contact with a solid surface. The word solid here is used to describe an ideal solid surface meaning it has atomic flatness, no irregularities present at the surface, and the solid itself is composed of an ideal material with no defects. Here it is assumed
that the material system is a thin Au film of nanometer thickness on top of an infinitely thick Si solid. Though the assumption of a specific material system has been made, this theory can be applied in its most general form to any material system.

If 363°C heat is supplied to the material system such that the eutectic temperature is reached, then the Au will form eutectic droplets on top of the Si surface as shown in Figure 2-1 (a). These droplets are 69% Au and 21% Si by atomic composition and form a liquid alloy. The size of this droplet both in volume and radius is thermodynamically determined by the net forces of the surface energies of the phases present in the system. The mathematical relation between these surface energies is modeled by the Young equation,

$$SE_{SV} = SE_{SL} + SE_{LV} \cos(a_c)$$  \hspace{1cm} \text{Equation 2-1}

where the solid-vapor surface energy is denoted by $SE_{SV}$, the solid liquid surface energy by $SE_{SL}$, the liquid-vapor surface energy by $SE_{LV}$, and the contact angle the droplet forms with the substrate is given by $a_c$. This mathematical equation describes how the liquid alloy droplet holds its shape on the surface of the substrate beneath it. The balance of forces that maintain the shape of the droplet also determines the diameter of the droplet, and thus the diameter of the wire. The minimum diameter that can be assumed by the Si nanowire is usually governed by the Gibbs-Thomson [18] equation that states mathematically,

$$r_{min} = \frac{2SE_{LV}V_L}{RTln\sigma}$$ \hspace{1cm} \text{Equation 2-2}

Here $r_{min}$ is the minimum radius, $SE_{LV}$ is the surface energy of the liquid vapor interface, $V_L$ is the molar volume of the molten material, $R$ is the Rydberg constant, $T$ is temperature, and $\sigma$ is the degree of supersaturation of the liquid droplet. This equation states that the diameter of the
nanowire that can be obtained is function of the catalyst material, although the non-equilibrium state of the plasma changes this, a physical phenomenon that will be explained in Section 2.1.3.

After annealing for a desired amount of time, SiH$_4$ gas is admitted to the chamber. This is depicted in Figure 2-1 (b). At temperatures just above the eutectic temperature of 363°C there is not sufficient thermal energy for the SiH$_4$ to decompose into radical species. Instead plasma is enacted to break the SiH$_4$ into its respective gaseous components which can include SiH, SiH$_2$, SiH$_3$, H$_2$, and even H.

As the SiH$_4$ radicals diffuse into the eutectic particle, the material system is forced out of its equilibrium state. At this point, a Si flux is present at the surface of the vapor liquid interface and simultaneously a Si flux is present at the liquid solid interface. When a steady state equilibrium is reached between the two fluxes, the liquid droplet becomes supersaturated with Si and begins to precipitate out Si at the solid liquid interface in order to remain in equilibrium. This precipitation process is schematically shown in Figure 2-1 (b). With continued diffusion of Si bearing radicals into the liquid droplet, the crystal continues to grow. As this growth process takes place, the Au at the tip of the wire changes morphology because the Au is consumed by the plasma and diffusion into the wire, as shown in Figure 2-1 (c). This causes some amount of Au doping, which could be detrimental to the properties of electronic device as Au forms a mid-gap state within the Si lattice [19].

The extent to which the Au dopes the Si is a subject that has not been proven one way or another, and it remains to be seen if it is even a viable threat. Methods from which Au doping
concentrations can be extracted include local electrode atom probe (LEAP) microscopy which was used by Perea et. al. to show that concentrations of Au can be as high as $1 \times 10^{16}$ cm$^{-3}$ to $1 \times 10^{20}$ cm$^{-3}$ at technologically relevant temperatures [20]. The distribution of the Au dopants is something that is still debated as conflicting data show different doping scenarios with some stating Au dopants reside near the surface, while others state that they are evenly distributed throughout the wire [21], [22]. The discrepancy in detrimental Au doping in Si nanowires is a relevant issue to be explored because Au can catalyze Si nanowire growth with relative ease when compared with other metal catalysts such as Al, In, or Ga. This is an issue that is outside the scope of this thesis. It is mentioned here as this Au contamination is a feature of VLS grown Si nanowires and it cannot be ignored.

Another method by which silicon nanowires can be nucleated is referred to as the Vapor-Solid-Solid (VSS) mechanism. Just as the name indicates, this mechanism relies upon a vapor that diffuses into a solid particle or film on top of a solid substrate thus forcing it into a non-equilibrium state making it precipitate out material at the solid/solid interface. This is a growth mechanism that takes place when the material system is at sub-eutectic temperatures such that no liquid droplets form. Researchers have shown that Cu can be used to grow Si nanowires using a VSS mechanism because of Cu$_3$Si formation at the tip of the wire [23]. This silicide formation was not noted as being the key to the VSS growth but it was used to prove that the growth was occurring by a solid phase diffusion. This research shows that VSS is possible with the right processing conditions and is an important growth mechanism as it could be the gateway to low temperature growth of Si nanowires with CMOS compatible benign metals such as Al.
2.1.2 Effect of Metal Catalyst

Since the growth process of the silicon nanowires is largely dependent upon the surface energy of the interfaces involved, it is important to consider the effect of metal catalyst choice. The relationship between the substrate and the metal catalyst can be thought of as an active driver in the growth process. It is the binary phase diagram of the two materials that most individuals turn to when attempting to grow wires. The information provided in the phase diagram allows one to determine at which temperatures, what compositions of the binary material system will be available and thus, which metals can serve as suitable catalysts.

This requirement of binary phase composition, is not the only determinant of the growth process, as a number of practical requirements dominate as well. As mentioned previously, Au can possibly contaminate the nanowires with large numbers of deep-level impurities. Au, though, is able to nucleate Si wires with relative ease compared to other metals as the Au-Si eutectic temperature of 363°C is relatively low. The binary phase diagram reveals a Si rich eutectic aiding in the saturation of the liquid alloy droplet. Additionally, Au is known to crack SiH₄, which would contribute more Si to the liquid alloy droplet. Au has very low chemical reactivity, and does not form an oxide, which is advantage in wire growth.

When looking to choose an alternative catalyst material, one looks at technologically relevant metals that readily incorporate into the semiconductor industry in standard processing lines and have well studied phase diagrams with Si. These metals include, Al, Cu, Ag, In, and Sn to name a few. All of these metals present impurities into Si, though Al actually has energy levels that dope Si p-type. One concentration of this thesis is to use Al to nucleate Si nanowires, as it is
technologically compatible with Si. One problem that Al is notorious for though is its high chemical reactivity. It readily forms bonds with oxygen creating a strong oxide preventing the growth of Si nanowires. Individuals have grown Si nanowires using an Al catalyst, but have usually done so at UHV pressures or at high temperatures [24]. The Si-Al eutectic occurs at 577 °C, which is nearly double that of the Au-Si eutectic. A method that could produce p-type Si nanowires with Al at a lower temperature could be readily accepted into technological applications.

A good review of metal catalyst effects on the growth of Si nanowires is provided by Schmidt et. al. and this will be summarized here [25]. Effectively, metals can be organized into different categories based upon solubility and chemical reactivity with Si. Metals such as Al, Au, and Ag are all similar in that they have high Si solubility, but are not known for forming silicides. Other metals form no silicides, but have low Si solubility such as Ga, Zn, and Cd. A third category of metals are those that are known to form silicides such as Ti, Fe, Cu, and Ni. Both VLS and VSS type growth is possible with those metals having high Si solubility, growth is limited for those metals having low Si solubility, and silicide forming metals only seem to grow wires at high temperatures in a VLS like mode [25].

Primarily one would like to only use those metals that can form low temperature eutectics with high Si solubility. The only metals belonging to this category are those of Au, Ag, and Al. Since Au can be used to create silicon nanowires with ease and because Al is highly compatible metal with Si, the focus of this thesis is on experimentation involving both Au and Al. Both of
these materials are excellent candidates for low temperature nucleation of silicon nanowires due to their simple eutectic relationships and high Si solubility.

The metal catalyst plays an important role in determining the growth mode of the silicon nanowire. This is mainly due to the interactions between the metal catalyst and the substrate on which it is grown. Another factor that may even alter the aspects of the metal catalyst/substrate relationship is that of the plasma environment in which PECVD grown silicon nanowires are introduced. The next section discusses the role of the plasma in the growth of silicon nanowires.

2.1.3 Plasma Enhancement

The role the plasma plays in the Si nanowire growth process is one that has been experimentally reported but little research has been done on the plasma itself. The only known cases of such research come from Ostrikov et al. and Mehdipour et al. [26], [27]. Working together these researchers developed numerical studies that take into account parameters of the plasma to show minimization of the Gibbs-Thomson effect [26] and simultaneous supersaturation of metal catalyst particles [28]. While the modeling presented by these researchers was based upon relevant works in the field of plasma grown nanowires, no one has experimentally verified the outcomes of these simulations. Nonetheless, this section will give brief discussion of the plasma’s role in the silicon nanowire growth process.

PECVD is a process that was developed out of the need to deposit high quality dielectric film layers at low temperatures. The main difference between PECVD and other CVD method is the use of the plasma to add additional energy to the growth system. The plasma is of
nonequilibrium nature that gives added flexibility to the growth process. Ions and free electrons of the gaseous species populate the plasma through high energy ionization reactions that are a result of the RF power that is applied to the gas in the processing chamber.

The ionization reactions cause the gas molecules to dissociate into a variety of gaseous species. Some of the gaseous species include free-radicals, which are neutral states of molecules with high levels of chemical reactivity. Often, models of the nanowire growth process start from a thermally dissociated gas that diffuses into a nanoparticle. In the presence of plasma, radicals could diffuse into the metal catalyst particle and high energy surface processes could act to create interesting science involving the growth process.

Ostrikov and Mehdipour examined Au catalyzed growth of a Si nanowire in a plasma of Ar+H₂+SiH₄ gas by developing a model including a plasma sheath, diffusion, thermal effects, and Si monolayer creation [26]. The modeling shows that the energy barrier for the creation of the Au-Si islands is inversely related to the chemical potential as is described in the Gibbs-Thomson equation. This energy barrier is lowered due to the local heating effects created by the plasma which tend to mitigate the GT effect [26]. The plasma also can act to speed super saturation of different size Au-Si particles across the surface of the substrate, thus simultaneously activating particles of different size. This is largely driven by the locality of heating due to the plasma, as well as the ion-assisted creation of Si bearing radicals that can more easily diffuse into the Au-Si particle.
The plasma acts to disturb almost every aspect of the growth process from its equilibrium state, and in doing so alters the growth physics of the silicon nanowire. This research field is in its infancy and it will be interesting to see what other developments arise in determining how the plasma alters the growth process. Already, a beneficial aspect is noted in that the Gibbs-Thomson effect does not place a lower limit on the radius of PECVD grown nanowires. This means that PECVD can accommodate a larger range of growth diameters than other methods, thus adding to its advantages as a superior fabrication method for the nucleation of silicon nanowires.

2.2 Nanowire Theory and Devices

Silicon nanowires are sought after for the use in device implementation mainly due to the interesting quantum effects that arise from the nano-scale level. This nano-scale physics can provide opportunities for using Si in ways that was previously not possible using the bulk characteristics alone. Here a brief overview of confinement in silicon nanowires is given followed by sections concerning how silicon nanowires can be used and implemented in devices. This is meant to give the reader a current understanding of why nanowires are an attractive device platform and the state-of-the art devices being created from them.

2.2.1 Confinement and Its Effects

The result of creating a Si nanowire tends to alter the electronic properties due to the constraint placed on physical size. When the dimensions of a bulk sample are reduced such that the size is limited to the nanometer scale in 2 dimensions a nanowire is created. Si nanowires are 1D devices, so called because the constraint placed on the physical dimensions also places
constraints on the density of states inside the material. This section serves to give a general overview of how the interesting properties of nanowires come about.

Density of states in a normal semiconductor sample are those states that are available to be occupied by electrons in the material. More specifically, the density of states is the number of allowed occupation states per unit volume of a material as a function of energy. The density of states arises from examining the behavior of a free electron as it is confined to the boundaries associated with a periodic lattice. This ultimately arises from examining the momentum that is available in 3 dimensions. If one begins to examine what occurs when the momentum space of a free electron is restricted to lower dimensional values, one finds that the density of states varies by $1/\sqrt{E}$ [29] and for a 1-D system the density of states varies exactly as $1/\sqrt{E}$. When combining the density of states with the Fermi-Dirac statistics (those statistics governing the probability of occupation of a state an electron can assume) the concentration of electrons is found. The concentration of electrons, or holes, for that matter, is an important factor in semiconductor devices as so many parameters are dependent upon these values. Such factors that are dependent upon electron concentration are resistivity and conductivity, intrinsic concentration, and mobility. The direct effect of confining states to one dimension directly alters everything about the semiconductor as compared to its bulk counterpart due to the effect of the change in electron concentration that is allowed for that system.

In the literature, there are several investigations that have explored the one dimensional aspects of Si nanowire technology. Main areas where the dimensionality effects of silicon nanowires have been realized include the optical properties of Si [11], the thermal conductivity of Si [30],
and electrical properties of silicon nanowires [31]. The implications of such alterations of physical properties are presented in the next sections.

### 2.2.2 Electronic Device Uses

The CMOS transistor technology that has dominated electronic applications for years is running into a major problem, the physical limitations imposed by device miniaturization. Nanowire transistors may circumvent such fundamental problems by decreasing design trade-offs in gate lengths, contact areas, and to increase flexibility of circuit design. This section provides an overview of proposed applications where Si nanowires might help to circumvent the CMOS scaling problem.

Early studies of Si nanowire based transistors found that the Si based nanowire devices yielded low transconductance and mobility values in the range of 0.01 cm²/V-s [32]. It was discovered that such deficiency in mobility was largely a result of contact methods, and so thermal annealing studies revealed that nanowires had comparable performance to state-of-the-art planar MOSFET technology on silicon on insulator substrates [33]. At this time, Si nanowire based transistors were shown to have promise to exceed the performance of conventional device technology. However, Si nanowire transistors were fabricated using a top down method that required extensive lithography steps to define individual transistors. Innovations in Si nanowire device design led to the creation of vertically integrated FETs with surrounding gates [34], These designs were sought after for their subthreshold behavior and significant increase in device density per substrate. The density was increased over conventional CMOS technology by using gate electrodes along the length of the nanowires [34]. Additionally, the transport
properties of such transistors were shown to have the same order of magnitude as planar MOSFET technology [34].

Since the time when new transistors innovations were emerging that promised to exceed the performance of traditional CMOS technology, other innovative discoveries were made. These discoveries come through in recent works where reconfigurable transistors [35], junctionless transistors [36], nanowire circuits [37], and Tunneling-FETs [38] have been proposed that are all based upon Si nanowire technology. These technologies are all working proof that Si nanowires can either be used to match or exceed CMOS technology through enhanced transport characteristics or that Si nanowires can be used in innovative ways to allow enhanced capabilities to come forth that were not previously possible with CMOS technologies.

2.2.3 Energy Conversion Uses

Silicon nanowire based energy conversion devices are sought after for their unique ability to overcome traditional barriers of device implementation. Here three energy conversion technologies, battery technology, thermoelectric devices, and solar cells, are reviewed. This is by no means exhaustive, but it is used to inform of the potential solutions to problematic obstacles that have arisen as researchers try to implement Si nanowire device technology for energy conversion purposes.

With miniaturization and increasing portability of electronic devices and innovations in electric vehicles, energy storage demands are increasing. Industry has favored the use of the Li-ion battery for many years due to its ability to lose charge slowly when not in use, lack of memory effect and superior energy density. Increasing energy storage demands have urged new
innovations in battery technology that utilize silicon nanowires as an anode material [39]. This use of Si nanowire technology stems from the fact that Si can store ten times as much Li as traditional graphite anodes, dramatically increasing energy density of the batteries while reducing weight. Specifically the diameter of the Si nanowires tolerates volumetric changes better. Electric conduction is produced by each individual nanowire in contact with a metal electrode, and 1D conduction routes allow for superior charge transport [39]. These improvements are in contrast to thin a-Si films and Si nanoparticles that have been utilized as anodes in Li based battery technology. Si nanowires based batteries have recently begun to be implemented in industry based upon the results of Cui’s research at Stanford University [40]. The practical implementation of such a technology is proof that it is a working concept and society will see the emergence of Si NW based Li battery technology soon.

Another realm of energy conversion where Si nanowires show promise of increasing device performance is that of thermoelectrics. A thermoelectric material is one that produces electricity from heat. This is done through the Peltier effect, a physical phenomenon whereby charge carriers in a temperature gradient diffuse from hot regions to cold regions carrying thermal energy with them. Thermoelectrics can be used to heat or cool devices and can also be used to collect heat energy to produce an electric current. The figure of merit by which thermoelectric materials are examined is called $ZT$ defined as,

$$ZT = \frac{S^2T}{\rho k}$$  \hspace{1cm} \text{Equation 2-3}$$

where $S$ is the Seebeck coefficient, $T$ is temperature, $\rho$ is electrical resistivity, and $k$ is thermal conductivity. Having a $ZT > 1$ is a technologically relevant figure of merit and it has been difficult for researchers to achieve this value because the factors involved in $ZT$ are mostly
independent [41]. Individuals have used compositions of BiTe to reach a $ZT$ of about 1, but these materials are both cost prohibitive and introduce significant industrial scaling problems. Silicon nanowires can replace BiTe and in doing so will mitigate cost barriers and scaling issues. This application of Si nanowires to thermo electrics has been proven by Hochbaum et. al. when they utilized a solution based method to fabricate Si nanowires across an entire wafer and measured the parameters needed to calculate $ZT$ using 4-point IV methods and standard optical lithography [30]. For nanowires exhibiting diamteres <300 nm phononic path lengths are confined over the typical bulk Si parameters giving rise to thermal conductivities that are a factor of 100 lower than that of bulk Si. This acts to increase the $ZT$ value by roughly two orders of magnitude from 0.01 to 0.6, thus making Si nanowires a viable candidate for thermoelectric devices [30]. Others have created Si nanowire devices that exhibited close to a value of 1 for $ZT$ but at lower temperatures than the 300K mark achieved by Hochbaum [42]. Boukai et al. used a lithographic method to define their silicon nanowires which differed in the approach that Hochbaum used. The wires developed by Boukai were smaller in diameter and it is though that the phonon confinement contributed to a higher Seebeck coefficient [43]. Regardless, this type of work that examines the suitability of Si nanowires for thermoelectrics opens up the door to yet another application where Si nanowires maintain dominance over other materials.

Silicon nanowire based solar cells offer several advantages over the traditional wafer based Si solar cell design. The most notable of these advantages are inherent light trapping, material quality tolerance, and cost reduction. Garnett and Yang showed that ordered arrays of silicon nanowire structures could actually exceed the theoretical Lambertian scattering limits due to the effective light trapping of the nanowire array [44]. The ability of a solar cell to trap light with its
structure alone is of great benefit as this reduces the number of fabrication steps needed to construct the cell. Additionally, the level of light trapping induced by the silicon nanowire structures is superior to that provided by single layer AR coatings that are typically put on traditional wafer based solar cells. A main cost driver of Si solar cell technology is the purity of material required to produce a high quality c-Si base solar cell. Kayes et. al. showed that the material quality of nanorod base solar cells can be reduced due to the radial nature of the pn junction [45]. He showed that the radial dimensions of the wire are optimal when they match the diffusion lengths. Having junctions within a diffusion length of the charge carriers leads to increased charge collection as the minority carriers can successfully be collected without recombining. The relaxation of material purity requirements also leads to dramatically reduced cost of the final solar cell. In addition, the amount of absorber material needed to successfully collect light has been shown to be a significant fraction of that that would required in a typical thin film c-Si solar cell [46]. Despite the fact that the nanowire solar cell remains a promising candidate a number of factors stand in the way of successful implementation. Such factors are given in a review by Garnett et al. which include, surface and interface recombination, chemical stability, mechanical strength, controlled fabrication of geometrical characteristics, uniformity of growth, and scalability [47].

Silicon nanowires have great potential of replacing bulk counterparts in many device applications in the area of energy conversion. Many obstacles still stand in the way of device implementation for battery, thermoelectric, and solar energy conversion. These obstacles will require in-depth investigation of nano-scale physics in order to truly overcome them. Part of the goal of this research is to successfully learn how to control the growth of the nanowires so that a
controllable and scalable fabrication technique can be realized. Achieving this goal alone would advance silicon nanowire device implementation by many orders of magnitude.
Chapter 3: Experimental Investigation and Research Tools

This chapter begins with a section concerning the approach taken to design a set of experiments so that silicon nanowire growth could be obtained. This is followed by a description of the experimental methods and tools used to grow and characterize silicon nanowires.

3.1 Experimental Approach

In order to make sure that the results obtained from experimentation would be valid enough to reproduce, a systematic method of experimentation was chosen. The method of experiment chosen for growing Si nanowires with Au and Al catalysts was a fractional factorial design. A fractional factorial design is an efficient way to approach experimentation, to extract the maximum amount of information about factor interaction with the minimum number of runs. The cost associated with this thesis method is that it does not result in sufficient data to create a model of the interactions across the experimental space.

In the case of the Si nanowire experiments, a two-level six factor fractional factorial design was chosen that was optimized to extract 3 main effects of the processing with 16 experimental runs. The runs that were generated by the fractional factorial design are included in Table 3-1.
Table 3-1. Fractional factorial design showing experiments performed for both Au and Al catalysts. The selection of factors was based upon factors from the literature that were reported to give nanowire growth. The experiments were automatically randomized so that bias errors could be eliminated.

<table>
<thead>
<tr>
<th>ID</th>
<th>Metal</th>
<th>Time (min)</th>
<th>Power (W/cm²)</th>
<th>Flow Rate (sccm)</th>
<th>Thickness (nm)</th>
<th>Pressure (torr)</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>Au</td>
<td>90</td>
<td>0.04</td>
<td>20</td>
<td>1</td>
<td>0.1</td>
<td>400</td>
</tr>
<tr>
<td>B2</td>
<td>Au</td>
<td>15</td>
<td>0.02</td>
<td>50</td>
<td>5</td>
<td>0.1</td>
<td>400</td>
</tr>
<tr>
<td>B3</td>
<td>Au</td>
<td>15</td>
<td>0.04</td>
<td>50</td>
<td>1</td>
<td>1</td>
<td>150</td>
</tr>
<tr>
<td>B4</td>
<td>Au</td>
<td>90</td>
<td>0.02</td>
<td>20</td>
<td>5</td>
<td>1</td>
<td>150</td>
</tr>
<tr>
<td>B5</td>
<td>Au</td>
<td>15</td>
<td>0.02</td>
<td>20</td>
<td>5</td>
<td>0.1</td>
<td>150</td>
</tr>
<tr>
<td>B6</td>
<td>Au</td>
<td>90</td>
<td>0.04</td>
<td>50</td>
<td>5</td>
<td>1</td>
<td>400</td>
</tr>
<tr>
<td>B7</td>
<td>Au</td>
<td>90</td>
<td>0.02</td>
<td>50</td>
<td>1</td>
<td>0.1</td>
<td>150</td>
</tr>
<tr>
<td>B8</td>
<td>Au</td>
<td>15</td>
<td>0.02</td>
<td>20</td>
<td>1</td>
<td>1</td>
<td>400</td>
</tr>
<tr>
<td>B9</td>
<td>Al</td>
<td>90</td>
<td>0.04</td>
<td>20</td>
<td>1</td>
<td>0.1</td>
<td>400</td>
</tr>
<tr>
<td>B10</td>
<td>Al</td>
<td>15</td>
<td>0.02</td>
<td>50</td>
<td>1</td>
<td>0.1</td>
<td>400</td>
</tr>
<tr>
<td>B11</td>
<td>Al</td>
<td>15</td>
<td>0.04</td>
<td>50</td>
<td>1</td>
<td>1</td>
<td>150</td>
</tr>
<tr>
<td>B12</td>
<td>Al</td>
<td>90</td>
<td>0.02</td>
<td>20</td>
<td>1</td>
<td>1</td>
<td>150</td>
</tr>
<tr>
<td>B13</td>
<td>Al</td>
<td>15</td>
<td>0.04</td>
<td>20</td>
<td>5</td>
<td>0.1</td>
<td>150</td>
</tr>
<tr>
<td>B14</td>
<td>Al</td>
<td>90</td>
<td>0.04</td>
<td>50</td>
<td>5</td>
<td>1</td>
<td>400</td>
</tr>
<tr>
<td>B15</td>
<td>Al</td>
<td>90</td>
<td>0.02</td>
<td>50</td>
<td>5</td>
<td>0.1</td>
<td>150</td>
</tr>
<tr>
<td>B16</td>
<td>Al</td>
<td>15</td>
<td>0.02</td>
<td>20</td>
<td>5</td>
<td>1</td>
<td>400</td>
</tr>
</tbody>
</table>

The initial experimental parameter space was chosen as a result of both machine limitation and literature survey. As explained in Section 1.3, Hofmann had successfully nucleated silicon nanowires using a temperature above the eutectic of the Au/Si interface and with a 30 mW/cm² plasma density [3]. Originally, a wider flow rate range of up to 100 sccm was included as this was what the mass flow controllers (MFC) could nominally regulate. Upon experimentation, it was found that 50 sccm was a practical flow rate for the MFCs and the experimentation had to be amended accordingly. The original temperature range that was desired to be covered by the experimentation included temperatures up to the 600°C range, so that experiments covering the Al/Si eutectic of 577°C could be investigated. It was discovered a more practical temperature range would be 400°C as testing to beyond this temperature often proved to degrade the cabling.
that ran to the heater rings. After making these amendments to the parameter space, the initial table of experiments was formed into the 16 experiments that are depicted in Table 3-1.

Prior to loading samples into a deposition chamber, Si samples were cleaned in a chemical process. The chemical process utilized 1:1:1 H$_2$SO$_4$:H$_2$O$_2$:DIH$_2$O. The Si samples were immersed in the solution for a period of 10 minutes, followed by a DI H$_2$O rinse for 3 minutes. Following the rinse, the samples were immersed in a 10:1 DIH$_2$O:HF solution for 30-45 seconds until the surface of the Si became hydrophobic. The sample was then dried in N$_2$ gas. This process was to ensure that the surface of the Si remained atomically clean prior to metal deposition. Glass samples were cleaned in ultra sonic baths of acetone and methanol at 40°C for 10 minutes each. First the glass samples were immersed in the heated acetone, then immediately immersed in the heated methanol. The samples were dried in a steady stream of N$_2$ following the cleaning processes.

After cleaning, the substrate was loaded into the thermal evaporator for metal deposition. The thermal evaporator resistively heated a metal boat that contained a solid piece of metal. Since the evaporation process took place at high vacuum pressures, the vapor pressure of the solid metal was such that the material began to evaporate when heated to the correct temperature. This evaporation physically deposited a metal film onto the (Si or glass) substrates. An in-situ crystal monitor detected how much film was deposited on the sample by sampling the crystal surface via high frequency resonance of vibrational modes to determine the thickness of the film.
After a metal film was evaporated, the samples were transported to the MVSystems cluster deposition tool as described in Section 3.2.1. Additional experiments were performed in a single chamber PECVD tool as described in Section 3.2.2. The initial 16 experiments shown in Table 3-1 were performed in the MVSystems multi-cluster tool described in Section 3.2.1. Samples were allowed to pump down to high vacuum regimes in the MVSystems reactor \(10^{-8} \text{ torr}\) and the single chamber reactor \(10^{-6} \text{ torr}\). Differences in pump technology prevented the two systems from having the same pumping capabilities.

3.2 Deposition Tools

A brief overview of the two PECVD system used in experimentation are given. One tool was a MVSystems deposition tool referred to as the MVS and featured an automated robotic arm for sample delivery. The second PECVD tool, referred to as the GSI system, was a custom built tool (based upon the Glasstech Solar Inc. design) that was less complex than the MVS, but did not have all of the capabilities that the MVS had. Each machine is discussed in the sections that follow.

3.2.1 MVSystems Tool System Overview

The MVS deposition tool that was located at the Engineering Research Center consists of several stainless steel chambers that allowed one continuous vacuum state inside the chambers. A picture of the tool is shown in Figure 3.1. The system featured two chambers devoted to plasma enhanced chemical vapor deposition (MPZ 1 and MPZ 2), two chambers devoted to sputtering (MPZ 3 and MPZ 4), and one chamber devoted to annealing (MPZ 5). MPZ 1-5 were connected to an even larger cylindrical chamber that was referred to as the intermediate transfer zone (ITZ).
The ITZ featured a load lock door for user access so that samples could be loaded into the chamber. Isolation between chambers was achieved through high vacuum gate valves that acted as vacuum tight doors between the ITZ and various MPZ chambers. The ITZ featured one mechanical pump that allowed the chamber to reach pressures of approximately $5 \times 10^{-2}$ torr. The ITZ also had appropriate valving so as to allow nitrogen to fill the chamber during venting processes. The mechanical pump was also valved so that the pump could be isolated from the

![Figure 3-1. Photograph of MVSytems Inc. Multi-cluster deposition tool showing all of the deposition chambers as of February 2012. Starting at the left and going clock wise to the right, the chambers are MPZ 1, MPZ 2, MPZ 4, MPZ 3, and MPZ 5. The load lock door is shown on the front of the system. The computer monitor displayed shows the interface that allows one to control the robotic arm.](image-url)
chamber during venting. The ITZ also contained the robotic arm that delivers samples from chamber to chamber.

MPZ 1 was devoted to the deposition of high quality intrinsic hydrogenated amorphous silicon compatible with thin film solar cell applications. To do this, it shared a corrosion resistant turbo pump and a corrosion resistant mechanical pump with MPZ 2. After a 24 hour period of pumping at room temperature, the chamber was able to reach pressures as low as the high $10^{-9}$ torr range. Gases that could be introduced into the chamber included silane ($\text{SiH}_4$) and nitrogen ($\text{N}_2$). The system featured a pancake type heater on the top that was connected to an Omega temperature controller. The Omega temperature controller was connected to a solid state relay that opened and closed in order to deliver 120 VAC to the pancake heater located on top of the chamber. The chamber was able to reach temperatures up to 600 °C, with the substrate limited to a maximum temperature around the 450 °C range. The system possessed an RF feed through that allowed RF power to be coupled to the electrode inside the chamber. A photograph of the electrode that was inside the chamber is shown in Figure 3-2.
Figure 3-2. Photograph of the inside of the MPZ 1 chamber showing the top of the electrode that ignites the plasma with RF power. The parallel rails in the picture are the tracks that the substrate sits on during a deposition. The bar at the left of the image is where the gases are admitted to the chamber.

MPZ 2 featured a configuration highly similar to that of MPZ 1. The chamber shared the same pumping system as previously described in MPZ 1. The main difference was the gases that were allowed inside of the chamber. The gases allowed in the chamber were SiH₄, phosphine (PH₄), diborane (B₂H₆), hydrogen (H₂), N₂, and nitrogen trifluoride (NF₃). This chamber was originally configured for the deposition of high quality doped amorphous silicon films for thin film solar cell applications. The electrode configuration was equivalent to that of MPZ 1 and is shown in Figure 3-2.

MPZ 4 was a sputtering chamber used for the sputter deposition of aluminum (Al). The chamber featured a vertically configured sputtering system, with a 4” sputtering target below the
substrate. The track system was similar to that shown in Figure 3-2. The system features a non-corrosive turbo molecular pump and a rotary vane mechanical pump to evacuate the chamber of gases. This pumping system is shared with MPZ 3. The system was heated by the same heater configuration as MPZ1, MPZ2, and MPZ 3, which featured a pancake heater mounted on top of the chamber.

MPZ 3 was also a sputtering chamber that featured a 4” silicon target for the deposition of unhyrdogenated amorphous silicon films. Oxygen was also connected to the chamber for sputtering of silicon dioxide and other oxygen bearing silicon materials. The configuration was identical to that of MPZ 4.

MPZ 5 was a stainless steel tee that was connected directly to the ITZ without a gate valve. The chamber could reach pressures equivalent to that of the ITZ. It features a set of four halogen lamps mounted above the substrate. The halogen lamps were connected to a controller that was in turn connected to a solid state relay that provided on-off control for the lamps. The system was able to reach temperatures up to 600 °C in less than 30 minutes.

The system featured several devices to control and measure the pressure. Each MPZ chamber had a baratron that measured pressures up to the roughing range. This pressure information was utilized by the throttle valve that controlled the chamber pressure during film deposition by throttling the turbo pump. Each chamber also featured a nude ionization gauge that was capable of detecting pressures prior to depositions down to the $10^{-9}$ torr range. The ITZ had a convectron type pressure gauge that was displayed on the front of the system.
Gases were admitted to the chamber through one quarter inch stainless steel tubing that had a series of pneumatically controlled needle valves and mass flow controllers connected through VCR connectors. These needle valves were controlled by a switching system on the front of the MVS that allowed for user controlled delivery of gases to the chamber. A picture of the gas manifold is shown in Figure 3-3.

![Figure 3-3. Photograph of the gas manifold for the MV Systems Inc. cluster deposition tool. The gas manifold consists of a series of mass flow controllers (MFCs) that sit in parallel to each other. Each MFC has a pneumatically controlled needle valve that allows gases to be admitted to various sections of the gas line.](image)

### 3.2.2 Single Chamber System Overview

A second PECVD chamber was used to synthesize additional Si nanowire experiments beyond those presented in Section 3.1. This was done mainly to experimentally validate the work that appears in this thesis. This validation occurs because wire samples were successfully grown in
the single chamber system with the same parameters as those used in the multi-cluster deposition tool, thus proving the parameters were free of dependencies of the machine in which they are grown. Examples of the transportability of the growth parameters to the single chamber deposition tool are provided in Section 4.2.

Figure 3-4. Photographs of the single chamber PECVD tool used in some experimentation presented in this thesis. (A) Thermocouple wire, (B) top lid and substrate holder, (C) 2 ¾ in. glass viewport, (D) computer controlled throttle valve, (E) steel tubing to roots blower, (F) gate valve, (H) high vacuum valve, (I) stainless steel nipple, (J) turbomolecular pump, (K) exhaust to rotary vane backing pump.

The single chamber system featured a small stainless steel tee that comprised the main vacuum chamber. Inside of this tee was a capacitively coupled electrode that was fed through an RF feedthrough from an RF generator. Heating of substrates was performed via pancake heater that was situated directly on top of the substrate but external to the vacuum chamber. Beneath the table that the tee sat on was the rest of the vacuum components of the processing chamber.
system. The turbo pump pictured in Figure 3-4 was isolated from the main processing chamber via the gate valve. The turbomolecular pump was backed by a mechanical rotary vane pump. The exhaust of the rotary vane pump was interfaced with house plumbing that delivered the exhaust external to the building.

Processing pressure was controlled by a computer controlled throttle valve that is show in Figure 3-4 (D). Beyond the throttle valve was the high vacuum valve which was manually controlled and ensured isolation from the roots blower pump and the processing chamber. This system was configured so that the roots blower pump handled the corrosive gas load and safely pumped it from the chamber to the Edwards Inc. GRC gas abatement system.

Figure 3-5 shows the control rack next to the single chamber system as well as the gas manifold and the roots blower pump. The control rack featured both a computer and monitor that allowed interface with the throttle valve to control pressure in the chamber. The control rack also featured a switching box to control the pneumatically operating vacuum valves that controlled gas flow in the gas manifold. The RF generator, SiH₄ mass flow controller, pressure measurement gauges, and turbo power supply and controller were also housed within the control rack.

The gas manifold featured a number of mass flow controllers that regulated the flow rate of the different processing gases that could be admitted to the chambers. The gas manifold also featured manually operated needle valves. These manually operated valves were in place to allow a user to back purge the gas lines in the case of a part needing to be replaced or in the case
of a cylinder change. Back purging was an essential safety feature that guaranteed that any dangerous gases were evacuated from the gas lines prior to opening them to atmosphere.

In order to utilize the single chamber system, the user first applied power to the control rack by plugging in the 120 Vac plug. Then the power was applied to the rotary vane pump that backed the turbo pump. A manual roughing valve was opened that sat on top of the rotary vane pump that allowed the backing pump to begin to pump the back stage of the turbo pump down to

Figure 3-5. Photographs of control rack (left), gas manifold (upper right) and roots blower pump (lower right). (L) Computer monitor, (M) switching board for pneumatically controlled needle valves, (N) mass flow controller interface, (O) RF generator, (P) silane mass flow controller interface (Q) pressure monitoring controls,(R) turbo pump power supply, (S) temperature controller, (T) computer, (U) roots blower pump, (V) mechanical pump, (W) incoming line from system, (X) mass flow controllers, (Z) ¼ in. stainless steel gas tubing for gas delivery.
proper backing pressures ($10^{-3}$ torr range). After waiting 5-10 seconds the turbo power supply was turned on and the turbo was initiated after ensuring the gate valve was closed. The user then walks to the chase to switch the exhaust flow to the GRC from the MVS machine to the GSI machine. The user also opened valves in the chiller line to apply recirculation cooling water to the turbo. The roots blower was turned on by first turning on the mechanical pump that sat below the roots blower, then the blower was started.

After all of the pumps were switched on the user made sure that high vacuum valve and throttle valve were both closed. Nitrogen was admitted to the chamber at a rate of 1 SLM to vent the chamber for sample loading. After about 7 minutes, the pressure inside the processing chamber rose to atmosphere and the lid of the chamber was removed. Samples were inserted into a stainless steel substrate holder and the lid of the chamber was replaced. The $N_2$ that vented the chamber was turned off, and the throttle valve and high vacuum valve were opened to pump the chamber down. The roots blower was only capable of pumping the chamber down to the $10^{-2}$ or $10^{-3}$ torr range. After the chamber reached roughing pressures, the throttle valve and high vacuum valve were closed and the gate valve was opened to allow the chamber to pump to the high vacuum range. Once the appropriate base pressure was reached the user then closed the gate valve and opened the throttle valve and high vacuum valve again. The pressure set point was given to the computer and processing gases were admitted to the chamber. Once gas pressure was stabilized, the user used the RF generator and matching network to ignite a plasma in the chamber. After processing, a 10 cycle nitrogen purge was used to evacuate all gases in the chamber such that it could safely be opened to retrieve samples.
3.3 Characterization Tools

This section describes the main characterization tools that were used in this experimentation. Scanning electron microscope (SEM), transmission electron microscope (TEM), and optical transmission measurements were gathered. Wherever possible, information was included on unique ways in which the instrumentation was used to characterize silicon nanowires that went beyond the normal functionality of the equipment.

3.3.1 Scanning Electron Microscope

A SEM is not unlike an optical microscope that one may use in any scientific setting. The main difference is that in an optical microscope the result of the image is the reflection of photons from the sample surface. With an SEM electrons are reflected from the sample surface and these are examined to yield a computer generated image. The scanning part comes from the fact that an electron beam is rastered, or moved back and forth, over the substrate surface in order to produce an image of the sample.

One may naturally ask what advantage does this hold over a normal microscope. This advantage comes from the fact that the resolution of the SEM can be much higher than that of the optical microscope. To examine how we determine this fact we look to Abbe’s Equation [48] which tells us that the resolution is directly related to wavelength or stated mathematically,

$$d = \frac{0.61 \lambda}{n \sin(\alpha)}$$

Equation 3-1

where $d$ is the resolution in nm, $\lambda$ is wavelength of incident radiation in nm, $n$ is the refractive index, and $\alpha$ is the aperture angle. Here it is also of importance that the resolution is inversely proportional to both the refractive index that an electron is passing through and as the angle of
the aperture, the opening through which the electron beam is being projected. For an electron microscope the assumption that $n \approx 1$ and $\sin(\alpha) = \alpha$ is appropriate [48], giving,

$$d = \frac{0.61 \lambda}{\alpha}$$  \hspace{1cm} \text{Equation 3-2}

The only thing left to know now is the wavelength of an electron. Through a potential field, such as that established in an SEM the equation for wavelength is inversely related to the square root of the accelerating voltage [48]. The final equation determining resolution in the SEM is,

$$d = \frac{1.23}{\alpha \sqrt{V}} \text{nm}$$  \hspace{1cm} \text{Equation 3-3}

A reasonable estimate of $\alpha$ is 0.01 radians [48]. One can easily estimate what the resolution will be given an accelerating voltage which is a user determined input. Assuming a 100kV potential we arrive at 0.238 nm for the resolution. An optimal resolution for an optical microscope is determine by Equation 3-2 above. Using reasonable approximations one could conclude that a optimal resolution is about 200 nm. The SEM can yield resolutions 1000x greater than that of the optical microscope, thus explaining why it is a widely used instrument in examining nanowires. Scanning electron microscopes are most commonly used to obtain images of nanowires that are fabricated on a substrate. An example of an SEM image of an array of silicon nanowires is shown in Figure 3-6.
3.3.2 Transmission Electron Microscope

A transmission electron microscope (TEM) is quite similar to an SEM in that the interaction of electrons with electrons within a sample is analyzed to produce an image. The primary difference between the TEM and the SEM is that, in a TEM, electrons are transmitted through a sample rather than reflected from the sample surface. Because of this, samples that are used in the TEM must be <100 nm in thickness and be transparent to electrons.

TEM samples must be prepared on a TEM grid that is then placed in a substrate holder that is inserted into the vacuum of the TEM. The grid is often fabricated from Ni with a C film on top so as to create a continuous layer on which materials can be placed.
Nanowires grown by PECVD grow in such a way that they are attached to the growth substrate at the base of the wire. To remove such wires for analysis within a TEM, a method needed to be devised to remove the wires from the substrate and place them onto the TEM grid without any destruction of the wires. One method for doing this was simply to hold the substrate with the nanowires above the TEM grid and use a sharp blade to remove the wires from the substrate. It was found that longer continuous strokes of the blade across the sample surface produced better results. Figure 3-7 shows a TEM image of several nanowire pieces that were obtained using the scratching method.

![TEM image of nanowires](image)

**Figure 3-7** TEM image portraying result of scratching wires off onto a TEM grid. The wires vary in size and distribution due to the fact that the mechanical removal broke many wires.
Some other methods to extract nanowires that were found in the literature include extracting the wires into a liquid solution. The nanowires are then dispersed into the solution and controlled amounts are deposited onto a TEM grid [49]. The superiority of this method over the simple scratch off method is that a surfactant can be included into the liquid in order to help separate out individual nanowires.

Another method relies upon embedding the nanowires, as grown, into an epoxy [50]. When the epoxy hardens, extremely thin slices of the nanowire/epoxy composite are removed from the substrate.

While these methods exist for extracting nanowires onto the sample surface, they were not used in this thesis. The simplicity of the “scratch-off” method was by far the overwhelming reason for using that method. Though wires of various size were obtained, enough data still existed to extract meaningful information.
Chapter 4: Results of Growth

This chapter presents the results of the experiments performed during the course of this thesis work. As described in Chapter 3, a set of fractional factorial experiments was performed to determine main effects of the growth process. Additional experiments were performed to test the effects of different parameters on the controlled growth of Au catalyzed nanowires. First the main experiments from the fractional factorial design are presented followed by additional analysis of results. TEM images of individual nanowires extracted from the substrate provide analysis of the crystallinity and additional information regarding the relationship between length and diameter of the nanowires.

4.1 Au Catalyst versus Al Catalyst

As described in section 3.1, both Au and Al catalysts were evaporated onto Si substrates in order to initiate growth when subjected to the plasma environment. The factors determining growth that were analyzed included growth time, processing pressure, plasma power, SiH$_4$ flow rate, metal thickness, and substrate temperature. Observations of the experiments taken by SEM images were recorded and are presented. Discussion involving the main effects of the experiment and observational relationships between factors are given as well. When wires were successfully synthesized, they were removed for further analysis by TEM to determine the crystalline nature of the wires.
Tables 4-1. The top table shows the experimental matrix for Au and Al catalyzed experiments. The MVS was used to process all samples shown in Table 4-1.

<table>
<thead>
<tr>
<th>ID</th>
<th>Metal</th>
<th>Time (min)</th>
<th>Power (W/cm²)</th>
<th>Flow Rate (sccm)</th>
<th>Thickness (nm)</th>
<th>Pressure (torr)</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1</td>
<td>Au</td>
<td>90</td>
<td>0.04</td>
<td>20</td>
<td>1</td>
<td>0.1</td>
<td>400</td>
</tr>
<tr>
<td>B2</td>
<td>Au</td>
<td>15</td>
<td>0.02</td>
<td>50</td>
<td>5</td>
<td>0.1</td>
<td>400</td>
</tr>
<tr>
<td>B3</td>
<td>Au</td>
<td>15</td>
<td>0.04</td>
<td>50</td>
<td>1</td>
<td>1</td>
<td>150</td>
</tr>
<tr>
<td>B4</td>
<td>Au</td>
<td>90</td>
<td>0.02</td>
<td>20</td>
<td>5</td>
<td>1</td>
<td>150</td>
</tr>
<tr>
<td>B5</td>
<td>Au</td>
<td>15</td>
<td>0.04</td>
<td>20</td>
<td>5</td>
<td>0.1</td>
<td>150</td>
</tr>
<tr>
<td>B6</td>
<td>Au</td>
<td>90</td>
<td>0.04</td>
<td>50</td>
<td>5</td>
<td>1</td>
<td>400</td>
</tr>
<tr>
<td>B7</td>
<td>Au</td>
<td>90</td>
<td>0.02</td>
<td>50</td>
<td>1</td>
<td>0.1</td>
<td>150</td>
</tr>
<tr>
<td>B8</td>
<td>Au</td>
<td>15</td>
<td>0.02</td>
<td>20</td>
<td>1</td>
<td>1</td>
<td>400</td>
</tr>
<tr>
<td>B9</td>
<td>Al</td>
<td>90</td>
<td>0.04</td>
<td>20</td>
<td>1</td>
<td>0.1</td>
<td>400</td>
</tr>
<tr>
<td>B10</td>
<td>Al</td>
<td>15</td>
<td>0.02</td>
<td>50</td>
<td>1</td>
<td>0.1</td>
<td>400</td>
</tr>
<tr>
<td>B11</td>
<td>Al</td>
<td>15</td>
<td>0.04</td>
<td>50</td>
<td>1</td>
<td>1</td>
<td>150</td>
</tr>
<tr>
<td>B12</td>
<td>Al</td>
<td>90</td>
<td>0.02</td>
<td>20</td>
<td>1</td>
<td>1</td>
<td>150</td>
</tr>
<tr>
<td>B13</td>
<td>Al</td>
<td>15</td>
<td>0.04</td>
<td>20</td>
<td>5</td>
<td>0.1</td>
<td>150</td>
</tr>
<tr>
<td>B14</td>
<td>Al</td>
<td>90</td>
<td>0.04</td>
<td>50</td>
<td>5</td>
<td>1</td>
<td>400</td>
</tr>
<tr>
<td>B15</td>
<td>Al</td>
<td>90</td>
<td>0.02</td>
<td>50</td>
<td>5</td>
<td>0.1</td>
<td>150</td>
</tr>
<tr>
<td>B16</td>
<td>Al</td>
<td>15</td>
<td>0.02</td>
<td>20</td>
<td>5</td>
<td>1</td>
<td>400</td>
</tr>
</tbody>
</table>

The experimental matrix that was generated for these experiments is shown in Table 4-1. The parameters listed at the tops of the columns are two-level factors, meaning that only two different levels were considered while performing the experiments. The two-level parameter space considered is given in Table 4-2.
Table 4-2. Parameter space used in fractional factorial experiments. A high and low level value for each factor is listed.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Low</th>
<th>High</th>
</tr>
</thead>
<tbody>
<tr>
<td>Plasma Power (W/cm²)</td>
<td>0.02</td>
<td>0.04</td>
</tr>
<tr>
<td>SiH₄ Flow Rate (sccm)</td>
<td>20</td>
<td>50</td>
</tr>
<tr>
<td>Processing Pressure (torr)</td>
<td>0.1</td>
<td>1</td>
</tr>
<tr>
<td>Time (min)</td>
<td>15</td>
<td>90</td>
</tr>
<tr>
<td>Substrate Temperature (°C)</td>
<td>150</td>
<td>400</td>
</tr>
<tr>
<td>Metal Thickness (Al or Au) (nm)</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>Metal Type</td>
<td>Au</td>
<td>Al</td>
</tr>
</tbody>
</table>

Using these sets of two-level factors and depending upon whether Au or Al was used in an experiment naturally organized the results into two different regimes dependent upon the eutectic temperature of the metal/Si interface. For Au/Si the eutectic occurs at 363 °C whereas for Al the Al/Si eutectic occurs at 577°C. For temperatures below the eutectic value nanowire growth was assumed to have to grown through a VSS type mechanism, where as for temperatures above the eutectic temperature a more typical vapor-liquid-solid characteristic was expected. The vapor-liquid-solid method referred to the three phases present in wire nucleation, a gaseous precursor or vapor, liquid Au/Si droplet (or other metal), and a solid phase that precipitates out of the Au/Si droplet when saturated by the vapor phase.

All of the experiments performed with Al and 4 of the experiments performed with a Au catalyst were below the Si eutectic that is formed by that particular metal. SEM images of samples using a Au catalyst or Al catalyst are given and relative discussions are formed around these images. The main factors that were examined from the SEM images were density of the Si nanowires, the average wire diameters, the wire lengths, and percent coverage.
Figure 4-1 Plain view SEM images of four different experiments at 150°C. The image is divided according to what parameters the samples were produced with. RA stands for random artifact.

Figure 4-1 shows four different samples that were coated with either 1 nm or 5 nm of Au prior to being loaded into the deposition chamber. Sample B3 (Upper Left) had isolated bubble-like growths on the sample surface (bubbles, here, is used to describe the shape of the object and not its structural characteristic). These bubbles appeared to grow within the region of the sample that was coated with Au, but coverage was <1% of the total area of the sample with random
patterning. The bubbles all appeared to be < 1 μm in diameter but with a clustering effect that formed larger regions up to 2 μm in diameter. The areas of interest on the sample were too few and far between to obtain any kind of accurate analysis to determine if they were more amorphous in nature or some other composition. The Au thickness of this sample was 1 nm as determined by the in-situ crystal monitor of the thermal evaporator. It is unknown how consistent the 1 nm Au layer was on the sample, but it is possible that areas of the Au film either did not adhere well or were scratched off while transferring the samples from the evaporator to the PECVD tool. This would make sense if these isolated regions of Au were left on the sample and a growth process was initiated at these locations. If the Au/Si layer was 1 nm thick, but had been scratched during handling, then crystal terraces could have been exposed from which this growth may have begun to catalyze.

Sample B4 had similar looking bubble like structures, accept that these covered 100% of the growth area. The coverage of the bubble structures on the surface of the substrate gave an optical effect to the sample as having a silver appearance. The sample appeared to be less reflective than that of bare Si, but had a shimmering effect visually indicating scattering mechanisms. The individual bubbles were much smaller than those of sample B3 with an average diameter < 500 nm, but the clustering effects yielded structures much larger than 1 μm. An SEM image capturing the coverage of the bubbles on the sample surface is shown in Figure 4-2.
Figure 4-2. Si nano-bubbles formed on the surface of a Si substrate after exposure to a SiH$_4$ plasma for 15 minutes. Au thickness on the sample was 5 nm prior to annealing at 150 °C. Photograph shows the sample on the left compared to a bare Si sample on the right.

This formation of bubbles all over the sample surface was believed to be brought about in the same way through which silicon nanowires would be formed, although the processing conditions tended to form plump bubbles rather than elongated structures. The growth of these bubbles would have to have occurred through a VSS type mechanism, although the plasma could have affected the sample by locally heating regions of the substrate that might result in Au droplets forming and the nucleation of wire like structures. Towards the edge of the sample where a-Si:H deposition uniformity was less consistent more worm like structures were noted, even with some Au droplets located at the end as seen in Figure 4-3. The total volume of Au evaporated in a 5 nm layer over the 1 in.$^2$ substrate is equivalent to 3.23x10$^{-6}$ cm$^3$. Viewing Figure 4-3 10 to 11
Au droplets at the end of the worm structures are noted in the image. The total area over which these droplets is identified corresponds to a 4500 nm$^2$ area which, when assuming a half sphere geometry for each Au droplet, the average radius of a droplet ends up being 100 nm. This 100 nm radius is consistent with the radius of the droplets as identified from Figure 4-3. The total volume of Au evaporated onto the sample is 5x10$^{16}$ nm$^3$ which corresponds to enough Au to form 10 to 11 droplets for an area the size of Figure 4-3.

Figure 4-3. Worm like structures near edge of sample B4 where less a-Si deposition occurs. Less a-Si deposition occurs due to the non uniformity of deposition of the plasma. Gold droplets can be seen at the tips of the worm structures as indicated by the red circles.
These results suggested that Au thickness played a direct role into whether wires nucleated or not since those samples with 1 nm of Au showed almost no sign of structure growth. This conclusion was made based upon the fact that the other samples exposed to 150°C growth conditions did not create 100% coverage of growth structures on the sample surface. In addition, this sample was one where low plasma power was used with high pressure, indicating that pressure could be a driving factor in growth as well.

Sample B5 was the only sample out of all the sub-eutetic experiments with Au catalyst that produced wire structures. Again, only patches of wires were noted in < 1% of the sample area, which lead to the conclusion that plasma power was a driving factor as pressure was maintained at 0.1 torr and growth only occurred for 15 minutes. The Au thickness was kept constant between B5 and B4, which supported a conclusion that Au thickness was an important factor in nucleating wires.

Sample B7 in Figure 4-1 shows larger structures that seemed to form more square like rods than wires. These structures were discovered on <1% of the sample surface. No other growth was noted on the sample. This sparse structure population across the surface was typical of sample B3 and B5 that were coated with 1 nm of Au.
Experiments performed with an Al catalyst at 150°C. The layout of this image is similar to that of Figure 4-1 and features a grid-like structure that divides up the samples according to what parameters they were synthesized with. The blue frame around the SEM images indicates a 1 nm Al thickness and a SiH₄ flow rate of 50 sccm, while the red frame denotes 5 nm of Al and a 20 sccm SiH₄ flow rate.

The SEM images in Figure 4-4 show those experiments occurring at 150°C with an Al catalyst. All samples were left out in an atmospheric ambient, resulting in the probable oxidation of the Al catalyst. Thus, it was likely that the Al on the surface of the samples was part Al₂O₃, especially in the case of the 1 nm Al film. The 5 nm Al films might have been converted to Al₂O₃ partially.
with a layer of Al underneath the Al$_2$O$_3$. Unlike the Au catalyzed samples, little was seen in the way of wire growth with these samples. The eutectic temperature of Al and Si is at 577°C, which was nearly 3x greater than the temperatures at which these experiments took place. As a result, it was believed that the Al stayed in a solid phase and a-Si:H deposited on top of it during processing. Each sample is discussed pointing out relevant observations while noting any exceptions to the hypothesis that a-Si:H would coat the surface.

Sample B11 in the upper left corner of Figure 4-4 shows four nodules were observed on the surface of the substrate in the SEM image. These smallest of nodules were 250 nm in diameter whereas the largest nodule was 500 nm. The average size of the nodules was 312 nm. The surface of the sample was coated in a film of a-Si:H, which was observed by a fringe pattern occurring around the sample.

The upper right portion of Figure 4-4 shows the plain view SEM image of sample B12. More bubble like structures were noted to grow on this sample, but only minor patches existed across most of the surface totaling a coverage of < 1%. These bubbles differed from those that were observed in the Au catalyzed samples in that the surface was dimpled, somewhat like a golf ball, which is shown in Figure 4-5.
Figure 4-5. More magnified image of Figure 4-4 showing the dimpled surface that was observed with Al catalyzed samples. These structures only occurred in one region of the sample no large than 20 µm² in area making it difficult to both find and probe for more information.

Sample B13 shown in the lower left portion of Figure 4-4 had a resemblance to Sample B11. The features pictured in Figure 4-4 resemble surface impurities and therefore were not attributed to the deposition conditions. The structures on the surface of Sample B13 in Figure 4-4 were experimentally noted to have occurred on some samples prior to processing. This surface impurity was a result of impurities such as dust in the air that might have landed on the sample surface, after processing, but before characterization. B13 was another sample in which a-Si coated the surface as shown in Figure 4-6.
This shows the transition region between the c-Si substrate and the a-Si:H that was deposited on the substrate surface. The transition region existed because the substrate holder used in the PECVD chamber featured a metal lip which the sample rested against, producing an area where deposition did not occur.

Figure 4-7 shows samples that were catalyzed with Al of varying thickness at 400°C. This temperature remained below the Al/Si eutectic of 577°C. If wires were to grow in this regime it would have been cause by the plasma activation of the Al film since, the Al was not in a liquid state. Additionally, at the Al/Si eutectic less Si (<2%) diffused into Al at 400°C with the Al and Si remaining in solid phases. Therefore, any growth occurring in this temperature regime was most likely through a Vapor-Solid-Solid process rather than the Vapor-Liquid-Solid process that dominates above eutectic temperatures.
Figure 4-7. Al catalyzed samples that were grown at 400°C. The thickness of the Al catalyst and flow rate of SiH₄ is indicated by the colored frame around each of the SEM images. Other processing parameters are denoted by the grid. The ‘X’ located in the cell for sample B14 represents the fact that machine error invalidated Sample B14.

Sample B10 (lower left of Figure 4-7) shows an SEM image taken after synthesis. Total coverage of <5 % was noted on the sample where the normal appearance of the Si surface had that shown in Figure 4-8. This was an indication of either interaction between Al and Si or Al₂O₃ and Si. Figure 4-8 shows a close up image of one of the regions which seemed to show
discontinuities in the surface that appeared somewhat fractal in nature, indicating possible crystalline type growth.

![Image](image_url)

**Figure 4-8.** Close up image of surface disturbance that was observed across surface of Sample B10. The regions appear to have platelet like appearances and seem to show evidence of growth through the fractal like appearance of the platelets.

Other areas (<1%) on the sample surface of B10 showed regions where the structures in Figure 4-8 appeared in the wake of objects that seemed to have migrated across the surface during growth. This migration behavior is shown in Figure 4-9. The word migration here is used to describe the observation as it appeared in the SEM image, though it was not felt that the particle actually moved across the sample surface during processing.
Figure 4.9. SEM image showing platelet like objects that appear in the wake of larger particle.

Sample B9 had various locations across the surface of the sample that showed patches of wire growth. The wires appeared small in diameter (average of 117 nm) and long in length (average of 2.4 µm) and tended to cluster together. This indicated a possible Al grain boundary where Si might have diffused during processing, thus creating a template for growth. Figure 4-10 shows more examples of the wire growth that was observed on sample B9.
Another instance of wire growth that was located on sample B9. These regions occurred on < 5% of the total area of the sample and always were in clustered regions such as shown in the large image. The smaller image to the lower left of the large image is magnified showing that many wires existed within the region but no order was apparent.

The wires in Figure 4-10 had lengths of 2 µm and diameters of about 20 nm, but the sparsity of the wires across the sample as well as the fact that they are entangled with each other prevents them from being of use. This also prevented further characterization as it was difficult to locate this region on the sample using conventional tools. An interesting discovery was made with sample B9, however, in that it was found that multiple types of growth seemed to coexist on the same substrate as shown in Figure 4-11.
Figure 4-11. SEM images of locations on sample B9 that show different types of growth on the same substrate. These structures appear to be more nodule like (left) and more worm like (right). These kind of structures occurred in < 5% on the surface of the sample, but might exist due to a difference in the Al/Si interaction on the substrate.

Again the occurrence of these growth structures was rare, but one can see worm-like structures in the image on the right of Figure 4-11. These worm-like structures gave an indication that some wire synthesis had begun to occur, as this same growth behavior was noted on samples that produced wire growth.

Those samples that were processed above the eutectic temperature included different experiments from the Au catalyzed batch. The significance of these samples was that the processing temperature occurred at a point at which the Au film and Si substrate formed a eutectic, leading to liquid alloy droplets on the surface if left for an extended period of time. The type of growth occurring in this temperature regime was that of VLS. This growth method was quite prolific at producing wires, especially with a Au catalyst, mainly due to the rich Si/Au alloy that was formed. Once more Si was added to the alloy via the gaseous precursor, then the droplet tended to become supersaturated and must get rid of the extra silicon somehow, usually
through wire growth. Figure 4-12 shows SEM images of the 4 samples that were processed at a temperatures above the eutectic of Au/Si.

**Figure 4-12.** SEM images of Au catalyzed samples that were processed at 400°C which is above the Au/Si eutectic. The colored frames around images correspond to the colored text.

Figure 4-12 shows all of the Au catalyzed samples that were processed above the Au/Si eutectic temperature of 363°C where 69% Au and 21% Si by atomic composition exist in a liquid alloy. Each sample is individually analyzed to give in depth discussion about what was observed.
Where prolific wire growth was observed, TEM results are presented that show crystallinity of the as grown wires. As compared to other samples thus presented, being above the eutectic temperature seems to be of great benefit in obtaining wire growth.

Sample B1 in the upper right portion of Figure 4-12 showed that several small structures existed across the surface. Upon closer examination, such as that in Figure 4-13, small clusters that resembled structures seen on other samples, but these differed in that wires stuck out from the clusters.

![Figure 4-13](image)

*Figure 4-13* Closer examination of the surface of Sample B1 after processing.

The first interesting thing noted about the surface of Sample B1 was the clusters from which the wires protruded. The wires were all short with low aspect ratios and nucleated out of discontinuities present on the sample surface. The grainy background image revealed Au droplets on the surface of the sample. These clusters resembled clusters from other samples, most notably those of Samples B9 and B5. From these clusters wires protruded outward from the surface and random angles. The Au droplets from which the wires nucleate are observed to be at the tip as indicated in the image on the left of Figure 4-13. The wires were < 1 µm in
length and 30 nm in diameter, and some possessed kinks that indicated a change in growth conditions. There was some amount of experimental error in this sample because the SiH$_4$ was intermittently shut off to the chamber, extinguishing the plasma. This was probably the reason why the kinks were related to a change in growth condition. The grainy background image of Figure 4-13 shows Au droplets that had formed on top of the Si substrate.

Sample B2 shows Au diamonds that formed on the surface of the $<111>$ Si substrate sample after processing. It was concluded from this sample that wires did not nucleate due to insufficient plasma power, as the only difference between B2 and B1 was a lower plasma power and time.

Sample B8 shows the growth structure of straight Si nanowires that stood at angles ($35^\circ$ from vertical) to the substrate on which they grow. Wires nucleated from clusters of Au/Si droplets as shown in Figure 4-14. The straight wires on this sample showed a deviation from normal of 10 to $15^\circ$ in reference to the substrate surface. Wires tapered but had uniform diameters of 10 to 50 nm with a length on the order of 2-5 µm. Some wires appeared shorter than others, just barely nucleating from the cluster and being no more than 100 nm long but with the same diameter as the larger wires.
Figure 4-14. Close up look at clusters from which the Si nanowires of sample B8 grow. Multiple wires are noted immerging from each cluster and appear to do at random. Photograph shows the nanowires as grown on Si substrate. Nanowire film is on left, bare c-Si surface is on the right.

Interesting structures were noted at the tops of the vertical wires as seen in Figure 4-15. These structures appeared to adopt a diameter similar in size to the wire itself but had a worm-like random growth aspect.
This growth was ascribed to the fact that ending an experiment was not an abrupt process; temperature was reduced slowly, plasma was abruptly shut off, and the flow rate diminished at a slow rate.

Sample B6 showed a thick carpet of nanowires that had nucleated from the substrate surface. The wire growth occurred everywhere on the substrate where a Au film had been deposited and growth abruptly stopped where the Au film was terminated. The lack of wire growth where the Au had not been deposited supported the idea that Au acts as a driving catalyst for the growth of the wire. Self nucleation of the wires from the bare substrate was not likely, as typical a-Si:H deposition occurred in a normal PECVD process under these conditions.

Towards the edges of the sample, the wires tended to become much thicker and showed drastic changes in growth direction as the wire itself grew. This behavior was best exemplified as shown in Figure 4-16.
These structures might have formed as a reduction in the amount of available SiH$_4$ towards the edges of the samples due to nutrient depletion of the gaseous species. This sort of non-uniformity is common with PECVD samples towards the edges of a sample. Less available amounts of Si could have acted to slow down the diffusive process, increasing the amount of time needed for a Au/Si eutectic particle to begin precipitating out crystalline silicon at the droplet/substrate interface. The longer it takes for the particle to nucleate, the larger the eutectic particle can grow due to Ostwald ripening. The larger diameter particle could have created different growth physics due to geometrical relationships.

The general population of nanowires on the sample surface all appeared to have similar characteristics upon examining the SEM image. Figure 4-17 shows the ribbed surface of the nanowire and also shows how the wire intersects another. This sample featured nanowires with roughened surfaces covered in ribbed structures. The wire shown in Figure 4-17 appears to be intersecting another wire. This was due to one wire growing into another wire or by the secondary electrons in the SEM transmitting through the wire and creating a false image. If the secondary electrons generated a false image by transmitting through the nanowire, it would be
expected that all crossings in Figure 4-17 would show this property. Since this is not evident in other portions of the image, it is concluded that the intersection of the nanowires occurred because of the close proximity of one nanowire to the other.

![Figure 4-17. Nanowire grown on sample B6.](image)

If one imagines a crystal growing straight from the surface, one would think that it would be a solid column of crystal perpendicular to the substrate surface. In this case, the ribbed structures appeared. In a PECVD process, if a crystal were growing into a nanowire that was perfectly vertical one would also expect deposition of a-Si:H on the wire as the wire grows. In this case, a smooth structure would still be expected. Using this logic, it was hypothesized that the ribbed structures appeared because of an underlying structure beneath some a-Si:H deposition that had coated the wire. This could be thought of as analogous to snowfall onto an area of land with hills and valleys, the profile of the land is preserved as the snow coats the land, much the same way as the profile of the underlying crystal was preserved in this case.

It was noted that in some instances that wires grew in clusters together, sprouting out similar to a bush as shown in Figure 4-18.
Prior to processing it was difficult to determine exactly how these bushes nucleated, but thinking in terms of the VLS process gave some idea. If one had a hole in the Au film that was large enough so that when the Au film was annealed then a ring of eutectic droplets would be created. If the distance between the eutectic droplets was such that Ostwald ripening would cause them to merge together, it would be possible to obtain this bush like growth.

The results presented in this section were the results obtained from the initial exploration of nanowire growth to obtain information about which parameters had the greatest impact on silicon nanowire growth. The following sections show the growth of nanowires on different
substrates, notably glass, and provide some TEM analysis indicating crystallinity of grown wires as well as geometrical relationships between wire length and diameter.

Silicon nanowires grown on different substrates will yield different results due to the properties of the metal/substrate interface. This was best exemplified, in this work, by examining the difference in observations made from wires grown on different substrates. In this experimentation, wires were nucleated on <111> and <100> type Si as well as on Corning 1759 glass. SEM images are used to show the relevant differences between results and explanations are given accordingly. TEM images of individual silicon nanowires grown on <111> and <100> type Si substrates are shown and some in depth analysis of wire length, diameter, and crystallinity is given as determined by basic image processing.

Figure 4-19 shows the difference in wire morphology between Si nanowires grown on a <100> Si substrate and a <111> Si substrate. Wires appear long with tens of micron size lengths and nanometer size diameters.

![Figure 4-19](image)

*Figure 4-19* (Left) SEM image of silicon nanowires grown on a <100> Si substrate. (Right) SEM image of silicon nanowires grown on a <111> Si substrate. Both samples used the parameters the same as sample B6.
All wires tapered to a sharp tip that was 25 times smaller than the average diameter of the wire. This tapering effect was most probably a result of the consumption of Au either by the wire or by the plasma. The tapering was also attributed to the thickening of the as-grown nanowires through a-Si:H deposition. Wires did not have any preferred growth direction and grew at random. The Si nanowires had a smooth radius of curvature to them. This is felt to be a result of stress-strain relationships of the material interfaces that existed within the wires as they grow.

Figure 4-20 shows the results of Si wires grown on a Si substrate and a Corning 1737 substrate. Processing occurred for only 10 minutes, and as a result a drastic change in wire morphology is noted. The difference in the wire growth can be attributed to the Au/substrate interface. Dramatic differences in wire morphologies exist as a result of the absence of Si in the formation of eutectic droplets on the 1737 substrate.

Figure 4-20. (Left) SEM image of silicon nanowires synthesized on a <111> Si substrate with growth time of 10 minutes. (Right) SEM image of Si nanowires grown on Corning 1737 substrate in same process. Parameters for growth are the same as Sample B6 except time was limited to 10 minutes.
Wires that were nucleated on the Si substrate came from a Si rich particle. This occurred because the Au film was annealed, forming eutectic droplets on the substrate. The glass substrate also created droplets on the surface, but they were expected to be less Si rich as the underlying substrate is composed of both Si and oxygen. Oxygen might have also played a role in the creation of droplets on the glass surface with annealing. This had the effect of producing fattened “nanowire” structures, such as those shown in Figure 4-21. Interestingly, greater than 3 \( \mu \)m long wires also coexisted with the short fat wires with lengths and diameters of about 250 nm. This can best be related to the size of the particle before growth occurs. A smaller particle would take less time to become saturated with Si and thus a wire would be synthesized more quickly. A larger particle would take a longer time to become saturated with Si. It is conjectured that a difference in particle size created two different regimes of growth on the same substrate.

![Figure 4-21](image)

**Figure 4-21.** Same Si nanowires that are shown in Figure 4-20 but with higher magnification. The left image is on <111> Si and the right image is on glass.

Closer inspection of both substrates showed that a layer existed beneath the longer structures on the substrate where shorter structures were noted to grow. The substrate seems covered by both
thin wire growth and thicker worm like wire growth, where as the Si substrate features straight and stocky wire structures with defined spherical heads. Large particles could also have resulted in a slower growth rate, which would have created shorter wires. Nutrient depletion could also have contributed to the growth rate. These wires grew close to the substrate, contributing to the difficulty in imaging the wires due to depth of focus.

Another experiment was performed along with Sample B8 from the fractional factorial experiments. A glass sample with 5 nm of Au was placed in the processing chamber along with Sample B8 which had only 1 nm of Au. Figure 4-22 shows a side-by-side comparison of the wires grown with these parameters. Wire diameters on the 1737 substrate had a diameter of 50-60 nm and those on the Si substrate also fell in this range.

Figure 4-22. Side by side comparison of sample B8 grown at the same time. The Corning 1737 sample is on the right and was grown using a Au thickness of 5 nm. The <111> Si substrate on the left was grown using a 1nm Au thickness.

Some of the wires on the Si substrate were nearly vertical with angles of growth varying by only 20° from normal while others appeared flat. The wires grown on the glass substrate showed a
random growth pattern, which was attributed to the thicker layer of Au used to nucleate the wires.

The 1737 sample shown in Figure 4-22 had Au only selectively deposited on some regions of the sample. This was done by patterning the substrate using Kapton tape prior to Au deposition. This left strips of Au across the glass surface after metal evaporation. Figure 4-23 shows a SEM image of the selective growth of nanowires on certain areas of the glass substrate.

![Figure 4-23. Band of a-Si:H deposited between two films of silicon nanowires on one substrate.](image)

Where Au was not evaporated on the glass surface a-Si:H film was deposited, whereas where Au was evaporated on the glass surface wires grew. This result demonstrated the ability of being able to selectively define areas where the nanowires can be grown. This type of selective growth could be useful to the creation of devices.
4.2 TEM Analysis of Individual Silicon Nanowires

Those samples where prolific silicon nanowire growth was obtained were used to collect individual silicon nanowire samples on TEM grids for more thorough analysis of the nanowires. All nanowires shown in the section were grown at 400°C for 90 minutes at a pressure of 1 torr. Individual nanowires from <100> and <111> Si growth substrates were analyzed for crystallographic composition by examining the distance between crystal planes and by SAD analysis.

Figure 4-24. TEM image of two single silicon nanowires that were extracted from their respective growth substrates. On the left is a nanowire extracted from a <100> growth substrate and on the right one that was extracted from a <111> substrate.

Figure 4-24 shows TEM images of a single Si nanowire extracted from a <100> substrate and from a <111> substrate. Detailed analysis of the image reveals the wire diameter of 130 ± 11 nm
for the <100> wire and 127 ± 8 nm for the <111> silicon nanowire. The silicon nanowires were grown using the same processing conditions and at the same time. The similarity in the diameters was thus expected. The length of each wire as given in the photo is only a partial length of the nanowire. This is because the nanowires were extracted from the growth substrate in a mechanical manner that led to the breaking of the nanowires into pieces. Figure 4-25 shows a magnified image of the <111> grown Si nanowire. A distinct region of crystal planes in the upper portion of the enlarged inset was observed.

**Figure 4-25.** The TEM image on the left shows a magnified view of the silicon nanowire grown on the <111> substrate in Figure 4-24. The image on the right shows crystal planes as denoted by the red two-way arrow. The blue two-way arrows show an area that is thought to be a native oxide.

The rest of the wire appeared to be amorphous with a different looking material composition toward the edge. The discoloration of the wire surface in this TEM image is due to electron diffraction indicating crystalline properties. The diffraction patterns obtained show wavelike patterns in the TEM image of the Si nanowire because of the collective interference produced by
multiple electron scattering upon impact with the nanowire. The smooth regions without the disordered appearance indicate amorphous material because the short range order of an amorphous solid does not produce the same type of interference that was produced by the electrons striking crystalline material. The region toward the edge appears amorphous from this perspective and can be reasoned to be SiO₂. From the TEM image the thickness of this a-Si region near the edge was 3.45 ± 0.45 nm which was consistent with a native oxide thickness. A self passivating native film layer grown on a Si substrate at room temperatures often has a thickness of 2 to 3 nm. This layer could have been formed because the nanowire sample was exposed to atmospheric conditions and one would naturally conjecture that the surface of the wire must be oxidized. Figure 4-26 shows the end of the wire that was shown in Figure 4-25.

![Image](image_url)

**Figure 4-26.** Same nanowire as that shown in Figure 4-25, but the focus is on the end of the wire where it was mechanically cleaved from the substrate or a longer piece of nanowire. The inset shows a diffraction pattern taken on the wire in this region.
Upon magnifying the image it was noticed that the same row of crystal planes that existed within the center of the wire (as denoted by the red two-way arrow in Figure 4-26 and Figure 4-25). The red two-way arrow denoted a distance of 16 nm which covered 16 rows of atoms. This gave the distance between the atom spacings as 10 Å, which is indicative of a lattice fault as this is larger than the distance between different crystal plane directions in Si. The inset diffraction image showed rings and points that indicate both c-Si material and a-Si:H material together in the nanowire. The appearance of a-Si was consistent with the growth method, as the PECVD created SiH₄ radicals that constantly coated the sidewalls of the wire as it grew. The theory of the growth process in section 2.1.3 gives reasoning as to why both crystalline and a-Si:H material existed in the nanowire structures.

Figure 4-27 shows TEM images of a single Si nanowire that were mechanically extracted from a <100> oriented Si growth substrate.
One notices that the wire had distinct crystal planes visible. The red two-way arrow denotes these planes, and the shorter yellow two-way arrow gives the distance of 10 atomic planes of atoms. This distance of 3.14 nm over 10 planes was equivalent to 3.14 Å plan to plane spacing, identifying these crystal planes as the <111> direction. By comparing the <111> planes to the direction at which the wire grew yielded the probable growth direction. The angle measured between the growth direction and the <111> plane was 31.9°, which was close to the 35.3° angle between <111> and <110> planes in c-Si. Using this logic, the growth direction was thought to be <110> which meant that the wire grew at an angle of 45° from the growth substrate (as this is the angle between the <110> and <100> planes in c-Si). However, it was noted that this section of nanowire was only an extracted piece. As such, the same stress-strain relationship was not applied to this nanowire so that the growth direction that is documented here may actually be an
apparent growth direction and not a true growth direction. The Si nanowires shown in Figures 4-24 through 4-27 were all Si nanowires extracted from Sample B6 growth conditions. SEM images of these wires attached to the growth substrate are shown in Figure 4-19. Because of the dense random growth that the nanowires assumed, it was difficult to make a decision about the true angle at which the Si nanowire grew relative to the substrate surface. This is why an apparent growth direction will be assumed here.

Figure 4-28 shows another image of a Si nanowire from the same growth substrate with \( <111> \), \( <100> \), and \( <110> \) planes identified. The triangles formed from the yellow and green lines in the image corresponded to a face of the pyramid formed by the \( <111> \) and \( <100> \) planes. The angles in the pyramid faces corresponded to the correct geometrical relationships for \( <111> \) and \( <100> \) planes. The \( <110> \) planes were also identified in the lower region of the image as denoted by the red lines. The distance of 10 atomic planes in the image corresponded to 1.9 nm which indicated a distance of 1.9 Å between adjacent crystal planes, consistent with the distance between \( <110> \) planes. The schematic inset of the image shows four crystal unit cells with the yellow lines representing sidewalls of the \( <111> <100> \) pyramid and the green lines representing the \( <100> \) base. The red lines that are included in the schematic show the \( <110> \) planes in relation to the crystal pyramids. The growth direction of the wire was determined to be \( <100> \) by examining the orthogonality between \( <100> \) planes of the pyramids and the \([100]\) direction denoted by the black arrow.
Figure 4-28. TEM image of Si nanowire grown on <100> substrate. The crystal planes that are identified in this image are labeled in the image. The blue land red lines show a distance of 10 atomic planes with the distance given in the image. The blue corresponds to <111> planes and the red <110> planes. The schematic in the lower right indicates the crystal planes in relation to a cubic unit cell. The yellow triangles show a side of the pyramid formed by the <111> and <100> planes, which is depicted in the schematic in the lower right of the image.
The tips of the silicon nanowires are a site where it was expected that Au contamination would be at its greatest. Selected Area Diffraction (SAD) images are provided in Figure 4-29 that show diffraction patterns from three different portions of a silicon nanowire extracted from a <100> substrate. Figure 4-29 also depicts the section of the wire from which the SAD was collected and a view of the wire indicating the partial length. The SAD image of the tip in Figure 4-29 showed additional crystalline points that were indicative of crystalline planes of Au intermixed with Si, as this diffraction image differed from those taken from the body of the wire.

**Figure 4-29.** A silicon nanowire extracted from a <100> growth substrate that was analyzed for indication of Au contaminants at the wire tip. The SAD pattern show rings that indicate a-Si:H and dots typical of crystalline samples. Arrows indicate approximate regions where SAD data was gathered.
TEM images showed that the silicon nanowires grown on Si substrates were composed of both a-Si:H and c-Si as indicated by SAD images. Atomic crystal planes were identified in the nanowires coming from <100> substrates and it was shown that both <111> and <110> crystal planes were evident in the composition of the wire. Growth directions were hard to determine, but it appeared that nanowires grown on both <111> and <100> substrates grew in the <100> direction. This was determined to be an apparent direction because of the removal of substrate effects when the nanowires were extracted and placed on a TEM grid. Solid evidence of Au contamination in the tip of a Si nanowire was not evident. SAD images collected from the center of the nanowire differed from those collected at the tip, with more crystalline patterns appearing at the tip. All silicon nanowires analyzed by TEM analysis were grown using the parameters from sample B6.

4.3 Effect of Time on the Growth of Au Catalyzed Nanowires

Controlling the growth of Si nanowires via the PECVD process will ultimately result in the control of factors involved in Si nanowire synthesis. An experiment was performed to see the effect that time has on the growth of Si nanowires. One sample was processed for only 10 minutes, and the other sample was processed for 90 minutes. Figure 4-30 shows a side-by-side comparison of the effect that time has on the growth of Si nanowires at a given set of fixed parameters. Since the time was limited in the 10 minute run wire diameters were found to be 90 nm with wire lengths of 1 µm whereas those given 90 minutes to grow had diameters of 250 nm with lengths of 70 µm.
By comparing the lengths of the nanowires grown between the two samples depicted in Figure 4-30 it was determined that the growth rate for the 90 minute sample was 777 nm/min. while the 10 minute sample had a growth rate of about 1 µm/min. This result suggested that the growth rate of the nanowires was not linear. Wires in the 10 minute sample also seemed to have a more constant diameter, whereas those wires nucleated for 90 minutes have displayed tapering effect.

4.4 Optical Properties of Bulk Nanowire Films on Glass

This section presents the results of transmission data that was gathered from a nanowire film that was grown on a glass substrate. As opposed to individual nanowires that were shown in section 4.2, the transmission data presented is a collective property of the nanowire film. This type of characterization is significant as it demonstrates the viability of the nanowires for optical applications.
The optical effect produced from an array of synthesized Si nanowires was quite dramatic in reducing the reflection on the front of the Si surface. This is best shown by examining Figure 4-31, which shows an experimentally obtained transmission/reflection curve of the Si nanowire sample grown on a Corning 1737 substrate.

![Image of transmission/reflection curve](image)

**Figure 4-31.** Transmission curves of silicon nanowire film that was grown on glass. The schematic depicts that light was incident at normal and 30°. The brown layer on top of the blue layer represents the nanowire on glass structure. The SEM image shows a top down view of the nanowires appearance. The picture in the upper right of the figure shows a photograph of the Si nanowire film on glass.

A drastic reduction in transmission was seen over the entire UV/VIS range. Transmission was even minimized, as compared to a typical Si sample, into the near-IR range. The 90% reduction in transmission was an excellent indicator that the wires could be useful in a photovoltaic device. The spacing of the distance between the nanowires (<100 nm) was less than the wavelength of light, while the wires themselves varied in size from base to tip, with the base
being closer to the size of the wavelength of light in Si. Though no experimental or theoretical results have been used to determine the type of scattering events occurring, it was likely to be a combination of scattering events. Most prominently, the “porous” like nature created by the web of Si nanowires on the sample surface gave rise to Rayleigh scattering, whereas the interaction of the nanowires themselves with the light created more of a Mie scattering type event. Though these optical theories are typically applied to spherical objects, an extension of them could apply to the Si nanowires. This might have contributed to the dark coloration of the surface when the sample was viewed by the naked eye.

This section has presented optical transmission data that shows the nanowires minimized transmission of light from the 300 to 1400 nm range. This data supported the hypothesis that nanowires could be used in an optical application such as a photodetector or solar cell.
Chapter 5: Concluding Remarks and Future Work

This section summarizes the results obtained in this thesis and gives an indication of future work that is to occur.

5.1 Summary of Observations

Silicon nanowires were successfully nucleated on <111> and <100> oriented Si substrates and on Corning 1737 glass substrates using a Au catalyst. The ability to pattern the Si nanowire growth substrate was demonstrated on a glass substrate by a simple method, which could extend to more complex patterning techniques involving photolithography and electron beam lithography techniques. Vertical growth of nanowires was achieved, though perfectly perpendicular nanowires were not noted to grow on any samples. This suggests that more study is needed to determine which parameters drive vertical growth.

SEM images of all of the fractional factorial experiments were presented, with discussions explaining results where relevant. Si nano-bubble structures were obtained at low temperatures using a Au catalyst. The most relevant structures grown with an Al catalyst resembled clusters where sub-micron wire like structures nucleated. Dense arrays of silicon nanowires were nucleated on multiple substrates and in multiple deposition chambers at 400°C. Controllable wire length and diameter was demonstrated by reducing processing time. Main drivers of the growth were determined to be plasma power, pressure, and temperature. Au thickness was noted to have a connection to density of wire growth as the distribution and size of Au droplets determined the initial diameter of wire growth.
TEM images revealed that wires were made of a-Si:H and c-Si composition. Atomic planes of c-Si were identified on silicon nanowires grown on both <111> and <100> substrates, but wires from both substrates were determined to have a <100> growth direction. SAD images showed that both amorphous rings and crystalline points existed at different locations on the sample. Au contamination in the wires was not conclusive from SAD images, but it was likely that Au was contained within the nanowire, especially at the tip.

Optical transmission data supported that the nanowires collectively acted to reduce transmission of light over typical bulk based c-Si and a-Si films. In fact, transmission was noted to be under 10% even beyond the bandgap of c-Si, indicating that the silicon nanowires absorbed beyond the band gap of silicon, due to photonic effects of the nanowire array. This information led to the conclusion that the nanowires could be incorporated into a photovoltaic device, or at the very least, be used as an anti-reflection coating for optical devices.

5.2 Generalization of Growth Method

The results presented support evidence for the formation of a modeling framework from which the Si nanowires grow. The growth process can be divided into four different phases including sample preparation and annealing, nanowire nucleation, nanowire growth, and the end of experiment.
The sample preparation and annealing phase involves the steps needed to clean and apply a metal film to the substrate on which the Si nanowires are to be grown. The substrate can be any material whose thermal properties can withstand the temperature of fabrication. In this modeling proposal, both Si substrates and glass substrates will be considered as these substrates were used in this thesis work. The goal of the initial annealing phase is to create a distribution of droplets across the surface of the sample, from which nanowires can grow. Many different configurations of droplets could be formed and are depicted in Figure 5-1.

Particles could be controlled and ordered and made into different arrays (Figure 5-1 a), the particles could form droplets that vary in size and are randomly distributed (Figure 5-1 b), particles could be uniform in size and form a vacancy leading to bush-like wire nucleation (Figure 5-1 c), or the metal film could remain in a solid phase if experimentation takes place below the substrate/metal eutectic temperature (Figure 5-1 d). Phase 2 and 3 of the growth process is pictured in Figure 5-2.

**Figure 5-1.** Possible configurations of metal particle distribution after initial annealing before Si nanowire growth.
The purple cloud represents a nutrient supply from the plasma decomposing SiH$_4$ into different gas species. As the process time is extended, a crystalline Si nanowire begins to nucleation, having a vertical growth as in Figure 5-2 b. The nutrient supply at the top of the wire is greater than that at the bottom. This kind of nutrient depletion as the wire grows is typical of PECVD as deposition in trenches tends to occur in an anisotropic manner. With continued growth, a-Si:H deposition begins to form on the sidewalls of the nanowire with a-Si:H deposition also occurring on the substrate around the wire as depicted in Figure 5-2 c. Phase 3 of the growth comes near the end of the deposition process.

Figure 5-2. Schematic illustration of the growth of a single Si nanowire. The arrow at the bottom of the image indicates that growth time is increasing from left to right. The green color represents a-Si:H deposition. The purple clouds represent nutrient availability from the plasma, with the darker colors indicating more nutrient availability.
As the wire grows taller, nutrient depletion near the base of the wire becomes less, but that portion of the wire closer to the substrate has also been in existence longer, so more a-Si:H deposition is expected. This leads to the tapering effect that the Si nanowires are observed to have. Further, the depletion of nutrients versus growth time could lead to different growth modes as that shown in Figure 5-2 d.

In Figure 5-3 the silicon nanowire has been growing for sometime with the continued deposition of a-Si:H on the side of the nanowire. The tensile strain placed upon the growing Si nanowire will have the tendency to create a bend to the wire. When the wire bends the underside of the wire experiences less a-Si:H deposition, thus causing the nanowire to relax and continue to grow as originally had. But, with the wire curving back during growth, more a-Si:H deposition occurs.

Figure 5-3. A grown silicon nanowire is pictured in the SEM image that shows some amount of oscillation to the growth process causing the wire to grow spirally. The schematic at the left depicts how this type of growth mode might occur due to the tensile strain placed upon the growing wire by the a-Si:H.
which causes the wire to oscillate between growth modes. This type of behavior was observed on some samples as shown in the SEM image of Figure 5-3.

Phase 4 of the growth process is the termination of the experiment. Growth conditions do not all abruptly end. The plasma is immediately stopped when the deposition is ending, but gas flow rate and temperature both steadily decrease. This leads to non-uniformities in wire ends as the experiment comes to completion.

5.3 Where We Go From Here

More work is needed to determine what parameters control the exact aspects of nanowire growth. Further TEM analysis is needed to determine how the composition of the nanowires change in response to different growth characteristics. Advanced characterization techniques of silicon nanowires utilizing focused ion beam preparation to examine the cross section of the nanowires would be beneficial to further understanding the material properties. Raman spectroscopy of the wires would yield information concerning crystallinity and phononic confinement effects. Electronic characterization is necessary to determine both electronic confinement and electronic quality of nanowires for use in electronic applications such as high frequency transistors. Further processing work will yield information about how to synthesize nanowires with an Al catalyst as this would be technologically preferred. In addition, vertical growth of nanowires can be investigated.

The silicon nanowires can be used in applications ranging from transistors to solar cells. The intended use of the nanowires is in a Si based solar cell as the transmission results presented in this thesis lead one to believe that Si nanowires could have advantages when incorporated into a
solar cell. Future work might involve optimization of nanowire arrays for both superior electronic and optical properties for use in photovoltaic and electronic applications.
References


A new revolutionary way to create electronics at low temperatures without any expense has been developed, at the University of Arkansas Laboratory by Dr. Hameed Naseem and µEP M.S. student Matthew Young. This technology grows Si nanowires, tiny crystals that look and grow much like a thick lawn of grass and act to collect light with tremendous efficiency.

The inventor of the nanowires, Matthew Young, says “This method of nanowire growth allows us to make inexpensive electronics which should give us an edge in commercializing the technology and establishing high-tech businesses that would bring much needed jobs to Northwest Arkansas”. Young was also quick to point out that none of this would have been possible without the funding provided by the citizens of the state. With more support from the public who knows what could come out next? Cancer could be cured, foreign dependency on oil would be removed, and the best televisions could be manufactured. With further development new solar cell and other electronic technology could come out that could allow everyone to generate power from the sun and use tablets that think for you, so that you no longer have to decide which bird to throw at a pile of rocks and some pigs.
Appendix B: Executive Summary of Newly Created Intellectual Property

The following items were developed during the performance of creating this thesis and should be considered for both intellectual property and commercialization interest:

1.) Method to create nano structures in a composite material at low temperatures. The composite material is a combination of c-Si nanowires embedded in an a-Si:H matrix.

2.) Method to create large and small aspect ratio silicon nanowires for technological applications.

3.) A new material and device made of a nano-composite material that combines the optical and electronic properties of amorphous silicon and crystalline silicon for the creation of highly absorbing solar cells.
Appendix C: Potential Patent and Commercialization Aspects of listed Intellectual Property Items

C.1 Patentability of Intellectual Property

1. The growth method used to fabricate the Si nanowires could be patented in this application.

2. The ability to have control over fabricating large and small aspect ratio nanowires could also be patented. Though other technologies exist, it is not clear as to how easily they can produce such a wide range of nanowire structures.

3. A nano-composite material using the nanowires as a crystalline/amorphous interface for advanced collection of light in novel solar cell designs could also be patented.

C.2 Commercialization Prospects

The three items listed were then considered from the perspective of whether or not the item should be patented.

1. The creation of Si nanowires by PECVD should definitely be patented. PECVD can produce the nanowires at low temperatures and is readily scalable to manufacturing. PECVD lines also exist in many commercial integrated circuit fabrication houses, so it is a technology that could be adopted by an existing company.

2. The diversity of nanowires grown in the experiments that embody this thesis research vary extensively. While it is not known whether exact control over specific wire morphologies could be obtained, it would be an attractive piece of IP that one would like to secure.
3. The idea of a nano-composite material for superior performance in a photovoltaic device should be patented with absolute certainty. In fact, a patent disclosure for this technology has been filed and has high probability of being adopted by a currently existing company (Silicon Solar Solutions).

**C.3 Possible Prior Disclosure of IP**

The following items were discussed in a public forum or have published information that could impact the patentability of the listed IP.

1. The growth of the Si nanowires by PECVD has been featured in a publication that PVSC 38 that is scheduled to occur June 3-8, 2012 in Austin, TX. Other forums where information has been publically disclosed feature research group meetings over the past 1.5 years.

2. The development of nanostructures via PECVD has never been publically disclosed.

3. A nano-composite material featuring the as grown Si nanowires has been disclosed in the past and this information is included in the formal disclosure that has been issued for the technology.
Appendix D: Broader Impact of Research

D.1 Applicability of Research Methods to Other Problems

While investigating the growth of Si nanowires it was determined that the Si nanowires themselves could be used in a variety of applications. The nanowires could find probable uses in sensor based devices, transistors, and energy conversion devices. The method used to grow the wires also can be used to study the growth of crystals and binary material systems. Many different aspects of material science could be explored using the growth method used to grow Si nanowires. New modeling platforms could also be created which would produce discoveries in scientific computation.

D.2 Impact of Research Results on U.S. and Global Society

The direct results of this thesis have not directly impacted the global society as of yet. One major impact on the U.S. or the global society comes from the applications that the as-grown Si nanowires could be used for. A low cost photovoltaic solution that could compete with current electrical fuel sources would have dramatic impact on society. For one it would free dependence on any other country in the world, de-coupling a world economy to extent. The de-coupling such an economy would reduce possibilities of global depressions, that could occur given the state of connectivity. Transistor applications could act to produce new devices with abilities to the end consumer that were previously not possible. One such instance is the real time processing of information without the need to first gather data and then seek out computational methods from which to interpret something.
D.3 Impact of Research Results on the Environment

Creation of Si nanowires through gas phase deposition is a more environmentally friendly process than other methods used to produce Si based electronics. The use of Si, itself, is environmentally friendly as the source material is abundant and it is innocuous to the biology of the human body. The PECVD tool used to create the nanowires in this experiment does require electricity to power various aspects of the machine. This electricity of course comes from another method such as coal that pollutes the air. If the nanowires were used to create solar cells that could produce enough energy to fuel the process of Si nanowire growth, then the process could be viewed as clean and environmentally friendly.
## Appendix E: Microsoft Project for MS MicroEP Degree Plan

<table>
<thead>
<tr>
<th>Task Name</th>
<th>2010</th>
<th>2011</th>
<th>2012</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Qtr 1</td>
<td>Qtr 2</td>
<td>Qtr 3</td>
</tr>
<tr>
<td>Graduate School Events</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Master's Program Advisory Committee</td>
<td>5/16</td>
<td>4/23</td>
<td>4/23</td>
</tr>
<tr>
<td>Thesis Registration 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thesis Registration 2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Preliminary Copies</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Final Copies</td>
<td></td>
<td></td>
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<tr>
<td>Master's Examination</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Graduation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Application for the Degree</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Defining Research Topic</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Research Document Rev. 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Project File Rev. 0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Research Document Rev. 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Project File Rev. 1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Research Document Rev. 2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Project File Rev. 2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Research Document Rev. 3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Project File Rev. 3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Research Document Rev. 4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Project File Rev. 4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Research Document Rev. 5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Project File Rev. 5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Research Document Rev. 6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Project File Rev. 6</td>
<td></td>
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</tbody>
</table>
Appendix F: Identification of All Software Used in Research and Thesis/Dissertation

Generation

Computer #1:
- Model Number: Dell Precision M4400
- Serial Number: GXTGPJ1
- Location: Personal Computer
- Owner: Matthew G. Young

Software #1:
- Name: Microsoft Office 2007
- Purchased by: Matthew G. Young

Software #2:
- Name: Microsoft Powerpoint 2007
- Purchased by: Matthew G. Young

Software #3:
- Name: GIMP
  - Open Source: Matthew G. Young

Software #4:
- Name: JMP 9
  - Purchase by: Matthew G. Young

Software #5:
- Name: ImageJ
  - Open Source: Matthew G. Young
Appendix G: All Publications Published, Submitted and Planned

Young, M.G., Benamara, M., Abu-Safe H., Yu F., Naseem, H. A., “a-Si:H/c-Si Nanocomposite Material for Solar Cells Fabricated from PECVD”, PVSC 38, 2012, Austin, TX. (Submitted and Accepted)

Young, M.G., Abu-safe H., Naseem, H. A. “Comparison of Au and Al catalysts for Si nanowires grown by PECVD”, Nanotechnology. (Planned)